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Mixed-Signal Front-End (MxFE™) Baseband Transceiver for Broadband Applications

Data Sheet **AD9861**

FEATURES

- Receive path includes dual 10-bit analog-to-digital converters with internal or external reference, 50 MSPS and 80 MSPS versions
- Transmit path includes dual 10-bit, 200 MSPS digital-to-analog converters with 1×, 2×, or 4× interpolation and programmable gain control
- Internal clock distribution block includes a programmable phase-locked loop and timing generation circuitry, allowing single-reference clock operation
- 20-pin flexible I/O data interface allows various interleaved or noninterleaved data transfers in half-duplex mode and interleaved data transfers in full-duplex mode
- Configurable through register programmability or optionally limited programmability through mode pins
- Independent Rx and Tx power-down control pins
- 64-lead LFCSP package (9 mm × 9 mm footprint)
- 3 configurable auxiliary converter pins

APPLICATIONS

- Broadband access
- Broadband LAN
- Communications (modems)

FUNCTIONAL BLOCK DIAGRAM

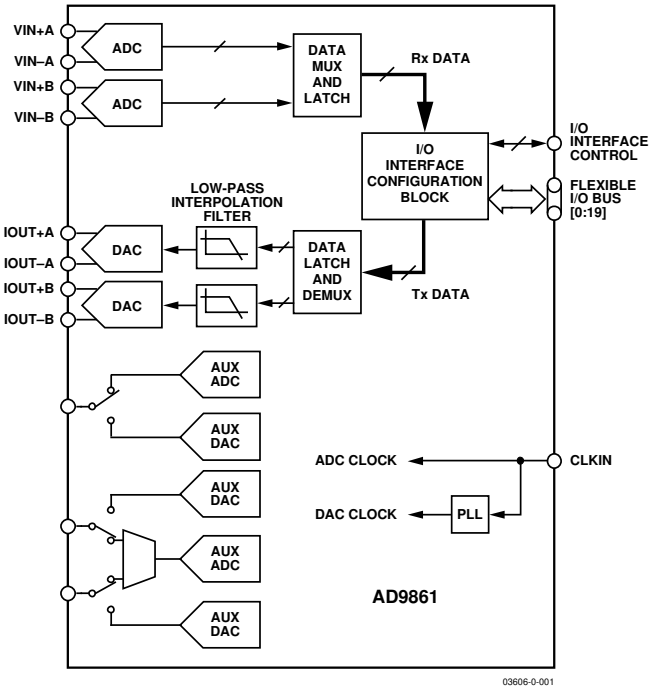

Figure 1.

GENERAL DESCRIPTION

The AD9861 is a member of the MxFE family—a group of integrated converters for the communications market. The AD9861 integrates dual 10-bit analog-to-digital converters (ADC) and dual 10-bit digital-to-analog converters (TxDAC®). Two speed grades are available, -50 and -80. The -50 is optimized for ADC sampling of 50 MSPS and less, while the -80 is optimized for ADC sample rates between 50 MSPS and 80 MSPS. The dual TxDACs operate at speeds up to 200 MHz and include a bypassable 2× or 4× interpolation filter. Three auxiliary converters are also available to provide required system level control voltages or to monitor system signals. The AD9861 is optimized for high performance, low power, small form factor, and to provide a cost-effective solution for the broadband communication market.

The AD9861 uses a single input clock pin (CLKIN) to generate all system clocks. The ADC and TxDAC clocks are generated within a timing generation block that provides user programmable options such as divide circuits, PLL multipliers, and switches.

A flexible, bidirectional 20-bit I/O bus accommodates a variety of custom digital back ends or open market DSPs.

In half-duplex systems, the interface supports 20-bit parallel transfers or 10-bit interleaved transfers. In full-duplex systems, the interface supports an interleaved 10-bit ADC bus and an interleaved 10-bit TxDAC bus. The flexible I/O bus reduces pin count and, therefore, reduces the required package size on the AD9861 and the device to which it connects.

The AD9861 can use either mode pins or a serial programmable interface (SPI) to configure the interface bus, operate the ADC in a low power mode, configure the TxDAC interpolation rate, and control ADC and TxDAC power-down. The SPI provides more programmable options for both the TxDAC path (for example, coarse and fine gain control and offset control for channel matching) and the ADC path (for example, the internal duty cycle stabilizer, and twos complement data format).

The AD9861 is packaged in a 64-lead LFCSP (low profile, fine pitched, chip scale package). The 64-lead LFCSP footprint is only 9 mm × 9 mm, and is less than 0.9 mm high, fitting into tightly spaced applications such as PCMCIA cards.

Rev. A Document Feedback

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AD9861* PRODUCT PAGE QUICK LINKS

Last Content Update: 04/29/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9861/AD9863 Evaluation Tools

DOCUMENTATION

Application Notes

- AN-928: Understanding High Speed DAC Testing and Evaluation

Data Sheet

- AD9861: Mixed-Signal Front-End (MxFE™) Processor For Broadband Applications Data Sheet

TOOLS AND SIMULATIONS

- AD9861 IBIS Models

REFERENCE MATERIALS

Informational

- Advantiv™ Advanced TV Solutions

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9861 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9861 EngineerZone Discussions.

SAMPLE AND BUY

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Submit a technical question or find your regional support number.

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REVISION HISTORY

4/2017—Rev. 0 to Rev. A

Changes to Figure 3 and Table 8 8
Updated Outline Dimensions 44
Changes to Ordering Guide 44

11/2003—Revision 0: Initial Version

TX PATH SPECIFICATIONS

Table 1. AD9861-50 and AD9861-80
F_{DAC} = 200 MSPS; 4× interpolation; R_{SET} = 4.02 kΩ; differential load resistance of 100 Ω[1]; TxPGA = 20 dB, AVDD = DVDD = 3.3 V, unless otherwise noted

Parameter	Temp	Test Level	Min	Typ	Max	Unit
Tx PATH GENERAL						
Resolution	Full	IV		10		Bits
Maximum DAC Update Rate	Full	IV	200			MHz
Maximum Full-Scale Output Current	Full	IV	20			mA
Full-Scale Error	Full	V		1%		
Gain Mismatch Error	25°C	IV	−3.5		+3.5	% FS
Offset Mismatch Error	Full	IV	−0.1		+0.1	% FS
Reference Voltage	Full	V		1.23		V
Output Capacitance	Full	V		5		pF
Phase Noise (1 kHz Offset, 6 MHz Tone)	25°C	V		−115		dBc/Hz
Output Voltage Compliance Range	Full	IV	−1.0		+1.0	V
TxPGA Gain Range	Full	V		20		dB
TxPGA Step Size	Full	V		0.10		dB
Tx PATH DYNAMIC PERFORMANCE (I_{OUTFS} = 20 mA; F_{OUT} = 1 MHz)						
SNR	Full	IV	60.2	60.8		dB
SINAD	Full	IV	59.7	60.7		dB
THD	Full	IV		−77.5	−65.8	dBc
SFDR, Wideband (DC to Nyquist)	Full	IV	64.6	76.0		dBc
SFDR, Narrowband (1 MHz Window)	Full	IV	72.5	81.0		dBc

[1] See Figure 2 for description of the TxDAC termination scheme.

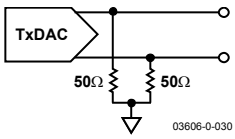

Figure 2. Diagram Showing Termination of 100 Ω Differential Load for Some TxDAC Measurements

Rx PATH SPECIFICATIONS

Table 2. AD9861-50 and AD9861-80
F_{ADC} = 50 MSPS for the AD9861-50, 80 MSPS for the AD9861-80; internal reference; differential analog inputs, ADC_AVDD = DVDD = 3.3V, unless otherwise noted

Parameter	Temp	Test Level	Min	Typ	Max	Unit
Rx PATH GENERAL						
Resolution	Full	V		10		Bits
Maximum ADC Sample Rate	Full	IV	50/80			MSPS
Gain Mismatch Error	Full	V		±0.2		% FS
Offset Mismatch Error	Full	V		±0.1		% FS
Reference Voltage	Full	V		1.0		V
Reference Voltage (REFT–REFB) Error	Full	IV	−30	±6	+30	mV
Input Resistance (Differential)	Full	V		2		kΩ
Input Capacitance	Full	V		5		pF
Input Bandwidth	Full	V		30		MHz
Differential Analog Input Voltage Range	Full	V		2		V p-p differential
Rx PATH DC ACCURACY						
Integral Nonlinearity (INL)	25°C	V		±0.75		LSB
Differential Nonlinearity (DNL)	25°C	V		±0.75		LSB
Aperature Delay	25°C	V		2.0		ns
Aperature Uncertainty (Jitter)	25°C	V		1.2		ps rms
Input Referred Noise	25°C	V		450		uV
AD9861-50 Rx PATH DYNAMIC PERFORMANCE (V_{IN} = −0.5 dBFS; F_{IN} = 10 MHz)						
SNR	Full	IV	55.5	60		dBc
SINAD	Full	IV	55.6	60		dBc
SINAD	25°C	IV	58.5	60		dBc
THD (Second to Ninth Harmonics)	Full	IV		−71.5	−64.6	dBc
SFDR, Wideband (DC to Nyquist)	Full	IV	65.7	73.5		dBc
Crosstalk between ADC Inputs	Full	V		80		dB
AD9861-80 Rx PATH DYNAMIC PERFORMANCE (V_{IN} = −0.5 dBFS; F_{IN} = 10 MHz)						
SNR	Full	IV	55.4	59.5		dBc
SINAD	Full	IV	52.7	59.0		dBc
THD (Second to Ninth Harmonics)	Full	IV		−67		dBc
SFDR, Wideband (DC to Nyquist)	Full	IV		67		dBc
Crosstalk between ADC Inputs	Full	V		80		dB

POWER SPECIFICATIONS

Table 3. AD9861-50 and AD9861-80
Analog and digital supplies = 3.3 V; F_{CLKIN} = 50 MHz; PLL 4× setting; normal timing mode

Parameter	Temp	Test Level	Min	Typ	Max	Unit
POWER SUPPLY RANGE						
Analog Supply Voltage (AVDD)	Full	IV	2.7		3.6	V
Digital Supply Voltage (DVDD)	Full	IV	2.7		3.6	V
Driver Supply Voltage (DRVDD)	Full	IV	2.7		3.6	V
ANALOG SUPPLY CURRENTS						
TxPath (20 mA Full-Scale Outputs)	Full	V		70		mA
TxPath (2 mA Full-Scale Outputs)	Full	V		20		mA
Rx Path (-80, at 80 MSPS)	Full	V		165		mA
RxPath (-80, at 40 MSPS, Low Power Mode)	Full	V		82		mA
RxPath (-80, at 20 MSPS, Ultralow Power Mode)	Full	V		35		mA
Rx Path (-50, at 50 MSPS)	Full	V		103		mA
RxPath (-50, at 50 MSPS, Low Power Mode)	Full	V		69		mA
RxPath (-50, at 16 MSPS, Ultralow Power Mode)	Full	V		28		mA
TxPath, Power-Down Mode	Full	V		2		mA
RxPath, Power-Down Mode	Full	V		5		mA
PLL	Full	V		12		mA
DIGITAL SUPPLY CURRENTS						
TxPath, 1× Interpolation, 50 MSPS DAC Update for Both DACs, Half-Duplex 24 Mode	Full	V		20		mA
TxPath, 2× Interpolation, 100 MSPS DAC Update for Both DACs, Half-Duplex 24 Mode	Full	V		50		mA
TxPath, 4× Interpolation, 200 MSPS DAC Update for Both DACs, Half-Duplex 24 Mode	Full	V		80		mA
RxPath Digital, Half-Duplex 24 Mode	Full	V		15		mA

DIGITAL SPECIFICATIONS

Table 4. AD9861-50 and AD9861-80

Parameter	Temp	Test Level	Min	Typ	Max	Unit
LOGIC LEVELS						
Input Logic High Voltage, V_{IH}	Full	IV	DRVDD – 0.7			V
Input Logic Low Voltage, V_{IL}	Full	IV			0.4	V
Output Logic High Voltage, V_{OH} (1 mA Load)	Full	IV	DRVDD – 0.6			V
Output Logic Low Voltage, V_{OL} (1 mA Load)	Full	IV			0.4	V
DIGITAL PIN						
Input Leakage Current	Full	IV			12	µA
Input Capacitance	Full	IV		3		pF
Minimum RESET Low Pulse Width	Full	IV	5			Input Clock Cycles
Digital Output Rise/Fall Time	Full	IV	2.8		4	ns

TIMING SPECIFICATIONS

Table 5. AD9861-50 and AD9861-80

Parameter	Temp	Test Level	Min	Typ	Max	Unit
INPUT CLOCK						
CLKIN Clock Rate (PLL Bypassed)	Full	IV	1		200	MHz
PLL Input Frequency	Full	IV	16		200	MHz
PLL Ouput Frequency	Full	IV	32		350	MHz
TxPATH DATA						
Setup Time (HD20 Mode, Time Required Before Data Latching Edge)	Full	V		5		ns (see Clock Distribution Block section)
Hold Time (HD20 Mode, Time Required After Data Latching Edge)	Full	V		–1.5		ns (see Clock Distribution Block section)
Latency 1× Interpolation (data in until peak output response)	Full	V		7		DAC Clock Cycles
Latency 2× Interpolation (data in until peak output response)	Full	V		35		DAC Clock Cycles
Latency 4× Interpolation (data in until peak output response)	Full	V		83		DAC Clock Cycles
RxPATH DATA						
Output Delay (HD20 Mode, t_{OD})	Full	V		–1.5		ns (see Clock Distribution Block section)
Latency	Full	V		5		ADC Clock Cycles

Table 6. Explanation of Test Levels

Level	Description
I	100% production tested.
II	100% production tested at 25°C and guaranteed by design and characterization at specified temperatures.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	100% production tested at 25°C and guaranteed by design and characterization for industrial temperature range.

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Electrical	
AVDD Voltage	3.9 V max
DRVDD Voltage	3.9 V max
Analog Input Voltage	–0.3 V to AVDD + 0.3 V
Digital Input Voltage	–0.3 V to DVDD – 0.3 V
Digital Output Current	5 mA max
Environmental	
Operating Temperature Range (Ambient)	–40°C to +85°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range (Ambient)	–65°C to +150°C

Thermal Resistance

64-lead LFCSP (4-layer board):

θ_{JA} = 24.2 (paddle soldered to ground plan, 0 LPM Air)

θ_{JA} = 30.8 (paddle not soldered to ground plan, 0 LPM Air)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND PIN FUNCTION DESCRIPTIONS

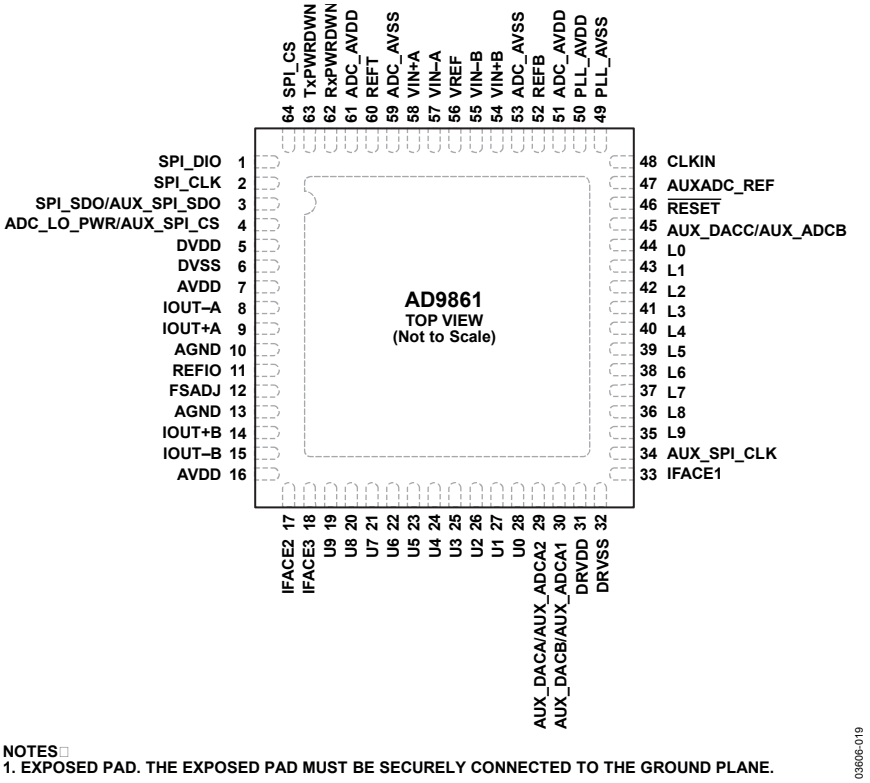

Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Name[1]	Description[2, 3]
1	SPI_DIO (Interp1)	**SPI:** Serial Port Data Input. **No SPI:** Tx Interpolation Pin, MSB.
2	SPI_CLK (Interp0)	**SPI:** Serial Port Shift Clock. **No SPI:** Tx Interpolation Pin, LSB.
3	SPI_SDO/AUXSPI_SDO (FD/$\overline{HD}$)	**SPI:** 4-Wire Serial Port Data Output/Data Output Pin for AuxSPI. **No SPI:** Configures Full-Duplex or Half-Duplex Mode.
4	ADC_LO_PWR/AUX_SPI_CS	ADC Low Power Mode Enable. Defined at power-up. CS for AuxSPI.
5, 31	DVDD	Digital Supply.
6, 32	DVSS	Digital Ground.
7, 16, 50, 51, 61	AVDD	Analog Supply.
8, 9	IOUT–A, IOUT+A	DAC A Differential Output.
10, 13, 49, 53, 59	AGND, AVSS	Analog Ground.
11	REFIO	Tx DAC Band Gap Reference Decoupling Pin.
12	FSADJ	Tx DAC Full-Scale Adjust Pin.
14, 15	IOUT+B, IOUT−B	DAC B Differential Output.
17	IFACE2 (10/$\overline{20}$)	**SPI**: Buffered CLKIN. Can be configured as system clock output. **No SPI**: For **FD**: Buffered CLKIN; For **HD20** or **HD10** : 10/$\overline{20}$ Configuration Pin.
18	IFACE3	Clock Output.
19–28	U9–U0	Upper Data Bit 9 to Upper Data Bit 0.
29	AUX1	Configurable as either AuxADC_A2 or AuxDAC_A.
30	AUX2	Configurable as either AuxADC_A1 or AuxDAC_B.
33	IFACE1	**SPI**: For **FD**: TxSYNC; For **HD20, HD10**, or **Clone**: Tx/$\overline{Rx}$. **No SPI**: **FD** >> TxSYNC; **HD20** or **HD10**: Tx/$\overline{Rx}$.
34	AUX_SPI_CLK	CLK for AuxSPI.
35–44	L9–L0	Lower Data Bit 9 to Lower Data Bit 0.

Pin No.	Name[1]	Description[2, 3]
45	AUX3	Configurable as either AuxADC_B or AuxDAC_C.
46	$\overline{\text{RESET}}$	Chip Reset When Low.
47	AUX_ADC_REF	Decoupling for AuxADC On-Chip Reference.
48	CLKIN	Clock Input.
52	REFB	ADC Bottom Reference.
54, 55	VIN+B, VIN−B	ADC B Differential Input.
56	VREF	ADC Band Gap Reference.
57, 58	VIN−A, VIN+A	ADC A Differential Input.
60	REFT	ADC Top Reference.
62	RxPwrDwn	Rx Analog Power-Down Control.
63	TxPwrDwn	Tx Analog Power-Down Control.
64	SPI_CS	**SPI:** Serial Port Chip Select. At power-up or reset, this must be high. **No SPI:** Tie low to disable SPI and use mode pins. This pin must be tied low.
	EPAD	Exposed Pad. The exposed pad must be securely connected to the ground plane.

[1] Underlined pin names and descriptions apply when the device is configured without a serial port interface, referred to as no SPI mode.
[2] Pin function depends if the serial port is used to configure the AD9861 (called SPI mode) or if mode pins are used to configure the AD9861 (called No SPI mode). The differences are indicated by the **SPI** and **No SPI** labels in the description column.
[3] Some pin descriptions depend on the interface configuration, full-duplex (FD), half-duplex interleaved data (HD10), half-duplex parallel data (HD20), and a half-duplex interface similar to the AD9860 and AD9862 data interface called clone mode (Clone). Clone mode requires a serial port interface.

TYPICAL PERFORMANCE CHARACTERISTICS

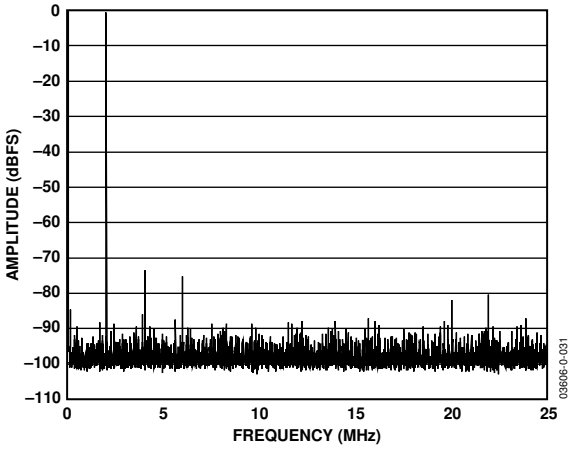

Figure 4. AD9861-50 Rx Path Single-Tone FFT of Rx Channel B Path Digitizing 2 MHz Tone

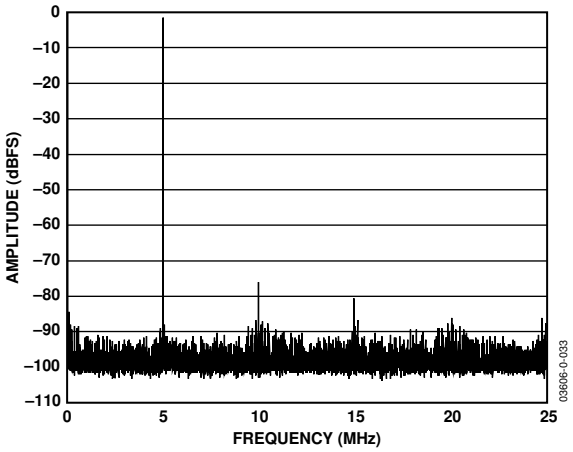

Figure 5. AD9861-50 Rx Path Single-Tone FFT of Rx Channel B Path Digitizing 5 MHz Tone

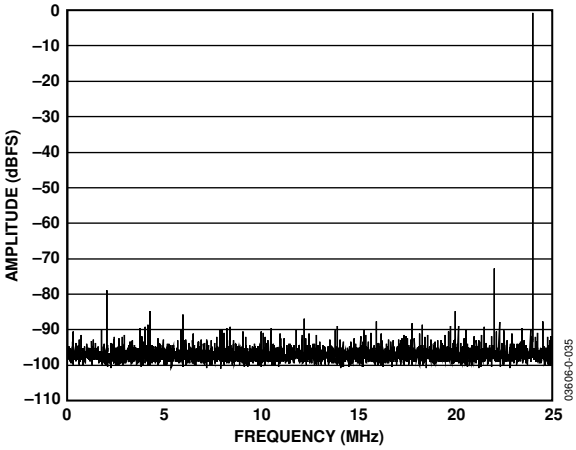

Figure 6. AD9861-50 Rx Path Single-Tone FFT of Rx Channel B Path Digitizing 24 MHz Tone

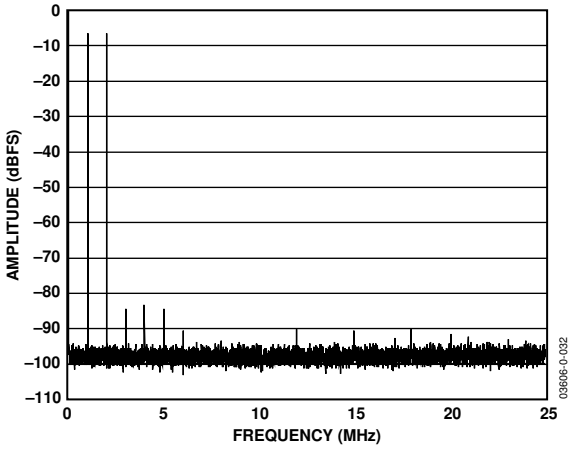

Figure 7. AD9861-50 Rx Path Dual-Tone FFT of Rx Channel A Path Digitizing 1 MHz and 2 MHz Tones

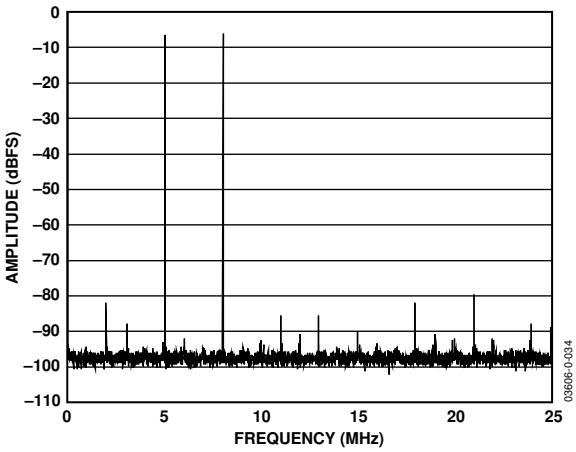

Figure 8. AD9861-50 Rx Path Dual-Tone FFT of Rx Channel A Path Digitizing 5 MHz and 8 MHz Tones

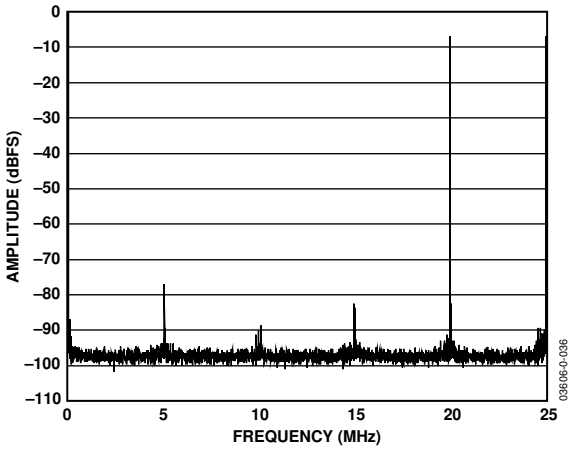

Figure 9. AD9861-50 Rx Path Dual-Tone FFT of Rx Channel A Path Digitizing 20 MHz and 25 MHz Tones

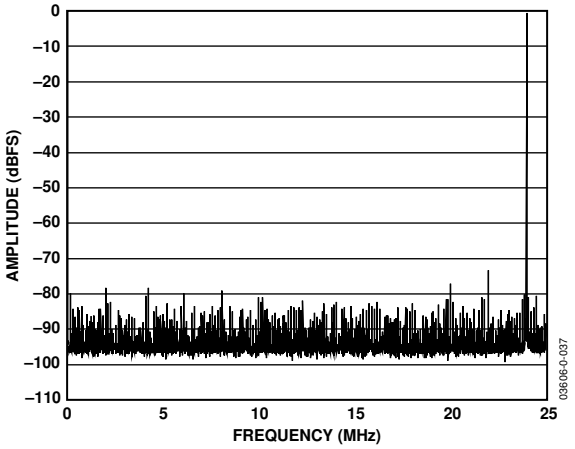

Figure 10. AD9861-50 Rx Path Single-Tone FFT of Rx Channel B Path Digitizing 76 MHz Tone

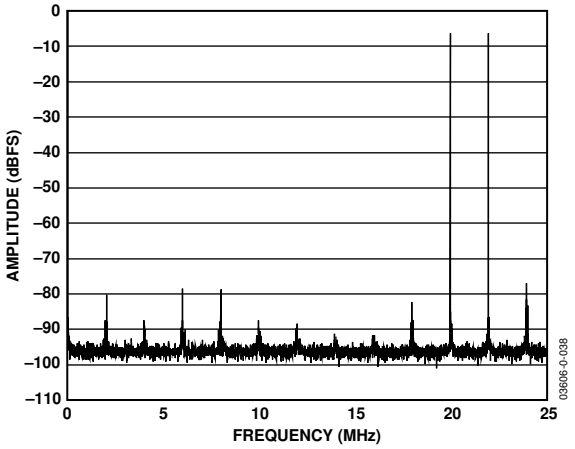

Figure 13. AD9861-50 Rx Path Dual-Tone FFT of Rx Channel A Path Digitizing 70 MHz and 72 MHz Tones

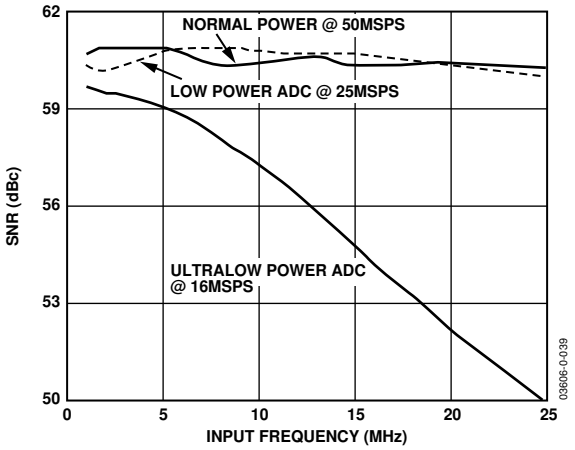

Figure 11. AD9861-50 Rx Path at 50 MSPS, 10 MHz Input Tone SNR Performance vs. Input Frequency

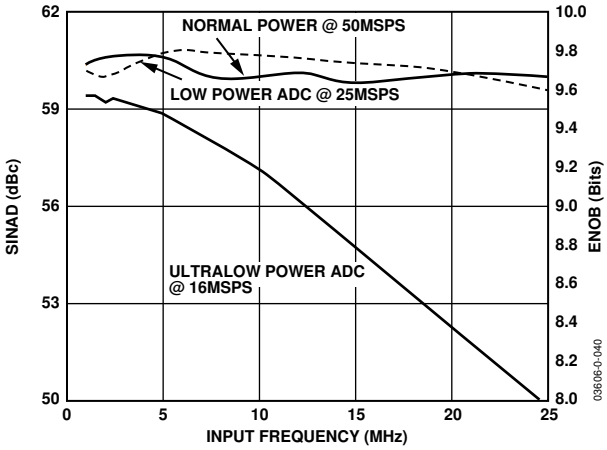

Figure 14. AD9861-50 Rx Path at 50 MSPS, 10 MHz Input Tone SINAD Performance vs. Input Frequency

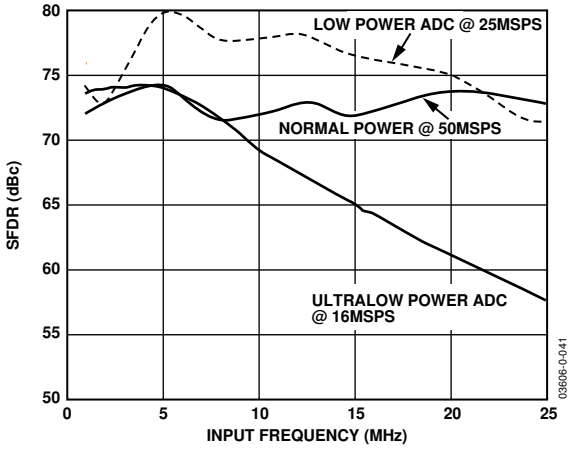

Figure 12. AD9861-50 Rx Path at 50 MSPS, 10 MHz Input Tone SFDR Performance vs. Input Frequency

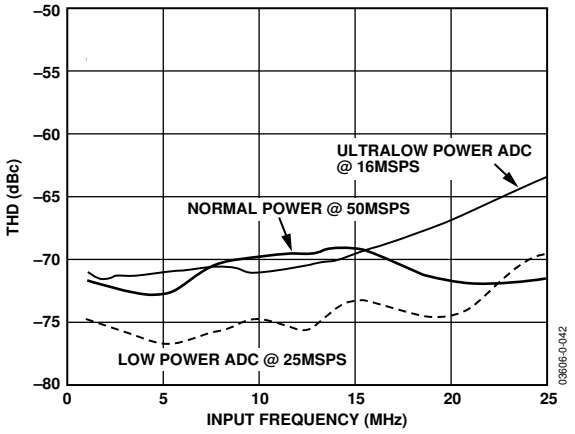

Figure 15. AD9861-50 Rx Path at 50 MSPS, 10 MHz Input Tone THD Performance vs. Input Frequency

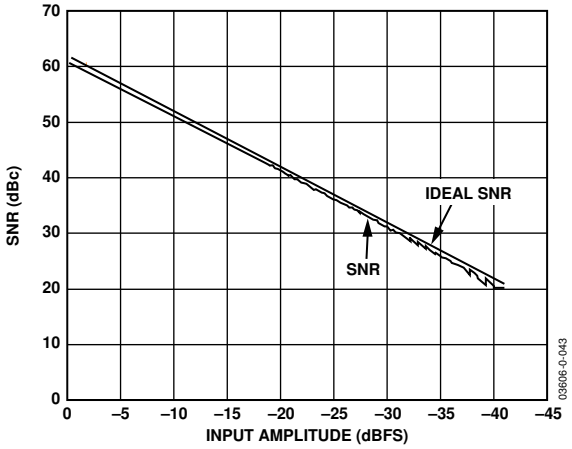

Figure 16. AD9861-50 Rx Path at 50 MSPS, 10 MHz Input Tone SNR Performance vs. Input Amplitude

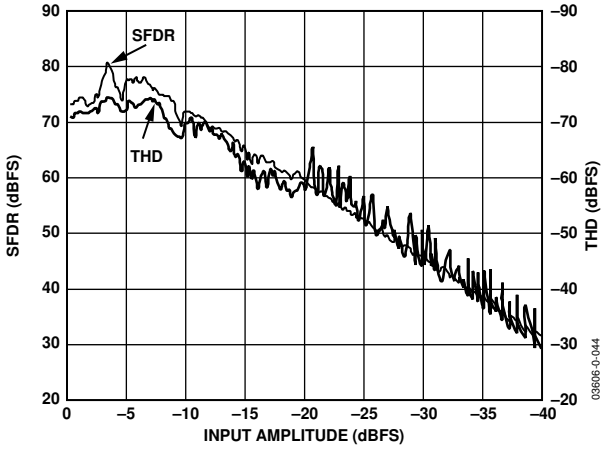

Figure 19. AD9861-50 Rx Path at 50 MSPS, 10 MHz Input Tone THD and SFDR Performance vs. Input Amplitude

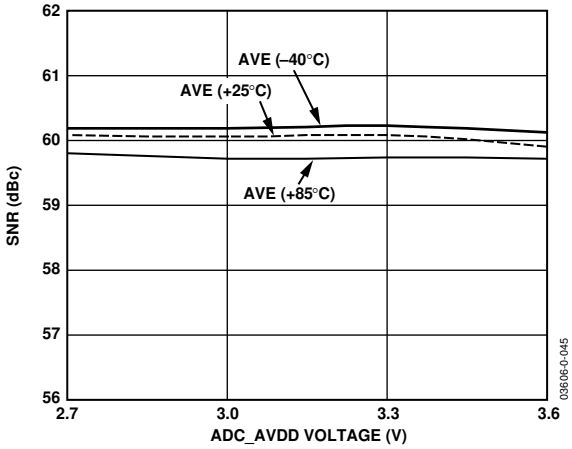

Figure 17. AD9861-50 Rx Path at 50 MSPS, 10 MHz Input Tone SNR Performance vs. ADC_AVDD and Temperature

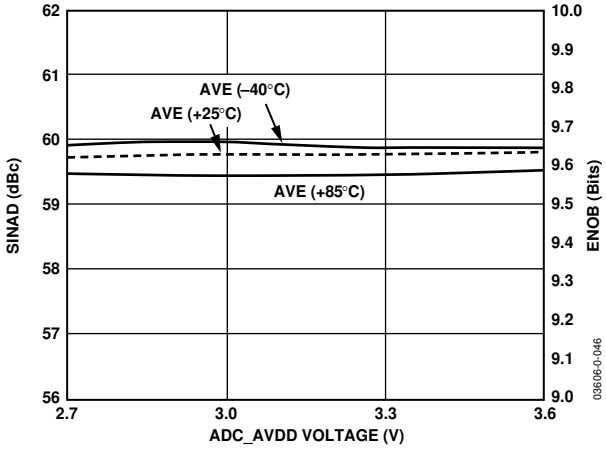

Figure 20. AD9861-50 Rx Path at 50 MSPS, 10 MHz Input Tone SINAD Performance vs. ADC_AVDD and Temperature

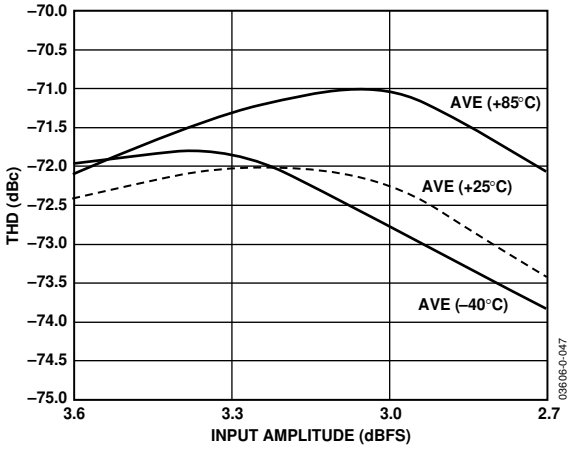

Figure 18. AD9861-50 Rx Path Single-Tone THD Performance vs. ADC_AVDD and Temperature

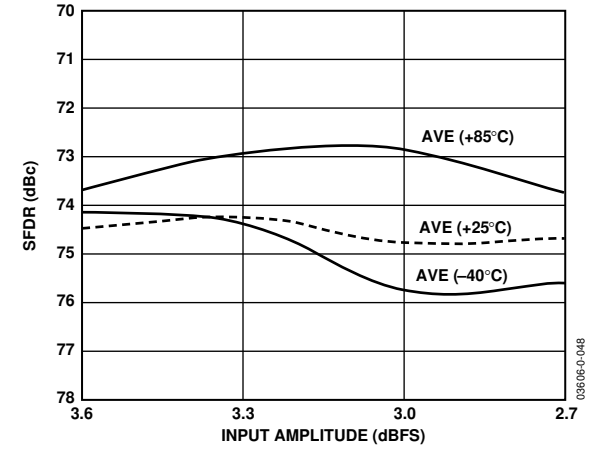

Figure 21. AD9861-50 Rx Path Single-Tone SFDR Performance vs. ADC_AVDD and Temperature

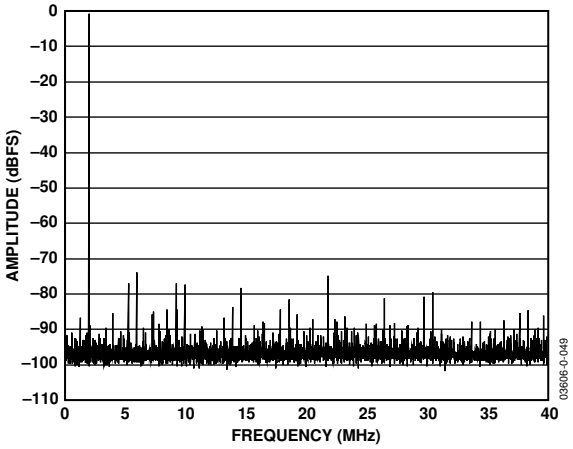

Figure 22. AD9861-80 Rx Path Single-Tone FFT of Rx Channel B Path Digitizing 2 MHz Tone

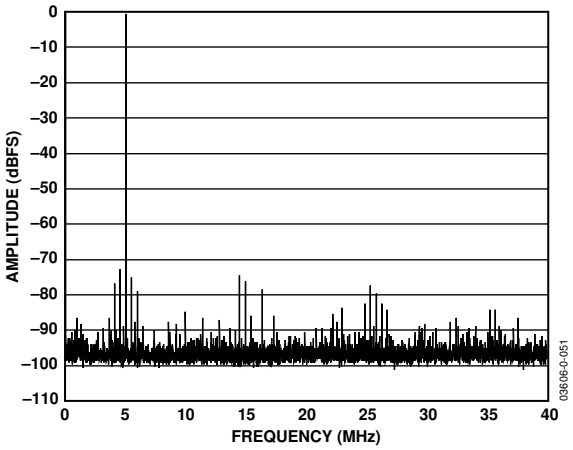

Figure 23. AD9861-80 Rx Path Single-Tone FFT of Rx Channel B Path Digitizing 5 MHz Tone

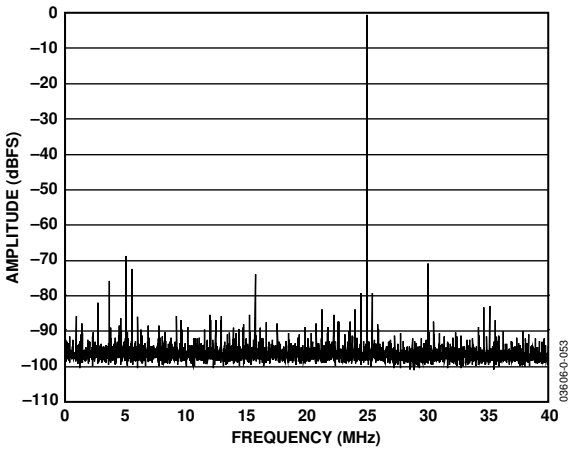

Figure 24. AD9861-80 Rx Path Single-Tone FFT of Rx Channel B Path Digitizing 24 MHz Tone

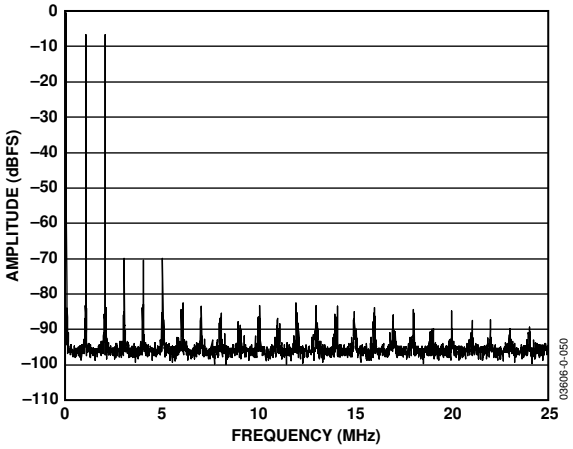

Figure 25. AD9861-80 Rx Path Dual-Tone FFT of Rx Channel A Path Digitizing 1 MHz and 2 MHz Tones

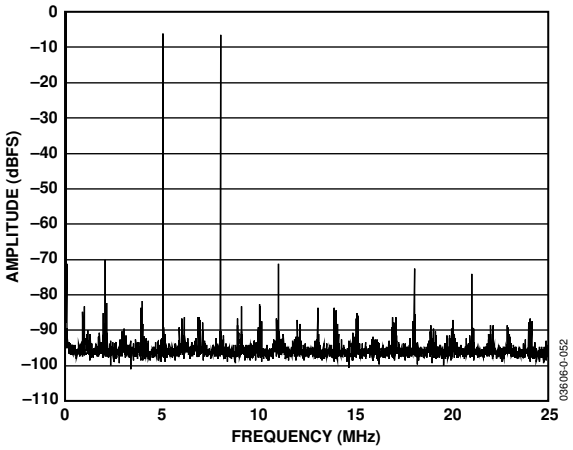

Figure 26. AD9861-80 Rx Path Dual-Tone FFT of Rx Channel A Path Digitizing 5 MHz and 8 MHz Tones

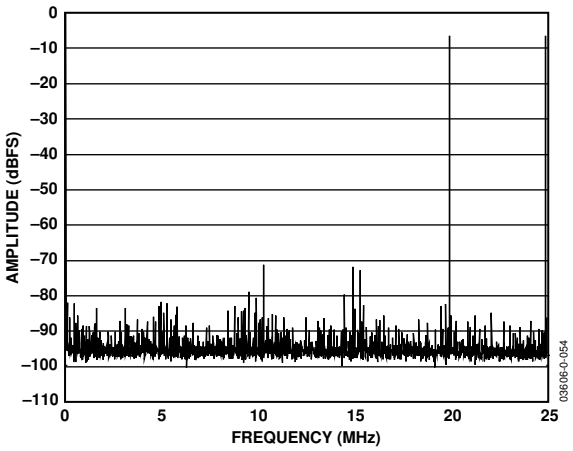

Figure 27. AD9861-80 Rx Path Dual-Tone FFT of Rx Channel A Path Digitizing 20 MHz and 25 MHz Tones

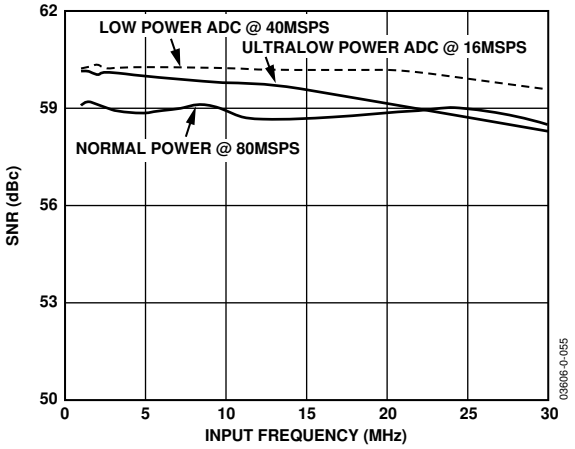

Figure 28. AD9861-80 Rx Path at 80 MSPS, 10 MHz Input Tone SNR Performance vs. Input Frequency and Power Setting

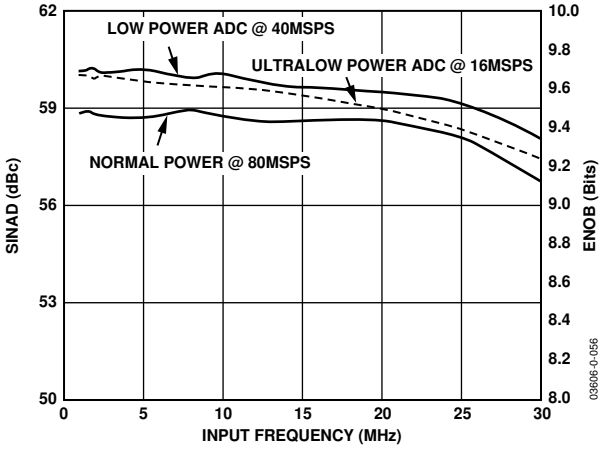

Figure 31. AD9861-80 Rx Path at 80 MSPS, 10 MHz Input Tone SINAD Performance vs. Input Frequency and Power Setting

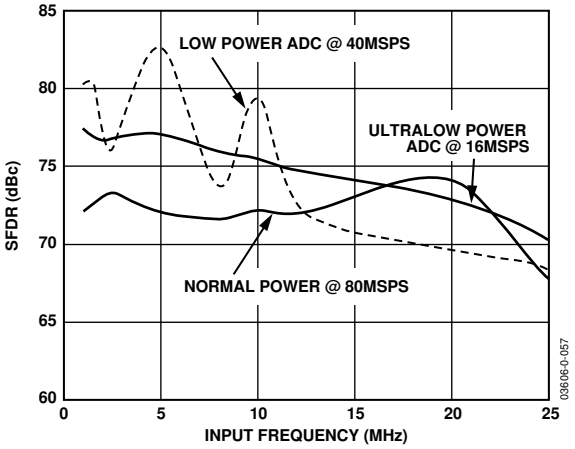

Figure 29. AD9861-80 Rx Path at 80 MSPS, 10 MHz Input Tone SFDR Performance vs. Input Frequency and Power Setting

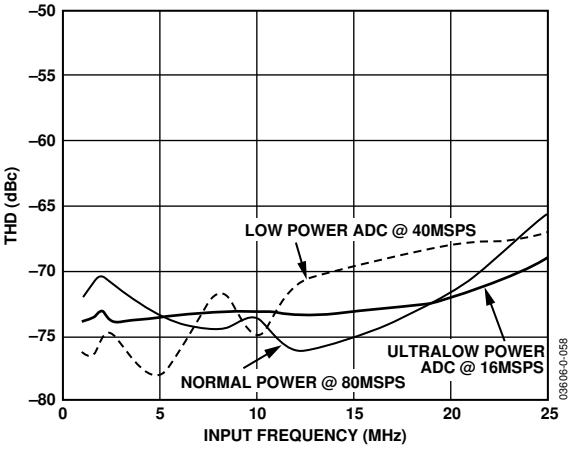

Figure 32. AD9861-80 Rx Path at 80 MSPS, 10 MHz Input Tone THD Performance vs. Input Frequency and Power Setting

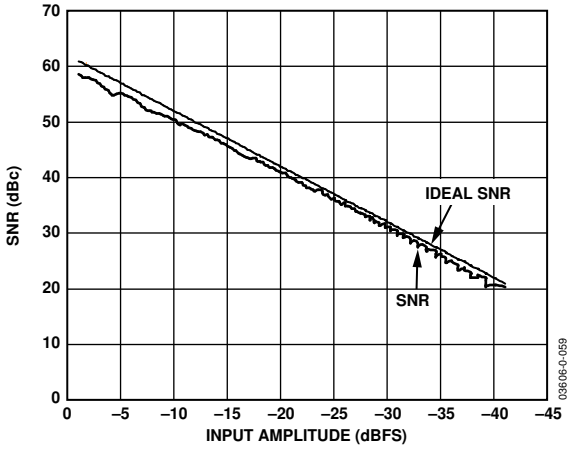

Figure 30. AD9861-80 Rx Path at 80 MSPS, 10 MHz Input Tone SNR Performance vs. Input Amplitude

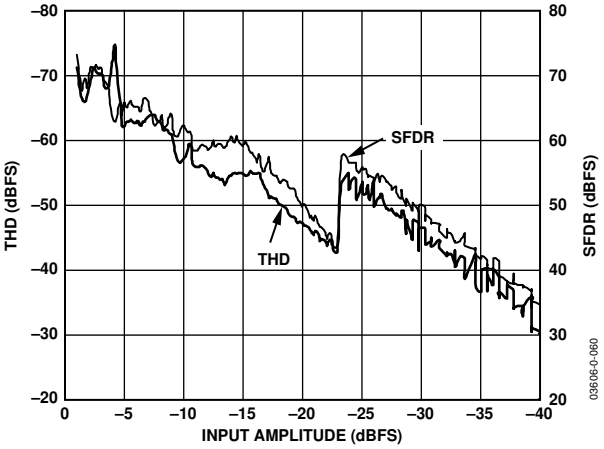

Figure 33. AD9861-80 Rx Path at 80 MSPS, 10 MHz Input Tone THD Performance vs. Input Amplitude

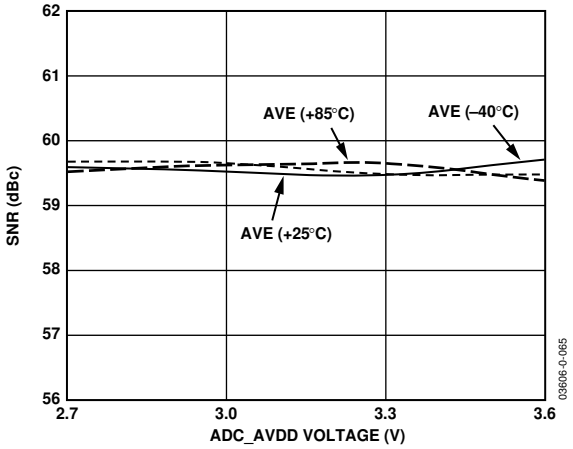

Figure 34. AD9861-80 Rx Path at 80 MSPS, 10 MHz Input Tone SNR Performance vs. AVDD and Temperature

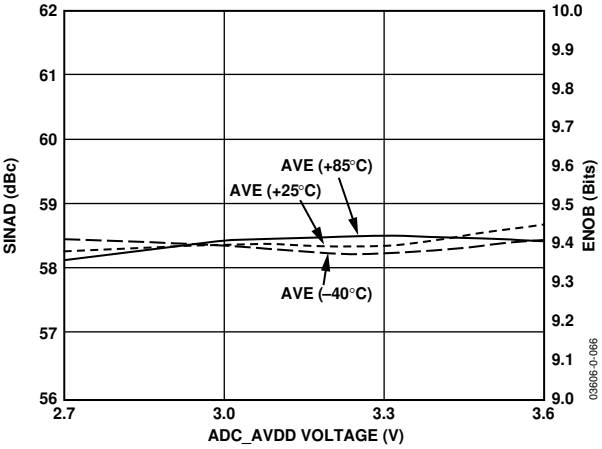

Figure 37. AD9861-80 Rx Path at 80 MSPS, 10 MHz Input Tone SINAD Performance vs. AVDD and Temperature

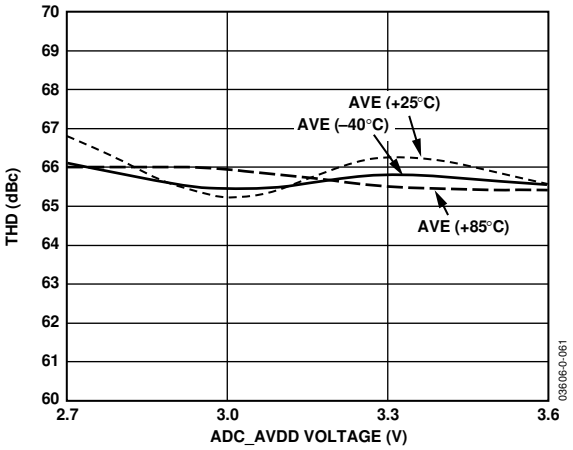

Figure 35. AD9861-80 Rx Path at 80 MSPS, 10 MHz Input Tone THD Performance vs. AVDD and Temperature

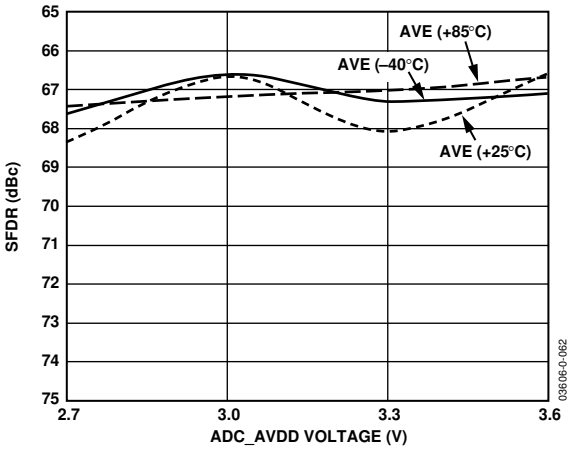

Figure 38. AD9861-80 Rx Path at 80 MSPS, 10 MHz Input Tone SFDR Performance vs. AVDD and Temperature

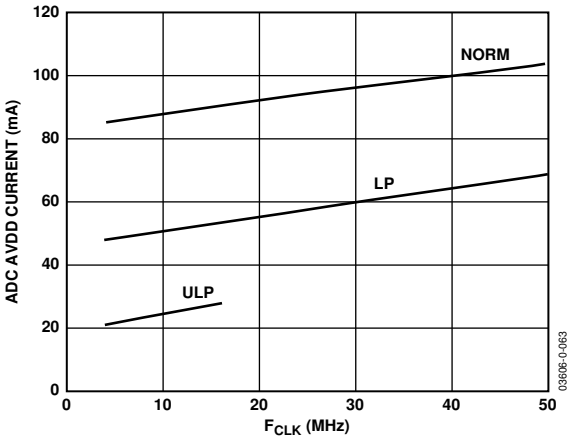

Figure 36. AD9861-50 ADC_AVDD Current vs. Sampling Rate for Different ADC Power Levels

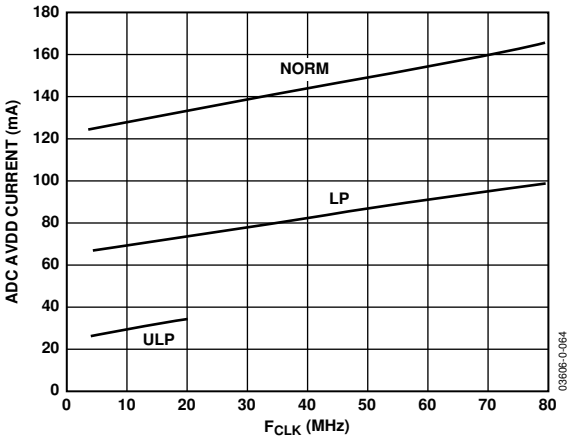

Figure 39. AD9861-80 ADC_AVDD Current vs. ADC Sampling Rate for Different ADC Power Levels

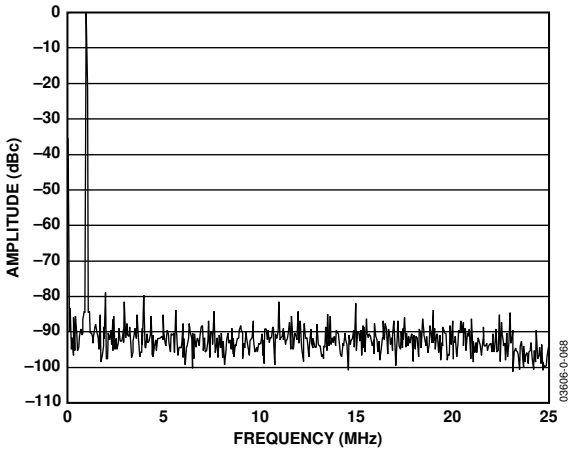

Figure 40. AD9861 Tx Path 1 MHz Single-Tone Output FFT of Tx Path with 20 mA Full-Scale Output into 33 Ω Differential Load

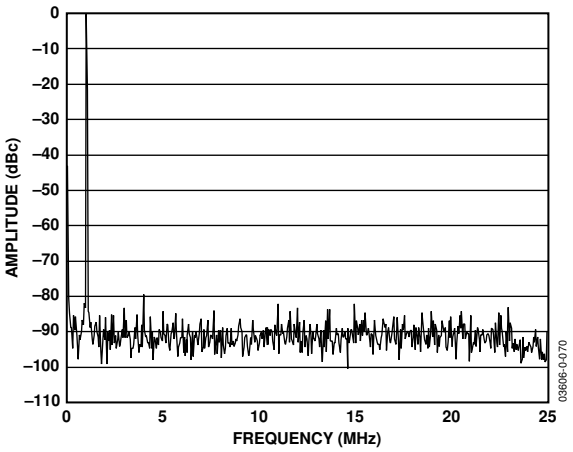

Figure 41. AD9861 Tx Path 1 MHz Single-Tone Output FFT of Tx Path with 20 mA Full-Scale Output into 60 Ω Differential Load

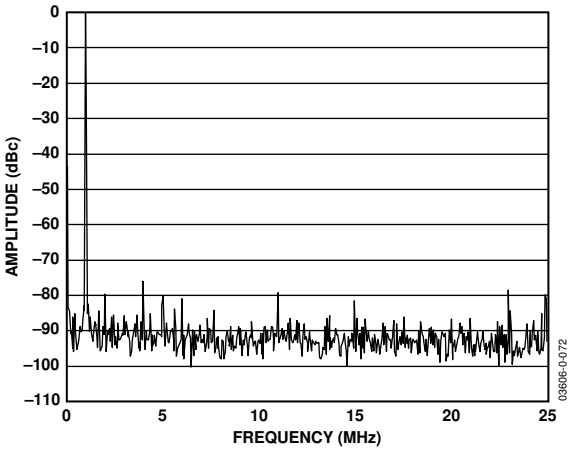

Figure 42. AD9861 Tx Path 1 MHz Single-Tone Output FFT of Tx Path with 2 mA Full-Scale Output into 600 Ω Differential Load

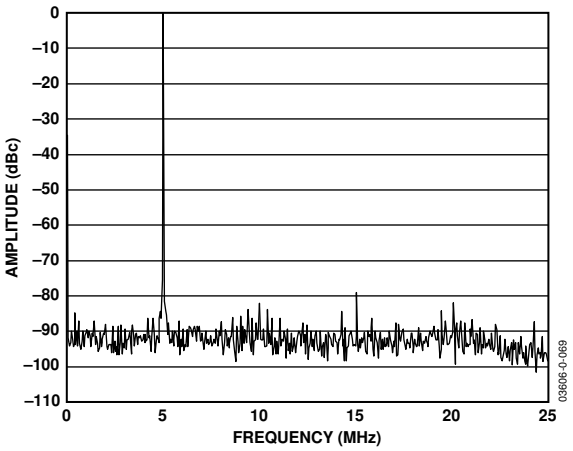

Figure 43. AD9861 Tx Path 5 MHz Single-Tone Output FFT of Tx Path with 20 mA Full-Scale Output into 33 Ω Differential Load

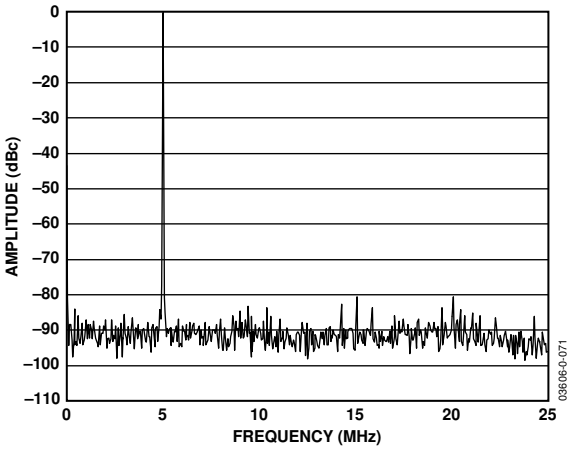

Figure 44. AD9861 Tx Path 5 MHz Single-Tone Output FFT of Tx Path with 20 mA Full-Scale Output into 60 Ω Differential Load

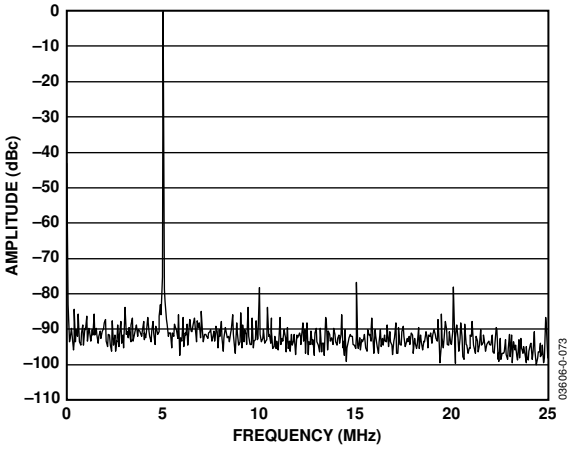

Figure 45. AD9861 Tx Path 5 MHz Single-Tone Output FFT of Tx Path with 2 mA Full-Scale Output into 600 Ω Differential Load

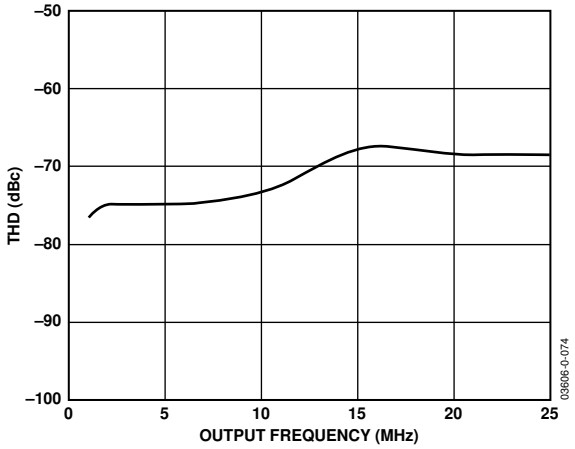

Figure 46. AD9861 Tx Path THD vs. Output Frequency of Tx Path with 20 mA Full-Scale Output into 60 Ω Differential Load

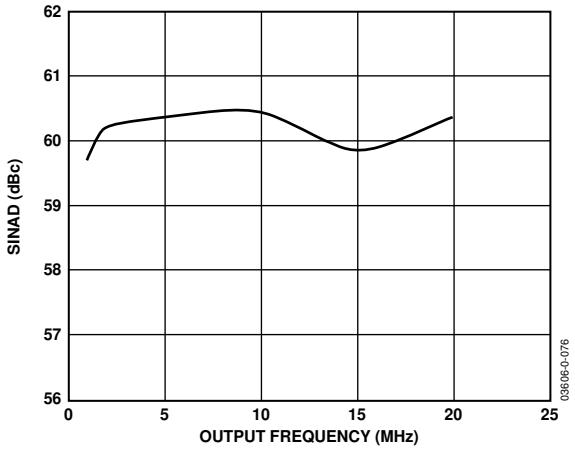

Figure 47. AD9861 Tx Path SINAD vs. Output Frequency of Tx Path, with 20 mA Full-Scale Output into 60 Ω Differential Load

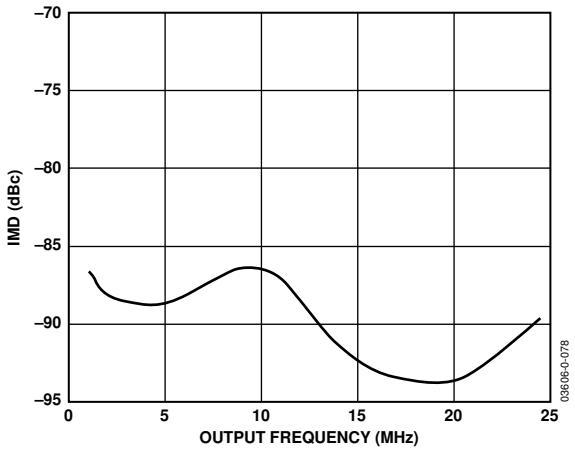

Figure 48. AD9861 Tx Path Dual-Tone (0.5 MHz Spacing) IMD vs. Output Frequency of Tx Path, with 20 mA Full-Scale Output into 60 Ω Differential Load

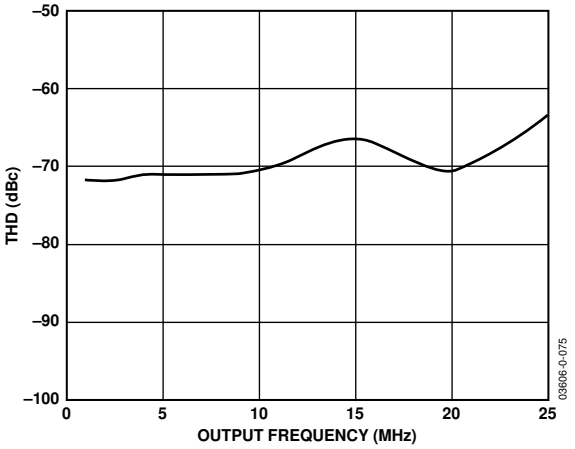

Figure 49. AD9861 Tx Path THD vs. Output Frequency of Tx Path with 2 mA Full-Scale Output into 600 Ω Differential Load

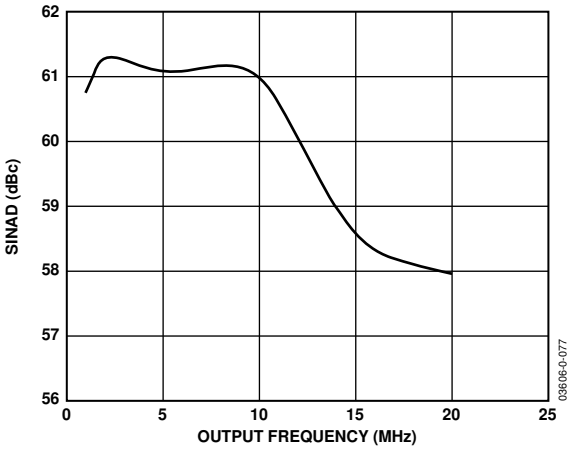

Figure 50. AD9861 Tx Path SINAD vs. Output Frequency of Tx Path, with 2 mA Full-Scale Output into 600 Ω Differential Load

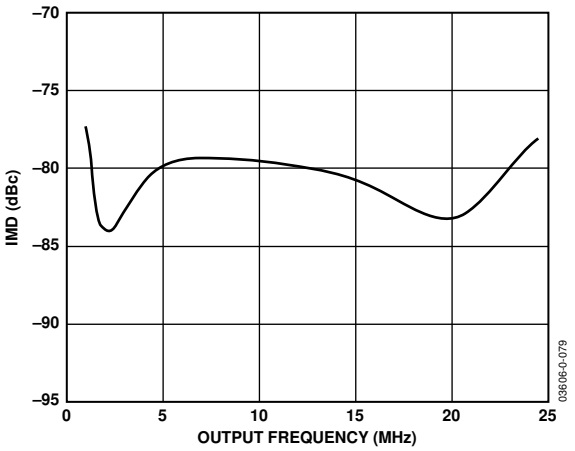

Figure 51. AD9861 Tx Path Dual-Tone (0.5 MHz Spacing) IMD vs. Output Frequency of Tx Path, with 2 mA Full-Scale Output into 600 Ω Differential Load

Figure 52 to Figure 57 use the same input data to the Tx path, a 64-carrier OFDM signal over a 20 MHz bandwidth, centered at 20 MHz. The center two carriers are removed from the signal to observe the in-band intermodulation distortion (IMD) from the DAC output.

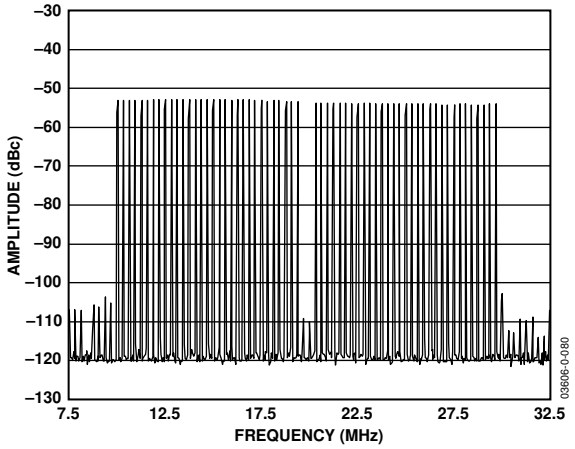

Figure 52. AD9861 Tx Path FFT, 64-Carrier (Center Two Carriers Removed) OFDM Signal over 20 MHz Bandwidth, Centered at 20 MHz, with 20 mA Full-Scale Output into 60 Ω Differential Load

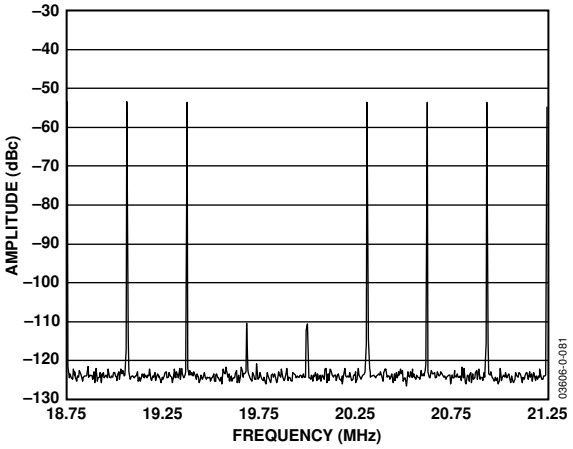

Figure 55. AD9861 Tx Path FFT, In-Band IMD Products of OFDM Signal in Figure 52

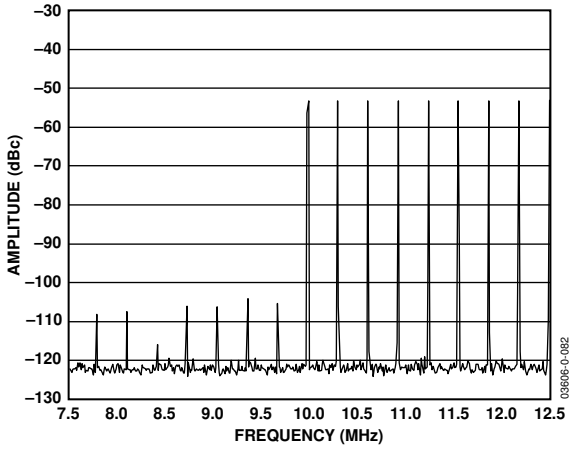

Figure 53. AD9861 Tx Path FFT, Lower-Band IMD Products of OFDM Signal in Figure 52

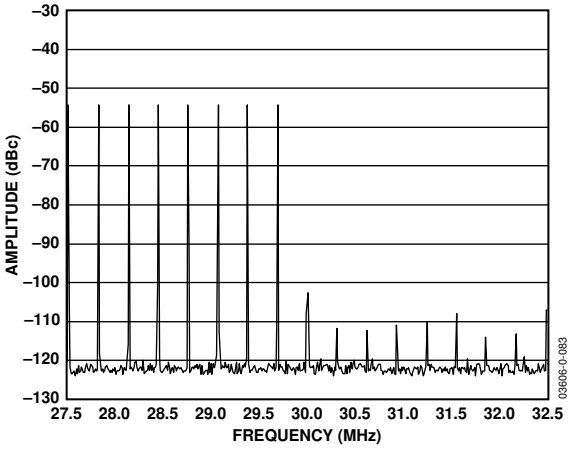

Figure 56. AD9861 Tx Path FFT, Upper-Band IMD Products of OFDM Signal in Figure 52

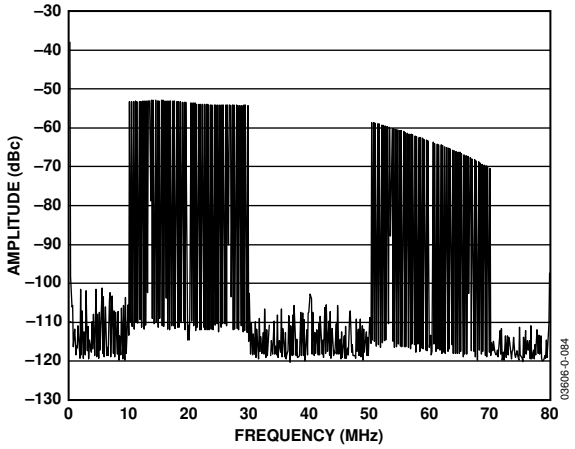

Figure 54. AD9861 Tx Path FFT of OFDM Signal in Figure 52, with 1× Interpolation

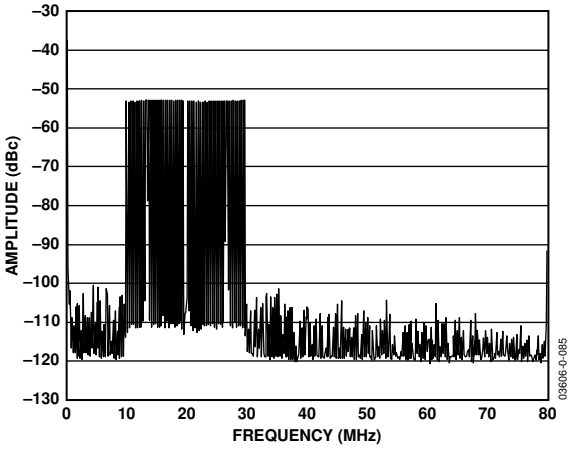

Figure 57. AD9861 Tx Path FFT of OFDM Signal in Figure 52, with 4× Interpolation

Figure 58 to Figure 63 use the same input data to the Tx path, a 256-carrier OFDM signal over a 1.75 MHz bandwidth, centered at 7 MHz. The center four carriers are removed from the signal to observe the in-band intermodulation distortion (IMD) from the DAC output.

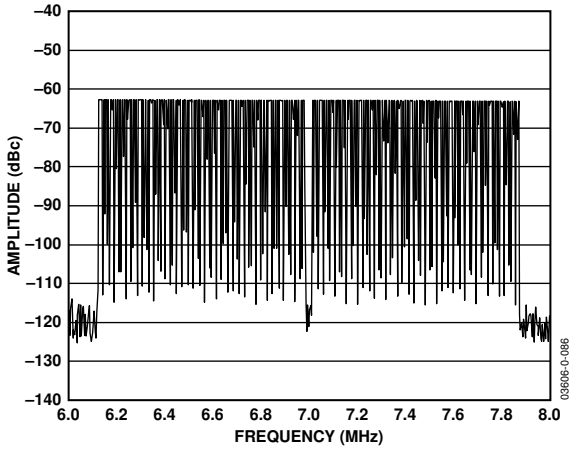

Figure 58. AD9861 Tx Path FFT, 256-Carrier (Center Four Carriers Removed) OFDM Signal over 1.75 MHz Bandwidth, Centered at 7 MHz, with 20 mA Full-Scale Output into 60 Ω Differential Load

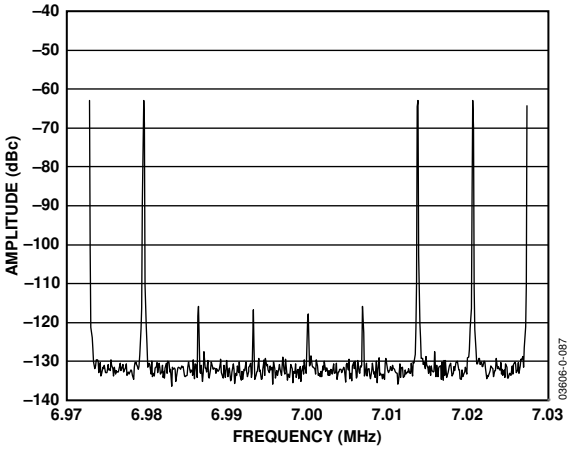

Figure 61. AD9861 Tx Path FFT, In-Band IMD Products of OFDM Signal in Figure 58

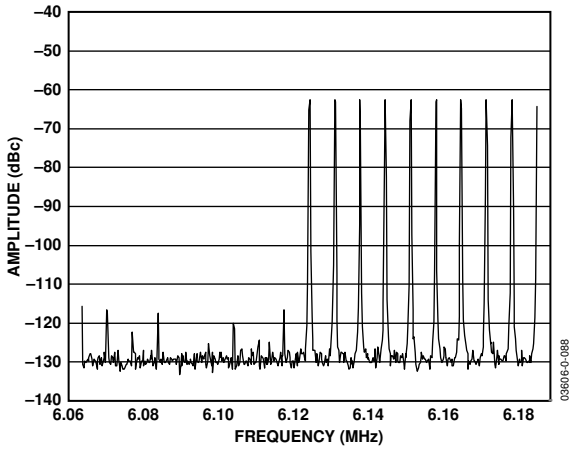

Figure 59. AD9861 Tx Path FFT, Lower-Band IMD Products of OFDM Signal in Figure 58

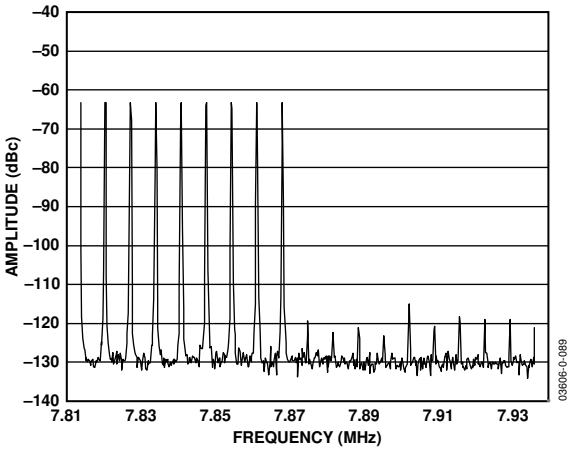

Figure 62. AD9861 Tx Path FFT, Upper-Band IMD Products of OFDM Signal in Figure 52

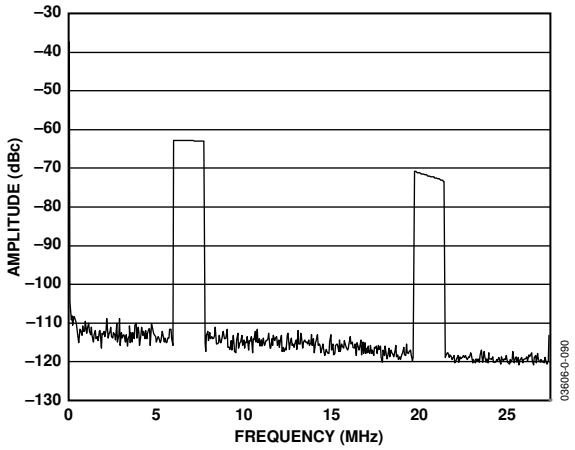

Figure 60. AD9861 Tx Path FFT of OFDM Signal in Figure 52, with 1× Interpolation

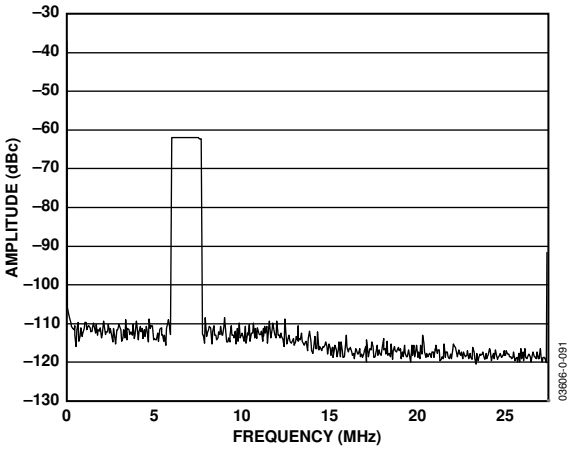

Figure 63. AD9861 Tx Path FFT of OFDM Signal in Figure 52, with 4× Interpolation

Figure 64 to Figure 69 use the same input data to the Tx path, a 256-carrier OFDM signal over a 23 MHz bandwidth, centered at 23 MHz. The center four carriers are removed from the signal to observe the in-band intermodulation distortion (IMD) from the DAC output.

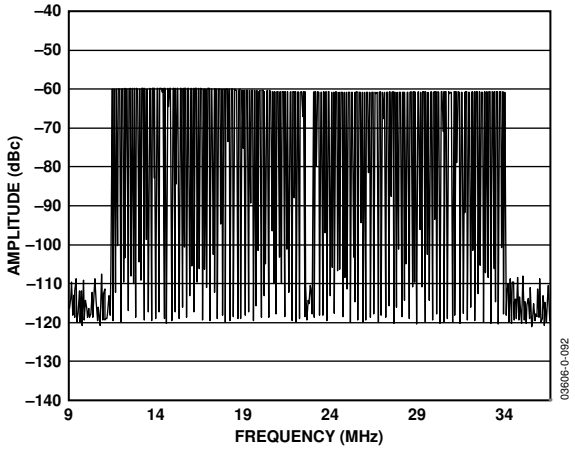

Figure 64. AD9861 Tx Path FFT, 256-Carrier (Center Four Carriers Removed) OFDM Signal over 23 MHz Bandwidth, Centered at 7 MHz, with 20 mA Full-Scale Output into 60 Ω Differential Load

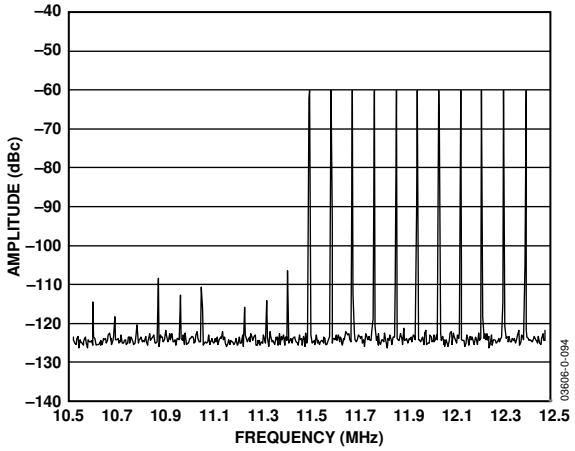

Figure 65. AD9861 Tx Path FFT, Lower-Band IMD Products of OFDM Signal in Figure 64

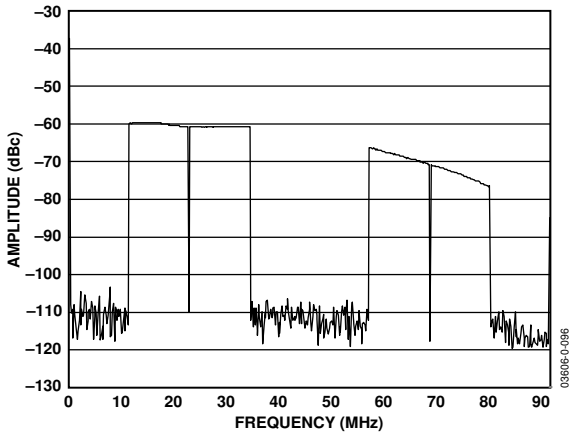

Figure 66. AD9861 Tx Path FFT of OFDM Signal in Figure 52 with 1× Interpolation

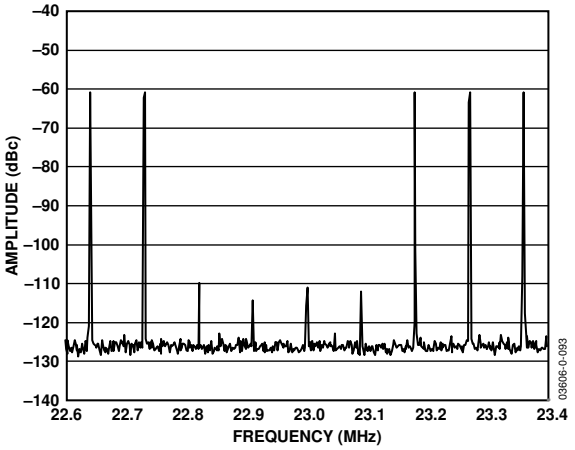

Figure 67. AD9861 Tx Path FFT, In-Band IMD Products of OFDM Signal in Figure 64

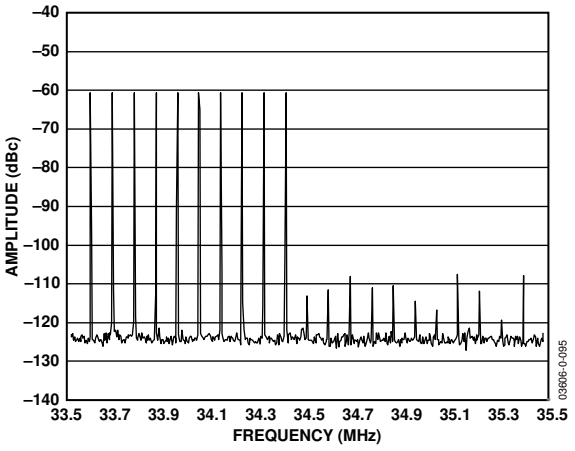

Figure 68. AD9861 Tx Path FFT, Upper-Band IMD Products of OFDM Signal in Figure 64

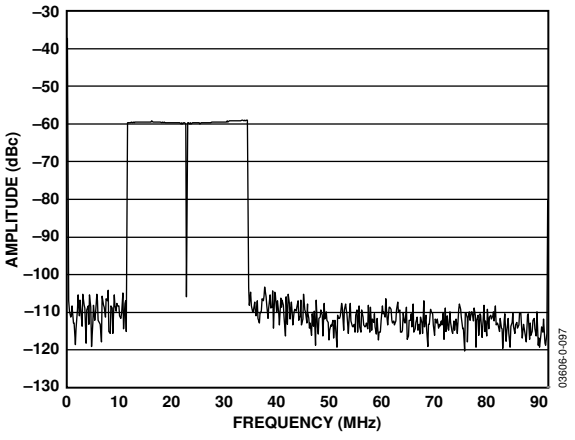

Figure 69. AD9861 Tx Path FFT of OFDM Signal in Figure 52 with 4× Interpolation

TERMINOLOGY

Input Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the CLKIN signal and the instant at which the analog input is actually sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Crosstalk
Coupling onto one channel being driven by a −0.5 dBFS signal when the adjacent interfering channel is driven by a full-scale signal.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180° out of phase. Peak-to-peak differential is computed by rotating the input phase 180° and taking the peak measurement again. Then the difference is computed between both peak measurements.

Differential Nonlinearity
The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB)
The effective number of bits is calculated from the measured SNR based on the following equation:

$$ENOB = \frac{SNR_{MEASURED} - 1.76\ dB}{6.02}$$

Pulse Width/Duty Cycle
Pulse width high is the minimum amount of time that a signal must be left in the logic high state to achieve rated performance; pulse width low is the minimum time a signal must be left in the low state, logic low.

Full-Scale Input Power
Expressed in dBm, full-scale input power is computed using the following equation:

$$Power_{FULLSCALE} = 10\log\left(\frac{V_{FULLSCALE-RMS}^2 / Z_{INPUT}}{0.001}\right)$$

Gain Error
Gain error is the difference between the measured and ideal full-scale input voltage range of the ADC.

Harmonic Distortion, Second
The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

Harmonic Distortion, Third
The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of an LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate

The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between a differential crossing of CLK+ and CLK− and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise and Distortion (SINAD)
The ratio of the rms signal amplitude (set 1 dB below full-scale) to the rms value of the sum of all other spectral components, including harmonics, but excluding dc.

Signal-to-Noise Ratio (without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. It also may be reported in dBc (i.e., degrades as signal level is lowered) or dBFS (i.e., always related back to converter full scale). SFDR does not include harmonic distortion components.

Worst Other Spur
The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonics) reported in dBc.

THEORY OF OPERATION

SYSTEM BLOCK

The AD9861 is targeted to cover the mixed-signal front end needs of multiple wireless communication systems. It features a receive path that consists of dual 10-bit receive ADCs, and a transmit path that consists of dual 10-bit transmit DACs (TxDAC). The AD9861 integrates additional functionality typically required in most systems, such as power scalability, additional auxiliary converters, Tx gain control, and clock multiplication circuitry.

The AD9861 minimizes both size and power consumption to address the needs of a range of applications from the low power portable market to the high performance base station market. The part is provided in a 64-lead lead frame chip scale package (LFCSP) that has a footprint of only 9 mm × 9 mm. Power consumption can be optimized to suit the particular application beyond just a speed grade option by incorporating power-down controls, low power ADC modes, TxDAC power scaling, and a half-duplex mode, which automatically disables the unused digital path.

The AD9861 uses two 10-bit buses to transfer Rx path data and Tx path data. These two buses support 20-bit parallel data transfers or 10-bit interleaved data transfers. The bus is configurable through either external mode pins or through internal registers settings. The registers allow many more options for configuring the entire device.

The following sections discuss the various blocks of the AD9861: Rx block, Tx block, the auxiliary converters, the digital block, programmable registers and the clock distribution block.

Rx PATH BLOCK

Rx Path General Description

The AD9861 Rx path consists of two 10-bit, 50 MSPS (for the AD9861-50) or 80 MSPS (for the AD9861-80) analog-to-digital converters (ADCs). The dual ADC paths share the same clocking and reference circuitry to provide optimal matching characteristics. Each of the ADCs consists of a 9-stage differential pipelined switched capacitor architecture with output error correction logic.

The pipelined architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. Sampling occurs on the falling edge of the input clock. Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC and a residual multiplier to drive the next stage of the pipeline. The residual multiplier uses the flash ADC output to control a switched capacitor digital-to-analog converter (DAC) of the same resolution. The DAC output is subtracted from the stage's input signal, and the residual is amplified (multiplied) to drive the next pipeline stage. The residual multiplier stage is also called a multiplying DAC (MDAC). One bit of redundancy is used in each one of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The differential input stage is dc self-biased and allows differential or single-ended inputs. The output-staging block aligns the data, carries out the error correction, and passes the data to the output buffers.

The latency of the Rx path is about 5 clock cycles.

Rx Path Analog Input Equivalent Circuit

The Rx path analog inputs of the AD9861 incorporate a novel structure that merges the function of the input sample-and-hold amplifiers (SHAs) and the first pipeline residue amplifiers into a single, compact switched capacitor circuit. This structure achieves considerable noise and power savings over a conventional implementation that uses separate amplifiers by eliminating one amplifier in the pipeline.

Figure 70 illustrates the equivalent analog inputs of the AD9861 (a switched capacitor input). Bringing CLK to logic high opens switch S3 and closes switches S1 and S2; this is the sample mode of the input circuit. The input source connected to VIN+ and VIN− must charge capacitor C_H during this time. Bringing CLK to a logic low opens S2, and then switch S1 opens followed by closing S3. This puts the input circuit into hold mode.

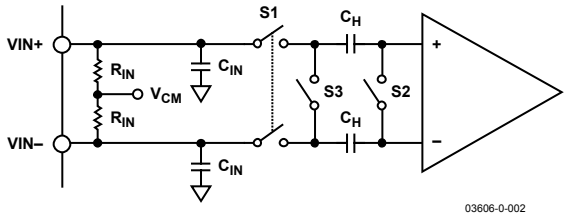

Figure 70. Differential Input Architecture

The structure of the input SHA places certain requirements on the input drive source. The differential input resistors are typically 2 kΩ each. The combination of the pin capacitance, C_{IN}, and the hold capacitance, C_H, is typically less than 5 pF. The input source must be able to charge or discharge this capacitance to 10-bit accuracy in one-half of a clock cycle. When the SHA goes into sample mode, the input source must charge or discharge capacitor C_H from the voltage already stored on it to the new voltage. In the worst case, a full-scale voltage step on the input source must provide the charging current through the R_{ON} of switch S1 (typically 100 Ω) to a settled voltage within one-half of the ADC sample period. This situation corresponds to driving a low input impedance. On the other hand, when the source voltage equals the value previously stored on C_H, the hold capacitor requires no input current and the equivalent input impedance is extremely high.

Rx Path Application Section

Adding series resistance between the output of the signal source and the VIN pins reduces the drive requirements placed on the signal source. Figure 71 shows this configuration.

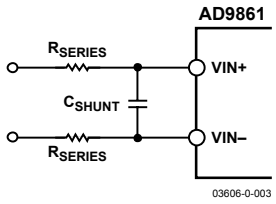

Figure 71. Typical Input

The bandwidth of the particular application limits the size of this resistor. For applications with signal bandwidths less than 10 MHz, the user may insert series input resistors and a shunt capacitor to produce a low-pass filter for the input signal. Additionally, adding a shunt capacitance between the VIN pins can lower the ac load impedance. The value of this capacitance depends on the source resistance and the required signal bandwidth.

The Rx input pins are self-biased to provide this midsupply, common-mode bias voltage, so it is recommended to ac couple the signal to the inputs using dc blocking capacitors. In systems that must use dc coupling, use an op amp to comply with the input requirements of the AD9861. The inputs accept a signal with a 2 V p-p differential input swing centered about one-half of the supply voltage (AVDD/2). If the dc bias is supplied externally, the internal input bias circuit must be powered down by writing to registers Rx_A dc bias [Register 0x3, Bit 6] and Rx_B dc bias [Register 0x4, Bit 7].

The ADCs in the AD9861 are designed to sample differential input signals. The differential input provides improved noise immunity and better THD and SFDR performance for the Rx path. In systems that use single-ended signals, these inputs can be digitized, but it is recommended that a single-ended-to-differential conversion be performed. A single-ended-to-differential conversion can be performed by using a transformer coupling circuit (typically for signals above 10 MHz) or by using an operational amplifier, such as the AD8138 (typically for signals below 10 MHz).

ADC Voltage References

The AD9861 10-bit ADCs use internal references that are designed to provide for a 2 V p-p differential input range. The internal band gap reference generates a stable 1 V reference level and is decoupled through the VREF pin. REFT and REFB are the differential references generated based on the voltage level of VREF. Figure 72 shows the proper decoupling of the reference pins VREF, REFT, and REFB when using the internal reference. Decoupling capacitors must be placed as close to the reference pins as possible.

External references REFT and REFB are centered at AVDD/2 with a differential voltage equal to the voltage at VREF (by default 1 V when using the internal reference), allowing a peak-to-peak differential voltage swing of 2× VREF. For example, the default 1 V VREF reference accepts a 2 V p-p differential input swing and the offset voltage must be

$$REFT = AVDD/2 + 0.5\ V$$
$$REFB = AVDD/2 - 0.5\ V$$

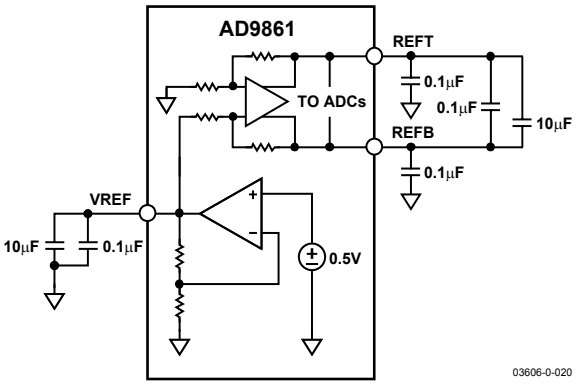

Figure 72. Typical Rx Path Decoupling

An external reference may be used for systems that require a different input voltage range, high accuracy gain matching between multiple devices, or improvements in temperature drift and noise characteristics. When an external reference is desired, the internal Rx band gap reference must be powered down using the VREF2 register [Register 0x5, Bit 4] and the external reference driving the voltage level on the VREF pin. The external voltage level must be one-half of the desired peak-to-peak differential voltage swing. The result is that the differential voltage references are driven to new voltages:

$$REFT = AVDD/2 + V_{REF}/2\ V$$
$$REFB = AVDD/2 - V_{REF}/2\ V$$

If an external reference is used, it is recommended not to exceed a differential offset voltage for the reference greater than 1 V.

Clock Input and Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9861 contains clock duty cycle stabilizer circuitry (DCS). The DCS retimes the internal ADC clock (nonsampling edge) and provides the ADC with a nominal 50% duty cycle. Input clock rates of over 40 MHz can use the DCS so that a wide range of input clock duty cycles can be accommodated. Conversely, DCS must not be used for Rx sampling below 40 MSPS. Maintaining a 50% duty cycle clock is particularly important in high speed applications when proper sample-and-hold times for the converter are required to maintain high performance. The DCS can be enabled by writing highs to the Rx_A/Rx_B CLK duty register bits [Register 0x06/0x07, Bit 4].

The duty cycle stabilizer uses a delay-locked loop to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately 2 µs to 3 µs to allow the DLL to adjust to the new rate and settle. High speed, high resolution ADCs are sensitive to the quality of the clock input.

The degradation in SNR at a given full-scale input frequency (f_{INPUT}), due only to aperture jitter (t_A), can be calculated with the following equation:

$$SNR\ degradation = 20 \log [(½)\pi F_{IN} t_A)]$$

In the equation, the rms aperture jitter, t_A, represents the root-sum-square of all jitter sources, which includes the clock input, analog input signal, and ADC aperture jitter specification. Undersampling applications are particularly sensitive to jitter. The clock input is a digital signal that must be treated as an analog signal with logic level threshold voltages, especially in cases where aperture jitter may affect the dynamic range of the AD9861. Power supplies for clock drivers must be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it must be retimed by the original clock at the last step.

Power Dissipation and Standby Mode

The power dissipation of the AD9861 Rx path is proportional to its sampling rate. The Rx path portion of the digital (DRVDD) power dissipation is determined primarily by the strength of the digital drivers and the load on each output bit. The digital drive current can be calculated by

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times f_{CLOCK} \times N$$

where N is the number of bits changing and C_{LOAD} is the average load on the digital pins that changed.

The analog circuitry is optimally biased so that each speed grade provides excellent performance while affording reduced power consumption. Each speed grade dissipates a baseline power at low sample rates, which increases with clock frequency. The baseline power dissipation for either speed grade can be reduced by asserting the ADC_LO_PWR pin, which reduces internal ADC bias currents by half, in some case resulting in degraded performance.

To further reduce power consumption of the ADC, the ADC_LO_PWR pin can be combined with a serial programmable register setting to configure an ultralow power mode. The ultralow power mode reduces the power consumption by a fourth of the normal power consumption. The ultralow power mode can be used at slower sampling frequencies or if reduced performance is acceptable. To configure the ultralow power mode, assert the ADC_LO_PWR pin and write the following register settings:

Register 0x08 (MSB) '0000 1100'
Register 0x09 (MSB) '0111 0000'
Register 0x0A (MSB) '0111 0000'

Either of the ADCs in the AD9861 Rx path can be placed in standby mode independently by writing to the appropriate SPI register bits in Registers 3, 4, and 5. The minimum standby power is achieved when both channels are placed in full power-down mode using the appropriate SPI register bits in Registers 3, 4, and 5. Under this condition, the internal references are powered down.

When either or both of the channel paths are enabled after a power-down, the wake-up time is directly related to the recharging of the REFT and REFB decoupling capacitors and the duration of the power-down. Typically, it takes approximately 5 ms to restore full operation with fully discharged 0.1 µF and 10 µF decoupling capacitors on REFT and REFB.

Tx PATH BLOCK

The AD9861 transmit (Tx) path includes dual interpolating 10-bit current output DACs that can be operated independently or can be coupled to form a complex spectrum in an image reject transmit architecture. Each channel includes two FIR filters, making the AD9861 capable of 1×, 2×, or 4× interpolation. High speed input and output data rates can be achieved within the limitations of Table 9.

Table 9. AD9861 Tx Path Maximum Data Rate

Interpolation Rate	20-Bit Interface Mode	Input Data Rate per Channel (MSPS)	DAC Sampling Rate (MSPS)
1×	FD, HD10, Clone	80	80
	HD20	160	160
2×	FD, HD10, Clone	80	160
	HD20	80	160
4×	FD, HD10, Clone	50	200
	HD20	50	200

By using the dual DAC outputs to form a complex signal, an external analog quadrature modulator, such as the Analog Devices AD8349, can enable an image rejection architecture. (Note: the AD9861 evaluation board includes a quadrature modulator in the Tx path that accommodates the AD8345, AD8346 and the AD8345 footprints.) To optimize the image rejection capability, as well as LO feedthrough suppression in this architecture, the AD9861 offers programmable (via the SPI port) fine (trim) gain and offset adjustment for each DAC.

Also included in the AD9861 are a phase-locked loop (PLL) clock multiplier and a 1.2 V band gap voltage reference. With the PLL enabled, a clock applied to the CLKIN input is multiplied internally and generates all necessary internal synchronization clocks. Each 10-bit DAC provides two complementary current outputs whose full-scale currents can be determined from a single external resistor.

An external pin, TxPWRDWN, can be used to power down the Tx path, when not used, to optimize system power consumption. Using the TxPWRDWN pin disables clocks and some analog circuitry, saving both digital and analog power. The power-down mode leaves the biases enabled to facilitate a quick recovery time, typically <10 µs. Additionally, a sleep mode is available, which turns off the DAC output current, but leaves all other circuits active, for a modest power savings. An SPI compliant serial port is used to program the many features of the AD9861. Note that in power-down mode, the SPI port is still active.