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FEATURES

- Receive path includes dual 12-bit, 50 MSPS analog-to-digital converters with internal or external reference
- Transmit path includes dual 12-bit, 200 MSPS digital-to-analog converters with 1×, 2×, or 4× interpolation and programmable gain control
- Internal clock distribution block includes a programmable phase-locked loop and timing generation circuitry, allowing single-reference clock operation
- 24-pin flexible I/O data interface allows various interleaved or noninterleaved data transfers in half-duplex mode and interleaved data transfers in full-duplex mode
- Configurable through register programmability or optionally limited programmability through mode pins
- Independent Rx and Tx power-down control pins
- 64-lead LFCSP package (9 mm × 9 mm footprint)

APPLICATIONS

- Broadband access
- Broadband LAN
- Communications (modems)

GENERAL DESCRIPTION

The AD9863 is a member of the MxFE family—a group of integrated converters for the communications market. The AD9863 integrates dual 12-bit analog-to-digital converters (ADC) and dual 12-bit digital-to-analog converters (TxDAC®). The AD9863 ADCs are optimized for ADC sampling of 50 MSPS and less. The dual TxDACs operate at speeds up to 200 MHz and include a bypassable 2× or 4× interpolation filter. The AD9863 is optimized for high performance, low power, and small form factor to provide a cost-effective solution for the broadband communications market.

The AD9863 uses a single input clock pin (CLKIN) or two independent clocks for the Tx path and the Rx path. The ADC and TxDAC clocks are generated within a timing generation block that provides user programmable options such as divide circuits, PLL multipliers, and switches.

A flexible, bidirectional 24-bit I/O bus accommodates a variety of custom digital back ends or open market DSPs.

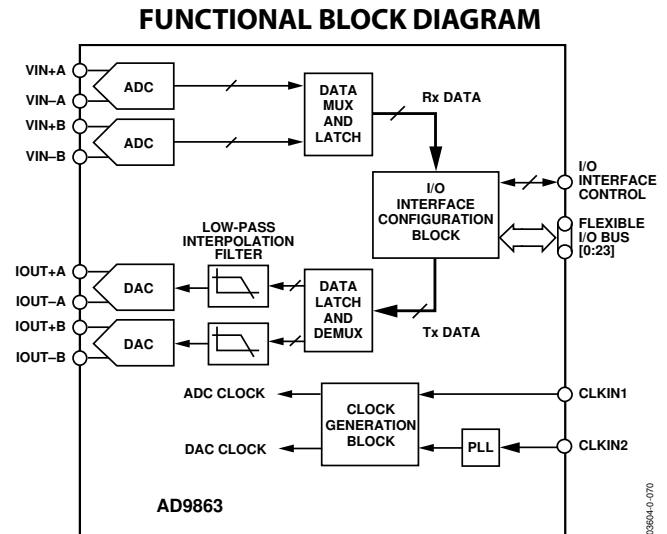


Figure 1.

In half-duplex systems, the interface supports 24-bit parallel transfers or 12-bit interleaved transfers. In full-duplex systems, the interface supports a 12-bit interleaved ADC bus and a 12-bit interleaved TxDAC bus. The flexible I/O bus reduces pin count, also reducing the required package size on the AD9863 and the device to which it connects.

The AD9863 can use either mode pins or a serial programmable interface (SPI) to configure the interface bus, operate the ADC in a low power mode, configure the TxDAC interpolation rate, and control ADC and TxDAC power-down. The SPI provides more programmable options for both the TxDAC path (for example, coarse and fine gain control and offset control for channel matching) and the ADC path (for example, the internal duty cycle stabilizer and twos complement data format).

The AD9863 is packaged in a 64-lead LFCSP (low profile, fine pitched, chip scale package). The 64-lead LFCSP footprint is only 9 mm × 9 mm and is less than 0.9 mm high, fitting into such tightly spaced applications as PCMCIA cards.

AD9863* PRODUCT PAGE QUICK LINKS

Last Content Update: 04/29/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD-DAC-FMC-ADP
- AD9861/AD9863 Evaluation Tools

DOCUMENTATION

Application Notes

- AN-808: Multicarrier CDMA2000 Feasibility
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design
- AN-928: Understanding High Speed DAC Testing and Evaluation

Data Sheet

- AD9863 12-Bit Mixed-Signal Front-End (MxFE™) Baseband Transceiver For Broadband Applications Data Sheet

TOOLS AND SIMULATIONS

- AD9863 IBIS Models

REFERENCE MATERIALS

Informational

- Advantiv™ Advanced TV Solutions

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9863 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9863 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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REVISION HISTORY

4/2017—Rev. A to Rev. B

Changes to Figure 3 and Table 8.....	8
Updated Outline Dimensions	42
Changes to Ordering Guide	42

4/2005—Rev. 0 to Rev. A

Changes to Ordering Guide	40
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11/2003—Revision 0: Initial Version

Tx PATH SPECIFICATIONS

FDAC = 200 MSPS; 4× interpolation; RSET = 4.02 kΩ; differential load resistance of 100 Ω¹; TxPGA = 20 dB; AVDD = DVDD = 3.3 V, unless otherwise noted.

Table 1.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
Tx PATH GENERAL						
Resolution	Full	IV		12		Bits
Maximum DAC Update Rate	Full	IV	200			MHz
Maximum Full-Scale Output Current	Full	IV	20			mA
Full-Scale Error	Full	V		1%		
Gain Mismatch Error	25°C	IV	-3.5		+3.5	% FS
Offset Mismatch Error	Full	IV	-0.1		+0.1	% FS
Reference Voltage	Full	V		1.23		V
Output Capacitance	Full	V		5		pF
Phase Noise (1 kHz Offset, 6 MHz Tone)	25°C	V		-115		dBc/Hz
Output Voltage Compliance Range	Full	IV	-1.0		+1.0	V
TxPGA Gain Range	Full	V		20		dB
TxPGA Step Size	Full	V		0.10		dB
Tx PATH DYNAMIC PERFORMANCE (I _{OUTFS} = 20 mA; F _{OUT} = 1 MHz)						
SNR	Full	IV	70.8	71.6		dB
SINAD	Full	IV	64.3	71		dB
THD	Full	IV		-79	-66.3	dBc
SFDR, Wide Band (DC to Nyquist)	Full	IV	68.5	77		dBc
SFDR, Narrow Band (1 MHz Window)	Full	IV	72.8	81		dBc

¹ See Figure 2 for description of the TxDAC termination scheme.

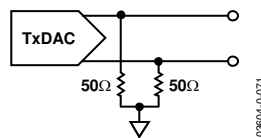


Figure 2. Diagram Showing Termination of 100 Ω Differential Load for Some TxDAC Measurements

RX PATH SPECIFICATIONS

$F_{ADC} = 50$ MSPS; internal reference; differential analog inputs, $ADC_AVDD = DVDD = 3.3$ V, unless otherwise noted.

Table 2.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
Rx PATH GENERAL						
Resolution	Full	V		12		Bits
Maximum ADC Sample Rate	Full	IV	50			MSPS
Gain Mismatch Error	Full	V		± 0.2		% FS
Offset Mismatch Error	Full	V		± 0.1		% FS
Reference Voltage	Full	V		1.0		V
Reference Voltage (REFT-REFB) Error	Full	IV	-30	± 6	+30	mV
Input Resistance (Differential)	Full	V		2		k Ω
Input Capacitance	Full	V		5		pF
Input Bandwidth	Full	V		30		MHz
Differential Analog Input Voltage Range	Full	V		2		V p-p differential
Rx PATH DC ACCURACY						
Integral Nonlinearity (INL)	25°C	V		± 0.75		LSB
Differential Nonlinearity (DNL)	25°C	V		± 0.75		LSB
Aperture Delay	25°C	V		2.0		ns
Aperture Uncertainty (Jitter)	25°C	V		1.2		ps rms
Input Referred Noise	25°C	V		250		μ V
AD9863 Rx PATH DYNAMIC PERFORMANCE ($V_{IN} = -0.5$ dBFS; $F_{IN} = 10$ MHz)						
SNR	Full	V		67		dBc
SINAD	Full	V		65.5		dBc
THD (Second to Ninth Harmonics)	Full	IV		-73	-66.6	dBc
SFDR, Wide Band (DC to Nyquist)	Full	IV	68.3	74		dBc
Crosstalk Between ADC Inputs	Full	V		80		dB

POWER SPECIFICATIONS

Analog and digital supplies = 3.3 V; $F_{CLKIN1} = F_{CLKIN2} = 50$ MHz; PLL 4× setting; normal timing mode.

Table 3.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
POWER SUPPLY RANGE						
Analog Supply Voltage (AVDD)	Full	IV	2.7		3.6	V
Digital Supply Voltage (DVDD)	Full	IV	2.7		3.6	V
Driver Supply Voltage (DRVDD)	Full	IV	2.7		3.6	V
ANALOG SUPPLY CURRENTS						
Tx Path (20 mA Full-Scale Outputs)	Full	V		70		mA
Tx Path (2 mA Full-Scale Outputs)	Full	V		20		mA
Rx Path (50 MSPS)	Full	V		103		mA
Rx Path (50 MSPS, Low Power Mode)	Full	V		69		mA
Rx Path (20 MSPS, Low Power Mode)	Full	V		55		mA
Tx Path, Power-Down Mode	Full	V		2		mA
Rx Path, Power-Down Mode	Full	V		5		mA
PLL	Full	V		12		mA
DIGITAL SUPPLY CURRENTS						
Tx Path, 1× Interpolation, 50 MSPS DAC Update for Both DACs, Half-Duplex 24 Mode	Full	V		20		mA
Tx Path, 2× Interpolation, 100 MSPS DAC Update for Both DACs, Half-Duplex 24 Mode	Full	V		50		mA
Tx Path, 4× Interpolation, 200 MSPS DAC Update for Both DACs, Half-Duplex 24 Mode	Full	V		80		mA
Rx Path Digital, Half-Duplex 24 Mode	Full	V		15		mA

DIGITAL SPECIFICATIONS

Table 4.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
LOGIC LEVELS						
Input Logic High Voltage, V_{IH}	Full	IV	DRVDD – 0.7			V
Input Logic Low Voltage, V_{IL}	Full	IV			0.4	V
Output Logic High Voltage, V_{OH} (1 mA Load)	Full	IV	DRVDD – 0.6			V
Output Logic Low Voltage, V_{OL} (1 mA Load)	Full	IV			0.4	V
DIGITAL PIN						
Input Leakage Current	Full	IV			12	μA
Input Capacitance	Full	IV		3		pF
Minimum RESET Low Pulse Width	Full	IV	5			Input clock cycles
Digital Output Rise/Fall Time	Full	IV	2.8		4	ns

TIMING SPECIFICATIONS

Table 5.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
INPUT CLOCK						
CLKIN2 Clock Rate (PLL Bypassed)	Full	IV	1		200	MHz
PLL Input Frequency	Full	IV	16		200	MHz
PLL Output Frequency	Full	IV	32		350	MHz
TxPATH DATA						
Setup Time (HD24 Mode, Time Required Before Data Latching Edge)	Full	V		5		ns (see Clock Distribution Block section)
Hold Time (HD24 Mode, Time Required After Data Latching Edge)	Full	V		-1.5		ns (see Clock Distribution Block section)
Latency 1x Interpolation (Data In Until Peak Output Response)	Full	V		7		DAC clock cycles
Latency 2x Interpolation (Data In Until Peak Output Response)	Full	V		35		DAC clock cycles
Latency 4x Interpolation (Data In Until Peak Output Response)	Full	V		83		DAC clock cycles
RxPATH DATA						
Output Delay (HD24 Mode, t_{OD})	Full	V		-1.5		ns (see Clock Distribution Block section)
Latency	Full	V		5		ADC clock cycles

Table 6. Explanation of Test Levels

Level	Description
I	100% production tested.
II	100% production tested at 25°C and guaranteed by design and characterization at specified temperatures.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	100% production tested at 25°C and guaranteed by design and characterization for industrial temperature range.

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Electrical	
AVDD Voltage	3.9 V max
DRVDD Voltage	3.9 V max
Analog Input Voltage	-0.3 V to AVDD + 0.3 V
Digital Input Voltage	-0.3 V to DVDD - 0.3 V
Digital Output Current	5 mA max
Environmental	
Operating Temperature Range (Ambient)	-40°C to +85°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range (Ambient)	-65°C to +150°C

THERMAL RESISTANCE

64-lead LFCSP (4-layer board):

$$\theta_{JA} = 24.2 \text{ (paddle soldered to ground plan, 0 LPM air)}$$

$$\theta_{JA} = 30.8 \text{ (paddle not soldered to ground plan, 0 LPM air)}$$

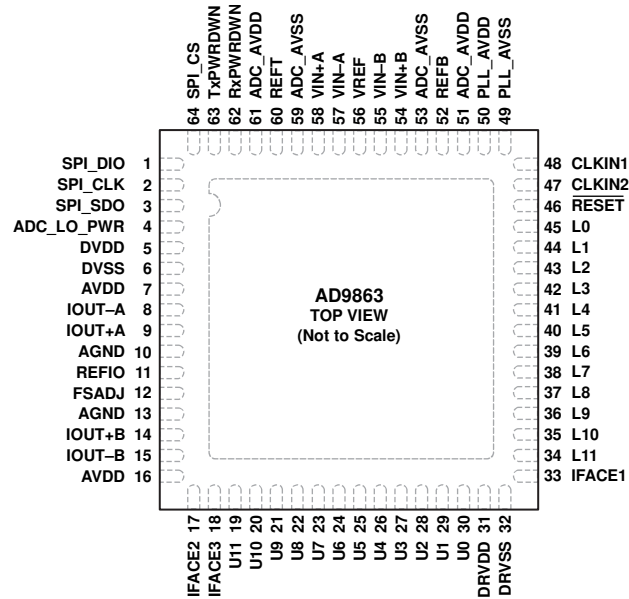
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. EXPOSED PAD. THE EXPOSED PAD MUST BE SECURELY CONNECTED TO THE GROUND PLANE.

03804-0-072

Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Name ¹	Description ^{2,3}
1	SPI_DIO (Interp1)	SPI: Serial Port Data Input. No SPI: Tx Interpolation Pin, MSB.
2	SPI_CLK (Interp0)	SPI: Serial Port Shift Clock. No SPI: Tx Interpolation Pin, LSB.
3	SPI_SDO (FD/HD)	SPI: 4-Wire Serial Port Data Output. No SPI: Configures Full-Duplex or Half-Duplex Mode.
4	ADC_LO_PWR	ADC Low Power Mode Enable. Defined at power-up.
5, 31	DVDD, DRVDD	Digital Supply.
6, 32	DVSS, DRVDD	Digital Ground.
7, 16, 50, 51, 61	AVDD	Analog Supply.
8, 9	IOUT-A, IOUT+A	DAC A Differential Output.
10, 13, 49, 53, 59	AGND, AVSS	Analog Ground.
11	REFIO	Tx DAC Band Gap Reference Decoupling Pin.
12	FSADJ	Tx DAC Full-Scale Adjust Pin.
14, 15	IOUT+B, IOUT-B	DAC B Differential Output.
17	IFACE2 (12/24)	SPI: Buffered CLKIN. Can be configured as system clock output. No SPI: Buffered CLKIN for FD; 12/24 configuration pin for HD24 or HD12.
18	IFACE3	Clock Output.
19 to 30	U11 to U0	Upper Data Bit 11 to Upper Data Bit 0.
33	IFACE1	SPI: TxSYNC for FD; Tx/Rx for HD24, HD12, or clone. No SPI: FD >> TxSYNC; HD24 or HD12: Tx/Rx. Clone mode requires a serial port interface.
34 to 45	L11 to L0	Lower Data Bit 11 to Lower Data Bit 0.
46	RESET	Chip Reset When Low.
47	CLKIN2	Clock Input 2.
48	CLKIN1	Clock Input 1.
52	REFB	ADC Bottom Reference.
54, 55	VIN+B, VIN-B	ADC B Differential Input.

Pin No.	Name ¹	Description ^{2,3}
56	VREF	ADC Band Gap Reference.
57, 58	VIN–A, VIN+A	ADC A Differential Input.
60	REFT	ADC Top Reference.
62	RxPWRDWN	Rx Analog Power-Down Control.
63	TxPWRDWN	Tx Analog Power-Down Control.
64	SPI_CS	SPI: Serial Port Chip Select. At power-up or reset, this must be high. No SPI: Tie low to disable SPI and use mode pins. This pin must be tied low.
	EPAD	Exposed Pad. The exposed pad must be securely connected to the ground plane.

¹ Underlined pin names and descriptions apply when the device is configured without a serial port interface, referred to as No SPI mode.

² Some pin descriptions depend on whether a serial port is used (SPI mode) or not (No SPI mode), indicated by the labels SPI and No SPI.

³ Some pin descriptions depend on the interface configuration: full-duplex (FD), half-duplex interleaved data (HD12), half-duplex parallel data (HD24), and a half-duplex interface similar to the AD9860 and AD9862 data interface called clone mode (Clone). Clone mode requires a serial port interface.

TYPICAL PERFORMANCE CHARACTERISTICS

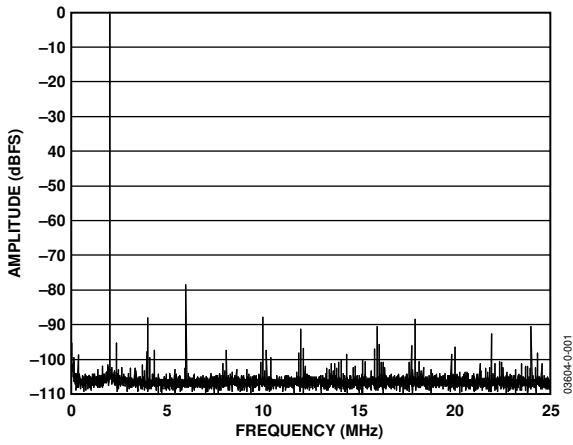


Figure 4. AD9863 Rx Path Single-Tone FFT of Rx Channel B Path Digitizing 2 MHz Tone

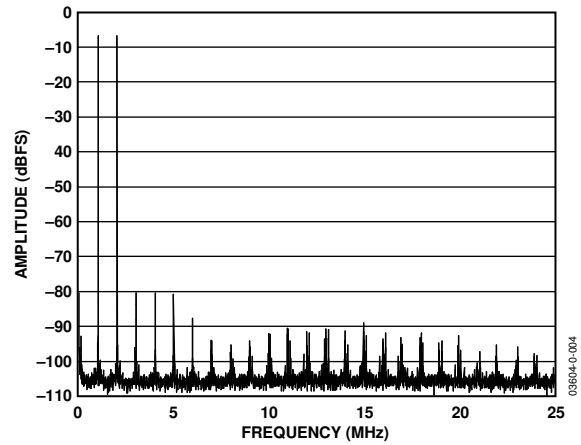


Figure 7. AD9863 Rx Path Dual-Tone FFT of Rx Channel A Path Digitizing 1 MHz and 2 MHz Tones

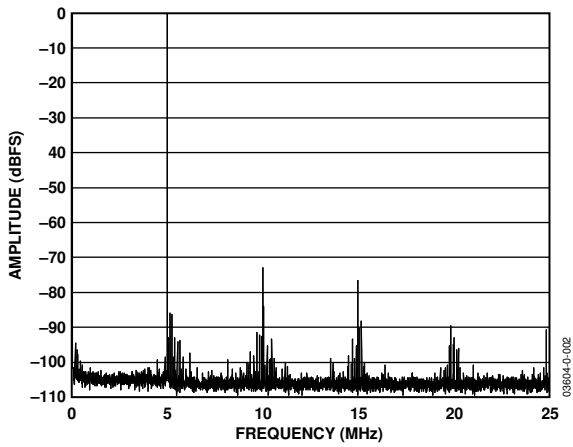


Figure 5. AD9863 Rx Path Single-Tone FFT of Rx Channel B Path Digitizing 5 MHz Tone

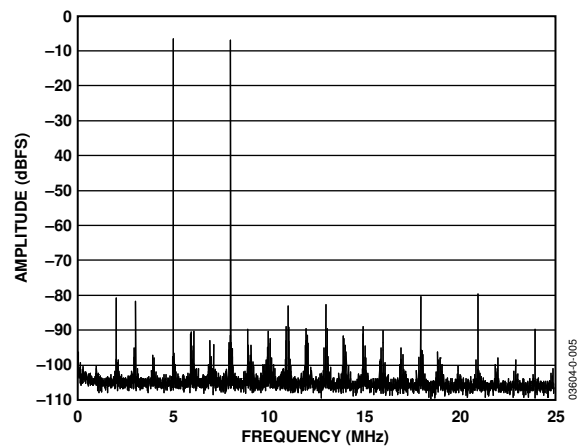


Figure 8. AD9863 Rx Path Dual-Tone FFT of Rx Channel A Path Digitizing 5 MHz and 8 MHz Tones

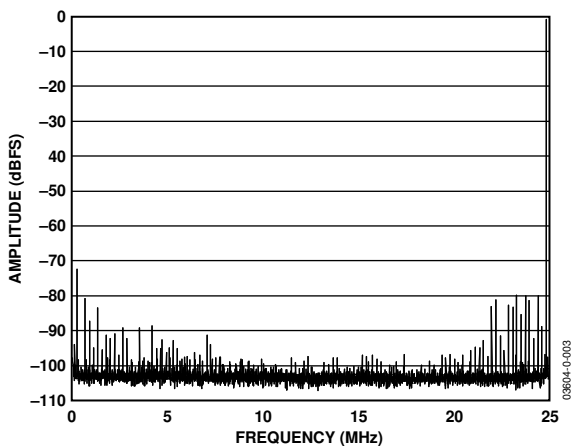


Figure 6. AD9863 Rx Path Single-Tone FFT of Rx Channel B Path Digitizing 24 MHz Tone

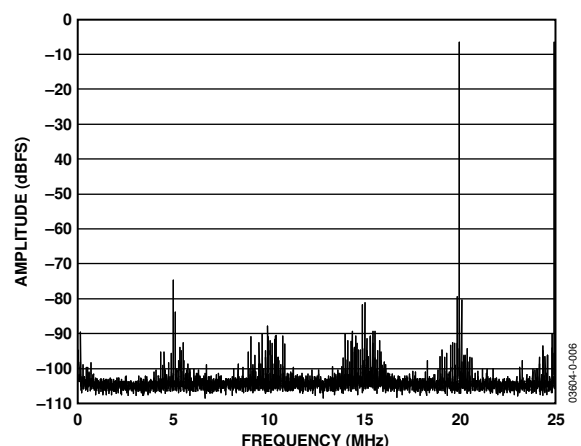


Figure 9. AD9863 Rx Path Dual-Tone FFT of Rx Channel A Path Digitizing 20 MHz and 25 MHz Tones

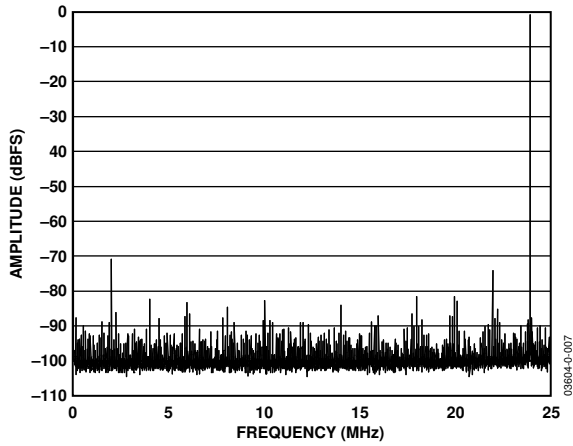


Figure 10. AD9863 Rx Path Single-Tone FFT of Rx Channel B Path Digitizing 76 MHz Tone

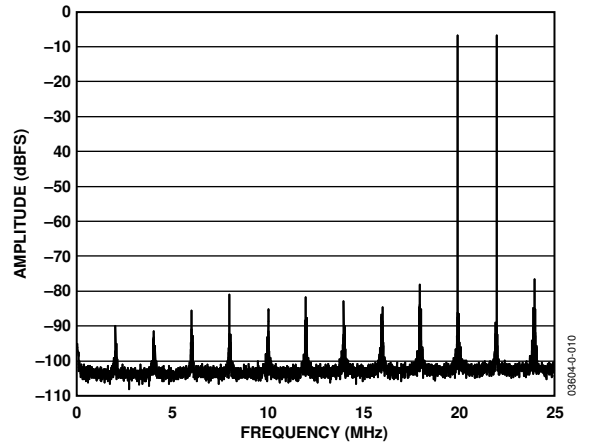


Figure 13. AD9863 Rx Path Dual-Tone FFT of Rx Channel A Path Digitizing 70 MHz and 72 MHz Tones

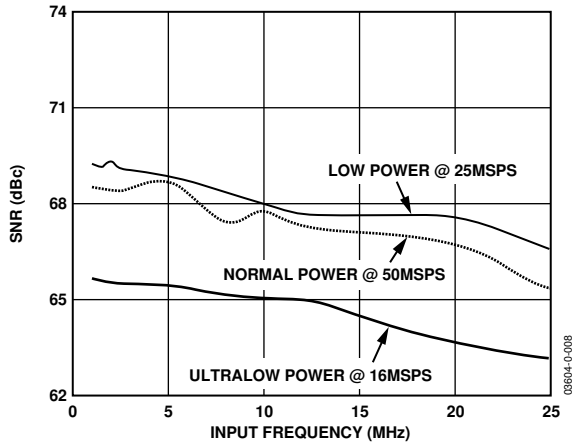


Figure 11. AD9863 Rx Path at 50 MSPS, 10 MHz Input Tone SNR Performance vs. Input Frequency

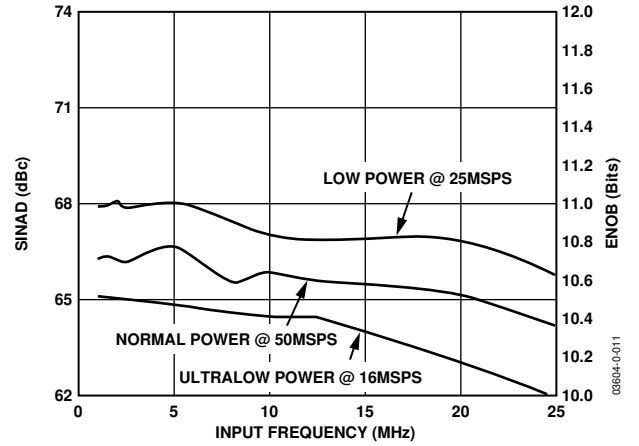


Figure 14. AD9863 Rx Path at 50 MSPS, 10 MHz Input Tone SINAD Performance vs. Input Frequency

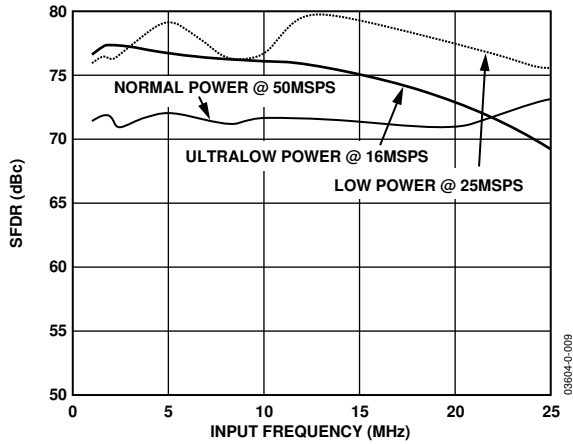


Figure 12. AD9863 Rx Path at 50 MSPS, 10 MHz Input Tone SFDR Performance vs. Input Frequency

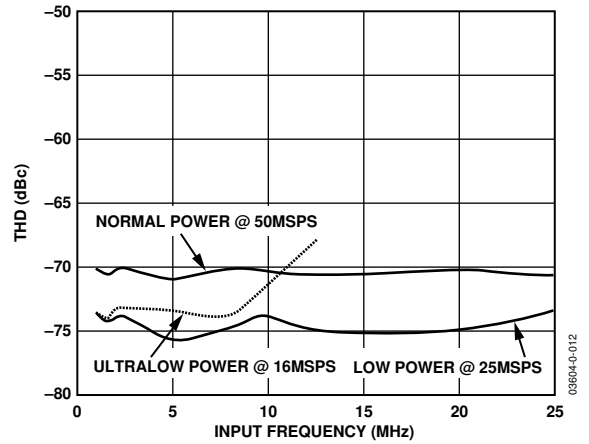


Figure 15. AD9863 Rx Path at 50 MSPS, 10 MHz Input Tone THD Performance vs. Input Frequency

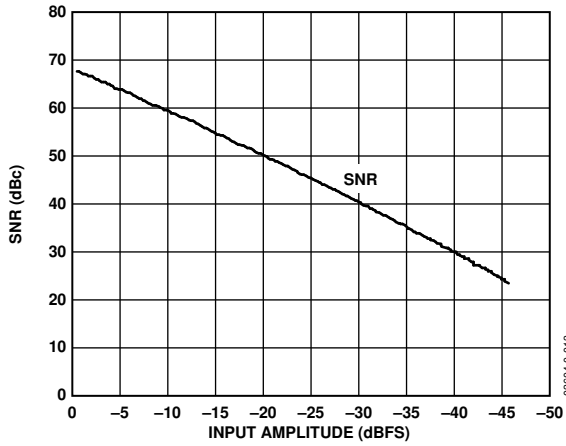


Figure 16. AD9863 Rx Path at 50 MSPS, 10 MHz Input Tone SNR Performance vs. Input Amplitude

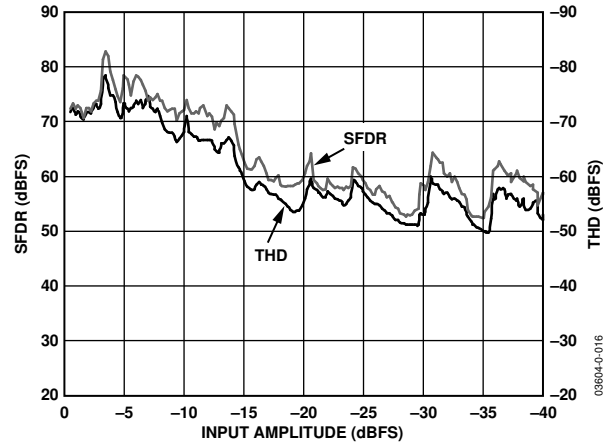


Figure 19. AD9863 Rx Path at 50 MSPS, 10 MHz Input Tone THD and SFDR Performance vs. Input Amplitude

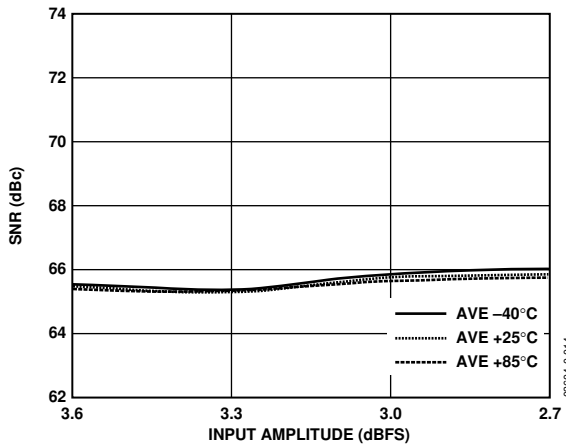


Figure 17. AD9863 Rx Path at 50 MSPS, 10 MHz Input Tone SNR Performance vs. ADC_AVDD and Temperature

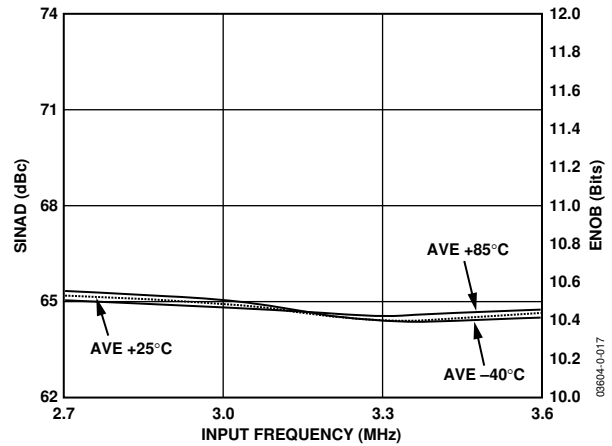


Figure 20. AD9863 Rx Path at 50 MSPS, 10 MHz Input Tone SINAD Performance vs. ADC_AVDD and Temperature

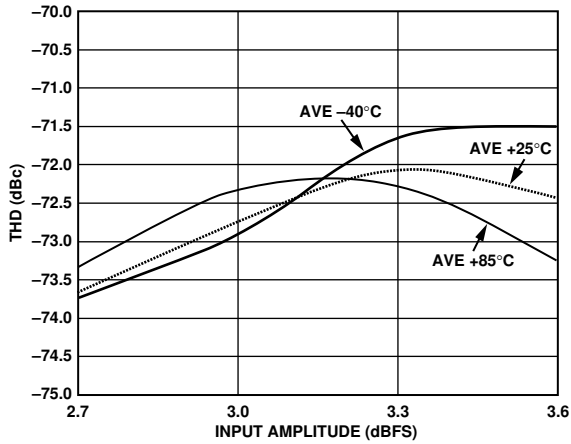


Figure 18. AD9863 Rx Path Single-Tone THD Performance vs. ADC_AVDD and Temperature

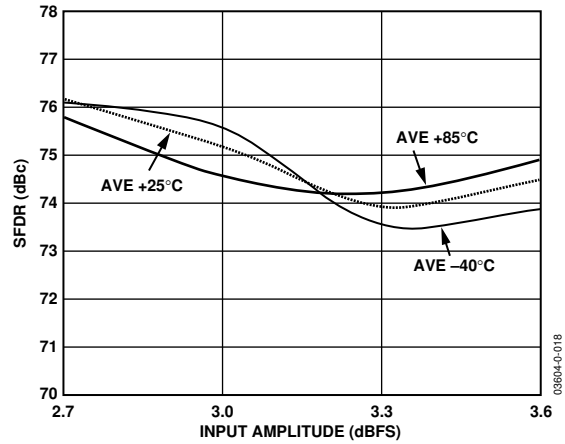


Figure 21. AD9863 Rx Path Single-Tone SFDR Performance vs. ADC_AVDD and Temperature

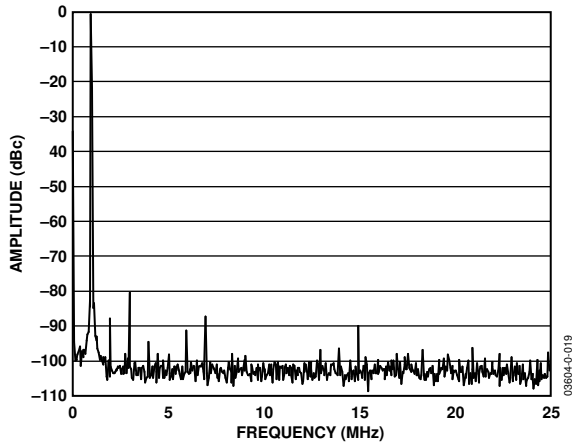


Figure 22. AD9863 Tx Path 1 MHz Single-Tone Output FFT of Tx Path with 20 mA Full-Scale Output into 33 Ω Differential Load

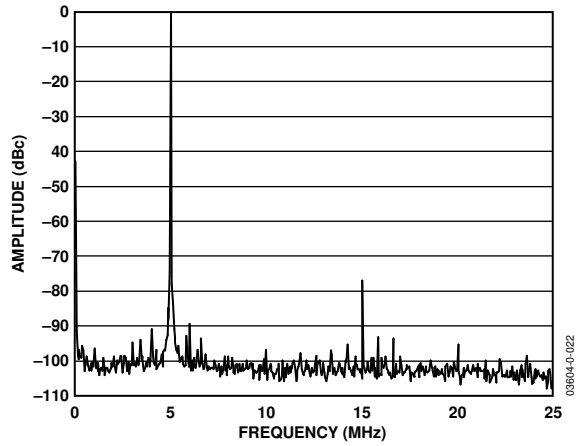


Figure 25. AD9863 Tx Path 5 MHz Single-Tone Output FFT of Tx Channel A with 20 mA Full-Scale Output into 33 Ω Differential Load

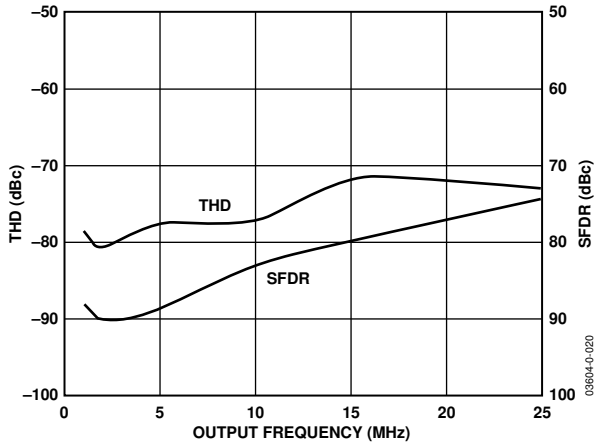


Figure 23. AD9863 Tx Path THD/SFDR vs. Output Frequency of Tx Channel A, with 20 mA Full-Scale Output into 60 Ω Differential Load

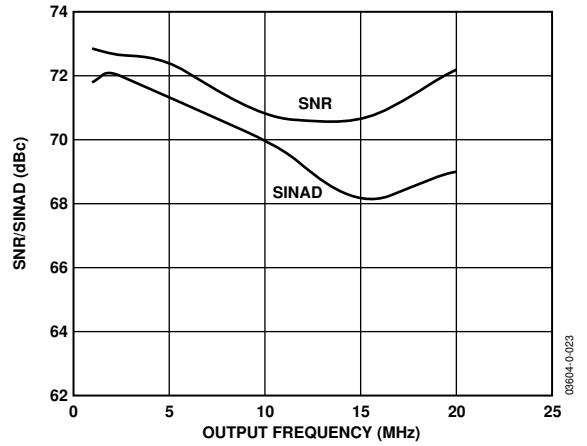


Figure 26. AD9863 Tx Path SINAD/SNR vs. Output Frequency of Tx Path with 20 mA Full-Scale Output into 60 Ω Differential Load

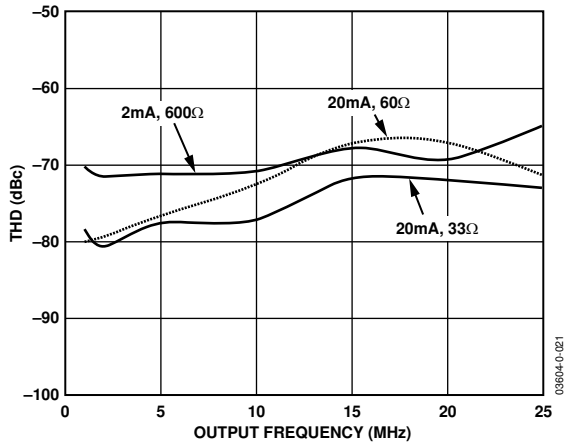


Figure 24. AD9863 Tx Path THD vs. Output Frequency of Tx Channel A

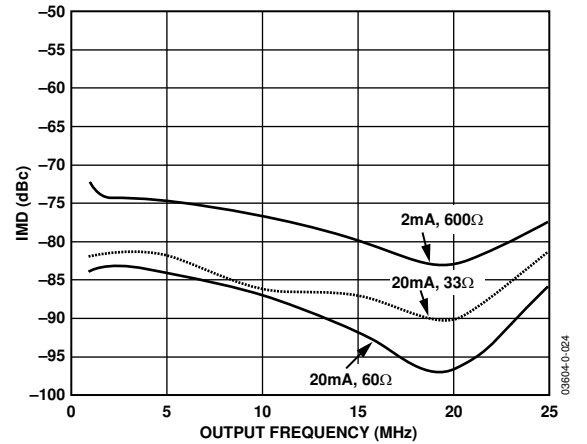


Figure 27. AD9863 Tx Path Dual-Tone (0.5 MHz Spacing) IMD vs. Output Frequency

Figure 28 to Figure 33 use the same input data to the Tx path, a 64-carrier OFDM signal over a 20 MHz bandwidth, centered at 20 MHz. The two center carriers are removed from the signal to observe the in-band intermodulation distortion (IMD) from the DAC output.

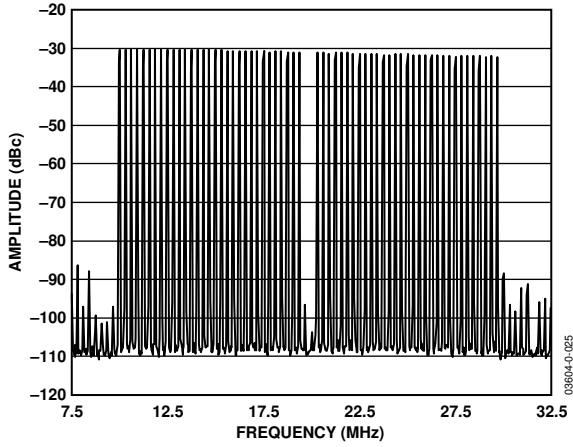


Figure 28. AD9863 Tx Path FFT, 64-Carrier (Two Center Carriers Removed) OFDM Signal over 20 MHz Bandwidth, Centered at 20 MHz, with 20 mA Full-Scale Output into 60 Ω Differential Load

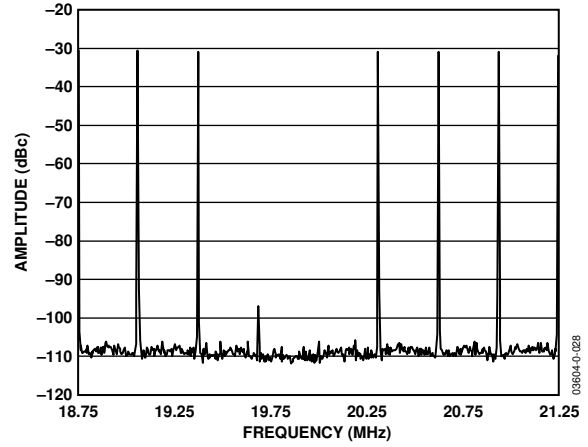


Figure 31. AD9863 Tx Path FFT, In-Band IMD Products of OFDM Signal in Figure 28

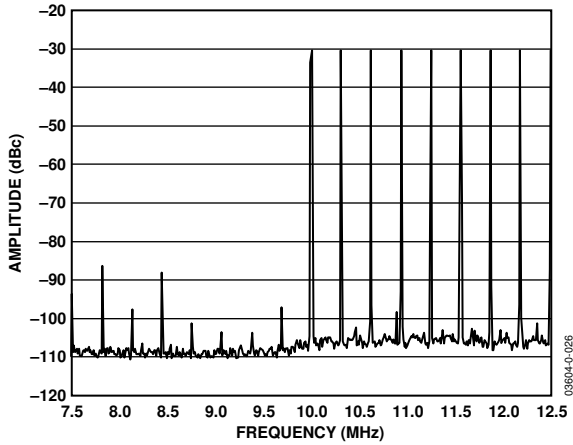


Figure 29. AD9863 Tx Path FFT, Lower-Band IMD Products of OFDM Signal in Figure 28

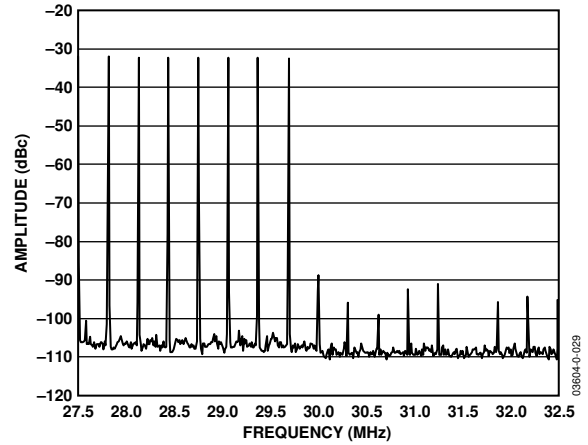


Figure 32. AD9863 Tx Path FFT, Lower-Band IMD Products of OFDM Signal in Figure 28

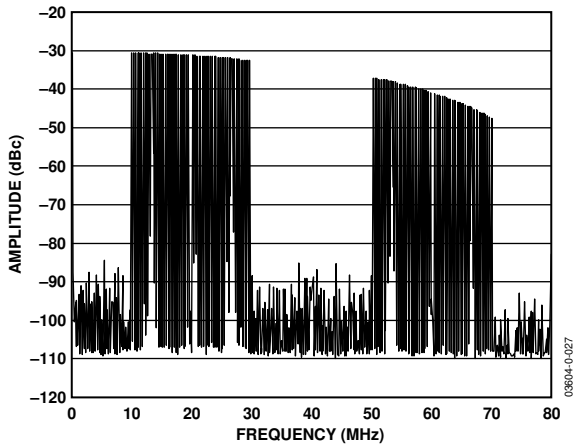


Figure 30. AD9863 Tx Path FFT of OFDM Signal in Figure 28 with 1x Interpolation

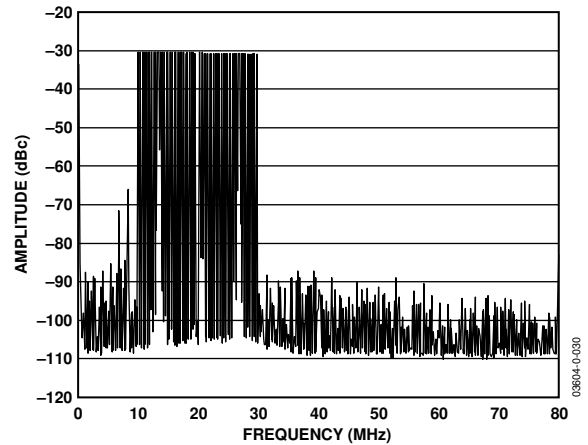


Figure 33. AD9863 Tx Path FFT of OFDM Signal in Figure 28 with 2x Interpolation

Figure 34 to Figure 39 use the same input data to the Tx path, a 256-carrier OFDM signal over a 1.75 MHz bandwidth, centered at 7 MHz. The four center carriers are removed from the signal to observe the in-band intermodulation distortion (IMD) from the DAC output.

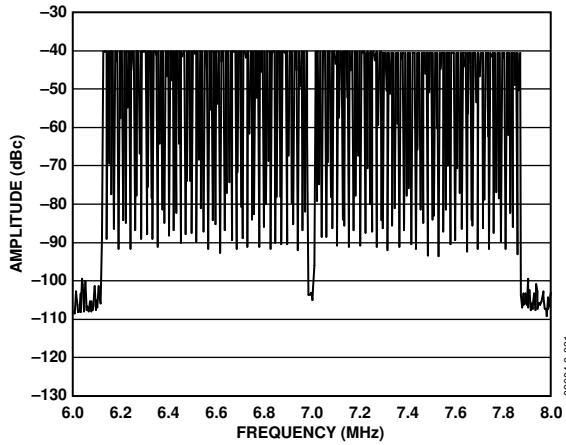


Figure 34. AD9863 Tx Path FFT, 256-Carrier (Four Center Carriers Removed) OFDM Signal over 1.75 MHz Bandwidth, Centered at 7 MHz, with 20 mA Full-Scale Output into 60 Ω Differential Load

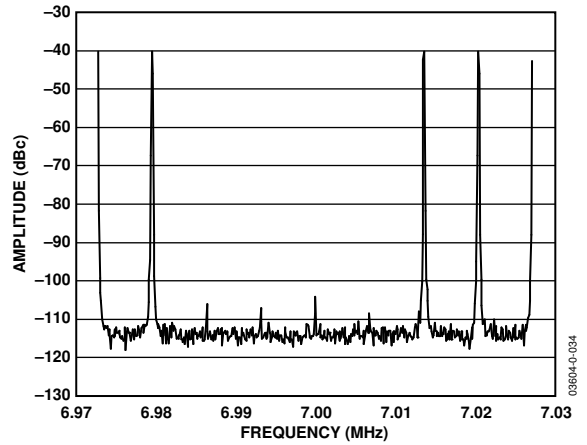


Figure 37. AD9863 Tx Path FFT, In-Band IMD Products of OFDM Signal in Figure 34

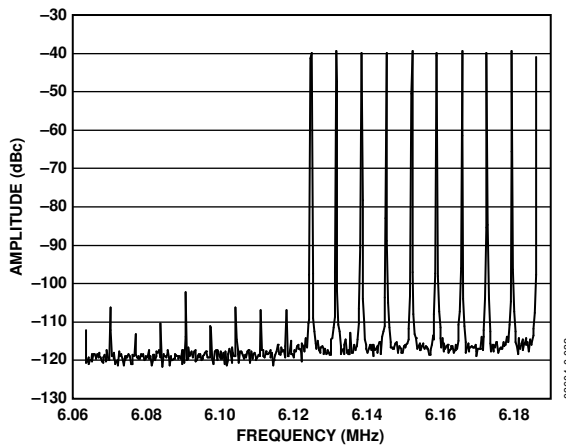


Figure 35. AD9863 Tx Path FFT, Lower-Band IMD Products of OFDM Signal in Figure 34

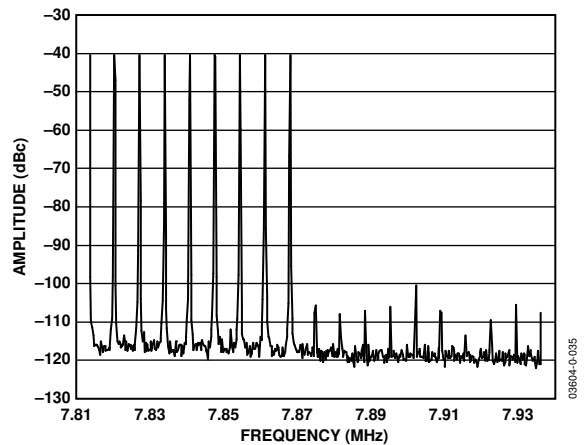


Figure 38. AD9863 Tx Path FFT, Upper-Band IMD Products of OFDM Signal in Figure 34

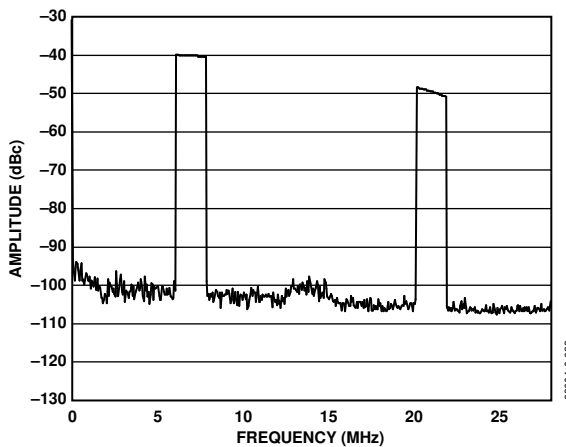


Figure 36. AD9863 Tx Path FFT of OFDM Signal in Figure 34, with 1× Interpolation

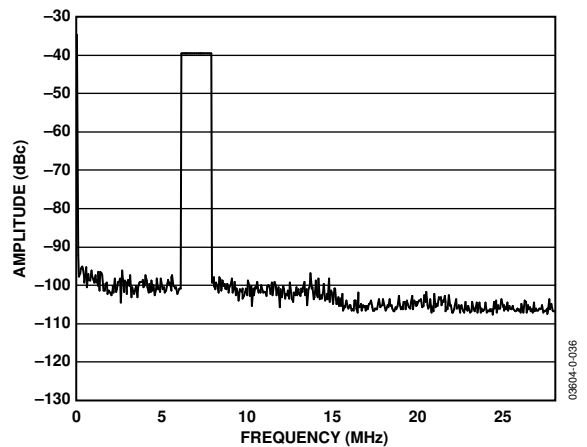


Figure 39. AD9863 Tx Path FFT of OFDM Signal in Figure 34, with 2× Interpolation

Figure 40 to Figure 45 use the same input data to the Tx path, a 256-carrier OFDM signal over a 23 MHz bandwidth, centered at 23 MHz. The four center carriers are removed from the signal to observe the in-band intermodulation distortion (IMD) from the DAC output.

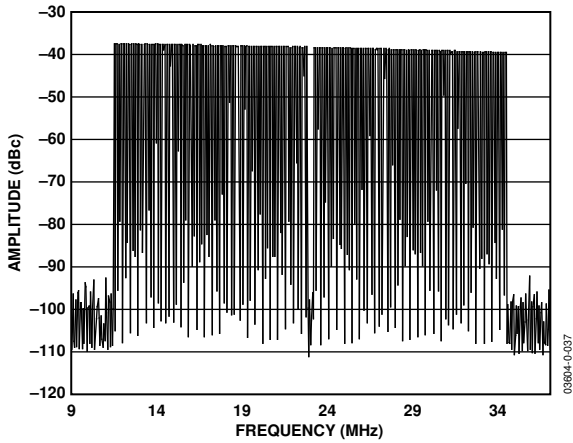


Figure 40. AD9863 Tx Path FFT, 256-Carrier (Four Center Carriers Removed) OFDM Signal over 23 MHz Bandwidth, Centered at 7 MHz, with 20 mA Full-Scale Output into 60 Ω Differential Load

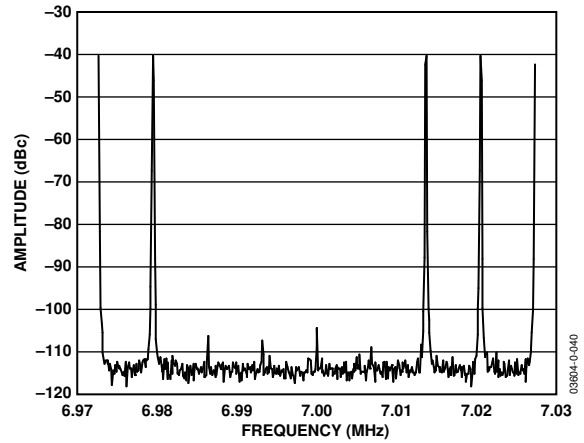


Figure 43. AD9863 Tx Path FFT, In-Band IMD Products of OFDM Signal in Figure 40

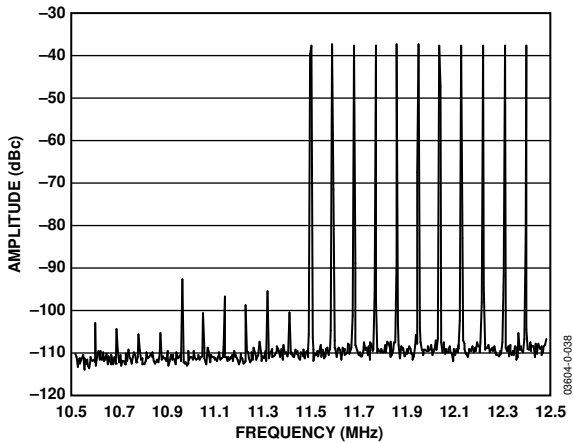


Figure 41. AD9863 Tx Path FFT, Lower-Band IMD Products of OFDM Signal in Figure 40

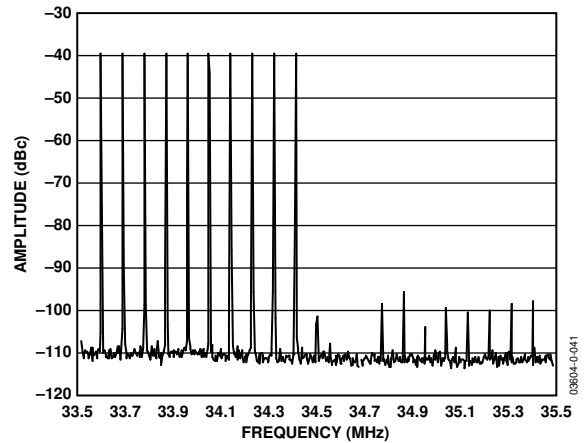


Figure 44. AD9863 Tx Path FFT, Upper-Band IMD Products of OFDM Signal in Figure 40

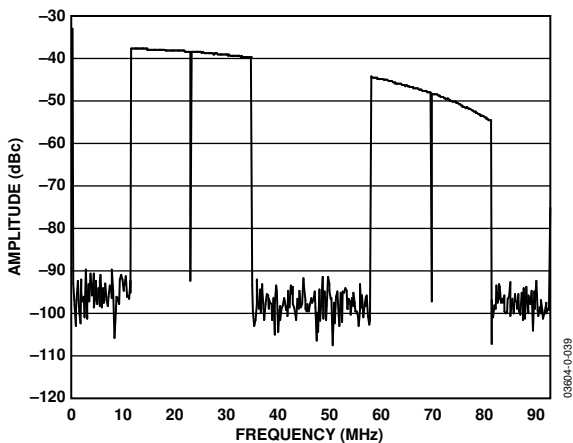


Figure 42. AD9863 Tx Path FFT of OFDM Signal in Figure 40, with 1× Interpolation

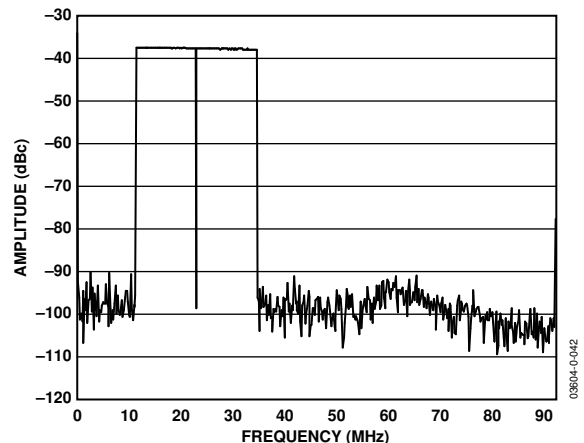


Figure 45. AD9863 Tx Path FFT of OFDM Signal in Figure 40, with 2× Interpolation

TERMINOLOGY

Input Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay

The delay between the 50% point of the rising edge of the CLKIN1 signal and the instant at which the analog input is actually sampled.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Crosstalk

Coupling onto one channel being driven by a -0.5 dBFS signal when the adjacent interfering channel is driven by a full-scale signal.

Differential Analog Input Voltage Range

The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180° out of phase. Peak-to-peak differential is computed by rotating the input phase 180° and taking the peak measurement again. Then the difference is computed between both peak measurements.

Differential Nonlinearity

The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB)

The effective number of bits is calculated from the measured SNR based on the following equation:

$$ENOB = \frac{SNR_{MEASURED} - 1.76 \text{ dB}}{6.02}$$

Pulse Width/Duty Cycle

Pulse width high is the minimum amount of time that a signal must be left in the logic high state to achieve rated performance; pulse width low is the minimum time a signal must be left in the low state, logic low.

Full-Scale Input Power

Expressed in dBm, full-scale input power is computed using the following equation:

$$Power_{FULLSCALE} = 10 \log \left(\frac{V_{FULLSCALE-RMS}^2 / Z_{INPUT}}{0.001} \right)$$

Gain Error

Gain error is the difference between the measured and ideal full-scale input voltage range of the ADC.

Harmonic Distortion, Second

The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

Harmonic Distortion, Third

The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Integral Nonlinearity

The deviation of the transfer function from a reference line measured in fractions of an LSB using a “best straight line” determined by a least square curve fit.

Minimum Conversion Rate

The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate

The encode rate at which parametric testing is performed.

Output Propagation Delay

The delay between a differential crossing of CLK+ and CLK– and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio

The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise and Distortion (SINAD)

The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics, but excluding dc.

Signal-to-Noise Ratio (without Harmonics)

The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. It also may be reported in dBc (for example, degrades as signal level is lowered) or dBFS (for example, always related back to converter full scale). SFDR does not include harmonic distortion components.

Worst Other Spur

The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonics) reported in dBc.

THEORY OF OPERATION

SYSTEM BLOCK

The AD9863 is targeted to cover the mixed-signal front end needs of multiple wireless communications systems. It features a receive path that consists of dual 12-bit receive ADCs and a transmit path that consists of dual 12-bit transmit DACs (TxDAC). The AD9863 integrates additional functionality typically required in most systems, such as power scalability, Tx gain control, and clock multiplication circuitry.

The AD9863 minimizes both size and power consumption to address the needs of a range of applications from the low power portable market to the high performance base station market. The part is provided in a 64-lead lead frame chip scale package (LFCSP) that has a footprint of only 9 mm × 9 mm. Power consumption can be optimized to suit the particular application beyond just a speed grade option by incorporating power-down controls, low power ADC modes, TxDAC power scaling, and a half-duplex mode, which automatically disables the unused digital path.

The AD9863 uses two 12-bit buses to transfer Rx path data and Tx path data. These two buses support 24-bit parallel data transfers or 12-bit interleaved data transfers. The bus is configurable through either external mode pins or internal registers settings. The registers allow many more options for configuring the entire device.

The following sections discuss the various blocks of the AD9863: Rx Path Block, Tx Path Block, Digital Block, Programmable Registers, and Clock Distribution Block.

Rx PATH BLOCK

Rx Path General Description

The AD9863 Rx path consists of two 12-bit, 50 MSPS analog-to-digital converters (ADCs). The dual ADC paths share the same clocking and reference circuitry to provide optimal matching characteristics. Each of the ADCs consists of a 9-stage differential pipelined switched capacitor architecture with output error correction logic.

The pipelined architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. Sampling occurs on the falling edge of the input clock. Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC and a residual multiplier to drive the next stage of the pipeline. The residual multiplier uses the flash ADC output to control a switched capacitor digital-to-analog converter (DAC) of the same resolution. The DAC output is subtracted from the stage's input signal, and the residual is amplified (multiplied) to drive the next pipeline stage. The residual multiplier stage is also called a multiplying DAC (MDAC). One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The differential input stage is dc self-biased and allows differential or single-ended inputs. The output-staging block aligns the data, carries out the error correction, and passes the data to the output buffers.

The latency of the Rx path is about 5 clock cycles.

Rx Path Analog Input Equivalent Circuit

The Rx path analog inputs of the AD9863 incorporate a novel structure that merges the function of the input sample-and-hold amplifiers (SHAs) and the first pipeline residue amplifiers into a single, compact switched capacitor circuit. By eliminating one amplifier in the pipeline, this structure achieves considerable noise and power savings over a conventional implementation that uses separate amplifiers.

Figure 46 illustrates the equivalent analog inputs of the AD9863 (a switched capacitor input). Bringing CLK to logic high opens Switch S3 and closes Switch S1 and Switch S2; this is the sample mode of the input circuit. The input source connected to VIN+ and VIN- must charge capacitor C_H during this time. Bringing CLK to a logic low opens Switch S2, and then Switch S1 opens, followed by the closing of Switch S3. This puts the input circuit into hold mode.

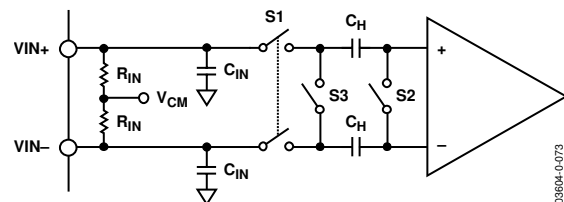


Figure 46. Differential Input Architecture

The structure of the input SHA places certain requirements on the input drive source. The differential input resistors are typically 2 kΩ each. The combination of the pin capacitance, C_{IN}, and the hold capacitance, C_H, is typically less than 5 pF. The input source must be able to charge or discharge this capacitance to 12-bit accuracy in one-half of a clock cycle. When the SHA goes into sample mode, the input source must charge or discharge capacitor C_H from the voltage already stored on it to the new voltage. In the worst case, a full-scale voltage step on the input source must provide the charging current through the R_{ON} of Switch S1 (typically 100 Ω) to a settled voltage within one-half of the ADC sample period. This situation corresponds to driving a low input impedance. On the other hand, when the source voltage equals the value previously stored on C_H, the hold capacitor requires no input current and the equivalent input impedance is extremely high.

Rx Path Application Section

Adding series resistance between the output of the signal source and the VIN pins reduces the drive requirements placed on the signal source. Figure 47 shows this configuration.

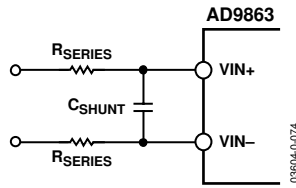


Figure 47. Typical Input

The bandwidth of the particular application limits the size of this resistor. For applications with signal bandwidths less than 10 MHz, the user may insert series input resistors and a shunt capacitor to produce a low-pass filter for the input signal. In addition, adding a shunt capacitance between the VIN pins can lower the ac load impedance. The value of this capacitance depends on the source resistance and the required signal bandwidth.

The Rx input pins are self-biased to provide this midsupply, common-mode bias voltage, so it is recommended to ac couple the signal to the inputs using dc blocking capacitors. In systems that must use dc coupling, use an op amp to comply with the input requirements of the AD9863. The inputs accept a signal with a 2 V p-p differential input swing centered about one-half of the supply voltage ($AVDD/2$). If the dc bias is supplied externally, the internal input bias circuit must be powered down by writing to registers Rx_A dc bias [Register 0x03, Bit 6] and Rx_B dc bias [Register 0x04, Bit 7].

The ADCs in the AD9863 are designed to sample differential input signals. The differential input provides improved noise immunity and better THD and SFDR performance for the Rx path. In systems that use single-ended signals, these inputs can be digitized, but it is recommended that a single-ended-to-differential conversion be performed. A single-ended-to-differential conversion can be performed by using a transformer coupling circuit (typically for signals above 10 MHz) or by using an operational amplifier, such as the AD8138 (typically for signals below 10 MHz).

ADC Voltage References

The AD9863 12-bit ADCs use internal references that are designed to provide for a 2 V p-p differential input range. The internal band gap reference generates a stable 1 V reference level and is decoupled through the VREF pin. REFT and REFB are the differential references generated based on the voltage level of VREF. Figure 48 shows the proper decoupling of the reference pins VREF, REFT, and REFB when using the internal reference. Decoupling capacitors must be placed as close to the reference pins as possible.

External references REFT and REFB are centered at $AVDD/2$ with a differential voltage equal to the voltage at VREF (by default 1 V when using the internal reference), allowing a peak-to-peak differential voltage swing of $2 \times VREF$.

For example, the default 1 V VREF reference accepts a 2 V p-p differential input swing, and the offset voltage must be

$$REFT = AVDD/2 + 0.5 V$$

$$REFB = AVDD/2 - 0.5 V$$

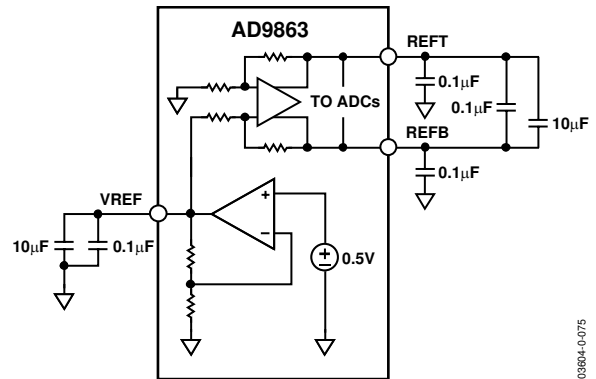


Figure 48. Typical Rx Path Decoupling

An external reference may be used for systems that require a different input voltage range, high accuracy gain matching between multiple devices, or improvements in temperature drift and noise characteristics. When an external reference is desired, the internal Rx band gap reference must be powered down using the VREF register [Register 0x05, Bit 4], with the external reference driving the voltage level on the VREF pin. The external voltage level must be one-half of the desired peak-to-peak differential voltage swing. The result is that the differential voltage references are driven to new voltages:

$$REFT = AVDD/2 + V_{REF}/2 V$$

$$REFB = AVDD/2 - V_{REF}/2 V$$

If an external reference is used, it is recommended not to exceed a differential offset voltage greater than 1 V for the reference.

Clock Input and Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9863 contains clock duty cycle stabilizer circuitry (DCS). The DCS retimes the internal ADC clock (nonsampling edge) and provides the ADC with a nominal 50% duty cycle. Input clock rates of over 40 MHz can use the DCS so that a wide range of input clock duty cycles can be accommodated. Conversely, DCS must not be used for Rx sampling below 40 MSPS. Maintaining a 50% duty cycle clock is particularly important in high speed applications when proper sample-and-hold times for the converter are required to maintain high performance. The DCS can be enabled by writing highs to the Rx_A/Rx_B CLK duty register bits [Register 0x06/ Register 0x07, Bit 4].

The duty cycle stabilizer uses a delay-locked loop to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately 2 μ s to 3 μ s to allow the DLL to adjust to the new rate and settle. High speed, high resolution ADCs are sensitive to the quality of the clock input.

The degradation in SNR at a given full-scale input frequency (f_{INPUT}), due to aperture jitter (t_A), can be calculated with the following equation:

$$\text{SNR degradation} = 20 \log \left[\left(\frac{1}{2} \right) \pi f_{\text{INTA}} t_A \right]$$

In the equation, the rms aperture jitter, t_A , represents the root-sum-square of all jitter sources, which includes the clock input, analog input signal, and ADC aperture jitter specification. Undersampling applications are particularly sensitive to jitter. The clock input is a digital signal that must be treated as an analog signal with logic level threshold voltages, especially in cases where aperture jitter may affect the dynamic range of the AD9863. Power supplies for clock drivers must be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it must be retimed by the original clock at the last step.

Power Dissipation and Standby Mode

The power dissipation of the AD9863 Rx path is proportional to its sampling rate. The Rx path portion of the digital (DRVDD) power dissipation is determined primarily by the strength of the digital drivers and the load on each output bit. The digital drive current can be calculated by

$$I_{\text{DRVDD}} = V_{\text{DRVDD}} \times C_{\text{LOAD}} \times f_{\text{CLOCK}} \times N$$

where N is the number of bits changing and C_{LOAD} is the average load on the digital pins that changed.

The analog circuitry is optimally biased so that each speed grade provides excellent performance while affording reduced power consumption. Each speed grade dissipates a baseline power at low sample rates, which increases with clock frequency. The baseline power dissipation for either speed grade can be reduced by asserting the ADC_LO_PWR pin, which reduces internal ADC bias currents by half, in some cases resulting in degraded performance.

To further reduce power consumption of the ADC, the ADC_LO_PWR pin can be combined with a serial programmable register setting to configure an ultralow power mode. The ultralow power mode reduces power consumption by a fourth of the normal power consumption. The ultralow power mode can be used at slower sampling frequencies or if reduced performance is acceptable. To configure the ultralow power mode, assert the ADC_LO_PWR pin during power-up and write the following register settings:

Register 0x08 (MSB) 0000 1100
 Register 0x09 (MSB) 0111 0000
 Register 0x0A (MSB) 0111 0000

Figure 49 shows the typical analog power dissipation ($\text{ADC_AVDD} = 3.3 \text{ V}$) for the ADC vs. sampling rate for the normal power, low power, and ultralow power modes.

Either of the ADCs in the AD9863 Rx path can be placed in standby mode independently by writing to the appropriate SPI register bits in Register 3, Register 4, and Register 5. The minimum standby power is achieved when both channels are placed in full power-down mode using the appropriate SPI register bits in Register 3, Register 4, and Register 5. Under this condition, the internal references are powered down. When either or both of the channel paths are enabled after a power-down, the wake-up time is directly related to the recharging of the REFT and REFB decoupling capacitors and the duration of the power-down. Typically, it takes approximately 5 ms to restore full operation with fully discharged 0.1 μF and 10 μF decoupling capacitors on REFT and REFB.

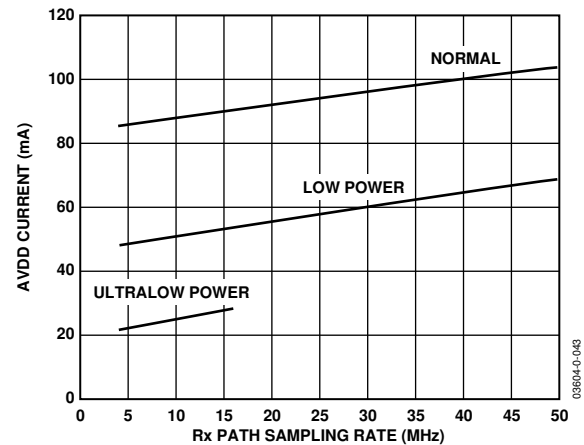


Figure 49. Typical Rx Path Analog Supply Current vs. Sample Rate, $V_{\text{DD}} = 3.3 \text{ V}$ for Normal, Low, and Ultralow Power Modes

Tx PATH BLOCK

The AD9863 transmit (Tx) path includes dual interpolating 12-bit current output DACs that can be operated independently or can be coupled to form a complex spectrum in an image reject transmit architecture. Each channel includes two FIR filters, making the AD9863 capable of 1 \times , 2 \times , or 4 \times interpolation. High speed input and output data rates can be achieved within the limitations listed in Table 9.

Table 9. AD9863 Tx Path Maximum Data Rate

Interpolation Rate	24-Bit Interface Mode	Input Data Rate per Channel (MSPS)	DAC Sampling Rate (MSPS)
1 \times	FD, HD12, Clone	80	80
	HD24	160	160
2 \times	FD, HD12, Clone	80	160
	HD24	80	160
4 \times	FD, HD12, Clone	50	200
	HD24	50	200

By using the dual DAC outputs to form a complex signal, an external analog quadrature modulator, such as the Analog Devices AD8349, can enable an image rejection architecture. (Note: the AD9863 evaluation board includes a quadrature modulator in the Tx path that accommodates the AD8345, AD8346, and AD8349 footprints.)

To optimize the image rejection capability as well as LO feedthrough suppression in this architecture, the AD9863 offers programmable (via the SPI port), fine (trim) gain and offset adjustment for each DAC.

Also included in the AD9863 are a phase-locked loop (PLL) clock multiplier and a 1.2 V band gap voltage reference. With the PLL enabled, a clock applied to the CLKIN2 input is multiplied internally and generates all necessary internal synchronization clocks. Each 12-bit DAC provides two complementary current outputs whose full-scale currents can be determined from a single external resistor.

An external pin, TxPWRDWN, can be used to power down the Tx path when not in use, optimizing system power consumption. Using the TxPWRDWN pin disables clocks and some analog circuitry, saving both digital and analog power. The power-down mode leaves the biases enabled to facilitate a quick recovery time, typically <math><10\ \mu\text{s}</math>. In addition, a sleep mode is available that turns off the DAC output current but leaves all other circuits active for a modest power savings. An SPI-compliant serial port is used to program the many features of the AD9863. Note that in power-down mode, the SPI port is still active.

DAC Equivalent Circuits

The AD9863 Tx path, consisting of dual 12-bit DACs, is shown in Figure 50. The DACs integrate a high performance TxDAC core, a programmable gain control through a programmable gain amplifier (TxPGA), coarse gain control, and offset adjustment and fine gain control to compensate for system mismatches. Coarse gain applies a gross scaling to either DAC by $1\times$, $(1/2)\times$, or $(1/11)\times$. The TxPGA provides gain control from 0 dB to -20 dB in steps of 0.1 dB and is controlled via the 8-bit TxPGA setting. A fine gain adjustment of $\pm 4\%$ for each channel is controlled through a 6-bit fine gain register. By default, coarse gain is $1\times$, the TxPGA is set to 0 dB, and the fine gain is set to 0%.

The TxDAC core of the AD9863 provides dual, differential, complementary current outputs generated from the 12-bit data. The 12-bit dual DACs support update rates up to 200 MSPS. The differential outputs (IOUT+ and IOUT-) of each dual DAC are complementary, meaning that they always add up to the full-scale current output of the DAC, I_{OUTFS} . Optimum ac performance is achieved when the differential current interface drives balanced loads or a transformer.

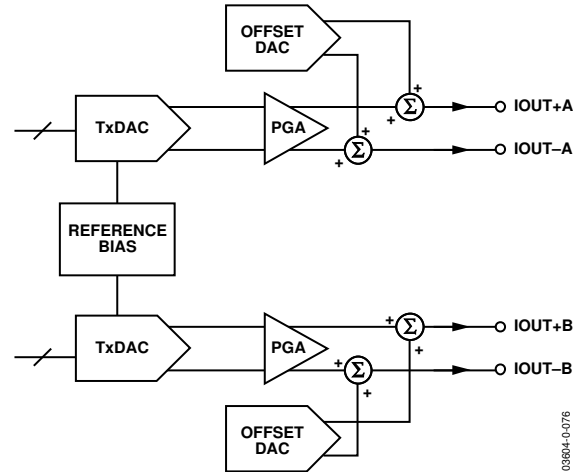


Figure 50. TxDAC Output Structure Block Diagram

The fine gain control provides improved balance of QAM modulated signals, resulting in improved modulation accuracy and image rejection.

The independent DAC A and DAC B offset control adds a small dc current to either IOUT+ or IOUT- (not both). The selection of which IOUT this offset current is directed toward is programmable via register setting. Offset control can be used for suppression of a LO leakage signal that typically results at the output of the modulator.

If the AD9863 is dc-coupled to an external modulator, this feature can be used to cancel the output offset on the AD9863 as well as the input offset on the modulator. The reference circuitry is shown in Figure 51.

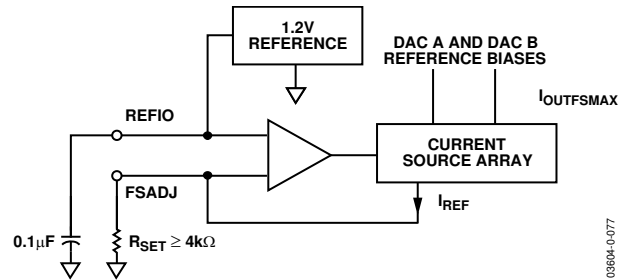


Figure 51. Reference Circuitry

Referring to the transfer function of the following equation, I_{OUTFSMAX} is the maximum current output of the DAC with the default gain setting (0 dB) and is based on a reference current, I_{REF} . I_{REF} is set by the internal 1.2 V reference and the external R_{SET} resistor.

$$I_{\text{OUTFSMAX}} = 64 \times (\text{REFIO}/R_{\text{SET}})$$

Typically, R_{SET} is 4 k Ω , which sets I_{OUTFSMAX} to 20 mA, the optimal dynamic setting for the TxDACs. Increasing R_{SET} by a factor of 2 proportionally decreases I_{OUTFSMAX} by a factor of 2. I_{OUTFSMAX} of each DAC can be rescaled either simultaneously, using the TxPGA gain register, or independently, using the DAC A/DAC B coarse gain registers.

The TxPGA function provides 20 dB of simultaneous gain range for both DACs, and it is controlled by writing to the SPI register TxPGA gain for a programmable full-scale output of 10% to 100% of $I_{OUTFSMAX}$. The gain curve is linear in dB, with steps of about 0.1 dB. Internally, the gain is controlled by changing the main DAC bias currents with an internal TxPGA DAC whose output is heavily filtered via an on-chip R-C filter to provide continuous gain transitions. Note that the settling time and bandwidth of the TxPGA DAC can be improved by a factor of 2 by writing to the TxPGA fast update register.

Each DAC has independent coarse gain control. Coarse gain control can be used to accommodate different I_{OUTFS} from the dual DACs. The coarse full-scale output control can be adjusted by using the DAC A/DAC B coarse gain registers to 1/2 or 1/11 of the nominal full-scale current.

Fine gain controls and dc offset controls can be used to compensate for mismatches (for system level calibration), allowing improved matching characteristics of the two Tx channels and aiding in suppressing LO feedthrough. This is especially useful in image rejection architectures. The 10-bit dc offset control of each DAC can be used independently to provide an offset of up to $\pm 12\%$ of $I_{OUTFSMAX}$ to either differential pin, thus allowing calibration of any system offset. The fine gain control with 5-bit resolution allows the $I_{OUTFSMAX}$ of each DAC to be varied over a $\pm 4\%$ range, allowing compensation of any DAC or system gain mismatches. Fine gain control is set through the DAC A/DAC B fine gain registers, and the offset control of each DAC is accomplished using the DAC A/DAC B offset registers.

Clock Input Configuration

The quality of the clock and data input signals is important in achieving optimum performance. The external clock driver circuitry provides the AD9863 with a low jitter clock input that meets the min/max logic levels while providing fast edges. When a driver is used to buffer the clock input, it must be placed very close to the AD9863 clock input, thereby negating any transmission line effects such as reflections due to mismatch.

Programmable PLL

CLKIN2 can function either as an input data rate clock (PLL enabled) or as a DAC data rate clock (PLL disabled).

The PLL clock multiplier and distribution circuitry produce the necessary internal timing to synchronize the rising edge triggered latches for the enabled interpolation filters and DACs. This circuitry consists of a phase detector, charge pump, voltage controlled oscillator (VCO), and clock distribution block, all under SPI port control. The charge pump, phase detector, and VCO are powered from PLL_AVDD, while the clock distribution circuits are powered from the DVDD supply.

To ensure optimum phase noise performance from the PLL clock multiplier circuits, PLL_AVDD must originate from a clean analog supply. The speed of the VCO within the PLL also has an effect on phase noise.

The PLL locks with VCO speeds as low as 32 MHz up to 350 MHz, but optimal phase noise with respect to VCO speed is achieved by running it in the range of 64 MHz to 200 MHz.

Power Dissipation

The AD9863 Tx path power is derived from three voltage supplies: AVDD, DVDD, and DRVDD.

IDRVDD and IDVDD are very dependent on the input data rate, the interpolation rate, and the activation of the internal digital modulator. IAVDD has the same type of sensitivity to data, interpolation rate, and the modulator function, but to a much lesser degree ($<10\%$).

Sleep/Power-Down Modes

The AD9863 provides multiple methods for programming power saving modes. The externally controlled TxPWRDWN or SPI programmed sleep mode and the full power-down mode are the main options.

TxPWRDWN is used to disable all clocks and much of the analog circuitry in the Tx path when asserted. In this mode, the biases remain active, therefore reducing the time required for re-enabling the Tx path. The time of recovery from power-down for this mode is typically less than 10 μ s.

Sleep mode, when activated, turns off the DAC output currents, but the rest of the chip remains functioning. When coming out of sleep mode, the AD9863 immediately returns to full operation.

A full power-down mode can be enabled through the SPI register, which turns off all Tx path related analog and digital circuitry in the AD9863. When returning from full power-down mode, enough clock cycles must be allowed to flush the digital filters of random data acquired during the power-down cycle.

Interpolation Stage

Interpolation filters are available for use in the AD9863 transmit path, providing 1 \times (bypassed), 2 \times , or 4 \times interpolation.

The interpolation filters effectively increase the Tx data rate while suppressing the original images. The interpolation filters digitally shift the worst-case image further away from the desired signal, thus reducing the requirements on the analog output reconstruction filter.

There are two 2 \times interpolation filters available in the Tx path. An interpolation rate of 4 \times is achieved using both interpolation filters; an interpolation rate of 2 \times is achieved by enabling only the first 2 \times interpolation filter.

The first interpolation filter provides 2 \times interpolation using a 39-tap filter. It suppresses out-of-band signals by 60 dB or more and has a flat pass-band response (less than 0.1 dB ripple) extending to 38% of the input Tx data rate (19% of the DAC update rate, f_{DAC}). The maximum input data rate is 80 MSPS per channel when using 2 \times interpolation.

The second interpolation filter provides an additional 2 \times interpolation for an overall 4 \times interpolation. The second filter is a 15-tap filter, which suppresses out-of-band signals by 60 dB or more.

The flat pass-band response (less than 0.1 dB attenuation) is 38% of the Tx input data rate (9.5% of f_{DAC}). The maximum input data rate per channel is 50 MSPS per channel when using 4× interpolation.

Latch/Demultiplexer

Data for the dual-channel Tx path can be latched in parallel through two ports in half-duplex operations (HD24 mode) or through a single port by interleaving the data (FD, HD12, and clone modes). See the Flexible I/O Interface Options section in the Digital Block description that follows and the Clock Distribution Block section for further descriptions of each mode.

DIGITAL BLOCK

The AD9863 digital block allows the device to be configured in various timing and operation modes. The following sections discuss the flexible I/O interfaces, the clock distribution block, and the programming of the device through mode pins or SPI registers.

Flexible I/O Interface Options

The AD9863 can accommodate various data interface transfer options (flexible I/O). The AD9863 uses two 12-bit buses, an upper bus (U12) and a lower bus (L12), to transfer the dual-channel 12-bit ADC data and dual-channel 12-bit DAC data by means of interleaved data, parallel data, or a mix of both. Table 10 shows the different I/O configurations of the modes depending on half-duplex or full-duplex operation. Table 11 and Table 12 summarize the pin configurations vs. the modes.

Table 10. Flexible Data Interface Modes

Mode Name	Tx Only Mode (Half-Duplex)	Rx Only Mode (Half-Duplex)	Concurrent Tx + Rx Mode (Full-Duplex)	General Notes
HD24			N/A	Rx data rate = 1 × ADC sample rate Two 12-bit parallel Rx data buses Tx data rate = 1 × ADC sample rate Two 12-bit parallel Tx data buses
HD12			N/A	Rx data rate = 2 × ADC sample rate One 12-bit interleaved Rx data bus Tx data rate = 2 × ADC sample rate One 12-bit interleaved Tx data bus
FD				Rx data rate = 2 × ADC sample rate One 12-bit interleaved Rx data bus Tx data rate = 2 × ADC sample rate One 12-bit interleaved Tx data bus
Clone			N/A	Rx data rate = 1 × ADC sample rate Two 12-bit parallel Rx data buses Tx data rate = 2 × ADC sample rate One 12-bit interleaved Tx data bus Requires SPI interface to configure; similar to AD9862 data interface

Table 11 describes AD9863 pin function (when mode pins are used) relative to I/O mode and for half-duplex modes, whether transmitting or receiving.

Table 11. AD9863 Pin Function vs. Interface Mode (No SPI Cases)¹

Mode Name	U12 Bus	L12 Bus	IFACE1	IFACE2	IFACE3
FD	Interleaved Tx data	Interleaved Rx data	TxSYNC	Buffered Rx Clock	Buffered Tx clock
HD12 (Tx/Rx = High)	Interleaved Tx data	MSB = TxSYNC Others = three-state	Tx/Rx = tied high	12/24 pin control tied high	Buffered Tx clock
HD12 (Tx/Rx = Low)	MSB = RxSYNC Others = three-state	Interleaved Rx data	Tx/Rx = tied low	12/24 pin control tied high	Buffered Rx clock
HD24 (Tx/Rx = High)	Tx_A data	Tx_B data	Tx/Rx = tied high	12/24 pin control tied low	Buffered Tx clock
HD24 (Tx/Rx = Low)	Rx_B data	Rx_A data	Tx/Rx = tied low	12/24 pin control tied low	Buffered Rx clock
Clone Mode (Tx/Rx = High)	x	x	x	x	x
Clone Mode (Tx/Rx = Low)	x	x	x	x	x

¹ Clone mode not available without SPI.

Table 12 describes AD9863 pin function (when SPI programming is used) relative to flexible I/O mode and for half-duplex modes, whether transmitting or receiving.

Table 12. AD9863 Pin Function vs. Interface Mode (Configured through the SPI Registers)

Mode Name	U12 Bus	L12 Bus	IFACE1	IFACE2	IFACE3
FD	Interleaved Tx data	Interleaved Rx data	TxSYNC	Buffered system clock	Buffered Tx clock
HD12, Tx Mode (Tx/Rx = High)	Interleaved Tx data	MSB = TxSYNC others = three-state	Tx/Rx = tied high	Optional buffered system clock	Buffered Tx clock
HD12, Rx Mode (Tx/Rx = Low)	MSB = RxSYNC Other = three-state	Interleaved Tx data	Tx/Rx = tied low	Optional buffered system clock	Buffered Rx clock
HD24, Tx Mode (Tx/Rx = High)	Tx_A data	Tx_B data	Tx/Rx = tied high	Optional buffered system clock	Buffered Tx clock
HD24, Rx Mode (Tx/Rx = Low)	Rx_B data	Rx_A data	Tx/Rx = tied low	Optional buffered system clock	Buffered Rx clock
Clone Mode, Tx Mode (Tx/Rx = High)	Interleaved Tx data	MSB = TxSYNC Others = three-state	Tx/Rx = tied high	Optional buffered system clock	Buffered Tx clock
Clone Mode, Rx Mode (Tx/Rx = Low)	Rx_B data	Rx_A data	Tx/Rx = tied low	Optional buffered system clock	Buffered Rx clock

Summary of Flexible I/O Modes

FD Mode

The full-duplex (FD) mode can be configured by using mode pins or with SPI programming. Using the SPI allows additional configuration flexibility of the device.

FD mode is the only mode that supports full-duplex, receive, and transmit concurrent operations. The upper 12-bit bus (U12) is used to accept interleaved Tx data, and the lower 12-bit bus (L12) is used to output interleaved Rx data. Either the Rx path or the Tx path (or both) can be independently powered down using either (or both) the RxPwrDwn and TxPwrDwn pins. FD mode requires interpolation of 2× or 4×.

The following notes provide a general description of the FD mode configuration. For more information, refer to Table 15.

Note the following about the Tx path in FD mode:

- Interpolation rate of 2× or 4× can be programmed with mode pins or SPI.
- Max DAC update rate = 200 MSPS.
Max Tx input data rate = 80 MSPS/channel (160 MSPS interleaved).
- TxSYNC is used to direct Tx input data.
TxSYNC = high indicates channel Tx_A data.
TxSYNC = low indicates channel Tx_B data.
- Buffered Tx clock output (from IFACE3 pin) equals 2× the DAC update rate; one rising edge per interleaved Tx sample.