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IF Digitizing Subsystem

Data Sheet

AD9864

FEATURES

10 MHz to 300 MHz input frequency
6.8 kHz to 270 kHz output signal bandwidth
7.5 dB single sideband noise figure (SSB NF)
−7.0 dBm input third-order intercept (IIP3)
AGC free range up to −34 dBm
12 dB continuous AGC range
16 dB front-end attenuator
Baseband I/Q 16-bit (or 24-bit) serial digital output
LO and sampling clock synthesizers
Programmable decimation factor, output format, AGC, and synthesizer settings
370 Ω input impedance
2.7 V to 3.6 V supply voltage
Low current consumption: 17 mA
48-lead LFCSP package

APPLICATIONS

Multimode narrow-band radio products
Analog/digital UHF/VHF FDMA receivers
TETRA, APCO25, GSM/EDGE
Portable and mobile radio products
SATCOM terminals

GENERAL DESCRIPTION

The AD9864[1] is a general-purpose IF subsystem that digitizes a low level, 10 MHz to 300 MHz IF input with a signal bandwidth ranging from 6.8 kHz to 270 kHz. The signal chain of the AD9864 consists of a low noise amplifier (LNA), a mixer, a band-pass Σ-Δ analog-to-digital converter (ADC), and a decimation filter with programmable decimation factor. An automatic gain control (AGC) circuit gives the AD9864 12 dB of continuous gain adjustment. Auxiliary blocks include both clock and local oscillator (LO) synthesizers.

The high dynamic range of the AD9864 and inherent antialiasing provided by the band-pass Σ-Δ converter allow the device to cope with blocking signals up to 95 dB stronger than the desired signal. This attribute often reduces the cost of a radio by reducing IF filtering requirements. Also, it enables multimode radios of varying channel bandwidths, allowing the IF filter to be specified for the largest channel bandwidth.

The SPI port programs numerous parameters of the AD9864, allowing the device to be optimized for any given application. Programmable parameters include synthesizer divide ratios, AGC attenuation and attack/decay time, received signal strength level, decimation factor, output data format, 16 dB attenuator, and the selected bias currents.

The AD9864 is available in a 48-lead LFCSP package and operates from a single 2.7 V to 3.6 V supply. The total power consumption is typically 56 mW and a power-down mode is provided via serial interfacing.

FUNCTIONAL BLOCK DIAGRAM

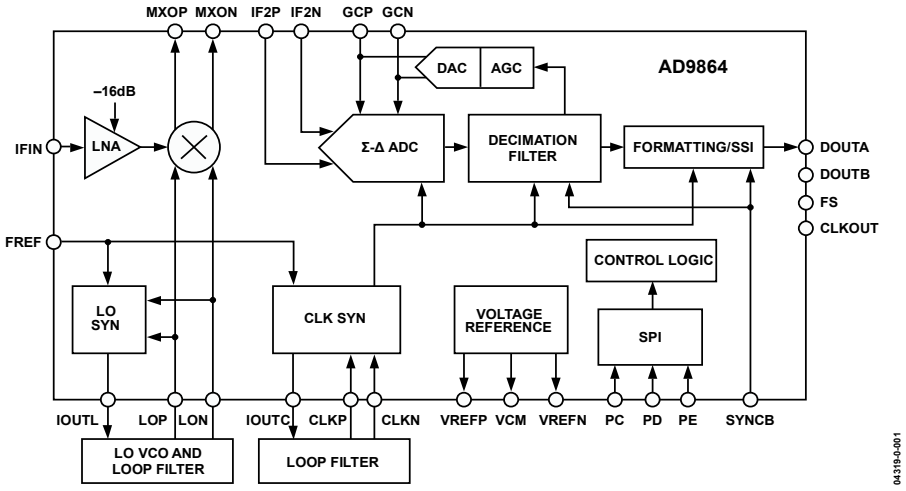

Figure 1.

[1] Protected by U.S. Patent No. 5,969,657; other patents pending.

Rev. A Document Feedback

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COMPARABLE PARTS

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EVALUATION KITS

- Evaluation Board for AD9864 and AD9874

DOCUMENTATION

Data Sheet

- AD9864: IF Digitizing Subsystem Data Sheet

TOOLS AND SIMULATIONS

- AD9864 IBIS Models

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC
- MS-2735: Maximizing the Dynamic Range of Software-Defined Radio

DESIGN RESOURCES

- AD9864 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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SPECIFICATIONS

VDDI = VDDF = VDDA = VDDC = VDDL = VDDH = 2.7 V to 3.6 V, VDDQ = VDDP = 2.7 V to 5.5 V, f_{CLK} = 18 MSPS, f_{IF} = 109.65 MHz, f_{LO} = 107.4 MHz, f_{REF} = 16.8 MHz, unless otherwise noted. Standard operating mode: VGA at minimum attenuation setting, synthesizers in normal (not fast acquire) mode, decimation factor = 900, 16-bit digital output, and 10 pF load on SSI output pins.

Table 1.

Parameter	Temperature	Test Level	Min	Typ	Max	Unit
SYSTEM DYNAMIC PERFORMANCE[1]						
SSB Noise Figure at Minimum VGA Attenuation[2, 3]	Full	IV		7.5	9.5	dB
SSB Noise Figure at Maximum VGA Attenuation[2, 3]	Full	IV		13		dB
Dynamic Range with AGC Enabled[2, 3]	Full	IV	91	95		dB
IF Input Clip Point at Maximum VGA Attenuation[3]	Full	IV	−20	−19		dBm
IF Input Clip Point at Minimum VGA Attenuation[3]	Full	IV	−32	−31		dBm
Input Third-Order Intercept (IIP3)	Full	IV	−12	−7.0		dBm
Gain Variation over Temperature	Full	IV		0.7	2	dB
LNA + MIXER						
Maximum RF and LO Frequency Range	Full	IV	300	500		MHz
LNA Input Impedance	25°C	V		370||1.4		Ω||pF
Mixer LO Input Resistance	25°C	V		1		kΩ
LO SYNTHESIZER						
LO Input Frequency	Full	IV	7.75		300	MHz
LO Input Amplitude	Full	IV	0.3		2.0	V p-p
FREF Frequency (for Sinusoidal Input Only)	Full	IV	8		26	MHz
FREF Input Amplitude	Full	IV	0.3		3	V p-p
FREF Slew Rate	Full	IV	7.5			V/µs
Minimum Charge Pump Current at 5 V[4]	Full	VI		0.67		mA
Maximum Charge Pump Current at 5 V[4]	Full	VI		5.3		mA
Charge Pump Output Compliance[5]	Full	VI	0.4		VDDP − 0.4	V
Synthesizer Resolution	Full	IV	6.25			kHz
CLOCK SYNTHESIZER						
CLK Input Frequency	Full	IV	13		26	MHz
CLK Input Amplitude	Full	IV	0.3		VDDC	V p-p
Minimum Charge Pump Output Current[4]	Full	VI		0.67		mA
Maximum Charge Pump Output Current[4]	Full	VI		5.3		mA
Charge Pump Output Compliance[5]	Full	VI	0.4		VDDQ − 0.4	V
Synthesizer Resolution	Full	VI	2.2			kHz
Σ-Δ ADC						
Resolution	Full	IV	16		24	Bits
Clock Frequency (f_{CLK})	Full	IV	13		26	MHz
Center Frequency	Full	V		$f_{CLK}/8$		MHz
Pass-Band Gain Variation	Full	IV			1.0	dB
Alias Attenuation	Full	IV	80			dB
GAIN CONTROL						
Programmable Gain Step	Full	V		16		dB
AGC Gain Range	Full	V		12		dB
GCP Output Resistance	Full	IV	50	72.5	95	kΩ

Parameter	Temperature	Test Level	Min	Typ	Max	Unit
OVERALL						
Analog Supply Voltage (VDDA, VDDF, VDDI)	Full	VI	2.7	3.0	3.6	V
Digital Supply Voltage (VDDD, VDDC, VDDL)	Full	VI	2.7	3.0	3.6	V
Interface Supply Voltage (VDDH)[6]	Full	VI	1.8		3.6	V
Charge Pump Supply Voltage (VDDP, VDDQ)	Full	VI	2.7	5.0	5.5	V
Total Current						
Operation Mode[7]	Full	VI		17		mA
Standby	Full	VI		0.01		mA
OPERATING TEMPERATURE RANGE			−40		+85	°C

[1] This includes 0.9 dB loss of matching network.
[2] AGC with DVGA enabled.
[3] Measured in 10 kHz bandwidth.
[4] Programmable in 0.67 mA steps.
[5] Voltage span in which LO (or CLK) charge pump output current is maintained within 5% of nominal value of VDDP/2 (or VDDQ/2).
[6] VDDH must be less than VDDD + 0.5 V.
[7] Clock VCO off and additional 0.7 mA with VGA at maximum attenuation.

DIGITAL SPECIFICATIONS

VDDI = VDDF = VDDA = VDDC = VDDL = VDDH = 2.7 V to 3.6 V, VDDQ = VDDP = 2.7 V to 5.5 V, f_{CLK} = 18 MSPS, f_{IF} = 109.65 MHz, f_{LO} = 107.4 MHz, f_{REF} = 16.8 MHz, unless otherwise noted. Standard operating mode: VGA at minimum attenuation setting, synthesizers in normal (not fast acquire) mode, decimation factor = 900, 16-bit digital output, and 10 pF load on SSI output pins.

Table 2.

Parameter	Temperature	Test Level	Min	Typ	Max	Unit
DECIMATOR						
Decimation Factor[1]	Full	IV	48		960	
Pass-Band Width	Full	V		50%		f_{CLKOUT}
Pass-Band Gain Variation	Full	IV			1.2	dB
Alias Attenuation	Full	IV	88			dBm
SPI READ OPERATION (See Figure 30)						
PC Clock Frequency	Full	IV			10	MHz
PC Clock Period (t_{CLK})	Full	IV	100			ns
PC Clock High (t_{HI})	Full	IV	45			ns
PC Clock Low (t_{LOW})	Full	IV	45			ns
PC to PD Setup Time (t_{DS})	Full	IV	2			ns
PC to PD Hold Time (t_{DH})	Full	IV	2			ns
PE to PC Setup Time (t_S)	Full	IV	5			ns
PC to PE Hold Time (t_H)	Full	IV	5			ns
SPI WRITE OPERATION[2] (See Figure 29)						
PC Clock Frequency	Full	IV			10	MHz
PC Clock Period (t_{CLK})	Full	IV	100			ns
PC Clock High (t_{HI})	Full	IV	45			ns
PC Clock Low (t_{LOW})	Full	IV	45			ns
PC to PD Setup Time (t_{DS})	Full	IV	2			ns
PC to PD Hold Time (t_{DH})	Full	IV	2			ns
PC to PD (or DOUTB) Data Valid Time (t_{DV})	Full	IV	3			ns
PE to PD Output Valid to High-Z (t_{EZ})	Full	IV		8		ns
SSI[2] (See Figure 33)						
CLKOUT Frequency	Full	IV	0.867		26	MHz
CLKOUT Period (t_{CLK})	Full	IV	38.4		1153	ns
CLKOUT Duty Cycle (t_{HI}, t_{LOW})	Full	IV	33	50	67	ns
CLKOUT to FS Valid Time (t_V)	Full	IV	−1		+1	ns
CLKOUT to DOUT Data Valid Time (t_{DV})	Full	IV	−1		+1	ns
CMOS LOGIC INPUTS[3]						
Logic 1 Voltage (V_{IH})	Full	IV	0.7 × VDDH			V
Logic 0 Voltage (V_{IL})	Full	IV			0.3 × VDDH	V
Logic 1 Current (I_{IH})	Full	IV		10		µA
Logic 0 Current (I_{IL})	Full	IV		10		µA
Input Capacitance	Full	IV		3		pF
CMOS LOGIC OUTPUTS[2, 3, 4]						
Logic 1 Voltage (V_{OH})	Full	IV	VDDH − 0.2			V
Logic 0 Voltage (V_{OL})	Full	IV			0.2	V

[1] Programmable in steps of 48 or 60.
[2] CMOS output mode with C_{LOAD} = 10 pF and drive strength = 7.
[3] Absolute maximum and minimum input/output levels are VDDH + 0.3 V and −0.3 V.
[4] I_{OL} = 1 mA; specification is also dependent on drive strength setting.

ABSOLUTE MAXIMUM RATINGS

Table 3. AD9864 Absolute Maximum Ratings

Parameter	With Respect To	Rating
VDDF, VDDA, VDDC, VDDD, VDDH, VDDL, VDDI	GNDF, GNDA, GNDC, GNDD, GNDH, GNDL, GNDI, GNDS	−0.3 to +4.0
VDDF, VDDA, VDDC, VDDD, VDDH, VDDL, VDDI	VDDR, VDDA, VDDC, VDDD, VDDH, VDDL, VDDI	−4.0 V to +4.0 V
VDDP, VDDQ	GNDP, GNDQ	−0.3 V to +6.0 V
GNDF, GNDA, GNDC, GNDD, GNDH, GNDL, GNDI, GNDQ, GNDP, GNDS	GNDF, GNDA, GNDC, GNDD, GNDH, GNDL, GNDI, GNDQ, GNDP, GNDS	−0.3 V to +0.3 V
MXOP, MXON, LOP, LON, IFIN, CXIF, CXVL, CXVM	GNDH	−0.3 V to VDDI + 0.3 V
PC, PD, PE, CLKOUT, DOUTA, DOUTB, FS, SYNCB	GNDH	−0.3 V to VDDH + 0.3 V
IF2N, IF2P, GCP, GCN	GNDF	−0.3 V to VDDF + 0.3 V
VFEFP, VREGN, RREF	GNDA	−0.3 V to VDDA + 0.3 V
IOUTC	GNDQ	−0.3 V to VDDQ + 0.3 V
IOUTL	GNDP	−0.3 V to VDDP + 0.3 V
CLKP, CLKN	GNDC	−0.3 V to VDDC + 0.3 V
FREF	GNDL	−0.3 V to VDDL + 0.3 V
Maximum Junction Temperature		150°C
Storage Temperature		−65°C to +150°C
Maximum Lead Temperature		300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
48-Lead LFCSP	29.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

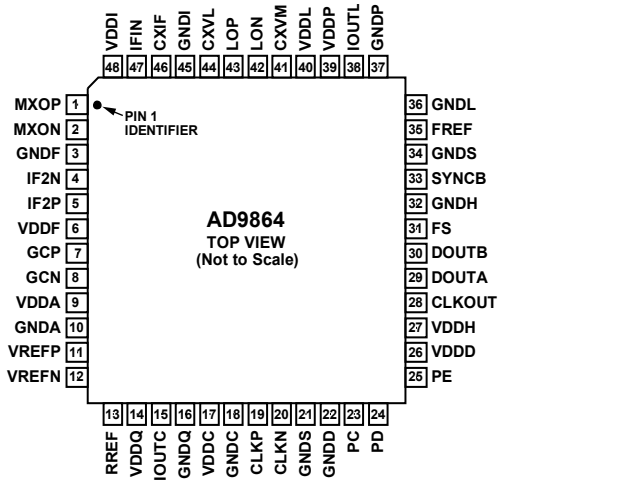

Figure 2. 48-Lead LFCSP Pin Configuration

Table 5. 48-Lead Lead Frame Chip Scale Package (LFCSP) Pin Function Descriptions

Pin No.	Mnemonic	Description
1	MXOP	Mixer Output, Positive.
2	MXON	Mixer Output, Negative.
3	GNDF	Ground for Front End of ADC.
4	IF2N	Second IF Input (to ADC), Negative.
5	IF2P	Second IF Input (to ADC), Positive.
6	VDDF	Positive Supply for Front End of ADC.
7	GCP	Filter Capacitor for ADC Full-Scale Control.
8	GCN	Full-Scale Control Ground.
9	VDDA	Positive Supply for ADC Back End.
10	GNDA	Ground for ADC Back End.
11	VREFP	Voltage Reference, Positive.
12	VREFN	Voltage Reference, Negative.
13	RREF	Reference Resistor: Requires 100 kΩ to GNDA.
14	VDDQ	Positive Supply for Clock Synthesizer.
15	IOUTC	Clock Synth Charge Pump Out Current.
16	GNDQ	Ground for Clock Synthesizer Charge Pump.
17	VDDC	Positive Supply for Clock Synthesizer.
18	GNDC	Ground for Clock Synthesizer.
19	CLKP	Sampling Clock Input/Clock VCO Tank, Positive.
20	CLKN	Sampling Clock Input/Clock VCO Tank, Negative.
21	GNDS	Substrate Ground.
22	GNDD	Ground for Digital Functions.
23	PC	Clock Input for SPI Port.
24	PD	Data I/O for SPI Port.
25	PE	Enable Input for SPI Port.
26	VDDD	Positive Supply for Internal Digital.
27	VDDH	Positive Supply for Digital Interface.
28	CLKOUT	Clock Output for SSI Port.
29	DOUTA	Data Output for SSI Port.
30	DOUTB	Data Output for SSI Port (Inverted) or SPI Port.
31	FS	Frame Sync for SSI Port.

Pin No.	Mnemonic	Description
32	GNDH	Ground for Digital Interface.
33	SYNCB	Resets SSI and Decimator Counters; Active Low. Connect to VDDH if unused.
34	GNDS	Substrate Ground.
35	FREF	Reference Frequency Input for Both Synthesizers.
36	GNDL	Ground for LO Synthesizer.
37	GNDP	Ground for LO Synthesizer Charge Pump.
38	IOUTL	LO Synthesizer Charge Pump Out Current.
39	VDDP	Positive Supply for LO Synthesizer Charge Pump.
40	VDDL	Positive Supply for LO Synthesizer.
41	CXVM	External Filter Capacitor; DC Output of LNA.
42	LON	LO Input to Mixer and LO Synthesizer, Negative.
43	LOP	LO Input to Mixer and LO Synthesizer, Positive.
44	CXVL	External Bypass Capacitor for LNA Power Supply.
45	GNDI	Ground for Mixer and LNA.
46	CXIF	External Capacitor for Mixer V-I Converter Bias.
47	IFIN	First IF Input (to LNA).
48	VDDI	Positive Supply for LNA and Mixer.
	EPAD	Exposed Pad. The backside paddle contact is not connected to ground. A PCB ground pad is optional.

TYPICAL PERFORMANCE CHARACTERISTICS

VDDI = VDDF = VDDA = VDDC = VDDL = VDDH = VDDx , VDDQ = VDDP = 2.7 V to 5.5 V, f_{CLK} = 18 MSPS, f_{IF} = 109.65 MHz, f_{LO} = 107.4 MHz, f_{REF} = 16.8 MHz, T_A=25 C°, LO and CLK synthesizer disabled, 16-bit data with AGC and DVGA enabled, unless otherwise noted.

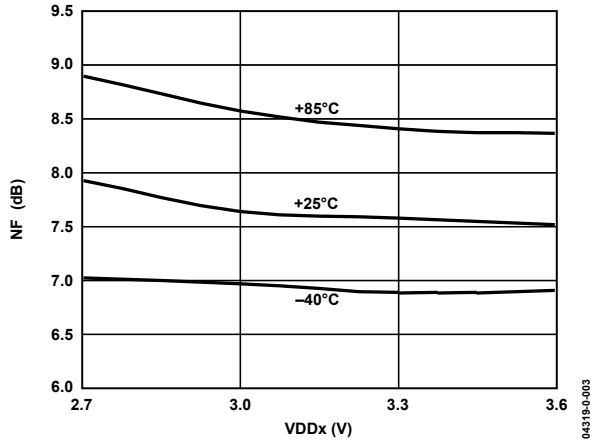

Figure 3. SSB Noise Figure vs. Supply

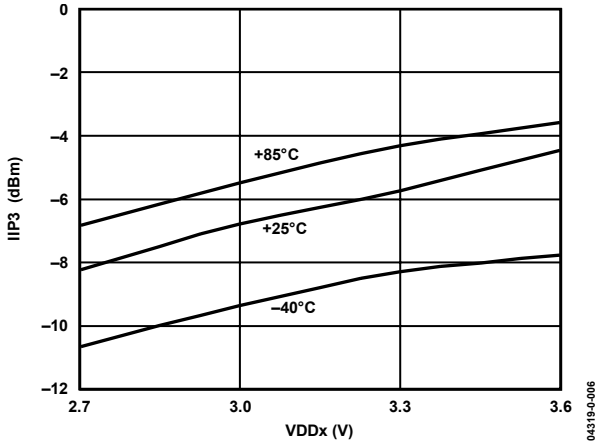

Figure 6. IIP3 vs. Supply

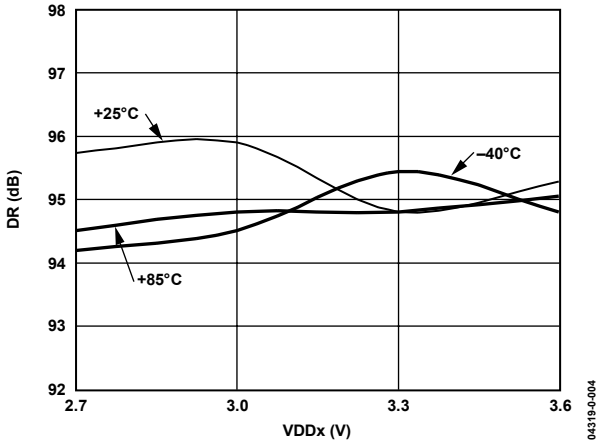

Figure 4. Dynamic Range (DR) vs. Supply

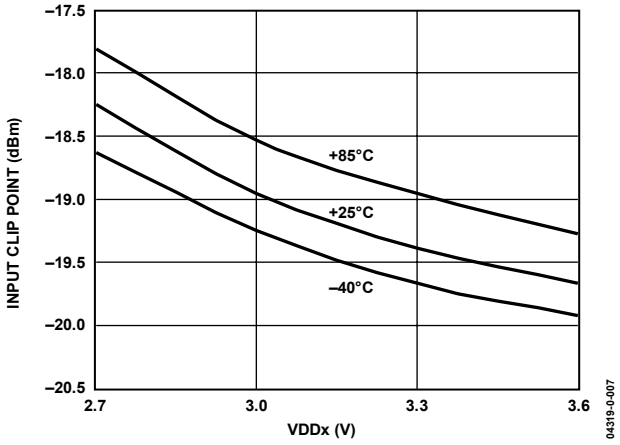

Figure 7. Maximum VGA Attenuation Clip Point vs. Supply

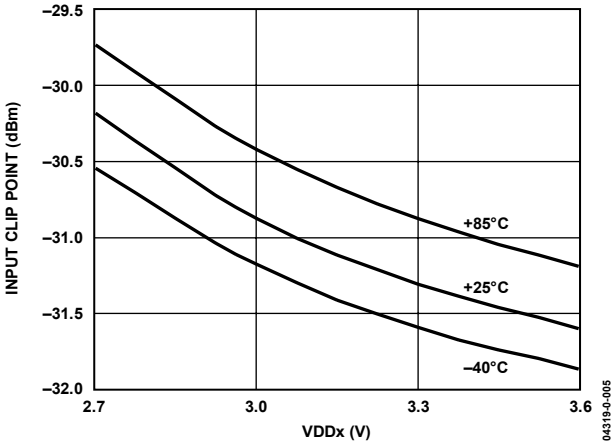

Figure 5. Minimum VGA Attenuation Clip Point vs. Supply

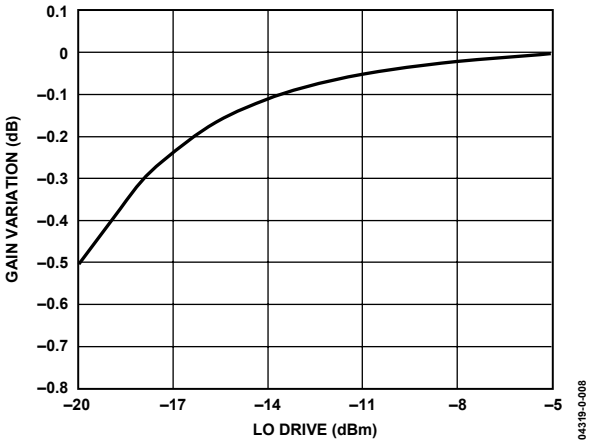

Figure 8. Normalized Gain Variation vs. LO Drive (VDDx = 3.0 V)

VDDI = VDDF = VDDA = VDDC = VDDL = VDDH = 3.0 V , VDDQ = VDDP = 2.7 V to 5.5 V, f_{CLK} = 18 MSPS, f_{IF} = 109.65 MHz, f_{LO} = 107.4 MHz, f_{REF} = 16.8 MHz, T_A=25 C°, LO and CLK synthesizer disabled, unless otherwise noted.

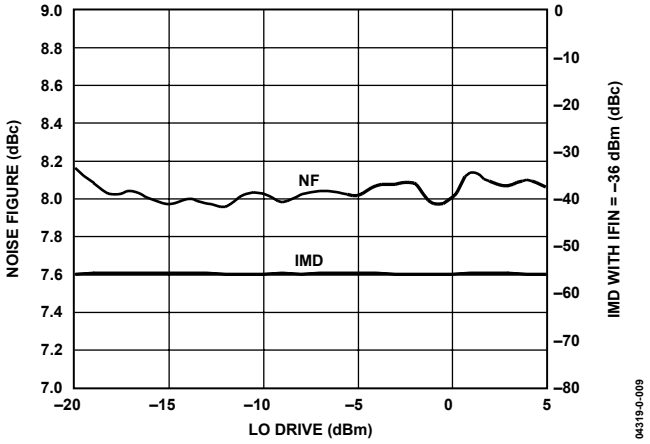

Figure 9. Noise Figure and IMD vs. LO Drive (VDDx = 3.0 V)

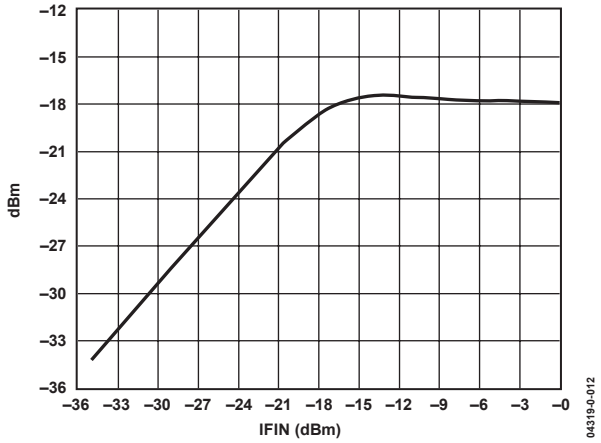

Figure 12. Gain Compression vs. IFIN with 16 dB LNA Attenuator Enabled

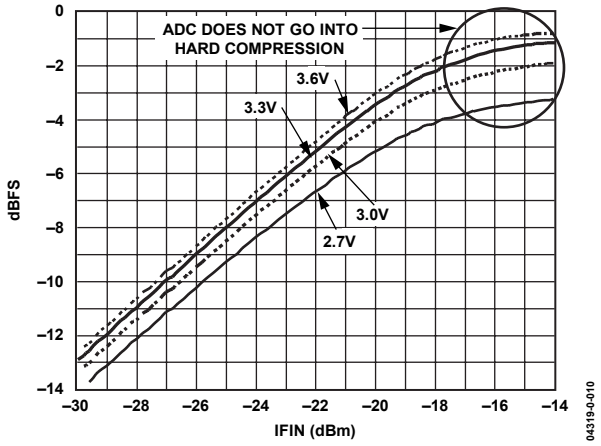

Figure 10. Gain Compression vs. IFIN

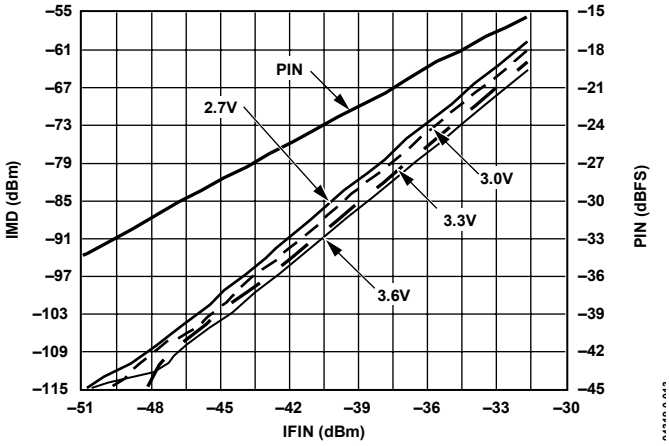

Figure 13. IMD vs. IFIN

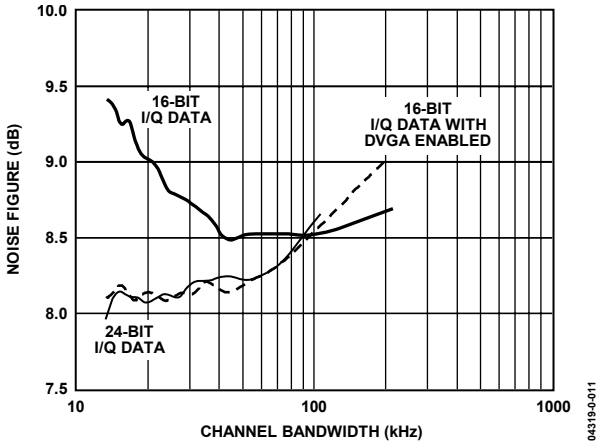

Figure 11. Noise Figure vs. Bandwidth (Minimum Attenuation, f_{CLK} = 13 MSPS)

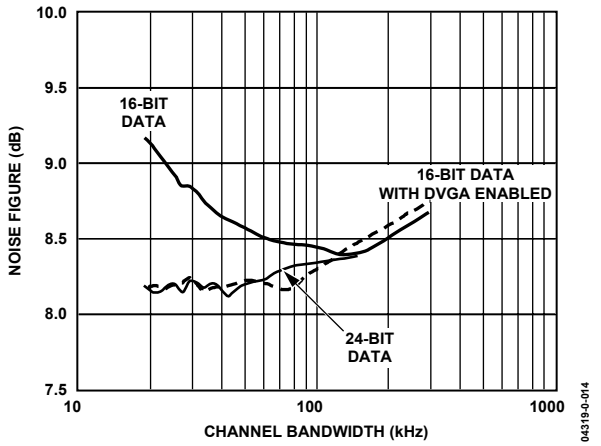

Figure 14. Noise Figure vs. Bandwidth (Minimum Attenuation, f_{CLK} = 18 MSPS)

VDDI = VDDF = VDDA = VDDC = VDDL = VDDH = 3.0 V , VDDQ = VDDP = 2.7 V to 5.5 V, f_{CLK} = 18 MSPS, f_{IF} = 109.65 MHz, f_{LO} = 107.4 MHz, f_{REF} = 16.8 MHz, T_A=25 C°, LO and CLK Synthesizer Disabled, unless otherwise noted.

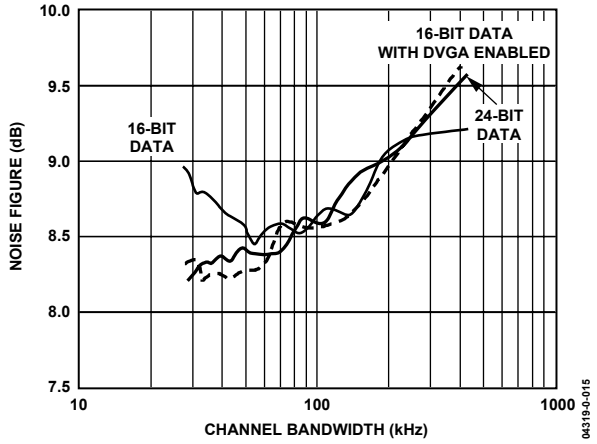

Figure 15. Noise Figure vs. Bandwidth (Minimum Attenuation, f_{CLK} = 26 MSPS)

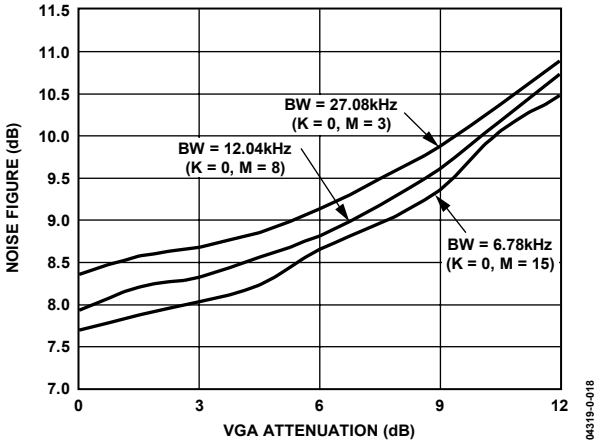

Figure 18. Noise Figure vs. VGA Attenuation (f_{CLK} = 13 MSPS)

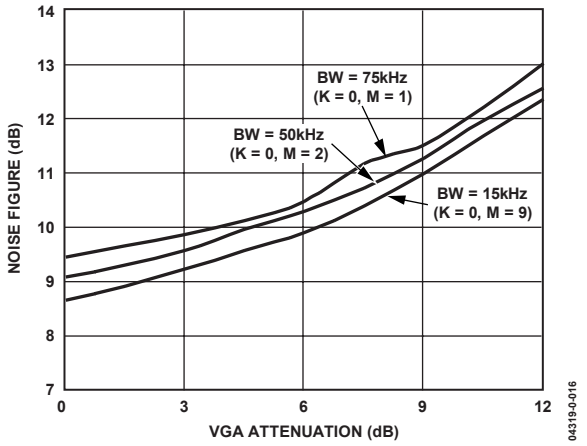

Figure 16. Noise Figure vs. VGA Attenuation (f_{CLK} = 18 MSPS)

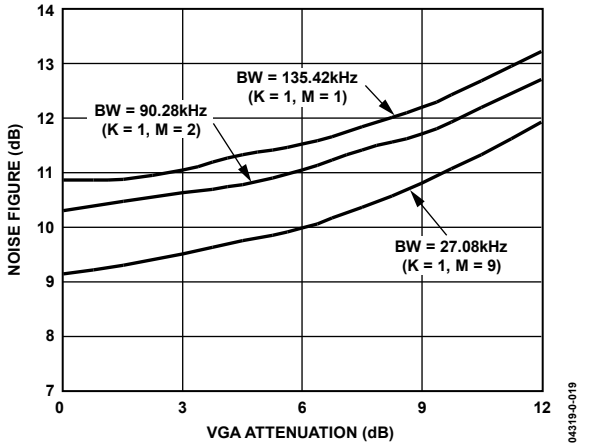

Figure 19. Noise Figure vs. VGA Attenuation (f_{CLK} = 26 MSPS)

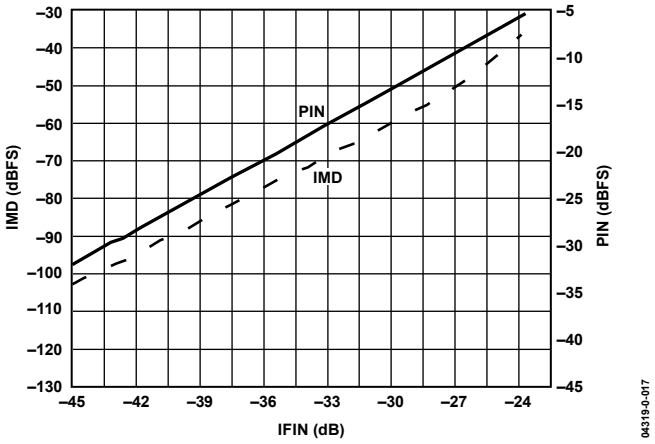

Figure 17. IMD vs. IFIN (f_{CLK} = 13 MSPS)

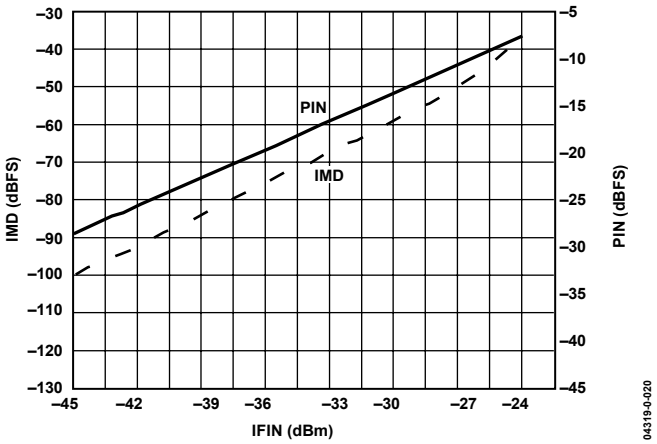

Figure 20. IMD vs. IFIN (f_{CLK} = 18 MSPS)

VDDI = VDDF = VDDA = VDDC = VDDL = VDDH = 3.0 V , VDDQ = VDDP = 2.7 V to 5.5 V, f_{CLK} = 18 MSPS, f_{IF} = 109.65 MHz, f_{LO} = 107.4 MHz, f_{REF} = 16.8 MHz, T_A=25 C°, LO and CLK synthesizer disabled, 16-bit data with AGC and DVGA enabled, unless otherwise noted.

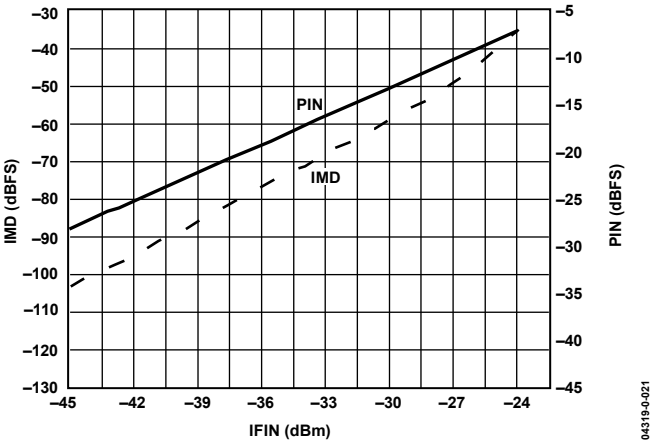

Figure 21. IMD vs. IFIN (f_{CLK} = 26 MSPS)

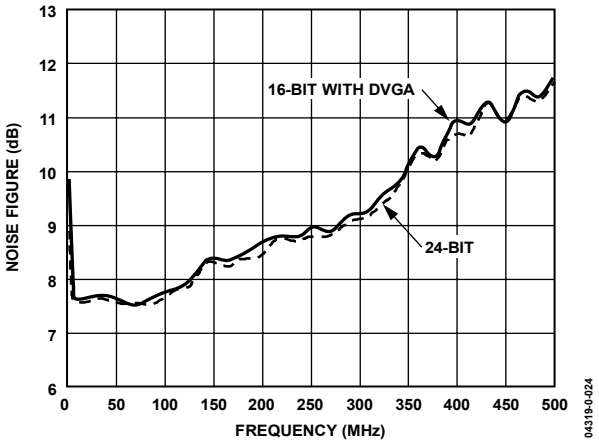

Figure 24. Noise Figure vs. Frequency (Minimum Attenuation, f_{CLK} = 18 MSPS, BW = 10 kHz)

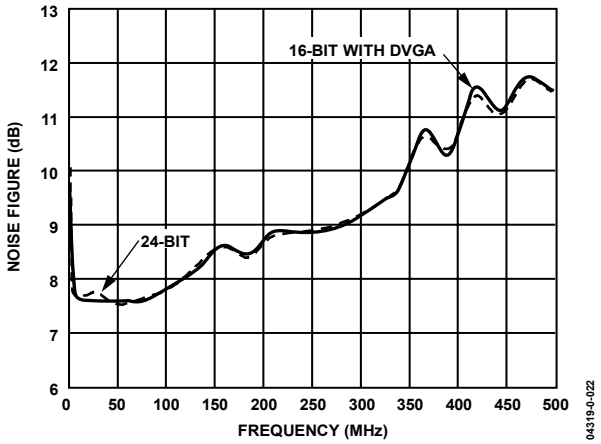

Figure 22. Noise Figure vs. Frequency (Minimum Attenuation, f_{CLK} = 26 MSPS, BW = 10 kHz)

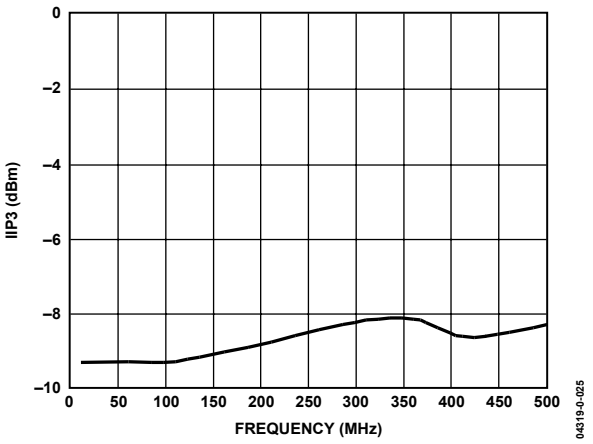

Figure 25. Input IIP3 vs. Frequency (f_{CLK} = 18 MSPS)

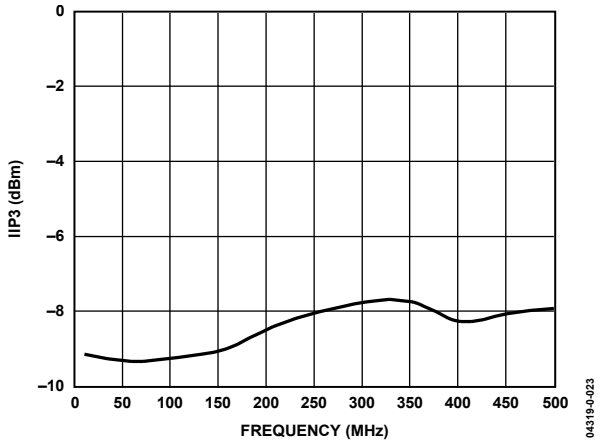

Figure 23. Input IIP3 vs. Frequency (f_{CLK} = 26 MSPS)

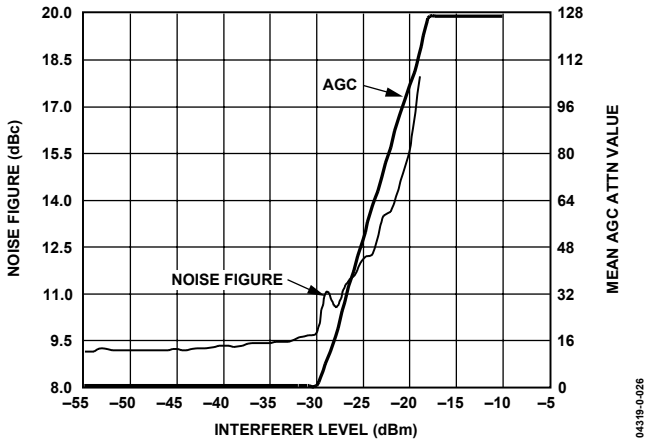

Figure 26. Noise Figure vs. Interferer Level (16-Bit Data, BW = 12.5 kHz, AGCR = 1, $f_{INTERFERER} = f_{IF} + 110$ kHz)

VDDI = VDDF = VDDA = VDDC = VDDL = VDDH = 3.0 V , VDDQ = VDDP = 2.7 V to 5.5 V, f_{CLK} = 18 MSPS, f_{IF} = 109.65 MHz, f_{LO} = 107.4 MHz, f_{REF} = 16.8 MHz, T_A=25 C°, LO and CLK Synthesizer Disabled, AGC enabled, unless otherwise noted.

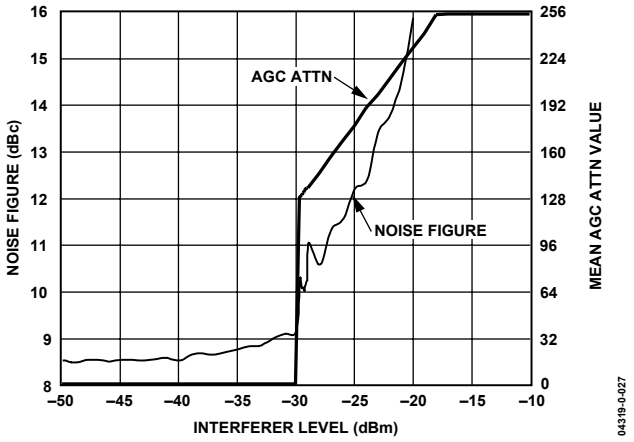

Figure 27. Noise Figure vs. Interferer Level (16-Bit Data with DVGA, BW = 12.5 kHz, AGCR = 1, $f_{INTERFERER} = f_{IF} + 110$ kHz)

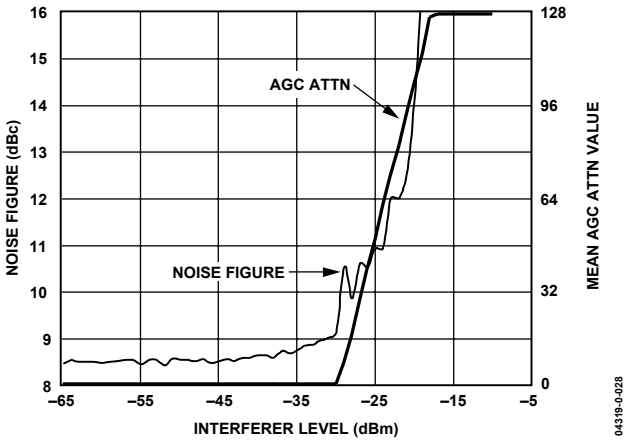

Figure 28. Noise Figure vs. Interferer Level (24-Bit Data, BW = 12.5 kHz, AGCR = 1, $f_{INTERFERER} = f_{IF} + 110$ kHz)

TERMINOLOGY

Single Sideband Noise Figure (SSB NF)

Noise figure (NF) is defined as the degradation in SNR performance (in dB) of an IF input signal after it passes through a component or system. It can be expressed with the equation

$$Noise\ Figure = 10 \times \log(SNR_{IN}/SNR_{OUT})$$

The term SSB is applicable for heterodyne systems containing a mixer. It indicates that the desired signal spectrum resides on only one side of the LO frequency (that is, single sideband); therefore, a noiseless mixer has a noise figure of 3 dB.

The SSB noise figure of the AD9864 is determined by the equation

$$SSB\ NF = P_{IN} - [10 \times \log(BW)] - (-174\ \text{dBm/Hz}) - SNR$$

where:
P_{IN} is the input power of an unmodulated carrier.
BW is the noise measurement bandwidth.
−174 dBm/Hz is the thermal noise floor at 293 K.
SNR is the measured signal-to-noise ratio in dB of the AD9864.

Note that P_{IN} is set to −85 dBm to minimize any degradation in measured SNR due to phase noise from the RF and LO signal generators. The IF frequency, CLK frequency, and decimation factors are selected to minimize any spurious components falling within the measurement bandwidth. Note also that a bandwidth of 10 kHz is used for the data sheet specification. All references to noise figures within this data sheet imply single sideband noise figure.

Input Third-Order Intercept (IIP3)

IIP3 is a figure of merit used to determine the susceptibility of a component or system to intermodulation distortion (IMD) from its third-order nonlinearities. Two unmodulated carriers at a specified frequency relationship (f1 and f2) are injected into a nonlinear system exhibiting third-order nonlinearities producing IMD components at 2f1 − f2 and 2f2 − f1. IIP3 graphically represents the extrapolated intersection of the carrier's input power with the third-order IMD component when plotted in dB. The difference in power (D in dBc) between the two carriers, and the resulting third-order IMD components can be determined from the equation

$$D = 2 \times (IIP3 - P_{IN})$$

Dynamic Range (DR)

Dynamic range is the measure of a small target input signal (P_{TARGET}) in the presence of a large unwanted interferer signal (P_{INTER}). Typically, the large signal causes some unwanted characteristic of the component or system to degrade, thus making it unable to detect the smaller target signal correctly. For the AD9864, it is often a degradation in noise figure at increased VGA attenuation settings that limits its dynamic range.

The test method for the AD9864 is as follows. The small target signal (an unmodulated carrier) is input at the center of the IF frequency, and its power level (P_{TARGET}) is adjusted to achieve an SNR_{TARGET} of 6 dB. The power of the signal is then increased by 3 dB prior to injecting the interferer signal. The offset frequency of the interferer signal is selected so that aliases produced by the response of the decimation filter, as well as phase noise from the LO (due to reciprocal mixing), do not fall back within the measurement bandwidth. For this reason, an offset of 110 kHz was selected. The interferer signal (also an unmodulated carrier) is then injected into the input and its power level is increased to the point (P_{INTER}) where the target signal SNR is reduced to 6 dB. The dynamic range is determined with the equation

$$DR = P_{INTER} - P_{TARGET} + SNR_{TARGET}$$

Note that the AGC of the AD9864 is enabled for this test.

IF Input Clip Point

The IF input clip point is defined as the input power that results in a digital output level 2 dB below full scale. Unlike other linear components that typically exhibit a soft compression (characterized by its 1 dB compression point), an ADC exhibits a hard compression when its input signal exceeds its rated maximum input signal range. For the AD9864, which contains a Σ-Δ ADC, hard compression must be avoided because it causes severe SNR degradation.

SERIAL PERIPHERAL INTERFACE (SPI)

The SPI is a bidirectional serial port. It is used to load the configuration information into the registers listed in Table 6, as well as to read back their contents. Table 6 provides a list of the registers that can be programmed through the SPI port. Addresses and default values are given in hexadecimal form.

Table 6. SPI Address Map

Address (Hex)	Bit(s)	Width	Default Value	Name	Description
Power Control Registers					
0x00	[7:0]	8	0xFF	STBY	Standby control bits (REF, LO, CKO, CK, GC, LNAMX, unused, and ADC). Default is power-up condition of standby.
0x01	[3:2]	2	0x00	CKOB	CK oscillator bias (0 = 0.25 mA, 1 = 0.35 mA, 2 = 0.40 mA, 3 = 0.65 mA).
	[1:0]	2	0x00	ADCB	Do not use.
0x02	[7:0]	8	0x00	TEST	Factory test mode. Do not use.
AGC					
0x03	7	1	0	ATTEN	Apply 16 dB attenuation in the front end.
	[6:0]	7	0x00	AGCG [14:8]	AGC attenuation setting (7 MSBs of a 15-bit unsigned word).
0x04	[7:0]	8	0x00	AGCG [7:0]	AGC attenuation setting (8 LSBs of a 15-bit unsigned word).
0x05	[7:4]	4	0x00	AGCA	AGC attack bandwidth setting. Default yields 50 Hz loop bandwidth.
	[3:0]	4	0x00	AGCD	AGC decay time setting. Default is decay time = attack time.
0x06	7	1	0	AGCV	Enable digital VGA to increase AGC range by 12 dB.
	[6:4]	3	0x00	AGCO	AGC overload update setting. Default is slowest update.
	3	1	0	AGCF	Fast AGC (minimizes resistance seen between GCP and GCN).
	[2:0]	3	0x00	AGCR	AGC enable/reference level (disabled, 3 dB, 6 dB, 9 dB, 12 dB, 15 dB below clip).
Decimation Factor					
0x07	[7:5]	3		Unused	
	4	1	0	K	Decimation factor = 60 × (M + 1), if K = 0; 48 × (M + 1), if K = 1.
	[3:0]	4	0x04	M	Default is decimate-by-300.
LO Synthesizer					
0x08	[5:0]	6	0x00	LOR [13:8]	Reference frequency divider (6 MSBs of a 14-bit word).
0x09	[7:0]	8	0x38	LOR [7:0]	Reference frequency divisor (8 LSBs of a 14-bit word). Default (56) yields 300 kHz from f_{REF} = 16.8 MHz.
0x0A	[7:5]	3	0x05	LOA	A counter (prescaler control counter).
	[4:0]	5	0x00	LOB [12:8]	B counter MSB (5 MSB of a 13-bit word). Default LOA and LOB values yield 300 kHz from 73.35 MHz to 2.25 MHz.
0x0B	[7:0]	8	0x1D	LOB [7:0]	B counter LSB (8 LSB of a 13-bit word).
0x0C	6	1	0	LOF	Enable fast acquire.
	5	1	0	LOINV	Invert charge pump (0 = source current to increase VCO frequency).
	[4:2]	3	0x00	LOI	Charge pump current in normal operation. I_{PUMP} = (LOI +1) × 0.625 mA.
	[1:0]	2	0x03	LOTM	Manual control of LO charge pump (0 = off, 1 = up, 2 = down, and 3 = normal).
0x0D	[5:0]	6	0x00	LOFA [13:8]	LO fast acquire time unit (6 MSBs of a 14-bit word).
0x0E	[7:0]	8	0x04	LOFA [7:0]	LO fast acquire time unit (8 LSBs of a 14-bit word).
Clock Synthesizer					
0x10	[5:0]	6	0x00	CKR [13:8]	Reference frequency divisor (6 MSBs of a 14-bit word).
0x11	[7:0]	8	0x38	CKR [7:0]	Reference frequency divisor (8 LSBs of a 14-bit word). Default yields 300 kHz from f_{REF} = 16.8 MHz; minimum = 3, maximum = 16383.
0x12	[4:0]	5	0x00	CKN [12:8]	Synthesized frequency divisor (5 MSBs of a 13-bit word).
0x13	[7:0]	8	0x3C	CKN [7:0]	Synthesized frequency divisor (8 LSBs of a 13-bit word). Default yields 300 kHz from 18 MHz; minimum = 3, maximum = 8191.

Address (Hex)	Bit(s)	Width	Default Value	Name	Description
0x14	6	1	0	CKF	Enable fast acquire.
	5	1	0	CKINV	Invert charge pump (0 = source current to increase VCO frequency).
	[4:2]	3	0x00	CKI	Charge pump current in normal operation. I_{PUMP} = (CKI + 1) × 0.625 mA.
	[1:0]	2	0x03	CKTM	Manual control of CLK charge pump (0 = off, 1 = up, 2 = down, and 3 = normal).
0x15	[5:0]	6	0x00	CKFA [13:8]	CK fast acquire time unit (6 LSBs of a 14-bit word).
0x16	[7:0]	8	0x04	CKFA [7:0]	CK fast acquire time unit (8 LSBs of a 14-bit word).
SSI Control					
0x18	[7:0]	8	0x12	SSICRA	SSI Control Register A. See the SSI Control Registers section. Default is FS and CLKOUT three-stated.
0x19	[7:0]	8	0x07	SSICRB	SSI Control Register B. See the SSI Control Registers section (16-bit data, maximum drive strength).
0x1A	[3:0]	4	0x01	SSIORD	Output rate divisor. $f_{CLKOUT} = f_{CLK}$/SSIORD.
ADC Tuning					
0x1C	1	1	0	TUNE_LC	Perform tuning on LC portion of the ADC (cleared when done).
	0	1	0	TUNE_RC	Perform tuning on RC portion of the ADC (cleared when done).
0x1D	[3:0]	3	0x00	CAPL1 [2:0]	Coarse capacitance setting of LC tank (LSB is 25 pF, differential).
0x1E	[5:0]	6	0x00	CAPL0 [5:0]	Fine capacitance setting of LC tank (LSB is 0.4 pF, differential).
0x1F	[7:0]	8	0x00	CAPR	Capacitance setting for RC resonator (64 LSB of fixed capacitance).
Test Registers and SPI Port Read Enable					
0x37	[7:0]	8	0x00	TEST	Factory test mode. Do not use.
0x38	[7:1]	7	0x00	TEST	Factory test mode. Do not use.
	0	1	0	DACCR	Manual feedback DAC control
0x39	[7:0]	8	0x00	DACDATA	Feedback DAC data setting in manual mode.
0x3A	[7:4]	4	0x00	TEST	Factory test mode. Do not use.
	3	1	0	SPIREN	Enable read from SPI port.
	[2:0]	3	0x00	TEST	Factory test mode. Do not use.
0x3B	[7:4]	4	0x00	TEST	Factory test mode. Do not use.
	3	1	0	TRI	Three-state DOUTB.
	[2:0]	3	0x00	TEST	Factory test mode. Do not use.
0x3C to 0x3D	[7:0]	8	0x00	TEST	Factory test mode. Do not use.
0x3E	7	1	0	TEST	Factory test mode. Do not use.
	6	1	0	OVL	ADC overload detector.
	[5:3]	3	0	TEST	Factory test mode. Do not use.
	2	2	0	RC_Q	RC Q enhancement.
	1	1	0	RC_BYP	Bypass RC resonator.
	0	1	0	SC_BYP	Bypass SC resonators.
0x3F	[7:0]	8	Subject to change	ID	Revision ID (read-only). A write of 0x99 to this register is equivalent to a power-on reset.

THEORY OF OPERATION

INTRODUCTION

The AD9864 is a general-purpose, narrow-band IF subsystem that digitizes a low level, 10 MHz to 300 MHz IF input with a signal bandwidth ranging from 6.8 kHz to 270 kHz. The signal chain of the AD9864 consists of an LNA, a mixer, a band-pass Σ-Δ ADC, and a decimation filter with programmable decimation factor.

The input LNA is a fixed gain block with an input impedance of approximately 370 Ω||1.4 pF. The LNA input is single-ended and self biasing, allowing the input IF to be ac-coupled. The LNA can be disabled through the serial interface, providing a fixed 16 dB attenuation to the input signal.

The LNA drives the input port of a Gilbert-type active mixer. The mixer LO port is driven by the on-chip LO buffer, which can be driven externally, single-ended, or differential. The LO buffer inputs are self biasing and allow the LO input to be ac-coupled. The open-collector outputs of the mixer drive an external resonant tank consisting of a differential LC network tuned to the IF of the band-pass Σ-Δ ADC.

The external differential LC tank forms the resonator for the first stage of the band-pass Σ-Δ ADC. The tank LC values must be selected for a center frequency of $f_{CLK}/8$, where f_{CLK} is the sample rate of the ADC. The $f_{CLK}/8$ frequency is the IF digitized by the band-pass Σ-Δ ADC. On-chip calibration allows standard tolerance inductor and capacitor values. The calibration is typically performed once at power-up.

The ADC contains a sixth-order, multibit band-pass Σ-Δ modulator that achieves very high instantaneous dynamic range over a narrow frequency band centered at $f_{CLK}/8$. The modulator output is quadrature mixed to baseband and filtered by three cascaded linear phase FIR filters to remove out-of-band noise.

The first FIR filter is a fixed, decimate by 12, using a fourth-order comb filter. The second FIR filter also uses a fourth-order comb filter with programmable decimation from 1 to 16. The third FIR stage is programmable for decimation of either 4 or 5.

The cascaded decimation factor is programmable from 48 to 960. The decimation filter data is output via the synchronous serial interface (SSI) of the chip.

Additional functionality built into the AD9864 includes LO and clock synthesizers, programmable AGC, and a flexible synchronous serial interface for output data.

The LO synthesizer is a programmable phase-locked loop (PLL) consisting of a low noise phase frequency detector (PFD), a variable output current charge pump (CP), a 14-bit reference divider, A and B counters, and a dual modulus prescaler. The user only needs to add an appropriate loop filter and VCO for complete operation.

The clock synthesizer is equivalent to the LO synthesizer with the following differences:

- It does not include the prescaler or A counter.
- It includes a negative resistance core used for VCO generation.

The AD9864 contains both a variable gain amplifier (VGA) and a digital VGA (DVGA). Both of these can operate manually or automatically. In manual mode, the gain for each is programmed through the SPI. In automatic gain control mode, the gains are adjusted automatically to ensure that the ADC does not clip and that the rms output level of the ADC is equal to a programmable reference level.

The VGA has 12 dB of attenuation range and is implemented by adjusting the ADC full-scale reference level. The DVGA gain is implemented by scaling the output of the decimation filter. The DVGA is most useful in extending the dynamic range in narrow-band applications requiring 16-bit I and Q data format.

The SSI provides a programmable frame structure, allowing 24-bit or 16-bit I and Q data and flexibility by including attenuation and RSSI data if required.

SERIAL PORT INTERFACE (SPI)

The serial port of the AD9864 has 3-wire or 4-wire SPI capability, allowing read/write access to all registers that configure the internal parameters of the device. The default 3-wire serial communication port consists of a clock (PC), peripheral enable (PE), and bidirectional data (PD) signal. The inputs to PC, PE, and PD contain a Schmitt trigger with a nominal hysteresis of 0.4 V centered about the digital interface supply, that is, VDDH/2.

A 4-wire SPI interface can be enabled by setting the MSB of the SSICRB register (Register 0x19, Bit 7) and setting Register 0x3A to 0x00, resulting in the output data appearing on only the DOUTB pin with the PD pin functioning as an input pin only. Note that because the default power-up state sets DOUTB low, bus contention is possible for systems sharing the SPI output line. To avoid any bus contention, the DOUTB pin can be three-stated by setting the fourth control bit in the three-state bit (Register 0x3B, Bit 3). This bit can then be toggled to gain access to the shared SPI output line.

An 8-bit instruction header must accompany each read and write SPI operation. Only the write operation supports an auto-increment mode, which allows the entire chip to be configured in a single write operation. The instruction header is shown in Table 7. It includes a read/not-write indicator bit, six address bits, and a Don't Care bit. The data bits immediately follow the instruction header for both read and write operations. Note that the address and data are always given MSB first.

Table 7. Instruction Header Information

MSB							LSB
I7	**I6**	**I5**	**I4**	**I3**	**I2**	**I1**	**I0**
R/W	A5	A4	A3	A2	A1	A0	X[1]

[1] X = don't care.

Figure 29 illustrates the timing requirements for a write operation to the SPI port. After the peripheral enable (PE) signal goes low, data (PD) pertaining to the instruction header is read on the rising edges of the clock (PC). To initiate a write operation, the read/not-write bit is set low. After the instruction header is read, the eight data bits pertaining to the specified register are shifted into the data pin (PD) on the rising edges of the next eight clock cycles. PE stays low during the operation and goes high at the end of the transfer. If PE rises before the eight clock cycles have passed, the operation is aborted. If PE stays low for an additional eight clock cycles, the destination address is incremented and another eight bits of data are shifted in. Again, if PE rises early, the current byte is ignored. By using this implicit addressing mode, the chip can be configured with a single write operation. Registers identified as being subject to frequent updates, namely those associated with power control and AGC operation, have been assigned adjacent addresses to minimize the time required to update them. Note that multibyte registers are big endian (the most significant byte has the lower address) and are updated when a write to the least significant byte occurs.

Figure 30 and Figure 31 illustrates the timing for 3-wire and 4-wire SPI read operations. Although the AD9864 does not require read access for proper operation, it is often useful in the product development phase or for system authentication. Note that the readback enable bit (Register 0x3A, Bit 3) must be set for a read operation with a 3-wire SPI interface. For 4-wire SPI operation, this bit remains low (Register 0x3A = 0x00) but DOUTB is enabled via the SSICRB register (Register 0x19, Bit 7). Note that for the 4-wire SPI interface, the eight data bits appear on the DOUTB pin with the same timing relationship as those appearing at PD for 3-wire SPI interface case.

After the peripheral enable (PE) signal goes low, data (PD) pertaining to the instruction header is read on the rising edges of the clock (PC). A read operation occurs if the read/not-write indicator is set high. After the address bits of the instruction header are read, the eight data bits pertaining to the specified register are shifted out of the data pin (PD) on the falling edges of the next eight clock cycles. After the last data bit is shifted out, the user must return PE high, causing PD to become three-stated (for 3-wire case) and return to its normal status as an input pin. Since the auto-increment mode is not supported for read operations, an instruction header is required for each register read operation and PE must return high before initiating the next read operation.

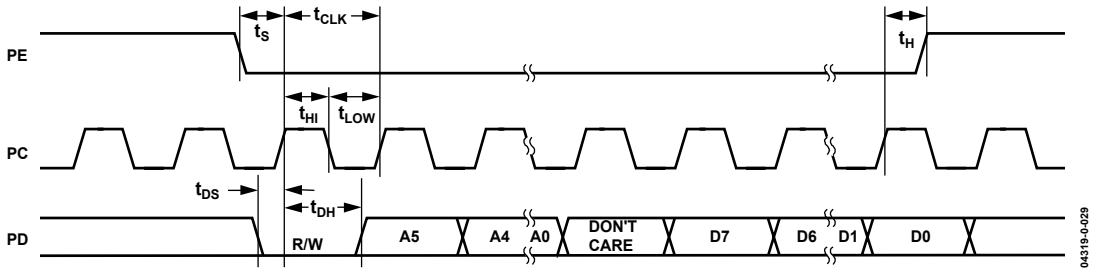

Figure 29. SPI Write Operation Timing

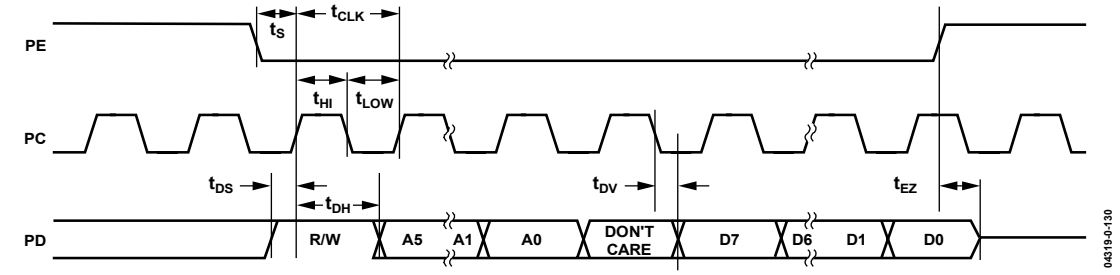

Figure 30. 3-Wire SPI Read Operation Timing

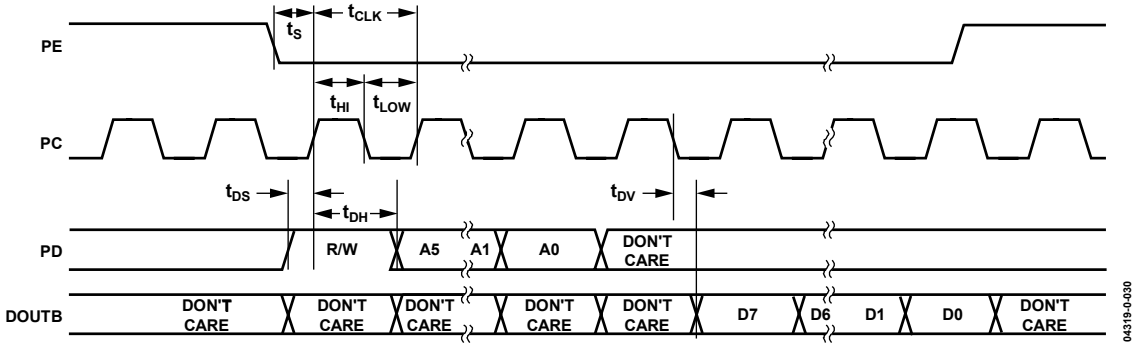

Figure 31. 4-Wire SPI Read Operation Timing

POWER-ON RESET

The SPI registers are automatically set to their default settings upon power-up when the VDDD supply crosses a threshold. This ensures that the AD9864 is in a known state and placed in standby for minimal power consumption. In the unlikely event that the SPI registers were not reset to their default settings, an equivalent software reset by writing 0x99 to Register 0x3F can be used as the first SPI write command to provide additional assurance.

SYNCHRONOUS SERIAL INTERFACE (SSI)

The AD9864 provides a high degree of programmability of its SSI output data format, control signals, and timing parameters to accommodate various digital interfaces. In a 3-wire digital interface, the AD9864 provides a frame sync signal (FS), a clock output (CLKOUT), and a serial data stream (DOUTA) signal to the host device. In a 2-wire interface, the frame sync information is embedded into the data stream, thus only CLKOUT and DOUTA output signals are provided to the host device. The SSI control registers are SSICRA, SSICRB, and SSIORD. Table 8 to Table 13 show the bit fields associated with these registers.

The primary output of the AD9864 is the converted I and Q demodulated signal available from the SSI port as a serial bit stream contained within a frame. The output frame rate is equal to the modulator clock frequency (f_{CLK}) divided by the digital filter's decimation factor that is programmed in the Decimator Register (0x07). The bit stream consists of an I word followed by a Q word, where each word is either 24 bits or 16 bits long and is given MSB first in twos complement form. Two optional bytes may also be included within the SSI frame following the Q word. One byte contains the AGC attenuation and the other byte contains both a count of modulator reset events and an estimate of the received signal amplitude (relative to full scale of the AD9864 ADC). Figure 32 illustrates the structure of the SSI data frames in a number of SSI modes.

The two optional bytes are output if the EAGC bit of SSICRA is set. The first byte contains the 8-bit attenuation setting (0 = no attenuation, 255 = 24 dB of attenuation), whereas the second byte contains a 2-bit reset field and 6-bit received signal strength field. The reset field contains the number of modulator reset events since the last report, saturating at 3. The received signal strength (RSSI) field is a linear estimate of the signal strength at the output of the first decimation stage; 60 corresponds to a full-scale signal.

The two optional bytes follow the I and Q data as a 16-bit word provided that the AAGC bit of SSICRA is not set. If the AAGC bit is set, the two bytes follow the I and Q data in an alternating fashion. In this alternate AGC data mode, the LSB of the byte containing the AGC attenuation is a 0, whereas the LSB of the byte containing reset and RSSI information is always a 1.

In a 2-wire interface, the embedded frame sync bit (EFS) within the SSICRA register is set to 1. In this mode, the framing information is embedded in the data stream, with each eight bits of data surrounded by a start bit (low) and a stop bit (high), and each frame ends with at least 10 high bits. FS remains either low or three-stated (default), depending on the state of the SFST bit. Other control bits can be used to invert the frame sync (SFSI), to delay the frame sync pulse by one clock period (SLFS), to invert the clock (SCKI), or to three-state the clock (SCKT). Note that if EFS is set, SLFS is a don't care bit.

The SSIORD register controls the output bit rate (f_{CLKOUT}) of the serial bit stream. f_{CLKOUT} can be set equal to the modulator clock frequency (f_{CLK}) or an integer fraction of it. It is equal to f_{CLK} divided by the contents of the SSIORD register. Note that f_{CLKOUT} must be chosen such that it does not introduce harmful spurs within the pass band of the target signal. Users must verify that the output bit rate is sufficient to accommodate the required number of bits per frame for a selected word size and decimation factor. Idle (high) bits are used to fill out each frame.

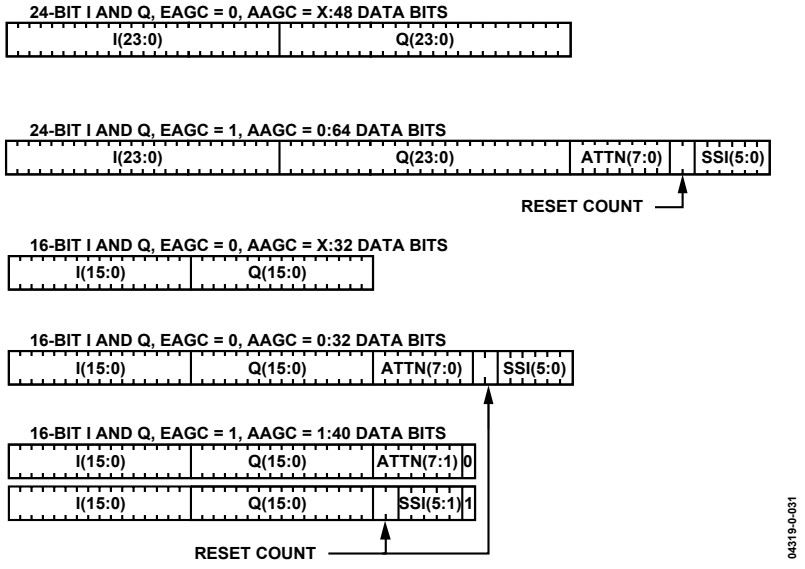

Figure 32. SSI Frame Structure

SSI CONTROL REGISTERS

SSICRA (Address 0x18)

Table 8. SSICRA Bitmap

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AAGC	EAGC	EFS	SFST	SFSI	SLFS	SCKT	SCKI

Table 9. SSICRA Bit Descriptions

Bit(s)	Name	Width	Default	Description
7	AAGC	1	0	Alternate AGC data bytes.
6	EAGC	1	0	Embed AGC data.
5	EFS	1	0	Embed frame sync.
4	SFST	1	1	Three-state frame sync.
3	SFSI	1	0	Invert frame sync.
2	SLFS	1	0	Late frame sync (1 = late, 0 = early).
1	SCKT	1	1	Three-state CLKOUT.
0	SCKI	1	0	Invert CLKOUT.

SSICRB (Address 0x19)

Table 10. SSICRB Bitmap

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
4_SPI	Reserved	Reserved	Reserved	DW	DS_2	DS_1	DS_0

Table 11. SSICRB Bit Descriptions

Bit(s)	Name	Width	Default	Description
7	4_SPI	1	0	Enable 4-wire SPI interface for SPI read operation via DOUTB.
[6:4]	Reserved	3	0	Reserved.
3	DW	1	0	I/Q data-word width (0 = 16 bit, 1 = 24 bit). Automatically 16-bit when AGCV = 1.
[2:0]	DS	3	7	FS, CLKOUT, and DOUT drive strength Level 0 to Level 7, with 7 being the highest level.

SSIORD (Address 0x1A)

Table 12. SSIORD Bitmap

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	DIV_3	DIV_2	DIV_1	DIV_0

Table 13. SSIORD Bit Descriptions

Bit(s)	Name	Width	Default	Description
[7:4]	Reserved	4	0	Reserved.
[3:0]	SSIORD	4	1	Output bit rate divisor setting $f_{CLKOUT} = f_{CLK}$/SSIORD where SSIORD = 1 to 15.

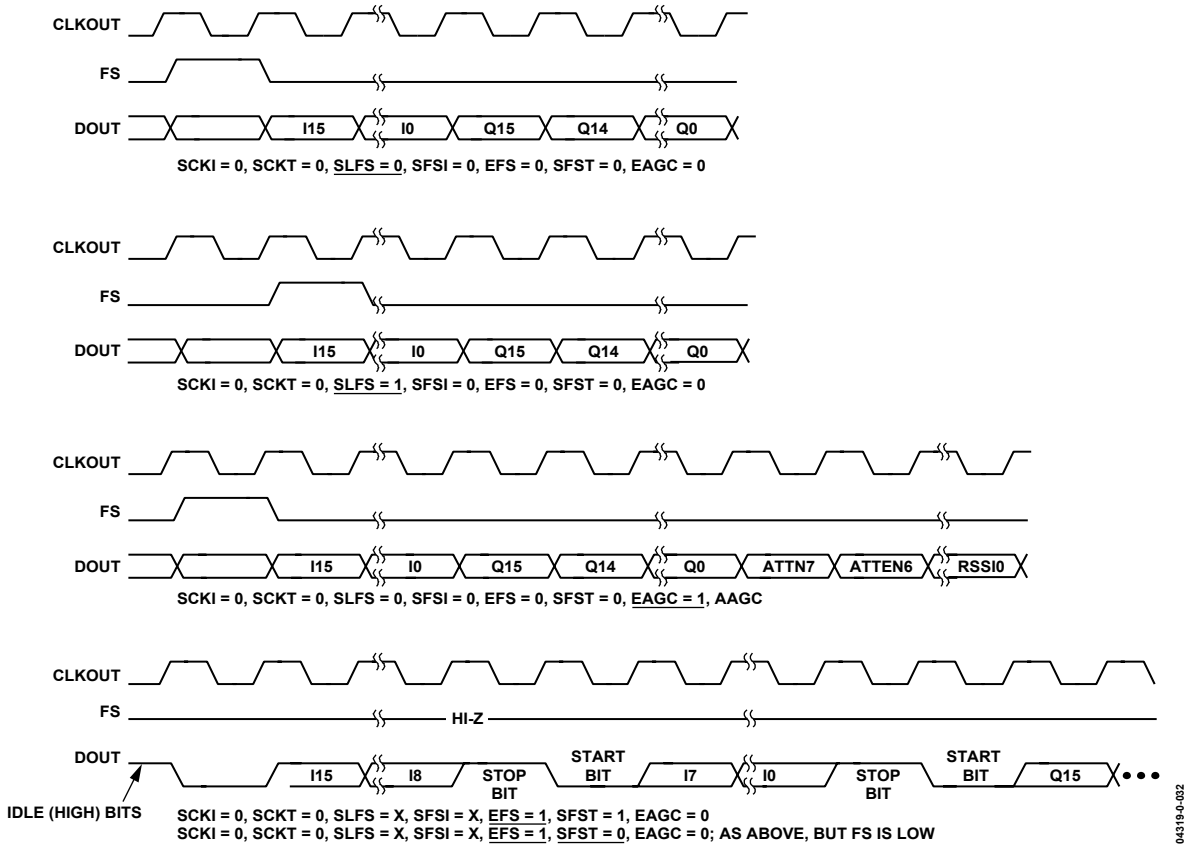

Figure 33. SSI Timing for Several SSICRA Settings with 16-Bit I/Q Data

Table 14. Number of Bits per Frame for Different SSICR Settings

DW	EAGC	EFS	AAGC	Number of Bits per Frame
0 (16 Bits)	0	0	N/A	32
	0	1	N/A	49[1]
	1	0	0	48
	1	0	1	40
	1	1	0	69[1]
	1	1	1	59[1]
1 (24 Bits)	0	0	N/A	48
	0	1	N/A	69[1]
	1	0	0	64
	1	0	1	56
	1	1	0	89[1]
	1	1	1	79[1]

[1] The number of bits per frame with embedded frame sync (EFS = 1); assume at least 10 idle bits are desired.
[2] N/A means not applicable.

The maximum SSIORD setting can be determined by the following equation:

$$SSIORD < TRUNC[(Decimation\ Factor)/(Number\ of\ Bits\ per\ Frame)] \quad (1)$$

where *TRUNC* is the truncated integer value.

If SSIORD = (decimation factor)/(number of bits per frame), the last bit in the SSI frame is not clocked out prior to FS returning high.

Table 14 lists the number of bits within a frame for 16-bit and 24-bit output data formats for all of the different SSICR settings. The decimation factor is determined by the contents of Register 0x07.

An example helps illustrate how the maximum SSIORD setting is determined. Suppose a user selects a decimation factor of 600 (Register 0x07, K = 0, M = 9) and prefers a 3-wire interface with a dedicated frame sync (EFS = 0) containing 24-bit data (DW = 1) with nonalternating embedded AGC data included (EAGC = 1, AAGC = 0). Referring to Table 14, each frame consists of 64 data bits. Using Equation 1, the maximum SSIORD setting is 9 (= *TRUNC*(600/64)). Therefore, the user can select any SSIORD setting between 1 and 9.

Figure 33 illustrates the output timing of the SSI port for several SSI control register settings with 16-bit I/Q data, and Figure 34 shows the associated timing parameters. Note that the same timing relationship holds for 24-bit I/Q data, with the exception that I and Q word lengths now become 24 bits. In the default mode of operation, data is shifted out on rising edges of CLKOUT after a pulse equal to a clock period is output from the frame sync (FS) pin. As described above, the output data consists of a 16-bit or 24-bit I sample followed by a 16-bit or 24-bit Q sample, plus two optional bytes containing AGC and status information.

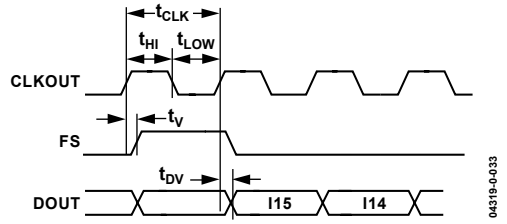

Figure 34. SSI Timing Parameters for SSI Timing

In Figure 34, the timing parameters also apply to inverted CLKOUT or FS modes, with t_{DV} relative to the falling edge of the CLK and/or FS.

The AD9864 also provides the means for controlling the switching characteristics of the digital output signals via the drive strength (DS) field of the SSICRB. This feature is useful in limiting switching transients and noise from the digital output that may ultimately couple back into the analog signal path, potentially degrading the sensitivity performance of the AD9864. Figure 35 and Figure 36 show how the NF can vary as a function of the SSI setting for an IF frequency of 109.65 MHz. The following two observations can be made from these figures:

1. The NF becomes more sensitive to the SSI output drive strength level at higher signal bandwidth settings.
2. The NF is dependent on the number of bits within an SSI frame that become more sensitive to the SSI output drive strength level as the number of bits is increased. Therefore, select the lowest possible SSI drive strength setting that still meets the SSI timing requirements.

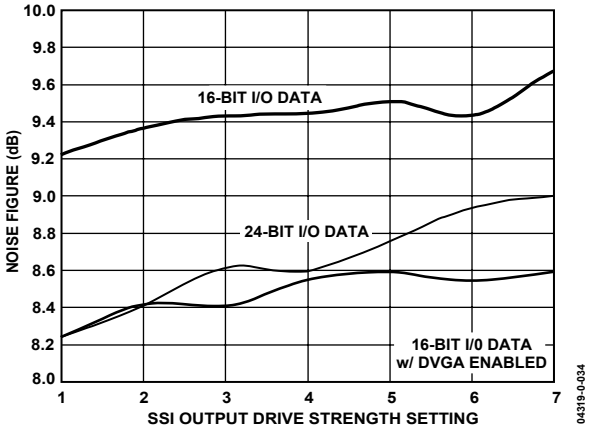

Figure 35. NF vs. SSI Output Drive Strength (VDDx = 3.0 V, f_{CLK} = 18 MSPS, BW = 10 kHz)

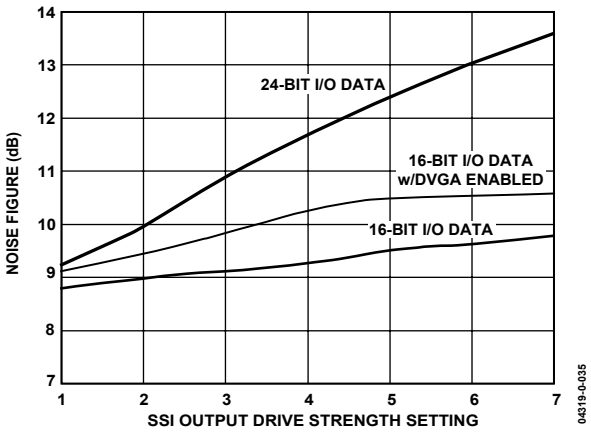

Figure 36. NF vs. SSI Output Drive Strength (VDDx = 3.0 V, f_{CLK} = 18 MSPS, BW = 75 kHz)

Table 15 lists the typical output rise/fall times as a function of DS for a 10 pF load. Rise/fall times for other capacitor loads can be determined by multiplying the typical values presented by a scaling factor equal to the desired capacitive load divided by 10 pF.

Table 15. Typical Rise/Fall Times (±25%) with a 10 pF Capacitive Load for Each DS Setting

DS	Typ (ns)
0	13.5
1	7.2
2	50
3	3.7
4	3.2
5	2.8
6	2.3
7	2.0

SYNCHRONIZATION USING SYNCB

Many applications require the ability to synchronize one or more AD9864 devices in a way that causes the output data to be precisely aligned to an external asynchronous signal. For example, receiver applications employing diversity often require synchronization of the digital outputs of multiple AD9864 devices. Satellite communication applications using TDMA methods may require synchronization between payload bursts to compensate for reference frequency drift and Doppler effects.

SYNCB can be used for this purpose. It is an active-low signal that clears the clock counters in both the decimation filter and the SSI port. The counters in the clock synthesizers are not reset because it is presumed that the CLK signals of multiple chips would be connected. SYNCB also resets the modulator, resulting in a large-scale impulse that must propagate through the digital filter and SSI data formatting circuitry of the AD9864 before recovering valid output data. As a result, data samples unaffected by this SYNCB induced impulse can be recovered 12 output data samples after SYNCB goes high (independent of the decimation factor). Because SYNCB also resets the modulator, apply SYNCB only after the tuning of the band-pass Σ-Δ ADC has been completed during the initialization phase. For applications that may be performing a periodic SYNCB signal that is synchronous to FS, it is recommended that SYNCB assertion be applied after the rising edge of FS and three CLKOUT cycles before the arrival of the next FS pulse to avoid a possible runt FS pulse that could disrupt the host DSP/FPGA. Lastly, SYNCB must be tied high if unused because it does not include an internal pull-up resistor.

Figure 37 shows the timing relationship between SYNCB and the CLKOUT and FS signals of the SSI port. When the clock synthesizer is enabled to generate the input ADC clock, SYNCB is considered an asynchronous active-low signal that must remain low for at least half an input clock period, that is, $1/(2 \times f_{CLK})$. CLKOUT remains high while FS remains low upon SYNCB going low. CLKOUT becomes active within one to two output clock periods upon SYNCB returning high. If an external ADC clock input is supplied along with a synchronous SYNCB signal, it is recommended that SYNCB go low and returns high on the falling edges of the CLKIN signal to ensure consistent CLKOUT delay relative to rising edge of SYNCB. FS reappears several output cycles later, depending on the decimation factor of the digital filter and the SSIORD setting. Note that for any decimation factor and SSIORD setting, this delay is fixed and repeatable. To verify proper synchronization, monitor the FS signals of the multiple AD9864 devices.

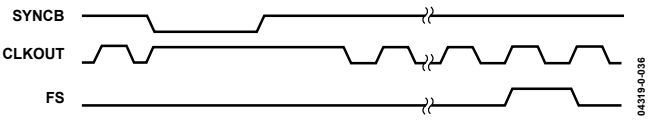

Figure 37. SYNCB Timing

INTERFACING TO DSPS

The AD9864 connects directly to an Analog Devices programmable digital signal processor (DSP). Figure 38 illustrates an example with the Blackfin® series processors, such as the ADSP-BF609. The Blackfin DSP series of 16-bit products is optimized for low power telecommunications applications with its dynamic power management feature, making it well suited for portable radio products. The code compatible family members share the fundamental core attributes of high performance, low power consumption, and the ease-of-use advantages of a microcontroller instruction set.

As shown in Figure 38, the synchronous serial interface (SSI) of the AD9864 links the receive data stream to the serial port (SPORT) of the DSP. For AD9864 setup and register programming, the device connects directly to the SPI port of the DSP. Dedicated select lines (SEL) allow the DSP to program and read back registers of multiple devices using only one SPI port. The DSP driver code pertaining to this interface is available on the AD9864 product page.

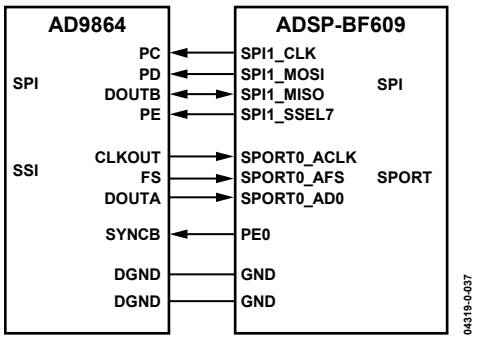

Figure 38. Example of AD9864 and ADSP-BF609 Interface

POWER CONTROL

To allow power consumption to be minimized, the AD9864 possesses numerous SPI programmable power-down and bias control bits. The AD9864 powers up with all of its functional blocks placed into a standby state, that is, STBY register default is 0xFF. Each major block can then be powered up by writing a 0 to the appropriate bit of the STBY register. This scheme provides the greatest flexibility for configuring the IC to a specific application as well as for tailoring the power-down and wake-up characteristics of the IC. Table 16 summarizes the function of each of the STBY bits. Note that when all the blocks are in standby, the master reference circuit is also put into standby, and therefore the current is reduced further by 0.4 mA.