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Broadband Modem Mixed-Signal Front End

Data Sheet **AD9865**

FEATURES

Low cost 3.3 V CMOS MxFE™ for broadband modems
10-bit D/A converter
- **2×/4× interpolation filter**
- **200 MSPS DAC update rate**

Integrated 23 dBm line driver with 19.5 dB gain control
10-bit, 80 MSPS A/D converter
−12 dB to +48 dB low noise RxPGA (< 3.0 nV/rtHz)
Third order, programmable low-pass filter
Flexible digital data path interface
- **Half- and full-duplex operation**
- **Backward-compatible with AD9975 and AD9875**

Various power-down/reduction modes
Internal clock multiplier (PLL)
2 auxiliary programmable clock outputs
Available in 64-lead chip scale package or bare die

APPLICATIONS

Powerline networking
VDSL and HPNA

FUNCTIONAL BLOCK DIAGRAM

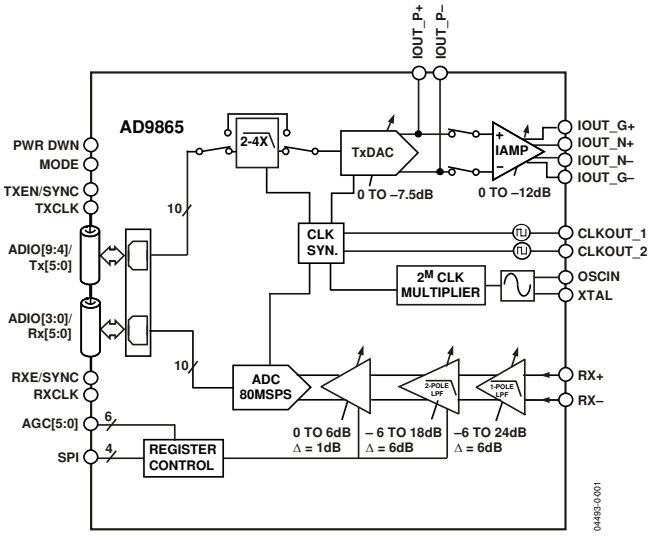

Figure 1.

GENERAL DESCRIPTION

The AD9865 is a mixed-signal front end (MxFE) IC for transceiver applications requiring Tx and Rx path functionality with data rates up to 80 MSPS. Its flexible digital interface, power saving modes, and high Tx-to-Rx isolation make it well suited for half- and full-duplex applications. The digital interface is extremely flexible allowing simple interfaces to digital back ends that support half- or full-duplex data transfers, thus often allowing the AD9865 to replace discrete ADC and DAC solutions. Power saving modes include the ability to reduce power consumption of individual functional blocks, or to power down unused blocks in half-duplex applications. A serial port interface (SPI®) allows software programming of the various functional blocks. An on-chip PLL clock multiplier and synthesizer provide all the required internal clocks, as well as two external clocks from a single crystal or clock source.

The Tx signal path consists of a bypassable 2×/4× low-pass interpolation filter, a 10-bit TxDAC, and a line driver. The transmit path signal bandwidth can be as high as 34 MHz at an input data rate of 80 MSPS. The TxDAC provides differential current outputs that can be steered directly to an external load or to an internal low distortion current amplifier. The current amplifier (IAMP) can be configured as a current- or voltage-mode line driver (with two external npn transistors) capable of delivering in excess of 23 dBm peak signal power. Tx power can be digitally controlled over a 19.5 dB range in 0.5 dB steps.

The receive path consists of a programmable amplifier (RxPGA), a tunable low-pass filter (LPF), and a 10-bit ADC. The low noise RxPGA has a programmable gain range of −12 dB to +48 dB in 1 dB steps. Its input referred noise is less than 3 nV/rtHz for gain settings beyond 36 dB. The receive path LPF cutoff frequency can be set over a 15 MHz to 35 MHz range or simply bypassed. The 10-bit ADC achieves excellent dynamic performance over a 5 MSPS to 80 MSPS span. Both the RxPGA and the ADC offer scalable power consumption allowing power/performance optimization.

The AD9865 provides a highly integrated solution for many broadband modems. It is available in a space saving 64-pin chip scale package and is specified over the commercial (−40°C to +85°C) temperature range.

Rev. B Document Feedback

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COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-700: Instructions for the AD9865/AD9866 Evaluation Software
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design

Data Sheet

- AD9865: Broadband Modem Mixed-Signal Front End Data Sheet

REFERENCE MATERIALS

Informational

- Advantiv™ Advanced TV Solutions

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD9865 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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9/2016—Rev. A to Rev. B

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11/2003—Revision 0: Initial Version

SPECIFICATIONS

Tx PATH SPECIFICATIONS

AVDD = 3.3 V ± 5%, DVDD = CLKVDD = DRVDD = 3.3 V ± 10%; f_{OSCIN} = 50 MHz, f_{DAC} = 200 MHz, R_{SET} = 2.0 kΩ, unless otherwise noted.

Table 1.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
TxDAC DC CHARACTERISTICS						
Resolution	Full			10		Bits
Update Rate	Full	II			200	MSPS
Full-Scale Output Current (IOUTP_FS)	Full	IV	2		25	mA
Gain Error[1]	25°C	I		±2		% FS
Offset Error	25°C	V		2		µA
Voltage Compliance Range	Full		−1		+1.5	V
TxDAC GAIN CONTROL CHARACTERISTICS						
Minimum Gain	25°C	V		−7.5		dB
Maximum Gain	25°C	V		0		dB
Gain Step Size	25°C	V		0.5		dB
Gain Step Accuracy	25°C	IV		Monotonic		
Gain Range Error	25°C	V		±2		dB
TxDAC AC CHARACTERISTICS[2]						
Fundamental				0.5		dBm
Signal-to-Noise and Distortion (SINAD)	Full	IV	62.0	63.1		dBc
Signal-to-Noise Ratio (SNR)	Full	IV	62.5	63.2		dBc
Total Harmonic Distortion (THD)	Full	IV		−77.7	−67.0	dBc
Spurious-Free Dynamic Range (SFDR)	Full	IV	67.1	79.3		dBc
IAMP DC CHARACTERISTICS						
IOUTN Full-Scale Current = IOUTN+ + IOUTN−	Full	IV	2		105	mA
IOUTG Full-Scale Current = IOUTG+ + IOUTG−	Full	IV	2		150	mA
AC Voltage Compliance Range	Full	IV	1		7	V
IAMPN AC CHARACTERISTICS[3]						
Fundamental	25°C			13		dBm
IOUTN SFDR (Third Harmonic)	Full	IV	43.3	45.2		dBc
IAMP GAIN CONTROL CHARACTERISTICS						
Minimum Gain	25°C	V		−19.5		dB
Maximum Gain	25°C	V		0		dB
Gain Step Size	25°C	V		0.5		dB
Gain Step Accuracy	25°C	IV		Monotonic		dB
IOUTN Gain Range Error	25°C	V		0.5		dB
REFERENCE						
Internal Reference Voltage[4]	25°C	I		1.23		V
Reference Error	Full	V		0.7	3.4	%
Reference Drift	Full	V		30		ppm/°C
Tx DIGITAL FILTER CHARACTERISTICS (2× Interpolation)						
Latency (Relative to $1/f_{DAC}$)	Full	V		43		Cycles
−0.2 dB Bandwidth	Full	V		0.2187		f_{OUT}/f_{DAC}
−3 dB Bandwidth	Full	V		0.2405		f_{OUT}/f_{DAC}
Stop-Band Rejection (0.289 f_{DAC} to 0.711 f_{DAC})	Full	V		50		dB

Parameter	Temp	Test Level	Min	Typ	Max	Unit
Tx DIGITAL FILTER CHARACTERISTICS (4× Interpolation)						
Latency (Relative to 1/ F_{DAC})	Full	V		96		Cycles
−0.2 dB Bandwidth	Full	V		0.1095		f_{OUT}/f_{DAC}
−3 dB Bandwidth	Full	V		0.1202		f_{OUT}/f_{DAC}
Stop Band Rejection (0.289 f_{OSCIN} to 0.711 f_{OSCIN})	Full	V		50		dB
PLL CLK MULTIPLIER						
OSCIN Frequency Range	Full	IV	5		80	MHz
Internal VCO Frequency Range	Full	IV	20		200	MHz
Duty Cycle	Full	II	40		60	%
OSCIN Impedance	25°C	V		100//3		MΩ/pF
CLKOUT1 Jitter[5]	25°C	III		12		ps rms
CLKOUT2 Jitter[6]	25°C	III		6		ps rms
CLKOUT1 and CLKOUT2 Duty Cycle[7]	Full	III	45		55	%

[1] Gain error and gain temperature coefficients are based on the ADC only (with a fixed 1.23 V external reference and a 1 V p-p differential analog input).
[2] TxDAC IOUTFS = 20 mA, differential output with 1:1 transformer with source and load termination of 50 Ω, F_{OUT} = 5 MHz, 4x interpolation.
[3] IOUN full-scale current = 80 mA, f_{OSCIN} = 80 MHz, f_{DAC} =160 MHz, 2x interpolation.
[4] Use external amplifier to drive additional load.
[5] Internal VCO operates at 200 MHz , set to divide-by-1.
[6] Because CLKOUT2 is a divided down version of OSCIN, its jitter is typically equal to OSCIN.
[7] CLKOUT2 is an inverted replica of OSCIN, if set to divide-by-1.

Rx PATH SPECIFICATIONS

AVDD = 3.3 V ± 5%, DVDD = CLKVDD = DRVDD = 3.3 V ± 10%; half- or full-duplex operation with CONFIG = 0 default power bias settings, unless otherwise noted.

Table 2.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
Rx INPUT CHARACTERISTICS						
Input Voltage Span (RxPGA Gain = −10 dB)	Full	III		6.33		V p-p
Input Voltage Span (RxPGA Gain = +48 dB)	Full	III		8		mV p-p
Input Common-Mode Voltage	25°C	III		1.3		V
Differential Input Impedance	25°C	III		400 4.0		Ω pF
Input Bandwidth (with RxLPF Disabled, RxPGA = 0 dB)	25°C	III		53		MHz
Input Voltage Noise Density (RxPGA Gain = 36 dB, $f_{-3\ dBF}$ = 26 MHz)	25°C	III		3.0		nV/rtHz
Input Voltage Noise Density (RxPGA Gain = 48 dB, $f_{-3\ dBF}$ = 26 MHz)	25°C	III		2.4		nV/rtHz
RxPGA CHARACTERISTICS						
Minimum Gain	25°C	III		−12		dB
Maximum Gain	25°C	III		48		dB
Gain Step Size	25°C	III		1		dB
Gain Step Accuracy	25°C	III		Monotonic		dB
Gain Range Error	25°C	III		0.5		dB
RxLPF CHARACTERISTICS						
Cutoff Frequency ($f_{-3\ dBF}$) Range	Full	III	15		35	MHz
Attenuation at 55.2 MHz with $f_{-3\ dBF}$ = 21 MHz	25°C	III		20		dB
Pass-Band Ripple	25°C	III		±1		dB
Settling Time to 5 dB RxPGA Gain Step @ f_{ADC} = 50 MSPS	25°C	III		20		ns
Settling Time to 60 dB RxPGA Gain Step @ f_{ADC} = 50 MSPS	25°C	III		100		ns
ADC DC CHARACTERISTICS						
Resolution	NA	NA		10		Bits
Conversion Rate	Full	II	5		80	MSPS

Parameter	Temp	Test Level	Min	Typ	Max	Unit
Rx PATH LATENCY[1]						
Full-Duplex Interface	Full	V		10.5		Cycles
Half-Duplex Interface	Full	V		10.0		Cycles
Rx PATH COMPOSITE AC PERFORMANCE @ f_{ADC} = 50 MSPS[2]						
RxPGA Gain = 48 dB (Full-Scale = 8.0 mV p-p)						
Signal-to-Noise and Distortion (SNR)	25°C	III		43.7		dBc
Total Harmonic Distortion (THD)	25°C	III		−71		dBc
RxPGA Gain = 24 dB (Full-Scale =126 mV p-p)						
Signal-to-Noise (SNR)	25°C	III		59		dBc
Total Harmonic Distortion (THD)	25°C	III		−67.2		dBc
RxPGA Gain = 0 dB (Full-Scale = 2.0 V p-p)						
Signal-to-Noise and Distortion (SINAD)	Full	IV	58	59		dBc
Total Harmonic Distortion (THD)	Full	IV		−66	−62.9	dBc
Rx PATH COMPOSITE AC PERFORMANCE @ f_{ADC} = 80 MSPS[3]						
RxPGA Gain = 48 dB (Full-Scale = 8.0 mV p-p)						
Signal-to-Noise (SNR)	25°C	III		41.8		dBc
Total Harmonic Distortion (THD)	25°C	III		−67		dBc
RxPGA Gain = 24 dB (Full-Scale = 126 mV p-p)						
Signal-to-Noise (SNR)	25°C	III		58.6		dBc
Total Harmonic Distortion (THD)	25°C	III		−62.9		dBc
RxPGA Gain = 0 dB (Full-Scale = 2.0 V p-p)						
Signal-to-Noise (SNR)	25°C	II	58.9	59.6		dBc
Total Harmonic Distortion (THD)	25°C	II		−69.7	−59.8	dBc
Rx-to-Tx PATH FULL-DUPLEX ISOLATION (1 V p-p, 10 MHz Sine Wave Tx Output)						
RxPGA Gain = 40 dB						
IOUTP± Pins to RX± Pins	25°C	III		83		dBc
IOUTG± Pins to RX± Pins	25°C	III		37		dBc
RxPGA Gain = 0 dB						
IOUTP± Pins to RX± Pins	25°C	III		123		dBc
IOUTG± Pins to RX± Pins	25°C	III		77		dBc

[1] Includes RxPGA, ADC pipeline, and ADIO bus delay relative to f_{ADC}.
[2] f_{IN} = 5 MHz, AIN = −1.0 dBFS , LPF cutoff frequency set to 15.5 MHz with Reg. 0x08 = 0x80.
[3] f_{IN} = 5 MHz, AIN = −1.0 dBFS , LPF cutoff frequency set to 26 MHz with Reg. 0x08 = 0x80.

POWER SUPPLY SPECIFICATIONS

AVDD = 3.3 V, DVDD = CLKVDD = DRVDD = 3.3 V; R_{SET} = 2 kΩ, full-duplex operation with f_{DATA} = 80 MSPS,[1] unless otherwise noted.

Table 3.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
SUPPLY VOLTAGES						
AVDD	Full	V	3.135	3.3	3.465	V
CLKVDD	Full	V	3.0	3.3	3.6	V
DVDD	Full	V	3.0	3.3	3.6	V
DRVDD	Full	V	3.0	3.3	3.6	V
IS_TOTAL (Total Supply Current)	Full	II		406	475	mA
POWER CONSUMPTION						
I_{AVDD} + I_{CLKVDD} (Analog Supply Current)		IV		311	342	mA
I_{DVDD} + I_{DRVDD} (Digital Supply Current)	Full	IV		95	133	mA

Parameter	Temp	Test Level	Min	Typ	Max	Unit
POWER CONSUMPTION (Half-Duplex Operation with f_{DATA} = 50 MSPS)[2]						
Tx Mode						
I_{AVDD} + I_{CLKVDD}	25°C	IV		112	130	mA
I_{DVDD} + I_{DRVDD}	25°C	IV		46	49.5	mA
Rx Mode						
I_{AVDD} + I_{CLKVDD}	25°C	IV		225	253	mA
I_{DVDD} + I_{DRVDD}	25°C	IV		36.5	39	mA
POWER CONSUMPTION OF FUNCTIONAL BLOCKS[1] (I_{AVDD} + I_{CLKVDD})						
RxPGA and LPF	25°C	III		87		mA
ADC	25°C	III		108		mA
TxDAC	25°C	III		38		mA
IAMP (Programmable)	25°C	III	10		120	mA
Reference	25°C	III		170		mA
CLK PLL and Synthesizer	25°C	III		107		mA
MAXIMUM ALLOWABLE POWER DISSIPATION	Full	IV			1.66	W
STANDBY POWER CONSUMPTION						
IS_TOTAL (Total Supply Current)	Full			13		mA
POWER DOWN DELAY (USING PWR_DWN PIN)						
RxPGA and LPF	25°C	III		440		ns
ADC	25°C	III		12		ns
TxDAC	25°C	III		20		ns
IAMP	25°C	III		20		ns
CLK PLL and synthesizer	25°C	III		27		ns
POWER UP DELAY (USING PWR_DWN PIN)						
RxPGA and LPF	25°C	III		7.8		µs
ADC	25°C	III		88		ns
TxDAC	25°C	III		13		µs
IAMP	25°C	III		20		ns
CLK PLL and Synthesizer	25°C	III		20		µs

[1] Default power-up settings for MODE = HIGH and CONFIG = LOW, IOUTP_FS = 20 mA, does not include IAMP's current consumption, which is application dependent.
[2] Default power-up settings for MODE = LOW and CONFIG = LOW.

DIGITAL SPECIFICATIONS

AVDD = 3.3 V ± 5%, DVDD = CLKVDD = DRVDD = 3.3 V ± 10%; R_{SET} = 2 kΩ, unless otherwise noted.

Table 4.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
CMOS LOGIC INPUTS						
High Level Input Voltage	Full	VI	DRVDD – 0.7			V
Low Level Input Voltage	Full	VI			0.4	V
Input Leakage Current					12	µA
Input Capacitance	Full	VI		3		pF
CMOS LOGIC OUTPUTS (C_{LOAD} = 5 pF)						
High Level Output Voltage (I_{OH} = 1 mA)	Full	VI	DRVDD – 0.7			V
Low Level Output Voltage (I_{OH} = 1 mA)	Full	VI			0.4	V
Output Rise/Fall Time (High Strength Mode and C_{LOAD} = 15 pF)	Full	VI		1.5/2.3		ns
Output Rise/Fall Time (Low Strength Mode and C_{LOAD} = 15 pF)	Full	VI		1.9/2.7		ns
Output Rise/Fall Time (High Strength Mode and C_{LOAD} = 5 pF)	Full	VI		0.7/0.7		ns
Output Rise/Fall Time (Low Strength Mode and C_{LOAD} = 5 pF)	Full	VI		1.0/1.0		ns
RESET						
Minimum Low Pulse Width (Relative to f_{ADC})			1			Clock cycles

SERIAL PORT TIMING SPECIFICATIONS

AVDD = 3.3 V ± 5%, DVDD = CLKVDD = DRVDD = 3.3 V ± 10%, unless otherwise noted.

Table 5.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
WRITE OPERATION (See Figure 46)						
SCLK Clock Rate (f_{SCLK})	Full	IV			32	MHz
SCLK Clock High (t_{HI})	Full	IV	14			ns
SCLK Clock Low (t_{LOW})	Full	IV	14			ns
SDIO to SCLK Setup Time (t_{DS})	Full	IV	14			ns
SCLK to SDIO Hold Time (t_{DH})	Full	IV	0			ns
$\overline{SEN}$ to SCLK Setup Time (t_S)	Full	IV	14			ns
SCLK to $\overline{SEN}$ Hold Time (t_H)	Full	IV	0			ns
READ OPERATION (See Figure 47 and Figure 48)						
SCLK Clock Rate (f_{SCLK})	Full	IV			32	MHz
SCLK Clock High (t_{HI})	Full	IV	14			ns
SCLK Clock Low (t_{LOW})	Full	IV	14			ns
SDIO to SCLK Setup Time (t_{DS})	Full	IV	14			ns
SCLK to SDIO Hold Time (t_{DH})	Full	IV	0			ns
SCLK to SDIO (or SDO) Data Valid Time (t_{DV})	Full	IV			14	ns
$\overline{SEN}$ to SDIO Output Valid to Hi-Z (t_{EZ})	Full	IV		2		ns

HALF-DUPLEX DATA INTERFACE (ADIO PORT) TIMING SPECIFICATIONS

AVDD = 3.3 V ± 5%, DVDD = CLKVDD = DRVDD = 3.3 V ± 10%, unless otherwise noted.

Table 6.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
READ OPERATION[1] (See Figure 50)						
Output Data Rate	Full	II	5		80	MSPS
Three-State Output Enable Time (t_{PZL})	Full	II			3	ns
Three-State Output Disable Time (t_{PLZ})	Full	II			3	ns
Rx Data Valid Time (t_{VT})	Full	II	1.5			ns
Rx Data Output Delay (t_{OD})	Full	II			4	ns
WRITE OPERATION (See Figure 49)						
Input Data Rate (1× Interpolation)	Full	II	20		80	MSPS
Input Data Rate (2× Interpolation)	Full	II	10		80	MSPS
Input Data Rate (4× Interpolation)	Full	II	5		50	MSPS
Tx Data Setup Time (t_{DS})	Full	II	1			ns
Tx Data Hold Time (t_{DH})	Full	II	2.5			ns
Latch Enable Time (t_{EN})	Full	II			3	ns
Latch Disable Time (t_{DIS})	Full	II			3	ns

[1] C_{LOAD} = 5 pF for digital data outputs.

FULL-DUPLEX DATA INTERFACE (Tx AND Rx PORT) TIMING SPECIFICATIONS

AVDD = 3.3 V ± 5%, DVDD = CLKVDD = DRVDD = 3.3 V ± 10%, unless otherwise noted.

Table 7.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
Tx PATH INTERFACE (See Figure 53)						
Input Nibble Rate (2× Interpolation)	Full	II	20		160	MSPS
Input Nibble Rate (4× Interpolation)	Full	II	10		100	MSPS
Tx Data Setup Time (t_{DS})	Full	II	2.5			ns
Tx Data Hold Time (t_{DH})	Full	II	1.5			ns
Rx PATH INTERFACE[1] (See Figure 54)						
Output Nibble Rate	Full	II	10		160	MSPS
Rx Data Valid Time (t_{DV})	Full	II	3			ns
Rx Data Hold Time (t_{DH})	Full	II	0			ns

[1] C_{LOAD} =5 pF for digital data outputs.

EXPLANATION OF TEST LEVELS

I 100% production tested.
II 100% production tested at 25°C and guaranteed by design and characterization at specified temperatures.
III Sample tested only.
IV Parameter is guaranteed by design and characterization testing.
V Parameter is a typical value only.
VI 100% production tested at 25°C and guaranteed by design and characterization for industrial temperature range.

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
ELECTRICAL	
AVDD, CLKVDD Voltage	3.9 V maximum
DVDD, DRVDD Voltage	3.9 V maximum
RX+, RX−, REFT, REFB	−0.3 V to AVDD + 0.3 V
IOUTP+, IOUTP−	−1.5 V to AVDD + 0.3 V
IOUTN+, IOUTN−, IOUTG+, IOUTG−	−0.3 V to +7 V
OSCIN, XTAL	−0.3 V to CLVDD + 0.3 V
REFIO, REFADJ	−0.3 V to AVDD + 0.3 V
Digital Input and Output Voltage	−0.3 V to DRVDD + 0.3 V
Digital Output Current	5 mA maximum
ENVIRONMENTAL	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature	125°C
Lead Temperature (Soldering, 10 s)	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

The exposed pad (EPAD) must be soldered to the ground plane for the 64-lead LFCSP. The EPAD provides an electrical, thermal, and mechanical connection to the board.

Junction temperature (T_J) can be estimated using the following equations:

$$T_J = T_T + (\Psi_{JT} \times P),$$

or

$$T_J = T_B + (\Psi_{JB} \times P)$$

where:
T_T is the temperature measured at the top of the package.
P is the total device power dissipation.
T_B is the temperature measured at the board.
Ψ_{JT} and Ψ_{JB} are thermal characteristic parameters obtained with θ_{JA} in still air test conditions.

Table 9. Thermal Resistance

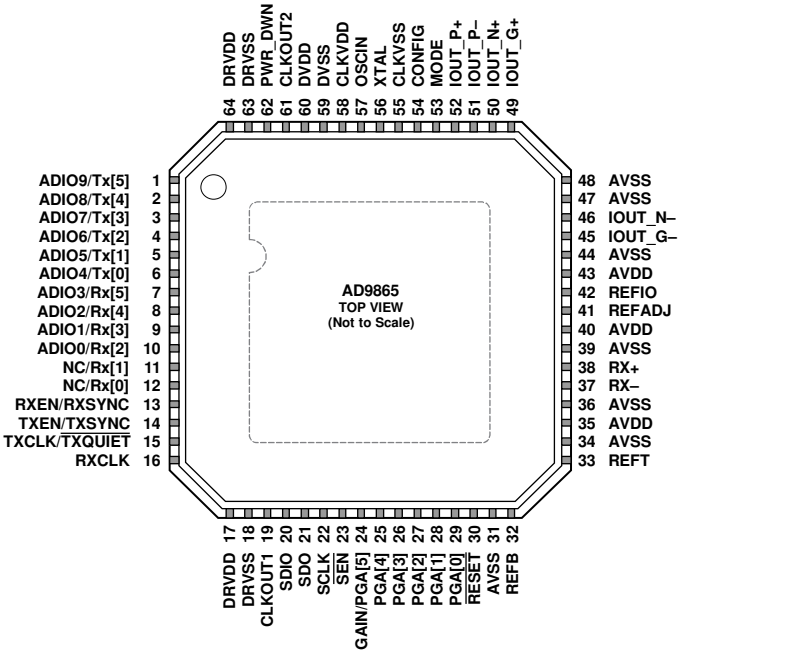
Package	θ_{JA}	θ_{JC}	Unit
CP-64-3[1]	23.32	0.7	°C/W

[1] Test condition 1: typical θ_{JA} and θ_{JC} values are specified for a 4-layer, JESD51-7 high effective thermal conductivity test board for leaded surface-mount packages. θ_{JA} is obtained in still air conditions (JESD51-2). Airflow increases heat dissipation, effectively reducing θ_{JA}. θ_{JC} is obtained with the test case temperature monitored at the bottom of the exposed pad.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD (EPAD) MUST BE SOLDERED TO THE GROUND PLANE FOR THE 64-LEAD LFCSP. THE EPAD PROVIDES AN ELECTRICAL, THERMAL, AND MECHANICAL CONNECTION TO THE BOARD.

4493-0-002

Figure 2. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Mode[1]	Description
1	ADIO9	HD	MSB of ADIO Buffer
	Tx[5]	FD	MSB of Tx Nibble Input
2 to 5	ADIO8 to 5	HD	Bits 8 to 5 of ADIO Buffer
	Tx[4 to 1]	FD	Bits 4 to 1 of Tx Nibble Input
6	ADIO4	HD	Bit 4 of ADIO Buffer
	Tx[0]	FD	LSB of Tx Nibble Input
7	ADIO3	HD	Bit 3 of ADIO Buffer
	Rx[5]	FD	MSB of Rx Nibble Output
8, 9	ADIO2, 1	HD	Bits 2 to 1 of ADIO Buffer
	Rx[4, 3]	FD	Bits 4 to 3 of Rx Nibble Output
10	ADIO0	HD	LSB of ADIO Buffer
	Rx[2]	FD	Bit 2 of Rx Nibble Output
11	NC	HD	No Connect
	Rx[1]	FD	Bit 1 of Rx Nibble Output
12	NC	HD	No Connect
	Rx[0]	FD	LSB of Rx Nibble Output
13	RXEN	HD	ADIO Buffer Control Input
	RXSYNC	FD	Rx Data Synchronization Output
14	TXEN	HD	Tx Path Enable Input
	TXSYNC	FD	Tx Data Synchronization Input

Pin No.	Mnemonic	Mode[1]	Description
15	TXCLK $\overline{\text{TXQUIET}}$	HD FD	ADIO Sample Clock Input Fast TxDAC/IAMP Power-Down
16	RXCLK	HD FD	ADIO Request Clock Input Rx and Tx Clock Output at 2 x f_{ADC}
17, 64	DRVDD		Digital Output Driver Supply Input
18, 63	DRVSS		Digital Output Driver Supply Return
19	CLKOUT1		f_{ADC}/N Clock Output (L = 1, 2, 4, or 8)
20	SDIO		Serial Port Data Input/Output
21	SDO		Serial Port Data Output
22	SCLK		Serial Port Clock Input
23	$\overline{\text{SEN}}$		Serial Port Enable Input
24	GAIN PGA[5]	FD HD or FD	Tx Data Port (Tx[5:0]) Mode Select MSB of PGA Input Data Port
25 to 29	PGA[4 to 0]	HD or FD	Bits 4 to 0 of PGA Input Data Port
30	$\overline{\text{RESET}}$		Reset Input (Active Low)
31, 34, 36, 39, 44, 47, 48	AVSS		Analog Ground
32, 33	REFB, REFT		ADC Reference Decoupling Nodes
35, 40, 43	AVDD		Analog Power Supply Input
37, 38	RX−, RX+		Receive Path − and + Analog Inputs
41	REFADJ		TxDAC Full-Scale Current Adjust
42	REFIO		TxDAC Reference Input/Output
45	IOUT_G−		−Tx Amp Current Output_Sink
46	IOUT_N−		−Tx Mirror Current Output_Sink
49	IOUT_G+		+Tx Amp Current Output_Sink
50	IOUT_N+		+Tx Mirror Current Output_Sink
51	IOUT_P−		−TxDAC Current Output_Source
52	IOUT_P+		+TxDAC Current Output_Source
53	MODE		Digital Interface Mode Select Input LOW = HD, HIGH = FD
54	CONFIG		Power-Up SPI Register Default Setting Input
55	CLKVSS		Clock Oscillator/Synthesizer Supply Return
56	XTAL		Crystal Oscillator Inverter Output
57	OSCIN		Crystal Oscillator Inverter Input
58	CLKVDD		Clock Oscillator/Synthesizer Supply
59	DVSS		Digital Supply Return
60	DVDD		Digital Supply Input
61	CLKOUT2		f_{OSCIN}/L Clock Output, (L = 1, 2, or 4)
62	PWR_DWN		Power-Down Input
	EPAD		Exposed Pad. The exposed pad (EPAD) must be soldered to the ground plane for the 64-lead LFCSP. The EPAD provides an electrical, thermal, and mechanical connection to the board.

[1] HD = half-duplex mode; FD = full-duplex mode.

TYPICAL PERFORMANCE CHARACTERISTICS

Rx PATH TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = CLKVDD = DVDD = DRVDD = 3.3 V, $f_{OSCIN} = f_{ADC}$ = 50 MSPS, low-pass filter's $f_{-3\,dB}$ = 22 MHz, AIN = −1 dBFS, RIN = 50 Ω, half- or full-duplex interface, default power bias settings.

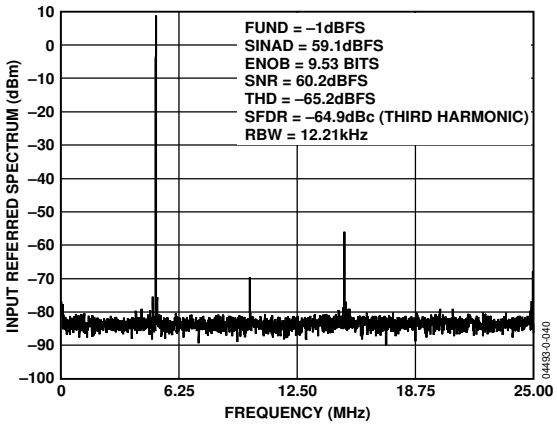


Figure 3. Spectral Plot with 4 k FFT of Input Sinusoid with RxPGA = 0 dB and P_{IN} = 9 dBm

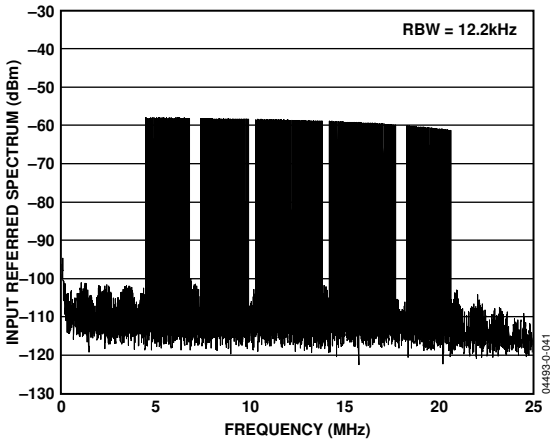


Figure 4. Spectral Plot with 4 k FFT of 84-Carrier DMT Signal with PAR = 10.2 dB, P_{IN} = −33.7 dBm, and RxPGA = 36 dB

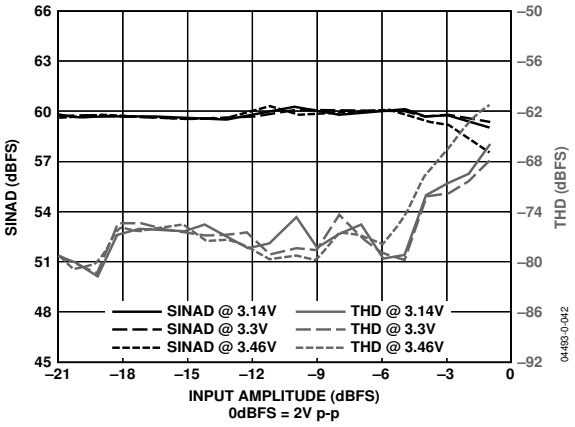


Figure 5. SINAD and THD vs. Input Amplitude and Supply (f_{IN} = 8 MHz, LPF $f_{-3\,dB}$ = 26 MHz; Rx PGA = 0 dB)

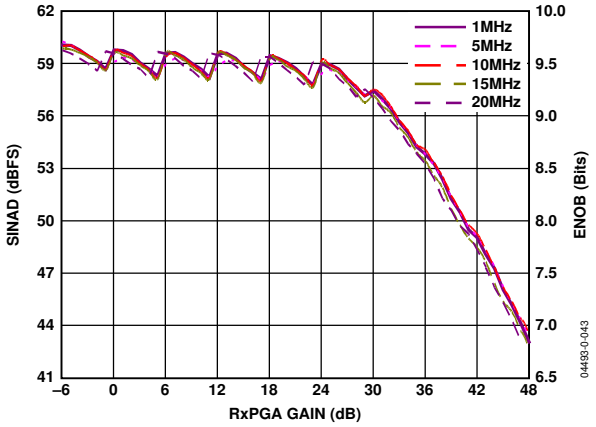


Figure 6. SINAD/ENOB vs. RxPGA Gain and Frequency

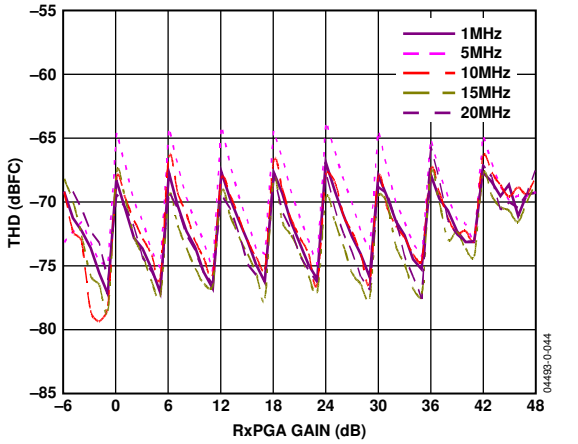


Figure 7. THD vs. RxPGA Gain and Frequency

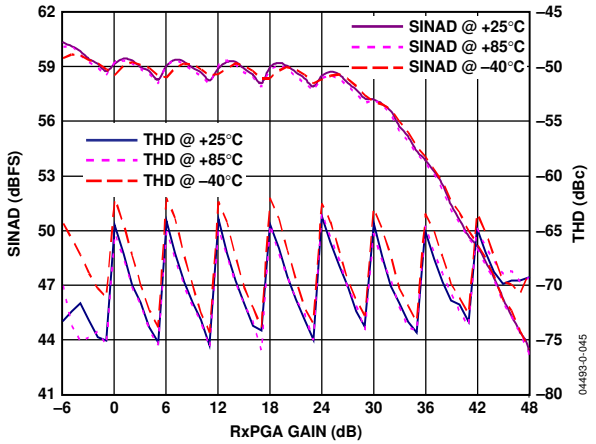


Figure 8. SINAD/THD Performance vs. RxPGA Gain and Temperature (f_{IN} = 5 MHz)

Rx PATH TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = CLKVDD = DVDD = DRVDD = 3.3 V, $f_{OSCIN} = f_{ADC}$ = 80 MSPS, low-pass filter's $f_{-3\,dB}$ = 30 MHz, AIN = −1 dBFS, RIN = 50 Ω, half- or full-duplex interface, default power bias settings.

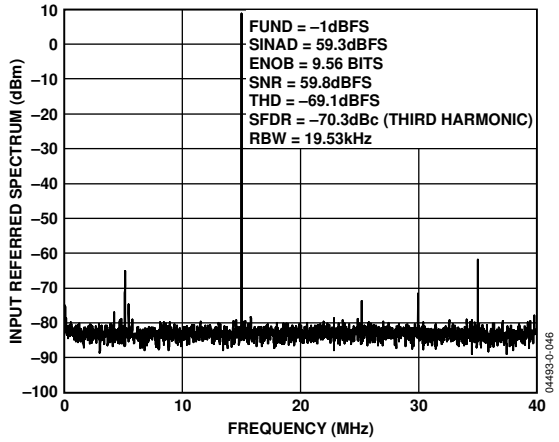


Figure 9. Spectral Plot with 4k FFT of Input Sinusoid with RxPGA = 0 dB and P_{IN} = 9 dBm

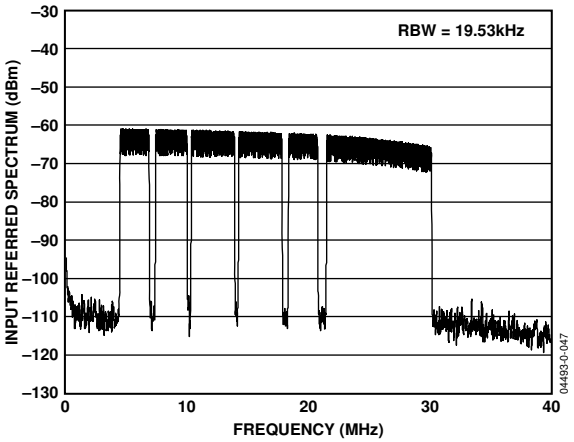


Figure 10. Spectral Plot with 4k FFT of 111-Carrier DMT Signal with PAR = 11 dB, P_{IN} = −33.7 dBm, LPF $f_{-3\,dB}$ = 32 MHz, and RxPGA = 36 dB

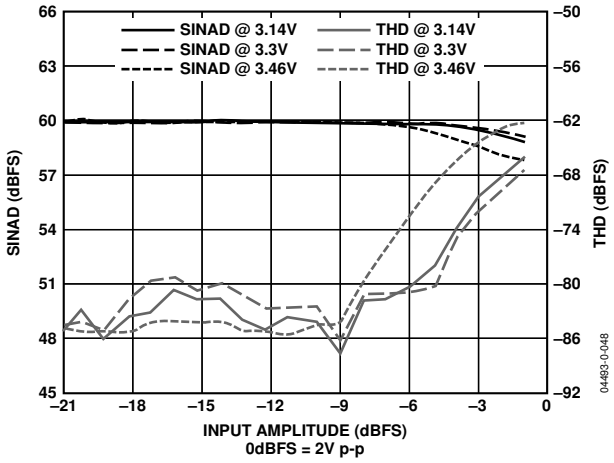


Figure 11. SINAD and THD vs. Input Amplitude and Supply (f_{IN} = 8 MHz, LPF $f_{-3\,dB}$ = 26 MHz; RxPGA = 0 dB)

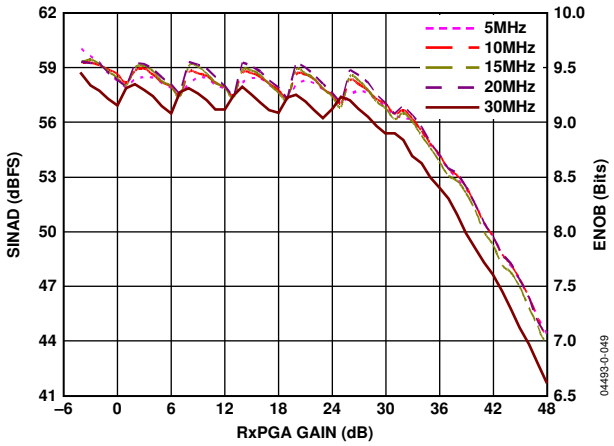


Figure 12. SINAD/ENOB vs. RxPGA Gain and Frequency

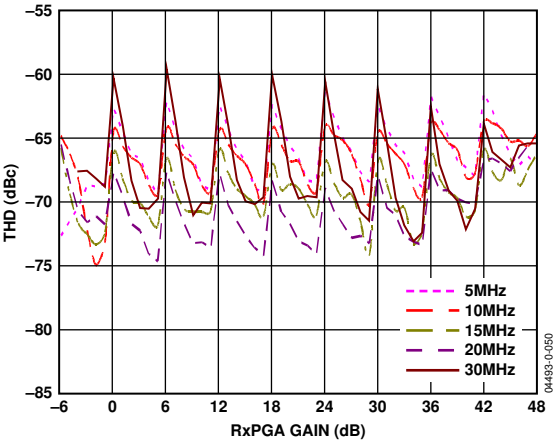


Figure 13. THD vs. RxPGA Gain and Frequency

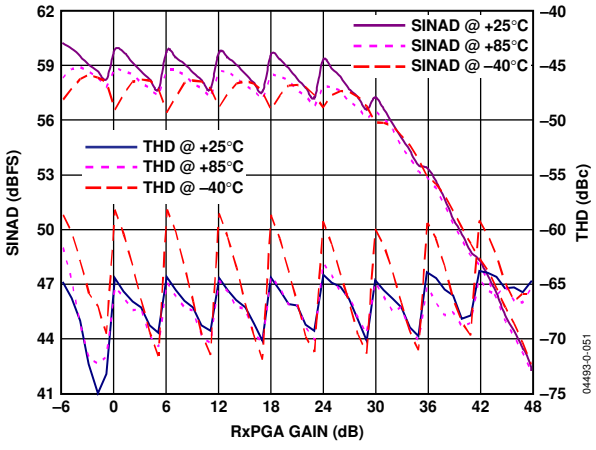


Figure 14. SINAD/THD Performance vs. RxPGA Gain and Temperature (f_{IN} = 10 MHz)

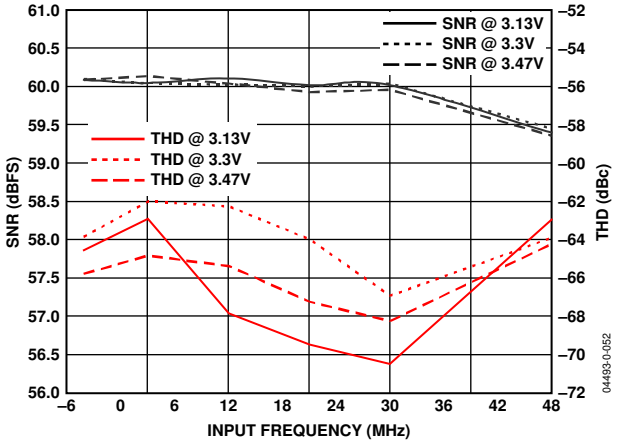


Figure 15. SNR and THD vs. Input Frequency and Supply (LPF $f_{-3\,dB}$ = 26 MHz; RxPGA = 0 dB)

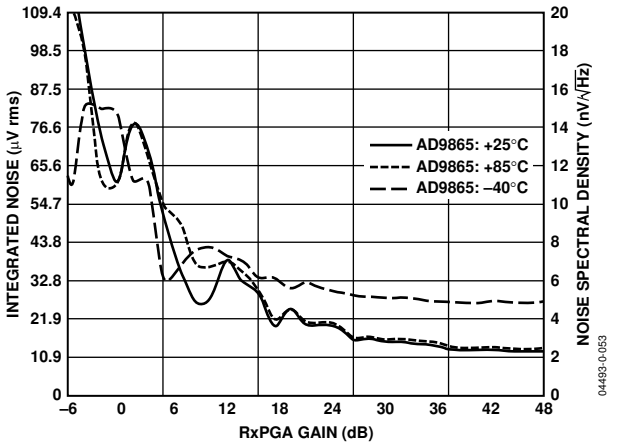


Figure 16. Input Referred Integrated Noise and Noise Spectral Density vs. RxPGA Gain (LPF $f_{-3\,dB}$ = 26 MHz)

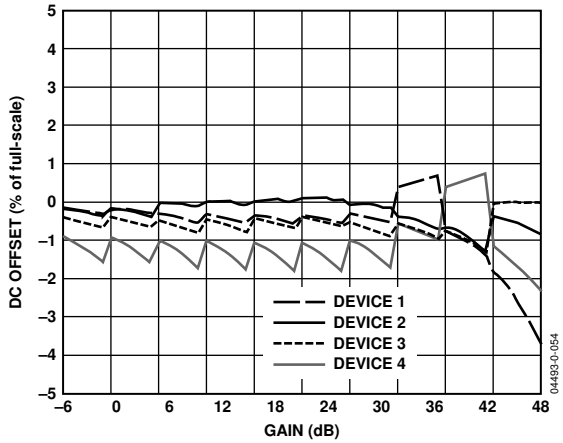


Figure 17. Rx DC Offset vs. RxPGA Gain

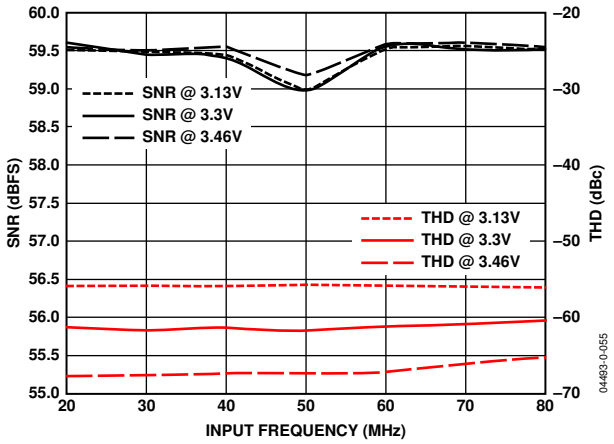


Figure 18. SNR and THD vs. Sample Rate and Supply (LPF Disabled; RxPGA = 0 dB; f_{IN} = 8 MHz)

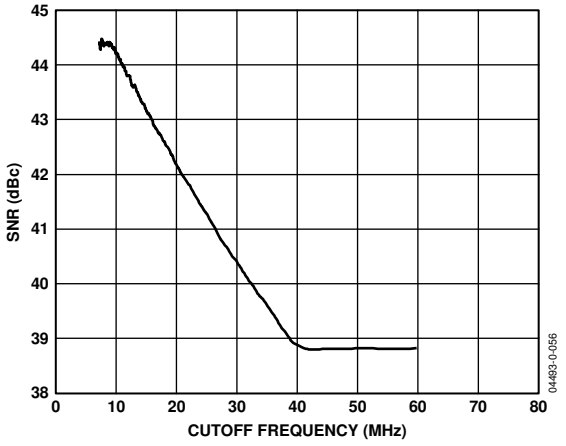


Figure 19. SNR vs. Filter Cutoff Frequency (50 MSPS; f_{IN} = 5 MHz; AIN = −1 dB; RxPGA = 48 dB)

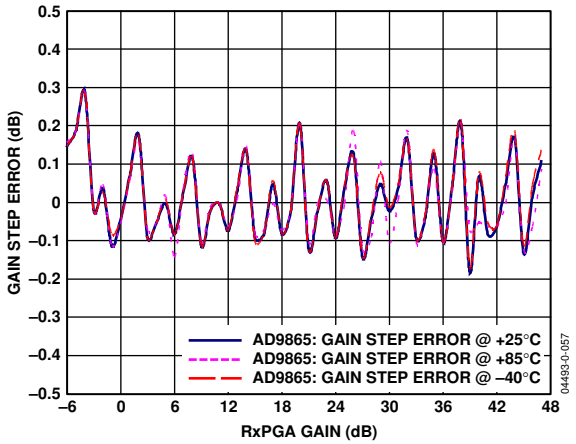


Figure 20. RxPGA Gain Step Error vs. Gain (f_{IN} = 10 MHz)

Rx PATH TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = CLKVDD = DVDD = DRVDD = 3.3 V, $f_{OSCIN} = f_{ADC}$ = 50 MSPS, low-pass filter disabled, RxPGA = 0 dB, AIN = −1 dBFS, RIN = 50 Ω, half- or full-duplex interface, default power bias settings.

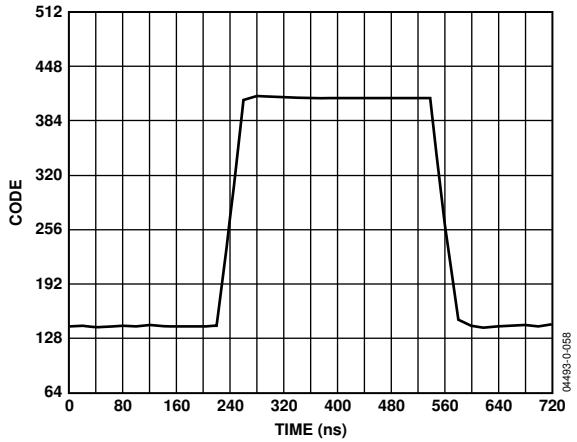


Figure 21. RxPGA Settling Time −12 dB to +48 dB Transition for DC Input (f_{ADC} = 50 MSPS, LPF Disabled)

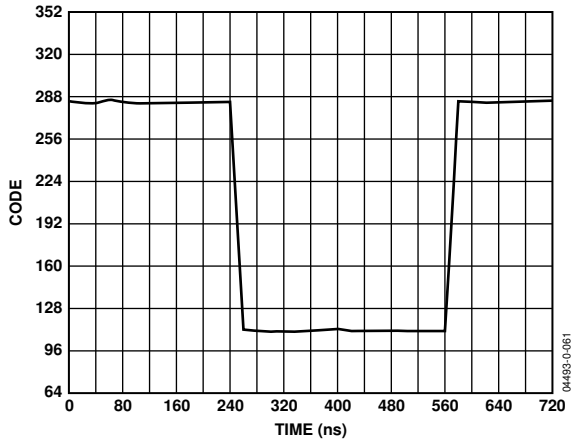


Figure 24. RxPGA Settling Time for 0 dB to +5 dB Transition for DC Input (f_{ADC} = 50 MSPS, LPF Disabled)

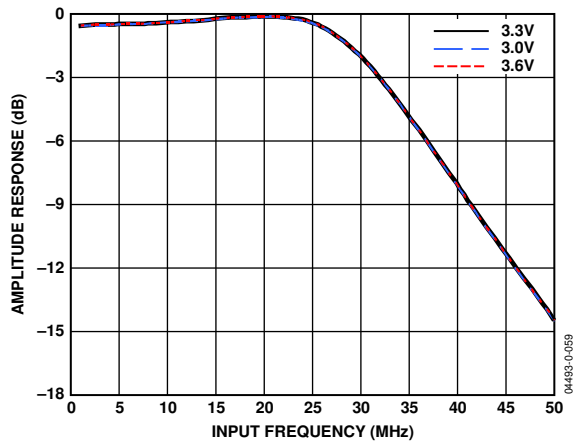


Figure 22. Rx Low-Pass Filter Amplitude Response vs. Supply (f_{ADC} = 50 MSPS, $f_{-3\,dB}$ = 33 MHz, RxPGA = 0 dB)

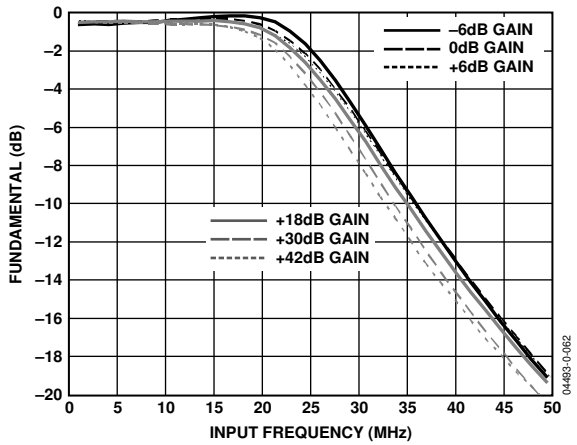


Figure 25. Rx Low-Pass Filter Amplitude Response vs. RxPGA Gain (LPF's $f_{-3\,dB}$ = 33 MHz)

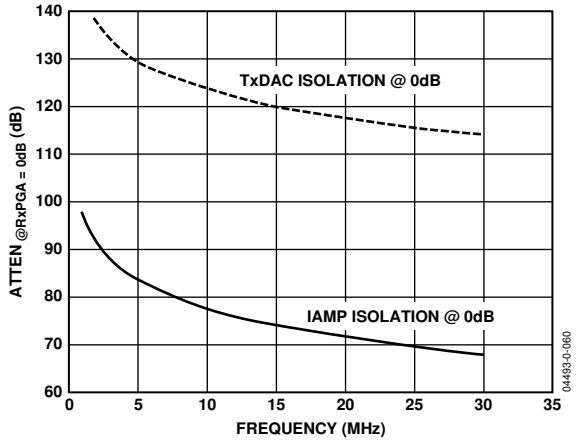


Figure 23. Rx to Tx Full-Duplex Isolation @ 0 RxPGA Setting (Note: ATTEN $_{@\,RxPGA\,=\,x\,dB}$ = ATTEN $_{@\,RxPGA\,=\,0\,dB}$ − RxPGA Gain)

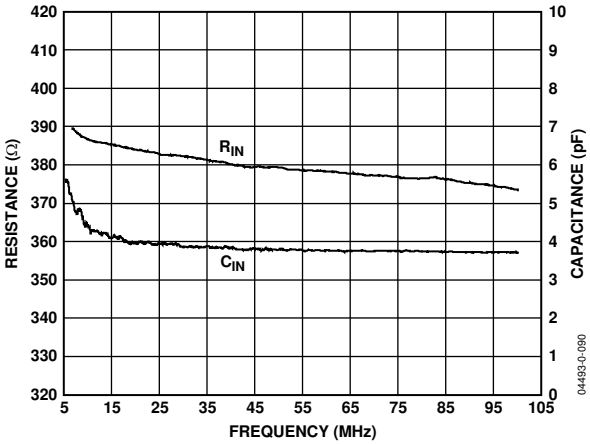


Figure 26. Rx Input Impedance vs. Frequency

TxDAC PATH TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = CLKVDD = DVDD = DRVDD = 3.3 V, f_{OSCIN} = 50 MSPS and 80 MSPS, RSET = 1.96 kΩ, 2:1 transformer coupled output (see Figure 63) into 50 Ω load half- or full-duplex interface, default power bias settings.

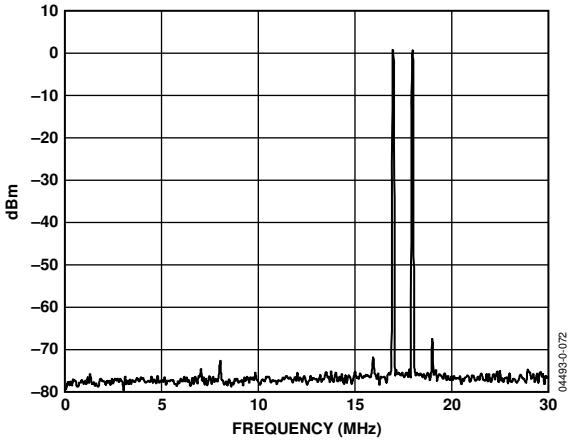


Figure 27. Dual-Tone Spectral Plot of TxDAC's Output (f_{DATA} = 50 MSPS, 4× Interpolation, 10 dBm Peak Power, F1 = 17 MHz, F2 = 18 MHz)

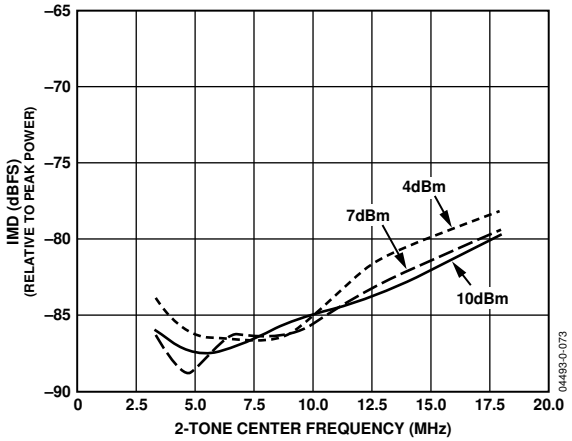


Figure 28. 2-Tone IMD Frequency Sweep vs. Peak Power with f_{DATA} = 50 MSPS, 4× Interpolation

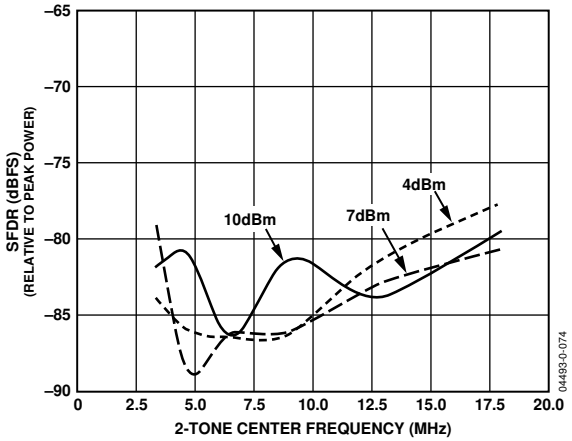


Figure 29. 2-Tone Worst Spur Frequency Sweep vs. Peak Power with f_{DATA} = 50 MSPS, 4× Interpolation

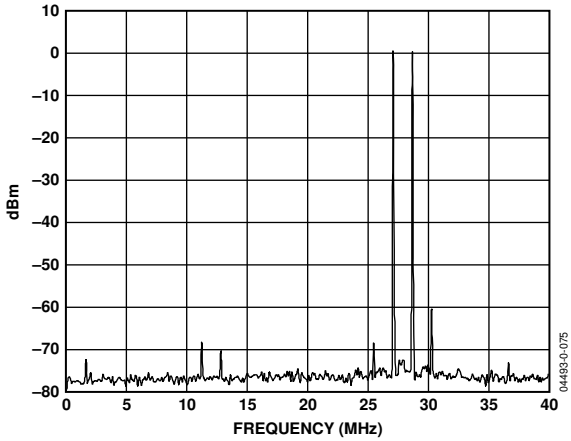


Figure 30. Dual-Tone Spectral Plot of TxDAC's Output (f_{DATA} = 80 MSPS, 2× Interpolation, 10 dBm Peak Power, F1 = 27.1 MHz, F2 = 28.7 MHz)

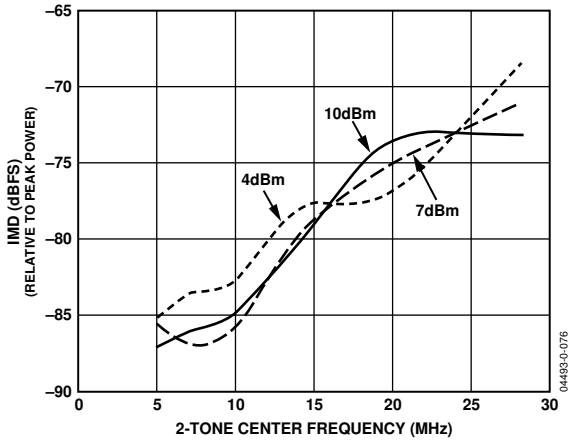


Figure 31. 2-Tone IMD Frequency Sweep vs. Peak Power with f_{DATA} = 80 MSPS, 2× Interpolation

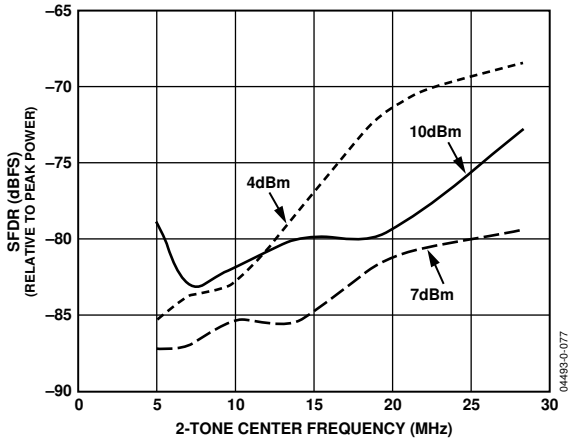


Figure 32. 2-Tone Worst Spur Frequency Sweep vs. Peak Power with f_{DATA} = 80 MSPS, 2× Interpolation

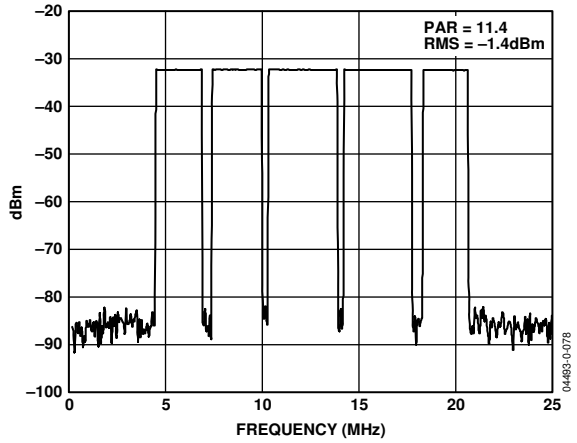


Figure 33. Spectral Plot of 84-Carrier OFDM Test Vector (f_{DATA} = 50 MSPS, 4× Interpolation)

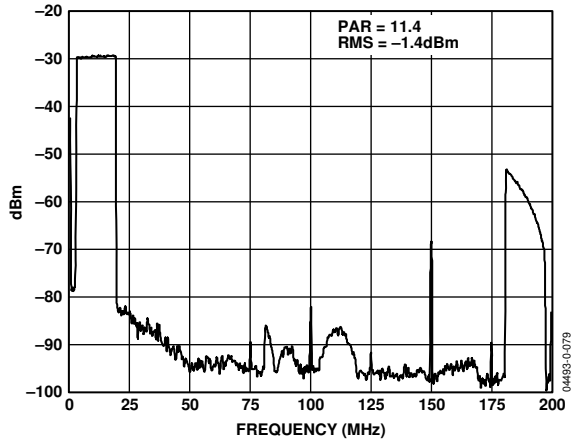


Figure 34. Wideband Spectral Plot of 88-Subcarrier OFDM Test Vector (f_{DATA} = 50 MSPS, 4× Interpolation)

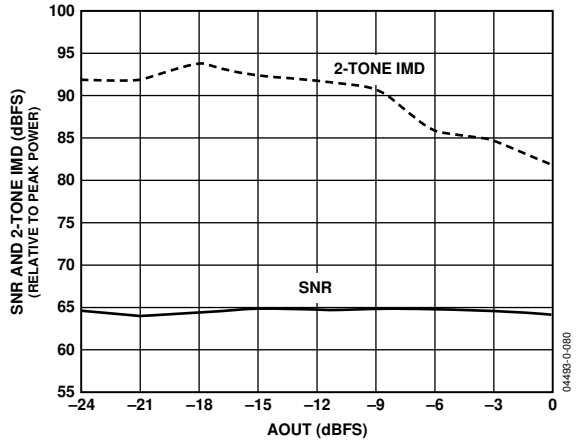


Figure 35. SNR and SFDR vs. P_{OUT} (f_{OUT} = 12.55 MHz, f_{DATA} = 50 MSPS, 4× Interpolation)

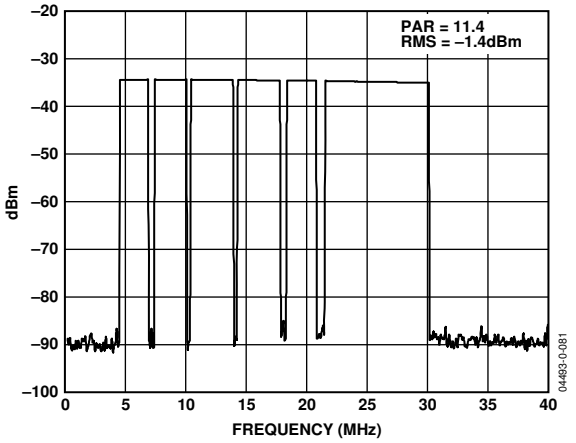


Figure 36. Spectral Plot of 111-Carrier OFDM Test Vector (f_{DATA} = 80 MSPS, 2× Interpolation)

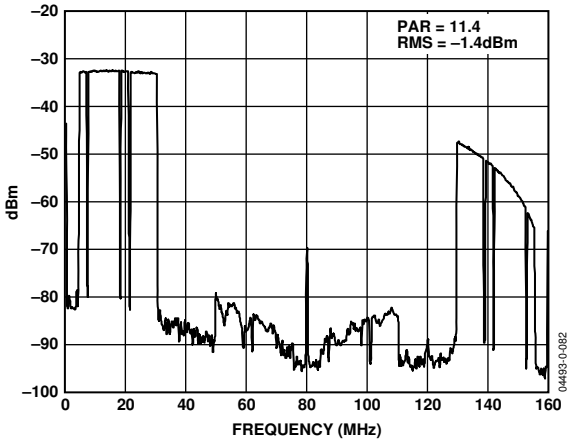


Figure 37. Wideband Spectral Plot of 111-Carrier OFDM Test Vector (f_{DATA} = 80 MSPS, 2× Interpolation)

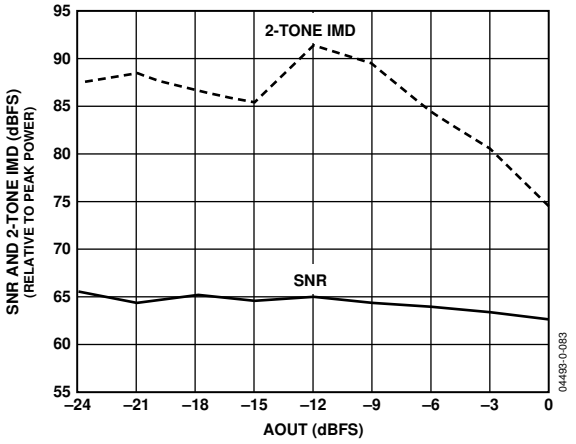


Figure 38. SNR and SFDR vs. P_{OUT} (f_{OUT} = 20 MHz, f_{DATA} = 80 MSPS, 2× Interpolation)

IAMP PATH TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = CLKVDD = DVDD = DRVDD = 3.3 V, f_{OSCIN} = 50 MSPS, R_{SET} = 1.58 kΩ, 1:1 transformer coupled output (see Figure 64 and Figure 65) into 50 Ω load, half- or full-duplex interface, default power bias settings.

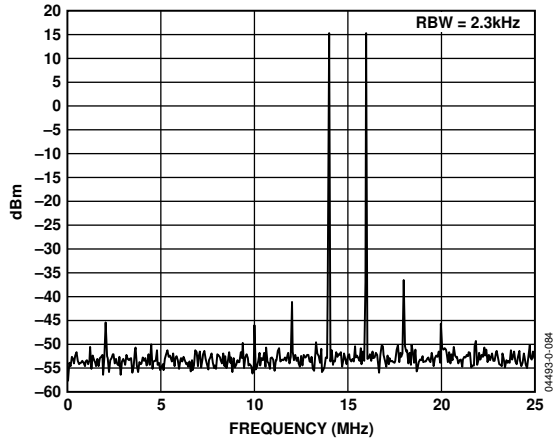


Figure 39. Dual-Tone Spectral Plot of IAMPN Output (IAMP Settings of I = 12.5 mA, N = 4, G = 0, 2:1 Transformer into 75 Ω Loader, VCM = 4.8 V)

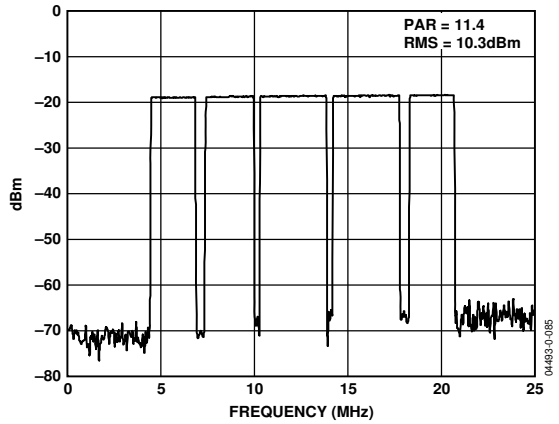


Figure 40. Spectral Plot of 84-Carrier OFDM Test Vector Using IAMPN in Current-Mode Configuration (IAMP Settings of I = 10 mA, N = 4, G = 0; VCM = 4.8 V)

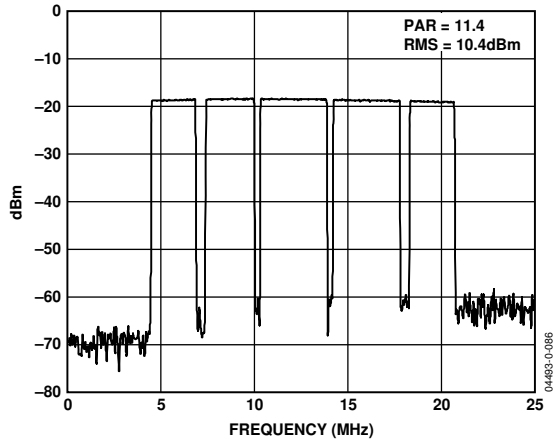


Figure 41. Spectral Plot of 84-Carrier OFDM Test Vector Using IAMP in Voltage-Mode Configuration with AVDD = 5 V (PBR951 Transistors, IAMP Settings of I = 6 mA, N = 2, G = 6)

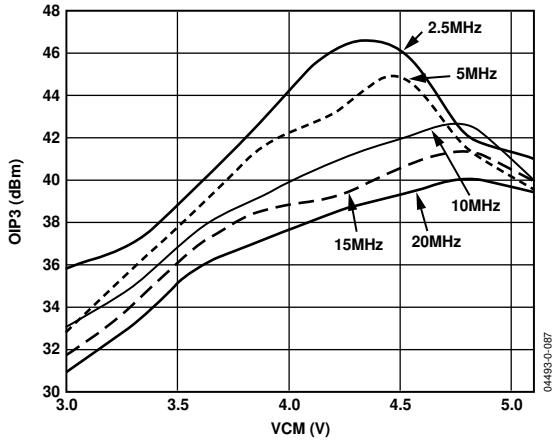


Figure 42. IOUTN Third-Order Intercept vs. Common-Mode Voltage (IAMP Settings of I = 12.5 mA, N = 4, G = 0, 2:1 Transformer into 75 Ω Load)

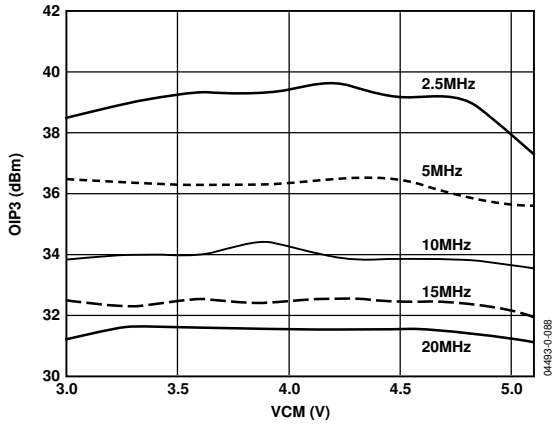


Figure 43. IOUTG Third-Order Intercept vs. Common-Mode Voltage (IAMP Settings of I = 4.25 mA, N = 0, G = 6, 2:1 Transformer into 75 Ω Load)

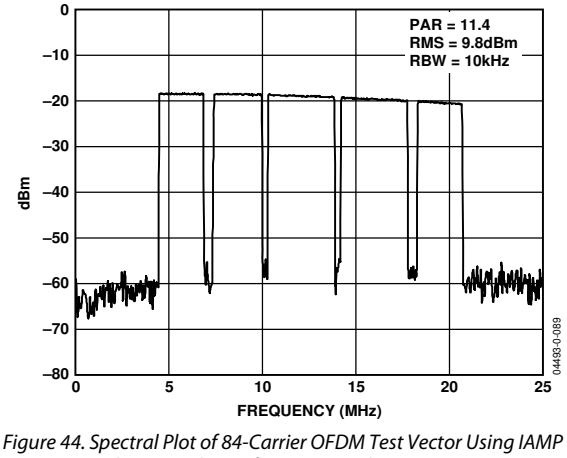


Figure 44. Spectral Plot of 84-Carrier OFDM Test Vector Using IAMP in Voltage-Mode Configuration with AVDD = 3.3 V (PBR951 Transistors, IAMP Settings of I = 6 mA, N = 2, G = 6)

SERIAL PORT

Table 11. SPI Register Mapping

Address (Hex)[1]	Bit Break-down	Description	Width	Power-Up Default Value				Comments
				MODE = 0 (Half-Duplex)		MODE = 1 (Full-Duplex)		
				CONFIG = 0	CONFIG = 1	CONFIG = 0	CONFIG = 1	
SPI PORT CONFIGURATION AND SOFTWARE RESET								
0x00	(7)	4-Wire SPI	1	0	0	0	0	Default SPI configuration is 3-wire, MSB first.
	(6)	LSB First	1	0	0	0	0	
	(5)	S/W Reset	1	0	0	0	0	
POWER CONTROL REGISTERS (via PWR_DWN pin)								
0x01	(7)	Clock Syn.	1	0	0	0	0	PWR_DWN = 0. Default setting is for all blocks powered on.
	(6)	TxDAC/IAMP	1	0	0	0	0	
	(5)	Tx Digital	1	0	0	0	0	
	(4)	REF	1	0	0	0	0	
	(3)	ADC CML	1	0	0	0	0	
	(2)	ADC	1	0	0	0	0	
	(1)	PGA Bias	1	0	0	0	0	
	(0)	RxPGA	1	0	0	0	0	
0x02	(7)	CLK Syn.	1	0	0	0	1*	PWR_DWN = 1. Default setting* is for all functional blocks powered down except PLL. *MODE = CONFIG = 1. Setting has PLL powered down with OSCIN input routed to RXCLK output.
	(6)	TxDAC/IAMP	1	1	1	1	1	
	(5)	Tx Digital	1	1	1	1	1	
	(4)	REF	1	1	1	1	1	
	(3)	ADC CML	1	1	1	1	1	
	(2)	ADC	1	1	1	1	1	
	(1)	PGA Bias	1	1	1	1	1	
	(0)	RxPGA	1	1	1	1	1	
HALF-DUPLEX POWER CONTROL								
0x03	(7:3)	Tx OFF Delay	5	0xFF	0xFF	N/A	N/A	Default setting is for TXEN input to control power on/off of Tx/Rx path. Tx driver delayed by 31 $1/f_{DATA}$ clock cycles.
	(2)	Rx _TXEN	1					
	(1)	Tx PWRDN	1					
	(0)	Rx PWRDN	1					
PLL CLOCK MULTIPLIER/SYNTHESIZER CONTROL								
0x04	(5)	Duty Cycle Enable	1	0	0	0	0	Default setting is Duty Cycle Restore disabled, ADC CLK from OSCIN input, and PLL multiplier × 2 setting. *PLL multiplier × 4 setting.
	(4)	f_{ADC} from PLL	1	0	0	0	0	
	(3:2)	PLL Divide-N	2	00	00	00	00	
	(1:0)	PLL Multiplier-M	2	01	10*	01	01	
0x05	(2)	OSCIN to RXCLK	1	0	0	0	1*	Full-duplex RXCLK normally at nibble rate. *Exception on power-up.
	(1)	Invert RXCLK	1	0	0	0	0	
	(0)	Disabled RXCLK	1	0	0	0	0	
0x06	(7:6)	CLKOUT2 Divide	2	01	01	01	01	Default setting is CLKOUT2 and CLKOUT1 enabled with divide-by-2. *CLKOUT1 and CLKOUT2 disabled.
	(5)	CLKOUT2 Invert	1	0	0	0	0	
	(4)	CLKOUT2 Disable	1	0	0	0	1*	
	(3:2)	CLKOUT1 Divide	2	01	01	01	01	
	(1)	CLKOUT1 Invert	1	0	0	0	0	
	(0)	CLKOUT1 Disable	1	0	0	0	1*	

Address (Hex)[1]	Bit Breakdown	Description	Width	Power-Up Default Value				Comments
				MODE = 0 (Half-Duplex)		MODE = 1 (Full-Duplex)		
				CONFIG = 0	CONFIG = 1	CONFIG = 0	CONFIG = 1	
Rx PATH CONTROL								
0x07	(5)	Initiate Offset Cal.	1	0	0	0	0	Default setting has LPF ON and Rx path at nominal power bias setting. *Rx path to low power.
	(4)	Rx Low Power	1	0	1*	0	1*	
	(0)	Rx Filter ON	1	1	1	1	1	
0x08	(7:0)	Rx Filter Tuning Cut-off Frequency	8	0x80	0x61	0x80	0x80	Refer to Low-Pass Filter section.
Tx/Rx PATH GAIN CONTROL								
0x09	(6)	Use SPI Rx Gain	1	0x00	0x00	0x00	0x00	Default setting is for hardware Rx gain code via PGA or Tx data port.
	(5:0)	Rx Gain Code	6					
0x0A	(6)	Use SPI Tx Gain	1	0x7F	0x7F	0x7F	0x7F	Default setting is for Tx gain code via SPI control.
	(5:0)	Tx Gain Code	6					
Tx AND Rx PGA CONTROL								
0x0B	(6)	PGA Code for Tx	1	0	0	0	0	Default setting is RxPGA control active. *Tx port with GAIN strobe (AD9875/AD9876-compatible). ** 3-bit RxPGA gain map (AD9975-compatible).
	(5)	PGA Code for Rx	1	1	1	1	1	
	(3)	Force GAIN strobe	1	0	0	0	0	
	(2)	Rx Gain on Tx Port	1	0	0	1*	1*	
	(1)	3-Bit RxPGA Port	1	0	1**	0	0	
Tx DIGITAL FILTER AND INTERFACE								
0x0C	(7:6)	Interpolation Factor	2	01	00	01	01	Default setting is 2× interpolation with LPF response. Data format is straight binary for half-duplex and twos complement for full-duplex interface. *Full-duplex only.
	(4)	Invert TXEN/TXSYNC	1	0	0	0	0	
	(3)	Tx 5/5 Nibble*	1	N/A	N/A	0	0	
	(2)	LS Nibble First*	1	N/A	N/A	0	0	
	(1)	TXCLK neg. edge	1	0	0	0	0	
	(0)	Twos complement	1	0	0	1	1	
Rx INTERFACE AND ANALOG/DIGITAL LOOPBACK								
0x0D	(7)	Analog Loopback	1	0	0	0	0	Data format is straight binary for half-duplex and twos complement for full-duplex interface. Analog loopback: ADC Rx data fed back to TxDAC. Digital loopback: Tx input data to Rx output port. *Full-duplex only.
	(6)	Digital Loopback*	1	0	0	0	0	
	(5)	Rx Port 3-State	1	N/A	N/A	0	0	
	(4)	Invert RXEN/RXSYNC	1	0	0	0	0	
	(3)	RX 5/5 Nibble	1	N/A	N/A	0	0	
	(2)	LS Nibble First*	1	N/A	N/A	0	0	
	(1)	RXCLK neg. edge	1	0	0	0	0	
	(0)	Twos complement	1	0	0	1	1	
DIGITAL OUTPUT DRIVE STRENGTH, TxDAC OUTPUT, AND REV ID								
0x0E	(7)	Low Drive Strength	1	0	0	0	0	Default setting is for high drive strength and IAMP enabled.
	(0)	TxDAC Output	1	0	0	0	0	
0x0F	(3:0)	REV ID Number	4	0x00	0x00	0x00	0x00	
Tx IAMP GAIN AND BIAS CONTROL								
0x10	(7)	Select Tx Gain	1	0x44	0x44	0x44	0x44	Secondary path G1 = 0, 1, 2, 3, 4. Primary path N = 0, 1, 2, 3, 4.
	(6:4)	G1	3					
	(2:0)	N	3					

Address (Hex)[1]	Bit Breakdown	Description	Width	Power-Up Default Value				Comments
				MODE = 0 (Half-Duplex)		MODE = 1 (Full-Duplex)		
				CONFIG = 0	CONFIG = 1	CONFIG = 0	CONFIG = 1	
0x11	(6:4)	G2	3	0x62	0x62	0x62	0x62	Secondary path stages: G2 = 0 to 1.50 in 0.25 steps and G3 = 0 to 6.
	(2:0)	G3	3					
0x12	(6:4)	Stand_Secondary	3	0x01	0x01	0x01	0x01	Standing current of primary and secondary path.
	(2:0)	Stand_Primary	3					
0x13	(7:5)	CPGA Bias Adjust	3	0x00	0x00	0x00	0x00	Current bias setting for Rx path's functional blocks. Refer to page 41.
	(4:3)	SPGA Bias Adjust	2					
	(2:0)	ADC Bias Adjust	4					

[1] Bits that are undefined should always be assigned a 0.

REGISTER MAP DESCRIPTION

The AD9865 contains a set of programmable registers described in Table 11 that are used to optimize its numerous features, interface options, and performance parameters from its default register settings. Registers pertaining to similar functions have been grouped together and assigned adjacent addresses to minimize the update time when using the multibyte serial port interface (SPI) read/write feature. Bits that are undefined within a register should be assigned a 0 when writing to that register.

The default register settings were intended to allow some applications to operate without the use of an SPI. The AD9865 can be configured to support a half- or full-duplex digital interface via the MODE pin, with each interface having two possible default register settings determined by the setting of the CONFIG pin.

For instance, applications that need to use only the Tx or Rx path functionality of the AD9865 can configure it for a half-duplex interface (MODE = 0), and use the TXEN pin to select between the Tx or Rx signal path with the unused path remaining in a reduced power state. The CONFIG pin can be used to select the default interpolation ratio of the Tx path and RxPGA gain mapping.

SERIAL PORT INTERFACE (SPI)

The serial port of the AD9865 has 3- or 4-wire SPI capability allowing read/write access to all registers that configure the device's internal parameters. Registers pertaining to the SPI are listed in Table 12. The default 3-wire serial communication port consists of a clock (SCLK), serial port enable ($\overline{SEN}$), and a bi-directional data (SDIO) signal. $\overline{SEN}$ is an active low control gating read and write cycle. When $\overline{SEN}$ is high, SDO and SDIO are three-stated. The inputs to SCLK, $\overline{SEN}$, and SDIO contain a Schmitt trigger with a nominal hysteresis of 0.4 V centered about VDDH/2. The SDO pin remains three-stated in a 3-wire SPI interface.

Table 12. SPI Registers Pertaining to SPI Options

Address (Hex)	Bit	Description
0x00	(7)	Enable 4-wire SPI
	(6)	Enable SPI LSB first

A 4-wire SPI can be enabled by setting the 4-wire SPI bit high, causing the output data to appear on the SDO pin instead of on the SDIO pin. The SDIO pin serves as an input-only throughout the read operation. Note that the SDO pin is active only during the transmission of data and remains three-stated at any other time.

An 8-bit instruction header must accompany each read and write operation. The instruction header is shown in Table 13. The MSB is an R/$\overline{W}$ indicator bit with logic high indicating a read operation. The next two bits, N1 and N0, specify the number of bytes (one to four bytes) to be transferred during the data transfer cycle. The remaining five bits specify the address bits to be accessed during the data transfer portion. The data bits immediately follow the instruction header for both read and write operations.

Table 13. Instruction Header Information

MSB						LSB	
17	16	15	14	13	12	11	10
R/$\overline{W}$	N1	N0	A4	A3	A2	A1	A0

The AD9865 serial port can support both MSB (most significant bit) first and LSB (least significant bit) first data formats. Figure 45 illustrates how the serial port words are built for the MSB first and LSB first modes. The bit order is controlled by the SPI LSB first bit (Register 0, Bit 6). The default value is 0, MSB first. Multibyte data transfers in MSB format can be completed by writing an instruction byte that includes the register address of the last address to be accessed. The AD9865 automatically decrements the address for each successive byte required for the multibyte communication cycle.

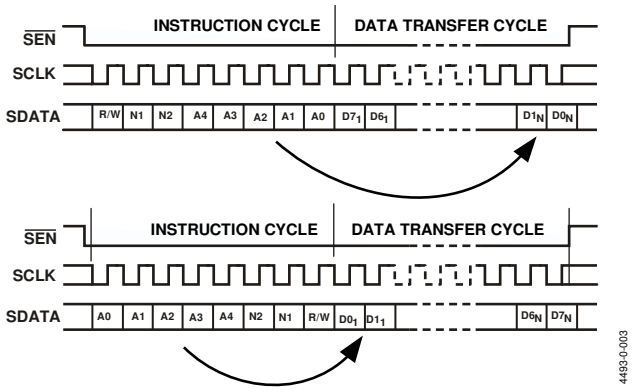


Figure 45. SPI Timing, MSB First (Upper), and LSB First (Lower)

When the SPI LSB first bit is set high, the serial port interprets both instruction and data bytes LSB first. Multibyte data transfers in LSB format can be completed by writing an instruction byte that includes the register address of the first address to be accessed. The AD9865 automatically increments the address for each successive byte required for the multibyte communication cycle.

Figure 46 illustrates the timing requirements for a write operation to the SPI port. After the serial port enable ($\overline{SEN}$) signal goes low, data (SDIO) pertaining to the instruction header is read on the rising edges of the clock (SCLK). To initiate a write operation, the read/not-write bit is set low. After the instruction header is read, the eight data bits pertaining to the specified register are shifted into the SDIO pin on the rising edge of the next eight clock cycles. If a multibyte communication cycle is specified, the destination address is decremented (MSB first) and shifts in another eight bits of data. This process repeats until all the bytes specified in the instruction header (N1, N0 bits) are shifted into the SDIO pin. $\overline{SEN}$ must remain low during the data transfer operation, only going high after the last bit is shifted into the SDIO pin.

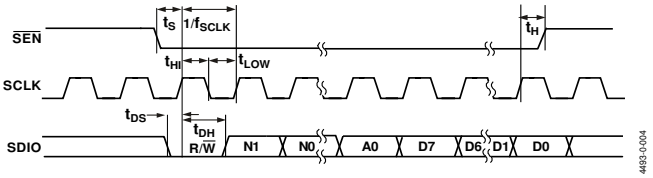


Figure 46. SPI Write Operation Timing

Figure 47 illustrates the timing for a 3-wire read operation to the SPI port. After $\overline{SEN}$ goes low, data (SDIO) pertaining to the instruction header is read on the rising edges of SCLK. A read operation occurs, if the read/not-write indicator is set high. After the address bits of the instruction header are read, the eight data bits pertaining to the specified register are shifted out of the SDIO pin on the falling edges of the next eight clock cycles. If a multibyte communication cycle is specified in the instruction header, a similar process as previously described for a multibyte SPI write operation applies. The SDO pin remains three-stated in a 3-wire read operation.

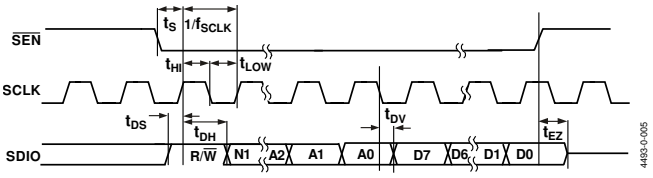


Figure 47. SPI 3-Wire Read Operation Timing

Figure 48 illustrates the timing for a 4-wire read operation to the SPI port. The timing is similar to the 3-wire read operation with the exception that data appears at the SDO pin, while the SDIO pin remains high impedance throughout the operation. The SDO pin is an active output only during the data transfer phase and remains three-stated at all other times.

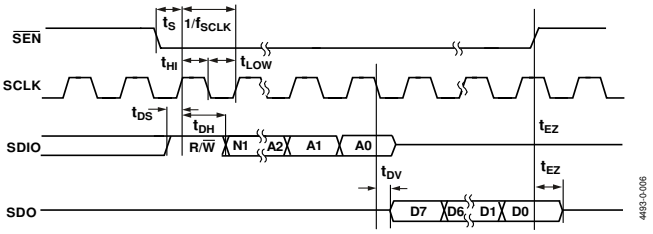


Figure 48. SPI 4-Wire Read Operation Timing

DIGITAL INTERFACE

The digital interface port is configurable for half-duplex or full-duplex operation by pin-strapping the MODE pin low or high, respectively. In half-duplex mode, the digital interface port becomes a 10-bit bidirectional bus called the ADIO port. In full-duplex mode, the digital interface port is divided into two 6-bit ports called Tx[5:0] and Rx[5:0] for simultaneous Tx and Rx operations. In this mode, data is transferred between the ASIC and AD9865 in 6-bit (or 5-bit) nibbles. The AD9865 also features a flexible digital interface for updating the RxPGA and TxPGA gain registers via a 6-bit PGA port or Tx[5:0] port for fast updates, or via the SPI port for slower updates. See the RxPGA Control section for more information.

HALF-DUPLEX MODE

The half-duplex mode functions as follows when the MODE pin is tied low. The bidirectional ADIO port is typically shared in burst fashion between the transmit path and receive path. Two control signals, TXEN and RXEN, from a DSP (or digital ASIC) control the bus direction by enabling the ADIO port's input latch and output driver, respectively. Two clock signals are also used: TXCLK to latch the Tx input data, and RXCLK to clock the Rx output data. The ADIO port can also be disabled by setting TXEN and RXEN low (default setting), thus allowing it to be connected to a shared bus.

Internally, the ADIO port consists of an input latch for the Tx path in parallel with an output latch with three-state outputs for the Rx path. TXEN is used to enable the input latch; RXEN is used to three-state the output latch. A five-sample-deep FIFO is used on the Tx and Rx paths to absorb any phase difference between the AD9865's internal clocks and the externally supplied clocks (TXCLK, RXCLK). The ADIO bus accepts input datawords into the transmit path when the TXEN pin is high, the RXEN pin is low, and a clock is present on the TXCLK pin, as shown in Figure 49.

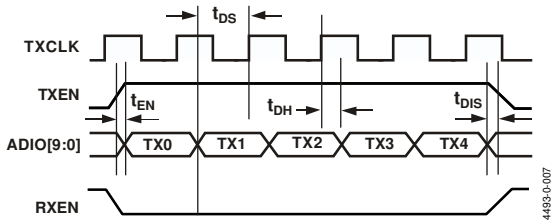


Figure 49. Transmit Data Input Timing Diagram

The Tx interpolation filter(s) following the ADIO port can be flushed with zeros, if the clock signal into the TXCLK pin is present for 33 clock cycles after TXEN goes low. Note that the data on the ADIO bus is irrelevant over this interval.

The output from the receive path is driven onto the ADIO bus when the RXEN pin is high, and a clock is present on the RXCLK pin. While the output latch is enabled by RXEN, valid data appears on the bus after a 6-clock-cycle delay due to the internal FIFO delay. Note that Rx data is not latched back into the Tx path, if TXEN is high during this interval with TXCLK present. The ADIO bus becomes three-stated once the RXEN pin returns low. Figure 50 shows the receive path output timing.

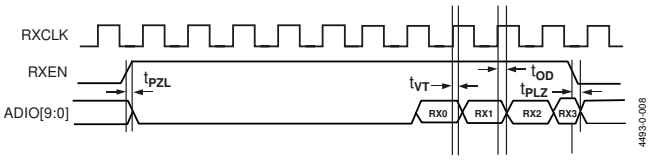


Figure 50. Receive Data Output Timing Diagram

To add flexibility to the digital interface port, several programming options are available in the SPI registers. These options are listed in Table 14. The default Tx and Rx data input formats are straight binary, but can be changed to twos complement. The default TXEN and RXEN settings are active high, but can be set to opposite polarities, thus allowing them to share the same control. In this case, the ADIO port can still be placed onto a shared bus by disabling its input latch via the control signal, and disabling the output driver via the SPI register. The clock timing can be independently changed on the transmit and receive paths by selecting either the rising or falling clock edge as the validating/sampling edge of the clock. Lastly, the output driver's strength can be reduced for lower data rate applications.

Table 14. SPI Registers for Half-Duplex Interface

Address (Hex)	Bit	Description
0x0C	(4)	Invert TXEN
	(1)	TXCLK negative edge
	(0)	Twos complement
0x0D	(5)	Rx port three-state
	(4)	Invert RXEN
	(1)	RXCLK negative edge
	(0)	Twos complement
0x0E	(7)	Low digital drive strength

The half-duplex interface can be configured to act as a slave or a master to the digital ASIC. An example of a slave configuration is shown in Figure 51. In this example, the AD9865 accepts all the clock and control signals from the digital ASIC. Because the sampling clocks for the DAC and ADC are derived internally from the OSCIN signal, the TXCLK and RXCLK signals must be at exactly the same frequency as the OSCIN signal. The phase relationships among the TXCLK, RXCLK, and OSCIN signals can be arbitrary. If the digital ASIC cannot provide a low jitter clock source to OSCIN, use the AD9865 to generate the clock for its DAC and ADC, and to pass the desired clock signal to the digital ASIC via CLKOUT1 or CLKOUT2.

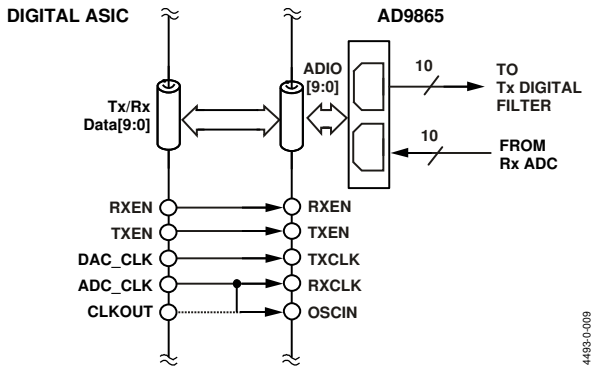


Figure 51. Example of a Half-Duplex Digital Interface with AD9865 Serving as the Slave

Figure 52 shows a half-duplex interface with the AD9865 acting as the master, generating all the required clocks. CLKOUT1 provides a clock equal to the bus data rate that is fed to the ASIC as well as back to the TXCLK and RXCLK inputs. This interface has the advantage of reducing the digital ASIC's pin count by three. The ASIC needs only to generate a bus control signal that controls the data flow on the bidirectional bus.

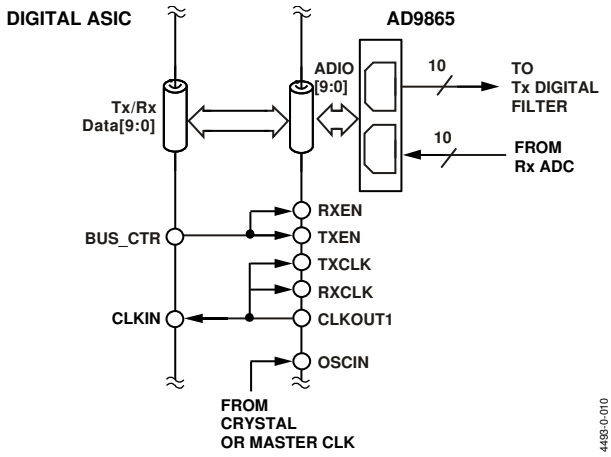


Figure 52. Example of a Half-Duplex Digital Interface with AD9865 Serving as the Master

FULL-DUPLEX MODE

The full-duplex mode interface is selected when the MODE pin is tied high. It can be used for full- or half-duplex applications. The digital interface port is divided into two 6-bit ports called Tx[5:0] and Rx[5:0], allowing simultaneous Tx and Rx operations for full-duplex applications. In half-duplex applications, the Tx[5:0] port can also be used to provide a fast update of the RxPGA (AD9875 backward-compatible) during an Rx operation. This feature is enabled by default and can be used to reduce the required pin count of the ASIC (refer to RxPGA Control section for details).

In either application, Tx and Rx data are transferred between the ASIC and AD9865 in 6-bit (or 5-bit) nibbles at twice the internal input/output word rates of the Tx interpolation filter and ADC. Note that the TxDAC update rate *must not* be less than the nibble rate. Therefore, the 2× or 4× interpolation filter must be used with a full-duplex interface.

The AD9865 acts as the master, providing RXCLK as an output clock that is used for the timing of both the Tx[5:0] and Rx[5:0] ports. RXCLK always runs at the nibble rate and can be inverted or disabled via an SPI register. Because RXCLK is derived from the clock synthesizer, it remains active, provided that this functional block remains powered on. A buffered version of the signal appearing at OSCIN can also be directed to RXCLK by setting Bit 2 of Register 0x05. This feature allows the AD9865 to be completely powered down (including the clock synthesizer) while serving as the master.

The Tx[5:0] port operates in the following manner with the SPI register default settings. Two consecutive nibbles of the Tx data are multiplexed together to form a 10-bit data-word in twos complement format. The clock appearing on the RXCLK pin is a buffered version of the internal clock used by the Tx[5:0] port's input latch with a frequency that is always twice the ADC sample rate ($2 \times f_{ADC}$). Data from the Tx[5:0] port is read on the rising edge of this sampling clock, as illustrated in the timing diagram shown in Figure 53. Note, $\overline{\text{TXQUIET}}$ must remain high for the reconstructed Tx data to appear as an analog signal at the output of the TxDAC or IAMP.

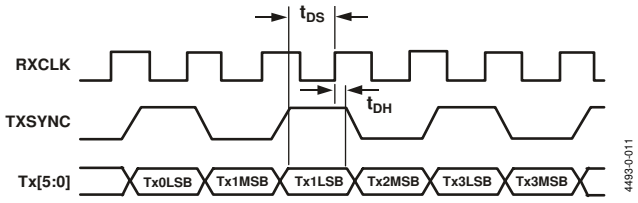


Figure 53. Tx[5:0] Port Full-Duplex Timing Diagram

The TXSYNC signal is used to indicate to which word a nibble belongs. While TXSYNC is low, the first nibble of every word is read as the most significant nibble. The second nibble of that same word is read on the following TXSYNC high level as the least significant nibble. If TXSYNC is low for more than one clock cycle, the last transmit data is read continuously until TXSYNC is brought high for the second nibble of a new transmit word. This feature can be used to flush the interpolator filters with zeros. Note that the GAIN signal must be kept low during a Tx operation.

The Rx[5:0] port operates in the following manner with the SPI register default settings. Two consecutive nibbles of the Rx data are multiplexed together to form a 10-bit data-word in twos complement format. The Rx data is valid on the rising edge of RXCLK, as illustrated in the timing diagram shown in Figure 54. The RXSYNC signal is used to indicate to which word a nibble belongs. While RXSYNC is low, the first nibble of every word is transmitted as the most significant nibble. The second nibble of that same word is transmitted on the following RXSYNC high level as the least significant nibble.