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IF Digitizing Subsystem

AD9874*

FEATURES

10 MHz to 300 MHz Input Frequency
7.2 kHz to 270 kHz Output Signal Bandwidth
8.1 dB SSB NF
0 dBm IIP3
AGC Free Range up to –34 dBm
12 dB Continuous AGC Range
16 dB Front End Attenuator
Baseband I/Q 16-Bit (or 24-Bit) Serial Digital Output
LO and Sampling Clock Synthesizers
Programmable Decimation Factor, Output Format, AGC, and Synthesizer Settings
370 Ω Input Impedance
2.7 V to 3.6 V Supply Voltage
Low Current Consumption: 20 mA
48-Lead LQFP Package (1.4 mm Thick)

APPLICATIONS

Multimode Narrow-Band Radio Products
Analog/Digital UHF/VHF FDMA Receivers
TETRA, APCO25, GSM/EDGE
Portable and Mobile Radio Products
Base Station Applications
SATCOM Terminals

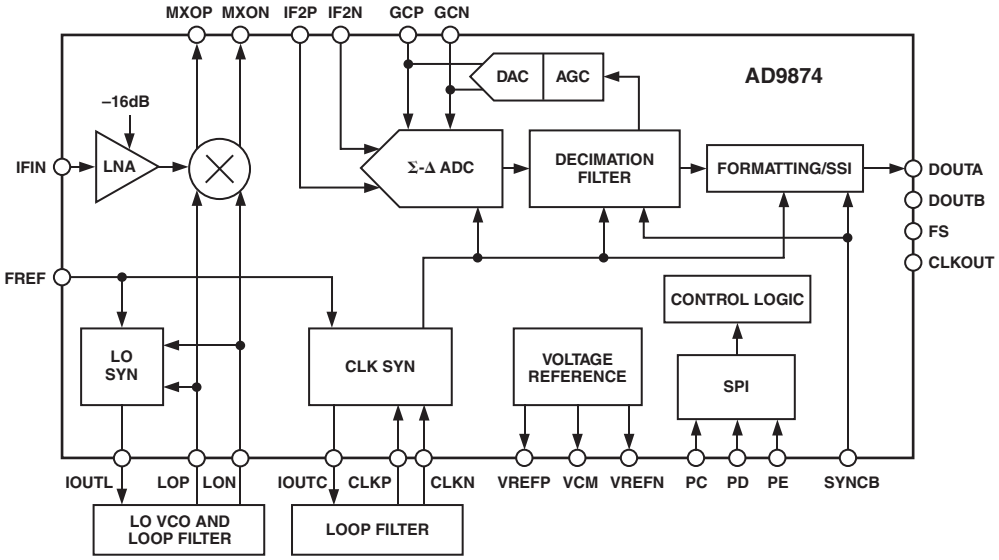
GENERAL DESCRIPTION

The AD9874 is a general-purpose IF subsystem that digitizes a low level 10 MHz to 300 MHz IF input with a signal bandwidth ranging from 6.8 kHz to 270 kHz. The signal chain of the AD9874 consists of a low noise amplifier, a mixer, a band-pass sigma-delta analog-to-digital converter, and a decimation filter with programmable decimation factor. An automatic gain control (AGC) circuit gives the AD9874 12 dB of continuous gain adjustment. Auxiliary blocks include both clock and LO synthesizers.

The AD9874's high dynamic range and inherent antialiasing provided by the band-pass sigma-delta converter allow the AD9874 to cope with blocking signals up to 95 dB stronger than the desired signal. This attribute can often reduce the cost of a radio by reducing its IF filtering requirements. Also, it enables multimode radios of varying channel bandwidths, allowing the IF filter to be specified for the largest channel bandwidth.

The SPI port programs numerous parameters of the AD9874, thus allowing the device to be optimized for any given application. Programmable parameters include synthesizer divide ratios, AGC attenuation and attack/decay time, received signal strength level, decimation factor, output data format, 16 dB attenuator, and the selected bias currents. The bias currents of the LNA and mixer can be further reduced at the expense of degraded performance for battery-powered applications.

FUNCTIONAL BLOCK DIAGRAM



*Protected by U.S. Patent No. 5,969,657;

REV. A

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AD9874* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- Evaluation Board for AD9864 and AD9874

DOCUMENTATION

Data Sheet

- AD9874: IF Digitizing Subsystem Data Sheet

REFERENCE MATERIALS

Technical Articles

- Low-Power IC Digitizes 300 MHz IF
- MS-2210: Designing Power Supplies for High Speed ADC
- MS-2735: Maximizing the Dynamic Range of Software-Defined Radio

DESIGN RESOURCES

- AD9874 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9874 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

AD9874–SPECIFICATIONS (VDDI = VDDF = VDDA = VDDC = VDDL = VDDD = VDDH = 2.7 V to 3.6 V, VDDQ = VDDP = 2.7 V to 5.5 V, f_{CLK} = 18 MSPS, f_{IF} = 109.65 MHz, f_{LO} = 107.4 MHz, f_{REF} = 16.8 MHz, unless otherwise noted.)[1]

Parameter	Temp	Test Level	Min	Typ	Max	Unit
SYSTEM DYNAMIC PERFORMANCE[2]						
SSB Noise Figure @ Min VGA Attenuation[3, 4]	Full	IV		8.1	9.5	dB
@ Max VGA Attenuation[3, 4]	Full	IV		13		dB
Dynamic Range with AGC Enabled[3, 4]	Full	IV	91	95		dB
IF Input Clip Point @ Max VGA Attenuation[3]	Full	IV	–20	–19		dBm
@ Min VGA Attenuation[3]	Full	IV	–32	–31		dBm
Input Third Order Intercept (IIP3)	Full	IV	–5	0		dBm
Gain Variation over Temperature	Full	IV		0.7	2	dB
LNA + MIXER						
Maximum RF and LO Frequency Range	Full	IV	300	500		MHz
LNA Input Impedance	25°C	V		370//1.4		Ω//pF
Mixer LO Input Resistance	25°C	V		1		kΩ
LO SYNTHESIZER						
LO Input Frequency	Full	IV	7.75		300	MHz
LO Input Amplitude	Full	IV	0.3		2.0	V p-p
FREF Frequency (for Sinusoidal Input ONLY)	Full	IV	8		25	MHz
FREF Input Amplitude	Full	IV	0.3		3	V p-p
FREF Slew Rate	Full	IV	7.5			V/μs
Minimum Charge Pump Current @ 5 V[5]	Full	VI	0.48	0.67	0.78	mA
Maximum Charge Pump Current @ 5 V[5]	Full	VI	3.87	5.3	6.2	mA
Charge Pump Output Compliance[6]	Full	VI	0.4		VDDP – 0.4	V
Synthesizer Resolution	Full	IV	6.25			kHz
CLOCK SYNTHESIZER						
CLK Input Frequency	Full	IV	13		26	MHz
CLK Input Amplitude	Full	IV	0.3		VDDC	V p-p
Minimum Charge Pump Output Current[5]	Full	VI	0.48	0.67	0.78	mA
Maximum Charge Pump Output Current[5]	Full	VI	3.87	5.3	6.2	mA
Charge Pump Output Compliance[6]	Full	VI	0.4		VDDQ – 0.4	V
Synthesizer Resolution	Full	IV	2.2			kHz
SIGMA-DELTA ADC						
Resolution	Full	IV	16		24	Bits
Clock Frequency (f_{CLK})	Full	IV	13		26	MHz
Center Frequency	Full	V		$f_{CLK}/8$		MHz
Pass-Band Gain Variation	Full	IV			1.0	dB
Alias Attenuation	Full	IV	80			dB
GAIN CONTROL						
Programmable Gain Step	Full	V		16		dB
AGC Gain Range (Continuous)	Full	V		12		dB
GCP Output Resistance	Full	IV	50	72.5	95	kΩ
OVERALL						
Analog Supply Voltage (VDDA, VDDF, VDDI)	Full	VI	2.7	3.0	3.6	V
Digital Supply Voltage (VDDD, VDDC, VDDL)	Full	VI	2.7	3.0	3.6	V
Interface Supply Voltage[7] (VDDH)	Full	VI	1.8		3.6	V
Charge Pump Supply Voltage (VDDP, VDDQ)	Full	VI	2.7	5.0	5.5	V
Total Current						
High Performance Setting[8]	Full	VI		20	26.5	mA
Low Power Mode[8]	Full	VI		17	22	mA
Standby	Full	VI		0.01	0.1	mA
OPERATING TEMPERATURE RANGE			–40		+85	°C

NOTES

[1]Standard operating mode: LNA/Mixer @ high bias setting, VGA @ Min ATTEN setting, synthesizers in normal (not fast acquire) mode, f_{CLK} = 18 MHz, decimation factor = 900, 16-bit digital output, and 10 pF load on SSI output pins.

[2]This includes 0.9 dB loss of matching network.

[3]AGC with DVGA enabled.

[4]Measured in 10 kHz bandwidth.

[5]Programmable in 0.67 mA steps.

[6]Voltage span in which LO (or CLK) charge pump output current is maintained within 5% of nominal value of VDDP/2 (or VDDQ/2).

[7]VDDH must be less than VDDD + 0.5 V.

[8] Clock VCO off, add additional 0.7 mA with VGA @ Max ATTEN setting.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (VDDI = VDDF = VDDA = VDDC = VDDL = VDDD = VDDH = 2.7 V to 3.6 V, VDDQ = VDDP = 2.7 V to 5.5 V, f_{CLK} = 18 MSPS, f_{IF} = 109.65 MHz, f_{LO} = 107.4 MHz, f_{REF} = 16.8 MHz, unless otherwise noted.)[1]

Parameter	Temp	Test Level	Min	Typ	Max	Unit
DECIMATOR						
Decimation Factor[2]	Full	IV	48		960	
Pass-Band Width	Full	V		50%		f_{CLKOUT}
Pass-Band Gain Variation	Full	IV			1.2	dB
Alias Attenuation	Full	IV	88			dB
SPI-READ OPERATION (See Figure 1a)						
PC Clock Frequency	Full	IV			10	MHz
PC Clock Period (t_{CLK})	Full	IV	100			ns
PC Clock HI (t_{HI})	Full	IV	45			ns
PC Clock LOW (t_{LOW})	Full	IV	45			ns
PC to PD Setup Time (t_{DS})	Full	IV	2			ns
PC to PD Hold Time (t_{DH})	Full	IV	2			ns
$\overline{PE}$ to PC Setup Time (t_S)	Full	IV	5			ns
PC to $\overline{PE}$ Hold Time (t_H)	Full	IV	5			ns
SPI-WRITE OPERATION[3] (See Figure 1b)						
PC Clock Frequency	Full	IV			10	MHz
PC Clock Period (t_{CLK})	Full	IV	100			ns
PC Clock HI (t_{HI})	Full	IV	45			ns
PC Clock LOW (t_{LOW})	Full	IV	45			ns
PC to PD Setup Time (t_{DS})	Full	IV	2			ns
PC to PD Hold Time (t_{DH})	Full	IV	2			ns
PC to PD (or DOUBT) Data Valid Time (t_{DV})	Full	IV	3			ns
$\overline{PE}$ to PD Output Valid to Hi-Z (t_{EZ})	Full	IV		8		ns
SSI[3] (see Figure 2b)						
CLKOUT Frequency	Full	IV	0.867		26	MHz
CLKOUT Period (t_{CLK})	Full	IV	38.4		1153	ns
CLKOUT Duty Cycle (t_{HI}, t_{LOW})	Full	IV	33	50	67	ns
CLKOUT to FS Valid Time (t_V)	Full	IV	–1		+1	ns
CLKOUT to DOUT Data Valid Time (t_{DV})	Full	IV	–1		+1	ns
CMOS LOGIC INPUTS[4]						
Logic "1" Voltage (V_{IH})	Full	IV	VDDH – 0.2			V
Logic "0" Voltage (V_{IL})	Full	IV			0.5	V
Logic "1" Current (V_{IH})	Full	IV		10		µA
Logic "0" Current (V_{IL})	Full	IV		10		µA
Input Capacitance	Full	IV		3		pF
CMOS LOGIC OUTPUTS[3, 4, 5]						
Logic "1" Voltage (V_{IH})	Full	IV		VDDH – 0.2		V
Logic "0" Voltage (V_{IL})	Full	IV			0.2	V

NOTES

[1]Standard operating mode: high IIP3 setting, synthesizers in normal (not fast acquire) mode, f_{CLK} = 18 MHz, decimation factor = 300, 10 pF load on SSI output pins: VDDx = 3.0 V.

[2]Programmable in steps of 48 or 60.

[3]CMOS output mode with C_{LOAD} = 10 pF and Drive Strength = 7.

[4]Absolute Max and Min input/output levels are VDDH +0.3 V and –0.3 V.

[5]I_{OL} = 1 mA; specification is also dependent on Drive Strength setting.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Unit
VDDF, VDDA, VDDC, VDDD, VDDH, VDDL, VDDI	GNDF, GNDA, GNDC, GNDD, GNDH, GNDL, GNDI, GNDS	–0.3	+4.0	V
VDDF, VDDA, VDDC, VDDD, VDDH, VDDL, VDDI	VDDR, VDDA, VDDC, VDDD, VDDH, VDDL, VDDI	–4.0	+4.0	V
VDDP, VDDQ	GNDP, GNDQ	–0.3	+6.0	V
GNDF, GNDA, GNDC, GNDD, GNDH, GNDL, GNDI, GNDQ, GNDP, GNDS	GNDF, GNDA, GNDC, GNDD, GNDH, GNDL, GNDI, GNDQ, GNDP, GNDS	–0.3	+0.3	V
MXOP, MXON, LOP, LON, IFIN, CXIF, CXVL, CXVM	GNDI	–0.3	VDDI + 0.3	V
PC, PD, PE, CLKOUT, DOUTA, DOUTB, FS, SYNCB	GNDH	–0.3	VDDH + 0.3	V
IF2N, IF2P, GCP, GCN	GNDF	–0.3	VDDF + 0.3	V
VREFP, VREFN, RREF	GNDA	–0.3	VDDA + 0.3	V
IOUTC	GNDQ	–0.3	VDDQ + 0.3	V
IOUTL	GNDP	–0.3	VDDP + 0.3	V
CLKP, CLKN	GNDC	–0.3	VDDC + 0.3	V
FREF	GNDL	–0.3	VDDL + 0.3	V
Junction Temperature			150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Thermal Resistance

48-Lead LQFP
θ_{JA} = 76.2°C/W

θ_{JC} = 17°C/W

EXPLANATION OF TEST LEVELS
TEST LEVEL

I. 100% production tested.

II. 100% production tested at 25°C and sample tested at specified temperatures. AC testing done on sample basis.

III. Sample tested only.

IV. Parameter is guaranteed by design and/or characterization testing.

V. Parameter is a typical value only.

VI. All devices are 100% production tested at 25°C; min and max guaranteed by design and characterization for industrial temperature range.

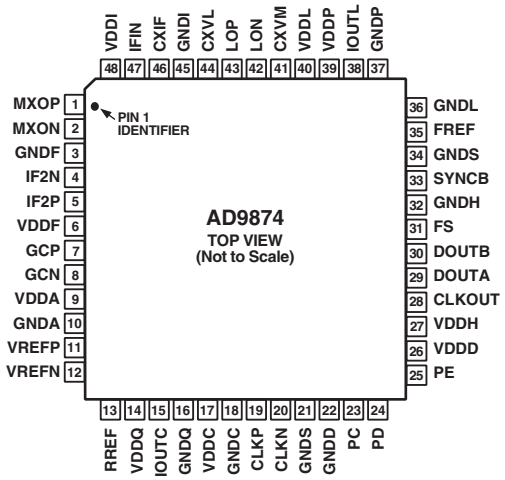
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9874ABST	–40°C to +85°C	48-Lead Thin Plastic Quad Flatpack (LQFP)	ST-48
AD9874EB		Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9874 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Description
1	MXOP	Mixer Output, Positive.
2	MXON	Mixer Output, Negative.
3	GNDF	Ground for Front End of ADC.
4	IF2N	Second IF Input (to ADC), Negative.
5	IF2P	Second IF Input (to ADC), Positive.
6	VDDF	Positive Power Supply for Front End of ADC.
7	GCP	Filter Capacitor for ADC Full-Scale Control.
8	GCN	Full-Scale Control Ground.
9	VDDA	Positive Power Supply for ADC Back End.
10	GNDA	Ground for ADC Back End.
11	VREFP	Voltage Reference, Positive.
12	VREFN	Voltage Reference, Negative.
13	RREF	Reference Resistor: Requires 100 kΩ to GNDA.
14	VDDQ	Positive Power Supply for Clock Synthesizer.
15	IOUTC	Clock Synthesizer Charge Pump Output Current.
16	GNDQ	Ground for Clock Synthesizer Charge Pump.
17	VDDC	Positive Power Supply for Clock Synthesizer.
18	GNDC	Ground for Clock Synthesizer.
19	CLKP	Sampling Clock Input/Clock VCO Tank, Positive.
20	CLKN	Sampling Clock Input/Clock VCO Tank, Negative.
21	GNDS	Substrate Ground.
22	GNDD	Ground for Digital Functions.
23	PC	Clock Input for SPI Port.
24	PD	Data I/O for SPI Port.
25	PE	Enable Input for SPI Port.
26	VDDD	Positive Power Supply for Internal Digital Function.

Pin	Mnemonic	Description
27	VDDH	Positive Power Supply for Digital Interface.
28	CLKOUT	Clock Output for SSI Port.
29	DOUTA	Data Output for SSI Port.
30	DOUTB	Data Output for SSI Port (Inverted) or SPI Port.
31	FS	Frame Sync for SSI Port.
32	GNDH	Ground for Digital Interface.
33	SYNCB	Resets SSI and Decimator Counters; Active Low.
34	GNDS	Substrate Ground.
35	FREF	Reference Frequency Input for Both Synthesizers.
36	GNDL	Ground for LO Synthesizer.
37	GNDP	Ground for LO Synthesizer Charge Pump.
38	IOUTL	LO Synthesizer Charge Pump Output Current Charge Pump.
39	VDDP	Positive Power Supply for LO Synthesizer Charge Pump.
40	VDDL	Positive Power Supply for LO Synthesizer.
41	CXVM	External Filter Capacitor; DC Output of LNA.
42	LON	LO Input to Mixer and LO Synthesizer, Negative.
43	LOP	LO Input to Mixer and LO Synthesizer, Positive.
44	CXVL	External Bypass Capacitor for LNA Power Supply.
45	GNDI	Ground for Mixer and LNA.
46	CXIF	External Capacitor for Mixer V-I Converter Bias.
47	IFIN	First IF Input (to LNA).
48	VDDI	Positive Power Supply for LNA and Mixer.

DEFINITION OF SPECIFICATIONS/TEST METHODS

Single-Sideband Noise Figure (SSB NF)
Noise figure (NF) is defined as the degradation in SNR performance (in dB) of an IF input signal after it passes through a component or system. It can be expressed with the equation

$$Noise\ Figure = 10 \times \log(SNR_{IN} / SNR_{OUT})$$

The term SSB is applicable for heterodyne systems containing a mixer. It indicates that the desired signal spectrum resides on only one side of the LO frequency (i.e., single sideband); thus a "noiseless" mixer has a noise figure of 3 dB.

The AD9874's *SSB* noise figure is determined by the equation

$$SSB\ NF = P_{IN} - \{10 \times \log(BW)\} - 174\ dBm/Hz - SNR$$

where P_{IN} is the input power of an unmodulated carrier, BW is the noise measurement bandwidth, –174 *dBm/Hz* is the thermal noise floor at 293 K, and *SNR* is the measured signal-to-noise ratio in dB of the AD9874.

Note that P_{IN} is set to –85 dBm to minimize any degradation in measured SNR due to phase noise from the RF and LO signal generators. The IF frequency, CLK frequency, and decimation factors are selected to minimize any spurious components falling within the measurement bandwidth. Note also that a bandwidth of 10 kHz is used for the data sheet specification. Refer to Figures 22a and 22b for an indication of how NF varies with BW. Also, refer to the TPCs to see how NF is affected by different operating conditions. All references to noise figures within this data sheet imply single-sideband noise figure.

Input Third Order Intercept (IIP3)
IIP3 is a figure of merit used to determine a component's or system's susceptibility to intermodulation distortion (IMD) from its third order nonlinearities. Two unmodulated carriers at a specified frequency relationship (f_1 and f_2) are injected into a nonlinear system exhibiting third order nonlinearities producing IMD components at $2f_1 - f_2$ and $2f_2 - f_1$. IIP3 graphically represents the extrapolated intersection of the carrier's input power with the third order IMD component when plotted in dB. The difference in power (D in dBc) between the two carriers and the resulting third order IMD components can be determined from the equation

$$D = 2 \times (IIP3 - P_{IN})$$

Dynamic Range (DR)
Dynamic range is the measure of a small target input signal (P_{TARGET}) in the presence of a large unwanted interferer signal (P_{INTER}). Typically, the large signal will cause some unwanted characteristic of the component or system to degrade, thus making it unable to detect the smaller target signal correctly. In the case of the AD9874, it is often a degradation in noise figure at increased VGA attenuation settings that limits its dynamic range (refer to TPCs 15a, 15b, and 15c).

The test method for the AD9874 is as follows. The small target signal (an unmodulated carrier) is input at the center of the IF frequency, and its power level (P_{TARGET}) is adjusted to achieve an SNR_{TARGET} of 6 dB. The power of the signal is then increased by 3 dB prior to injecting the interferer signal. The offset frequency of the interferer signal is selected so that aliases produced by the decimation filter's response as well as phase noise from the LO (due to reciprocal mixing) do not fall back within the measurement bandwidth. For this reason, an offset of 110 kHz was selected. The interferer signal (also an unmodulated carrier) is then injected into the input and its power level is increased to the point (P_{INTER}) where the target signal SNR is reduced to 6 dB. The dynamic range is determined with the equation:

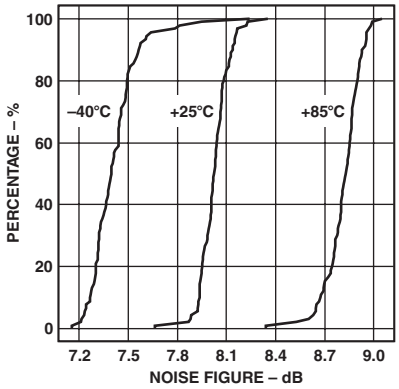
$$DR = P_{INTER} - P_{TARGET} + SNR_{TARGET}$$

Note that the AD9874's AGC is enabled for this test.

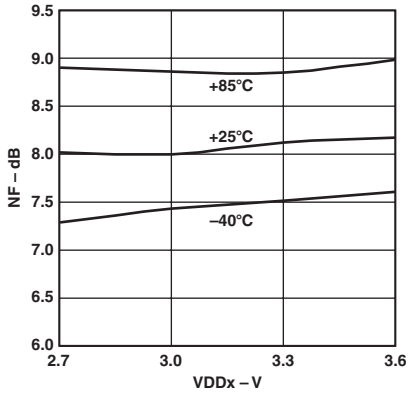
IF Input Clip Point
The IF input clip point is defined as 2 dB *below* the input power level (P_{IN}), resulting in the clipping of the AD9874's ADC. Unlike other linear components that typically exhibit a soft compression (characterized by its 1 dB compression point), an ADC exhibits a hard compression once its input signal exceeds its rated maximum input signal range. In the case of the AD9874, which contains a Σ-Δ ADC, hard compression should be avoided because it causes severe SNR degradation.

AD9874–Typical Performance Characteristics

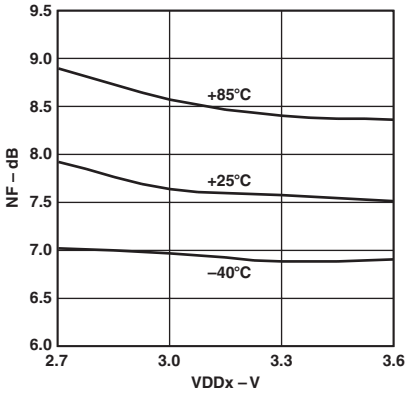
(VDDI = VDDF = VDDA = VDDC = VDDL = VDDD = VDDH = VDDx, VDDQ = VDDP = 5.0 V, f_{CLK} = 18 MSPS, f_{IF} = 109.56 MHz, f_{LO} = 107.4 MHz, T_A = 25°C, LO = –5 dBm, LO and CLK Synthesizer Disabled, 16-Bit Data with AGC and DVGA enabled, unless otherwise noted.)[1]



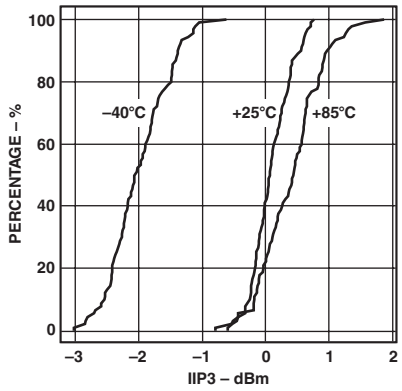
TPC 1a. CDF of SSB Noise Figure (VDDx = 3.0 V, High Bias[2])



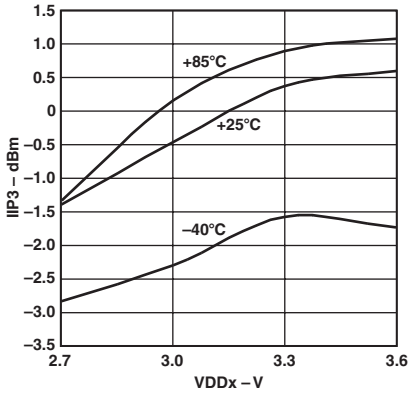
TPC 1b. SSB Noise Figure vs. Supply (High Bias[2])



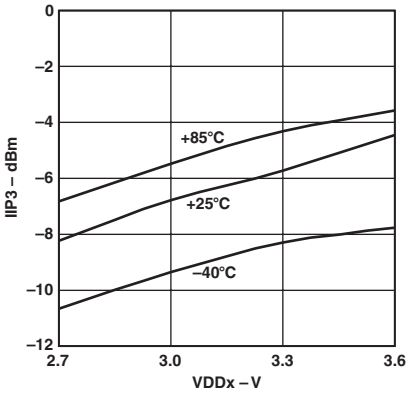
TPC 1c. SSB Noise Figure vs. Supply (Low Bias[3])



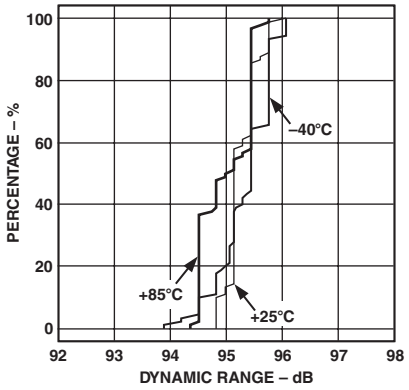
TPC 2a. CDF of IIP3 (VDDx = 3.0 V, High Bias[2])



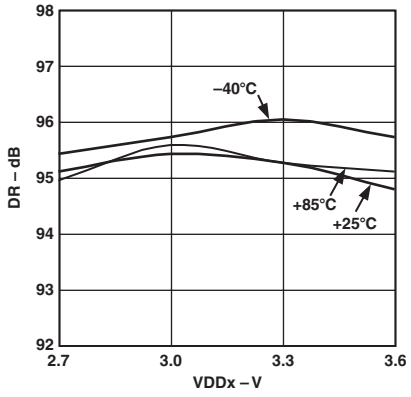
TPC 2b. IIP3 vs. Supply (High Bias[2])



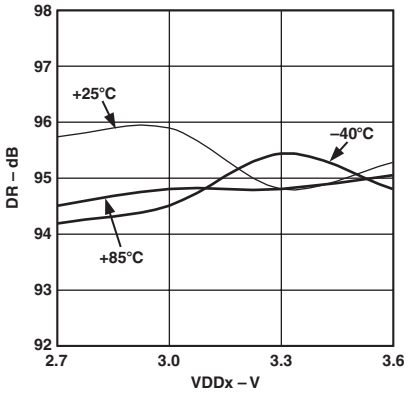
TPC 2c. IIP3 vs. Supply (Low Bias[3])



TPC 3a. CDF of Dynamic Range (VDDx = 3.0 V, High Bias[2])



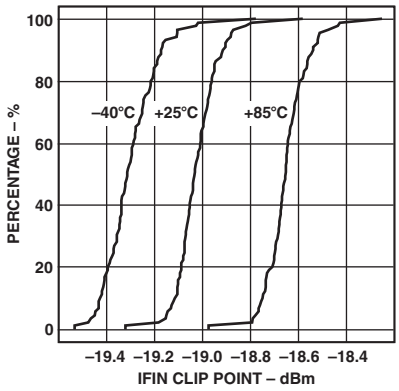
TPC 3b. Dynamic Range vs. Supply (High Bias[2])



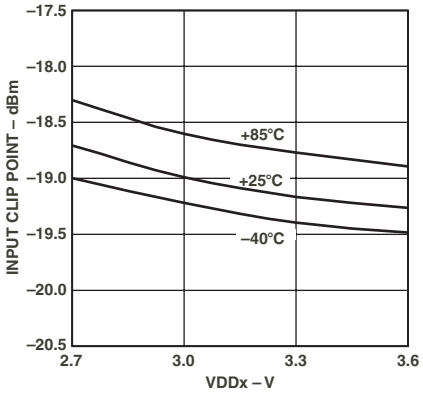
TPC 3c. Dynamic Range vs. Supply (Low Bias[3])

[1]Data taken with Toko FSLM series 10 µH inductors.
[2]High Bias corresponds to LNA_Mixer Setting of 33 in SPI Register 0x01.
[3]Low Bias corresponds to LNA_Mixer Setting of 12 in SPI Register 0x01.

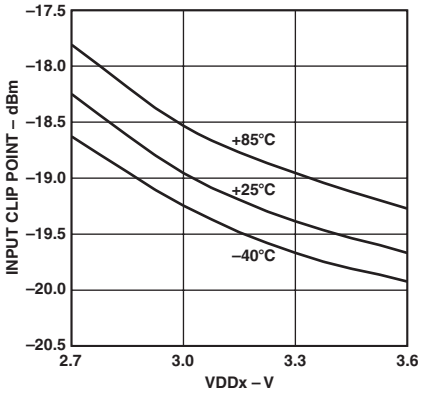
(VDDI = VDDF = VDDA = VDDC = VDDL = VDDD = VDDH = VDDx, VDDQ = VDDP = 5.0 V, f_{CLK} = 18 MSPS, f_{IF} = 109.56 MHz, f_{LO} = 107.4 MHz, T_A = 25°C, LO = –5 dBm, LO and CLK Synthesizer Disabled, 16-Bit Data with AGC and DVGA enabled, unless otherwise noted.)[1]



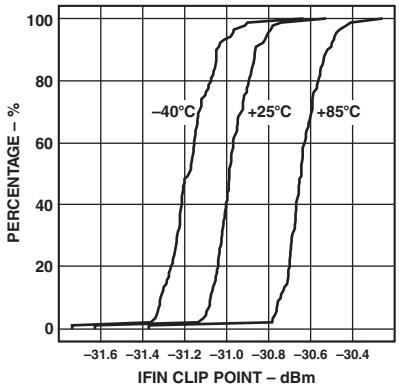
TPC 4a. CDF of Maximum VGA Attenuation Clip Point (VDDx = 3.0 V, High Bias[2])



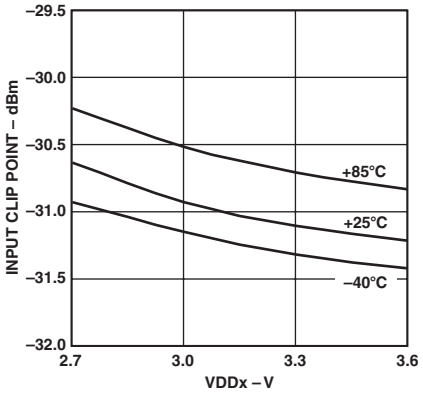
TPC 4b. Maximum VGA Attenuation Clip Point vs. Supply (High Bias[2])



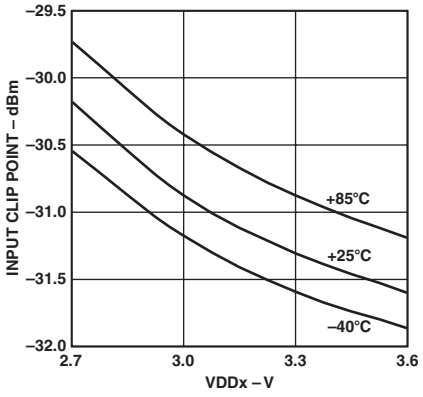
TPC 4c. Maximum VGA Attenuation Clip Point vs. Supply (Low Bias[3])



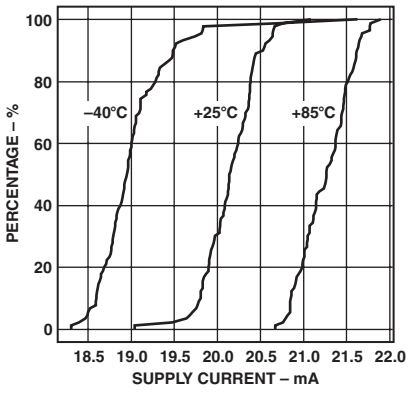
TPC 5a. CDF of Minimum VGA Attenuation Clip Point (VDDx = 3.0 V, High Bias[2])



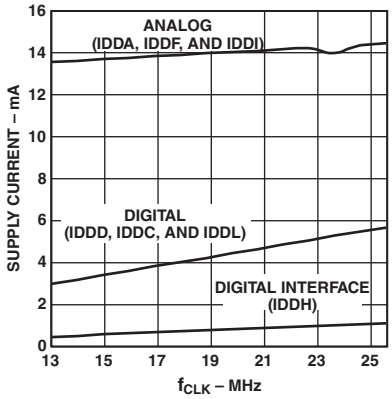
TPC 5b. Minimium VGA Attenuation Clip Point vs. Supply (High Bias[2])



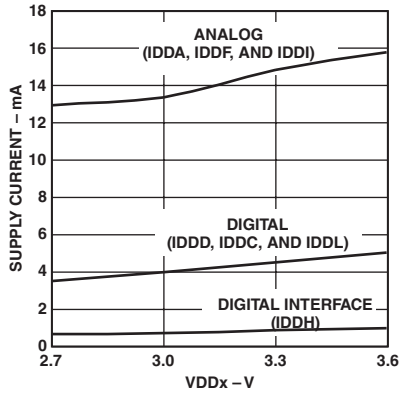
TPC 5c. Minimium VGA Attenuation Clip Point vs. Supply (Low Bias[3])



TPC 6a. CDF of Supply Current (VDDx = 3.0 V, High Bias[2])



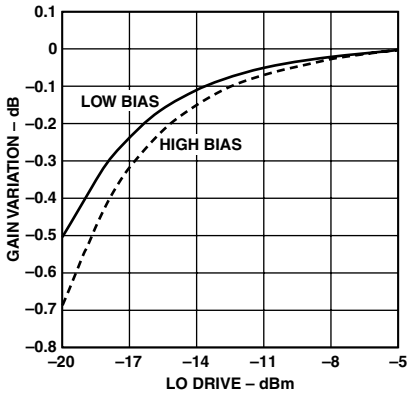
TPC 6b. Supply Current vs. f_{CLK} (VDDx = 3.0 V, High Bias[2])



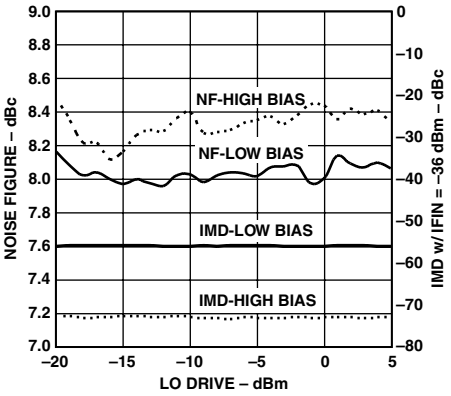
TPC 6c. Supply Current vs. Supply (High Bias[2])

[1]Data taken with Toko FSLM series 10 µH inductors.
[2]High Bias corresponds to LNA_Mixer Setting of 33 in SPI Register 0x01.
[3]Low Bias corresponds to LNA_Mixer Setting of 12 in SPI Register 0x01.

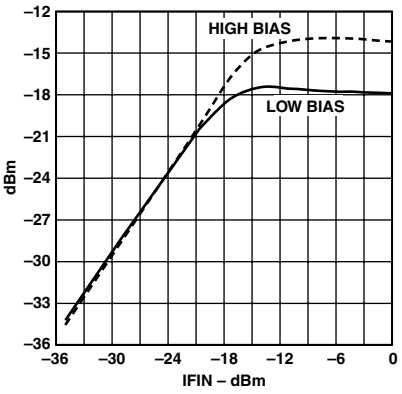
(VDDI = VDDF = VDDA = VDDC = VDDL = VDDD = VDDH = VDDx, VDDQ = VDDP = 5.0 V, f_{CLK} = 18 MSPS, f_{IF} = 109.56 MHz, f_{LO} = 107.4 MHz, T_A = 25°C, LO = –5 dBm, LO and CLK Synthesizer Disabled, 16-Bit Data with AGC and DVGA enabled, unless otherwise noted.)[1]



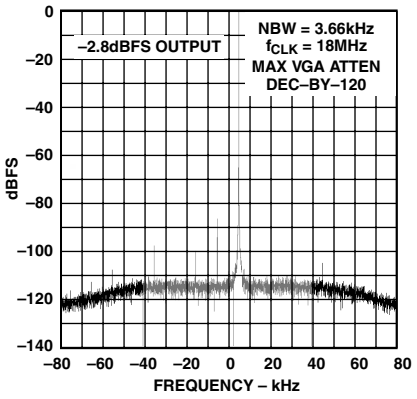
TPC 7a. Normalized Gain Variation vs. LO Drive (VDDx = 3.0 V)



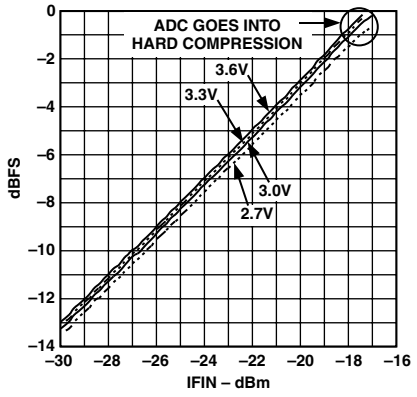
TPC 7b. Noise Figure and IMD vs. LO Drive (VDDx = 3.0 V)



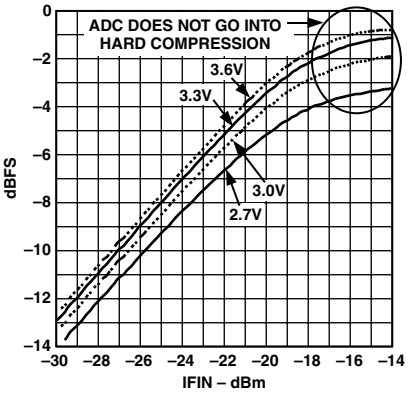
TPC 7c. Gain Compression vs. IFIN with 16 dB LNA Attenuator Enabled



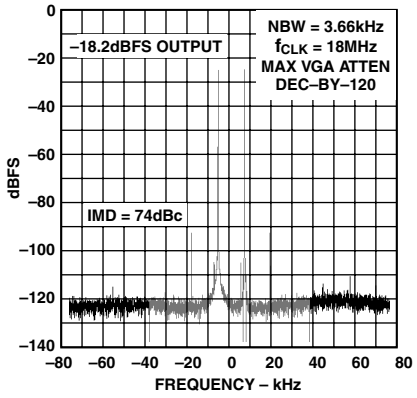
TPC 8a. Complex FFT of Baseband I/Q for Single-Tone (High Bias)



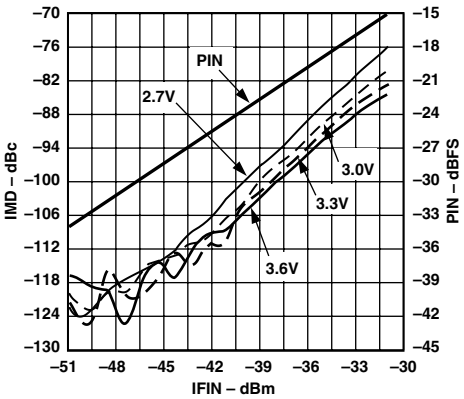
TPC 8b. Gain Compression vs. IFIN (High Bias[2])



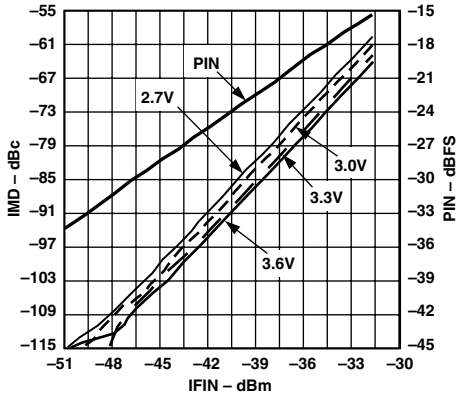
TPC 8c. Gain Compression vs. IFIN (Low Bias[3])



TPC 9a. Complex FFT of Baseband I/Q for Dual Tone IMD (High Bias with Each IFIN Tone @ –35 dBm)



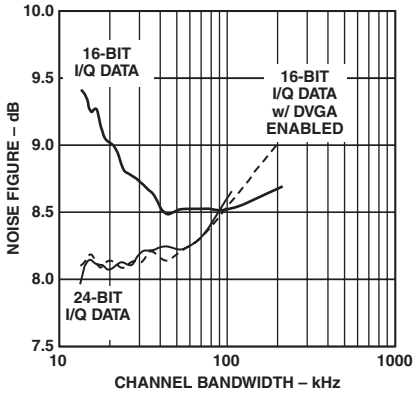
TPC 9b. IMD vs. IFIN (High Bias[2])



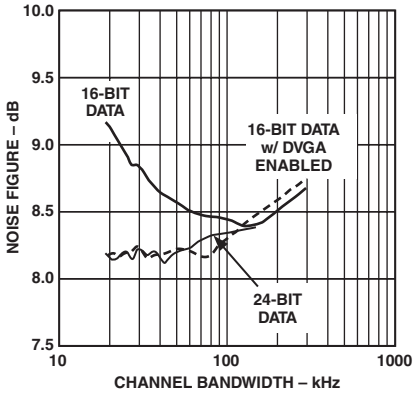
TPC 9c. IMD vs. IFIN (Low Bias[3])

[1]Data taken with Toko FSLM series 10 µH inductors.
[2]High Bias corresponds to LNA_Mixer Setting of 33 in SPI Register 0x01.
[3]Low Bias corresponds to LNA_Mixer Setting of 12 in SPI Register 0x01.

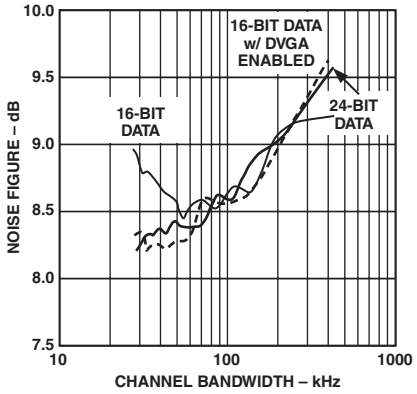
(VDDI = VDDF = VDDA = VDDC = VDDL = VDDD = VDDH = VDDx, VDDQ = VDDP = 5.0 V, f_{CLK} = 18 MSPS, f_{IF} = 109.56 MHz, f_{LO} = 107.4 MHz, T_A = 25°C, LO = –5 dBm, LO and CLK Synthesizer Disabled, 16-Bit Data with AGC and DVGA enabled, unless otherwise noted.)[1]



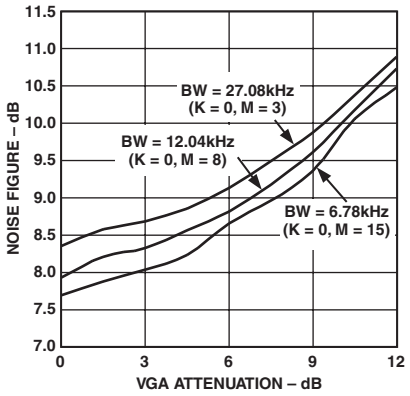
TPC 10a. Noise Figure vs. BW (Minimum Attenuation, f_{CLK} = 13 MSPS)



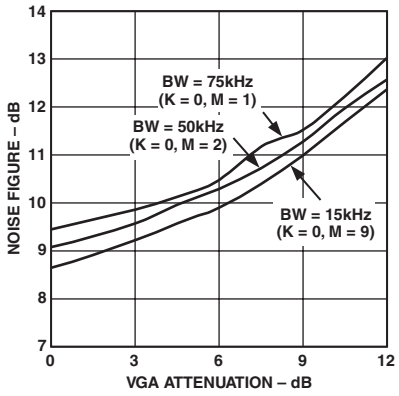
TPC 10b. Noise Figure vs. BW (Minimum Attenuation, f_{CLK} = 18 MSPS)



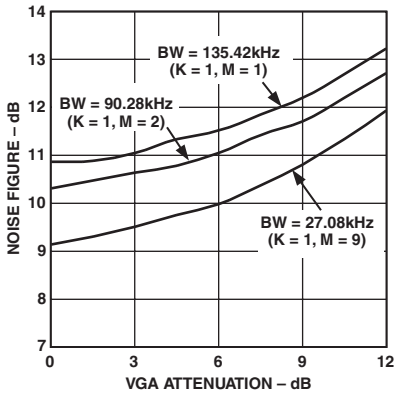
TPC 10c. Noise Figure vs. BW (Minimum Attenuation, f_{CLK} = 26 MSPS)



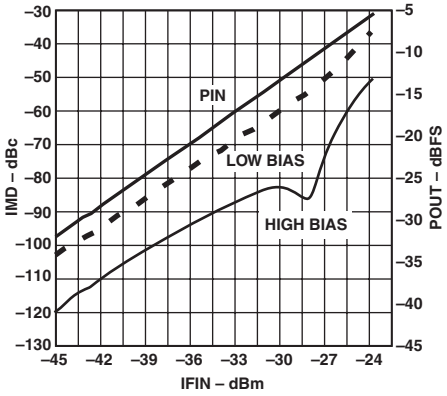
TPC 11a. Noise Figure vs. VGA Attenuation (f_{CLK} = 13 MSPS)



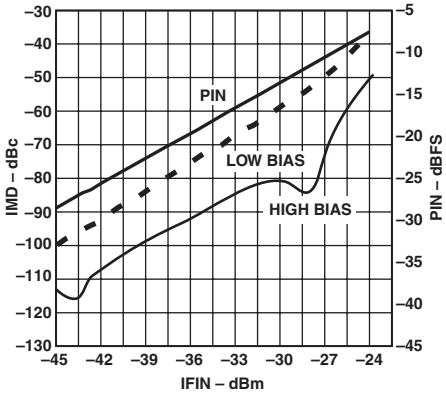
TPC 11b. Noise Figure vs. VGA Attenuation (f_{CLK} = 18 MSPS)



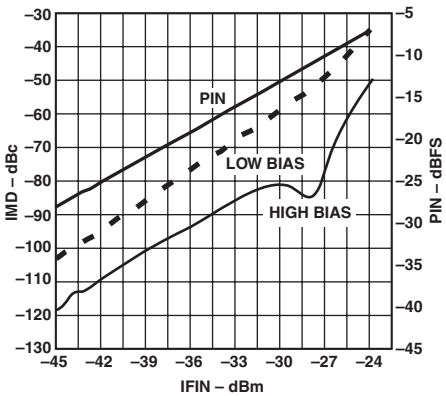
TPC 11c. Noise Figure vs. VGA Attenuation (f_{CLK} = 26 MSPS)



TPC 12a. IMD vs. IFIN (f_{CLK} = 13 MSPS)



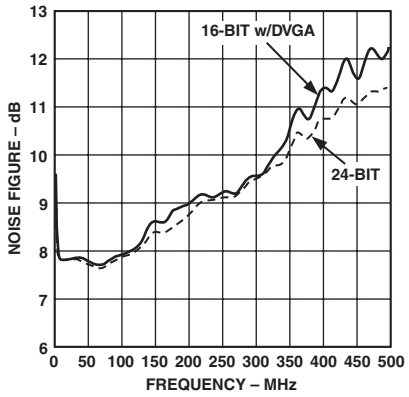
TPC 12b. IMD vs. IFIN (f_{CLK} = 18 MSPS)



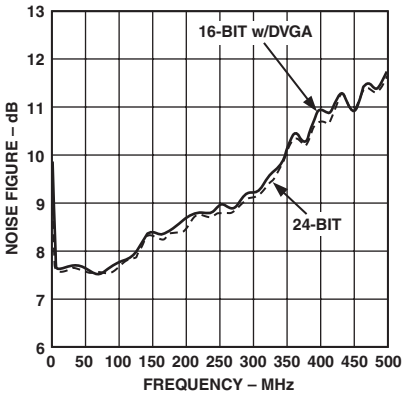
TPC 12c. IMD vs. IFIN (f_{CLK} = 26 MSPS)

[1]Data taken with Toko FSLM series 10 µH inductors.
[2]High Bias corresponds to LNA_Mixer Setting of 33 in SPI Register 0x01.
[3]Low Bias corresponds to LNA_Mixer Setting of 12 in SPI Register 0x01.

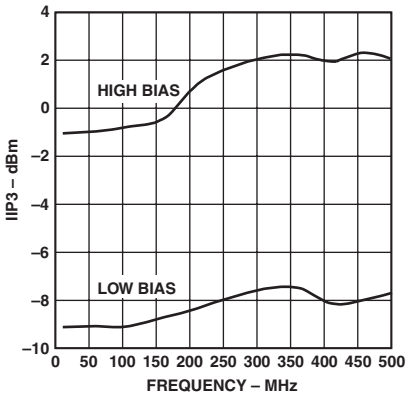
(VDDI = VDDF = VDDA = VDDC = VDDL = VDDD = VDDH = VDDx, VDDQ = VDDP = 5.0 V, f_{CLK} = 18 MSPS, f_{IF} = 109.56 MHz, f_{LO} = 107.4 MHz, T_A = 25°C, LO = –5 dBm, LO and CLK Synthesizer Disabled, 16-Bit Data with AGC and DVGA enabled, unless otherwise noted.)[1]



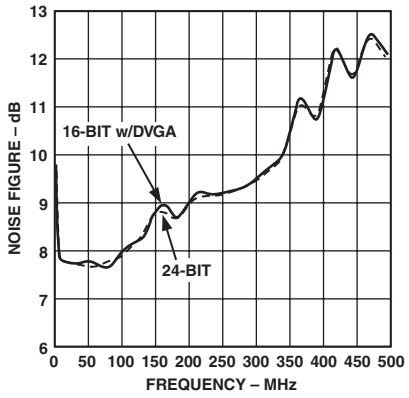
TPC 13a. Noise Figure vs. Frequency (Minimum Attenuation, f_{CLK} = 18 MSPS, BW = 10 kHz, High Bias)



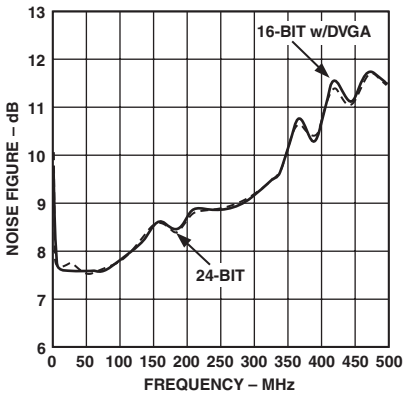
TPC 13b. Noise Figure vs. Frequency (Minimum Attenuation, f_{CLK} = 18 MSPS, BW = 10 kHz, Low Bias)



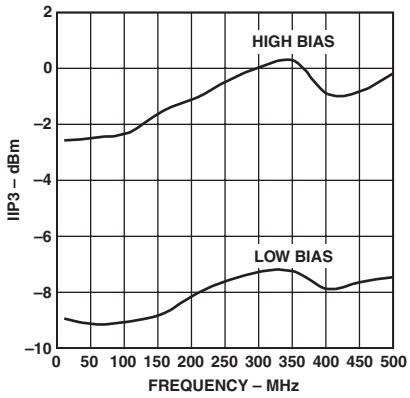
TPC 13c. Input IP3 vs. Frequency (f_{CLK} = 18 MSPS)



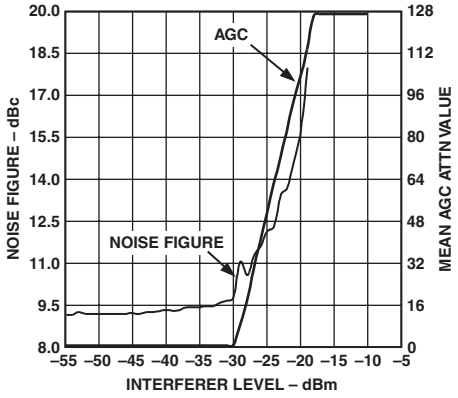
TPC 14a. Noise Figure vs. Frequency (Minimum Attenuation, f_{CLK} = 26 MSPS, BW = 24 kHz, High Bias)



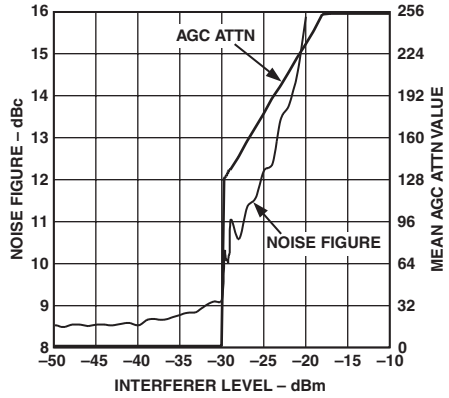
TPC 14b. Noise Figure vs. Frequency (Minimum Attenuation, f_{CLK} = 26 MSPS, BW = 24 kHz, Low Bias)



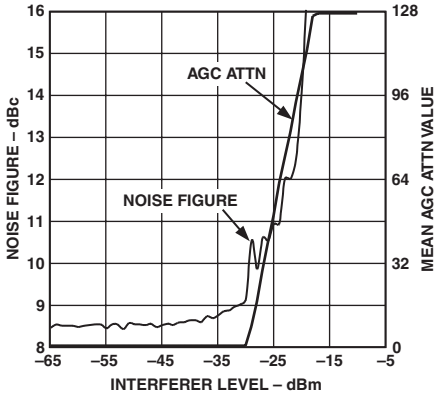
TPC 14c. Input IP3 vs. Frequency (f_{CLK} = 26 MSPS)



TPC 15a. Noise Figure vs. Interferer Level (16-Bit Data, BW = 12.5 kHz, AGCR = 1, $f_{INTERFERER}$ = f_{IF} + 110 kHz)



TPC 15b. Noise Figure vs. Interferer Level (16-Bit Data with DVGA, BW = 12.5 kHz, AGCR = 1, $f_{INTERFERER}$ = f_{IF} + 110 kHz)



TPC 15c. Noise Figure vs. Interferer Level (24-Bit Data, BW = 12.5 kHz, AGCR = 1, $f_{INTERFERER}$ = f_{IF} + 110 kHz)

[1]Data taken with Toko FSLM series 10 µH inductors.
[2]High Bias corresponds to LNA_Mixer Setting of 33 in SPI Register 0x01.
[3]Low Bias corresponds to LNA_Mixer Setting of 12 in SPI Register 0x01.

SERIAL PERIPHERAL INTERFACE (SPI)

The serial peripheral interface (SPI) is a bidirectional serial port. It is used to load configuration information into the registers listed below as well as to read back their contents. Table I provides a list of the registers that may be programmed through the SPI port. Addresses and default values are given in hexadecimal form.

Table I. SPI Address Map

Address (Hex)	Bit Breakdown	Width	Default Value	Name	Description
POWER CONTROL REGISTERS					
0x00	(7:0)	8	0xFF	STBY	Standby Control Bits (REF, LO, CKO, CK, GC, LNAMX, Unused, and ADC).
0x01	(7:6) (5:4) (3:2) (1:0)	2 2 2 2	0 0 0 0	LNAB MIXB CKOB ADCB	LNA Bias Current (0 = 0.5 mA, 1 = 1 mA, 2 = 2 mA, 3 = 3 mA). Mixer Bias Current (0 = 0.5 mA, 1 = 1.5 mA, 2 = 2.7 mA, 3 = 4 mA). CK Oscillator Bias (0 = 0.25 mA, 1 = 0.35 mA, 2 = 0.40 mA, 3 = 0.65 mA). Do not use.
0x02	(7:0)	8	0x00	TEST	Factory Test Mode. Do not use.
AGC					
0x03	(7) (6:0)	1 7	0 0x00	ATTEN AGCG(14:8)	Apply 16 dB attenuation in the front end. AGC Attenuation Setting (7 MSB of a 15-Bit Unsigned Word).
0x04	(7:0)	8	0x00	AGCG(7:0)	AGC Attenuation Setting (8 LSB of a 15-Bit Unsigned Word). Default corresponds to maximum gain.
0x05	(7:4) (3:0)	4 4	0 0	AGCA AGCD	AGC Attack Bandwidth Setting. Default yields 50 Hz raw loop bandwidth. AGC Decay Time Setting. Default is decay time = attack time.
0x06	(7) (6:4) (3) (2:0)	1 3 1 3	0 0 0 0	AGCV AGCO AGCF AGCR	Enable digital VGA to increase AGC range by 12 dB. AGC Overload Update Setting. Default is slowest update. Fast AGC (Minimizes resistance seen between GCP and GCN). AGC Enable/Reference Level (Disabled, 3 dB, 6 dB, 9 dB, 12 dB, 15 dB below Clip).
DECIMATION FACTOR					
0x07	(7:5) (4) (3:0)	3 1 4	 0 4	Unused K M	 Decimation Factor = 60 × (M + 1), if K = 0; 48 × (M + 1), if K = 1. Default is Decimate-by-300.
LO SYNTHESIZER					
0x08	(5:0)	6	0x00	LOR(13:8)	Reference Frequency Divisor (6 MSB of a 14-Bit Word).
0x09	(7:0)	8	0x38	LOR(7:0)	Reference Frequency Divisor (8 LSB of a 14-Bit Word). Default (56) yields 300 kHz from f_{REF} = 16.8 MHz.
0x0A	(7:5) (4:0)	3 5	0x5 0x00	LOA LOB(12:8)	"A" Counter (Prescaler Control Counter). "B" Counter MSB (5 MSB of a 13-Bit Word). Default LOA and LOB values yield 300 kHz from 73.35 MHz to 2.25 MHz.
0x0B	(7:0)	8	0x1D	LOB(7:0)	"B" Counter LSB (8 LSB of a 13-Bit Word).
0x0C	(6) (5) (4:2) (1:0)	1 1 3 2	0 0 0 3	LOF LOINV LOI LOTM	Enable fast acquire. Invert charge pump (0 = source current to increase VCO frequency). Charge Pump Current in Normal Operation. I_{PUMP} = (LOI + 1) × 0.625 mA. Manual Control of LO Charge Pump (0 = Off, 1 = Up, 2 = Down, 3 = Normal).
0x0D	(5:0)	4	0x0	LOFA(13:8)	LO Fast Acquire Time Unit (6 MSB of a 14-Bit Word).
0x0E	(7:0)	8	0x04	LOFA(7:0)	LO Fast Acquire Time Unit (8 LSB of a 14-Bit Word).

Table I. SPI Address Map (continued)

Address (Hex)	Bit Breakdown	Width	Default Value	Name	Description
CLOCK SYNTHESIZER					
0x10	(5:0)	6	00	CKR(13:8)	Reference Frequency Divisor (6 MSB of a 14-Bit Word).
0x11	(7:0)	8	0x38	CKR(7:0)	Reference Frequency Divisor (8 LSB of a 14-Bit Word). Default yields 300 kHz from f_{REF} =16.8 MHz; Min = 3, Max = 16383.
0x12	(4:0)	5	0x00	CKN(12:8)	Synthesized Frequency Divisor (5 MSB of a 13-Bit Word).
0x13	(7:0)	8	0x3C	CKN(7:0)	Synthesized Frequency Divisor (8 LSB of a 13-Bit Word). Default yields 300 kHz from f_{CLK} = 18 MHz; Min = 3, Max = 8191.
0x14	(6) (5) (4:2) (1:0)	1 1 3 2	0 0 0 3	CKF CKINV CKI CKTM	Enable fast acquire. Invert charge pump (0 = source current to increase VCO frequency). Charge Pump Current in Normal Operation. I_{PUMP} = (CKI + 1) × 0.625 mA. Manual Control of CLK Charge Pump (0 = Off, 1 = Up, 2 = Down, 3 = Normal).
0x15	(5:0)	6	0x0	CKFA(13:8)	CK Fast Acquire Time Unit (6 MSB of a 14-Bit Word).
0x16	(7:0)	8	0x04	CKFA(7:0)	CK Fast Acquire Time Unit (8 LSB of a 14-Bit Word).
SSI CONTROL					
0x18	(7:0)	8	0x12	SSICRA	SSI Control Register A. See Table III. (Default is FS and CLKOUT three-stated.)
0x19	(7:0)	8	0x07	SSICRB	SSI Control Register B. See Table III. (16-bit data, maximum drive strength.)
0x1A	(3:0)	4	1	SSIORD	Output Rate Divisor. f_{CLKOUT} = f_{CLK}/SSIORD.
ADC TUNING					
0x1C	(1) (0)	1 1	0 0	TUNE_LC TUNE_RC	Perform tuning on the LC portion of the ADC (cleared when done). Perform tuning on the RC portion of the ADC (cleared when done).
0x1D	(2:0)	3	0	CAPL1(2:0)	Coarse Capacitance Setting for LC Tank (LSB is 25 pF, Differential).
0x1E	(5:0)	6	0x00	CAPL0(5:0)	Fine Capacitance Setting for LC Tank (LSB is 0.4 pF, Differential).
0x1F	(7:0)	8	0x00	CAPR	Capacitance Setting for RC Resonator (64 LSB of Fixed Capacitance).
TEST REGISTERS AND SPI PORT READ ENABLE					
0x37–0x39	(7:0)	8	0x00	TEST	Factory Test Mode. Do not use.
0x3A	(7:4, 2:0) (3)	7 1	0x0 0	TEST SPIREN	Factory Test Mode. Do not use. Enable read from SPI port.
0x3B	(7:4, 2:0) (3)	7 1	0x0 0	TEST TRI	Factory Test Mode. Do not use. Three-state DOUTB.
0x3C–0x3E	(7:0)	1	0x00	TEST	Factory Test Mode. Do not use.
0x3F	(7:0)	8	Subject to Change	ID	Revision ID (Read-Only); A write of 0x99 to this register is equivalent to a power-on reset.

SERIAL PORT INTERFACE (SPI)

The serial port of the AD9874 has 3-wire or 4-wire SPI capability, allowing read/write access to all registers that configure the device's internal parameters. The default 3-wire serial communication port consists of a clock (PC), peripheral enable (PE), and bidirectional data (PD) signal. The inputs to PC, PE, and PD contain a Schmitt trigger with a nominal hysteresis of 0.4 V centered about the digital interface supply (i.e., VDDH/2).

A 4-wire SPI interface can be enabled by setting the MSB of the SSICRB register (Reg. 0x19, Bit 7), resulting in the output data also appearing on the DOUTB pin. Note that since the default power-up state sets DOUTB low, bus contention is possible for systems sharing the SPI output line. To avoid any bus contention, the DOUTB pin can be three-stated by setting the fourth control bit in the three-state bit (Reg 0x3B, Bit 3). This bit can then be toggled to gain access to the shared SPI output line.

An 8-bit instruction header must accompany each read and write SPI operation. Only the write operation supports an auto-increment mode, allowing the entire chip to be configured in a single write operation. The instruction header is shown in Table II. It includes a read/not-write indicator bit, six address bits, and a don't care bit. The data bits immediately follow the instruction header for both read and write operations. Note that the address and data are always given MSB first.

Table II. Instruction Header Information

MSB							LSB
I7	I6	I5	I4	I3	I2	I1	I0
R/W	A5	A4	A3	A2	A1	A0	X

Figure 1a illustrates the timing requirements for a write operation to the SPI port. After the peripheral enable (PE) signal goes low, data (PD) pertaining to the instruction header is read on the rising edges of the clock (PC). To initiate a write operation, the read/not-write bit is set low. After the instruction header is read, the eight data bits pertaining to the specified register are shifted into the data pin (PD) on the rising edge of the next eight clock cycles. PE stays low during the operation and goes high at the end of the transfer. If PE rises before the eight clock cycles have passed, the operation is aborted.

If PE stays low for an additional eight clock cycles, the destination address is incremented and another eight bits of data are shifted in. Again, should PE rise early, the current byte is ignored. By using this implicit addressing mode, the entire chip can be configured with a single write operation. Registers identified as being subject to frequent updates, namely those associated with power control and AGC operation, have been assigned adjacent addresses to minimize the time required to update them. Note that multibyte registers are big-endian (the most significant byte has the lower address) and are updated when a write to the least significant byte occurs.

Figure 1b illustrates the timing for a read operation to the SPI port. Although the AD9874 does not require read access for proper operation, it is often useful in the product development phase or for system authentication. Note that the readback enable bit (Register 0x3A, Bit 3) must be set for a read operation with a 3-wire SPI interface. After the peripheral enable (PE) signal goes low, data (PD) pertaining to the instruction header is read on the rising edges of the clock (PC). A read operation occurs if the read/not-write indicator is set high. After the address bits of the instruction header are read, the eight data bits pertaining to the specified register are shifted out of the data pin (PD) on the falling edges of the next eight clock cycles. If the 4-wire SPI interface is enabled, the eight data bits will also appear on the DOUTB pin with the same timing relationship as those appearing at PD. After the last data bit is shifted out, the user should return PE high, causing PD to become three-stated and return to its normal status as an input pin. Since the auto increment mode is not supported for read operations, an instruction header is required for each register read operation and PE must return high before initiating the next read operation.

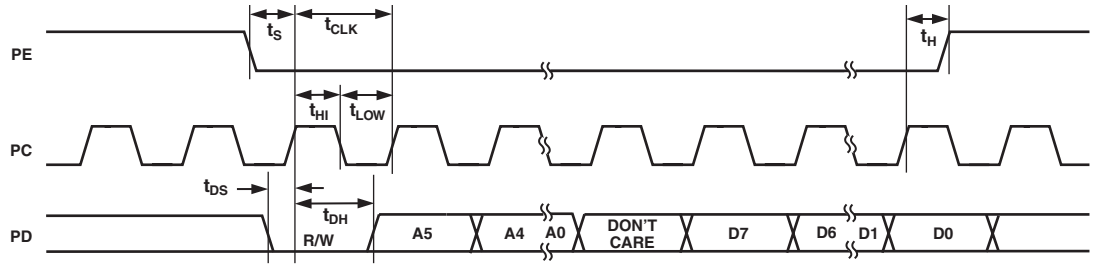


Figure 1a. SPI Write Operation Timing

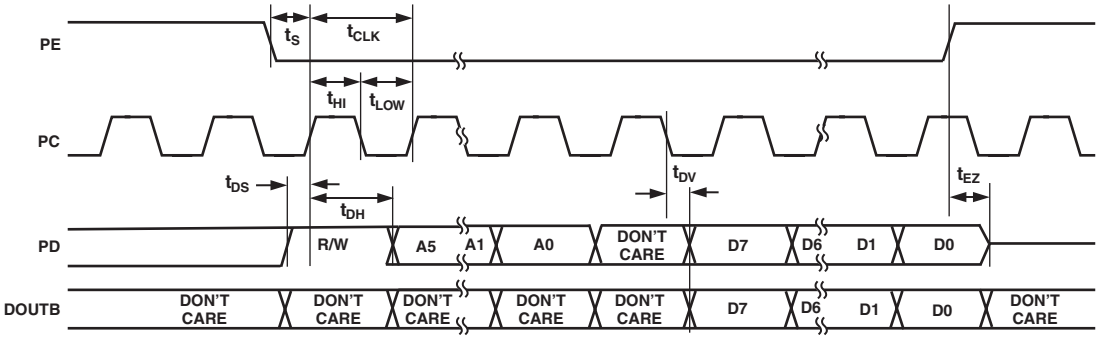


Figure 1b. SPI Read Operation Timing

SYNCHRONOUS SERIAL INTERFACE (SSI)

The AD9874 provides a high degree of programmability of its SSI output data format, control signals, and timing parameters to accommodate various digital interfaces. In a 3-wire digital interface, the AD9874 provides a frame sync signal (FS), a clock output (CLKOUT), and a serial data stream (DOUTA) signal to the host device. In a 2-wire interface, the frame sync information is embedded into the data stream, thus only CLKOUT and DOUTA output signals are provided to the host device. The SSI control registers are SSICRA, SSICRB, and SSIORD. Table III shows the different bit fields associated with these registers.

The primary output of the AD9874 is the converted I and Q demodulated signal available from the SSI port as a serial bit stream contained within a frame. The output frame rate is equal to the modulator clock frequency (f_{CLK}) divided by the digital filter's decimation factor that is programmed in the Decimator Register (0x07). The bit stream consists of an I word followed by a Q word, where each word is either 24 bits or 16 bits long and is given MSB first in twos complement form. Two optional bytes may also be included within the SSI frame following the Q word. One byte contains the AGC attenuation and the other byte contains both a count of modulator reset events and an estimate of the received signal amplitude (relative to full scale of the AD9874's ADC). Figure 2 illustrates the structure of the SSI data frames in a number of SSI modes.

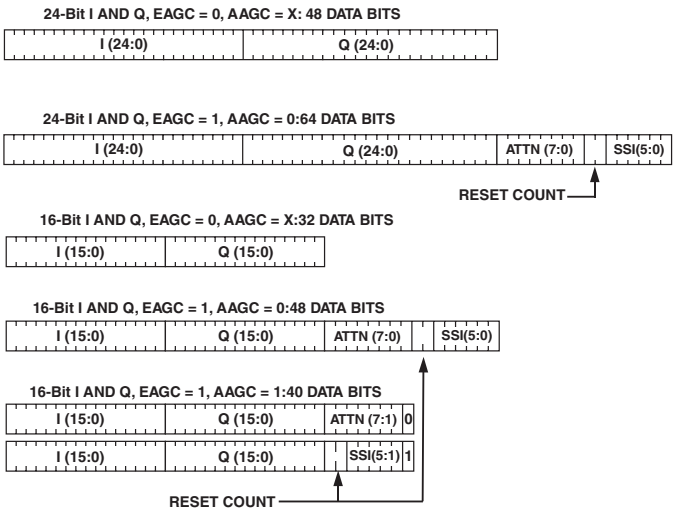


Figure 2. SSI Frame Structure

The two optional bytes are output if the EAGC bit of SSICRA is set. The first byte contains the 8-bit attenuation setting (0 = no attenuation, 255 = 24 dB of attenuation), while the second byte contains a 2-bit reset field and 6-bit received signal strength field. The reset field contains the number of modulator reset events since the last report, saturating at 3. The received signal strength (RSSI) field is a linear estimate of the signal strength at the output of the first decimation stage; 60 corresponds to a full-scale signal.

The two optional bytes follow the I and Q data as a 16-bit word provided that the AAGC bit of SSICRA is not set. If the AAGC bit is set, the two bytes follow the I and Q data in an alternating fashion. In this alternate AGC data mode, the LSB of the byte containing the AGC attenuation is a 0, while the LSB of the byte containing reset and RSSI information is always a 1.

In a 2-wire interface, the embedded frame sync bit (EFS) within the SSICRA register is set to 1. In this mode, the framing information is embedded in the data stream, with each eight bits of data surrounded by a start bit (low) and a stop bit (high), and each frame ends with at least 10 high bits. FS remains either low or three-stated (default), depending on the state of the SFST bit. Other control bits can be used to invert the frame sync (SFSI), to delay the frame sync pulse by one clock period (SLFS), to invert the clock (SCKI), or to three-state the clock (SCKT). Note that if EFS is set, SLFS is a don't care.

Table III. SSI Control Registers

Name	Width	Default	Description
SSICRA (ADDR = 0x18)			AAGC | EAGC | EFS | SFST | SFSI | SLFS | SCKT | SCKI
AAGC	1	0	Alternate AGC Data Bytes.
EAGC	1	0	Embed AGC data.
EFS	1	0	Embed frame sync.
SFST	1	1	Three-state frame sync.
SFSI	1	0	Invert frame sync.
SLFS	1	0	Late Frame Sync (1 = Late, 0 = Early).
SCKT	1	1	Three-state CLKOUT.
SCKI	1	0	Invert CLKOUT.
SSICRB (ADDR = 0x19)			4_SPI | | | | DW | DS_2 | DS_1 | DS_0
4_SPI	1	0	Enable 4-Wire SPI Interface for SPI Read operation via DOUTB.
DW	1	0	I/Q Data-Word Width (0 = 16 bit, 1 bit–24 bit). Automatically 16-bit when the AGCV = 1.
DS	3	7	FS, CLKOUT, and DOUT Drive Strength.
SSIORD (ADDR = 0x1A)			| | | | DIV_3 | DIV_2 | DIV_1 | DIV_0
DIV	4	1	Output Bit Rate Divisor $f_{CLKOUT} = f_{CLK}$/SSIORD.

The SSIORD register controls the output bit rate (f_{CLKOUT}) of the serial bit stream. f_{CLKOUT} can be set to equal the modulator clock frequency (f_{CLK}) or an integer fraction of it. It is equal to f_{CLK} divided by the contents of the SSIORD register. Note that f_{CLKOUT} should be chosen such that it does not introduce harmful spurs within the pass band of the target signal. Users must verify that the output bit rate is sufficient to accommodate the required number of bits per frame for a selected word size and decimation factor. Idle (high) bits are used to fill out each frame.

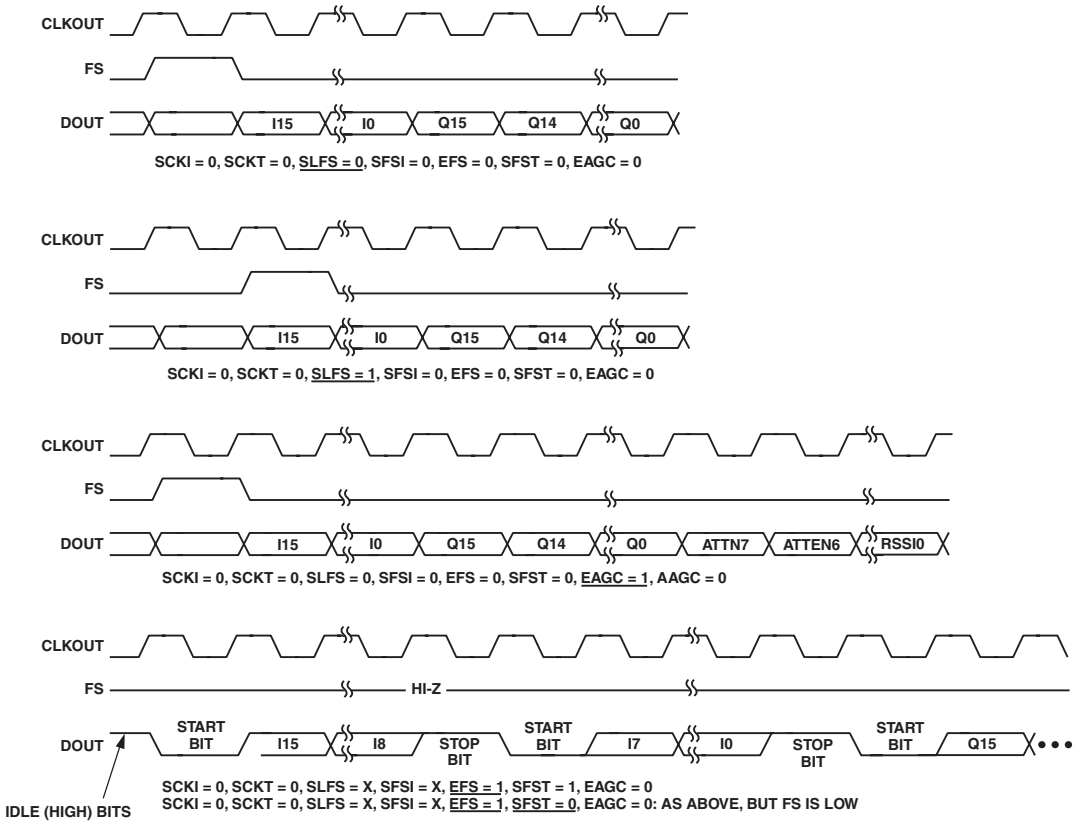


Figure 3a. SSI Timing for Several SSICRA Settings with 16-Bit I/Q Data

Table IV.
Number of Bits per Frame for Different SSICR Settings

DW	EAGC	EFS	AAGC	Number of Bits per Frame
0 (16-bit)	0	0	NA	32
	0	1	NA	49*
	1	0	0	48
	1	0	1	40
	1	1	0	69*
	1	1	1	59*
1 (24-bit)	0	0	NA	48
	0	1	NA	69*
	1	0	0	64
	1	0	1	56
	1	1	0	89*
	1	1	1	79*

*The number of bits per frame with embedded frame sync (EFS = 1) assume at least 10 idle bits are desired.

The *maximum* SSIORD setting can be determined by the equation

$$SSIORD \le TRUNC\{(Dec.Factor)/(\#\ of\ Bits\ per\ Frame)\} \quad (1)$$

where *TRUNC* is the truncated integer value.

Table IV lists the number of bits within a frame for 16-bit and 24-bit output data formats for all of the different SSICR settings. The decimation factor is determined by the contents of Register 0x07.

An example helps illustrate how the maximum SSIORD setting is determined. Suppose a user selects a decimation factor of 600 (Register 0x07, K = 0, M = 9) and prefers a 3-wire interface with a dedicated frame sync (EFS = 0) containing 24-bit data (DW = 1) with nonalternating embedded AGC data included (EAGC = 1, AAGC = 0). Referring to Table IV, each frame will consist of 64 data bits. Using Equation 1, the maximum SSIORD setting is 9 (= *TRUNC*(600/64)). Thus, the user can select any SSIORD setting between 1 and 9.

Figure 3a illustrates the output timing of the SSI port for several SSI control register settings with 16-bit I/Q data, while Figure 3b shows the associated timing parameters. Note that the same timing relationship holds for 24-bit I/Q data, with the exception that I and Q word lengths now become 24 bits. In the default mode of the operation, data is shifted out on rising edges of CLKOUT after a pulse equal to a clock period is output from the Frame Sync (FS) pin. As described above, the output data consists of a 16- or 24-bit I sample followed by a 16- or 24-bit Q sample, plus two optional bytes containing AGC and status information.

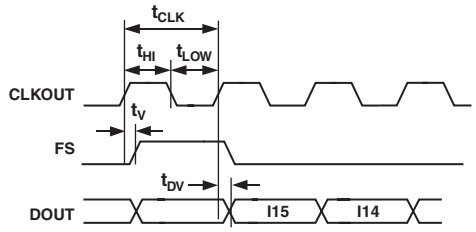


*Figure 3b. Timing Parameters for SSI Timing**

*Timing parameters also apply to inverted CLKOUT or FS modes, with t_{DV} relative to the falling edge of the CLK and/or FS.

The AD9874 also provides the means for controlling the switching characteristics of the digital output signals via the DS (drive strength) field of the SSICRB. This feature is useful in limiting switching transients and noise from the digital output that may ultimately couple back into the analog signal path, potentially degrading the AD9874's sensitivity performance. Figures 3c and 3d show how the NF can vary as a function of the SSI setting for an IF frequency of 109.65 MHz. The following two observations can be made from these figures:

- The NF becomes more sensitive to the SSI output drive strength level at higher signal bandwidth settings.
- The NF is dependent on the number of bits within an SSI frame, becoming more sensitive to the SSI output drive strength level as the number of bits is increased. As a result, one should select the lowest possible SSI drive strength setting that still meets the SSI timing requirements.

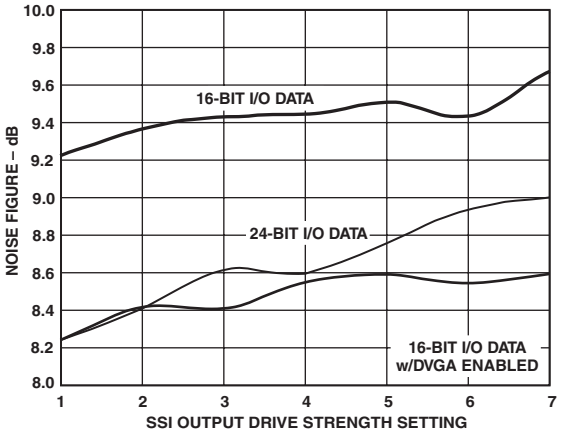


Figure 3c. NF vs. SSI Output Drive Strength (VDDx = 3.0 V, f_{CLK} = 18 MSPS, BW = 10 kHz)

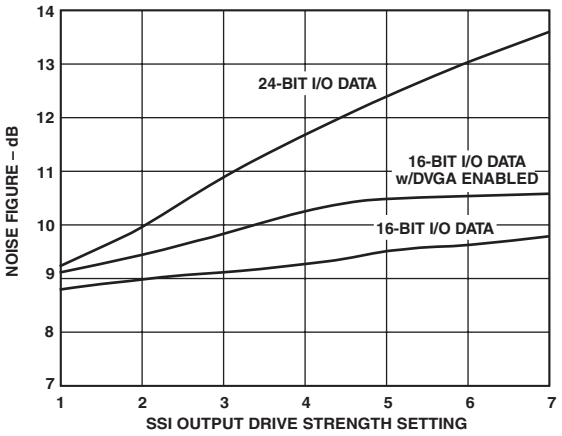


Figure 3d. NF vs. SSI Output Drive Strength (VDDx = 3.0 V, f_{CLK} = 18 MSPS, BW = 75 kHz)

Table V lists the typical output rise/fall times as a function of DS for a 10 pF load. Rise/fall times for other capacitor loads can be determined by multiplying the typical values presented in Table V by a scaling factor equal to the desired capacitive load divided by 10 pF.

Table V. Typical Rise/Fall Times (±25%) with a 10 pF Capacitive Load for Each DS Setting

DS	Typ (ns)
0	13.5
1	7.2
2	5.0
3	3.7
4	3.2
5	2.8
6	2.3
7	2.0

Synchronization Using SYNCB

Many applications require the ability to synchronize one or more AD9874 in a way that causes the output data to be precisely aligned to an external asynchronous signal. For example, receiver applications employing diversity often require synchronization of multiple AD9874 digital outputs. Satellite communication applications using TDMA methods may require synchronization between payload bursts to compensate for reference frequency drift and Doppler effects.

SYNCB can be used for this purpose. It is an active-low signal that clears the clock counters in both the decimation filter and the SSI port. The counters in the clock synthesizers are not reset because it is presumed that the CLK signals of multiple chips would be connected. SYNCB also resets the modulator, resulting in a large-scale impulse that must propagate through the AD9874's digital filter and SSI data formatting circuitry before recovering valid output data. At a result, data samples unaffected by this SYNCB induced impulse can be recovered 12 output data samples after SYNCB goes high (independent of the decimation factor).

Figure 4a shows the timing relationship between SYNCB and the SSI port's CLKOUT and FS signals. SYNCB is an asynchronous active-low signal that must remain low for at least half an input clock period (i.e., $1/(2 \times f_{CLK})$). CLKOUT remains high while FS remains low upon SYNCB going low. CLKOUT will become active within one to two output clock periods upon SYNCB returning high. FS will reappear several output cycles later, depending on the digital filter's decimation factor and the SSIORD setting. Note that for any decimation factor and SSIORD setting, this delay is fixed and repeatable. To verify proper synchronization, the FS signals of the multiple AD9874 devices should be monitored.

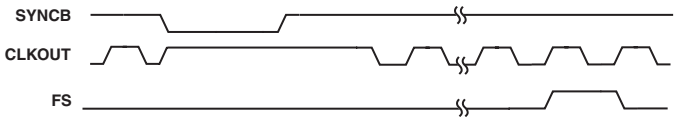


Figure 4a. SYNCB Timing

Interfacing to DSPs

The AD9874 connects directly to an Analog Devices programmable digital signal processor (DSP). Figure 4b illustrates an example with the Blackfin® series of ADSP-2153x processors. The Blackfin DSP series is a family of 16-bit products optimized for telecommunications applications with its dynamic power management feature, making it well suited for portable radio products. The code compatible family members share the fundamental core attributes of high performance, low power consumption, and the ease-of-use advantages of a microcontroller instruction set.

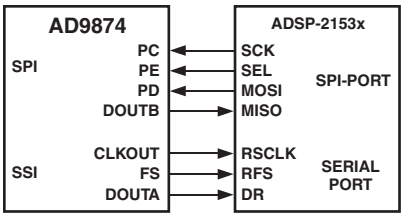


Figure 4b. Example of AD9874 and ADSP-2153x Interface

As shown in Figure 4b, AD9874's synchronous serial interface (SSI) links the receive data stream to the DSP's Serial Port (SPORT). For AD9874 setup and register programming, the device connects directly to ADSP-2153x's SPI port. Dedicated select lines (SEL) allow the ADSP-2153x to program and read back registers of multiple devices using only one SPI port. The DSP driver code pertaining to this interface is available on the AD9874 web page (http://www.analog.com/Analog_Root/static/techSupport/designTools/evaluationBoards/ad9874blackfinInterfacing.html).

POWER CONTROL

To allow power consumption to be minimized, the AD9874 possesses numerous SPI programmable power-down and bias control bits. The AD9874 powers up with all of its functional blocks placed into a standby state (i.e., STBY register default is 0xFF). Each major block may then be powered up by writing a 0 to the appropriate bit of the STBY register. This scheme provides the greatest flexibility for configuring the IC to a specific application as well as for tailoring the IC's power-down and wake-up characteristics. Table VI summarizes the function of each of the STBY bits. Note that when all the blocks are in standby, the master reference circuit is also put into standby, and thus the current is reduced by a further 0.4 mA.

Table VI. Standby Control Bits

STBY Bit	Effect	Current Reduction (mA)[1]	Wake-Up Time (ms)
7:REF	Voltage reference OFF; all biasing shut down.	0.6	<0.1 (C_{REF} = 4.7 nF)
6:LO	LO synthesizer OFF, IOUTL three-state.	1.2	Note 2
5:CKO	Clock Oscillator OFF.	1.1	Note 2
4:CK	Clock synthesizer OFF, IOUTC three-state. Clock buffer OFF if ADC is OFF.	1.3	Note 2
3:GC	Gain control DAC OFF. GCP and GCN three-state.	0.2	Depends on C_{GC}
2:LNAMX	LNA and Mixer OFF. CXVM, CXVL, and CXIF three-state.	8.2	<2.2
1:Unused			
0:ADC	ADC OFF; Clock Buffer OFF if CLK synthesizer OFF; VCM three-state; Clock to the digital filter halted; Digital outputs static.	9.2	<0.1

NOTES
[1]When all blocks are in standby, the master reference circuit is also put into standby, and thus the current is further reduced by 0.4 mA.
[2]Wake-up time is dependent on programming and/or external components.

The AD9874 also allows control over the bias current in the LNA, mixer, and clock oscillator. The effects on current consumption and system performance are described in the section dealing with the affected block.

LO SYNTHESIZER

The LO Synthesizer shown in Figure 5 is a fully programmable PLL capable of 6.25 kHz resolution at input frequencies up to 300 MHz and reference clocks of up to 25 MHz. It consists of a low noise digital phase-frequency detector (PFD), a variable output current charge pump (CP), a 14-bit reference divider, programmable A and B counters, and a dual-modulus 8/9 prescaler. The A (3-bit) and B (13-bit) counters, in conjunction with the dual 8/9 modulus prescaler, implement an N divider with N = 8 × B + A. In addition, the 14-bit reference counter (R Counter) allows selectable input reference frequencies, f_{REF}, at the PFD input. A complete PLL (phase-locked loop) can be implemented if the synthesizer is used with an external loop filter and VCO (voltage controlled oscillator).

The A, B, and R counters can be programmed via the following registers: LOA, LOB, and LOR. The charge pump output current is programmable via the LOI register from 0.625 mA to 5.0 mA using the equation

$$IPUMP = (LOI + 1) \times 0.625\ mA \quad (2)$$

An on-chip fast acquire function (enabled by the LOF bit) automatically increases the output current for faster settling during channel changes. The synthesizer may also be disabled using the LO standby bit located in the STBY register.

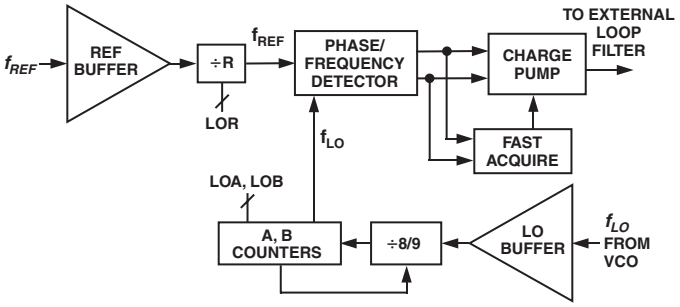


Figure 5. LO Synthesizer

The LO (and CLK) synthesizer works in the following manner. The externally supplied reference frequency, f_{REF}, is buffered and divided by the value held in the R counter. The internal f_{REF} is then compared to a divided version of the VCO frequency, f_{LO}. The phase/frequency detector provides UP and DOWN pulses whose widths vary, depending upon the difference in phase and frequency of the detector's input signals. The UP/DOWN pulses control the charge pump, making current available to charge the external low-pass loop filter when there is a discrepancy between the inputs of the PFD. The output of the low-pass filter feeds an external VCO whose output frequency, f_{LO}, is driven such that its divided down version, f_{LO}, matches that of f_{REF}, thus closing the feedback loop.

The synthesized frequency is related to the reference frequency and the LO register contents as follows:

$$f_{LO} = (8 \times LOB + LOA) / LOR \times f_{REF} \quad (3)$$

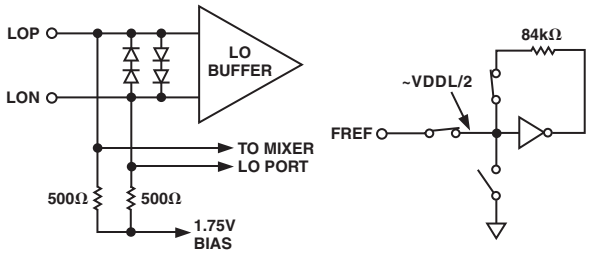
Note that the minimum allowable value in the *LOB* register is 3 and its value must always be greater than that loaded into *LOA*.

An example may help illustrate how the values of *LOA*, *LOB*, and *LOR* can be selected. Consider an application employing a 13 MHz crystal oscillator (i.e., f_{REF} = 13 MHz) with the requirement that f_{REF} = 100 kHz and f_{LO} = 143 MHz (i.e., high side injection with f_{IF} = 140.75 MHz and f_{CLK} = 18 MSPS). LOR is selected to be 130 such that f_{REF} = 100 kHz. The N-divider factor is 1430, which can be realized by selecting LOB = 178 and LOA = 6.

The stability, phase noise, spur performance, and transient response of the AD9874's LO (and CLK) synthesizers are determined by the external loop filter, the VCO, the N-divide factor, and the reference frequency, FREF. A good overview of the theory and practical implementation of PLL synthesizers (featured as a three-part series in Analog Dialogue) can be found at:

- www.analog.com/library/analogDialogue/archives/33-03/phase/index.html
- www.analog.com/library/analogDialogue/archives/33-05/phase_locked/index.html
- www.analog.com/library/analogDialogue/archives/33-07/phase3/index.html

Also, a free software copy of the Analog Devices ADIsimPLL, a PLL synthesizer simulation tool, is available at www.analog.com. Note that the ADF4112 model can be used as a close approximation to the AD9874's LO synthesizer when using this software tool.



NOTES
1. ESD DIODE STRUCTURES OMITTED FOR CLARITY.
2. FREF STBY SWITCHES SHOWN WITH LO SYNTHESIZER ON.

Figure 6. Equivalent Input of LO and REF Buffers

Figure 6 shows the equivalent input structures of the synthesizers' LO and REF buffers (excluding the ESD structures). The LO input is fed to the LO synthesizer's buffer as well as the AD9874's mixer's LO port. Both inputs are self-biasing and thus tolerate ac-coupled inputs. The LO input can be driven with a single-ended or differential signal. Single-ended dc-coupled inputs should ensure sufficient signal swing above and below the common-mode bias of the LO and REF buffers (i.e., 1.75 V and VDDL/2). Note that the f_{REF} input is slew rate dependent and must be driven with input signals exceeding 7.5 V/μs to ensure proper synthesizer operation. If this condition can not be met, an external logic gate can be inserted prior to the f_{REF} input to "square-up" the signal thus allowing a f_{REF} input frequency approching dc.

Fast Acquire Mode

The fast acquire circuit attempts to boost the output current when the phase difference between the divided-down LO (i.e., f_{LO}) and the divided-down reference frequency (i.e., f_{REF}) exceeds the threshold determined by the LOFA register. The LOFA register specifies a divisor for the f_{REF} signal that determines the period (T) of this divided-down clock. This period defines the time interval used in the fast acquire algorithm to control the charge pump current.

Assume for the moment that the nominal charge pump current is at its lowest setting (i.e., LOI = 0) and denote this minimum current by I_0. When the output pulse from the phase comparator exceeds T, the output current for the next pulse is $2I_0$. When the pulse is wider than 2T, the output current for the next pulse is $3I_0$, and so forth, up to eight times the minimum output current. If the nominal charge pump current is more than the minimum value (i.e., LOI > 0), the preceding rule is only applied if it results in an increase in the instantaneous charge pump current. If the charge pump current is set to its lowest value (LOI = 0) and the fast acquire circuit is enabled, the instantaneous charge pump current will never fall below $2I_0$ when the pulsewidth is less than T. Thus, the charge pump current when fast acquire is enabled is given by:

$$I_{PUMP-FA} = I_0 \times \{1 + \max(1, LOI, Pulsewidth/T)\} \quad (4)$$

The recommended setting for LOFA is LOR/16. Choosing a larger value for LOFA will increase T. Thus, for a given phase difference between the LO input and the f_{REF} input, the instantaneous charge pump current will be less than that available for a LOFA value of LOR/16. Similarly, a smaller value for LOFA will decrease T, making more current available for the same phase difference. In other words, a smaller value of LOFA will enable the synthesizer to settle faster in response to a frequency hop than will a large LOFA value. Care must be taken to choose a value for LOFA that is large enough (values greater than 4 recommended) to prevent the loop from oscillating back and forth in response to a frequency hop.

Table VII. SPI Registers Associated with LO Synthesizer

Address (Hex)	Bit Breakdown	Width	Default Value	Name
0x00	(7:0)	1	0xFF	STBY
0x08	(5:0)	6	0x00	LOR(13:8)
0x09	(7:0)	8	0x38	LOR(7:0)
0x0A	(7:5) (4:0)	3 5	0x5 0x00	LOA LOB(12:8)
0x0B	(7:0)	8	0x1D	LOB(7:0)
0x0C	(6) (5) (4:2) (1:0)	1 1 3 2	0 0 0 0	LOF LOINV LOI LOTM
0x0D	(3:0)	4	0x0	LOFA(13:8)
0x0E	(7:0)	8	0x04	LOFA(7:0)

CLOCK SYNTHESIZER

The clock synthesizer is a fully programmable integer-N PLL capable of 2.2 kHz resolution at clock input frequencies up to 18 MHz and reference frequencies up to 25 MHz. It is similar to the LO synthesizer described in Figure 5 with the following exceptions:

- It does not include an 8/9 prescaler nor an A counter.
- It includes a negative-resistance core that, when used in conjunction with an external LC tank and varactor, serves as the VCO.

The 14-bit reference counter and 13-bit N-divider counter can be programmed via registers *CKR* and *CKN*. The clock frequency, f_{CLK}, is related to the reference frequency by the equation

$$f_{CLK} = (CKN/CKR) \times f_{REF} \quad (5)$$

The charge pump current is programmable via the *CKI* register from 0.625 *mA* to 5.0 mA using the equation:

$$I_{PUMP} = (CKI + 1) \times 0.625\ mA \quad (6)$$

The fast acquire subcircuit of the charge pump is controlled by the CKFA register in the same manner as the LO synthesizer is controlled by the LOFA register. An on-chip lock detect function (enabled by the CKF bit) automatically increases the output current for faster settling during channel changes. The synthesizer may also be disabled using the CK standby bit located in the STBY register.

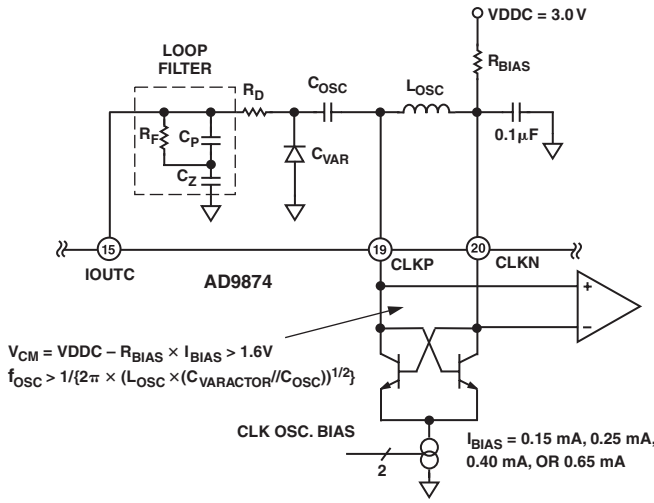


Figure 7a. External Loop Filter, Varactor, and LC Tank Are Required to Realize a Complete Clock Synthesizer

The AD9874 clock synthesizer circuitry includes a negative-resistance core so that only an external LC tank circuit with a varactor is needed to realize a voltage controlled clock oscillator (VCO). Figure 7a shows the external components required to complete the clock synthesizer along with the equivalent input circuitry of the CLK input. The resonant frequency of the VCO is approximately determined by L_{OSC} and the series equivalent capacitance of C_{OSC} and C_{VAR}. As a result, L_{OSC}, C_{OSC}, and C_{VAR} should be selected to provide a sufficient tuning range to ensure proper locking of the clock synthesizer.

The bias, I_{BIAS}, of the negative-resistance core has four programmable settings. Lower equivalent Q of the LC tank circuit may require a higher bias setting of the negative-resistance core to ensure proper oscillation. R_{BIAS} should be selected so the common-mode voltage at CLKP and CLKN is approximately 1.6 V. The synthesizer may be disabled via the CK standby bit to allow the user to employ an external synthesizer and/or VCO in place of those resident on the IC. Note that if an external CLK source or VCO is used, the clock oscillator must be disabled via the CKO standby bit.

The phase noise performance of the clock synthesizer is dependent on several factors, including the CLK oscillator I_{BIAS} setting, charge pump setting, loop filter component values, and internal f_{REF} setting. Figures 7b and 7c show how the measured phase noise attributed to the clock synthesizer varies (relative to an external f_{CLK}) as a function of the I_{BIAS} setting and charge pump setting for a –31 dBm IFIN signal at 73.35 MHz with an external LO signal at 71.1 MHz. Figure 7b shows that the optimum phase noise is achieved with the highest I_{BIAS} (CKO) setting, while Figure 7c shows that the higher charge pump values provide the optimum performance for the given loop filter configuration. The AD9874 clock synthesizer and oscillator were set up to provide an f_{CLK} of 18 MHz from an external f_{REF} of 16.8 MHz. The following external component values were selected for the synthesizer: R_F = 390 Ω, R_D = 2 kΩ, C_Z = 0.68 µF, C_P = 0.1 µF, C_{OSC} = 91 pF, L_{OSC} = 1.2 µH, and C_{VAR} = Toshiba 1SV228 Varactor.

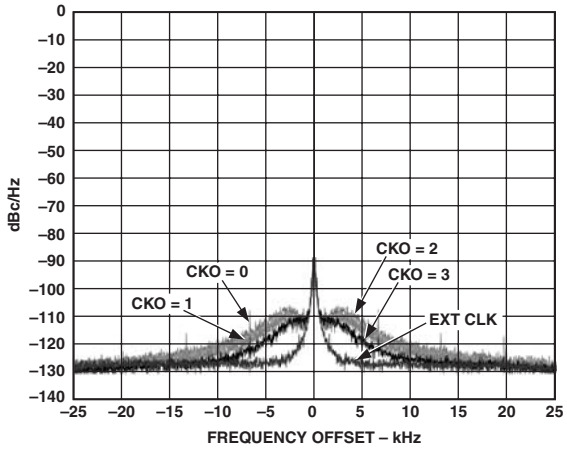


Figure 7b. CLK Phase Noise vs. I_{BIAS} Setting (CKO) (IF = 73.35 MHz, IF = 71.1 MHz, IFIN = –31 dBm, f_{CLK} = 18 MHz, f_{REF} = 16.8 MHz) (CLK SYN Settings: CKI = 7, CLR = 56, and CLN = 60 with f_{REF} = 300 kHz)

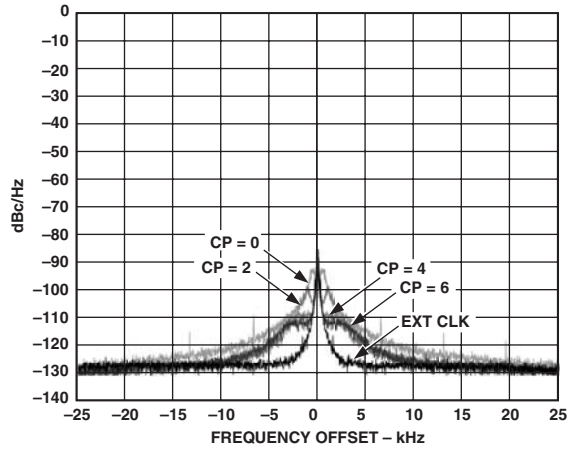


Figure 7c. CLK Phase Noise vs. Charge Pump Setting Bias (IF = 73.35 MHz, IF = 71.1 MHz, –31 dBm, f_{CLK} = 18 MHz, f_{REF} = 16.8 MHz) (CLK SYN Settings: CKO Bias = 3, CKR = 56, and CKN = 60 with f_{REF} = 300 kHz)

Table VIII. SPI Registers Associated with CLK Synthesizer

Address (Hex)	Bit Breakdown	Width	Default Value	Name
0x00	(7:0)	8	0xFF	STBY
0x01	(3:2)	2	0	CKOB
0x10	(5:0)	6	00	CKR(13:8)
0x11	(7:0)	8	0x38	CKR(7:0)
0x12	(4:0)	5	0x00	CKN(12:8)
0x13	(7:0)	8	0x3C	CKN(7:0)
0x14	(6) (5) (4:2) (1:0)	1 1 3 1	0 0 0 0	CKF CKINV CKI CKTM
0x15	(3:0)	4	0x0	CKFA(13:8)
0x16	(7:0)	8	0x04	CKFA(7:0)

IF LNA/MIXER

The AD9874 contains a single-ended LNA followed by a Gilbert-type active mixer, shown in Figure 8 with the required external components. The LNA uses negative shunt feedback to set its input impedance at the IFIN pin, thus making it dependent on the LNA bias setting and input frequency. It can be modeled as approximately 370 Ω//1.4 pF (620%) for the higher bias settings below 100 MHz. Figures 9a and 9b show the equivalent input impedance versus frequency characteristics of the AD9874 with all the LNA bias settings. The increase in shunt resistance versus frequency can be attributed to the reduction in bandwidth, thus the amount of negative feedback of the LNA. Note that the input signal into IFIN should be ac-coupled via a 10 nF capacitor since the LNA input is self-biasing.

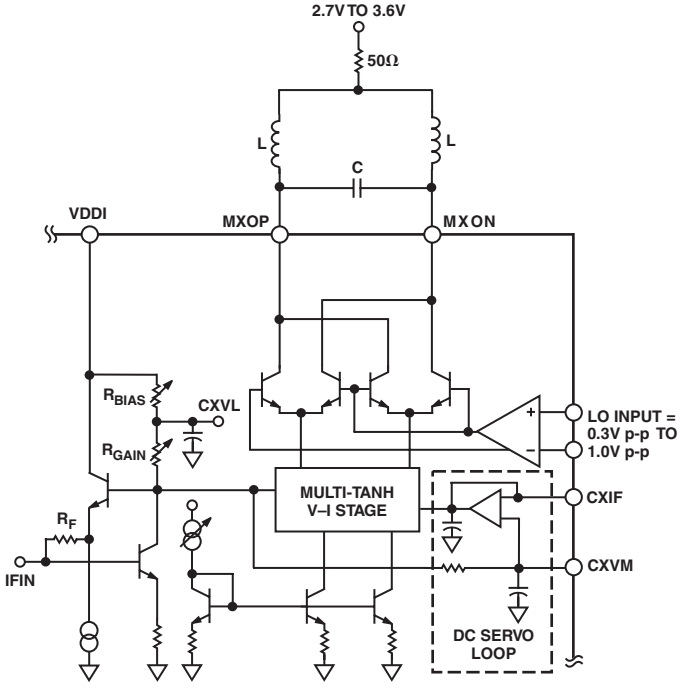


Figure 8. Simplified Schematic of AD9874's LNA/Mixer

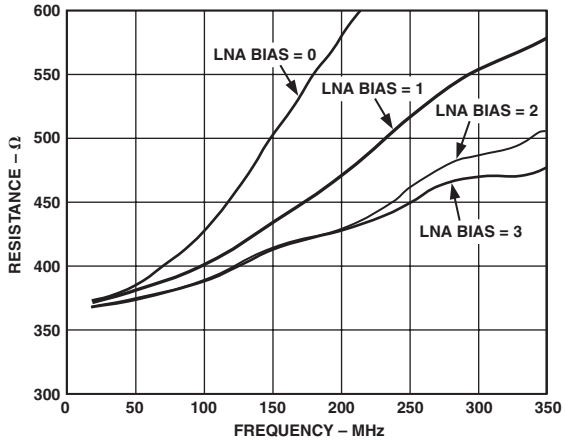


Figure 9a. The Shunt Input Resistance vs. the Frequency of the AD9874's IF1 Input

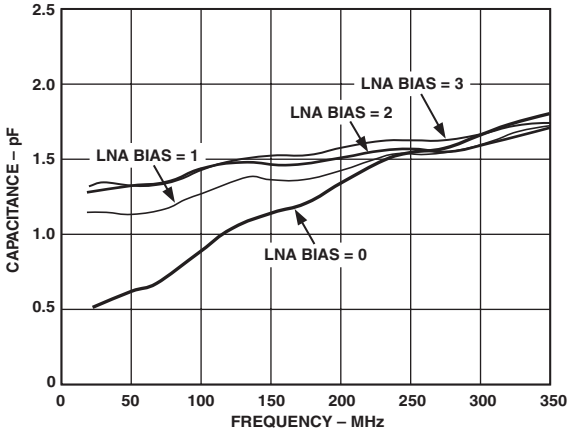


Figure 9b. The Shunt Capacitance vs. the Frequency of the AD9874's IF1 Input

The mixer's differential LO port is driven by the LO buffer stage shown in Figure 6, which can be driven single-ended or differential. Since it is self-biasing, the LO signal level can be ac-coupled and range from 0.3 V p-p to 1.0 V p-p with negligible effect on performance. The mixer's open-collector outputs, MXOP and MXON, drive an external resonant tank consisting of a differential LC network tuned to the IF of the band-pass Σ-Δ ADC (i.e., $f_{IF2\_ADC} = f_{CLK}/8$). The two inductors provide a dc bias path for the mixer core via a series resistor of 50 Ω, which is included to dampen the common-mode response. The mixer's output must be ac-coupled to the input of the band-pass Σ-Δ ADC, IF2P, and IF2N via two 100 pF capacitors to ensure proper tuning of the LC center frequency.

The external differential LC tank forms the resonant element for the first resonator of the band-pass Σ-Δ modulator, and so must be tuned to the $f_{CLK}/8$ center frequency of the modulator. The inductors should be chosen such that their impedance at $f_{CLK}/8$ is about 140 Ω (i.e., $L = 180/f_{CLK}$). An accuracy of 20% is considered to be adequate. For example, at f_{CLK} = 18 MHz, L = 10 µH is a good choice. Once the inductors have been selected, the required tank capacitance may be calculated using the relation $f_{CLK}/8 = 1/\{2 \times \pi \times (2L \times C)^{1/2}\}$.

For example, at f_{CLK} = 18 MHz and L = 10 µH, a capacitance of 250 pF is needed. However, in order to accommodate an inductor tolerance of ±10%, the tank capacitance must be adjustable from 227 pF to 278 pF. Selecting an external capacitor of 180 pF ensures that even with a 10% tolerance and stray capacitances as high as 30 pF, the total capacitance will be less than the minimum value needed by the tank. Extra capacitance is supplied by the AD9874's on-chip programmable capacitor array. Since the programming range of the capacitor array is at least 160 pF, the AD9874 has plenty of range to make up for the tolerances of low cost external components. Note that if f_{CLK} is increased by a factor of 1.44 MHz to 26 MHz so that $f_{CLK}/8$ becomes 3.25 MHz, reducing L and C by approximately the same factor (i.e., L = 6.9 µH and C = 120 pF) still satisfies the requirements stated above.

The selection of the inductors is an important consideration in realizing the full linearity performance of the AD9874. This is true when operating the LNA and mixer at maximum bias and low clock frequency. Figure 10 shows how the two-tone input-referred IMD versus the input level performance at an IF of 109 MHz and f_{CLK} of 18 MHz varies between Toko's FSLM series and Coilcraft's 1812CS series inductors. The graph also shows the extrapolated point of intersection used to determine the IIP3 performance. Note that the Coilcraft inductor provides a 7 dB to 8 dB improvement in performance and closely approximates the 3:1 slope associated with a third order linearity compared to the 2.65:1 slope associated with the Toko inductor. The Coilcraft 1008CS series showed performance similar to that of the 1812CS series. It is worth noting that the difference in IMD performance between these two inductor families with an f_{CLK} of 26 MHz is insignificant.

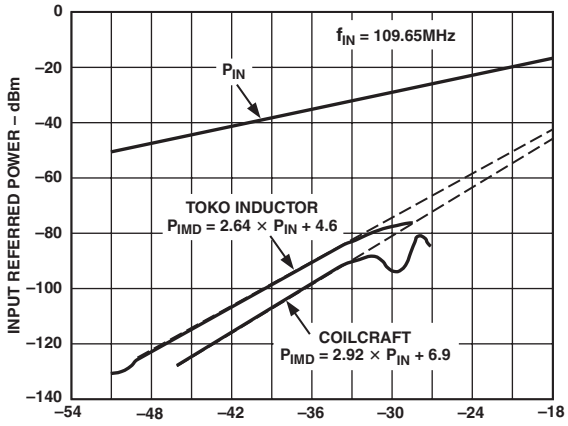


Figure 10. IMD Performance between Different Inductors with LNA and Mixer at Full Bias and f_{CLK} of 18 MHz

Both the LNA and mixer have four programmable bias settings so that current consumption can be minimized for a given application. Figures 11a, 11b, and 11c show how the LNA and mixer's noise figure (NF), linearity (IIP3), IF clip point, current consumption, and frequency response are affected for a given LNA/mixer bias setting. The measurements were taken at an IF = 73.35 MHz and LO = 71.1 MHz, with supplies set to 3 V.

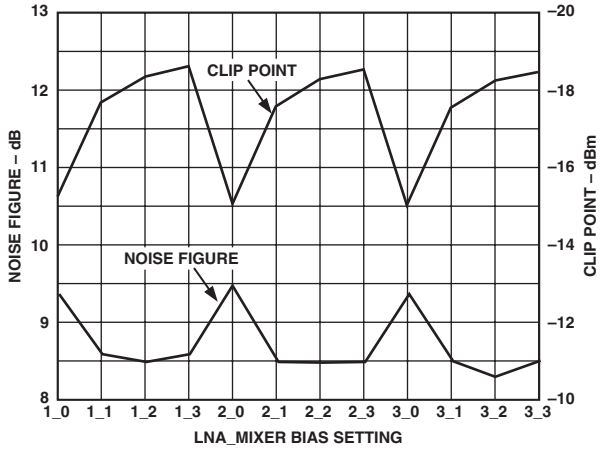


Figure 11a. LNA/Mixer Noise Figure and Conversion Gain vs. Bias Setting

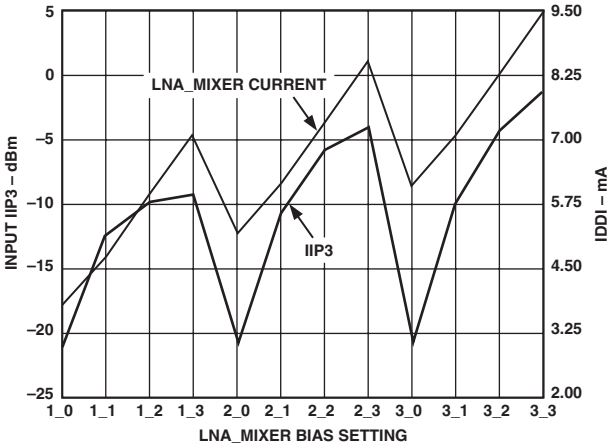


Figure 11b. LNA/Mixer IIP3 and Current Consumption vs. Bias Setting

Based on these characterization curves, a LNA/mixer bias setting of 3_3 is suitable for most applications since it will provide the greatest dynamic range in the presence of multiple unfiltered interferers. However, portable radio applications demanding the lowest possible power may benefit by changing the LNA/mixer bias setting based on the received signal strength power (i.e., RSSI) available from the SSI output data. For instance, selecting an LNA_Mixer bias setting of 1_2 for nominal input strength conditions (i.e., <–45 dBm) would result in 4 mA current savings (i.e., 18% reduction). If the signal exceeds this level, a bias setting of 3_3 could be selected. Refer to the Typical Performance Characteristics for more performance graphs characterizing the LNA and mixer's effect upon the AD9874's noise and linearity performance under different operating conditions.

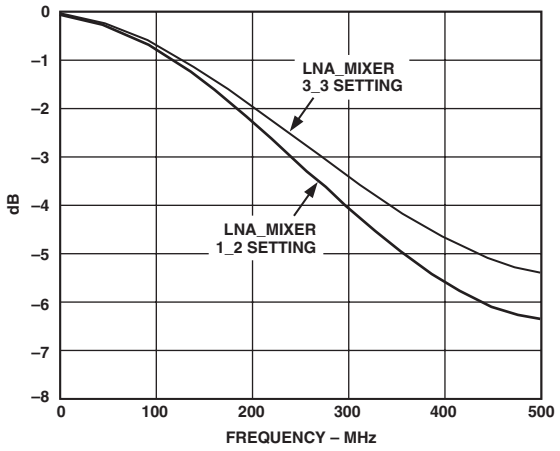


Figure 11c. LNA/Mixer Frequency Response vs. Bias Setting

A 16 dB step attenuator is also included within the LNA/mixer circuitry to prevent large signals (i.e., > –18 dBm) from overdriving the Σ-Δ modulator. In such instances, the Σ-Δ modulator will become unstable, thus severely desensitizing the receiver. The 16 dB step attenuator can be invoked by setting the ATTEN bit (Register 0x03, Bit 7), causing the mixer gain to be reduced by 16 dB. The 16 dB step attenuator could be used in applications in which a potential target or blocker signal could exceed the IF input clip point. Although the LNA will be driven into compression, it may still be possible to recover the desired signal if it is FM. Refer to TPC 7c to see the gain compression characteristics of the LNA and mixer with the 16 dB attenuator enabled.

Table IX. SPI Registers Associated with LNA/Mixer

Address (Hex)	Bit Breakdown	Width	Default Value	Name
0x00	(7:0)	8	0xFF	STBY
0x01	(7:6)	2	0	LNAB
0x01	(5:4)	2	0	MIXB
0x03	(7)	1	0	ATTEN

BAND-PASS SIGMA-DELTA (Σ-Δ) ADC

The ADC of the AD9874 is shown in Figure 12. The ADC contains a sixth order multibit band-pass Σ-Δ modulator that achieves very high instantaneous dynamic range over a narrow frequency band. The loop filter of the band-pass Σ-Δ modulator consists of two continuous-time resonators followed by a discrete-time resonator, with each resonator stage contributing a pair of complex poles. The first resonator is an external LC tank, while the second is an on-chip active RC filter. The output of the LC resonator is ac-coupled to the second resonator input via 100 pF capacitors. The center frequencies of these two continuous-time resonators must be tuned to $f_{CLK}/8$ for the ADC to function properly. The center frequency of the discrete-time resonator automatically scales with f_{CLK}, thus no tuning is required.

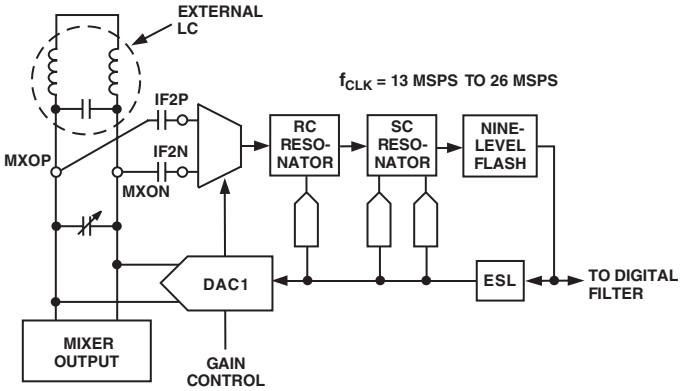


Figure 12. Equivalent Circuit of Sixth Order Band-Pass Σ-Δ Modulator

Figure 13a shows the measured power spectral density measured at the output of the undecimated band-pass Σ-Δ modulator. Note that the wide dynamic range achieved at the center frequency, $f_{CLK}/8$, is achieved once the LC and RC resonators of the Σ-Δ modulator have been successfully tuned. The out-of-band noise is removed by the decimation filters following quadrature demodulation.

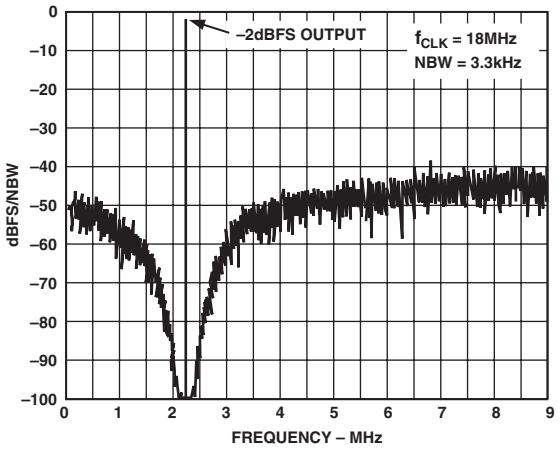


Figure 13a. Measured Undecimated Spectral Output of Σ-Δ Modulator ADC with f_{CLK} = 18 MSPS and Noise Bandwidth of 3.3 kHz