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110 MSPS/140 MSPS Analog Interface for Flat Panel Displays

AD9883A

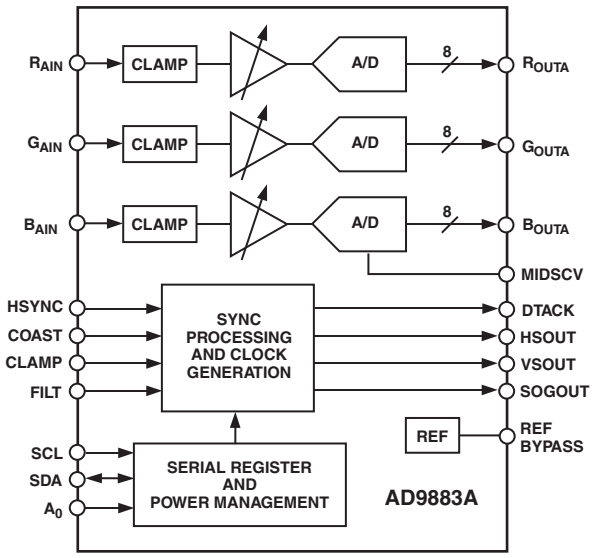
FEATURES

Industrial Temperature Range Operation
140 MSPS Maximum Conversion Rate
300 MHz Analog Bandwidth
0.5 V to 1.0 V Analog Input Range
500 ps p-p PLL Clock Jitter at 110 MSPS
3.3 V Power Supply
Full Sync Processing
Sync Detect for Hot Plugging
Midscale Clamping
Power-Down Mode
Low Power: 500 mW Typical
4:2:2 Output Format Mode

APPLICATIONS

RGB Graphics Processing
LCD Monitors and Projectors
Plasma Display Panels
Scan Converters
Microdisplays
Digital TV

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9883A is a complete 8-bit, 140 MSPS, monolithic analog interface optimized for capturing RGB graphics signals from personal computers and workstations. Its 140 MSPS encode rate capability and full power analog bandwidth of 300 MHz supports resolutions up to SXGA (1280 × 1024 at 75 Hz).

The AD9883A includes a 140 MHz triple ADC with internal 1.25 V reference, a PLL, and programmable gain, offset, and clamp control. The user provides only a 3.3 V power supply, analog input, and Hsync and COAST signals. Three-state CMOS outputs may be powered from 2.5 V to 3.3 V.

The AD9883A's on-chip PLL generates a pixel clock from the Hsync input. Pixel clock output frequencies range from 12 MHz to 140 MHz. PLL clock jitter is 500 ps p-p typical at 140 MSPS. When the COAST signal is presented, the PLL maintains its output frequency in the absence of Hsync. A sampling phase adjustment is provided. Data, Hsync, and clock output phase relationships are maintained. The AD9883A also offers full sync processing for composite sync and sync-on-green applications.

A clamp signal is generated internally or may be provided by the user through the CLAMP input pin. This interface is fully programmable via a 2-wire serial interface.

Fabricated in an advanced CMOS process, the AD9883A is provided in a space-saving 80-lead LQFP surface-mount plastic package and is specified over the –40°C to +85°C temperature range.

REV. B

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AD9883A* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

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DOCUMENTATION

Data Sheet

- AD9883A: 110 MSPS/140 MSPS Analog Interface for Flat Panel Interface Data Sheet

TOOLS AND SIMULATIONS

- AD9883 CCD PPL Settings

REFERENCE MATERIALS

Informational

- Advantiv™ Advanced TV Solutions

Technical Articles

- Analysis of Common Failures of HDMI CT

DESIGN RESOURCES

- AD9883A Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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AD9883A–SPECIFICATIONS

Analog Interface (V_D = 3.3 V, V_{DD} = 3.3 V, ADC Clock = Maximum Conversion Rate, unless otherwise noted.)

Parameter	Temp	Test Level	AD9883AKST-110 Min	AD9883AKST-110 Typ	AD9883AKST-110 Max	AD9883AKST-140 Min	AD9883AKST-140 Typ	AD9883AKST-140 Max	Unit
RESOLUTION				8			8		Bits
DC ACCURACY									
Differential Nonlinearity	25°C	I		±0.5	+1.25/–1.0		±0.5	+1.35/–1.0	LSB
	Full	VI			+1.35/–1.0			+1.45/–1.0	LSB
Integral Nonlinearity	25°C	I		±0.5	±1.85		±0.5	±2.0	LSB
	Full	VI			±2.0			±2.3	LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed		
ANALOG INPUT									
Input Voltage Range									
Minimum	Full	VI			0.5			0.5	V p-p
Maximum	Full	VI	1.0			1.0			V p-p
Gain Tempco	25°C	V		100			100		ppm/°C
Input Bias Current	25°C	IV			1			1	µA
	Full	IV			1			1	µA
Input Offset Voltage	Full	VI		7	50		7	70	mV
Input Full-Scale Matching	Full	VI		1.5	6.0		1.5	8.0	% FS
Offset Adjustment Range	Full	VI	46	49	52	46	49	52	% FS
REFERENCE OUTPUT									
Output Voltage	Full	VI	1.20	1.25	1.32	1.20	1.25	1.32	V
Temperature Coefficient	Full	V		±50			±50		ppm/°C
SWITCHING PERFORMANCE									
Maximum Conversion Rate	Full	VI	110			140			MSPS
Minimum Conversion Rate	Full	IV			10			10	MSPS
Data to Clock Skew	Full	IV	–0.5		+2.0	–0.5		+2.0	ns
t_{BUFF}	Full	VI	4.7			4.7			µs
t_{STAH}	Full	VI	4.0			4.0			µs
t_{DHO}	Full	VI	0			0			µs
t_{DAL}	Full	VI	4.7			4.7			µs
t_{DAH}	Full	VI	4.0			4.0			µs
t_{DSU}	Full	VI	250			250			ns
t_{STASU}	Full	VI	4.7			4.7			µs
t_{STOSU}	Full	VI	4.0			4.0			µs
HSYNC Input Frequency	Full	IV	15		110	15		110	kHz
Maximum PLL Clock Rate	Full	VI	110			140			MHz
Minimum PLL Clock Rate	Full	IV			12			12	MHz
PLL Jitter	25°C	IV		400	700[1]		400	700[1]	ps p-p
	Full	IV			1000[1]			1000[1]	ps p-p
Sampling Phase Tempco	Full	IV		15			15		ps/°C
DIGITAL INPUTS									
Input Voltage, High (V_{IH})	Full	VI	2.5			2.5			V
Input Voltage, Low (V_{IL})	Full	VI			0.8			0.8	V
Input Voltage, High (V_{IH})	Full	V			–1.0			–1.0	µA
Input Voltage, Low (V_{IL})	Full	V			+1.0			+1.0	µA
Input Capacitance	25°C	V		3			3		pF

Parameter	Temp	Test Level	AD9883AKST-110 Min	AD9883AKST-110 Typ	AD9883AKST-110 Max	AD9883AKST-140 Min	AD9883AKST-140 Typ	AD9883AKST-140 Max	Unit
DIGITAL OUTPUTS									
Output Voltage, High (V_{OH})	Full	VI	$V_D - 0.1$			$V_D - 0.1$			V
Output Voltage, Low (V_{OL})	Full	VI			0.1			0.1	V
Duty Cycle DATACK	Full	IV	45	50	55	45	50	55	%
Output Coding				Binary			Binary		
POWER SUPPLY									
V_D Supply Voltage	Full	IV	3.0	3.3	3.6	3.15	3.3	3.6	V
V_{DD} Supply Voltage	Full	IV	2.2	3.3	3.6	2.2	3.3	3.6	V
P_{VD} Supply Voltage	Full	IV	3.0	3.3	3.6	3.0	3.3	3.6	V
I_D Supply Current (V_D)	25°C	V		132			180		mA
I_{DD} Supply Current (V_{DD})[2]	25°C	V		19			26		mA
IP_{VD} Supply Current (P_{VD})	25°C	V		8			11		mA
Total Power Dissipation	Full	VI		525	650		650	800	mW
Power-Down Supply Current	Full	VI		5	10		5	10	mA
Power-Down Dissipation	Full	VI		16.5	33		16.5	33	mW
DYNAMIC PERFORMANCE									
Analog Bandwidth, Full Power	25°C	V		300			300		MHz
Transient Response	25°C	V		2			2		ns
Overvoltage Recovery Time	25°C	V		1.5			1.5		ns
Signal-to-Noise Ratio (SNR)	25°C	V		44			43		dB
(Without Harmonics)	Full	V		43			42		dB
f_{IN} = 40.7 MHz									
Crosstalk	Full	V		55			55		dBc
THERMAL CHARACTERISTICS									
θ_{JC} Junction-to-Case Thermal Resistance		V		16			16		°C/W
θ_{JA} Junction-to-Ambient Thermal Resistance		V		35			35		°C/W

NOTES
[1]VCO Range = 10, Charge Pump Current = 110, PLL Divider = 1693.
[2]DATACK Load = 15 pF, Data Load = 5 pF.

Specifications subject to change without notice.

Analog Interface (V_D = 3.3 V, V_{DD} = 3.3 V, ADC Clock = Maximum Conversion Rate, unless otherwise noted.)

Parameter	Temp	Test Level	AD9883ABST–110 Min	AD9883ABST–110 Typ	AD9883ABST–110 Max	AD9883ABST–140 Min	AD9883ABST–140 Typ	AD9883ABST–140 Max	Unit
RESOLUTION				8			8		Bits
DC ACCURACY									
Differential Nonlinearity	25°C	I		±0.5	+1.25/–1.0		±0.5	+1.5/–1.0	LSB
	Full	VI			+1.5/–1.0			+1.81/–1.0	LSB
Integral Nonlinearity	25°C	I		±0.5	±1.85		±0.5	±1.85	LSB
	Full	VI			±3.2			±3.2	LSB
ANALOG INPUT									
Input Voltage Range									
Minimum	Full	VI			0.5			0.5	V p-p
Maximum	Full	VI	1.0			1.0			V p-p
Gain Tempco	25°C	V		100			100		ppm/°C
Input Bias Current	25°C	IV			1			1	µA
	Full	IV			2			2	µA
Input Offset Voltage	Full	VI		7	75		7	75	mV
Input Full-Scale Matching	Full	VI		1.5	8.0		1.5	10.0	% FS
Offset Adjustment Range	Full	VI	46	49	52	46	49	52	% FS
REFERENCE OUTPUT									
Output Voltage	Full	VI	1.19	1.25	1.33	1.19	1.25	1.33	V
Temperature Coefficient	Full	V		±100			±100		ppm/°C
SWITCHING PERFORMANCE									
Maximum Conversion Rate	Full	VI	110			140			MSPS
Minimum Conversion Rate	Full	IV			10			10	MSPS
Data to Clock Skew	Full	IV	–0.5		+2.0	–0.5		+2.0	ns
t_{BUFF}	Full	VI	4.7			4.7			µs
t_{STAH}	Full	VI	4.0			4.0			µs
t_{DHO}	Full	VI	0			0			µs
t_{DAL}	Full	VI	4.7			4.7			µs
t_{DAH}	Full	VI	4.0			4.0			µs
t_{DSU}	Full	VI	250			250			µs
t_{STASU}	Full	VI	4.7			4.7			µs
t_{STOSU}	Full	VI	4.0			4.0			µs
HSYNC Input Frequency	Full	IV	15		110	15		110	kHz
Maximum PLL Clock Rate	Full	VI	110			140			MHz
Minimum PLL Clock Rate	Full	IV			12			12	MHz
PLL Jitter	25°C	IV		400	700[1]		400	700[1]	ps p-p
	Full	IV			1100[1]			1100[1]	ps p-p
Sampling Phase Tempco	Full	IV		15			15		ps/°C
DIGITAL INPUTS									
Input Voltage, High (V_{IH})	Full	VI	2.5			2.5			V
Input Voltage, Low (V_{IL})	Full	VI			0.8			0.8	V
Input Current, High (I_{IH})	Full	V			–1.0			–1.0	µA
Input Current, Low (I_{IL})	Full	V			1.0			1.0	µA
Input Capacitance	+25°C	V		3			3		pF
DIGITAL OUTPUTS									
Output Voltage, High (V_{OH})	Full	VI	V_D – 0.1			V_D – 0.1			V
Output Voltage, Low (V_{OL})	Full	VI			0.1			0.1	V
Duty Cycle, DATACK	Full	IV	45	50	55	45	50	55	%
Output Coding				Binary			Binary		

Parameter	Temp	Test Level	AD9883ABST–110 Min	AD9883ABST–110 Typ	AD9883ABST–110 Max	AD9883ABST–140 Min	AD9883ABST–140 Typ	AD9883ABST–140 Max	Unit
POWER SUPPLY									
V_D Supply Voltage	Full	IV	3.0	3.3	3.6	3.0	3.3	3.6	V
V_{DD} Supply Voltage	Full	IV	2.2	3.3	3.6	2.2	3.3	3.6	V
P_{VD} Supply Voltage	Full	IV	3.0	3.3	3.6	3.0	3.3	3.6	V
I_D Supply Current (V_D)	25°C	V		132			163		mA
I_{DD} Supply Current (V_{DD})[2]	25°C	V		19			24		mA
IP_{VD} Supply Current (P_{VD})	25°C	V		8			10		mA
Total Power Dissipation	Full	VI		525	700		650	850	mW
Power-Down Supply Current	Full	VI		5	15		5	15	mA
Power-Down Dissipation	Full	VI		16.5	33		16.5	33	mW
DYNAMIC PERFORMANCE									
Analog Bandwidth, Full Power	25°C	V		300			300		MHz
Transient Response	25°C	V		2			2		ns
Overvoltage Recovery Time	25°C	V		1.5			1.5		ns
Signal-to-Noise Ratio (SNR)	25°C	V		44			43		dB
(Without Harmonics)	Full	V		43			42		dB
f_{IN} = 40.7 MHz									
Crosstalk	Full	V		55			55		dBc
THERMAL CHARACTERISTICS									
θ_{JC} Junction-to-Case Thermal Resistance	V			16			16		°C/W
θ_{JA} Junction-to-Ambient Thermal Resistance	V			35			35		°C/W

NOTES
[1]VCO Range = 10, Charge Pump Current = 110, PLL Divider = 1693.
[2]DATACK Load = 15 pF, Data Load = 5 pF.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_D	3.6 V
V_{DD}	3.6 V
Analog Inputs	V_D to 0.0 V
VREF IN	V_D to 0.0 V
Digital Inputs	5 V to 0.0 V
Digital Output Current	20 mA
Operating Temperature	–40°C to +85°C
Storage Temperature	–65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

Test Level

I. 100% production tested.
II. 100% production tested at 25°C and sample tested at specified temperatures.
III. Sample tested only.
IV. Parameter is guaranteed by design and characterization testing.
V. Parameter is a typical value only.
VI. 100% production tested at 25°C; guaranteed by design and characterization testing.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9883AKST-140	0°C to 70°C	LQFP	ST-80
AD9883AKST-110	0°C to 70°C	LQFP	ST-80
AD9883AKSTZ-110*	0°C to 70°C	LQFP	ST-80
AD9883AKSTZ-140*	0°C to 70°C	LQFP	ST-80
AD9883ABST-110	–40°C to +85°C	LQFP	ST-80
AD9883ABST-140	–40°C to +85°C	LQFP	ST-80
AD9883ABST-RL110	–40°C to +85°C	LQFP	ST-80
AD9883ABST-RL140	–40°C to +85°C	LQFP	ST-80
AD9883A/PCB	25°C	Evaluation Board	

*Lead-free product

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9883A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

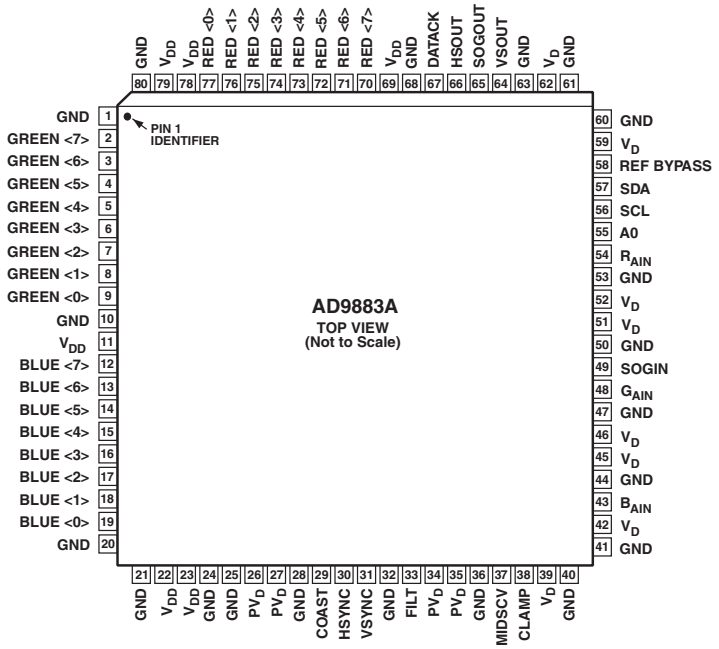

Table I. Complete Pinout List

Pin Type	Mnemonic	Function	Value	Pin No.
Inputs	R_{AIN}	Analog Input for Converter R	0.0 V to 1.0 V	54
	G_{AIN}	Analog Input for Converter G	0.0 V to 1.0 V	48
	B_{AIN}	Analog Input for Converter B	0.0 V to 1.0 V	43
	HSYNC	Horizontal SYNC Input	3.3 V CMOS	30
	VSYNC	Vertical SYNC Input	3.3 V CMOS	31
	SOGIN	Input for Sync-on-Green	0.0 V to 1.0 V	49
	CLAMP	Clamp Input (External CLAMP Signal)	3.3 V CMOS	38
	COAST	PLL COAST Signal Input	3.3 V CMOS	29
Outputs	Red [7:0]	Outputs of Converter Red, Bit 7 is the MSB	3.3 V CMOS	70–77
	Green [7:0]	Outputs of Converter Green, Bit 7 is the MSB	3.3 V CMOS	2–9
	Blue [7:0]	Outputs of Converter Blue, Bit 7 is the MSB	3.3 V CMOS	12–19
	DATACK	Data Output Clock	3.3 V CMOS	67
	HSOUT	HSYNC Output (Phase-Aligned with DATACK)	3.3 V CMOS	66
	VSOUT	VSYNC Output (Phase-Aligned with DATACK)	3.3 V CMOS	64
	SOGOUT	Sync-on-Green Slicer Output	3.3 V CMOS	65
References	REF BYPASS	Internal Reference Bypass	1.25 V	58
	MIDSCV	Internal Midscale Voltage Bypass		37
	FILT	Connection for External Filter Components for Internal PLL		33
Power Supply	V_D	Analog Power Supply	3.3 V	39, 42, 45, 46, 51, 52, 59, 62
	V_{DD}	Output Power Supply	3.3 V	11, 22, 23, 69, 78, 79
	PV_D	PLL Power Supply	3.3 V	26, 27, 34, 35
	GND	Ground	0 V	1, 10, 20, 21, 24, 25, 28, 32, 36, 40, 41, 44, 47, 50, 53, 60, 61, 63, 68, 80
Control	SDA	Serial Port Data I/O	3.3 V CMOS	57
	SCL	Serial Port Data Clock (100 kHz Maximum)	3.3 V CMOS	56
	A0	Serial Port Address Input 1	3.3 V CMOS	55

PIN FUNCTION DESCRIPTIONS

Pin Name	Function
OUTPUTS	
HSOUT	Horizontal Sync Output A reconstructed and phase-aligned version of the Hsync input. Both the polarity and duration of this output can be programmed via serial bus registers. By maintaining alignment with DATACK and Data, data timing with respect to horizontal sync can always be determined.
VSOUT	Vertical Sync Output A reconstructed and phase-aligned version of the video Vsync. The polarity of this output can be controlled via a serial bus bit. The placement and duration in all modes is set by the graphics transmitter.
SOGOUT	Sync-On-Green Slicer Output This pin outputs either the signal from the Sync-on-Green slicer comparator or an unprocessed but delayed version of the Hsync input. See the Sync Processing Block Diagram (Figure 12) to view how this pin is connected. (Note: Besides slicing off SOG, the output from this pin gets no other additional processing on the AD9883A. Vsync separation is performed via the sync separator.)
SERIAL PORT (2-Wire)	
SDA	Serial Port Data I/O
SCL	Serial Port Data Clock
A0	Serial Port Address Input 1 For a full description of the 2-wire serial register and how it works, refer to the 2-Wire Serial Control Port section.
DATA OUTPUTS	
RED	Data Output, Red Channel
GREEN	Data Output, Green Channel
BLUE	Data Output, Blue Channel The main data outputs. Bit 7 is the MSB. The delay from pixel sampling time to output is fixed. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The DATACK and HSOUT outputs are also moved, so the timing relationship among the signals is maintained. For exact timing information, refer to Figures 7, 8, and 9.
DATA CLOCK OUTPUT	
DATACK	Data Output Clock This is the main clock output signal used to strobe the output data and HSOUT into external logic. It is produced by the internal clock generator and is synchronous with the internal pixel sampling clock. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The Data, DATACK, and HSOUT outputs are all moved, so the timing relationship among the signals is maintained.
INPUTS	
R_{AIN}	Analog Input for Red Channel
G_{AIN}	Analog Input for Green Channel
B_{AIN}	Analog Input for Blue Channel High impedance inputs that accept the Red, Green, and Blue channel graphics signals, respectively. (The three channels are identical, and can be used for any colors, but colors are assigned for convenient reference.) They accommodate input signals ranging from 0.5 V to 1.0 V full scale. Signals should be ac-coupled to these pins to support clamp operation.
HSYNC	Horizontal Sync Input This input receives a logic signal that establishes the horizontal timing reference and provides the frequency reference for pixel clock generation. The logic sense of this pin is controlled by serial register 0EH Bit 6 (Hsync Polarity). Only the leading edge of Hsync is active; the trailing edge is ignored. When Hsync Polarity = 0, the falling edge of Hsync is used. When Hsync Polarity = 1, the rising edge is active. The input includes a Schmitt trigger for noise immunity, with a nominal input threshold of 1.5 V.
VSYNC	Vertical Sync Input This is the input for vertical sync.
SOGIN	Sync-on-Green Input This input is provided to assist with processing signals with embedded sync, typically on the Green channel. The pin is connected to a high speed comparator with an internally generated threshold. The threshold level can be programmed in 10 mV steps to any voltage between 10 mV and 330 mV above the negative peak of the input signal. The default voltage threshold is 150 mV. When connected to an ac-coupled graphics signal with embedded sync, it will produce a noninverting digital output on SOGOUT. (This is usually a composite sync signal, containing both vertical and horizontal sync information that must be separated before passing the horizontal sync signal to Hsync.) When not used, this input should be left unconnected. For more details on this function and how it should be configured, refer to the Sync-on-Green section.

PIN FUNCTION DESCRIPTIONS (continued)

Pin Name	Function
CLAMP	External Clamp Input This logic input may be used to define the time during which the input signal is clamped to ground. It should be exercised when the reference dc level is known to be present on the analog input channels, typically during the back porch of the graphics signal. The CLAMP pin is enabled by setting control bit Clamp Function to 1, (register 0FH, Bit 7, default is 0). When disabled, this pin is ignored and the clamp timing is determined internally by counting a delay and duration from the trailing edge of the Hsync input. The logic sense of this pin is controlled by Clamp Polarity register 0FH, Bit 6. When not used, this pin must be grounded and Clamp Function programmed to 0.
COAST	Clock Generator Coast Input (Optional) This input may be used to cause the pixel clock generator to stop synchronizing with Hsync and continue producing a clock at its current frequency and phase. This is useful when processing signals from sources that fail to produce horizontal sync pulses during the vertical interval. The COAST signal is generally *not* required for PC-generated signals. The logic sense of this pin is controlled by Coast Polarity (register 0FH, Bit 3). When not used, this pin may be grounded and Coast Polarity programmed to 1, or tied HIGH (to V_D through a 10 kΩ resistor) and Coast Polarity programmed to 0. Coast Polarity defaults to 1 at power-up.
REF BYPASS	Internal Reference BYPASS Bypass for the internal 1.25 V band gap reference. It should be connected to ground through a 0.1 µF capacitor. The absolute accuracy of this reference is ±4%, and the temperature coefficient is ±50 ppm, which is adequate for most AD9883A applications. If higher accuracy is required, an external reference may be employed instead.
MIDSCV	Midscale Voltage Reference BYPASS Bypass for the internal midscale voltage reference. It should be connected to ground through a 0.1 µF capacitor. The exact voltage varies with the gain setting of the Blue channel.
FILT	External Filter Connection For proper operation, the pixel clock generator PLL requires an external filter. Connect the filter shown in Figure 6 to this pin. For optimal performance, minimize noise and parasitics on this node.
POWER SUPPLY	
V_D	Main Power Supply These pins supply power to the main elements of the circuit. They should be filtered and as quiet as possible.
V_{DD}	Digital Output Power Supply A large number of output pins (up to 25) switching at high speed (up to 110 MHz) generates a lot of power supply transients (noise). These supply pins are identified separately from the V_D pins so special care can be taken to minimize output noise transferred into the sensitive analog circuitry. If the AD9883A is interfacing with lower voltage logic, V_{DD} may be connected to a lower supply voltage (as low as 2.5 V) for compatibility.
PV_D	Clock Generator Power Supply The most sensitive portion of the AD9883A is the clock generation circuitry. These pins provide power to the clock PLL and help the user design for optimal performance. The designer should provide quiet, noise-free power to these pins.
GND	Ground The ground return for all circuitry on-chip. It is recommended that the AD9883A be assembled on a single solid ground plane, with careful attention given to ground current paths.

DESIGN GUIDE

General Description

The AD9883A is a fully integrated solution for capturing analog RGB signals and digitizing them for display on flat panel monitors or projectors. The circuit is ideal for providing a computer interface for HDTV monitors or as the front end to high performance video scan converters. Implemented in a high performance CMOS process, the interface can capture signals with pixel rates up to 110 MHz.

The AD9883A includes all necessary input buffering, signal dc restoration (clamping), offset and gain (brightness and contrast) adjustment, pixel clock generation, sampling phase control, and output data formatting. All controls are programmable via a 2-wire serial interface. Full integration of these sensitive analog functions makes system design straightforward and less sensitive to the physical and electrical environment.

With a typical power dissipation of only 500 mW and an operating temperature range of 0°C to 70°C, the device requires no special environmental considerations.

Digital Inputs

All digital inputs on the AD9883A operate to 3.3 V CMOS levels. However, all digital inputs are 5 V tolerant. Applying 5 V to them will not cause any damage.

Input Signal Handling

The AD9883A has three high impedance analog input pins for the Red, Green, and Blue channels. They will accommodate signals ranging from 0.5 V to 1.0 V p-p.

Signals are typically brought onto the interface board via a DVI-I connector, a 15-pin D connector, or via BNC connectors. The AD9883A should be located as close as practical to the input connector. Signals should be routed via matched-impedance traces (normally 75 Ω) to the IC input pins.

At that point the signal should be resistively terminated (75 Ω to the signal ground return) and capacitively coupled to the AD9883A inputs through 47 nF capacitors. These capacitors form part of the dc restoration circuit.

In an ideal world of perfectly matched impedances, the best performance can be obtained with the widest possible signal bandwidth. The ultrawide bandwidth inputs of the AD9883A (300 MHz) can track the input signal continuously as it moves from one pixel level to the next, and digitize the pixel during a long, flat pixel time. In many systems, however, there are mismatches, reflections, and noise, which can result in excessive ringing and distortion of the input waveform. This makes it more difficult to establish a sampling phase that provides good image quality. It has been shown that a small inductor in series with the input is effective in rolling off the input bandwidth slightly and providing a high quality signal over a wider range of conditions. Using a Fair-Rite #2508051217Z0 High Speed Signal Chip Bead inductor in the circuit of Figure 1 gives good results in most applications.

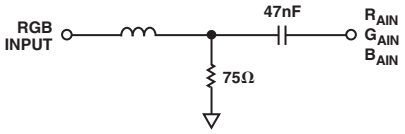

Figure 1. Analog Input Interface Circuit

Hsync, Vsync Inputs

The interface also takes a horizontal sync signal, which is used to generate the pixel clock and clamp timing. This can be either a sync signal directly from the graphics source, or a preprocessed TTL or CMOS level signal.

The Hsync input includes a Schmitt trigger buffer for immunity to noise and signals with long rise times. In typical PC based graphic systems, the sync signals are simply TTL-level drivers feeding unshielded wires in the monitor cable. As such, no termination is required.

Serial Control Port

The serial control port is designed for 3.3 V logic. If there are 5 V drivers on the bus, these pins should be protected with 150 Ω series resistors placed between the pull-up resistors and the input pins.

Output Signal Handling

The digital outputs are designed and specified to operate from a 3.3 V power supply (V_{DD}). They can also work with a V_{DD} as low as 2.5 V for compatibility with other 2.5 V logic.

Clamping

RGB Clamping

To properly digitize the incoming signal, the dc offset of the input must be adjusted to fit the range of the on-board A/D converters.

Most graphics systems produce RGB signals with black at ground and white at approximately 0.75 V. However, if sync signals are embedded in the graphics, the sync tip is often at ground and black is at 300 mV. Then white is at approximately 1.0 V. Some common RGB line amplifier boxes use emitter-follower buffers to split signals and increase drive capability. This introduces a 700 mV dc offset to the signal, which must be removed for proper capture by the AD9883A.

The key to clamping is to identify a portion (time) of the signal when the graphic system is known to be producing black. An offset is then introduced which results in the A/D converters producing a black output (code 00h) when the known black input is present. The offset then remains in place when other signal levels are processed, and the entire signal is shifted to eliminate offset errors.

In most PC graphics systems, black is transmitted between active video lines. With CRT displays, when the electron beam has completed writing a horizontal line on the screen (at the right side), the beam is deflected quickly to the left side of the screen (called horizontal retrace) and a black signal is provided to prevent the beam from disturbing the image.

In systems with embedded sync, a blacker-than-black signal (Hsync) is produced briefly to signal the CRT that it is time to begin a retrace. For obvious reasons, it is important to avoid clamping on the tip of Hsync. Fortunately, there is virtually always a period following Hsync, called the back porch, where a good black reference is provided. This is the time when clamping should be done.

The clamp timing can be established by simply exercising the CLAMP pin at the appropriate time (with External Clamp = 1). The polarity of this signal is set by the Clamp Polarity bit.

A simpler method of clamp timing employs the AD9883A internal clamp timing generator. The Clamp Placement register is programmed with the number of pixel times that should pass after the trailing edge of HSYNC before clamping starts. A second register (Clamp Duration) sets the duration of the clamp. These are both 8-bit values, providing considerable flexibility in clamp generation. The clamp timing is referenced to the trailing edge of Hsync because, though Hsync duration can vary widely, the back porch (black reference) always follows Hsync. A good starting point for establishing clamping is to set the clamp placement to 09H (providing 9 pixel periods for the graphics signal to stabilize after sync) and set the clamp duration to 14H (giving the clamp 20 pixel periods to reestablish the black reference).

Clamping is accomplished by placing an appropriate charge on the external input coupling capacitor. The value of this capacitor affects the performance of the clamp. If it is too small, there will be a significant amplitude change during a horizontal line time (between clamping intervals). If the capacitor is too large, then it will take excessively long for the clamp to recover from a large change in incoming signal offset. The recommended value (47 nF) results in recovering from a step error of 100 mV to within 1/2 LSB in 10 lines with a clamp duration of 20 pixel periods on a 60 Hz SXGA signal.

YUV Clamping

YUV graphic signals are slightly different from RGB signals in that the dc reference level (black level in RGB signals) can be at the midpoint of the graphics signal rather than at the bottom. For these signals, it can be necessary to clamp to the midscale range of the A/D converter range (80H) rather than at the bottom of the A/D converter range (00H).

Clamping to midscale rather than to ground can be accomplished by setting the clamp select bits in the serial bus register. Each of the three converters has its own selection bit so that they can be clamped to either midscale or ground independently. These bits are located in register 10H and are Bits 0–2. The midscale reference voltage that each A/D converter clamps to is provided on the MIDSCV pin, (Pin 37). This pin should be bypassed to ground with a 0.1 μF capacitor, (even if midscale clamping is not required).

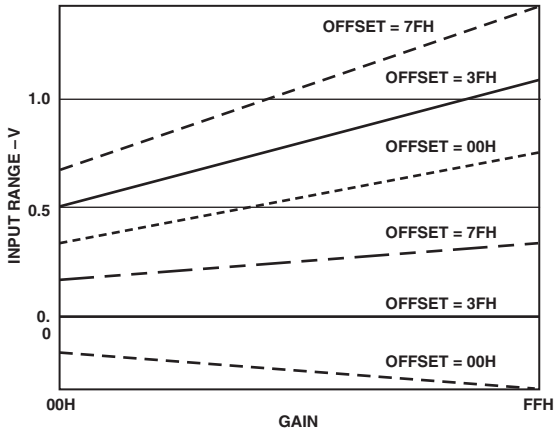

Figure 2. Gain and Offset Control

Gain and Offset Control

The AD9883A can accommodate input signals with inputs ranging from 0.5 V to 1.0 V full scale. The full-scale range is set in three 8-bit registers (Red Gain, Green Gain, and Blue Gain). Note that *increasing* the gain setting results in an image with *less* contrast.

The offset control shifts the entire input range, resulting in a change in image brightness. Three 7-bit registers (Red Offset, Green Offset, Blue Offset) provide independent settings for each channel. The offset controls provide a ±63 LSB adjustment range. This range is connected with the full-scale range, so if the input range is doubled (from 0.5 V to 1.0 V) then the offset step size is also doubled (from 2 mV per step to 4 mV per step).

Figure 2 illustrates the interaction of gain and offset controls. The magnitude of an LSB in offset adjustment is proportional to the full-scale range, so changing the full-scale range also changes the offset. The change is minimal if the offset setting is near midscale. When changing the offset, the full-scale *range* is not affected, but the full-scale *level* is shifted by the same amount as the zero scale level.

Sync-on-Green

The Sync-on-Green input operates in two steps. First, it sets a baseline clamp level off of the incoming video signal with a negative peak detector. Second, it sets the sync trigger level to a programmable level (typically 150 mV) above the negative peak. The Sync-on-Green input must be ac-coupled to the Green analog input through its own capacitor, as shown in Figure 3. The value of the capacitor must be 1 nF ± 20%. If Sync-on-Green is not used, this connection is not required. Note that the Sync-on-Green signal is always negative polarity.

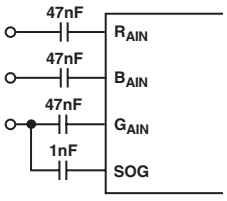

Figure 3. Typical Clamp Configuration

Clock Generation

A phase locked loop (PLL) is employed to generate the pixel clock. In this PLL, the Hsync input provides a reference frequency. A voltage controlled oscillator (VCO) generates a much higher pixel clock frequency. This pixel clock is divided by the PLL divide value (registers 01H and 02H) and phase compared with the Hsync input. Any error is used to shift the VCO frequency and maintain lock between the two signals.

The stability of this clock is a very important element in providing the clearest and most stable image. During each pixel time, there is a period during which the signal is slewing from the old pixel amplitude and settling at its new value. Then there is a time when the input voltage is stable, before the signal must slew to a new value (Figure 4). The ratio of the slewing time to the stable time is a function of the bandwidth of the graphics DAC and the bandwidth of the transmission system (cable and termination). It is also a function of the overall pixel rate. Clearly, if the dynamic characteristics of the system remain fixed, the slewing and settling time is likewise fixed. This time must be subtracted from the total pixel period, leaving the stable period. At higher pixel frequencies, the total cycle time is shorter, and the stable pixel time becomes shorter as well.

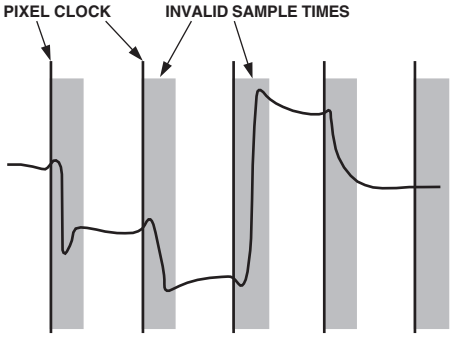

Figure 4. Pixel Sampling Times

Any jitter in the clock reduces the precision with which the sampling time can be determined, and must also be subtracted from the stable pixel time.

Considerable care has been taken in the design of the AD9883A's clock generation circuit to minimize jitter. As indicated in Figure 5, the clock jitter of the AD9883A is less than 5% of the total pixel time in all operating modes, making the reduction in the valid sampling time due to jitter negligible.

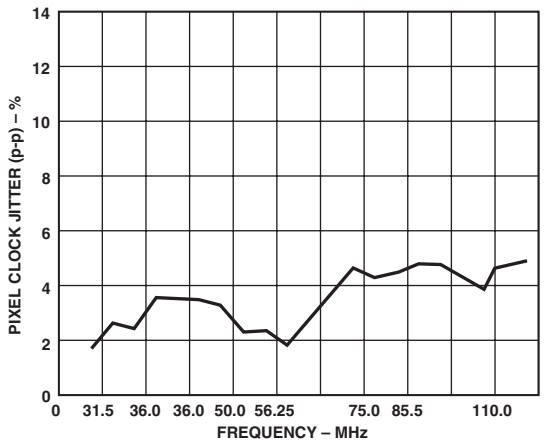

Figure 5. Pixel Clock Jitter vs. Frequency

The PLL characteristics are determined by the loop filter design, by the PLL Charge Pump Current, and by the VCO range setting. The loop filter design is illustrated in Figure 6. Recommended settings of VCO range and charge pump current for VESA standard display modes are listed in Table V.

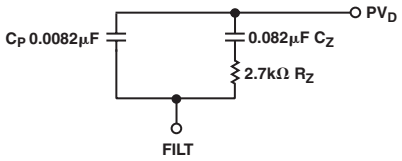

Figure 6. PLL Loop Filter Detail

Four programmable registers are provided to optimize the performance of the PLL. These registers are:

1. The 12-Bit Divisor Register. The input Hsync frequencies range from 15 kHz to 110 kHz. The PLL multiplies the frequency of the Hsync signal, producing pixel clock frequencies in the range of 12 MHz to 110 MHz. The Divisor Register controls the exact multiplication factor. This register may be set to any value between 221 and 4095. (The divide ratio that is actually used is the programmed divide ratio plus one.)
2. The 2-Bit VCO Range Register. To improve the noise performance of the AD9883A, the VCO operating frequency range is divided into three overlapping regions. The VCO Range Register sets this operating range. The frequency ranges for the lowest and highest regions are shown in Table II.

Table II. VCO Frequency Ranges

PV1	PV0	Pixel Clock Range (MHz) AD9883AKST	Pixel Clock Range (MHz) AD9883ABST
0	0	12–32	12–30
0	1	32–64	30–60
1	0	64–110	60–120
1	1	110–140	120–140

3. The 3-Bit Charge Pump Current Register. This register allows the current that drives the low-pass loop filter to be varied. The possible current values are listed in Table III.

Table III. Charge Pump Current/Control Bits

Ip2	Ip1	Ip0	Current (µA)
0	0	0	50
0	0	1	100
0	1	0	150
0	1	1	250
1	0	0	350
1	0	1	500
1	1	0	750
1	1	1	1500

4. The 5-Bit Phase Adjust Register. The phase of the generated sampling clock may be shifted to locate an optimum sampling point within a clock cycle. The Phase Adjust Register provides 32 phase-shift steps of 11.25° each. The Hsync signal with an identical phase shift is available through the HSOUT pin.

   The COAST pin is used to allow the PLL to continue to run at the same frequency, in the absence of the incoming Hsync signal or during disturbances in Hsync (such as equalization pulses). This may be used during the vertical sync period, or any other time that the Hsync signal is unavailable. The polarity of the COAST signal may be set through the Coast Polarity Register. Also, the polarity of the Hsync signal may be set through the Hsync Polarity Register. If not using automatic polarity detection, the Hsync and COAST Polarity bits should be set to match the respective polarities of the input signals.

Power Management

The AD9883A uses the activity detect circuits, the active interface bits in the serial bus, the active interface override bits, and the power-down bit to determine the correct power state. There are three power states, full-power, seek mode, and power-down. Table IV summarizes how the AD9883A determines what power mode to be in and which circuitry is powered on/off in each of these modes. The power-down command has priority over the automatic circuitry.

Table IV. Power-Down Mode Descriptions

Mode	Inputs Power-Down[1]	Sync Detect[2]	Powered On or Comments
Full-Power	1	1	Everything
Seek Mode	1	0	Serial Bus, Sync Activity Detect, SOG, Band Gap Reference
Power-Down	0	X	Serial Bus, Sync Activity Detect, SOG, Band Gap Reference

NOTES
[1]Power-down is controlled via Bit 1 in serial bus register 0FH.
[2]Sync detect is determined by OR-ing Bits 7, 4, and 1 in serial bus register 14H.

Table V. Recommended VCO Range and Charge Pump Current Settings for Standard Display Formats

Standard	Resolution	Refresh Rate	Horizontal Frequency	Pixel Rate	AD9883AKST		AD9883ABST	
					VCORNGE	Current	VCORNGE	Current
VGA	640 × 480	60 Hz	31.5 kHz	25.175 MHz	00	110	00	011
		72 Hz	37.7 kHz	31.500 MHz	00	110	01	010
		75 Hz	37.5 kHz	31.500 MHz	00	110	01	010
		85 Hz	43.3 kHz	36.000 MHz	01	100	01	010
SVGA	800 × 600	56 Hz	35.1 kHz	36.000 MHz	01	100	01	010
		60 Hz	37.9 kHz	40.000 MHz	01	100	01	011
		72 Hz	48.1 kHz	50.000 MHz	01	101	01	100
		75 Hz	46.9 kHz	49.500 MHz	01	101	01	100
		85 Hz	53.7 kHz	56.250 MHz	01	101	01	101
XGA	1024 × 768	60 Hz	48.4 kHz	65.000 MHz	10	101	10	011
		70 Hz	56.5 kHz	75.000 MHz	10	100	10	011
		75 Hz	60.0 kHz	78.750 MHz	10	100	10	011
		80 Hz	64.0 kHz	85.500 MHz	10	101	10	100
		85 Hz	68.3 kHz	94.500 MHz	10	101	10	100
SXGA	1280 × 1024	60 Hz	64.0 kHz	108.000 MHz	10	110	10	101
		75 Hz	80.0 kHz	135.000 MHz	11	110	11	101

Timing

The following timing diagrams show the operation of the AD9883A.

The output data clock signal is created so that its rising edge always occurs between data transitions, and can be used to latch the output data externally.

There is a pipeline in the AD9883A, which must be flushed before valid data becomes available. This means four data sets are presented before valid data is available.

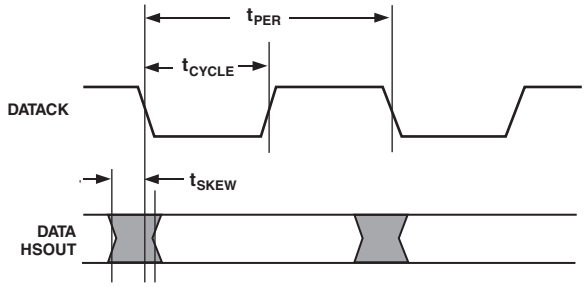

Figure 7. Output Timing

Hsync Timing

Horizontal Sync (Hsync) is processed in the AD9883A to eliminate ambiguity in the timing of the leading edge with respect to the phase-delayed pixel clock and data.

The Hsync input is used as a reference to generate the pixel sampling clock. The sampling phase can be adjusted, with respect to Hsync, through a full 360° in 32 steps via the Phase Adjust Register (to optimize the pixel sampling time). Display systems use Hsync to align memory and display write cycles, so it is important to have a stable timing relationship between Hsync output (HSOUT) and data clock (DATACK).

Three things happen to Horizontal Sync in the AD9883A. First, the polarity of Hsync input is determined and will thus have a known output polarity. The known output polarity can be programmed either active high or active low (register 0EH, Bit 5). Second, HSOUT is aligned with DATACK and data outputs. Third, the duration of HSOUT (in pixel clocks) is set via register 07H. HSOUT is the sync signal that should be used to drive the rest of the display system.

Coast Timing

In most computer systems, the Hsync signal is provided continuously on a dedicated wire. In these systems, the COAST input and function are unnecessary, and should not be used and the pin should be permanently connected to the inactive state.

In some systems, however, Hsync is disturbed during the Vertical Sync period (Vsync). In some cases, Hsync pulses disappear. In other systems, such as those that employ Composite Sync (Csync) signals or embedded Sync-on-Green (SOG), Hsync includes equalization pulses or other distortions during Vsync. To avoid upsetting the clock generator during Vsync, it is important to ignore these distortions. If the pixel clock PLL sees extraneous pulses, it will attempt to lock to this new frequency, and will have changed frequency by the end of the Vsync period. It will then take a few lines of correct Hsync timing to recover at the beginning of a new frame, resulting in a "tearing" of the image at the top of the display.

The COAST input is provided to eliminate this problem. It is an asynchronous input that disables the PLL input and allows the clock to free-run at its then-current frequency. The PLL can free-run for several lines without significant frequency drift.

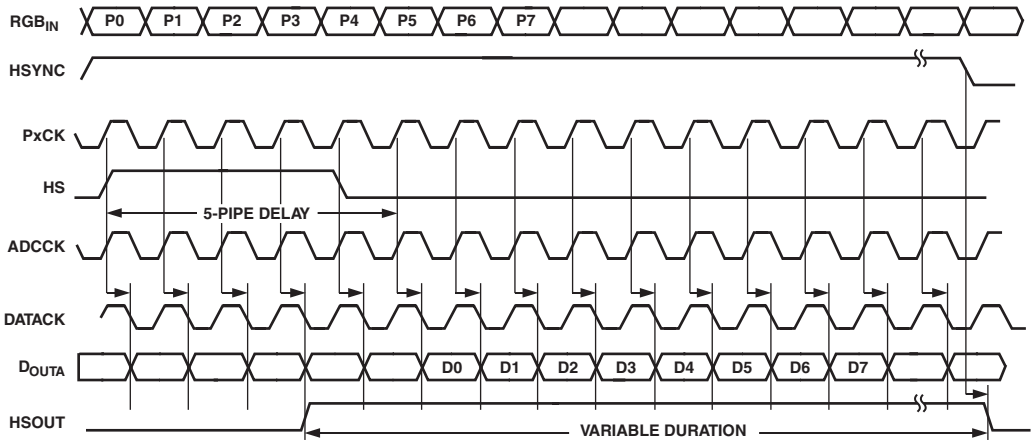

Figure 8. 4:4:4 Mode (For RGB and YUV)

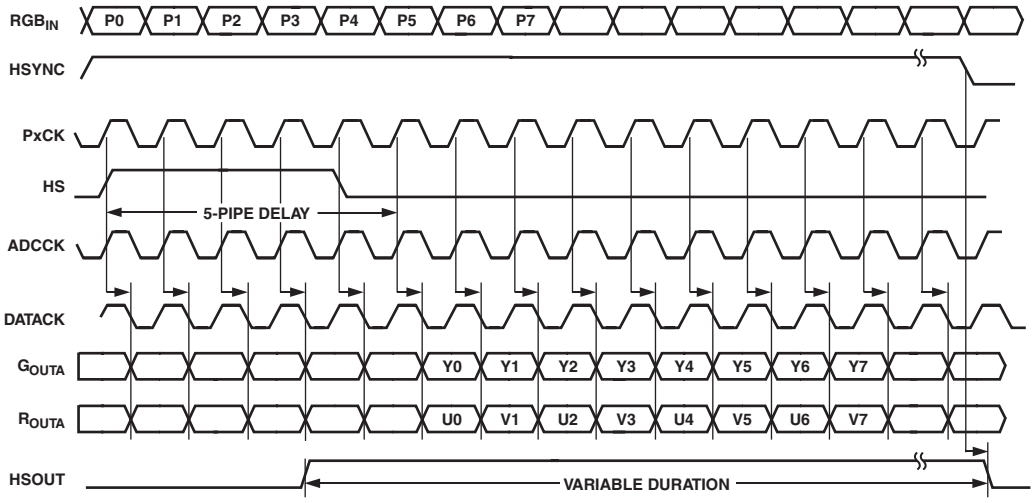

Figure 9. 4:2:2 Mode (For YUV Only)

2-Wire Serial Register Map

The AD9883A is initialized and controlled by a set of registers, which determine the operating modes. An external controller is employed to write and read the control registers through the two-line serial interface port.

Table VI. Control Register Map

Hex Address	Write and Read or Read Only	Bits	Default Value	Register Name	Function
00H	RO	7:0		Chip Revision	An 8-bit register that represents the silicon revision level. Revision 0 = 0000 0000.
01H*	R/$\overline{W}$	7:0	01101001	PLL Div MSB	This register is for Bits [11:4] of the PLL divider. Greater values mean the PLL operates at a faster rate. This register should be loaded first whenever a change is needed. This will give the PLL more time to lock.
02H*	R/$\overline{W}$	7:4	1101****	PLL Div LSB	Bits [7:4] of this word are written to the LSBs [3:0] of the PLL divider word.
03H	R/$\overline{W}$	7:3	01****** **001***		Bits [7:6] VCO Range. Selects VCO frequency range. (See PLL description.) Bits [5:3] Charge Pump Current. Varies the current that drives the low-pass filter. (See PLL description.)
04H	R/$\overline{W}$	7:3	10000***	Phase Adjust	ADC Clock Phase Adjustment. Larger values mean more delay. (1 LSB = T/32)
05H	R/$\overline{W}$	7:0	10000000	Clamp Placement	Places the Clamp signal an integer number of clock periods after the trailing edge of the Hsync signal.
06H	R/$\overline{W}$	7:0	10000000	Clamp Duration	Number of clock periods that the Clamp signal is actively clamping.
07H	R/$\overline{W}$	7:0	00100000	Hsync Output Pulsewidth	Sets the number of pixel clocks that HSOUT will remain active.
08H	R/W	7:0	10000000	Red Gain	Controls ADC input range (contrast) of each respective channel. Greater values give less contrast.
09H	R/W	7:0	10000000	Green Gain	
0AH	R/W	7:0	10000000	Blue Gain	
0BH	R/W	7:1	1000000*	Red Offset	Controls dc offset (brightness) of each respective channel. Greater values decrease brightness.
0CH	R/W	7:1	1000000*	Green Offset	
0DH	R/W	7:1	1000000*	Blue Offset	
0EH	R/$\overline{W}$	7:0	0******* *1****** **0***** ***0**** ****0*** *****0** ******0* *******0	Sync Control	Bit 7 – Hsync Polarity Override. (Logic 0 = Polarity determined by chip, Logic 1 = Polarity set by Bit 6 in register 0EH.) Bit 6 – Hsync Input Polarity. Indicates polarity of incoming Hsync signal to the PLL. (Logic 0 = Active Low, Logic 1 = Active High.) Bit 5 – Hsync Output Polarity. (Logic 0 = Logic High Sync, Logic 1 = Logic Low Sync.) Bit 4 – Active Hsync Override. If set to Logic 1, the user can select the Hsync to be used via Bit 3. If set to Logic 0, the active interface is selected via Bit 6 in register 14H. Bit 3 – Active Hsync Select. Logic 0 selects Hsync as the active sync. Logic 1 selects Sync-on-Green as the active sync. Note that the indicated Hsync will be used only if Bit 4 is set to Logic 1 or if both syncs are active. (Bits 1, 7 = Logic 1 in register 14H.) Bit 2 – Vsync Output Invert. (Logic 1 = No Invert, Logic 0 = Invert.) Bit 1 – Active Vsync Override. If set to Logic 1, the user can select the Vsync to be used via Bit 0. If set to Logic 0, the active interface is selected via Bit 3 in register 14H. Bit 0 – Active Vsync Select. Logic 0 selects Raw Vsync as the output Vsync. Logic 1 selects Sync Separated Vsync as the output Vsync. Note that the indicated Vsync will be used only if Bit 1 is set to Logic 1.

Table VI. Control Register Map (continued)

Hex Address	Write and Read or Read Only	Bits	Default Value	Register Name	Function
0FH	R/W	7:1	0******* *1****** **0***** ***0**** ****1*** *****1** ******1*		Bit 7 – Clamp Function. Chooses between Hsync for Clamp signal or another external signal to be used for clamping. (Logic 0 = Hsync, Logic 1 = Clamp.) Bit 6 – Clamp Polarity. Valid only with external Clamp signal. (Logic 0 = Active High, Logic 1 Selects Active Low.) Bit 5 – Coast Select. Logic 0 selects the coast input pins to be used for the PLL coast. Logic 1 selects Vsync to be used for the PLL coast. Bit 4 – Coast Polarity Override. (Logic 0 = Polarity determined by chip, Logic 1 = Polarity set by Bit 3 in register 0FH.) Bit 3 – Coast Polarity. Selects polarity of external Coast signal. (Logic 0 = Active Low, Logic 1 = Active High.) Bit 2 – Seek Mode Override. (Logic 1 = Allow Low Power Mode, Logic 0 = Disallow Low Power Mode.) Bit 1 – PWRDN. Full Chip Power-Down, Active Low. (Logic 0 = Full Chip Power-Down, Logic 1 = Normal.)
10H	R/W	7:3	10111*** *****0** ******0* *******0	Sync-on-Green Threshold	Sync-on-Green Threshold. Sets the voltage level of the Sync-on-Green slicer's comparator. Bit 2 – Red Clamp Select. Logic 0 selects clamp to ground. Logic 1 selects clamp to midscale (voltage at Pin 37). Bit 1 – Green Clamp Select. Logic 0 selects clamp to ground. Logic 1 selects clamp to midscale (voltage at Pin 37). Bit 0 – Blue Clamp Select. Logic 0 selects clamp to ground. Logic 1 selects clamp to midscale (voltage at Pin 37).
11H	R/W	7:0	00100000	Sync Separator Threshold	Sync Separator Threshold. Sets how many internal 5 MHz clock periods the sync separator will count to before toggling high or low. This should be set to some number greater than the maximum Hsync or equalization pulsewidth.
12H	R/W	7:0	00000000	Pre-Coast	Pre-Coast. Sets the number of Hsync periods that Coast becomes active prior to Vsync.
13H	R/W	7:0	00000000	Post-Coast	Post-Coast. Sets the number of Hsync periods that Coast stays active following Vsync.
14H	RO	7:0		Sync Detect	Bit 7 – Hsync detect. It is set to Logic 1 if Hsync is present on the analog interface; otherwise it is set to Logic 0. Bit 6 – AHS: Active Hsync. This bit indicates which analog Hsync is being used. (Logic 0 = Hsync Input Pin, Logic 1 = Hsync from Sync-on-Green.) Bit 5 – Input Hsync Polarity Detect. (Logic 0 = Active Low, Logic 1 = Active High.) Bit 4 – Vsync Detect. It is set to Logic 1 if Vsync is present on the analog interface; otherwise it is set to Logic 0. Bit 3 – AVS: Active Vsync. This bit indicates which analog Vsync is being used. (Logic 0 = Vsync Input Pin, Logic 1 = Vsync from Sync Separator.) Bit 2 – Output Vsync Polarity Detect. (Logic 0 = Active Low, Logic 1 = Active High.) Bit 1 – Sync-on-Green Detect. It is set to Logic 1 if sync is present on the Green video input; otherwise it is set to 0. Bit 0 – Input Coast Polarity Detect. (Logic 0 = Active Low, Logic 1 = Active High.)
15H	R/$\overline{W}$	7:0	1111**** ****1*** *****1** ******1* *******1	Test Register	Bits [7:4] Reserved for future use. Bit 3 – Must be set to 1 for proper operation. Bit 2 – Must be set to 1 for proper operation. Bit 1 – 4:2:2 Output Formatting Mode (Logic 0 = 4:2:2 mode, Logic 1= 4:4:4 mode) Bit 0 – Must be set to 0 for proper operation.

Table VI. Control Register Map (continued)

Hex Address	Write and Read or Read Only	Bits	Default Value	Register Name	Function
16H	R/$\overline{W}$	7:0		Test Register	Reserved for future use.
17H	RO	7:0		Test Register	Reserved for future use.
18H	RO	7:0		Test Register	Reserved for future use.

*The AD9883A only updates the PLL divide ratio when the LSBs are written to (register 02H).

2-WIRE SERIAL CONTROL REGISTER DETAIL CHIP IDENTIFICATION

00 7–0 Chip Revision

An 8-bit register that represents the silicon revision. Revision 0 = 0000 0000, Revision 1 = 0000 0001, Revision 2 = 0000 0010.

PLL DIVIDER CONTROL

01 7–0 PLL Divide Ratio MSBs

The 8 most significant bits of the 12-bit PLL divide ratio PLLDIV. (The operational divide ratio is PLLDIV + 1.)

The PLL derives a master clock from an incoming Hsync signal. The master clock frequency is then divided by an integer value, such that the output is phase-locked to Hsync. This PLLDIV value determines the number of pixel times (pixels plus horizontal blanking overhead) per line. This is typically 20% to 30% more than the number of active pixels in the display.

The 12-bit value of the PLL divider supports divide ratios from 2 to 4095. The higher the value loaded in this register, the higher the resulting clock frequency with respect to a fixed Hsync frequency.

VESA has established some standard timing specifications that assist in determining the value for PLLDIV as a function of horizontal and vertical display resolution and frame rate (Table V).

However, many computer systems do not conform precisely to the recommendations, and these numbers should be used only as a guide. The display system manufacturer should provide automatic or manual means for optimizing PLLDIV. An incorrectly set PLLDIV will usually produce one or more vertical noise bars on the display. The greater the error, the greater the number of bars produced.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 69H, PLLDIVL = DxH).

The AD9883A updates the full divide ratio only when the LSBs are changed. Writing to the MSB by itself will not trigger an update.

02 7–4 PLL Divide Ratio LSBs

The 4 least significant bits of the 12-bit PLL divide ratio PLLDIV. The operational divide ratio is PLLDIV + 1.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 69H, PLLDIVL = DxH).

The AD9883A updates the full divide ratio only when this register is written to.

CLOCK GENERATOR CONTROL

03 7–6 VCO Range Select

Two bits that establish the operating range of the clock generator.

VCORNGE must be set to correspond with the desired operating frequency (incoming pixel rate).

The PLL gives the best jitter performance at high frequencies. For this reason, to output low pixel rates and still get good jitter performance, the PLL actually operates at a higher frequency but then divides down the clock rate afterwards. Table VII shows the pixel rates for each VCO range setting. The PLL output divisor is automatically selected with the VCO range setting.

Table VII. VCO Ranges

VCORNGE	Pixel Rate Range
00	12–32
01	32–64
10	64–110
11	110–140

The power-up default value is 01.

03 5–3 CURRENT Charge Pump Current

Three bits that establish the current driving the loop filter in the clock generator.

Table VIII. Charge Pump Currents

CURRENT	Current (μA)
000	50
001	100
010	150
011	250
100	350
101	500
110	750
111	1500

CURRENT must be set to correspond with the desired operating frequency (incoming pixel rate).

The power-up default value is current = 001.

04 7–3 Clock Phase Adjust
A 5-bit value that adjusts the sampling phase in 32 steps across one pixel time. Each step represents an 11.25° shift in sampling phase.

The power-up default value is 16.

CLAMP TIMING

05 7–0 Clamp Placement
An 8-bit register that sets the position of the internally generated clamp.

When Clamp Function (Register 0FH, Bit 7) = 0, a clamp signal is generated internally, at a position established by the clamp placement and for a duration set by the clamp duration. Clamping is started (Clamp Placement) pixel periods after the trailing edge of Hsync. The clamp placement may be programmed to any value between 1 and 255.

The clamp should be placed during a time that the input signal presents a stable black-level reference, usually the back porch period between Hsync and the image.

When Clamp Function = 1, this register is ignored.

06 7–0 Clamp Duration
An 8-bit register that sets the duration of the internally generated clamp.

For the best results, the clamp duration should be set to include the majority of the black reference signal time that follows the Hsync signal trailing edge. Insufficient clamping time can produce brightness changes at the top of the screen, and a slow recovery from large changes in the average picture level (APL), or brightness.

When Clamp Function = 1, this register is ignored.

Hsync PULSEWIDTH

07 7–0 Hsync Output Pulsewidth
An 8-bit register that sets the duration of the Hsync output pulse.

The leading edge of the Hsync output is triggered by the internally generated, phase-adjusted PLL feedback clock. The AD9883A then counts a number of pixel clocks equal to the value in this register. This triggers the trailing edge of the Hsync output, which is also phase adjusted.

INPUT GAIN

08 7–0 Red Channel Gain Adjust
An 8-bit word that sets the gain of the Red channel. The AD9883A can accommodate input signals with a full-scale range of between 0.5 V and 1.0 V p-p. Setting REDGAIN to 255 corresponds to a 1.0 V input range. A REDGAIN of 0 establishes a 0.5 V input range. Note that increasing REDGAIN results in the picture having less contrast (the input signal uses fewer of the available converter codes). See Figure 2.

09 7–0 Green Channel Gain Adjust
An 8-bit word that sets the gain of the Green channel. See REDGAIN (08).

0A 7–0 Blue Channel Gain Adjust
An 8-bit word that sets the gain of the Blue channel. See REDGAIN (08).

INPUT OFFSET

0B 7–1 Red Channel Offset Adjust
A 7-bit offset binary word that sets the dc offset of the Red channel. One LSB of offset adjustment equals approximately one LSB change in the ADC offset. Therefore, the absolute magnitude of the offset adjustment scales as the gain of the channel is changed. A nominal setting of 63 results in the channel nominally clamping the back porch (during the clamping interval) to Code 00. An offset setting of 127 results in the channel clamping to Code 64 of the ADC. An offset setting of 0 clamps to Code –63 (off the bottom of the range). Increasing the value of Red Offset *decreases* the brightness of the channel.

0C 7–1 Green Channel Offset Adjust
A 7-bit offset binary word that sets the dc offset of the Green channel. See REDOFST (0B).

0D 7–1 Blue Channel Offset Adjust
A 7-bit offset binary word that sets the dc offset of the Green channel. See REDOFST (0B).

MODE CONTROL 1

0E 7 Hsync Input Polarity Override
This register is used to override the internal circuitry that determines the polarity of the Hsync signal going into the PLL.

Table IX. Hsync Input Polarity Override Settings

Override Bit	Function
0	Hsync Polarity Determined by Chip
1	Hsync Polarity Determined by User

The default for Hsync polarity override is 0 (polarity determined by chip).

0E 6 HSPOL Hsync Input Polarity
A bit that must be set to indicate the polarity of the Hsync signal that is applied to the PLL Hsync input.

Table X. Hsync Input Polarity Settings

HSPOL	Function
0	Active Low
1	Active High

Active Low means the leading edge of the Hsync pulse is negative going. All timing is based on the leading edge of Hsync, which is the falling edge. The rising edge has no effect.

Active high is inverted from the traditional Hsync, with a positive-going pulse. This means that timing will be based on the leading edge of Hsync, which is now the rising edge.

The device will operate if this bit is set incorrectly, but the internally generated clamp position, as established by Clamp Placement (Register 05H), will not be placed as expected, which may generate clamping errors.

The power-up default value is HSPOL = 1.

0E 5 Hsync Output Polarity
This bit determines the polarity of the Hsync output and the SOG output. Table XI shows the effect of this option. SYNC indicates the logic state of the sync pulse.

Table XI. Hsync Output Polarity Settings

Setting	SYNC
0	Logic 1 (Positive Polarity)
1	Logic 0 (Negative Polarity)

The default setting for this register is 0.

0E 4 Active Hsync Override
This bit is used to override the automatic Hsync selection, To override, set this bit to Logic 1. When overriding, the active Hsync is set via Bit 3 in this register.

Table XII. Active Hsync Override Settings

Override	Result
0	Autodetermines the Active Interface
1	Override, Bit 3 Determines the Active Interface

The default for this register is 0.

0E 3 Active Hsync Select
This bit is used under two conditions. It is used to select the active Hsync when the override bit is set (Bit 4). Alternately, it is used to determine the active Hsync when not overriding but both Hsyncs are detected.

Table XIII. Active HSYNC Select Settings

Select	Result
0	HSYNC Input
1	Sync-on-Green Input

The default for this register is 0.

0E 2 Vsync Output Invert
This bit inverts the polarity of the Vsync output. Table XIV shows the effect of this option.

Table XIV. Vsync Output Invert Settings

Setting	Vsync Output
0	Invert
1	No Invert

The default setting for this register is 0.

0E 1 Active Vsync Override
This bit is used to override the automatic Vsync selection. To override, set this bit to Logic 1. When overriding, the active interface is set via Bit 0 in this register.

Table XV. Active Vsync Override Settings

Override	Result
0	Autodetermine the Active Vsync
1	Override, Bit 0 Determines the Active Vsync

The default for this register is 0.

0E 0 Active Vsync Select
This bit is used to select the active Vsync when the override bit is set (Bit 1).

Table XVI. Active Vsync Select Settings

Select	Result
0	Vsync Input
1	Sync Separator Output

The default for this register is 0.

0F 7 Clamp Input Signal Source
This bit determines the source of clamp timing.

Table XVII. Clamp Input Signal Source Settings

Clamp Function	Function
0	Internally Generated Clamp Signal
1	Externally Provided Clamp Signal

A 0 enables the clamp timing circuitry controlled by clamp placement and clamp duration. The clamp position and duration is counted from the leading edge of Hsync.

A 1 enables the external CLAMP input pin. The three channels are clamped when the CLAMP signal is active. The polarity of CLAMP is determined by the Clamp Polarity bit (Register 0FH, Bit 6).

The power-up default value is Clamp Function = 0.

0F 6 Clamp Input Signal Polarity
This bit determines the polarity of the externally provided CLAMP signal.

Table XVIII. Clamp Input Signal Polarity Settings

Clamp Function	Function
1	Active Low
0	Active High

A Logic 1 means that the circuit will clamp when CLAMP is low, and it will pass the signal to the ADC when CLAMP is high.

A Logic 0 means that the circuit will clamp when CLAMP is high, and it will pass the signal to the ADC when CLAMP is low.

The power-up default value is Clamp Polarity = 1.

0F 5 Coast Select
This bit is used to select the active Coast source. The choices are the Coast Input Pin or Vsync. If Vsync is selected the additional decision of using the Vsync input pin or the output from the sync separator needs to be made (Register 0E, Bits 1, 0).

Table XIX. Power-Down Settings

Select	Result
0	Coast Input Pin
1	Vsync (See above Text)

0F 4 Coast Input Polarity Override
This register is used to override the internal circuitry that determines the polarity of the Coast signal going into the PLL.

Table XX. Coast Input Polarity Override Settings

Override Bit	Result
0	Determined by Chip
1	Determined by User

The default for coast polarity override is 0.

0F 3 Coast Input Polarity
This bit indicates the polarity of the Coast signal that is applied to the PLL COAST input.

Table XXI. Coast Input Polarity Settings

Coast Polarity	Function
0	Active Low
1	Active High

Active Low means that the clock generator will ignore Hsync inputs when Coast is low, and continue operating at the same nominal frequency until Coast goes high.

Active High means that the clock generator will ignore Hsync inputs when Coast is high, and continue operating at the same nominal frequency until Coast goes low.

This function needs to be used along with the Coast Polarity Override bit (Bit 4).

The power-up default value is 1.

0F 2 Seek Mode Override
This bit is used to either allow or disallow the low power mode. The low power mode (Seek Mode) occurs when there are no signals on any of the Sync inputs.

Table XXII. Seek Mode Override Settings

Select	Result
1	Allow Seek Mode
0	Disallow Seek Mode

The default for this register is 1.

0F 1 $\overline{\text{PWRDN}}$
This bit is used to put the chip in full power-down. See Power Management Section for details of which blocks are powered down.

Table XXIII. Power-Down Settings

Select	Result
0	Power-Down
1	Normal Operation

The default for this register is 1.

10 7-3 Sync-on-Green Slicer Threshold
This register allows the comparator threshold of the Sync-on-Green slicer to be adjusted. This register adjusts it in steps of 10 mV, with the minimum setting equaling 10 mV (11111) and the maximum setting equaling 330 mV (00000).

The default setting is 23, which corresponds to a threshold value of 100 mV; for a threshold of 150 mV, the setting should be 18.

10 2 Red Clamp Select
This bit determines whether the Red channel is clamped to ground or to midscale. For RGB video, all three channels are referenced to ground. For YCbCr (or YUV), the Y channel is referenced to ground, but the CbCr channels are referenced to midscale. Clamping to midscale actually clamps to Pin 37.

Table XXIV. Red Clamp Select Settings

Clamp	Function
0	Clamp to Ground
1	Clamp to Midscale (Pin 37)

The default setting for this register is 0.

10 1 Green Clamp Select
This bit determines whether the Green channel is clamped to ground or to midscale.

Table XXV. Green Clamp Select Settings

Clamp	Function
0	Clamp to Ground
1	Clamp to Midscale (Pin 37)

The default setting for this register is 0.

10 0 Blue Clamp Select
This bit determines whether the Blue channel is clamped to ground or to midscale.

Table XXVI. Blue Clamp Select Settings

Clamp	Function
0	Clamp to Ground
1	Clamp to Midscale (Pin 37)

The default setting for this register is 0.

11 7–0 Sync Separator Threshold
This register is used to set the responsiveness of the sync separator. It sets how many internal 5 MHz clock periods the sync separator must count to before toggling high or low. It works like a low-pass filter to ignore Hsync pulses in order to extract the Vsync signal. This register should be set to some number greater than the maximum Hsync pulsewidth. Note that the sync separator threshold uses an internal dedicated clock with a frequency of approximately 5 MHz.

The default for this register is 32.

12 7–0 Pre-Coast
This register allows the coast signal to be applied prior to the Vsync signal. This is necessary in cases where pre-equalization pulses are present. The step size for this control is one Hsync period.

The default is 0.

13 **7–0 Post-Coast**
This register allows the coast signal to be applied following the Vsync signal. This is necessary in cases where post-equalization pulses are present. The step size for this control is one Hsync period.

The default is 0.

14 **7 Hsync Detect**
This bit is used to indicate when activity is detected on the Hsync input pin (Pin 30). If Hsync is held high or low, activity will not be detected.

Table XXVII. Hsync Detection Results

Detect	Function
0	No Activity Detected
1	Activity Detected

The sync processing block diagram shows where this function is implemented.

14 **6 AHS – Active Hsync**
This bit indicates which Hsync input source is being used by the PLL (Hsync input or Sync-on-Green). Bits 7 and 1 in this register determine which source is used. If both Hsync and SOG are detected, the user can determine which has priority via Bit 3 in register 0EH. The user can override this function via Bit 4 in register 0EH. If the override bit is set to Logic 1, then this bit will be forced to whatever the state of Bit 3 in register 0EH is set to.

Table XXVIII. Active Hsync Results

Bit 7 (Hsync Detect)	Bit 1 (SOG Detect)	Bit 4, Reg 0EH (Override)	AHS
0	0	0	Bit 3 in 0EH
0	1	0	1
1	0	0	0
1	1	0	Bit 3 in 0EH
X	X	1	Bit 3 in 0EH

AHS = 0 means use the Hsync pin input for Hsync.
AHS = 1 means use the SOG pin input for Hsync.

The override bit is in register 0EH, Bit 4.

14 **5 Detected Hsync Input Polarity Status**
This bit reports the status of the Hsync input polarity detection circuit. It can be used to determine the polarity of the Hsync input. The detection circuit's location is shown in the Sync Processing Block Diagram (Figure 12).

Table XXIX. Detected Hsync Input Polarity Status

Hsync Polarity Status	Result
0	Negative
1	Positive

14 **4 Vsync Detect**
This bit is used to indicate when activity is detected on the Vsync input pin (Pin 31). If Vsync is held steady high or low, activity will not be detected.

Table XXX. Vsync Detection Results

Detect	Function
0	No Activity Detected
1	Activity Detected

The Sync Processing Block Diagram (Figure 12) shows where this function is implemented.

14 **3 AVS – Active Vsync**
This bit indicates which Vsync source is being used: the Vsync input or output from the sync separator. Bit 4 in this register determines which is active. If both Vsync and SOG are detected, the user can determine which has priority via Bit 0 in register 0EH. The user can override this function via Bit 1 in register 0EH. If the override bit is set to Logic 1, this bit will be forced to whatever the state of Bit 0 in register 0EH is set.

Table XXXI. Active Vsync Results

Bit 4, Reg 14H (Vsync Detect)	Bit 1, Reg 0EH (Override)	AVS
1	0	0
0	0	1
X	1	Bit 0 in 0EH

AVS = 0 means Vsync input.
AVS = 1 means Sync separator.

The override bit is in register 0EH, Bit 1.

14 **2 Detected Vsync Output Polarity Status**
This bit reports the status of the Vsync output polarity detection circuit. It can be used to determine the polarity of the Vsync output. The detection circuit's location is shown in the Sync Processing Block Diagram (Figure 12).

Table XXXII. Detected Vsync Output Polarity Status

Vsync Polarity Status	Result
0	Active Low
1	Active High

14 **1 Sync-on-Green Detect**
This bit is used to indicate when sync activity is detected on the Sync-on-Green input pin (Pin 49).

Table XXXIII. Sync-on-Green Detection Results

Detect	Function
0	No Activity Detected
1	Activity Detected

The Sync Processing Block Diagram (Figure 12) shows where this function is implemented.

14 **0 Detected Coast Polarity Status**
This bit reports the status of the Coast input polarity detection circuit. It can be used to determine the polarity of the Coast input. The detection circuit's location is shown in the Sync Processing Block Diagram (Figure 12).

Table XXXIV. Detected Coast Input Polarity Status

Polarity Status	Result
0	Coast Polarity Negative
1	Coast Polarity Positive

This indicates that Bit 1 of Register 5 is the 4:2:2 Output mode select bit.

15 1 **4:2:2 Output Mode Select**
A bit that configures the output data in 4:2:2 mode. This mode can be used to reduce the number of data lines used from 24 down to 16 for applications using YUV, YCbCr, or YPbPr graphics signals. A timing diagram for this mode is shown in Figure 9.

Recommended input and output configurations are shown in Table XXXV.

Table XXXV. 4:2:2 Output Mode Select

Select	Output Mode
0	4:2:2
1	4:4:4

Table XXXVI. 4:2:2 Input/Output Configuration

Channel	Input Connection	Output Format
Red	V	U/V
Green	Y	Y
Blue	U	High Impedance

2-WIRE SERIAL CONTROL PORT

A 2-wire serial interface control interface is provided. Up to two AD9883A devices may be connected to the 2-wire serial interface, with each device having a unique address.

The 2-wire serial interface comprises a clock (SCL) and a bidirectional data (SDA) pin. The analog flat panel interface acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled high by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is low. If SDA changes state while SCL is high, the serial interface interprets that action as a start or stop sequence.

There are five components to serial bus operation:

- Start Signal
- Slave Address Byte
- Base Register Address Byte
- Data Byte to Read or Write
- Stop Signal

When the serial interface is inactive (SCL and SDA are high) communications are initiated by sending a start signal. The start signal is a high-to-low transition on SDA while SCL is high. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprise a 7-bit slave address (the first seven bits) and a single R/$\overline{W}$ Bit (the eighth bit). The R/$\overline{W}$ Bit indicates the direction of data transfer, read from (1) or write to (0) the slave device. If the transmitted slave address matches the address of the device (set by the state of the SA_{1-0} input pins in Table XXXIV, the AD9883A acknowledges by bringing SDA low on the ninth SCL pulse. If the addresses do not match, the AD9883A does not acknowledge.

Table XXXVII. Serial Port Addresses

Bit 7 A_6 (MSB)	Bit 6 A_5	Bit 5 A_4	Bit 4 A_3	Bit 3 A_2	Bit 2 A_1	Bit 1 A_0
1	0	0	1	1	0	0
1	0	0	1	1	0	1

Data Transfer via Serial Interface

For each byte of data read or written, the MSB is the first bit of the sequence.

If the AD9883A does not acknowledge the master device during a write sequence, the SDA remains high so the master can generate a stop signal. If the master device does not acknowledge the AD9883A during a read sequence, the AD9883A interprets this as "end of data." The SDA remains high so the master can generate a stop signal.

Writing data to specific control registers of the AD9883A requires that the 8-bit address of the control register of interest be written after the slave address has been established. This control register address is the base address for subsequent write operations. The base address autoincrements by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address will not increment and remains at its maximum value of 14H. Any base address higher than 14H will not produce an acknowledge signal.

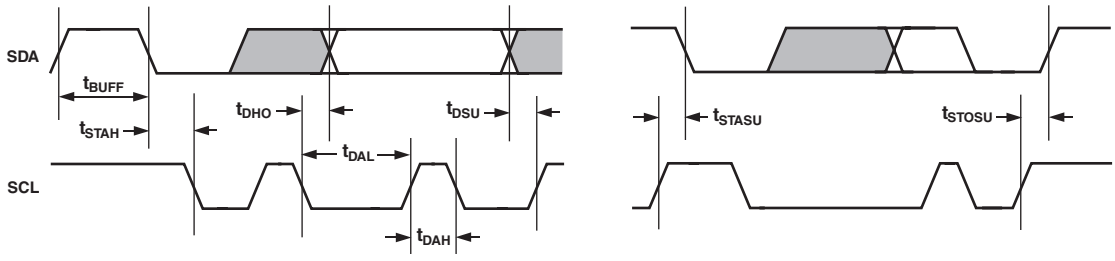

Figure 10. Serial Port Read/Write Timing

Data is read from the control registers of the AD9883A in a similar manner. Reading requires two data transfer operations:

The base address must be written with the R/$\overline{W}$ Bit of the slave address byte low to set up a sequential read operation.

Reading (the R/$\overline{W}$ Bit of the slave address byte high) begins at the previously established base address. The address of the read register autoincrements after each byte is transferred.

To terminate a read/write sequence to the AD9883A, a stop signal must be sent. A stop signal comprises a low-to-high transition of SDA while SCL is high.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

Serial Interface Read/Write Examples

Write to one control register
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = Low)
- Base Address Byte
- Data Byte to Base Address
- Stop Signal

Write to four consecutive control registers
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = Low)
- Base Address Byte
- Data Byte to Base Address
- Data Byte to (Base Address + 1)
- Data Byte to (Base Address + 2)
- Data Byte to (Base Address + 3)
- Stop Signal

Read from one control register
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = Low)
- Base Address Byte
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = High)
- Data Byte from Base Address
- Stop Signal

Read from four consecutive control registers
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = Low)
- Base Address Byte
- Start Signal
- Slave Address Byte (R/$\overline{W}$ Bit = High)
- Data Byte from Base Address
- Data Byte from (Base Address + 1)
- Data Byte from (Base Address + 2)
- Data Byte from (Base Address + 3)
- Stop Signal

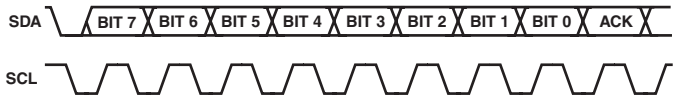

Figure 11. Serial Interface—Typical Byte Transfer

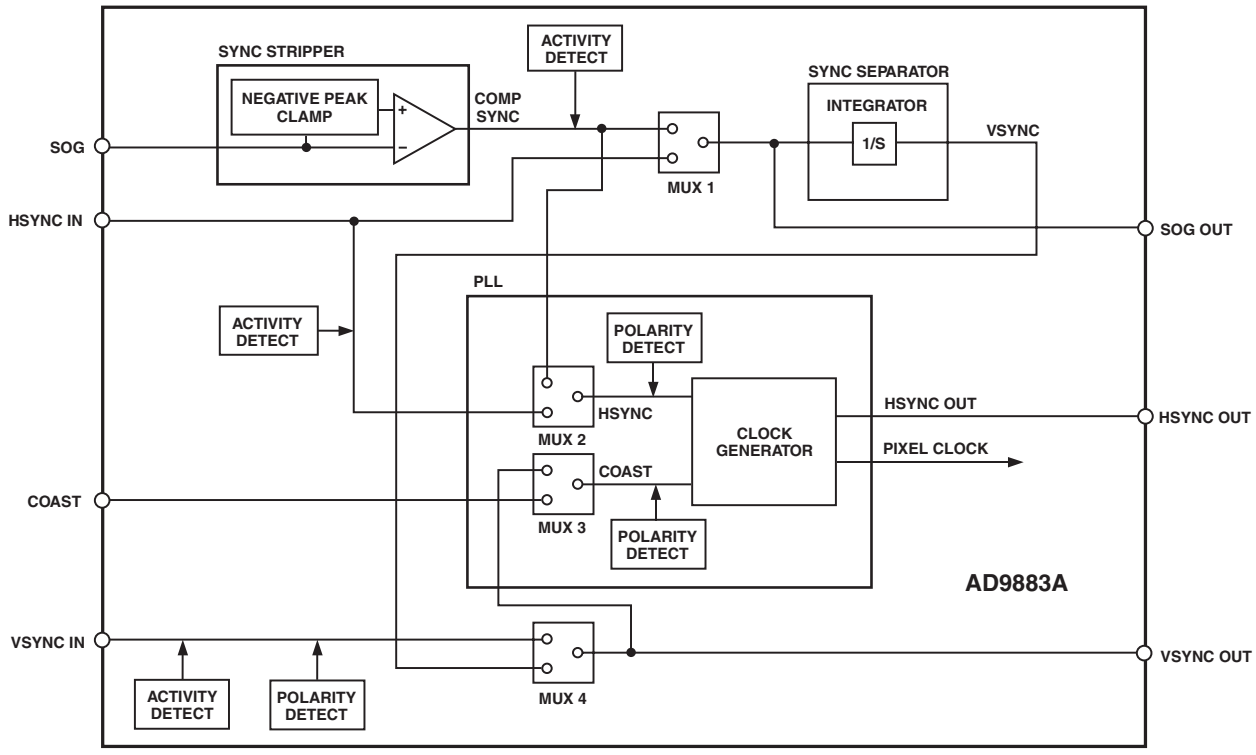

Figure 12. Sync Processing Block Diagram

Table XXXVIII. Control of the Sync Block Muxes via the Serial Register

Mux No.	Serial Bus Control Bit	Control Bit State	Result
1 and 2	0EH: Bit 3	0	Pass Hsync
		1	Pass Sync-on-Green
3	0FH: Bit 5	0	Pass Coast
		1	Pass Vsync
4	0EH: Bit 0	0	Pass Vsync
		1	Pass Sync Separator Signal

Sync Slicer

The purpose of the sync slicer is to extract the sync signal from the Green graphics channel. A sync signal is not present on all graphics systems, only those with Sync-on-Green. The sync signal is extracted from the Green channel in a two-step process. First, the SOG input is clamped to its negative peak (typically 0.3 V below the black level). Next, the signal goes to a comparator with a variable trigger level, nominally 0.15 V above the clamped level. The "sliced" sync is typically a composite sync signal containing both Hsync and Vsync.

Sync Separator

A sync separator extracts the Vsync signal from a composite sync signal. It does this through a low-pass filter-like or integrator-like operation. It works on the idea that the Vsync signal stays active for a much longer time than the Hsync signal, so it rejects any signal shorter than a threshold value, which is somewhere between an Hsync pulsewidth and a Vsync pulsewidth.

The sync separator on the AD9883A is simply an 8-bit digital counter with a 5 MHz clock. It works independently of the polarity of the composite sync signal. (Polarities are determined elsewhere on the chip.) The basic idea is that the counter counts up when Hsync pulses are present. But since Hsync pulses are relatively short in width, the counter only reaches a value of N before the pulse ends. It then starts counting down eventually reaching 0 before the next Hsync pulse arrives. The specific value of N will vary for different video modes, but will always be less than 255. For example with a 1 µs width Hsync, the counter will only reach 5 (1 µs/200 ns = 5). Now, when Vsync is present on the composite sync the counter will also count up. However, since the Vsync signal is much longer, it will count to a higher number M. For most video modes, M will be at least 255. So, Vsync can be detected on the composite sync signal by detecting when the counter counts to higher than N. The specific count that triggers detection (T) can be programmed through the serial register (11H).

Once Vsync has been detected, there is a similar process to detect when it goes inactive. At detection, the counter first resets to 0, then starts counting up when Vsync goes away. Similar to the previous case, it will detect the absence of Vsync when the counter reaches the threshold count (T). In this way, it will reject noise and/or serration pulses. Once Vsync is detected to be absent, the counter resets to 0 and begins the cycle again.

PCB LAYOUT RECOMMENDATIONS

The AD9883A is a high precision, high speed analog device. As such, to get the maximum performance out of the part, it is important to have a well laid out board. The following is a guide for designing a board using the AD9883A.

Analog Interface Inputs

Using the following layout techniques on the graphics inputs is extremely important.

Minimize the trace length running into the graphics inputs. This is accomplished by placing the AD9883A as close as possible to the graphics VGA connector. Long input trace lengths are undesirable because they pick up more noise from the board and other external sources.

Place the 75 Ω termination resistors (see Figure 1) as close to the AD9883A chip as possible. Any additional trace length between the termination resistors and the input of the AD9883A increases the magnitude of reflections, which will corrupt the graphics signal.

Use 75 Ω matched impedance traces. Trace impedances other than 75 Ω will also increase the chance of reflections.

The AD9883A has very high input bandwidth (500 MHz). While this is desirable for acquiring a high resolution PC graphics signal with fast edges, it means that it will also capture any high frequency noise present. Therefore, it is important to reduce the amount of noise that gets coupled to the inputs. Avoid running any digital traces near the analog inputs.

Due to the high bandwidth of the AD9883A, low-pass filtering the analog inputs can sometimes help to reduce noise. (For many applications, filtering is unnecessary.) Experiments have shown that placing a series ferrite bead prior to the 75 Ω termination resistor is helpful in filtering out excess noise. Specifically, the part used was the #2508051217Z0 from Fair-Rite, but each application may work best with a different bead value. Alternately, placing a 100 Ω to 120 Ω resistor between the 75 Ω termination resistor and the input coupling capacitor can also be beneficial.

Power Supply Bypassing

It is recommended to bypass each power supply pin with a 0.1 µF capacitor. The exception is when two or more supply pins are adjacent to each other. For these groupings of powers/grounds, it is necessary to have only one bypass capacitor. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin. Also, avoid placing the capacitor on the opposite side of the PC board from the AD9883A, as that interposes resistive vias in the path.

The bypass capacitors should be physically located between the power plane and the power pin. Current should flow from the power plane to the capacitor to the power pin. Do not make the power connection between the capacitor and the power pin. Placing a via underneath the capacitor pads, down to the power plane, is generally the best approach.

It is particularly important to maintain low noise and good stability of PV_D (the clock generator supply). Abrupt changes in PV_D can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by careful attention to regulation, filtering, and bypassing. It is highly desirable to provide separate regulated supplies for each of the analog circuitry groups (V_D and PV_D).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least PV_D, from a different, cleaner power source (for example, from a 12 V supply).