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Dual Interface for Flat Panel Display

AD9887A

FEATURES

Analog interface
- 170 MSPS maximum conversion rate
- Programmable analog bandwidth
- 0.5 V to 1.0 V analog input range
- 500 ps p-p PLL clock jitter at 170 MSPS
- 3.3 V power supply
- Full sync processing
- Midscale clamping
- 4:2:2 output format mode

Digital interface
- DVI 1.0-compatible interface
- 170 MHz operation (2 pixels/clock mode)
- High skew tolerance of 1 full input clock
- Sync detect for hot plugging
- Supports high bandwidth digital content protection

APPLICATIONS

RGB graphics processing
LCD monitors and projectors
Plasma display panels
Scan converters
Microdisplays
Digital TVs

GENERAL DESCRIPTION

The AD9887A offers an analog interface receiver and a digital visual interface (DVI) receiver integrated on a single chip, supports high bandwidth digital content protection (HDCP), and is software and pin-to-pin compatible with the AD9887.

Analog Interface

The complete 8-bit, 170 MSPS, monolithic analog interface is optimized for capturing RGB graphics signals from personal computers and workstations. Its 170 MSPS encode rate capability and full-power analog bandwidth of 330 MHz support resolutions of up to 1600 × 1200 (UXGA) at 60 Hz. The interface includes a 170 MHz triple ADC with internal 1.25 V reference; a phase-locked loop (PLL); and programmable gain, offset, and clamp controls. The user provides only a 3.3 V power supply, analog input, and Hsync. Three-state CMOS outputs can be powered from 2.5 V to 3.3 V. The analog interface also offers full sync processing for composite sync and sync-on-green (SOG) applications. The AD9887A on-chip PLL generates a pixel clock from Hsync with output frequencies ranging from 12 MHz to 170 MHz. PLL clock jitter is typically 500 ps p-p at 170 MSPS.

FUNCTIONAL BLOCK DIAGRAM

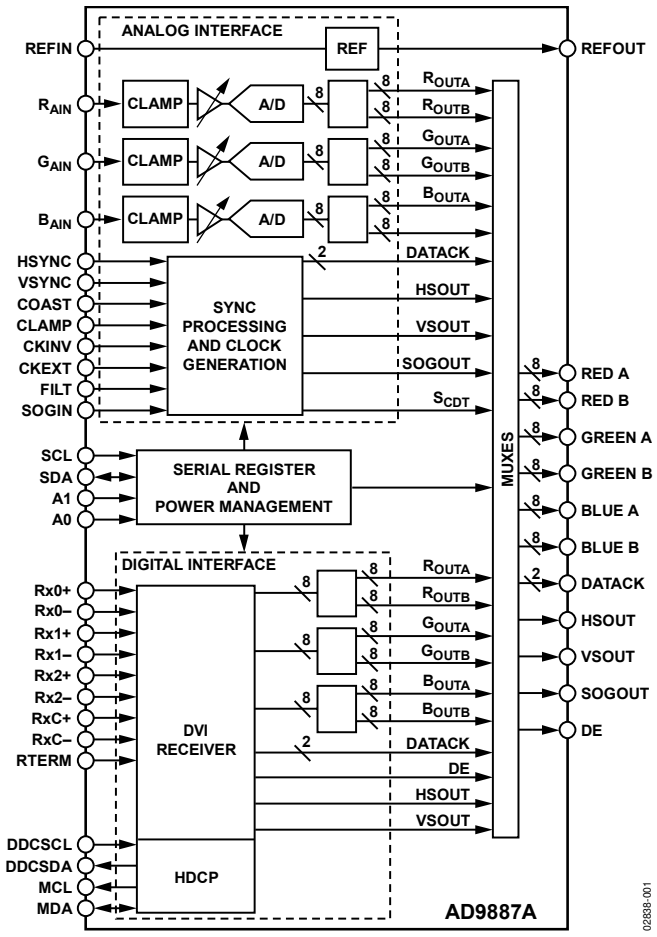

Figure 1.

Digital Interface

The AD9887A contains a DVI 1.0-compatible receiver and supports resolutions up to 1600 × 1200 (UXGA) at 60 Hz. The receiver operates with true color (24-bit) panels in one or two pixel(s) per clock mode and features an intrapair skew tolerance of up to one full clock cycle. With the inclusion of HDCP, displays can receive encrypted video content. The AD9887A allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewability of authentication during transmission, as specified by the HDCP v1.0 protocol. Fabricated in an advanced CMOS process, the AD9887A is provided in a 160-lead, surface-mount, plastic MQFP and is specified over the 0°C to 70°C temperature range. The AD9887A is also available in an RoHS compliant package.

Rev. B

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Fax: 781.461.3113

AD9887A* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-716: AD9887 Versus AD9887A Design Considerations

Data Sheet

- AD9887A: Dual Interface for Flat Panel Display Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD988x Evaluation Tools Software Program

TOOLS AND SIMULATIONS

- AD9887A CCD PLL Setting
- AD9887A IBIS Models

REFERENCE MATERIALS

Informational

- Advantiv™ Advanced TV Solutions

Technical Articles

- Analysis of Common Failures of HDMI CT

DESIGN RESOURCES

- AD9887A Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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SPECIFICATIONS

ANALOG INTERFACE

V_D = 3.3 V, V_{DD} = 3.3 V, ADC clock = maximum conversion rate, unless otherwise noted.

Table 1.

			AD9887AKS-100			AD9887AKS-140			AD9887AKS-170			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION				8			8			8		Bits
DC ACCURACY												
Differential Nonlinearity	25°C	I		±0.5	+1.15/−1.0		±0.5	+1.25/−1.0		±0.8	+1.25/−1.0	LSB
	Full	VI			+1.15/−1.0			+1.25/−1.0			+1.50/−1.0	LSB
Integral Nonlinearity	25°C	I		±0.5	±1.40		±0.5	±1.4		±1.0	±2.25	LSB
	Full	VI			±1.75			±2.5			±2.75	LSB
No Missing Codes	25°C	I		Guaranteed			Guaranteed			Guaranteed		
ANALOG INPUTS												
Voltage Range												
Minimum	Full	VI			0.5			0.5			0.5	V p-p
Maximum	Full	VI	1.0			1.0			1.0			V p-p
Gain Tempco	25°C	V		135			150			150		ppm/°C
Bias Current	25°C	IV			1			1			1	µA
	Full	IV			1			1			1	µA
Full-Scale Matching	Full	VI			8.0			8.0			8.0	% FS
Offset Adjustment Range	Full	VI	43	48	53	43	48	53	43	48	53	% FS
REFERENCE OUTPUTS												
Voltage Range	Full	V		1.3			1.3			1.3		V
Temperature Coefficient	Full	V		90			90			90		ppm/°C
SWITCHING PERFORMANCE[1]												
Max Conversion Rate	Full	VI	100			140			170			MSPS
Min Conversion Rate	Full	IV			10			10			10	MSPS
Clock-to-Data Skew, t_{SKEW}	Full	IV	−1.5		+2.5	−1.5		+2.5	−1.5		+2.5	ns
Serial Port Timing												
t_{BUFF}	Full	VI	4.7			4.7			4.7			µs
t_{STAH}	Full	VI	4.0			4.0			4.0			µs
t_{DHO}	Full	VI	250			250			250			ns
t_{DAL}	Full	VI	4.7			4.7			4.7			µs
t_{DAH}	Full	VI	4.0			4.0			4.0			µs
t_{DSU}	Full	VI	100			100			100			ns
t_{STASU}	Full	VI	4.7			4.7			4.7			µs
t_{STOSU}	Full	VI	4.0			4.0			4.0			µs
HSYNC Input Frequency	Full	IV	15		110	15		110	15		110	kHz
Max PLL Clock Rate	Full	VI	100			140			170			MHz
Min PLL Clock Rate	Full	IV			12			12			12	MHz
PLL Jitter	25°C	IV		500	700[2]		440	650[3]		370	500[4]	ps p-p
	Full	IV			1000[2]			700[3]			700[4]	ps p-p
Sampling Phase Tempco	Full	IV		10			10			10		ps/°C

Parameter	Temp	Test Level	AD9887AKS-100 Min	AD9887AKS-100 Typ	AD9887AKS-100 Max	AD9887AKS-140 Min	AD9887AKS-140 Typ	AD9887AKS-140 Max	AD9887AKS-170 Min	AD9887AKS-170 Typ	AD9887AKS-170 Max	Unit
DIGITAL INPUTS												
Voltage High, V_{IH}	Full	VI	2.6			2.6			2.6			V
Voltage Low, V_{IL}	Full	VI			0.8			0.8			0.8	V
Current High, V_{IH}	Full	IV			−1.0			−1.0			−1.0	µA
Current Low, V_{IL}	Full	IV			1.0			1.0			1.0	µA
Capacitance	25°C	V		3			3			3		pF
DIGITAL OUTPUTS												
Voltage High, V_{OH}	Full	VI	2.4			2.4			2.4			V
Voltage Low, V_{OL}	Full	VI			0.4			0.4			0.4	V
Duty Cycle DATACK, $\overline{DATACK}$	Full	IV	45	55	60	45	55	60	45	55	65	%
Output Coding				Binary			Binary			Binary		
POWER SUPPLIES												
V_D Supply Voltage	Full	IV	3.15	3.3	3.45	3.15	3.3	3.45	3.15	3.3	3.45	V
V_{DD} Supply Voltage	Full	IV	2.2	3.3	3.45	2.2	3.3	3.45	2.2	3.3	3.45	V
PV_D Supply Voltage	Full	IV	3.15	3.3	3.45	3.15	3.3	3.45	3.15	3.3	3.45	V
I_D Supply Current, V_D	25°C	V		167			185			230		mA
I_{DD} Supply Current, V_{DD}[5]	25°C	V		33			46			55		mA
IPV_D Supply Current, PV_D	25°C	V		43			43			60		mA
Total Supply Current[5]	Full	VI		243	330		274	360		345	390	mA
Power-Down Supply Current	Full	VI		90	120		90	120		90	120	mA
DYNAMIC PERFORMANCE												
Analog Bandwidth, Full Power	25°C	V		330			330			330		MHz
Transient Response	25°C	V		2			2			2		ns
Overvoltage Recovery Time	25°C	V		1.5			1.5			1.5		ns
Signal-to-Noise Ratio (SNR)[6] f_{IN} = 40.7 MHz	25°C	V		46			46			45		dB
Crosstalk	Full	V		60			60			60		dBc
THERMAL CHARACTERISTICS												
θ_{JA} Junction-to-Ambient Thermal Resistance[7]		V		37			37			37		°C/W

[1] Drive strength = 11.
[2] VCO range = 01, charge-pump current = 001, PLL divider = 1693.
[3] VCO range = 10, charge-pump current = 110, PLL divider = 1600.
[4] VCO range = 11, charge-pump current = 110, PLL divider = 2159.
[5] DEMUX = 1, DATACK and $\overline{DATACK}$ load = 10 pF, data load = 5 pF.
[6] Using external pixel clock.
[7] Simulated typical performance with package mounted to a 4-layer board.

DIGITAL INTERFACE

VD = 3.3 V, VDD = 3.3 V, clock = maximum, unless otherwise noted.

Table 2.

Parameter	Conditions	Temp	Test Level	AD9887AKS Min	Typ	Max	Unit
RESOLUTION					8		Bits
DC DIGITAL I/O SPECIFICATIONS							
High Level Input Voltage, V_{IH}		Full	VI	2.6			V
Low Level Input Voltage, V_{IL}		Full	VI			0.8	
High Level Output Voltage, V_{OH}		Full	VI	2.4			V
Low Level Output Voltage, V_{OL}		Full	VI			0.4	V
Input Clamp Voltage, V_{CINL}	I_{CL} = −18 mA		IV			GND − 0.8	V
Input Clamp Voltage, V_{CIPL}	I_{CL} = +18 mA		IV			V_{DD} + 0.8	V
Output Clamp Voltage, V_{CONL}	I_{CL} = −18 mA		IV			GND − 0.8	V
Output Clamp Voltage, V_{COPL}	I_{CL} = +18 mA		IV			V_{DD} + 0.8	V
Output Leakage Current, I_{OL}	High impedance	Full	IV	−10		+10	µA
DC SPECIFICATIONS							
Output High Drive, I_{OHD} (V_{OUT} = V_{OH})	Output drive = high	Full	IV		13		mA
	Output drive = med	Full	IV		8		mA
	Output drive = low	Full	IV		5		mA
Output Low Drive, I_{OLD} (V_{OUT} = V_{OL})	Output drive = high	Full	IV		−9		mA
	Output drive = med	Full	IV		−7		mA
	Output drive = low	Full	IV		−5		mA
DATACK High Drive, I_{OHC} (V_{OUT} = V_{OH})	Output drive = high	Full	IV		25		mA
	Output drive = med	Full	IV		12		mA
	Output drive = low	Full	IV		8		mA
DATACK Low Drive, I_{OLC} (V_{OUT} = V_{OL})	Output drive = high	Full	IV		−25		mA
	Output drive = med	Full	IV		−19		mA
	Output drive = low	Full	IV		−8		mA
Differential Input Voltage, Single-Ended Amplitude		Full	IV	75		800	mA
POWER SUPPLIES							
V_D Supply Voltage		Full	IV	3.15	3.3	3.45	V
V_{DD} Supply Voltage	Minimum value for two pixels per clock mode	Full	IV	2.2	3.3	3.45	V
PV_D Supply Voltage		Full	IV	3.15	3.3	3.45	V
I_D Supply Current[1]		25°C	V		350		mA
I_{DD} Supply Current[1, 2]		255°C	V		40		mA
IPV_D Supply Current[1]		255°C	IV		130		mA
Total Supply Current with HDCP[1, 2]			VI		520	560	mA
AC SPECIFICATIONS							
Intrapair (+ to −) Differential Input Skew, T_{DPS}		Full	IV			360	ps
Channel-to-Channel Differential Input Skew, T_{CCS}		Full	IV			1.0	Clock period
Low-to-High Transition Time for Data and Controls, D_{LHT}	Output drive = high; C_L = 10 pF	Full	IV			2.5	ns
	Output drive = med; C_L = 7 pF	Full	IV			3.1	ns
	Output drive = low; C_L = 5 pF	Full	IV			5.4	ns

Parameter	Conditions	Temp	Test Level	AD9887AKS Min	Typ	Max	Unit
Low-to-High Transition Time (D_{LHT}) for DATACK	Output drive = high; C_L = 10 pF	Full	IV			1.2	ns
	Output drive = med; C_L = 7 pF	Full	IV			1.6	ns
	Output drive = low; C_L = 5 pF	Full	IV			2.3	ns
High-to-Low Transition Time (D_{HLT}) for Data	Output drive = high; C_L = 10 pF	Full	IV			2.6	ns
	Output drive = med; C_L = 7 pF	Full	IV			3.0	ns
	Output drive = low; C_L = 5 pF	Full	IV			3.7	ns
High-to-Low Transition Time (D_{HLT}) for DATACK	Output drive = high; C_L =10 pF	Full	IV			1.4	ns
	Output drive = med; C_L = 7 pF	Full	IV			1.6	ns
	Output drive = low; C_L = 5 pF	Full	IV			2.4	ns
Clock-to-Data Skew, t_{SKEW}[3]		Full	IV	0		4.0	ns
Duty Cycle, DATACK, $\overline{DATACK}$[3]		Full	IV	45		55	% of period high
DATACK Frequency (f_{CIP})	1 pixel/clock	Full	VI	20		140	MHz
DATACK Frequency (f_{CIP})	2 pixels/clock	Full	IV	10		85	MHz

[1] The typical pattern contains a gray-scale area, output drive = high.
[2] DATACK and $\overline{DATACK}$ load = 10 pF, data load = 5 pF, and HDCP disabled.
[3] Drive strength = 11.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_D	3.6 V
V_{DD}	3.6 V
Analog Inputs	V_D to 0.0 V
VREFIN	V_D to 0.0 V
Digital Inputs	5 V to 0.0 V
Digital Output Current	20 mA
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

I. 100% production tested.

II. 100% production tested at 25°C; sample tested at specified temperatures.

III. Sample tested only.

IV. Guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at 25°C; guaranteed by design and characterization testing.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

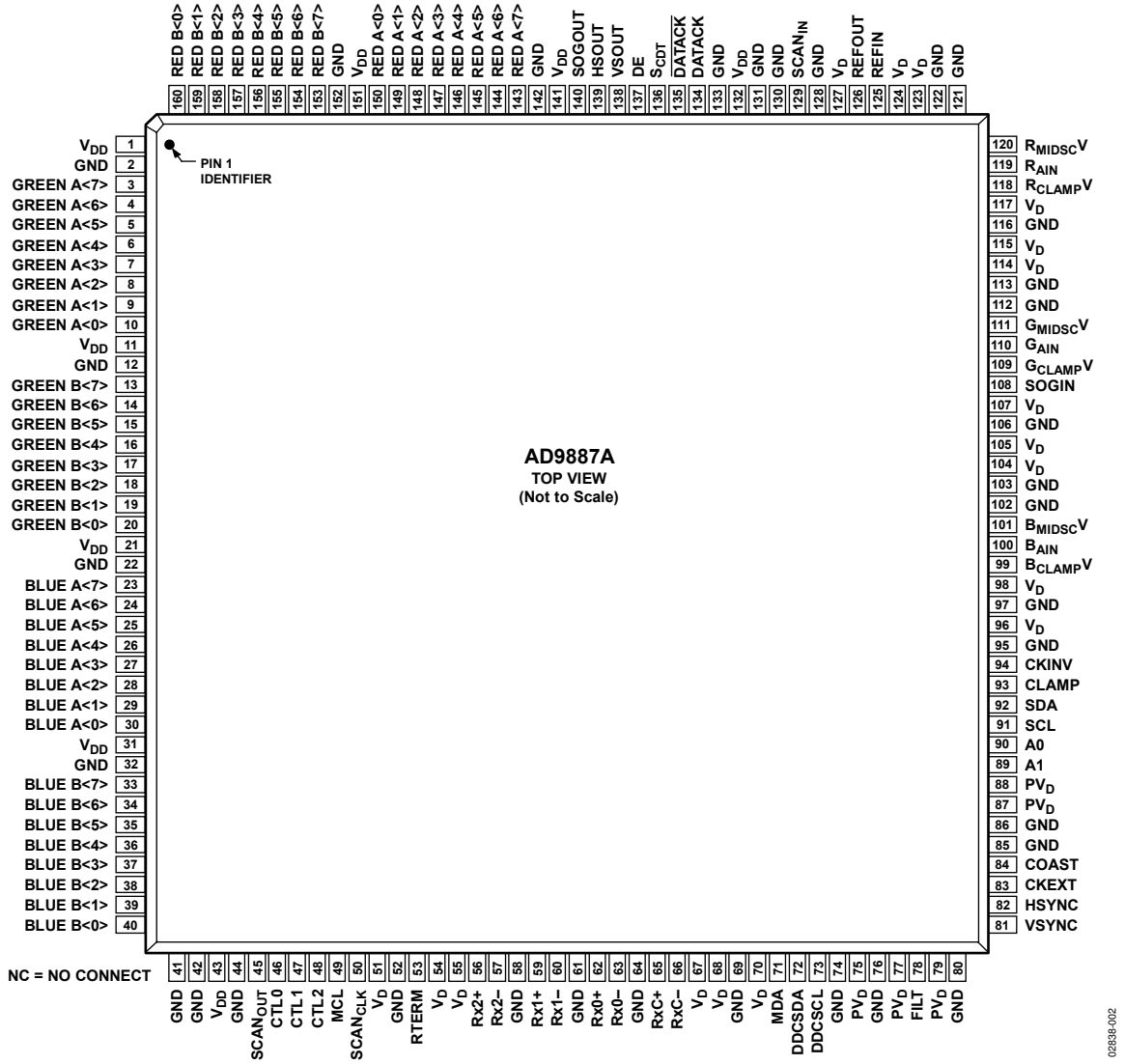

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin Type	Mnemonic	Description	Value	Pin No.	Interface
Analog Video Data Inputs	R_{AIN}	Analog Input for Red Channel	0.0 V to 1.0 V	119	Analog
	G_{AIN}	Analog Input for Green Channel	0.0 V to 1.0 V	110	Analog
	B_{AIN}	Analog Input for Blue Channel	0.0 V to 1.0 V	100	Analog
Sync/Clock Inputs	HSYNC	Horizontal Sync Input	3.3 V CMOS	82	Analog
	VSYNC	Vertical Sync Input	3.3 V CMOS	81	Analog
	SOGIN	Sync-on-Green Input	0.0 V to 1.0 V	108	Analog
	CLAMP	External Clamp Input (Optional)	3.3 V CMOS	93	Analog
	COAST	PLL Coast Signal Input (Optional)	3.3 V CMOS	84	Analog
	CKEXT	External Pixel Clock Input (to Bypass the PLL) to V_{DD} or Ground (Optional)	3.3 V CMOS	83	Analog
	CKINV	ADC Sampling Clock Invert (Optional)	3.3 V CMOS	94	Analog
Sync Outputs	HSOUT	Horizontal Sync Output	3.3 V CMOS	139	Analog/Digital
	VSOUT	Vertical Sync Output	3.3 V CMOS	138	Analog/Digital
	SOGOUT	Sync-on-Green Slicer Output or Raw Hsync	3.3 V CMOS	140	Analog
Voltage References	REFOUT	Internal Reference Output (bypass with 0.1 µF to Ground)	1.25 V	126	Analog
	REFIN	Reference Input (1.25 V ± 10%)	1.25 V ± 10%	125	Analog
Clamp Voltages	$R_{MIDSC}V$	Red Channel Midscale Clamp Voltage Output	0.5 V ± 50%	120	Analog
	$R_{CLAMP}V$	Red Channel Midscale Clamp Voltage Input	0.0 V to 0.75 V	118	Analog
	$G_{MIDSC}V$	Green Channel Midscale Clamp Voltage Output	0.5 V ± 50%	111	Analog
	$G_{CLAMP}V$	Green Channel Midscale Clamp Voltage Input	0.0 V to 0.75 V	109	Analog
	$B_{MIDSC}V$	Blue Channel Midscale Clamp Voltage Output	0.5 V ± 50%	101	Analog
	$B_{CLAMP}V$	Blue Channel Midscale Clamp Voltage Input	0.0 V to 0.75 V	99	Analog
PLL Filter	FILT	External Filter Connection (Component of PLL)		78	Analog
Power Supplies	V_D	Main Power Supply	3.3 V ± 5%	51, 54, 55, 67, 68, 70, 96, 98, 104, 105, 107, 114, 115, 117, 123, 124, 127	Analog/Digital
	V_{DD}	Output Power Supply	3.3 V ± 5%	1, 11, 21, 31, 43, 132, 141, 151	Analog/Digital
	PV_D	PLL Power Supply	3.3 V ± 5%	75, 77, 79, 87, 88	Analog/Digital
	GND	Ground	0 V	2, 12, 22, 32, 41, 42, 44, 52, 58, 61, 64, 69, 74, 76, 80, 85, 86, 95, 97, 102, 103, 106, 112, 113, 116, 121, 122, 128, 130, 131, 133, 142, 152	Analog/Digital
Serial Port	SDA	Serial Port Data I/O	3.3 V CMOS	92	Analog/Digital

Pin Type	Mnemonic	Description	Value	Pin No.	Interface
2-Wire Serial Interface	SCL	Serial Port Data Clock (100 kHz Maximum)	3.3 V CMOS	91	Analog/Digital
	A0	Serial Port Address Input 1	3.3 V CMOS	90	Analog/Digital
	A1	Serial Port Address Input 2	3.3 V CMOS	89	Analog/Digital
Data Outputs	RED B[7:0]	Data Output, Red Channel, Port B/Odd, Bit 7 is the MSB	3.3 V CMOS	153 to 160	Analog/Digital
	GREEN B[7:0]	Data Output, Green Channel, Port B/Odd	3.3 V CMOS	13 to 20	Analog/Digital
	BLUE B[7:0]	Data Output, Blue, Port B/Odd	3.3 V CMOS	33 to 40	Analog/Digital
	RED A[7:0]	Data Output, Red Channel, Port A/Even	3.3 V CMOS	143 to 150	Analog/Digital
	GREEN A[7:0]	Data Output, Green Channel, Port A/Even	3.3 V CMOS	3 to 10	Analog/Digital
	BLUE A[7:0]	Data Output, Blue Channel, Port A/Even	3.3 V CMOS	23 to 30	Analog/Digital
Data Clock Outputs	DATACK	Data Output Clock	3.3 V CMOS	134	Analog/Digital
	$\overline{\text{DATACK}}$	Data Output Clock Complement	3.3 V CMOS	135	Analog/Digital
Sync Detect	S_{CDT}	Sync Detect Output	3.3 V CMOS	136	Analog/Digital
Scan Function	$SCAN_{IN}$	Input for Scan Function	3.3 V CMOS	129	Analog/Digital
	$SCAN_{OUT}$	Output for Scan Function	3.3 V CMOS	45	Analog/Digital
	$SCAN_{CLK}$	Clock for Scan Function	3.3 V CMOS	50	Analog/Digital
Digital Video Data Inputs	Rx0+	Digital Differential Input Channel 0 True		62	Digital
	Rx0−	Digital Differential Input Channel 0 Complement		63	Digital
	Rx1+	Digital Differential Input Channel 1 True		59	Digital
	Rx1−	Digital Differential Input Channel 1 Complement		60	Digital
	Rx2+	Digital Differential Input Channel 2 True		56	Digital
	Rx2−	Digital Differential Input Channel 2 Complement		57	Digital
Digital Video Clock Inputs	RxC+	Digital Differential Data Clock True		65	Digital
	RxC−	Digital Differential Data Clock Complement		66	Digital
Data Enable	DE	Data Enable	3.3 V CMOS	137	Digital
Control Bit	CTL0, CTL1, CTL2	Digital Control Outputs	3.3 V CMOS	46 to 48	Digital
Termination Control	RTERM	Internal Termination Resistance Set Pin		53	Digital
HDCP	DDCSCL	HDCP Slave Serial Port Data Clock	3.3 V CMOS	73	Digital
	DDCSDA	HDCP Slave Serial Port Data I/O	3.3 V CMOS	72	Digital
	MCL	HDCP Master Serial Port Data Clock	3.3 V CMOS	49	Digital
	MDA	HDCP Master Serial Port Data I/O	3.3 V CMOS	71	Digital

PIN FUNCTION DETAILS—PINS SHARED BETWEEN DIGITAL AND ANALOG INTERFACES

Sync Outputs

HSOUT Horizontal Sync Output

The horizontal sync output is a reconstructed version of the video Hsync, phase-aligned with DATACK. The polarity of this output can be controlled via a serial bus bit. In analog interface mode, the placement and duration are variable. In digital interface mode, the placement and duration are set by the graphics transmitter.

VSOUT Vertical Sync Output

The Vsync is separated from a composite signal or a direct pass-through of the Vsync input. The polarity of this output can be controlled via a serial bus bit. The placement and duration in all modes are set by the graphics transmitter.

2-Wire Serial Port

SDA Serial Port Data I/O

SCL Serial Port Data Clock

A0 Serial Port Address Input 1

A1 Serial Port Address Input 2

For a full description of the 2-wire serial register and how it works, see the 2-Wire Serial Control Port section.

Data Outputs

RED A Data Output, Red Channel, Port A/Even

RED B Data Output, Red Channel, Port B/Odd

GREEN A Data Output, Green Channel, Port A/Even

GREEN B Data Output, Green Channel, Port B/Odd

BLUE A Data Output, Blue Channel, Port A/Even

BLUE B Data Output, Blue Channel, Port B/Odd

These outputs are the main data outputs. Bit 7 is the MSB. These outputs are shared between the two interfaces.

Data Clock Outputs

DATACK Data Output Clock

$\overline{\text{DATACK}}$ Data Output Clock Complement

Like the data outputs, the data clock outputs are shared between the two interfaces. They also behave differently, depending on which interface is active. See the Theory of Operation and Design Guide—Analog Interface and the Theory of Operation—Digital Interface sections for details on how these pins behave.

Sync Detect

S_{CDT} Chip Active/Inactive Detect Output

The logic for the S_{CDT} pin is analog interface HSYNC detection or digital interface DE detection. Therefore, the S_{CDT} pin switches to logic low under two conditions: when neither interface is active, or when the chip is in full power-down mode. The data outputs are automatically set to three-state when S_{CDT} is low. This pin can be read by a controller to identify periods of inactivity.

Scan Function

$SCAN_{IN}$ Data Input for Scan Function

By using the scan function, 48 bits of data can be loaded into the data outputs. Data is input serially through this pin, clocked with the $SCAN_{CLK}$ pin, and comes through the outputs as parallel words. This function is useful for loading known data into a graphics controller chip for testing purposes.

$SCAN_{OUT}$ Data Output for Scan Function

The data input serially into the $SCAN_{IN}$ register can be read through this pin. Data is read on a FIFO basis and is clocked via the $SCAN_{CLK}$ pin.

$SCAN_{CLK}$ Data Clock for Scan Function

This pin clocks the data for the scan function. It controls both data input and output.

Power Supplies

V_D Main Power Supply

These pins supply power to the main elements of the circuit. They should be filtered to be as quiet as possible.

V_{DD} Digital Output Power Supply

These supply pins are identified separately from the V_D pins; therefore, special care can be taken to minimize output noise transferred into the sensitive analog circuitry.

If the AD9887A is interfacing with lower voltage logic, V_{DD} can be connected to a lower supply voltage (as low as 2.2 V) for compatibility.

PV_D Clock Generator Power Supply

The most sensitive portion of the AD9887A is the clock generation circuitry. These pins provide power to the clock PLL and help the user design for optimal performance. The designer should provide noise-free power to these pins.

GND Ground

This is the ground return for all circuitry on the chip. It is recommended that the application circuit board have a single, solid ground plane.

PIN FUNCTION DETAILS—ANALOG INTERFACE

Analog Video Data Inputs

R_{AIN} Analog Input for Red Channel

G_{AIN} Analog Input for Green Channel

B_{AIN} Analog Input for Blue Channel

These are the high impedance inputs that accept graphics signals from the red, green, and blue channels, respectively. For RGB, the three channels are identical and can be used for any color, but colors are assigned for convenient reference. For proper 4:2:2 formatting in a YUV application, the Y channel must be connected to the G_{AIN} input, U must be connected to the B_{AIN} input, and V must be connected to the R_{AIN} input.

These pins accommodate input signals ranging from 0.5 V to 1.0 V full scale. Signals should be ac-coupled to these pins to support clamp operation.

External Inputs

HSYNC Horizontal Sync Input

This input receives a logic signal that establishes the horizontal timing reference and provides the frequency reference for pixel clock generation.

The logic sense of this pin is controlled by Serial Register 0x0F, Bit 7 (Hsync polarity). Only the leading edge of Hsync is active; the trailing edge is ignored. When Hsync polarity = 0, the falling edge of Hsync is used. When Hsync polarity = 1, the rising edge is active.

The input includes a Schmitt trigger for noise immunity with a nominal input threshold of 1.5 V.

Electrostatic discharge (ESD) protection diodes conduct heavily if this pin is driven more than 0.5 V above the maximum tolerance voltage (3.3 V) or more than 0.5 V below ground.

VSYNC Vertical Sync Input

This is the input for vertical sync.

Sync/Clock Inputs

SOGIN Sync-on-Green Input

This input is provided to assist with processing signals with embedded sync, typically on the green channel. The pin is connected to a high speed comparator with an internally generated threshold that is 0.15 V above the negative peak of the input signal.

When connected to an ac-coupled graphics signal with embedded sync, it produces a noninverting digital output on SOGOUT.

When not used, leave this input unconnected. For more details on this function and how it should be configured, refer to the Sync-on-Green Input section.

CLAMP External Clamp Input (Optional)

This logic input can be used to define the time during which the input signal is clamped to the reference dc level (ground for RGB, midscale for YUV). It should be used when the reference dc level is known to be present on the analog input channels, typically during a period called the back porch of the graphics signal following Hsync. The CLAMP pin is enabled by setting control bit EXTCLMP to 1 (the default at power-up is 0). When disabled, this pin is ignored and the clamp timing is determined internally by counting the delay and duration from the trailing edge of the HSYNC input. The logic sense of this pin is controlled by CLAMPOL. When not used, this pin must be grounded and EXTCLMP must be programmed to 0.

COAST Clock Generator Coast Input (Optional)

This input can be used to stop the pixel clock generator from synchronizing with Hsync while maintaining the clock at its current frequency and phase. This is useful when processing signals from sources that fail to produce horizontal sync pulses when in the vertical interval. The coast signal is generally not required for PC-generated signals. For applications requiring coast, it is provided through the internal coast found in the sync processing engine.

The logic sense of this pin is controlled by coast polarity. When not used, this pin can be grounded with coast polarity programmed to 1, or tied high with coast polarity programmed to 0. Coast polarity defaults to 1 at power-up.

CKEXT External Clock Input (Optional)

This pin can be used to provide an external clock to the AD9887A in place of the clock internally generated from HSYNC. It is enabled by programming CKEXT to 1. When an external clock is used, all other internal functions, including the clock phase adjustment, operate normally. When not used, this pin should be tied to V_{DD} or to ground and CKEXT should be programmed to 0.

CKINV Sampling Clock Inversion (Optional)

This pin can be used to invert the pixel sampling clock, which has the effect of shifting the sampling phase 180°. This supports the alternate pixel sampling mode, wherein higher frequency input signals (up to 340 MPPS) can be captured by sampling the odd pixels and capturing the even pixels on the subsequent frame.

This pin should be used only during blanking intervals (typically vertical blanking), because it might produce several samples of corrupted data during the phase shift.

CKINV should be grounded when not used.

Either or both signals can be used, depending on the timing mode and the interface design used.

Sync Outputs

HSOUT Horizontal Sync Output

A reconstructed, phase-aligned version of the HSYNC input. Both the polarity and duration of this output can be programmed via serial bus registers.

By maintaining alignment with DATACK, $\overline{\text{DATACK}}$, and Data, data timing with respect to horizontal sync can be determined.

SOGOUT Sync-on-Green Slicer Output

This pin can be programmed to output either the composite sync output from the sync-on-green slicer comparator or an unprocessed, but delayed, version of the HSYNC input. See the sync processing block diagram (Figure 43) to see how this pin is connected.

Voltage References

REFOUT Internal Reference Output

This is the output from the internal 1.25 V band gap reference. This output is intended to drive relatively light loads. It can drive the AD9887A reference input directly, but should be externally buffered if it is used to drive other loads, as well.

The absolute accuracy of this output is ±4%, and the temperature coefficient is ±50 ppm, which is adequate for most AD9887A applications. If higher accuracy is required, an external reference can be used instead. When using an external reference, connect this pin to ground through a 0.1 µF capacitor.

REFIN Reference Input

The reference input accepts the master reference voltage for all AD9887A internal circuitry (1.25 V ± 10%). It can be driven directly by the REFOUT pin. Its high impedance presents a very light load to the reference source.

This pin should always be bypassed to ground with a 0.1 µF capacitor.

PLL Filter

FILT External Filter Connection

For proper operation, the pixel clock generator, PLL, requires an external filter. Connect the filter shown in Figure 11 to this pin. For optimal performance, minimize noise and parasitics on this node.

Data Outputs

RED A Data Output, Red Channel, Port A/Even

RED B Data Output, Red Channel, Port B/Odd

GREEN A Data Output, Green Channel, Port A/Even

GREEN B Data Output, Green Channel, Port B/Odd

BLUE A Data Output, Blue Channel, Port A/Even

BLUE B Data Output, Blue Channel, Port B/Odd

These are the main data outputs. Bit 7 is the MSB.

Each channel has two ports. When the part is operated in single-channel mode (DEMUX = 0), all data presented to Port A and Port B is placed in a high impedance state. Programming demux to 1 establishes the dual-channel mode, wherein alternate pixels are presented to the Port A and Port B of each channel. These appear simultaneously; two pixels are presented at the time of every second input pixel when PAR is set to 1 (parallel mode). When PAR is set to 0, pixel data appears alternately on the two ports, one new sample with each incoming pixel (interleaved mode).

In dual-channel mode, the first pixel after Hsync is routed to Port A. The second pixel goes to Port B, the third to Port A, and so on.

The delay from pixel sampling time to output is fixed. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The DATACK, $\overline{\text{DATACK}}$, and HSOUT outputs are also moved; therefore, the timing relationship among the signals is maintained.

$R_{MIDSC}V$ Red Channel Midscale Clamp Voltage Output

$G_{MIDSC}V$ Green Channel Midscale Clamp Voltage Output

$B_{MIDSC}V$ Blue Channel Midscale Clamp Voltage Output

$R_{CLAMP}V$ Red Channel Midscale Clamp Voltage Input

$G_{CLAMP}V$ Green Channel Midscale Clamp Voltage Input

$B_{CLAMP}V$ Blue Channel Midscale Clamp Voltage Input

These pins are part of the circuit that provides a voltage reference for midscale clamping used in the capture of YUV and YPbPr input signals. These pins should be grounded through 0.1 µF capacitors, as shown in Figure 4.

Data Clock Outputs

DATACK Data Output Clock

$\overline{\text{DATACK}}$ Data Output Clock Complement

These differential data clock output signals are used to strobe the output data and HSOUT into external logic.

These signals are produced by the internal clock generator and are synchronous with the internal pixel sampling clock.

When the AD9887A is operated in single-channel mode, the output frequency is equal to the pixel sampling frequency. When the AD9887A is operated in dual-channel mode, the clock frequency is half the pixel frequency.

When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The Data, DATACK, $\overline{\text{DATACK}}$, and HSOUT outputs are moved; therefore, the timing relationship among the signals is maintained.

PIN FUNCTION DETAILS—DIGITAL INTERFACE

Digital Video Data Inputs

Rx0+ Digital Differential Input Channel 0 True

Rx0− Digital Differential Input Channel 0 Complement

Rx1+ Digital Differential Input Channel 1 True

Rx1− Digital Differential Input Channel 1 Complement

Rx2+ Digital Differential Input Channel 2 True

Rx2− Digital Differential Input Channel 2 Complement

These pins receive three pairs of differential, low voltage, swing input pixel data from a digital graphics transmitter.

Digital Video Clock Inputs

RxC+ Digital Differential Data Clock True

RxC− Digital Differential Data Clock Complement

These pins receive the differential, low voltage, swing input pixel clock from a digital graphics transmitter.

Termination Control

R_{TERM} Internal Termination Set Pin

This pin is used to set the termination resistance for all digital interface high speed inputs. To set this pin, place a resistor of 10 times the desired input termination resistance between this pin (Pin 53) and the ground supply. Typically, the value of this resistor should be 500 Ω.

Data Enable

DE Data Enable

This pin outputs the state of data enable (DE). The AD9887A decodes DE from the incoming stream of data. The DE signal is high during active video and low when there is no active video.

HDCP

DDCSCL HDCP Slave Serial Port Data Clock

For use in communicating with the HDCP-enabled DVI transmitter.

DDCSDA HDCP Slave Serial Port Data I/O

For use in communicating with the HDCP-enabled DVI transmitter.

MCL HDCP Master Serial Port Data Clock

Connects the EEPROM for reading the encrypted HDCP keys.

MDA HDCP Master Serial Port Data I/O

Connects the EEPROM for reading the encrypted HDCP keys.

CTL Digital Control Outputs

These pins output the control signals for the red and green channels. CTL0 and CTL1 correspond to the red channel input, and CTL2 and CTL3 correspond to the green channel input.

THEORY OF OPERATION AND DESIGN GUIDE—ANALOG INTERFACE

GENERAL DESCRIPTION

The AD9887A is a fully integrated solution for capturing analog RGB signals and digitizing them for display on flat panel monitors or projectors. The device is ideal for implementing a computer interface in HDTV monitors or for serving as the front end to high performance video scan converters.

Implemented in a high performance CMOS process, the interface can capture signals with pixel rates of up to 170 MHz, or of up to 340 MHz with an alternate pixel sampling mode.

The AD9887A includes all necessary input buffering, signal dc restoration (clamping), offset and gain (brightness and contrast) adjustment, pixel clock generation, sampling phase control, and output data formatting. All controls are programmable via a 2-wire serial interface. Full integration of these sensitive analog functions makes system design straightforward and less sensitive to the physical and electrical environment.

With an operating temperature range of 0°C to 70°C, the device requires no special environmental considerations.

INPUT SIGNAL HANDLING

The AD9887A has three high impedance analog input pins for the red, green, and blue channels that accommodate signals ranging from 0.5 V to 1.0 V p-p.

Signals are typically brought onto the interface board via a DVI-I connector, a 15-lead D connector, or BNC connectors. The AD9887A should be located as close as is practical to the input connector. Signals should be routed via matched-impedance traces (normally 75 Ω) to the IC input pins.

At this point, the signal should be resistively terminated (75 Ω to the signal ground return) and capacitively coupled to the AD9887A inputs through 47 nF capacitors. These capacitors form part of the dc-restoration circuit (see Figure 3).

In an ideal world of perfectly matched impedances, the best performance would be obtained with the widest possible signal bandwidth. The wide bandwidth inputs of the AD9887A (330 MHz) would track the input signal continuously as it moves from one pixel level to the next and would digitize the pixel during a long, flat pixel time. In many systems, however, there are mismatches, reflections, and noise that result in excessive ringing and distortion of the input waveform. This makes it difficult to establish a sampling phase that provides good image quality. A small inductor in series with the input can be effective in rolling off the input bandwidth slightly and providing a high quality signal over a wider range of conditions. Using a Fair-Rite #2508051217Z0 high speed signal chip bead inductor in the circuit of Figure 3 provides good results in most applications.

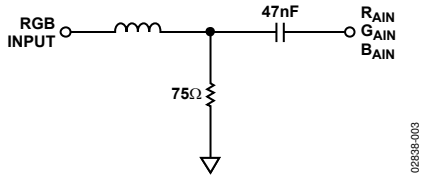

Figure 3. Analog Input Interface Circuit

HSYNC AND VSYNC INPUTS

The AD9887A receives a horizontal sync signal and uses it to generate the pixel clock and clamp timing. It is possible to operate the AD9887A without applying Hsync (using an external clock), but several of the chip's features are unavailable. Therefore, it is recommended to provide Hsync. It can be in the form of either a sync signal directly from the graphics source or a preprocessed TTL- or CMOS-level signal.

The HSYNC input includes a Schmitt-trigger buffer and is capable of handling signals that have long rise times with superior noise immunity. In typical PC-based graphics systems, the sync signals are simply TTL-level drivers feeding unshielded wires in the monitor cable. As such, no termination is required or desired.

When the VSYNC input is selected as the source for Vsync, it is used for coast generation and passed through to the VSOUT pin.

Serial Control Port

The serial control ports are designed for 3.3 V logic. If there are 5 V drivers on the bus, the serial control port pins should be protected with 150 Ω series resistors placed between the pull-up resistors and the input pins.

Output Signal Handling

The digital outputs are designed and specified to operate from a 3.3 V power supply (V_{DD}), but can operate with a V_{DD} as low as 2.5 V for compatibility with 2.5 V logic.

CLAMPING

RGB Clamping

To digitize the incoming signal properly, adjust the dc offset of the input to fit the range of the on-board ADCs.

Most graphics systems produce RGB signals with black at ground and white at approximately 0.75 V. However, if sync signals are embedded in the graphics, the sync tip is often at ground, the black level is at 300 mV, and the white level is at approximately 1.0 V. Some common RGB line amplifier boxes use emitter-follower buffers to split signals and increase drive capability. This introduces a 700 mV dc offset to the signal. Clamping removes this offset to allow proper capture.

The key to clamping is to identify a time when the graphics system is known to be producing a black signal. Originating from CRT displays, the electron beam is blanked by sending a black level during horizontal retrace to prevent disturbing the image. Most graphics systems maintain this format of sending a black level between active video lines.

An offset is then introduced that results in the ADCs producing a black output (Code 0x00) when the known black input is present. The offset remains in place when other signal levels are processed, and the entire signal is shifted to eliminate offset errors.

In systems with embedded sync, a blacker-than-black signal (Hsync) is produced briefly to signal the CRT that it is time to begin a retrace. For obvious reasons, it is important to avoid clamping on the tip of Hsync. Fortunately, there is virtually always a period following Hsync, called the back porch, when a good black reference is provided. This is the time when clamping should be done.

The clamp timing can be established by using the CLAMP pin at the appropriate time (with EXTCLMP = 1). The polarity of this signal is set by the clamp polarity bit.

An easier method of clamp timing uses the AD9887A internal clamp timing generator. The clamp placement register is programmed with the number of pixel clocks that should pass after the trailing edge of Hsync before clamping starts. A second register (clamp duration) sets the duration of the clamp. These are both 8-bit values, providing considerable flexibility in clamp generation. The clamp timing is referenced to the trailing edge of Hsync, and the back porch (black reference) always follows Hsync. To establish clamping, set the clamp placement to 0x08 (to provide eight pixel periods for the graphics signal to stabilize after sync) and set the clamp duration to 0x14 (to allow the clamp 20 pixel periods to re-establish the black reference).

The value of the external input coupling capacitor affects the performance of the clamp. If the value is too small, there is an amplitude change during a horizontal line time (between clamping intervals). If the capacitor is too large, it takes an excessively long time for the clamp to recover from a large change in incoming signal offset. The recommended value (47 nF) results in recovery from a step error of 100 mV to within ½ LSB in 10 lines, using a clamp duration of 20 pixel periods on a 60 Hz SXGA signal.

YUV Clamping

YUV signals are slightly different from RGB signals in that the dc-reference level (black level in RGB signals) is at the midpoint of the U and V video signals. For these signals, it may be necessary to clamp to the midscale range of the ADC range (0x80), rather than to the bottom of the ADC range (0x00).

Clamping to midscale, rather than to ground, can be accomplished by setting the clamp select bits in the serial bus register. Each of the three converters has its own selection bit so that it can be clamped to either midscale or ground independently. These bits (Bit 0 to Bit 2) are located in Register 0x0F.

The midscale reference voltage that each ADC clamps to is independently provided on the $R_{MIDSC}V$, $G_{MIDSC}V$, and $B_{MIDSC}V$ pins. Each converter must have its own midscale reference, because both offset adjustment and gain adjustment for each converter affect the dc level of midscale.

During clamping, the Y and V converters are clamped to their respective midscale reference inputs. These inputs are Pin $B_{CLAMP}V$ and Pin $R_{CLAMP}V$ for the U and V converters, respectively. The typical connections for both RGB and YUV clamping are shown in Figure 4. Note that even if midscale clamping is not required, all midscale voltage outputs should be connected to ground through a 0.1 µF capacitor.

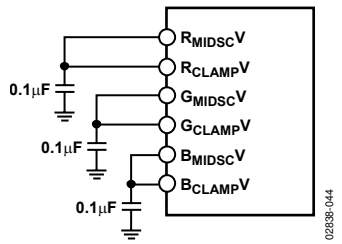

Figure 4. Typical Clamp Configuration for RGB and YUV Applications

GAIN AND OFFSET CONTROL

A block diagram of the gain and offset control integrated with each ADC is shown in Figure 5.

The AD9887A can accommodate input signals of 0.5 V to 1.0 V full scale. The full-scale range is set in three 8-bit registers (red gain, green gain, and blue gain).

Code 0 gives the minimum input range (a maximum of 0.5 V); Code 255 corresponds to the maximum input range (a minimum of 1.0 V). Increasing the gain setting results in an image with less contrast.

The offset control shifts the entire input range, resulting in a change in image brightness. Three 7-bit registers (red offset, green offset, and blue offset) provide independent settings for each channel.

The offset controls provide a ±63 LSB adjustment range. This range is connected with the full-scale range; therefore, if the input range is doubled (from 0.5 V to 1.0 V), the offset step size is also doubled (from 2 mV per step to 4 mV per step).

Figure 6 and Figure 7 illustrate the interaction of gain and offset controls. The magnitude of an LSB in offset adjustment is proportional to the full-scale range, which is controlled by the gain setting. Therefore, changing the full-scale range changes the offset (see Figure 6). The change is minimal if the offset setting is near midscale. When changing the offset, the full-scale range is not affected, but the full-scale level is shifted by the same amount as the zero-scale level.

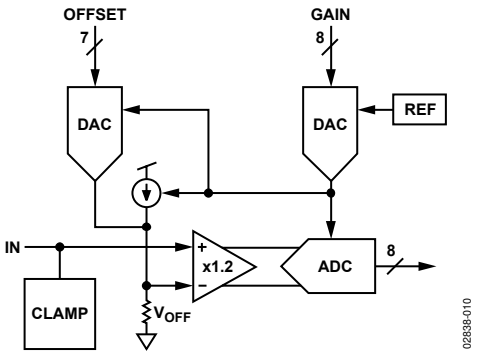

Figure 5. ADC Block Diagram (Single-Channel Output)

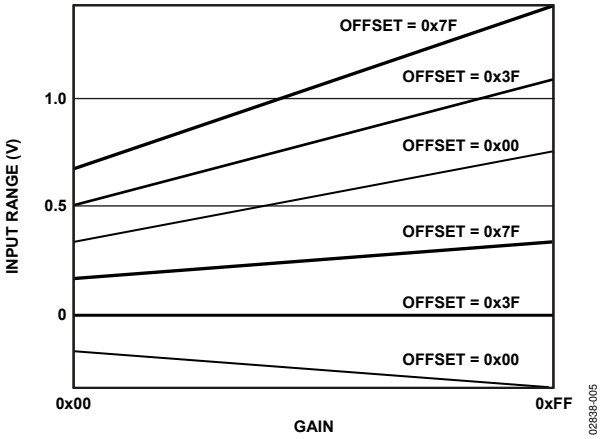

Figure 6. Gain and Offset Control

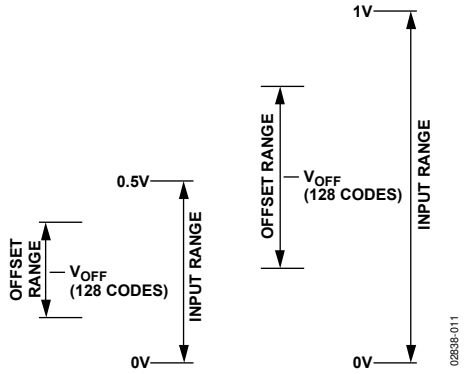

Figure 7. Relationship of Offset Range to Input Range

SYNC-ON-GREEN INPUT

The sync-on-green input operates in two steps. First, with the aid of a negative peak detector, it sets a baseline clamp level from the incoming video signal. Second, it sets the sync trigger level (nominally 150 mV above the negative peak). The exact trigger level is variable and can be programmed via Register 0x11. The sync-on-green input must be ac-coupled to the green analog input through its own capacitor, as shown in Figure 8.

The value of the capacitor must be 1 nF ± 20%. If sync-on-green is not used, this connection is not required and SOGIN should be left unconnected. (Note that the sync-on-green signal is always negative polarity.) See the Theory of Operation—Sync Processing section for more information.

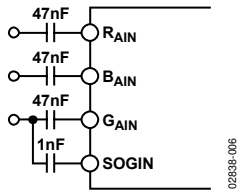

Figure 8. Typical Clamp Configuration for RGB and YUV Applications

CLOCK GENERATION

A phase-locked loop (PLL) is used to generate the pixel clock. The HSYNC input provides a reference frequency for the PLL. A voltage-controlled oscillator (VCO) generates a much higher pixel clock frequency. This is divided by the PLL divide value (MSBs in Register 0x01 and LSBs in Register 0x02) and phase compared with the HSYNC input. Any error is used to shift the VCO frequency and maintain lock between the two signals.

The stability of this clock is important for providing the clearest, most stable image. During each pixel time, there is a period when the signal slews from the old pixel amplitude and settles at its new value. Then, the input voltage is stable until the signal slews to a new value (see Figure 9). The ratio of the slewing time to the stable time is a function of the bandwidth of the graphics DAC, the bandwidth of the transmission system (cable and termination), and the overall pixel rate. Clearly, if the dynamic characteristics of the system remain fixed, the slewing and settling times are likewise fixed. Subtract these times from the total pixel period to determine the stable period. At higher pixel frequencies, both the total cycle time and stable pixel time are shorter.

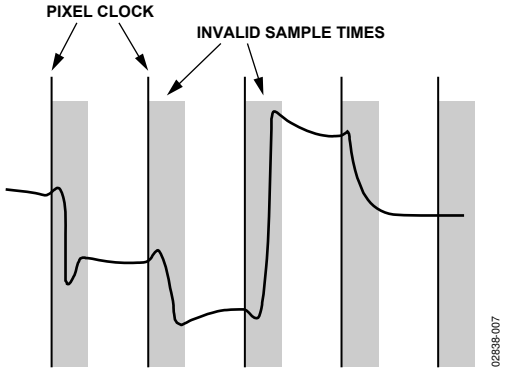

Figure 9. Pixel Sampling Times

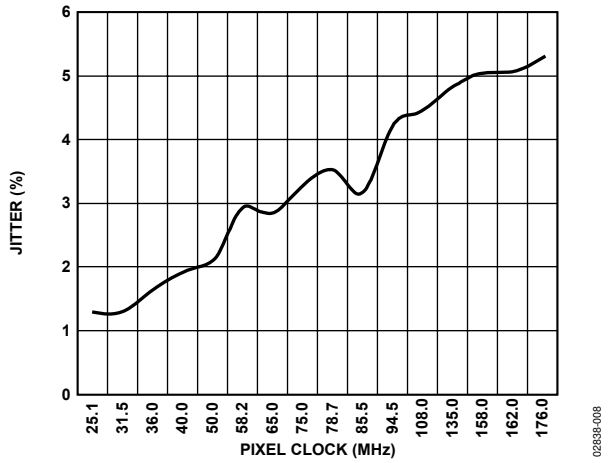

Figure 10. Pixel Clock Jitter vs. Frequency

Any jitter in the clock reduces the precision with which the sampling time can be determined and, thus, must be subtracted from the stable pixel time. The AD9887A clock generation circuit is designed to minimize jitter to less than 6% of the total pixel time in all operating modes, making its effect on valid sampling time negligible (see Figure 10).

The PLL characteristics are determined by the loop-filter design, the PLL charge-pump current, and the VCO range setting. The loop-filter design is illustrated in Figure 11. Recommended settings of VCO range and charge-pump current for VESA standard display modes are listed in Table 7.

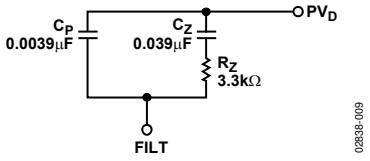

Figure 11. PLL Loop-Filter Detail

The following programmable registers are provided to optimize the performance of the PLL:

- The 12-Bit Divisor Register. The input Hsync frequencies range from 15 kHz to 110 kHz. The PLL multiplies the frequency of the Hsync signal, producing pixel clock frequencies in the range of 12 MHz to 170 MHz. The divisor register controls the exact multiplication factor. This register can be set to any value between 221 and 4095. (The divide ratio used is the programmed divide ratio plus one.)
- The 2-Bit VCO Range Register. To lower the sensitivity of the output frequency to noise on the control signal, the VCO operating frequency range is divided into four overlapping regions. The VCO range register sets this operating range. Because there are only three possible regions, just 2 LSBs of the VCO range register are used. The frequency ranges for the lowest and highest regions are shown in Table 5.

Table 5. VCO Frequency Ranges

PV1	PV0	Pixel Clock Range (MHz)
0	0	12 to 37
0	1	37 to 74
1	0	74 to 140
1	1	140 to 170

- The 3-Bit Charge-Pump Current Register. This register allows the current that drives the low-pass loop filter to be varied. The possible current values are listed in Table 6.

Table 6. Charge-Pump Current/Control Bits

Ip2	Ip1	Ip0	Current (µA)
0	0	0	50
0	0	1	100
0	1	0	150
0	1	1	250
1	0	0	350
1	0	1	500
1	1	0	750
1	1	1	1500

- The 5-Bit Phase Adjust Register. The phase of the generated sampling clock can be shifted to locate an optimum sampling point within a clock cycle. The phase-adjust register provides 32 phase-shift steps of 11.25° each. The Hsync signal with an identical phase shift is available through the HSOUT pin. Phase adjustment is operational even if the pixel clock is provided externally. The COAST signal allows the PLL to continue to run at the same frequency in the absence of the incoming Hsync signal. This can be used during the vertical sync period or any other time that the Hsync signal is unavailable. The polarity of the coast signal can be set through the COAST polarity bit, and the polarity of the Hsync signal can be set through the HSYNC polarity bit. If not using automatic polarity detection, set the HSYNC and COAST polarity bits to match the polarity of their respective signals.

Table 7. Recommended VCO Range and Charge-Pump Current Settings for Standard Display Formats

Standard	Resolution	Refresh Rate (Hz)	Horizontal Frequency (kHz)	Pixel Rate (MHz)	VCORNGE	CURRENT
VGA	640 × 480	60	31.5	25.175	00	011
		72	37.7	31.500	00	100
		75	3735	31.500	00	100
		85	43.3	36.000	00	101
SVGA	800 × 600	56	35.1	36.000	00	101
		60	3739	40.000	01	011
		72	4831	50.000	01	011
		75	46.9	49.500	01	011
		85	53.7	56.250	01	100
XGA	1024 × 768	60	48.4	65.000	01	101
		70	56.5	75.000	10	011
		75	60.0	78.750	10	011
		80	64.0	85.500	10	011
		85	68.3	94.500	10	100
SXGA	1280 × 1024	60	64.0	108.000	10	100
		75	80.0	135.000	10	101
		85	91.1	157.500	11	101
UXGA	1600 × 1200	60	75.0	162.000	10	101
TV	480i	60	15.75	13.51	00	001
	480p	60	31.47	27	00	100
	720p	60	45.0	74.250	10	011
	1080i	60	33.75	74.250	10	010
	1080p	60	33.75	148.5	11	011

ALTERNATE PIXEL SAMPLING MODE

Logic 1 input on CKINV (Pin 94) inverts the nominal ADC clock. CKINV can be switched between frames to implement the alternate pixel sampling mode. This allows higher effective image resolution to be achieved at lower pixel rates, but with lower frame rates.

On one frame, even pixels are digitized. On the subsequent frame, odd pixels are sampled. By reconstructing the entire frame in the graphics controller, a complete image can be reconstructed. This is very similar to the interlacing process used in broadcast television systems, but the interlacing is vertical instead of horizontal. The frame data is presented to the display at the full desired refresh rate (usually 60 Hz) so that no flicker artifacts are added.

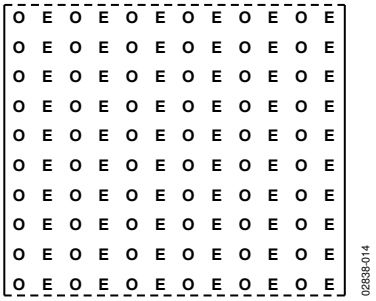

Figure 12. Odd and Even Pixels in a Frame

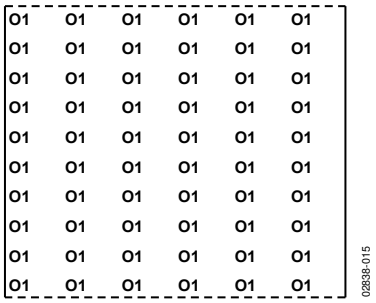

Figure 13. Odd Pixels from Frame 1

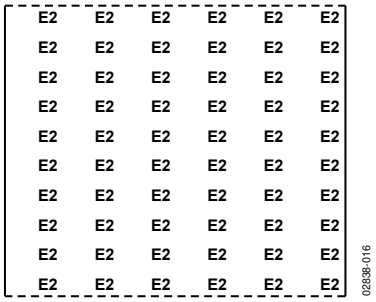

Figure 14. Even Pixels from Frame 2

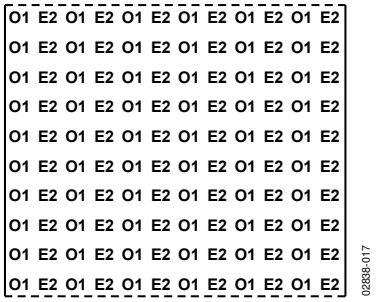

Figure 15. Combined Frame Output from Graphics Controller

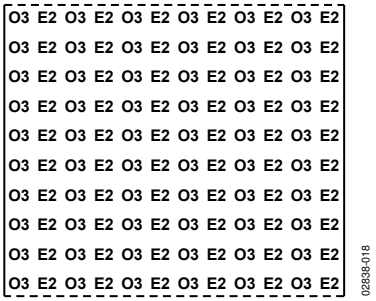

Figure 16. Subsequent Frame from Controller

TIMING—ANALOG INTERFACE

The timing diagrams (Figure 18 through Figure 27) show the operation of the AD9887A analog interface in all clock modes. The part establishes timing by sending the pixel corresponding with the leading edge of Hsync to Data Port A. In dual-channel mode, the next sample is sent to Data Port B. Subsequent samples are alternated between the A and B data ports. In single-channel mode, data is only sent to Data Port A, and Data Port B is placed in a high impedance state.

The output data clock signal is created so that its rising edge always occurs between transitions of Data Port A and can be used to latch the output data externally.

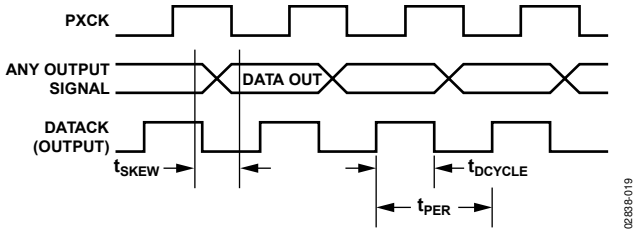

Figure 17. Analog Output Timing

Hsync Timing

Horizontal sync is processed in the AD9887A to eliminate ambiguity in the timing of the leading edge with respect to the phase-delayed pixel clock and data.

The HSYNC input is used as a reference to generate the pixel sampling clock. The sampling phase can be adjusted with respect to Hsync through a full 360° in 32 steps via the phase adjust register to optimize the pixel sampling time. Display systems use Hsync to align memory and display write cycles; therefore, it is important to have a stable timing relationship between the HSYNC output (HSOUT) and data clock (DATACK).

Three things happen to Hsync in the AD9887A. First, the polarity of the HSYNC input is determined and, thus, has a known output polarity. The known output polarity can be programmed either active high or active low (Register 0x04, Bit 4). Second, HSOUT is aligned with DATACK and data outputs. Third, the duration of HSOUT (in pixel clocks) is set via Register 0x07. Use the HSOUT signal to drive the rest of the display system.

Coast Timing

In most computer systems, the Hsync signal is provided continuously on a dedicated wire. In these systems, the coast input and function are unnecessary and should not be used. In some systems, however, Hsync is disturbed during the vertical sync (Vsync) period, and sometimes Hsync pulses disappear. In other systems, such as those that use composite sync (Csync) signals or those that embed sync-on-green (SOG), Hsync includes equalization pulses or other distortions during Vsync. To avoid upsetting the clock generator during Vsync, it is important to ignore these distortions. If the pixel clock PLL sees extraneous pulses, it attempts to lock on to this new frequency and changes frequency by the end of the Vsync period. It then requires a few lines of correct Hsync timing to recover at the beginning of a new frame, resulting in a tearing of the image at the top of the display.

The coast input is provided to eliminate this problem. It is an asynchronous input that disables the PLL input and holds the clock at its current frequency. The PLL can operate in this manner for several lines without significant frequency drift.

Coast can be provided by the graphics controller, or it can be internally generated by the AD9887A sync processing engine.

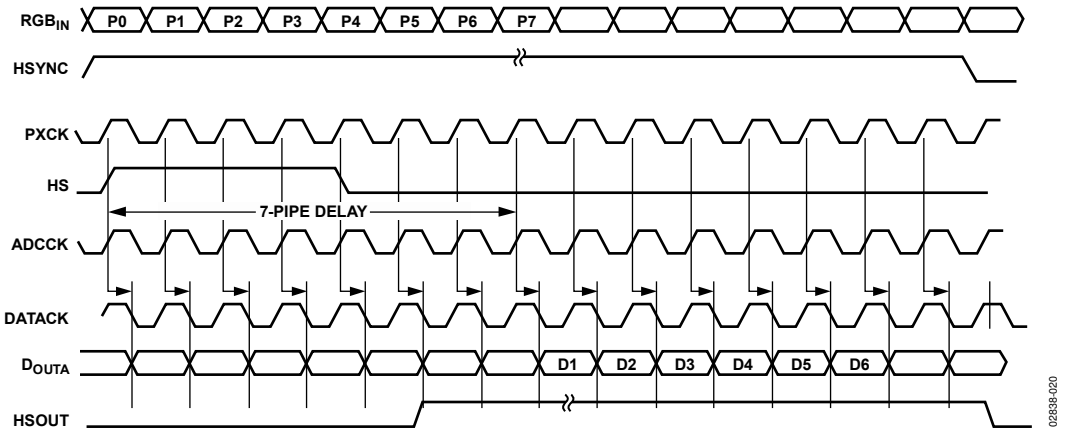

Figure 18. Single-Channel Mode (Analog Interface)

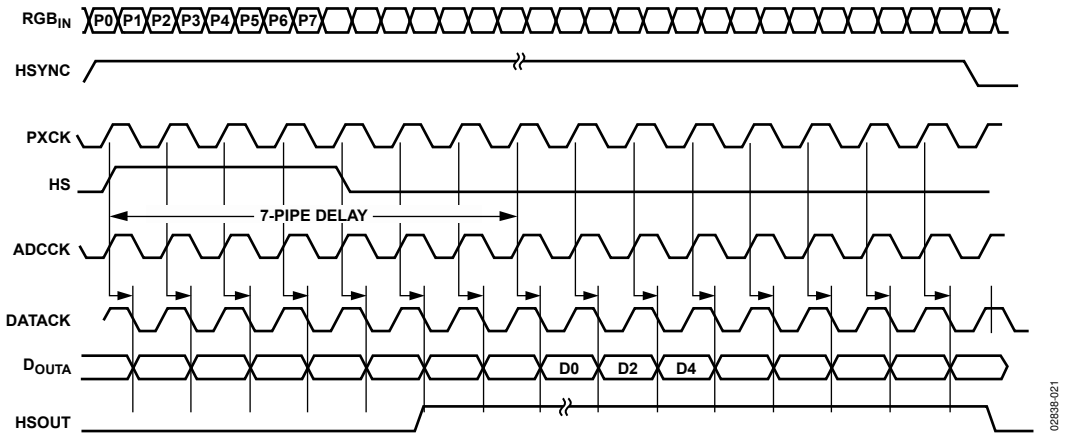

Figure 19. Single-Channel Mode, Alternate Pixel Sampling (Even Pixels, Analog Interface)

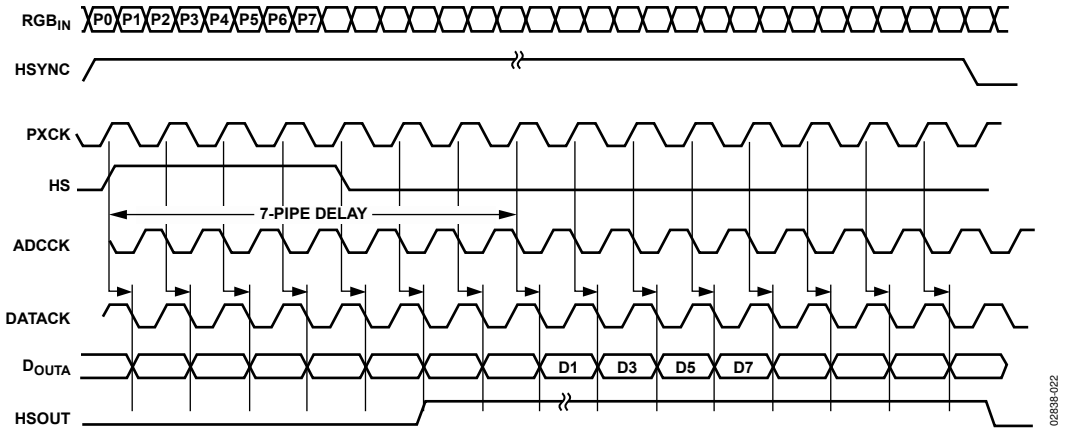

Figure 20. Single-Channel Mode, Alternate Pixel Sampling (Odd Pixels, Analog Interface)

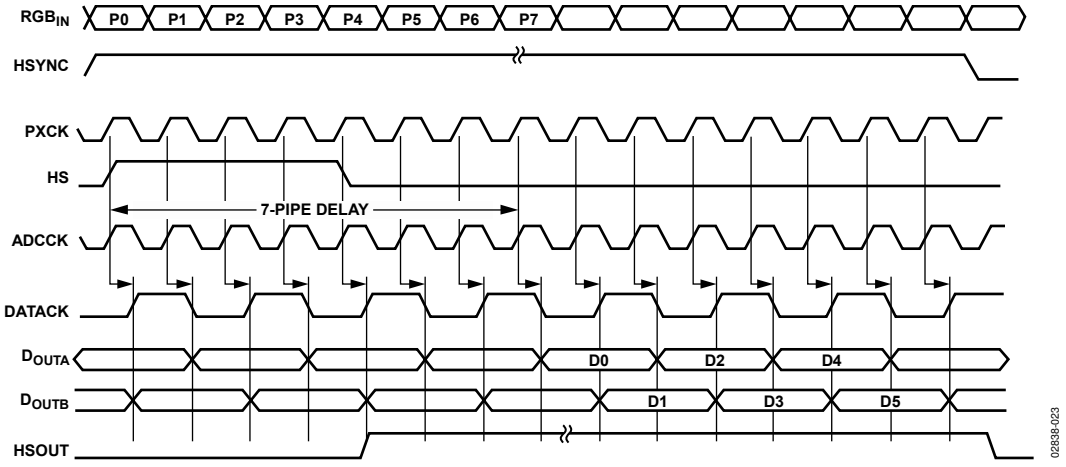

Figure 21. Dual-Channel Mode, Interleaved Outputs (Analog Interface), Outphase = 0