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CCD Signal Processors with *Precision Timing*™ Generator

AD9891/AD9895

FEATURES
AD9891: 10-Bit 20 MHz Version
AD9895: 12-Bit 30 MHz Version
Correlated Double Sampler (CDS)
4 ±6 dB Pixel Gain Amplifier (*PxGA*®)
2 dB to 36 dB 10-Bit Variable Gain Amplifier (VGA)
10-Bit 20 MHz A/D Converter (AD9891)
12-Bit 30 MHz A/D Converter (AD9895)
Black Level Clamp with Variable Level Control
Complete On-Chip Timing Generator
***Precision Timing* Core with 1 ns Resolution**
On-Chip 5 V Horizontal and RG Drivers
2-Phase and 4-Phase H-Clock Modes
4-Phase Vertical Transfer Clocks
Electronic and Mechanical Shutter Modes
On-Chip Driver for External Crystal
On-Chip Sync Generator with External Sync Option
64-Lead CSPBGA Package

APPLICATIONS
Digital Still Cameras
**Digital Video Camcorders**
Industrial Imaging

PRODUCT DESCRIPTION
The AD9891 and AD9895 are highly integrated CCD signal processors for digital still camera applications. Both include a complete analog front end with A/D conversion combined with a full-function programmable timing generator. A *Precision Timing* core allows adjustment of high speed clocks with 1 ns resolution at 20 MHz operation and 700 ps resolution at 30 MHz operation.

The AD9891 is specified at pixel rates of up to 20 MHz, and the AD9895 is specified at 30 MHz. The analog front end includes black level clamping, CDS, *PxGA*, VGA, and a 10-Bit or 12-Bit A/D converter. The timing generator provides all the necessary CCD clocks: RG, H-clocks, V-clocks, sensor gate pulses, substrate clock, and substrate bias control. Operation is programmed using a 3-wire serial interface.

Packaged in a space-saving 64-lead CSPBGA, the AD9891 and AD9895 are specified over an operating temperature range of –20°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM
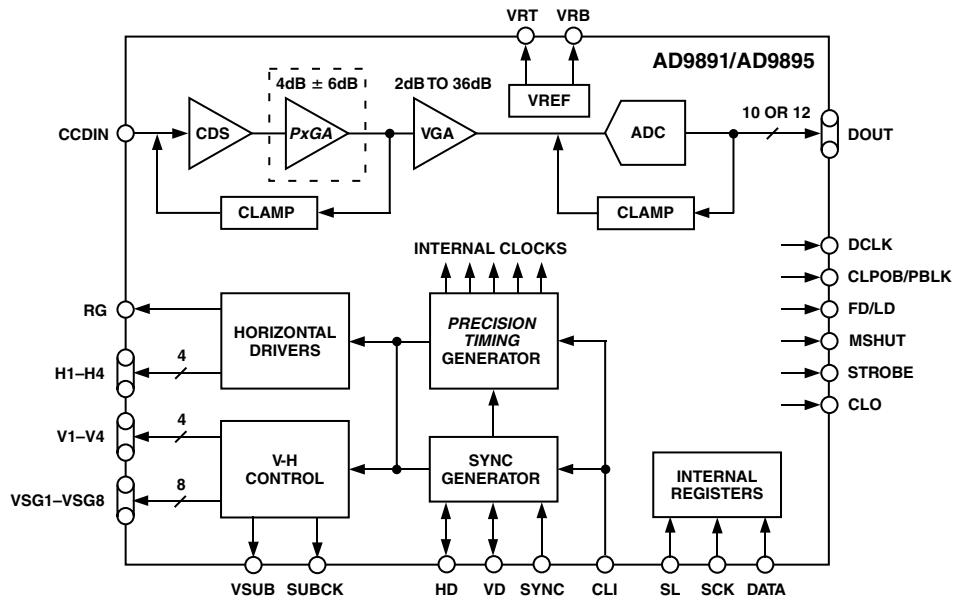
PxGA is a registered trademark and *Precision Timing* is a trademark of Analog Devices, Inc.

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AD9891/AD9895

TABLE OF CONTENTS

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating	–20		+85	°C
Storage	–65		+150	°C
POWER SUPPLY VOLTAGE				
AVDD1, AVDD2 (AFE Analog Supply)	2.7	3.0	3.6	V
TCVDD (Timing Core Analog Supply)	2.7	3.0	3.6	V
RGVDD (RG Driver)	3.0	5.0	5.25	V
HVDD (H1–H4 Drivers)	3.0	5.0	5.25	V
DRVDD (Data Output Drivers)	2.7	3.0	3.6	V
DVDD (Digital)	2.7	3.0	3.6	V
POWER DISSIPATION–AD9891 (See TPC 1 for Power Curves)				
20 MHz, Typ Supply Levels, 100 pF H1–H4 Loading		380		mW
Power from HVDD Only*		220		mW
Power-Down 1 Mode		42		mW
Power-Down 2 Mode		8		mW
Power-Down 3 Mode		2.5		mW
POWER DISSIPATION–AD9895 (See TPC 4 for Power Curves)				
30 MHz, Typ Supply Levels, 100 pF H1–H4 Loading		600		mW
Power from HVDD Only*		320		mW
Power-Down 1 Mode		138		mW
Power-Down 2 Mode		22		mW
Power-Down 3 Mode		2.5		mW
MAXIMUM CLOCK RATE (CLI)				
AD9891	20			MHz
AD9895	30			MHz

*The total power dissipated by the HVDD supply may be approximated using the equation:

$$Total\ HVDD\ Power = [C_{LOAD} \times HVDD \times Pixel\ Frequency] \times HVDD \times Number\ of\ H\text{-}Outputs\ Used$$

Reducing the H-loading, using only two of the outputs, and/or using a lower *HVDD* supply will reduce the power dissipation.
Actual HVDD power may be slightly higher than the calculated value because of stray capacitance inherent in the PCB layout/routing.
Specifications subject to change without notice.

DIGITAL SPECIFICATIONS
(RGVDD = HVDD = 4.75 V to 5.25 V, DVDD = DRVDD = 2.7 V to 3.5 V, C_L = 20 pF, T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.1			V
Low Level Input Voltage	V_{IL}			0.6	V
High Level Input Current	I_{IH}		10		μA
Low Level Input Current	I_{IL}		10		μA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS (Except H and RG)					
High Level Output Voltage @ I_{OH} = 2 mA	V_{OH}	2.2			V
Low Level Output Voltage @ I_{OL} = 2 mA	V_{OL}			0.5	V
RG and H-DRIVER OUTPUTS (H1–H4)					
High Level Output Voltage @ Max Current	V_{OH}	VDD – 0.5			V
Low Level Output Voltage @ Max Current	V_{OL}			0.5	V
Maximum Output Current (Programmable)		24			mA
Maximum Load Capacitance (for Each Output)		100			pF

Specifications subject to change without notice.

AD9891–ANALOG SPECIFICATIONS (AVDD1, AVDD2 = 3.0 V, f_{CLI} = 20 MHz, T_{MIN} to T_{MAX}, unless otherwise noted.)

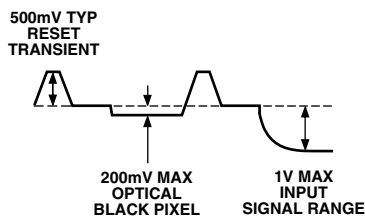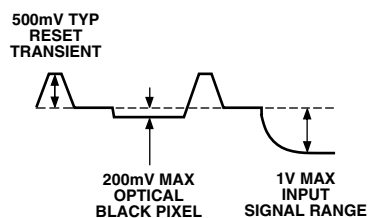| Parameter	Min	Typ	Max	Unit	Notes
CDS					
Gain		0		dB	
Allowable CCD Reset Transient		500		mV	Input signal characteristics*
Max Input Range before Saturation	1.0			V p-p	
Max CCD Black Pixel Amplitude		±200		mV	
PIXEL GAIN AMPLIFIER (*PxGA*)					
Max Input Range	1.0			V p-p	
Max Output Range	1.6			V p-p	
Gain Control Resolution		64		Steps	
Gain Monotonicity		Guaranteed			
Gain Range					
Min Gain (*PxGA* Code 32)		–2.5		dB	
Med Gain (*PxGA* Code 0)		+3.5		dB	Default setting
Max Gain (*PxGA* Code 31)		+9.5		dB	
VARIABLE GAIN AMPLIFIER (VGA)					
Max Input Range	1.6			V p-p	
Max Output Range	2.0			V p-p	
Gain Control Resolution		1024		Steps	
Gain Monotonicity		Guaranteed			
Gain Range					
Low Gain (VGA Code 70)		2		dB	
Max Gain (VGA Code 1023)		36		dB	
BLACK LEVEL CLAMP					
Clamp Level Resolution		256		Steps	
Clamp Level					Measured at ADC output
Min Clamp Level		0		LSB	
Max Clamp Level		63.75		LSB	
A/D CONVERTER					
Resolution	10			Bits	
Differential Nonlinearity (DNL)		±0.4	±1.0	LSB	
No Missing Codes		Guaranteed			
Full-Scale Input Voltage		2.0		V	
VOLTAGE REFERENCE					
Reference Top Voltage (VRT)		2.0		V	
Reference Bottom Voltage (VRB)		1.0		V	
SYSTEM PERFORMANCE					Includes entire signal chain
Gain Accuracy					Includes 4 dB default *PxGA* gain
Low Gain (VGA Code 70)	5	6	7	dB	Gain = (0.035 × Code) + 3.55 dB
Max Gain (VGA Code 1023)	38.5	39.5	40.5	dB	
Peak Nonlinearity, 500 mV Input Signal		0.2		%	12 dB gain applied
Total Output Noise		0.6		LSB rms	AC grounded input, 6 dB gain applied
Power Supply Rejection (PSR)		40		dB	Measured with step change on supply

*Input signal characteristics defined as follows:

Specifications subject to change without notice.

AD9895–ANALOG SPECIFICATIONS (AVDD1, AVDD2 = 3.0 V, f_{CLI} = 30 MHz, T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Notes
CDS					
Gain		0		dB	
Allowable CCD Reset Transient		500		mV	Input signal characteristics*
Max Input Range before Saturation	1.0			V p-p	
Max CCD Black Pixel Amplitude		±200		mV	
PIXEL GAIN AMPLIFIER (*PxGA*)					
Max Input Range	1.0			V p-p	
Max Output Range	1.6			V p-p	
Gain Control Resolution		64		Steps	
Gain Monotonicity		Guaranteed			
Gain Range					
Min Gain (*PxGA* Code 32)		–2.5		dB	
Med Gain (*PxGA* Code 0)		+3.5		dB	Default setting
Max Gain (*PxGA* Code 31)		+9.5		dB	
VARIABLE GAIN AMPLIFIER (VGA)					
Max Input Range	1.6			V p-p	
Max Output Range	2.0			V p-p	
Gain Control Resolution		1024		Steps	
Gain Monotonicity		Guaranteed			
Gain Range					
Low Gain (VGA Code 70)		2		dB	
Max Gain (VGA Code 1023)		36		dB	
BLACK LEVEL CLAMP					
Clamp Level Resolution		256		Steps	
Clamp Level					Measured at ADC output
Min Clamp Level		0		LSB	
Max Clamp Level		255		LSB	
A/D CONVERTER					
Resolution	12			Bits	
Differential Nonlinearity (DNL)		±0.5	±1.0	LSB	
No Missing Codes		Guaranteed			
Full-Scale Input Voltage		2.0		V	
VOLTAGE REFERENCE					
Reference Top Voltage (VRT)		2.0		V	
Reference Bottom Voltage (VRB)		1.0		V	
SYSTEM PERFORMANCE					Includes entire signal chain
Gain Accuracy					Includes 4 dB default *PxGA* gain
Low Gain (VGA Code 70)	5	6	7	dB	Gain = (0.035 × Code) + 3.55 dB
Max Gain (VGA Code 1023)	38.5	39.5	40.5	dB	
Peak Nonlinearity, 500 mV Input Signal		0.2		%	12 dB gain applied
Total Output Noise		0.8		LSB rms	AC grounded input, 6 dB gain applied
Power Supply Rejection (PSR)		40		dB	Measured with step change on supply

*Input signal characteristics defined as follows:

500mV TYP RESET TRANSIENT

200mV MAX OPTICAL BLACK PIXEL   **1V MAX INPUT SIGNAL RANGE**

Specifications subject to change without notice.

TIMING SPECIFICATIONS
(C_L = 20 pF, AVDD = DVDD = DRVDD = 3.0 V, f_{CLI} = 20 MHz [AD9891] or 30 MHz [AD9895], unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
MASTER CLOCK, CLI (Figure 7)					
CLI Clock Period, AD9891	t_{CONV}	50			ns
CLI High/Low Pulsewidth, AD9891		20	25		ns
CLI Clock Period, AD9895	t_{CONV}	33.3			ns
CLI High/Low Pulsewidth, AD9895		13	16.7		ns
Delay from CLI Rising Edge to Internal Pixel Position 0	t_{CLIDLY}		6		ns
AFE CLAMP PULSES[1] (Figure 13)					
CLPDM Pulsewidth		4	10		Pixels
CLPOB Pulsewidth[2]		2	20		Pixels
AFE SAMPLE LOCATION[1] (Figure 10)					
SHP Sample Edge to SHD Sample Edge, AD9891	t_{S1}	20	25		ns
SHP Sample Edge to SHD Sample Edge, AD9895	t_{S1}	13	16.7		ns
DATA OUTPUTS (Figure 12)					
Output Delay from DCLK Rising Edge[1]	t_{OD}		8		ns
Pipeline Delay from SHP/SHD Sampling			9		Cycles
SERIAL INTERFACE (Figures 52 and 53)					
Maximum SCK Frequency	f_{SCLK}	10			MHz
SL to SCK Setup Time	t_{LS}	10			ns
SCK to SL Hold Time	t_{LH}	10			ns
SDATA Valid to SCK Rising Edge Setup	t_{DS}	10			ns
SCK Falling Edge to SDATA Valid Hold	t_{DH}	10			ns
SCK Falling Edge to SDATA Valid Read	t_{DV}	10			ns

NOTES
[1]Parameter is programmable.
[2]Minimum CLPOB pulsewidth is for functional operation only. Wider typical pulses are recommended to achieve good clamp performance.

ABSOLUTE MAXIMUM RATINGS

Parameter	With Respect To	Min	Max	Unit
AVDD1, AVDD2	AVSS	–0.3	+3.9	V
TCVDD	TCVSS	–0.3	+3.9	V
HVDD	HVSS	–0.3	+5.5	V
RGVDD	RGVSS	–0.3	+5.5	V
DVDD	DVSS	–0.3	+3.9	V
DRVDD	DRVSS	–0.3	+3.9	V
RG Output	RGVSS	–0.3	RGVDD + 0.3	V
H1–H4 Output	HVSS	–0.3	HVDD + 0.3	V
Digital Outputs	DVSS	–0.3	DVDD + 0.3	V
Digital Inputs	DVSS	–0.3	DVDD + 0.3	V
SCK, SL, SDATA	DVSS	–0.3	DVDD + 0.3	V
VRT, VRB	AVSS	–0.3	AVDD + 0.3	V
BYP1–BYP3, CCDIN	AVSS	–0.3	AVDD + 0.3	V
Junction Temperature			150	°C
Lead Temperature, 10 sec			350	°C

PACKAGE THERMAL CHARACTERISTICS
Thermal Resistance
θ_{JA} = 61°C/W
θ_{JC} = 29.7°C/W

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9891KBC	–20°C to +85°C	CSPBGA	BC-64
AD9895KBC	–20°C to +85°C	CSPBGA	BC-64

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9891 and AD9895 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!
ESD SENSITIVE DEVICE

REV. A

AD9891 PIN CONFIGURATION
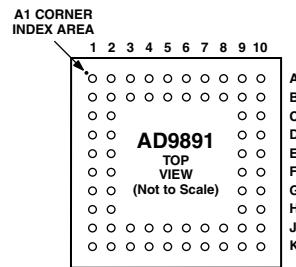
PIN FUNCTION DESCRIPTIONS[1]

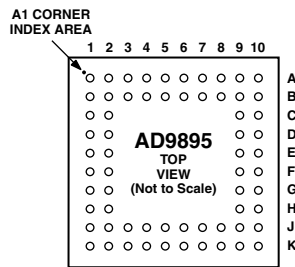| Pin	Mnemonic	Type[2]	Description	Pin	Mnemonic	Type[2]	Description
A1	VD	DO	Vertical Sync Pulse (Input for Slave Mode, Output for Master Mode)	K9	VSG5	DO	CCD Sensor Gate Pulse 5
				J9	VSG6	DO	CCD Sensor Gate Pulse 6
				K10	VSG7	DO	CCD Sensor Gate Pulse 7
B1	HD	DO	Horizontal Sync Pulse (Input for Slave Mode, Output for Master Mode)	J10	VSG8	DO	CCD Sensor Gate Pulse 8
				H10	H1	DO	CCD Horizontal Clock 1
				H9	H2	DO	CCD Horizontal Clock 2
C1	SYNC	DI	External System Sync Input	G10	HVDD	P	H1–H4 Driver Supply
C2	LD/FD	DO	Line or Field Designator Output	G9	HVSS	P	H1–H4 Driver Ground
				F10	H3	DO	CCD Horizontal Clock 3
D1	DCLK	DO	Data Clock Output	F9	H4	DO	CCD Horizontal Clock 4
D2	CLPOB/ PBLK	DO	CLPOB or PBLK Output	E10	RGVDD	P	RG Driver Supply
				E9	RGVSS	P	RG Driver Ground
E1	NC		Not Internally Connected	D9	RG	DO	CCD Reset Gate Clock
E2	NC		Not Internally Connected	D10	CLO	DO	Reference Clock Output for Crystal
F2	DO/SDO	DO	Data Output (LSB) (also Serial Data Output[3])	C10	CLI	DI	Reference Clock Input
F1	D1	DO	Data Output	B10	TCVDD	P	Analog Supply for Timing Core
G2	D2	DO	Data Output	C9	TCVSS	P	Analog Ground for Timing Core
G1	D3	DO	Data Output				
H2	D4	DO	Data Output	A10	AVDD1	P	Analog Supply for AFE
H1	D5	DO	Data Output	B9	AVSS1	P	Analog Ground for AFE
J2	D6	DO	Data Output	A9	BYP1	AO	Analog Circuit Bypass
J1	D7	DO	Data Output	B8	BYP2	AO	Analog Circuit Bypass
K2	D8	DO	Data Output	A8	CCDIN	AI	CCD Signal Input
K1	D9	DO	Data Output (MSB)	A7	BYP3	AO	Analog Circuit Bypass
K3	DRVDD	P	Data Output Driver Supply	B7	AVDD2	P	Analog Supply for AFE
K4	DRVSS	P	Data Output Driver Ground	B6	AVSS2	P	Analog Ground for AFE
J3	VSUB	DO	CCD Substrate Bias	A6	REFB	AO	Voltage Reference Bottom Bypass
J4	SUBCK	DO	CCD Substrate Clock (E-Shutter)	A5	REFT	AO	Voltage Reference Top Bypass
K5	V1	DO	CCD Vertical Transfer Clock 1	B5	SL	DI	3-Wire Serial Load Pulse
J5	V2	DO	CCD Vertical Transfer Clock 2	A4	SDI	DI	3-Wire Serial Data Input
K6	V3	DO	CCD Vertical Transfer Clock 3	B4	SCK	DI	3-Wire Serial Clock
J6	V4	DO	CCD Vertical Transfer Clock 4	A3	MSHUT	DO	Mechanical Shutter Pulse
K7	VSG1/V5	DO	CCD Sensor Gate Pulse 1 (also V5[4])	B3	STROBE	DO	Strobe Pulse
				B2	DVSS	P	Digital Ground
J7	VSG2/V6	DO	CCD Sensor Gate Pulse 2 (also V6[4])	A2	DVDD	P	Digital Supply for VSG, V1–V4, HD, VD, MSHUT, STROBE, and Serial Interface
K8	VSG3/V7	DO	CCD Sensor Gate Pulse 3 (also V7[4])				
J8	VSG4/V8	DO	CCD Sensor Gate Pulse 4 (also V8[4])				

NOTES
[1]See Figure 50 for circuit configuration.
[2]AI = Analog Input, AO = Analog Output, DI = Digital Input,
 DO = Digital Output, DIO = Digital Input/Output, P = Power.
[3]In Register Readback Mode
[4]In Frame Transfer CCD Mode

AD9891/AD9895

PIN FUNCTION DESCRIPTIONS[1]

Pin	Mnemonic	Type[2]	Description
A1	VD	DO	Vertical Sync Pulse (Input for Slave Mode, Output for Master Mode)
B1	HD	DO	Horizontal Sync Pulse (Input for Slave Mode, Output for Master Mode)
C1	SYNC	DI	External System Sync Input
C2	LD/FD	DO	Line or Field Designator Output
D1	DCLK	DO	Data Clock Output
D2	CLPOB/PBLK	DO	CLPOB or PBLK Output
E2	DO	DO	Data Output (LSB)
E1	D1	DO	Data Output
F2	D2/SDO	DO	Data Output (also Serial Data Output[3])
F1	D3	DO	Data Output
G2	D4	DO	Data Output
G1	D5	DO	Data Output
H2	D6	DO	Data Output
H1	D7	DO	Data Output
J2	D8	DO	Data Output
J1	D9	DO	Data Output
K2	D10	DO	Data Output
K1	D11	DO	Data Output (MSB)
K3	DRVDD	P	Data Output Driver Supply
K4	DRVSS	P	Data Output Driver Ground
J3	VSUB	DO	CCD Substrate Bias
J4	SUBCK	DO	CCD Substrate Clock (E-Shutter)
K5	V1	DO	CCD Vertical Transfer Clock 1
J5	V2	DO	CCD Vertical Transfer Clock 2
K6	V3	DO	CCD Vertical Transfer Clock 3
J6	V4	DO	CCD Vertical Transfer Clock 4
K7	VSG1/V5	DO	CCD Sensor Gate Pulse 1 (also V5[4])
J7	VSG2/V6	DO	CCD Sensor Gate Pulse 2 (also V6[4])
K8	VSG3/V7	DO	CCD Sensor Gate Pulse 3 (also V7[4])
J8	VSG4/V8	DO	CCD Sensor Gate Pulse 4 (also V8[4])
K9	VSG5	DO	CCD Sensor Gate Pulse 5
J9	VSG6	DO	CCD Sensor Gate Pulse 6
K10	VSG7	DO	CCD Sensor Gate Pulse 7
J10	VSG8	DO	CCD Sensor Gate Pulse 8
H10	H1	DO	CCD Horizontal Clock 1
H9	H2	DO	CCD Horizontal Clock 2
G10	HVDD	P	H1–H4 Driver Supply
G9	HVSS	P	H1–H4 Driver Ground
F10	H3	DO	CCD Horizontal Clock 3
F9	H4	DO	CCD Horizontal Clock 4
E10	RGVDD	P	RG Driver Supply
E9	RGVSS	P	RG Driver Ground
D9	RG	DO	CCD Reset Gate Clock
D10	CLO	DO	Reference Clock Output for Crystal
C10	CLI	DI	Reference Clock Input
B10	TCVDD	P	Analog Supply for Timing Core
C9	TCVSS	P	Analog Ground for Timing Core
A10	AVDD1	P	Analog Supply for AFE
B9	AVSS1	P	Analog Ground for AFE
A9	BYP1	AO	Analog Circuit Bypass
B8	BYP2	AO	Analog Circuit Bypass
A8	CCDIN	AI	CCD Signal Input
A7	BYP3	AO	Analog Circuit Bypass
B7	AVDD2	P	Analog Supply for AFE
B6	AVSS2	P	Analog Ground for AFE
A6	REFB	AO	Voltage Reference Bottom Bypass
A5	REFT	AO	Voltage Reference Top Bypass
B5	SL	DI	3-Wire Serial Load Pulse
A4	SDI	DI	3-Wire Serial Data Input
B4	SCK	DI	3-Wire Serial Clock
A3	MSHUT	DO	Mechanical Shutter Pulse
B3	STROBE	DO	Strobe Pulse
B2	DVSS	P	Digital Ground
A2	DVDD	P	Digital Supply for VSG, V1–V4, HD, VD, MSHUT, STROBE, and Serial Interface

NOTES
[1]See Figure 50 for circuit configuration.
[2]AI = Analog Input, AO = Analog Output, DI = Digital Input,
 DO = Digital Output, DIO = Digital Input/Output, P = Power.
[3]In Register Readback Mode
[4]In Frame Transfer CCD Mode

REV. A

SPECIFICATION DEFINITIONS

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Thus, every code must have a finite width. No missing codes guaranteed to 12-bit resolution indicates that all 4096 codes, respectively, must be present over all operating conditions.

Peak Nonlinearity

Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the output of the AD9891/AD9895 from a true straight line. The point used as "zero scale" occurs 0.5 LSB before the first code transition. "Positive full scale" is defined as a level 1 and 0.5 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always appropriately gained up to fill the ADC's full-scale range.

Total Output Noise

The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage, using the relationship 1 *LSB* = (*ADC Full Scale*/2^n *codes*) when *n* is the bit resolution of the ADC. For the AD9891, 1 LSB is 2 mV, while for the AD9895, 1 LSB is 0.5 mV.

Power Supply Rejection (PSR)

The PSR is measured with a step change applied to the supply pins. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.
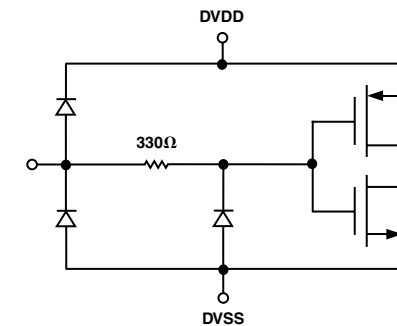
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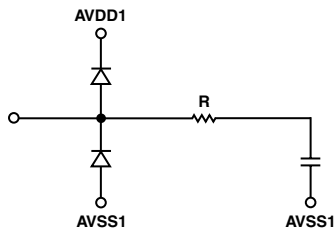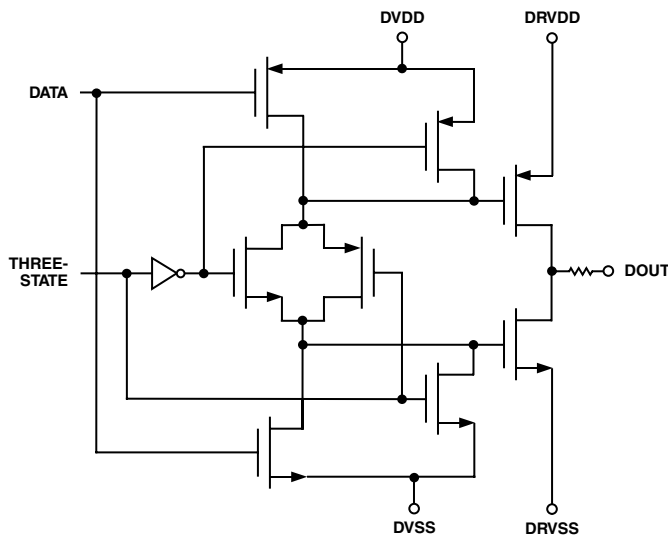

Figure 1. CCDIN

Figure 3. Digital Inputs

Figure 2. Digital Data Outputs
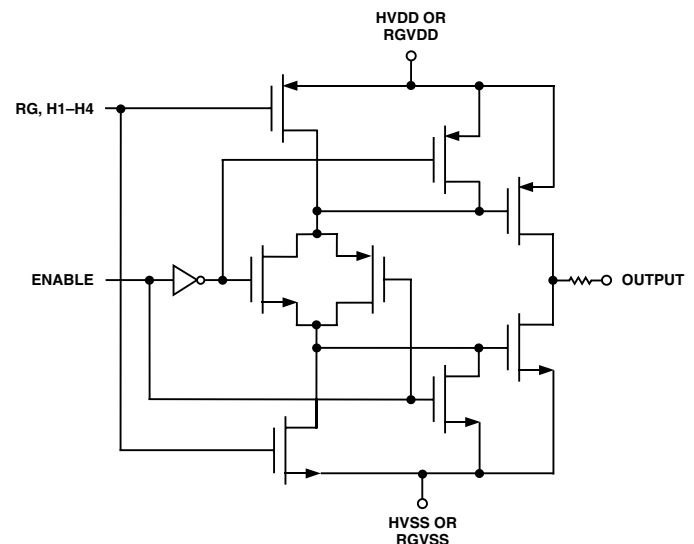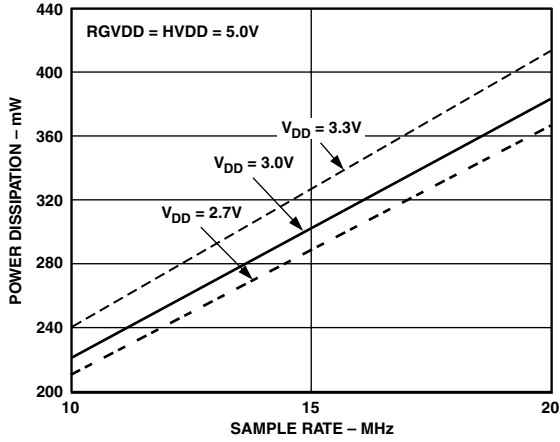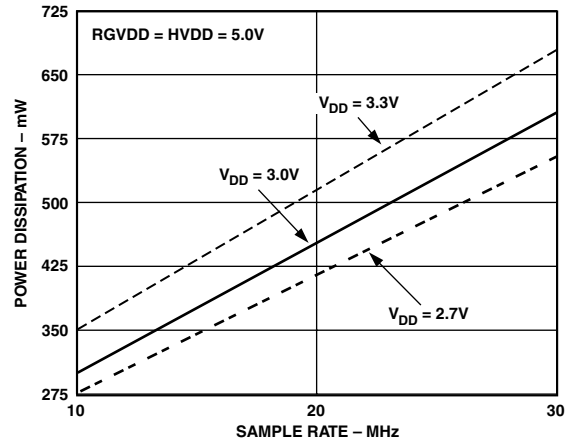

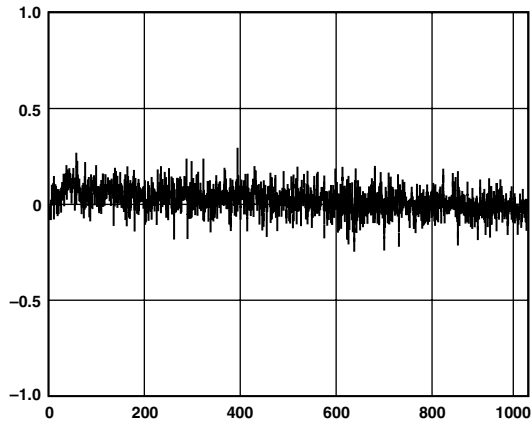Figure 4. H1–H4, RG Drivers

AD9891/AD9895–Typical Performance Characteristics
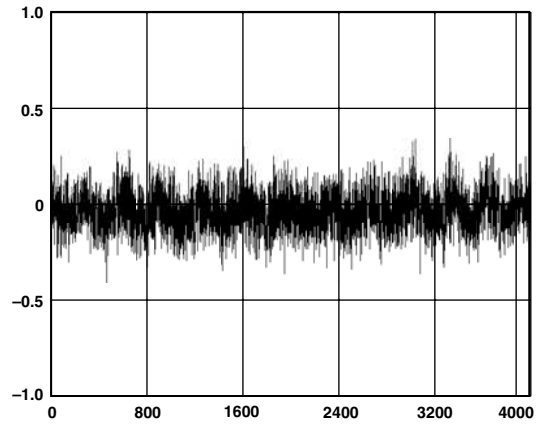

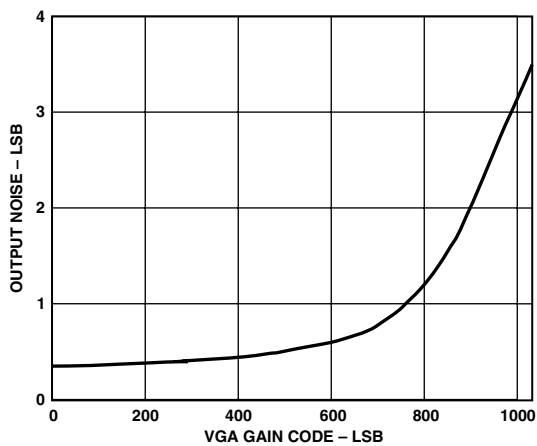TPC 1. AD9891 Power vs. Sample Rate

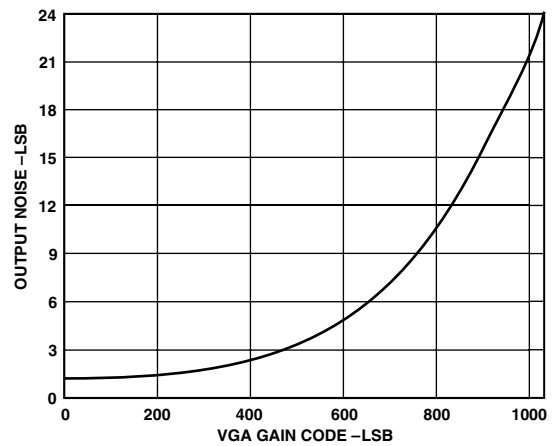
TPC 4. AD9895 Power vs. Sample Rate

TPC 2. AD9891 Typical DNL Performance

TPC 5. AD9895 Typical DNL Performance

TPC 3. AD9891 Output Noise vs. VGA Gain

TPC 6. AD9895 Output Noise vs. VGA Gain

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SYSTEM OVERVIEW

Figure 5 shows the typical system block diagram for the AD9891/AD9895 used in Master Mode. The CCD output is processed by the AD9891/AD9895's AFE circuitry, which consists of a CDS, *PxGA*, VGA, black level clamp, and an A/D converter. The digitized pixel information is sent to the digital image processor chip, which performs the post-processing and compression. To operate the CCD, all CCD timing parameters are programmed into the AD9891/AD9895 from the system microprocessor, through the 3-wire serial interface. From the system master clock, CLI, provided by the image processor or external crystal, the AD9891/AD9895 generates all of the CCD's horizontal and vertical clocks and all internal AFE clocks. External synchronization is provided by a SYNC pulse from the microprocessor, which will reset internal counters and resync the VD and HD outputs.
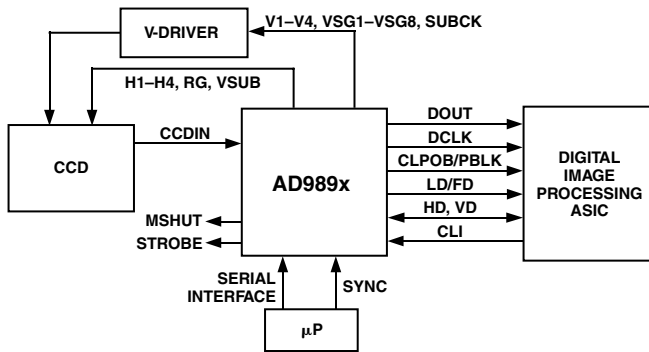

Figure 5. Typical System Block Diagram, Master Mode

Alternatively, the AD9891/AD9895 may be operated in Slave Mode, in which the VD and HD are provided externally from the image processor. In this mode, all AD9891/AD9895 timing will be synchronized with VD and HD.

The H-drivers for H1–H4 and RG are included in the AD9891/AD9895, allowing these clocks to be directly connected to the CCD.

H-drive voltage of up to 5 V is supported. An external V-driver is required for the vertical transfer clocks, the sensor gate pulses, and the substrate clock.

The AD9891/AD9895 also includes programmable MSHUT and STROBE outputs, which may be used to trigger mechanical shutter and strobe (flash) circuitry.

Figure 6 shows the horizontal and vertical counter dimensions for the AD9891/AD9895. All internal horizontal and vertical clocking is programmed using these dimensions to specify line and pixel locations.
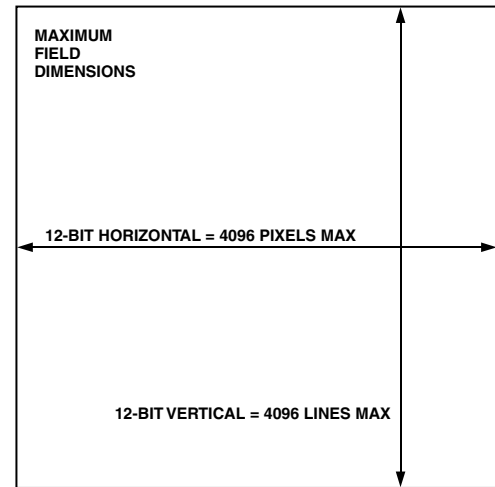

Figure 6. Vertical and Horizontal Counters

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PRECISION TIMING HIGH SPEED TIMING GENERATION
The AD9891/AD9895 generates flexible, high speed timing signals using the *Precision Timing* core. This core is the foundation for generating the timing used for both the CCD and the AFE: the reset gate RG, horizontal drivers H1–H4, and the SHP/SHD sample clocks. A unique architecture makes it routine for the system designer to optimize image quality by providing precise control over the horizontal CCD readout and the AFE correlated double sampling.

The high speed timing of the AD9891/AD9895 operates the same in either Master or Slave Mode configuration.

Timing Resolution
The *Precision Timing* core uses a 1× master clock input (CLI) as a reference. This clock should be the same as the CCD pixel clock frequency. Figure 7 illustrates how the internal timing core divides the master clock period into 48 steps or edge positions. Using a 20 MHz CLI frequency, the edge resolution of the *Precision Timing* core is 1 ns. If a 1× system clock is not available, it is also possible to use a 2× reference clock by programming the CLIDIVIDE Register (Addr x01F). The AD9891/AD9895 will then internally divide the CLI frequency by two.

The AD9891/AD9895 also includes a master clock output, CLO, which is the inverse of CLI. This output is intended to be used as a crystal driver. A crystal can be placed between the CLI and CLO Pins to generate the master clock for the AD9891/AD9895. For more information on using a crystal, see Figure 51.

**High Speed Clock Programmability**
Figure 8 shows how the high speed clocks RG, H1–H4, SHP, and SHD are generated. The RG pulse has programmable rising and falling edges, and may be inverted using the polarity control. The horizontal clocks H1 and H3 have programmable rising and falling edges and polarity control. The H2 and H4 clocks are always inverses of H1 and H3, respectively. Table I summarizes the high speed timing registers and their parameters. Figure 9 shows the typical 2-phase H-clock arrangement in which H3 and H4 are programmed for the same edge location as H1 and H2.

The edge location registers are six bits wide, but there are only 48 valid edge locations available. Therefore, the register values are mapped into four quadrants, with each quadrant containing 12 edge locations. Table II shows the correct register values for
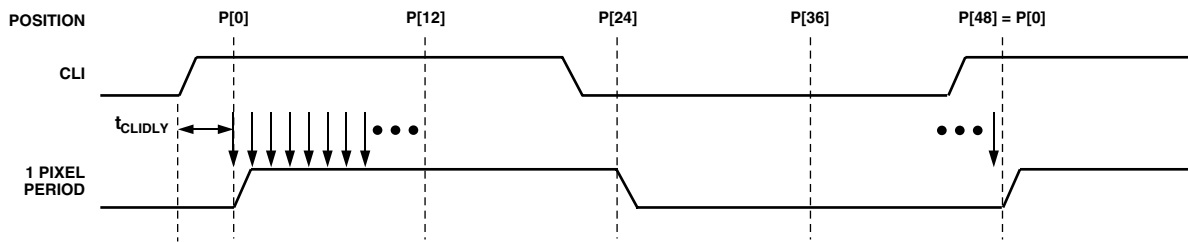
Figure 7. High Speed Clock Resolution from CLI Master Clock Input
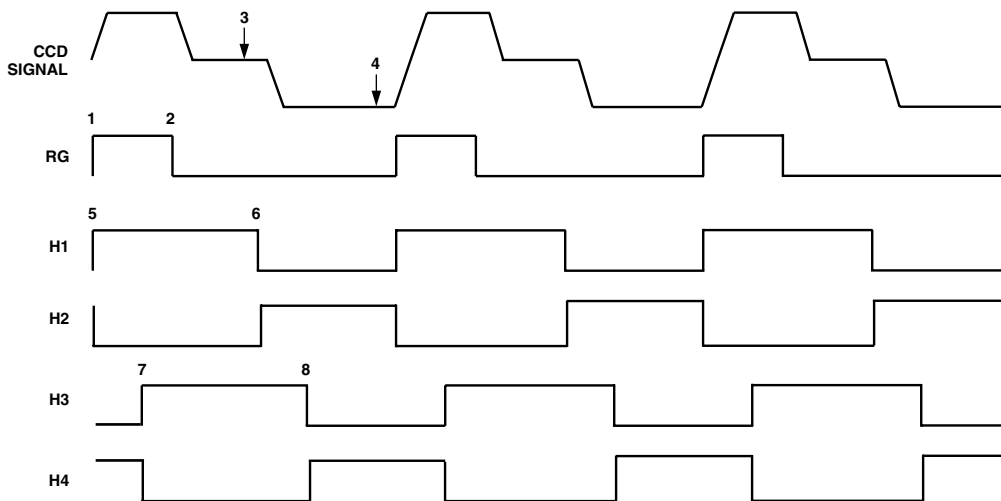
PROGRAMMABLE CLOCK POSITIONS:
1: RG RISING EDGE
2: RG FALLING EDGE
3: SHP SAMPLE LOCATION
4: SHD SAMPLE LOCATION
5: H1 RISING EDGE POSITION AND 6: H1 FALLING EDGE POSITION (H2 IS INVERSE OF H1)
7: H3 RISING EDGE POSITION AND 8: H3 FALLING EDGE POSITION (H4 IS INVERSE OF H3)

Figure 8. High Speed Clock Programmable Locations

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the corresponding edge locations. Figure 10 shows the range and default locations of the high speed clock signals.

H-Driver and RG Outputs

In addition to the programmable timing positions, the AD9891/AD9895 features on-chip output drivers for the RG and H1–H4 outputs. These drivers are powerful enough to directly drive the CCD inputs. The H-driver current can be adjusted for optimum rise/fall time into a particular load by using the DRV Registers (Addr x0E1 to x0E4). The RG drive current is adjustable using the RGDRV Register (Addr x0E8). Each 3-bit DRV Register is adjustable in 3.5 mA increments, with the minimum setting of 0 equal to OFF or three-state, and the maximum setting of 7 equal to 24.5 mA.

As shown in Figure 11, the H2 and H4 outputs are inverses of H1 and H3, respectively. The internal propagation delay resulting from the signal inversion is less than 1 ns, which is significantly less than the typical rise time driving the CCD load. This results

in an H1/H2 crossover voltage at approximately 50% of the output swing. The crossover voltage is not programmable.

Digital Data Outputs

The AD9891/AD9895 data output and DCLK phase are programmable using the DOUTPHASE Register (Addr x01D). Any edge from 0 to 47 may be programmed, as shown in Figure 12. Normally, the DOUT and DCLK signals will track in phase, based on the DOUTPHASE Register contents. The DCLK output phase can also be held fixed with respect to the data outputs, by changing the DCLKMODE Register (Addr x01E) HIGH. In this mode, the DCLK output will remain at a fixed phase equal to CLO (the inverse of CLI) while the data output phase is still programmable.

There is a fixed output delay from the DCLK rising edge to the DOUT transition, called t_{OD}. This delay can be programmed to four values between 0 ns and 12 ns, using the DOUT_DELAY Register (Addr x032). The default value is 8 ns.

Table I. H1–H4, RG, SHP, and SHD Timing Parameters

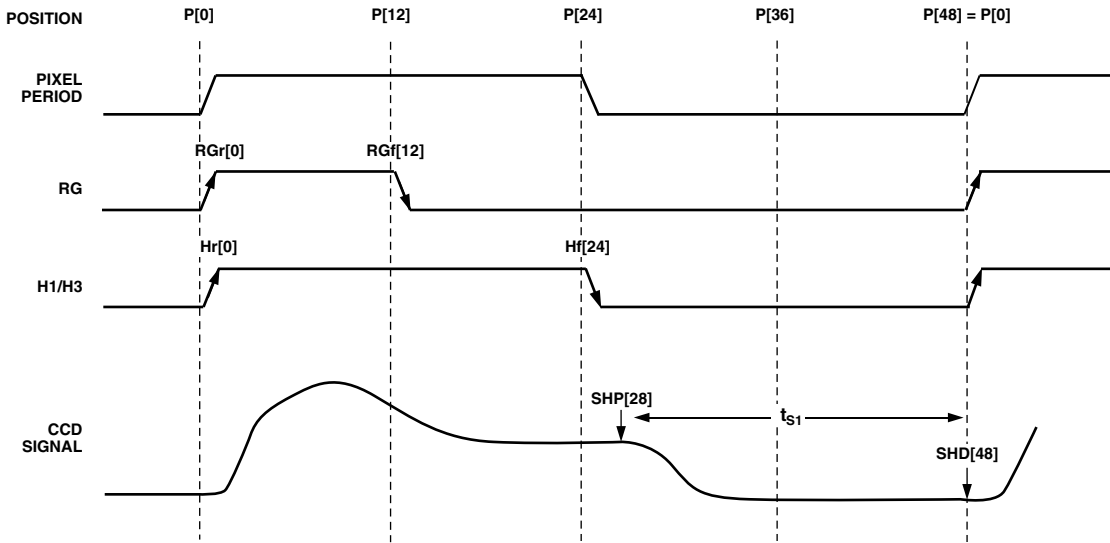| Register	Length	Range	Description
POL	1b	High/Low	Polarity Control for H1, H3, and RG (0 = No Inversion, 1 = Inversion)
POSLOC	6b	0–47 Edge Location	Positive Edge Location for H1, H3, and RG Sample Location for SHP, SHD
NEGLOC	6b	0–47 Edge Location	Negative Edge Location for H1, H3, and RG
DRV	3b	0–7 Current Steps	Drive Current for H1–H4 and RG Outputs (3.5 mA per Step)
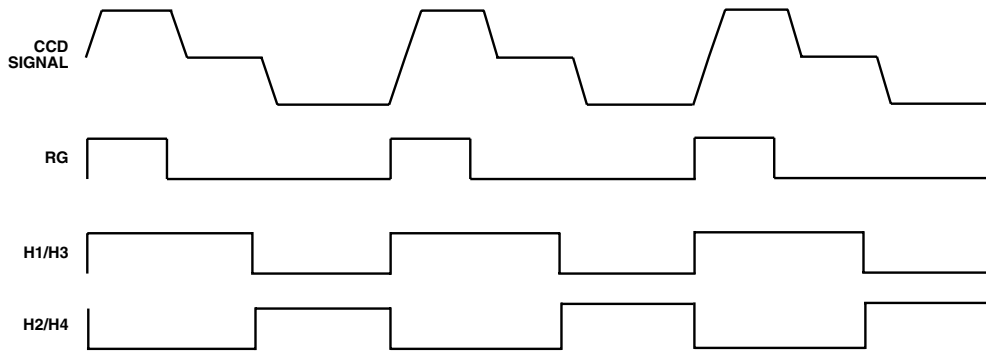
USING THE SAME TOGGLE POSITIONS FOR H1 AND H3 GENERATES STANDARD 2-PHASE H-CLOCKING.

Figure 9. 2-Phase H-Clock Operation

Table II. Precision Timing Edge Locations

Quadrant	Edge Location (Dec)	Register Value (Dec)	Register Value (Bin)
I	0 to 11	0 to 11	000000 to 001011
II	12 to 23	16 to 27	010000 to 011011
III	24 to 35	32 to 43	100000 to 101011
IV	36 to 47	48 to 59	110000 to 111011

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Figure 10. High Speed Clock Default and Programmable Locations
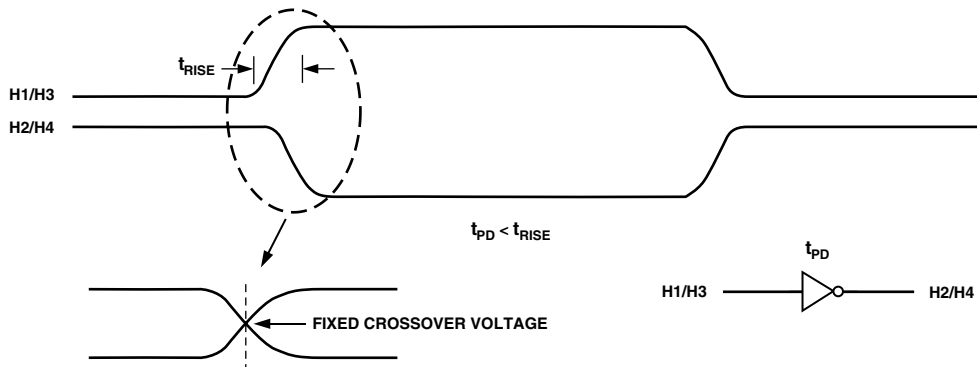
Figure 11. H-Clock Inverse Phase Relationship
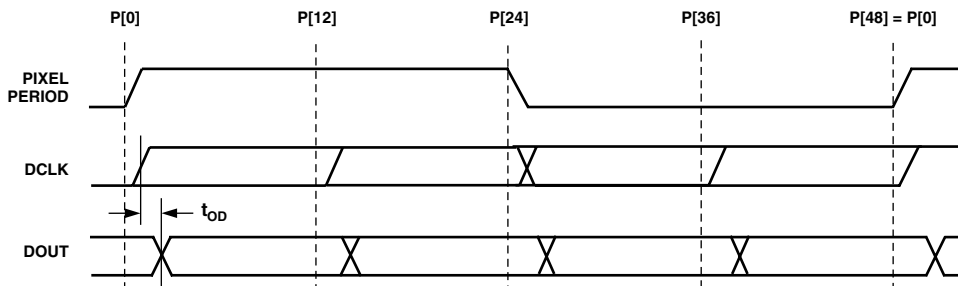
Figure 12. Digital Output Phase Adjustment

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HORIZONTAL CLAMPING AND BLANKING

The AD9891/AD9895's horizontal clamping and blanking pulses are fully programmable to suit a variety of applications. As with the vertical timing generation, individual sequences are defined for each signal, which are then organized into multiple regions during image readout. This allows the dark pixel clamping and blanking patterns to be changed at each stage of the readout in order to accommodate different image transfer timing and high speed line shifts.

Individual CLPOB, CLPDM, and PBLK Sequences

The AFE horizontal timing consists of CLPOB, CLPDM, and PBLK, as shown in Figure 13. These three signals are independently programmed using the registers in Table III. SPOL is the start polarity for the signal, and TOG1 and TOG2 are the first and second toggle positions of the pulse. All three signals are active low and should be programmed accordingly. Up to four individual sequences can be created for each signal.

To simplify the programming requirements, the CLPDM signal will track the CLPOB signal by default. If separate control of the CLPDM signal is desired, the SINGLE_CLAMP Register (Addr x031) should be set LOW.

Individual HBLK Sequences

The HBLK programmable timing shown in Figure 14 is similar to CLPOB, CLPDM, and PBLK. However, there is no start polarity control. Only the toggle positions are used to designate the start and the stop positions of the blanking period. Additionally, there is a polarity control, HBLKMASK, that designates the polarity of the horizontal clock signals H1–H4 during the blanking period. Setting HBLKMASK high will set H1 = H3 = Low and H2 = H4 = High during the blanking, as shown in Figure 15. Up to four individual sequences are available for HBLK.

Horizontal Sequence Control

The AD9891/AD9895 use sequence change positions (SCP) and sequence pointers (SPTR) to organize the individual hori-

PROGRAMMABLE SETTINGS:
1: START POLARITY (CLAMP AND BLANK REGION ARE ACTIVE LOW)
2: 1ST TOGGLE POSITION
3: 2ND TOGGLE POSITION

Figure 13. Clamp and Preblank Pulse Placement

PROGRAMMABLE SETTINGS:
1: 1ST TOGGLE POSITION = START OF BLANKING
2: 2ND TOGGLE POSITION = END OF BLANKING
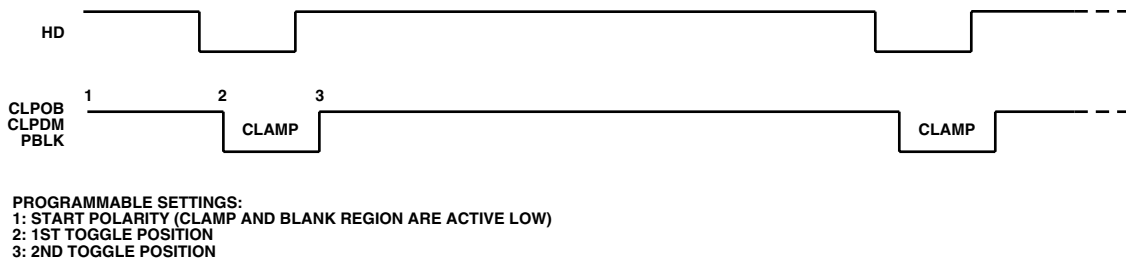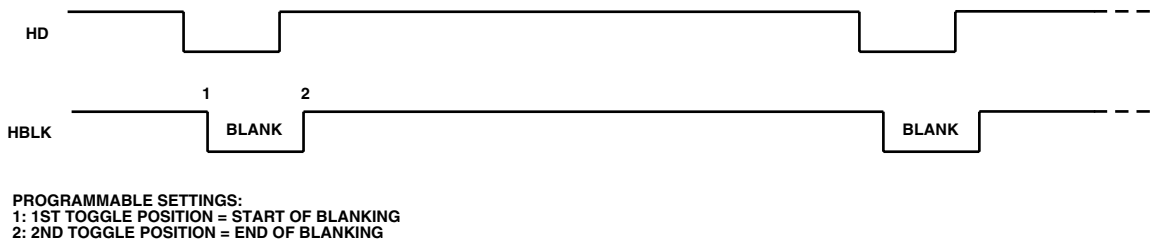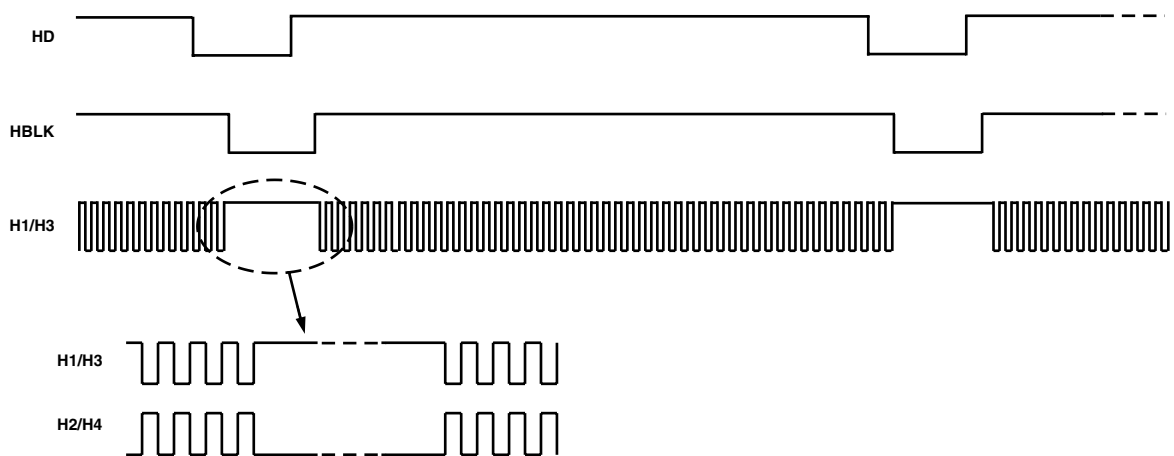
Figure 14. Horizontal Blanking (HBLK) Pulse Placement

THE POLARITY OF H1 DURING BLANKING IS PROGRAMMABLE (H2 IS OPPOSITE POLARITY OF H1)

Figure 15. HBLK Masking Control

zontal sequences. Up to four SCPs are available to divide the readout into four separate regions, as shown in Figure 16. The SCP0 is always hard-coded to line 0, and SCP1–SCP3 are register programmable. During each region bound by the SCP, the SPTR Registers designate which sequence is used by each signal. CLPOB and CLPDM share the same SCP, PBLK has a separate set of SCP, and HBLK shares the vertical RCP (see Vertical Timing Generation section). For example,

CLPSCP1 will define Region 0 for CLPOB and CLPDM, and in that region any of the four individual CLPOB and CLPDM sequences may be selected with the SPTR Registers. The next SCP defines a new region, and in that region each signal can be assigned to a different individual sequence. Because HBLK shares the vertical RCP, there are up to eight regions where HBLK sequences may be changed using the eight HBLKSPTR Registers.

Table III. CLPOB, CLPDM, and PBLK Individual Sequence Parameters

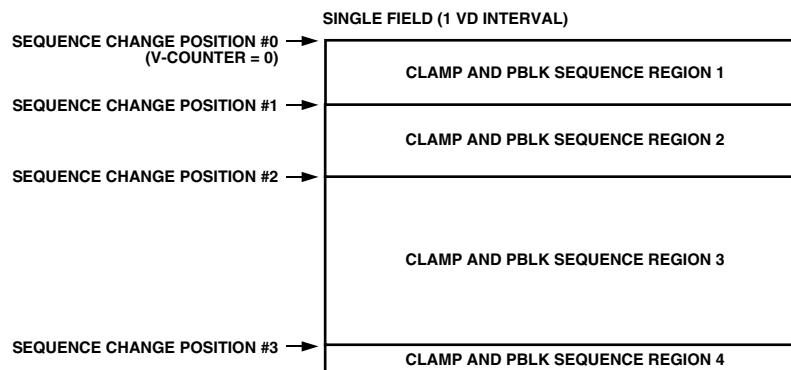| Register	Length	Range	Description
SPOL	1b	High/Low	Starting Polarity of Vertical Transfer Pulse for Sequences 0–3
TOG1	12b	0–4095 Pixel Location	First Toggle Position within Line for Sequences 0–3
TOG2	12b	0–4095 Pixel Location	Second Toggle Position within Line for Sequences 0–3

Table IV. HBLK Individual Sequence Parameters

Register	Length	Range	Description
HBLKMASK	1b	High/Low	Masking Polarity for H1 for Sequences 0–3 (0 = H1 Low, 1 = H1 High)
HBLKTOG1	12b	0–4095 Pixel Location	First Toggle Position within Line for Sequences 0–3
HBLKTOG2	12b	0–4095 Pixel Location	Second Toggle Position within Line for Sequences 0–3

Table V. Horizontal Sequence Control Parameters for CLPOB, CLPDM, and PBLK

Register	Length	Range	Description
SCP1–SCP3	12b	0–4095 Line Number	CLPOB/PBLK SCP to Define Horizontal Regions 0–3
SPTR0–SPTR3	2b	0–3 Sequence Number	Sequence Pointer for Horizontal Regions 0–3

Table VI. Horizontal Sequence Control Parameters for HBLK

Register	Length	Range	Description
VTPRCP1–VTPRCP7	12b	0–4095 Line Number	Vertical Region Change Positions (See Table IX.)
HBLKSPTR0–HBLKSPTR7	2b	0–3 Sequence Number	Sequence Pointer for HBLK Regions 0–7

SINGLE FIELD (1 VD INTERVAL)

SEQUENCE CHANGE POSITION #0 (V-COUNTER = 0) →

CLAMP AND PBLK SEQUENCE REGION 1

SEQUENCE CHANGE POSITION #1 →

CLAMP AND PBLK SEQUENCE REGION 2

SEQUENCE CHANGE POSITION #2 →

CLAMP AND PBLK SEQUENCE REGION 3

SEQUENCE CHANGE POSITION #3 →

CLAMP AND PBLK SEQUENCE REGION 4

UP TO FOUR INDIVIDUAL HORIZONTAL CLAMP AND BLANKING REGIONS MAY BE PROGRAMMED WITHIN A SINGLE FIELD, USING THE SEQUENCE CHANGE POSITIONS.

Figure 16. Clamp and Blanking Sequence Flexibility

VERTICAL TIMING GENERATION

The AD9891/AD9895 provide a very flexible solution for generating vertical CCD timing and can support multiple CCDs and different system architectures. The 4-phase vertical transfer clocks V1–V4 are used to shift each line of pixels into the horizontal output register of the CCD. The AD9891/AD9895 allow these outputs to be individually programmed into different pulse patterns. Vertical sequence control registers then organize the individual vertical pulses into the desired CCD vertical timing arrangement.

Figure 17 shows an overview of how the vertical timing is generated in three basic steps. First, the individual pulse patterns or sequences are created by using the Vertical Transfer Pulse (VTP) Registers. These sequences are a essentially a "pool" of pulse patterns that may be assigned to any of the V1-V4 outputs. Second, individual regions are built by assigning a sequence to each of the V1–V4 outputs. Up to five unique regions may be specified. Finally, the readout of the entire field is constructed by combining one or more of the individual regions sequentially. With up to eight region areas available, different steps of the readout such as high speed line shifts and vertical image transfer can be supported.
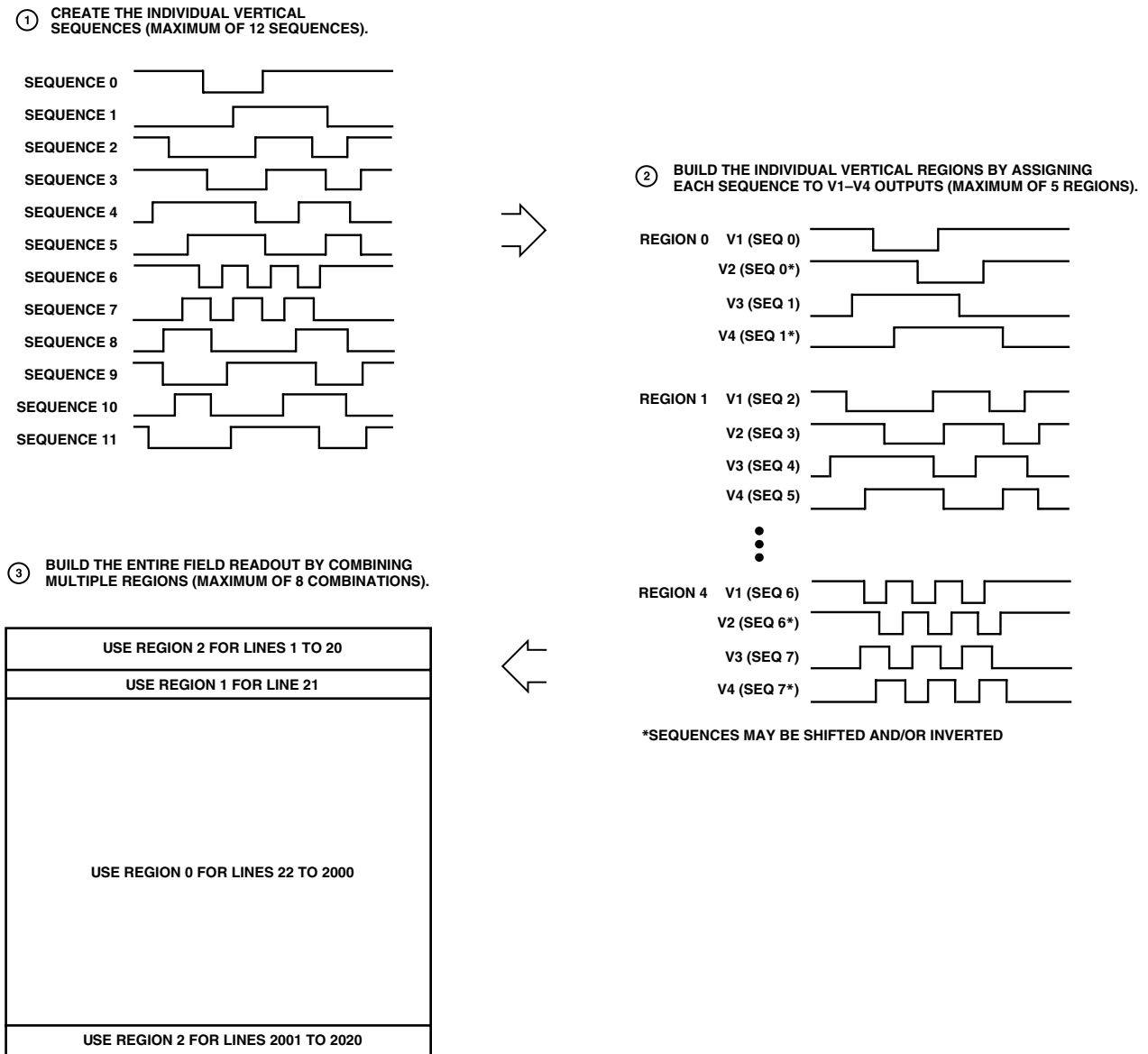
① CREATE THE INDIVIDUAL VERTICAL SEQUENCES (MAXIMUM OF 12 SEQUENCES).

SEQUENCE 0
SEQUENCE 1
SEQUENCE 2
SEQUENCE 3
SEQUENCE 4
SEQUENCE 5
SEQUENCE 6
SEQUENCE 7
SEQUENCE 8
SEQUENCE 9
SEQUENCE 10
SEQUENCE 11

② BUILD THE INDIVIDUAL VERTICAL REGIONS BY ASSIGNING EACH SEQUENCE TO V1–V4 OUTPUTS (MAXIMUM OF 5 REGIONS).

REGION 0   V1 (SEQ 0)
V2 (SEQ 0*)
V3 (SEQ 1)
V4 (SEQ 1*)

REGION 1   V1 (SEQ 2)
V2 (SEQ 3)
V3 (SEQ 4)
V4 (SEQ 5)

REGION 4   V1 (SEQ 6)
V2 (SEQ 6*)
V3 (SEQ 7)
V4 (SEQ 7*)

*SEQUENCES MAY BE SHIFTED AND/OR INVERTED

③ BUILD THE ENTIRE FIELD READOUT BY COMBINING MULTIPLE REGIONS (MAXIMUM OF 8 COMBINATIONS).

USE REGION 2 FOR LINES 1 TO 20

USE REGION 1 FOR LINE 21

USE REGION 0 FOR LINES 22 TO 2000

USE REGION 2 FOR LINES 2001 TO 2020

Figure 17. Summary of Vertical Timing Generation

Individual Vertical Sequences

To generate the individual vertical sequences or patterns shown in Figure 18, five registers are required for each sequence. Table VII summarizes these registers and their respective bit lengths. The start polarity (VTPPOL) determines the starting polarity of the vertical sequence and can be programmed high or low. The first toggle position (VTPTOG1) and second toggle position (VTPTOG2) are the pixel locations within the line where the pulse transitions. A third toggle position (VTPTOG3) is also available for sequences 0 through 7. All toggle positions are 10-bit values, which limits the placement of a pulse to within 1024 pixels of a line. A separate register, VSTART, sets the start position of the sequence within the line (see Individual Vertical Regions section). The Length (VTPLEN) Register determines the number of pixels between each of the pulse repetitions, if any repetitions have been programmed. The number of repetitions (VTPREP) simply determines the number of pulse repetitions desired within a single line. Programming "1" for VTPREP gives a single pulse, while setting to "0" will provide a fixed dc output based on the start polarity value. There is a total of 12 individual sequences that may be programmed.

When specifying the individual regions, each sequence may be assigned to any of the V1–V4 outputs. For example, Figure 19 shows a typical 4-phase V-clock arrangement. Two different sequences are needed to generate the different pulsewidths. The use of individual start positions for V1–V4 allows the four outputs to be generated from two sequences. Figure 20 shows a slightly different V-clock arrangement in which V2, V3, and V4 are simply shifted and/or inverted versions of V1. Only one individual sequence is needed because all signals have the same pulsewidth. The invert sequence registers (VINV) are used for V3 and V4 (see Table VII).

Note that for added flexibility, the VTPPOL Registers (Start Polarity) may be used as an extra toggle position.

Table VII. Individual VTP Sequence Parameters

Register	Length	Range	Description
VTPPOL	1b	High/Low	Starting Polarity of Vertical Transfer Pulse for Each Sequence 0–11
VTPTOG1	10b	0–1023 Pixel Location	First Toggle Position within Line for Each Sequence 0–11
VTPTOG2	10b	0–1023 Pixel Location	Second Toggle Position within Line for Each Sequence 0–11
VTPTOG3	10b	0–1023 Pixel Location	Third Toggle Position within Line for Each Sequence 0–7
VTPLEN	10b	0–1023 Pixels	Length between Pulse Repetitions for Each Sequence 0–11
VTPREP	12b	0–4095 Pulses	Number of Pulse Repetitions for Each Sequence 0–11 (0 = DC Output)

PROGRAMMABLE SETTINGS FOR EACH SEQUENCE:
1: START POLARITY
2: 1ST TOGGLE POSITION
3: 2ND TOGGLE POSITION (THERE IS ALSO A 3RD TOGGLE POSITION AVAILABLE FOR SEQUENCES 0 TO 7)
4: LENGTH BETWEEN REPEATS
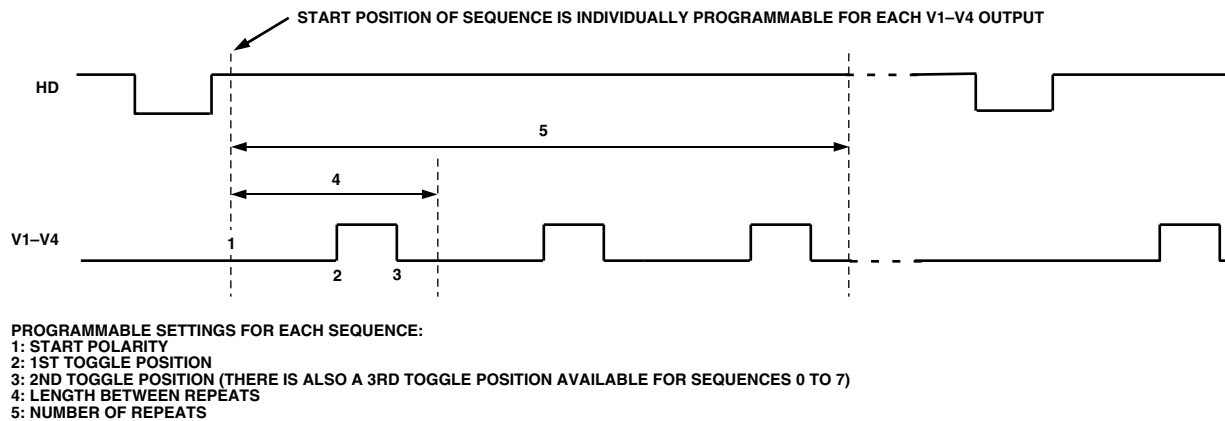5: NUMBER OF REPEATS

Figure 18. Individual Vertical Sequence Programmability
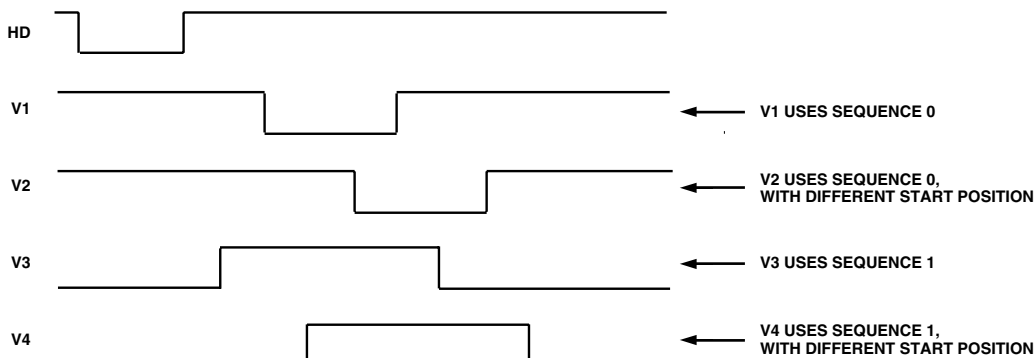

Figure 19. Example of Separate V1–V4 Signals Using Two Individual Sequences

Individual Vertical Regions
The AD9891/AD9895 arranges the individual sequences into re-gions through the use of Sequence Pointers (SPTR). Within each region, different sequences may be assigned to each V-clock output. Figure 21 shows the programmability of each region and Table VIII summarizes the registers needed for generating each region.

For each individual region, the line length (in pixels) is programmable using the HDLEN Registers. Each region can have a different line length to accommodate various image readout techniques. The maximum number of pixels per line is 4096. Also unique to each region are the sequence start positions for each V-output, which are programmed using the VSTART Registers. Each VSTART is a 12-bit value, allowing the start position to be placed anywhere in the line. There are five HDLEN Registers, one for each region. There is a total of 20 VSTART Registers: one for each V1–V4 output, for five different regions.

Note that the last line of the field is separately programmable using the HDLASTLEN Register.

The Sequence Pointer registers VxSPTRFIRST and VxSPTRSECOND assign the individual vertical sequences to each of the V-clock outputs (V1–V4) within a given region. Typically, only the SPTRFIRST Registers are used, with the SPTRSECOND Registers reserved for generating line-by-line alternation (see Vertical Sequence Alternation). Any of the 12 individual sequences may also be inverted using the VxINVFIRST and VxINVSECOND Registers, effectively dou-bling the number of sequences available. There is one SPTRFIRST Register for each V-output, for a total of four regis-ters per region. If all five regions are used, there is a total of 20 SPTRFIRST Registers. There is also the same number of SPTRSECOND Registers, if alternation is required. Note that the SPTR Registers are four bits wide; if a value greater than 11 is programmed, the Vx output will be dc at the level of the VxINV Register.
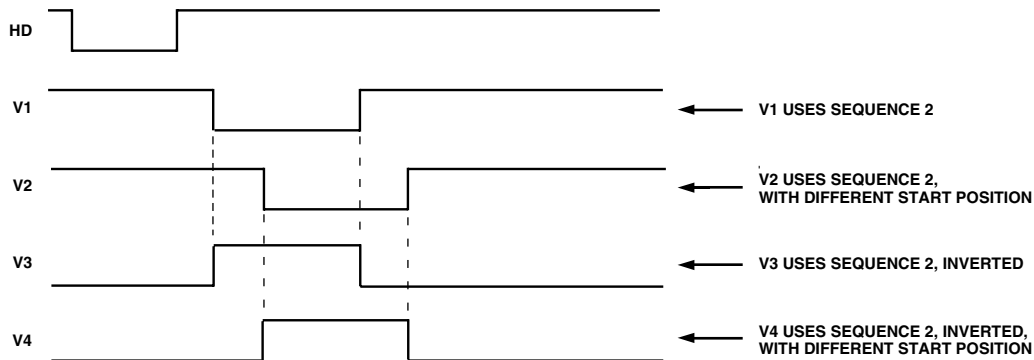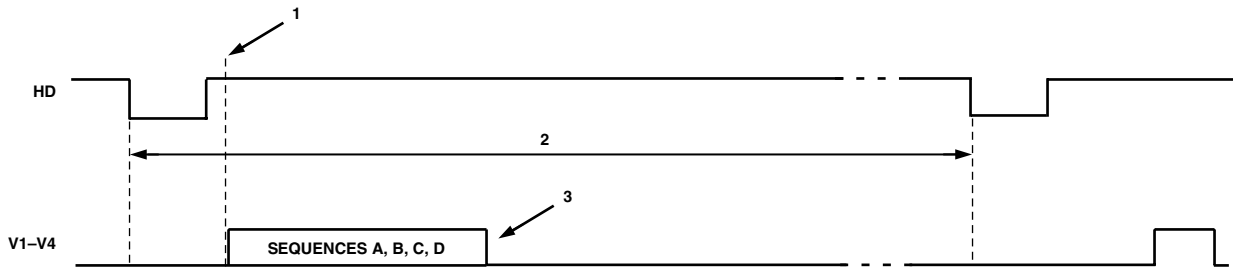

Figure 20. Example of Inverted V1–V4 Signals Using One Individual Sequence with Inversion

PROGRAMMABLE SETTINGS FOR EACH REGION:
1: START POSITION OF SELECTED SEQUENCE IS SEPARATELY PROGRAMMABLE FOR EACH OUTPUT
2: HD LINE LENGTH
3: SEQUENCE POINTERS (SPTR) TO SELECT AN INDIVIDUAL SEQUENCE FOR EACH OUTPUT
4: ANY SEQUENCES MAY ALSO BE ALTERNATED FOR ADDITIONAL FLEXIBILITY

Figure 21. Individual Vertical Region Programmability

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Table VIII. Individual Vertical Region Parameters

Register	Length	Range	Description
HDLEN	12b	0–4095 Pixels	HD Line Length for Lines in Each Region 0–4
VxSTART	12b	0–4095 Pixel Location	Sequence Start Position for Each Vx Output in Each Region 0–4
VxSPTRFIRST	4b	Sequence 0–11	Sequence Pointer for Vx Output during Each Region 0–4 (Can Be Used with SPTRSECOND for Alternation, See Text)
VxINVFIRST	1b	High/Low	When High, the Polarity of Sequence VxSPTRFIRST Is Inverted

x is the V-output from 1–4.

Complete Field: Combining the Regions

The individual regions are combined into a complete field readout by using region change positions (RCP) and region pointers (REGPTR). Figure 22 shows how each field is divided into multiple regions. This allows the user to change the vertical timing during various stages of the image readout. The boundaries of each region are defined by the sequence change positions (RCP). Each RCP is a 12-bit value representing the line number bounding the region. A total of seven RCPs allow up to eight

different region areas in the field to be defined. The first RCP is always hard-coded to zero, and the remaining seven are register programmable. Note that there are only five possible individual regions that can be defined, but the eight region areas allow the same region to be used in more than one place during the field. Within each region area, the region pointers specify which of the five individual regions will be used. There are eight region pointers, one for each region area. Table IX summarizes the registers for the region change positions and region pointers.
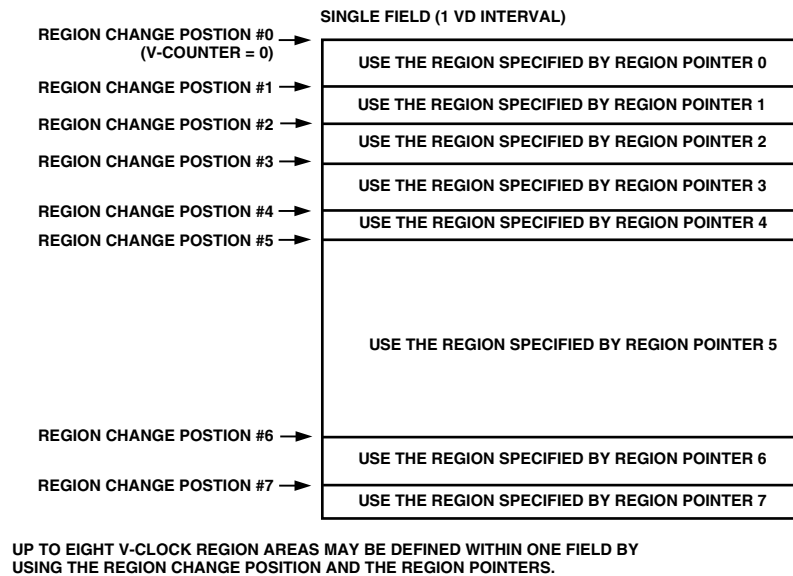

Figure 22. Complete Field Using Multiple Region Areas

Table IX. Complete Vertical Field Registers

Register	Length	Range	Description
VTPRCP	12b	0–4095 Line Location	Region Change Position for each Region Area in Field
VTPREGPTR	3b	Region 0–4	Region Pointer for each Region Area of Field

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Vertical Sequence Alternation

The AD9891/AD9895 also supports line-by-line alternation of vertical sequences within any region, as shown in Figure 23. Table X summarizes the additional registers used to support different alternation patterns. To create an alternating vertical pattern, the VxSPTRFIRST and VxSPTRSECOND Registers are programmed with the desired sequences to be alternated. The VTPALT Register must be set HIGH for that region to use alternation. If VTPALT is LOW, then the VxSPTRSECOND Registers will be ignored. Figure 24 shows an example of line-by-line alternation.
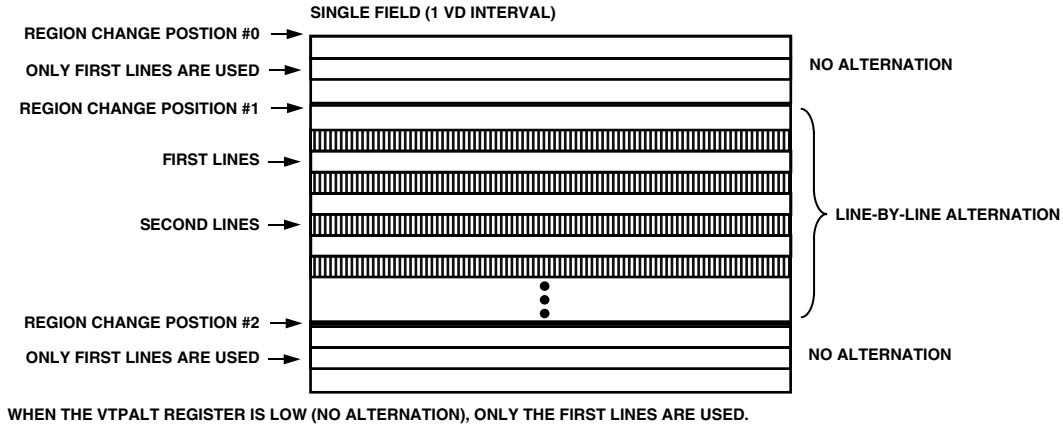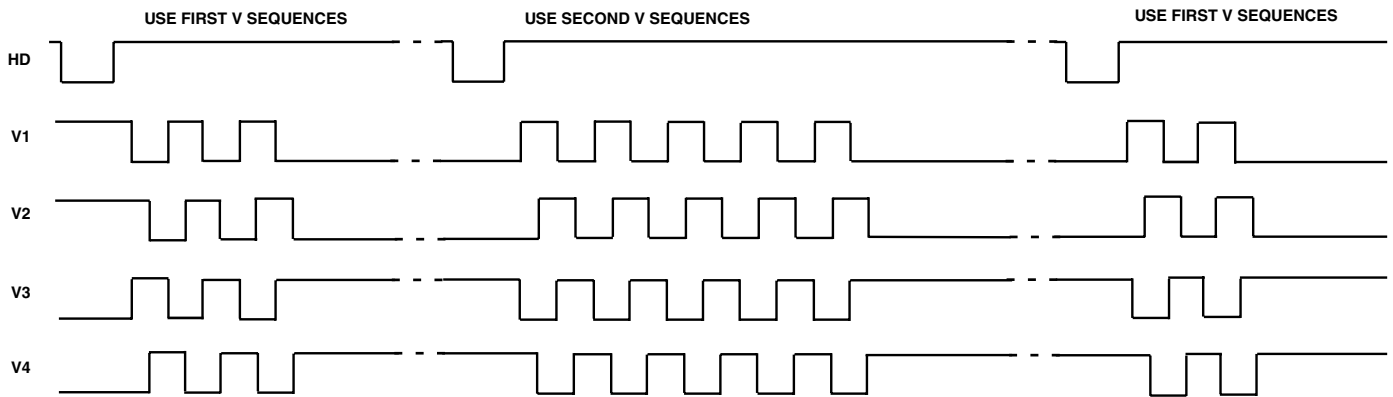

Figure 23. Use of Line Alteration in Vertical Sequencing

Figure 24. Example of Line Alteration within a Region

Table X. Vertical Sequence Alternation Parameters

Register	Length	Range	Description
VTPALT	1b	Enabled/Disabled	Enables the Line-by-Line Alternation (1 = Enabled)
VxSPTRFIRST	4b	Sequence 0–11	SPTR for Vx Output during Each Region 0–4 for FIRST Lines
VxINVFIRST	1b	High/Low	When High, the Polarity of VxSPTRFIRST Is Inverted
VxSPTRSECOND	4b	Sequence 0–11	SPTR for Vx Output during Each Region 0–4 for SECOND Lines
VxINVSECOND	1b	High/Low	When High, the Polarity of VxSPTRSECOND Is Inverted

x is the V-output from 1–4.

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Second Vertical Sequence During VSG Lines

Most CCDs require additional vertical timing during the sensor gate line. The AD9891/AD9895 supports the option to output a second set of sequences for V1–V4 during the line when the sensor gates VSG1–VSG4 are active. Figure 25 shows a typical VSG line, which includes two separate sets of vertical sequences on V1–V4. The sequences at the start of the line are the same as those generated in the previous line. But the second sequence only occurs in the line where the VSG signals are active. To select the sequences used for the second sequence, the registers in Table XI are used. To enable the second set of sequences during the VSG line, the VTP_SGLINEMODE is set HIGH. As with the standard vertical regions, each V1–V4 output has an individual start position, programmed in the VxSTART_SGLINE Registers. Each V1–V4 output can select from the pool of 12 unique sequences using individual sequence pointer registers, VxSPTR_SGLINE. Also, any sequence may be inverted for a particular V1–V4 output by using the VxINV_SGLINE Registers.

Vertical Sweep Mode Operation

The AD9891/AD9895 contains a special mode of vertical timing operation called Sweep Mode. This mode is used to generate a large number of repetitive pulses that span across multiple HD lines. One example of where this mode may be needed is at the start of the CCD readout operation. At the end of the image exposure, but before the image is transferred by the sensor gate pulses, the vertical interline CCD Registers should be "clean" of all charge. This can be accomplished by quickly shifting out any charge with a long series of pulses on the V1–V4 outputs. Depending on the vertical resolution of the CCD, up to two or three thousand clock cycles will be needed to shift the charge out of each vertical CCD line. This operation will span across multiple HD line lengths. Normally, the AD9891/AD9895 sequences are contained within one HD line length. But when Sweep Mode is enabled, the HD boundaries will be ignored until the region is finished. To enable Sweep Mode within any region, program the appropriate SWEEP (0–4) Registers to HIGH.

Figure 26 shows an example of the Sweep Mode operation. The number of vertical pulses needed will depend on the vertical resolution of the CCD. The V1–V4 output signals are generated using the Individual Vertical Sequence Registers (shown in Table VII). A single pulse is created using the first, second, and third toggle positions, and then the number of repeats is set to the number of vertical shifts required by the CCD. The maximum number of repeats is 4096 in this mode, using the VTPREP Register. This produces a pulse train of the appropriate length. Normally, the pulse train would be truncated at the end of the HD line length. But with Sweep Mode enabled for this region, the HD boundaries will be ignored. In Figure 26, the sweep region occupies 23 HD lines. After the Sweep Mode region is completed, normal sequence operation will resume in the next region.

Table XI. Second Vertical Sequence Registers During SG Lines

Register Name	Length	Range	Description
VTP_SGLINEMODE	1b	HIGH/LOW	To Turn on Second Sequences during SG Line, Set = HIGH
VxSTART_SGLINE	12b	0–4095 Pixel Location	Sequence Start Position for Each Vx Output for SG Line Sequence
VxSPTR_SGLINE	4b	0–11 Sequence #	Sequence Pointer for Vx Output during second SG Line Sequence
VxINV_SGLINE	1b	HIGH/LOW	When HIGH, the Polarity of Sequence VxSPTRFIRST Is Inverted

x is the V-output from 1–4.
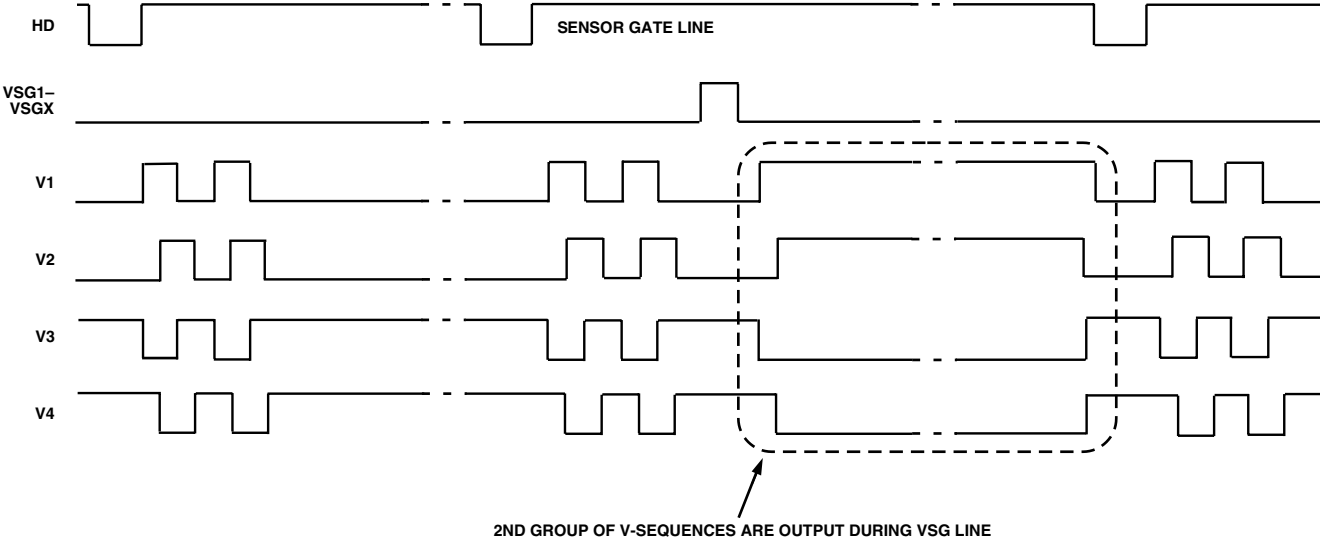
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2ND GROUP OF V-SEQUENCES ARE OUTPUT DURING VSG LINE
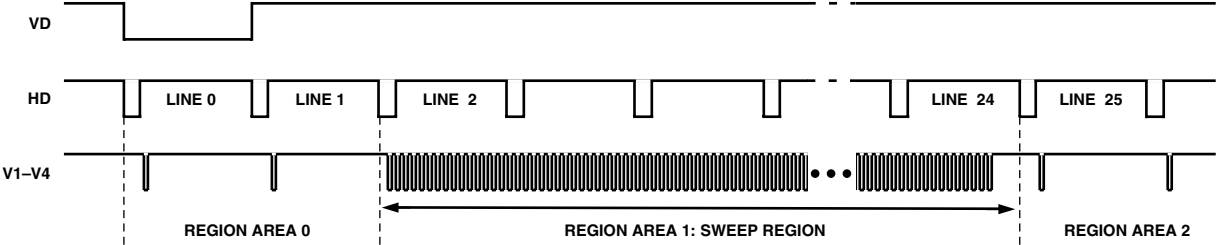
Figure 25. Example of Second Sequences During Sensor Gate Line

Figure 26. Example of Sweep Region for High Speed Vertical Shift

Vertical Multiplier Mode

To generate very wide vertical timing pulses, a vertical region may be configured into Multiplier Mode. This mode uses the vertical sequence registers in a slightly different manner. Multiplier Mode can be used to support unusual CCD timing requirements, such as vertical pulses that are wider than a single HD line length.

The start polarity and toggle positions are still used in the same manner as the standard sequence generation, but the length is used differently. Instead of using the pixel counter (HD counter) to specify the toggle position locations (VTPTOG1, 2, 3) of the sequence, VTP length (VTPLEN) is multiplied by the VTPTOG position to allow very long sequences to be generated. To calculate the exact toggle position, counted in pixels after the start position:
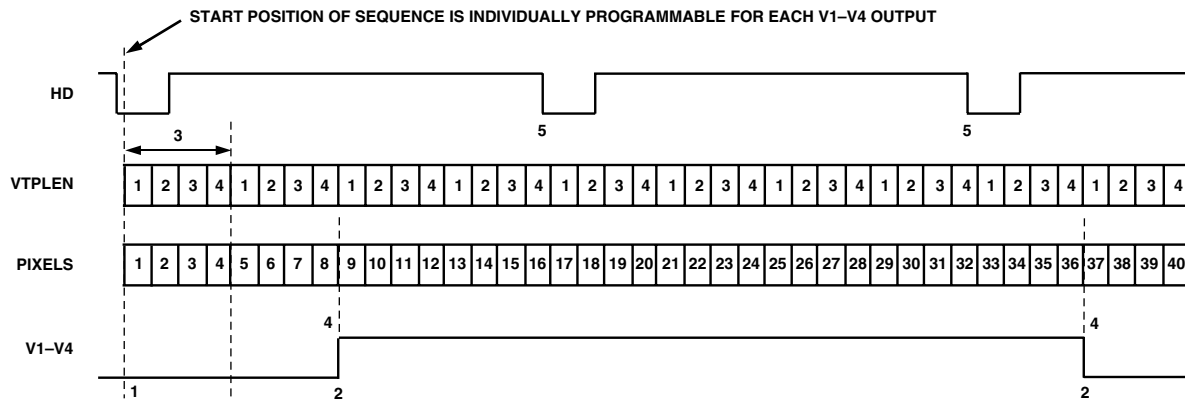
$$Multiplier\ Toggle\ Position = VTPTOG \times VTPLEN$$

Because the *VTPTOG* Register is multiplied by *VTPLEN*, the resolution of the toggle position placement is reduced. If *VTPLEN* = 4, the toggle position accuracy is now reduced to 4-pixel steps instead of single pixel steps. Table XII summarizes how the Individual Vertical Sequence Registers are programmed for Multiplier Mode operation. Note that the bit ranges for the VTPTOG and VTPREP Registers differ from the normal operation shown in Table VII. In Multiplier Mode, the VTPREP Register should always be programmed to the same value as the highest toggle position register.

The example shown in Figure 27 illustrates this operation. The first toggle position is 2 and the second toggle position is 9. In Nonmultiplier Mode, this would cause the V-sequence to toggle at pixel 2 and then pixel 9 within a single HD line. However, now toggle positions are multiplied by the VTPLEN = 4, so the first toggle occurs at pixel count = 8, and the second toggle occurs at pixel count = 36. Sweep Mode should be enabled to allow the toggle positions to cross the HD line boundaries.

Frame Transfer CCD Mode

The AD9891/AD9895 may also be configured for use with frame transfer CCDs. In Frame Transfer CCD (FTCCD) Mode, an additional four vertical outputs are available for a total of eight outputs (V1–V8). In this case, V1–V4 are used for clocking the active image area, and V5–V8 are used for clocking the storage area. In FTCCD Mode, the sequences assigned to the V1–V4 outputs are duplicated at the V5–V8 outputs to allow the storage area to be clocked along with the image area. Individual masking of the V1–V4 and V5–V8 outputs allows for vertical decimation techniques during transfer from the image to the storage area. The additional outputs V5–V8 are available on four of the sensor gate output pins, VSG1–VSG4. Figure 28 shows an example of the eight V-clocks configured for use with a frame transfer CCD.

MULTIPLIER MODE VERTICAL SEQUENCE PROPERTIES:
1: START POLARITY (ABOVE: STARTPOL = 0)
2: 1ST, 2ND, AND 3RD TOGGLE POSITIONS (ABOVE: VTPTOG1 = 2, VTPTOG2 = 9)
3: LENGTH OF VTP COUNTER (ABOVE: VTPLEN = 4). THIS IS THE MINIMUM RESOLUTION FOR TOGGLE POSITION CHANGES.
4: TOGGLE POSITIONS OCCUR AT LOCATION EQUAL TO (VTPTOG × VTPLEN)
5: ENABLE SWEEP REGION ALLOWS THE COUNTERS TO CROSS THE HD BOUNDARIES

Figure 27. Example of Multiplier Region for Wide Vertical Pulse Timing

Table XII. Multiplier Mode and Sequence Register Parameters

| Register	Length	Range	Description
MULTI	1b	HIGH/LOW	High Enables Multiplier Mode for Each Region 0–4
VTPPOL	1b	HIGH/LOW	Starting Polarity of Vertical Transfer Pulse for Each Sequence 0–11
VTPTOG1	12b	0–4095 Pixel Location	First Toggle Position for Each Sequence 0–11
VTPTOG2	12b	0–4095 Pixel Location	Second Toggle Position for Each Sequence 0–11
VTPTOG3	12b	0–4095 Pixel Location	Third Toggle Position for Each Sequence 0–7
VTPLEN	10b	0–1023 Pixels	"Multiplier" Factor for Repetition Counter
VTPREP	12b	0–4096	Should Be Programmed to the Same Value as the Highest Toggle Position
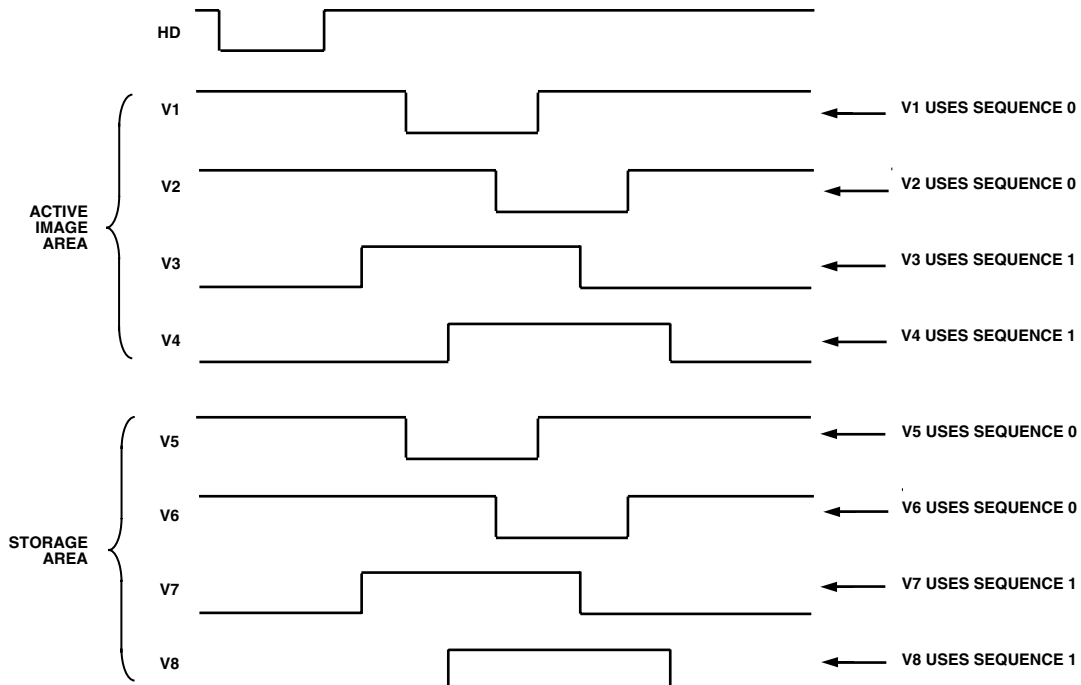
Figure 28. Example of Frame Transfer CCD Mode using V1–V8

The frame transfer CCD also requires additional timing control when decimating the image for Preview Mode. The AD9891/AD9895 contain registers to independently stop the operation of the V5–V8 outputs while the V1–V4 outputs continue to run or to stop the V1–V4 outputs, while the V5–V8 outputs remain operational. The FREEZE and RESUME Registers specify the pixel locations within each line of a region where the V1–V4 or V5–V8 clock outputs will start to hold their state, and where they will resume normal operation. FREEZE and RESUME can be used in any region during the frame readout.

Vertical Sensor Gate (Shift Gate) Timing
With an interline CCD, the vertical sensor gates (VSG) are used to transfer the pixel charges from the light-sensitive image area into the light-shielded vertical registers. When a mechanical shutter is not being used, this transfer will effectively end the exposure period during the image acquisition. From the light-shield vertical registers, the image is then read out line-by-line by using the vertical transfer pulses V1–V4 in conjunction with the high speed horizontal clocks.
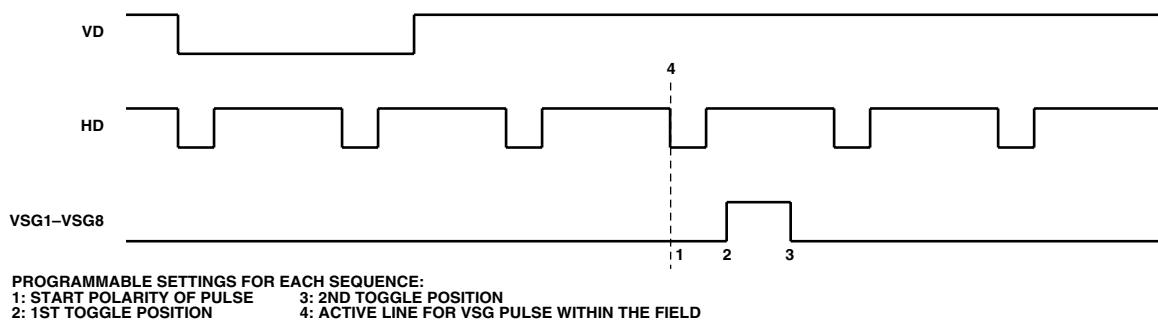

PROGRAMMABLE SETTINGS FOR EACH SEQUENCE:
1: START POLARITY OF PULSE   3: 2ND TOGGLE POSITION
2: 1ST TOGGLE POSITION   4: ACTIVE LINE FOR VSG PULSE WITHIN THE FIELD

Figure 29. Vertical Sensor Gate Pulse Placement

Table XIII. Sensor Gate Register Parameters

Register	Length	Range	Description
SGPOL	1b	High/Low	Sensor Gate Starting Polarity for Sequence 0–3
SGTOG1	12b	0–4095 Pixel Location	First Toggle Position for Sequence 0–11
SGTOG2	12b	0–4095 Pixel Location	Second Toggle Position for Sequence 0–11
SGACTLINE	12b	0–4095 Pixel Location	Line in Field where VSG1–VSG8 Are Active
SGSEL	2b	Sequence 0–3	Selects Sequence 0–3 for VSG1–VSG8
SGMASK	8b	8 Individual Bits	Masking for any of VSG1–VSG8 Signals (0 = On, 1 = Mask)