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1 GSPS, 14-Bit, 3.3 V CMOS Direct Digital Synthesizer

Data Sheet **AD9910**

FEATURES

- 1 GSPS internal clock speed (up to 400 MHz analog output)
- Integrated 1 GSPS, 14-bit DAC
- 0.23 Hz or better frequency resolution
- Phase noise ≤ −125 dBc/Hz @ 1 kHz offset (400 MHz carrier)
- Excellent dynamic performance with
  - >80 dB narrow-band SFDR
- Serial input/output (I/O) control
- Automatic linear or arbitrary frequency, phase, and amplitude sweep capability
- 8 frequency and phase offset profiles
- Sin(x)/(x) correction (inverse sinc filter)
- 1.8 V and 3.3 V power supplies
- Software and hardware controlled power-down
- 100-lead TQFP_EP package
- Integrated 1024 word × 32-bit RAM
- PLL REFCLK multiplier
- Parallel datapath interface
- Internal oscillator can be driven by a single crystal
- Phase modulation capability
- Amplitude modulation capability
- Multichip synchronization

APPLICATIONS

- Agile local oscillator (LO) frequency synthesis
- Programmable clock generators
- FM chirp source for radar and scanning systems
- Test and measurement equipment
- Acousto-optic device drivers
- Polar modulators
- Fast frequency hopping

FUNCTIONAL BLOCK DIAGRAM

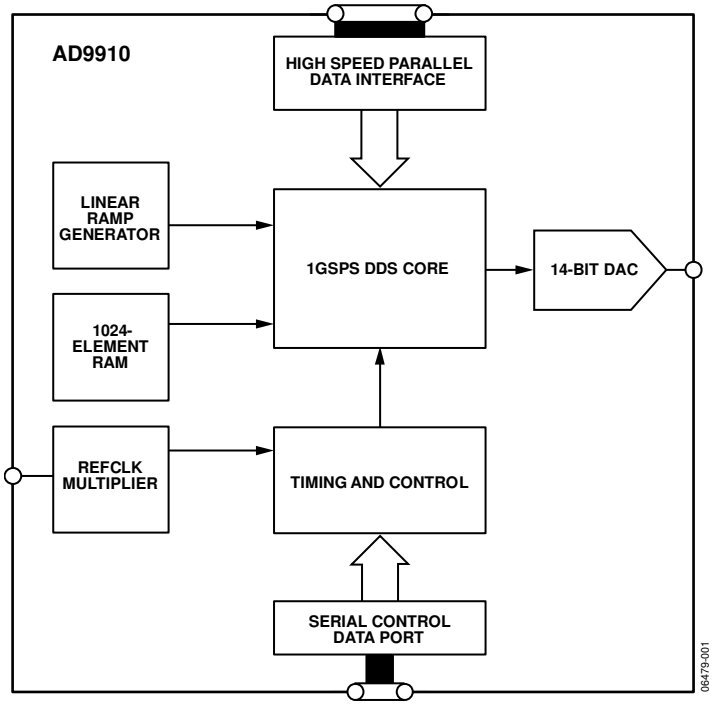

Figure 1.

Rev. E
Document Feedback

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AD9910* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9910 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1389: Recommended Rework Procedure for the Lead Frame Chip Scale Package (LFCSP)
- AN-237: Choosing DACs for Direct Digital Synthesis
- AN-280: Mixed Signal Circuit Technologies
- AN-342: Analog Signal-Handling for High Speed and Accuracy
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-419: A Discrete, Low Phase Noise, 125 MHz Crystal Oscillator for the AD9850
- AN-423: Amplitude Modulation of the AD9850 Direct Digital Synthesizer
- AN-543: High Quality, All-Digital RF Frequency Modulation Generation with the ADSP-2181 and the AD9850 DDS
- AN-557: An Experimenter's Project:
- AN-587: Synchronizing Multiple AD9850/AD9851 DDS-Based Synthesizers
- AN-605: Synchronizing Multiple AD9852 DDS-Based Synthesizers
- AN-621: Programming the AD9832/AD9835
- AN-632: Provisionary Data Rates Using the AD9951 DDS as an Agile Reference Clock for the ADN2812 Continuous-Rate CDR
- AN-769: Generating Multiple Clock Outputs from the AD9540
- AN-772: A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)
- AN-823: Direct Digital Synthesizers in Clocking Applications Time
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-843: Measuring a Loudspeaker Impedance Profile Using the AD5933
- AN-847: Measuring a Grounded Impedance Profile Using the AD5933
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design
- AN-927: Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)

- AN-939: Super-Nyquist Operation of the AD9912 Yields a High RF Output Signal
- AN-953: Direct Digital Synthesis (DDS) with a Programmable Modulus

Data Sheet

- AD9910: 1 GSPS, 14-Bit, 3.3 V CMOS Direct Digital Synthesizer Data Sheet

Product Highlight

- Introducing Digital Up/Down Converters: VersaCOMM™ Reconfigurable Digital Converters

Technical Books

- A Technical Tutorial on Digital Signal Synthesis, 1999

User Guides

- UG-207: Evaluation Board User Guide for AD9910

TOOLS AND SIMULATIONS

- AD9910 IBIS Model

REFERENCE DESIGNS

- CN0109
- CN0121

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

Technical Articles

- 400-MSample DDSs Run On Only +1.8 VDC
- ADI Buys Korean Mobile TV Chip Maker
- Basics of Designing a Digital Radio Receiver (Radio 101)
- DDS Applications
- DDS Circuit Generates Precise PWM Waveforms
- DDS Design
- DDS Device Produces Sawtooth Waveform
- DDS Device Provides Amplitude Modulation
- DDS IC Initiates Synchronized Signals
- DDS IC Plus Frequency-To-Voltage Converter Make Low-Cost DAC
- DDS Simplifies Polar Modulation
- Digital Potentiometers Vary Amplitude In DDS Devices
- Digital Up/Down Converters: VersaCOMM™ White Paper
- Digital Waveform Generator Provides Flexible Frequency Tuning for Sensor Measurement
- Improved DDS Devices Enable Advanced Comm Systems
- Integrated DDS Chip Takes Steps To 2.7 GHz
- Simple Circuit Controls Stepper Motors
- Speedy A/Ds Demand Stable Clocks
- Synchronized Synthesizers Aid Multichannel Systems
- The Year of the Waveform Generator
- Two DDS ICs Implement Amplitude-shift Keying
- Video Portables and Cameras Get HDMI Outputs

DESIGN RESOURCES

- AD9910 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9910 EngineerZone Discussions.

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5/2007—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9910 is a direct digital synthesizer (DDS) featuring an integrated 14-bit DAC and supporting sample rates up to 1 GSPS. The AD9910 employs an advanced, proprietary DDS technology that provides a significant reduction in power consumption without sacrificing performance. The DDS/DAC combination forms a digitally programmable, high frequency, analog output synthesizer capable of generating a frequency agile sinusoidal waveform at frequencies up to 400 MHz.

The user has access to the three signal control parameters that control the DDS: frequency, phase, and amplitude. The DDS provides fast frequency hopping and frequency tuning resolution with its 32-bit accumulator. With a 1 GSPS sample rate, the tuning resolution is ~0.23 Hz. The DDS also enables fast phase and amplitude switching capability.

The AD9910 is controlled by programming its internal control registers via a serial I/O port. The AD9910 includes an integrated static RAM to support various combinations of frequency, phase, and/or amplitude modulation. The AD9910 also supports a user defined, digitally controlled, digital ramp mode of operation. In this mode, the frequency, phase, or amplitude can be varied linearly over time. For more advanced modulation functions, a high speed parallel data input port is included to enable direct frequency, phase, amplitude, or polar modulation.

The AD9910 is specified to operate over the extended industrial temperature range (see the Absolute Maximum Ratings section for details).

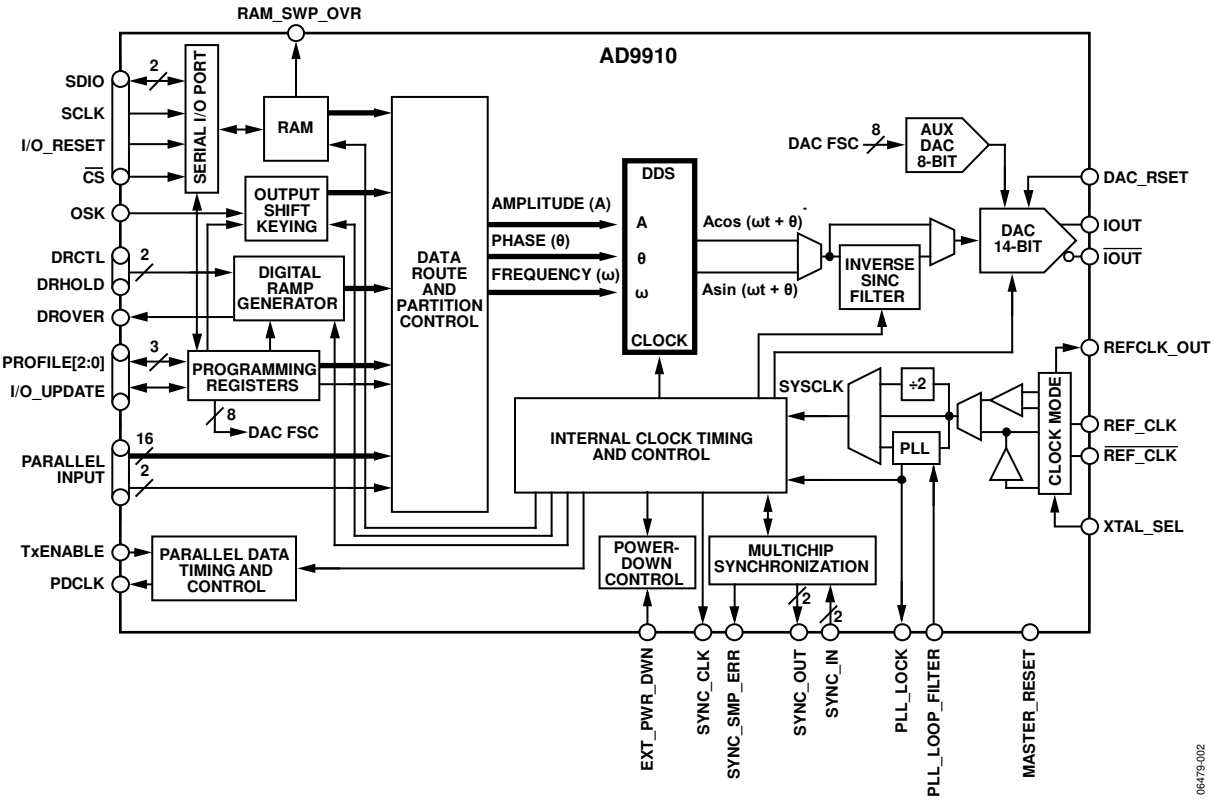


Figure 2. Detailed Block Diagram

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

AVDD (1.8 V) and DVDD (1.8 V) = 1.8 V ± 5%, AVDD (3.3 V) = 3.3 V ± 5%, DVDD_I/O (3.3 V) = 3.3 V ± 5%, T = 25°C, R_{SET} = 10 kΩ, I_{OUT} = 20 mA, external reference clock frequency = 1000 MHz with reference clock (REFCLK) multiplier disabled, unless otherwise noted.

Table 1.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
REFCLK INPUT CHARACTERISTICS					
Frequency Range					
REFCLK Multiplier	Disabled	60		1000	MHz
	Enabled	3.2		60	MHz
Maximum REFCLK Input Divider Frequency	Full temperature range	1500	1900		MHz
Minimum REFCLK Input Divider Frequency	Full temperature range		25	35	MHz
External Crystal			25		MHz
Input Capacitance			3		pF
Input Impedance	Differential		2.8		kΩ
	Single-ended		1.4		kΩ
Duty Cycle	REFCLK multiplier disabled	45		55	%
	REFCLK multiplier enabled	40		60	%
REFCLK Input Level	Single-ended	50		1000	mV p-p
	Differential	100		2000	mV p-p
REFCLK MULTIPLIER VCO CHARACTERISTICS					
VCO Gain (K_V) @ Center Frequency	VCO range Setting 0		429		MHz/V
	VCO range Setting 1		500		MHz/V
	VCO range Setting 2		555		MHz/V
	VCO range Setting 3		750		MHz/V
	VCO range Setting 4		789		MHz/V
	VCO range Setting 5[1]		850		MHz/V
REFCLK_OUT CHARACTERISTICS					
Maximum Capacitive Load			20		pF
Maximum Frequency			25		MHz
DAC OUTPUT CHARACTERISTICS					
Full-Scale Output Current		8.6	20	31.6	mA
Gain Error		−10		+10	% FS
Output Offset				2.3	µA
Differential Nonlinearity			0.8		LSB
Integral Nonlinearity			1.5		LSB
Output Capacitance			5		pF
Residual Phase Noise	@ 1 kHz offset, 20 MHz A_{OUT}				
REFCLK Multiplier	Disabled		−152		dBc/Hz
	Enabled @ 20×		−140		dBc/Hz
	Enabled @ 100×		−140		dBc/Hz
Voltage Compliance Range		−0.5		+0.5	V
Wideband SFDR	See the Typical Performance Characteristics section				
Narrow-Band SFDR					
50.1 MHz Analog Output	±500 kHz		−87		dBc
	±125 kHz		−87		dBc
	±12.5 kHz		−96		dBc
101.3 MHz Analog Output	±500 kHz		−87		dBc
	±125 kHz		−87		dBc
	±12.5 kHz		−95		dBc

Parameter	Conditions/Comments	Min	Typ	Max	Unit
201.1 MHz Analog Output	±500 kHz		–87		dBc
	±125 kHz		–87		dBc
	±12.5 kHz		–91		dBc
301.1 MHz Analog Output	±500 kHz		–86		dBc
	±125 kHz		–86		dBc
	±12.5 kHz		–88		dBc
401.3 MHz Analog Output	±500 kHz		–84		dBc
	±125 kHz		–84		dBc
	±12.5 kHz		–85		dBc
SERIAL PORT TIMING CHARACTERISTICS					
Maximum SCLK Frequency			70		Mbps
Minimum SCLK Clock Pulse Width	Low	4			ns
	High	4			ns
Maximum SCLK Rise/Fall Time			2		ns
Minimum Data Setup Time to SCLK		5			ns
Minimum Data Hold Time to SCLK		0			ns
Maximum Data Valid Time in Read Mode				11	ns
I/O_UPDATE/PROFILE[2:0] TIMING CHARACTERISTICS					
Minimum Setup Time to SYNC_CLK		1.75			ns
Minimum Hold Time to SYNC_CLK		0			ns
I/O_UPDATE Pulse Width	High	>1			SYNC_CLK cycle
Minimum Profile Toggle Period		2			SYNC_CLK cycles
TxENABLE and 16-BIT PARALLEL (DATA) BUS TIMING					
Maximum PDCLK Frequency			250		MHz
TxENABLE/Data Setup Time (to PDCLK)		1.75			ns
TxENABLE/Data Hold Time (to PDCLK)		0			ns
MISCELLANEOUS TIMING CHARACTERISTICS					
Wake-Up Time[2]					
Fast Recovery			8		SYSCLK cycles[3]
Full Sleep Mode	REFCLK multiplier enabled		1		ms
	REFCLK multiplier disabled			150	µs
Minimum Reset Pulse Width High			5		SYSCLK cycles[3]
DATA LATENCY (PIPELINE DELAY)					
Data Latency, Single Tone or Using Profiles					
Frequency, Phase, Amplitude-to-DAC Output	Matched latency enabled and OSK enabled		91		SYSCLK cycles[3]
Frequency, Phase-to-DAC Output	Matched latency enabled and OSK disabled		79		SYSCLK cycles[3]
	Matched latency disabled		79		SYSCLK cycles[3]
Amplitude-to-DAC Output	Matched latency disabled		47		SYSCLK cycles[3]
Data Latency Using RAM Mode					
Frequency, Phase-to-DAC Output	Matched latency enabled/disabled		94		SYSCLK cycles[3]
Amplitude-to-DAC Output	Matched latency enabled		106		SYSCLK cycles[3]
	Matched latency disabled		58		SYSCLK cycles[3]
Data Latency, Sweep Mode					
Frequency, Phase-to-DAC Output	Matched latency enabled/disabled		91		SYSCLK cycles[3]
Amplitude-to-DAC Output	Matched latency enabled		91		SYSCLK cycles[3]
	Matched latency disabled		47		SYSCLK cycles[3]
Data Latency, 16-Bit Input Modulation Mode					
Frequency, Phase-to-DAC Output	Matched latency enabled		103		SYSCLK cycles[3]
	Matched latency disabled		91		SYSCLK cycles[3]

Parameter	Conditions/Comments	Min	Typ	Max	Unit
CMOS LOGIC INPUTS					
Logic 1 Voltage		2.0			V
Logic 0 Voltage				0.8	V
Logic 1 Current			90	150	µA
Logic 0 Current			90	150	µA
Input Capacitance			2		pF
XTAL_SEL INPUT					
Logic 1 Voltage		1.25			V
Logic 0 Voltage				0.6	V
Input Capacitance			2		pF
CMOS LOGIC OUTPUTS	1 mA load				
Logic 1 Voltage		2.8			V
Logic 0 Voltage				0.4	V
POWER SUPPLY CURRENT					
I_{AVDD} (1.8 V)			110		mA
I_{AVDD} (3.3 V)			29		mA
I_{DVDD} (1.8 V)			222		mA
I_{DVDD} (3.3 V)			11		mA
TOTAL POWER CONSUMPTION					
Single Tone Mode			715	950	mW
Rapid Power-Down Mode			330	450	mW
Full Sleep Mode			19	40	mW

[1] The gain value for VCO range Setting 5 is measured at 1000 MHz.
[2] Wake-up time refers to the recovery time from a power-down state. The longest time required is for the reference clock multiplier PLL to relock to the reference. The wake-up time assumes that the recommended PLL loop filter values are used.
[3] SYSCLK cycle refers to the actual clock frequency used on-chip by the DDS. If the reference clock multiplier is used to multiply the external reference clock frequency, the SYSCLK frequency is the external frequency multiplied by the reference clock multiplication factor. If the reference clock multiplier is not used, the SYSCLK frequency is the same as the external reference clock frequency.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
AVDD (1.8V), DVDD (1.8V) Supplies	2 V
AVDD (3.3V), DVDD_I/O (3.3V) Supplies	4 V
Digital Input Voltage	−0.7 V to +4 V
XTAL_SEL	−0.7 V TO +2.2 V
Digital Output Current	5 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
θ_{JA}	22°C/W
θ_{JC}	2.8°C/W
Maximum Junction Temperature	150°C
Lead Temperature (10 sec Soldering)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

EQUIVALENT CIRCUITS

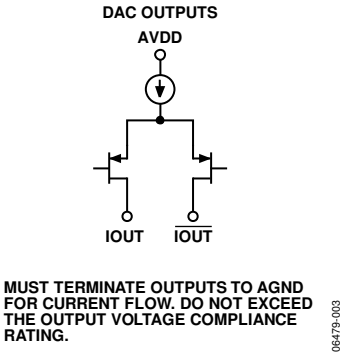


Figure 3. Equivalent Input Circuit

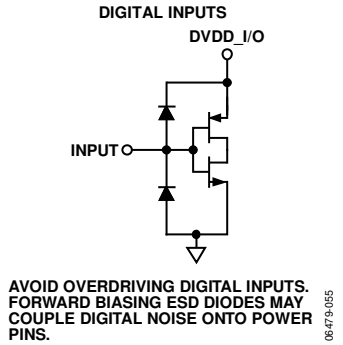
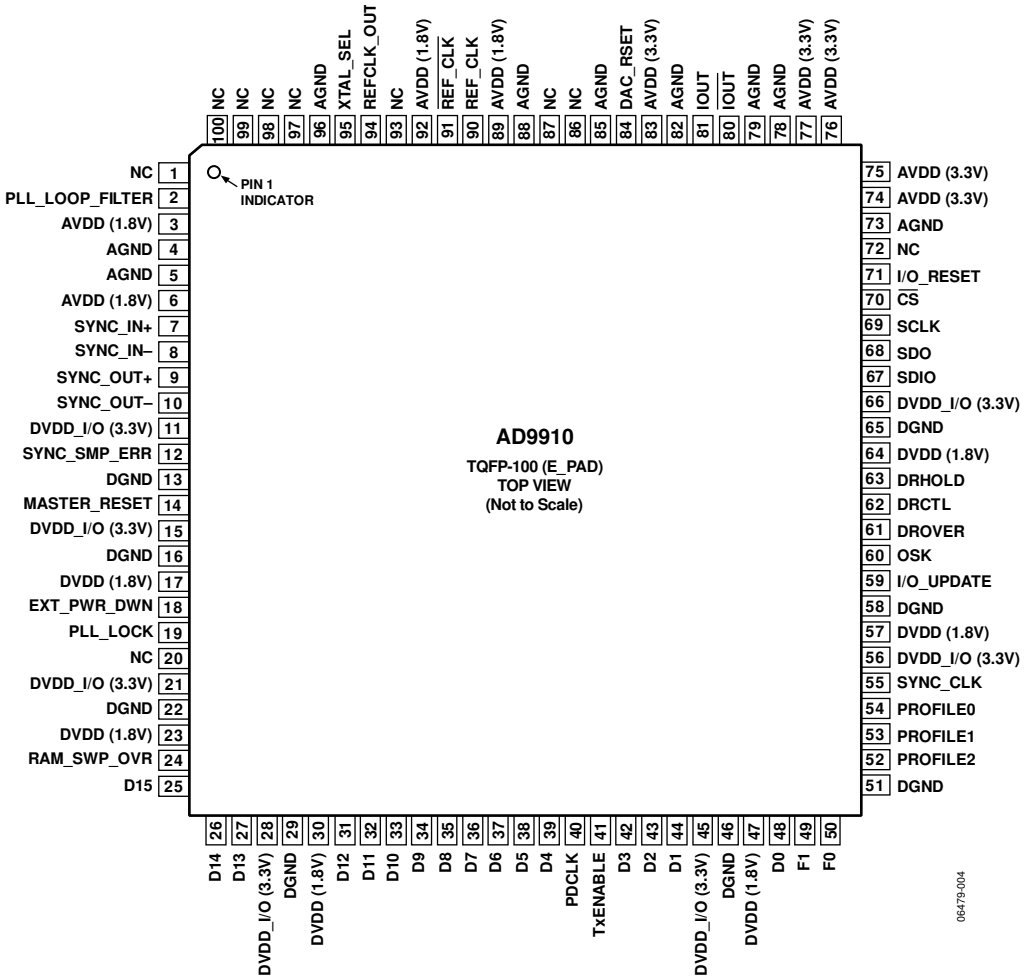


Figure 4. Equivalent Output Circuit

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES:
1. EXPOSED PAD SHOULD BE SOLDERED TO GROUND.
2. NC = NO CONNECT.

Figure 5. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	I/O[1]	Description
1, 20, 72, 86, 87, 93, 97 to 100	NC		Not Connected. Allow device pins to float.
2	PLL_LOOP_FILTER	I	PLL Loop Filter Compensation Pin. See the External PLL Loop Filter Components section for details.
3, 6, 89, 92	AVDD (1.8V)	I	Analog Core VDD, 1.8 V Analog Supplies.
74 to 77, 83	AVDD (3.3V)	I	Analog DAC VDD, 3.3 V Analog Supplies.
17, 23, 30, 47, 57, 64	DVDD (1.8V)	I	Digital Core VDD, 1.8 V Digital Supplies.
11, 15, 21, 28, 45, 56, 66	DVDD_I/O (3.3V)	I	Digital Input/Output VDD, 3.3 V Digital Supplies.
4, 5, 73, 78, 79, 82, 85, 88, 96	AGND	I	Analog Ground.
13, 16, 22, 29, 46, 51, 58, 65	DGND	I	Digital Ground.
7	SYNC_IN+	I	Synchronization Signal (LVDS), Digital Input (Rising Edge Active). The synchronization signal from the external master to synchronize internal subclocks. See the Synchronization of Multiple Devices section for details.
8	SYNC_IN–	I	Synchronization Signal (LVDS), Digital Input. The synchronization signal from the external master to synchronize internal subclocks. See the Synchronization of Multiple Devices section for details.
9	SYNC_OUT+	O	Synchronization Signal (LVDS), Digital Output (Rising Edge Active). The synchronization signal from the internal device subclocks to synchronize external slave devices. See the Synchronization of Multiple Devices section for details.
10	SYNC_OUT–	O	Synchronization Signal (LVDS), Digital Output. The synchronization signal from the internal device subclocks to synchronize external slave devices. See the Synchronization of Multiple Devices section for details.
12	SYNC_SMP_ERR	O	Synchronization Sample Error, Digital Output (Active High). Sync sample error: a high on this pin indicates that the AD9910 did not receive a valid sync signal on SYNC_IN+/SYNC_IN–.
14	MASTER_RESET	I	Master Reset, Digital Input (Active High). Master reset: clears all memory elements and sets registers to default values.
18	EXT_PWR_DWN	I	External Power-Down, Digital Input (Active High). A high level on this pin initiates the currently programmed power-down mode. See the Power-Down Control section for further details. If unused, connect to ground.
19	PLL_LOCK	O	Clock Multiplier PLL Lock, Digital Output (Active High). A high on this pin indicates that the Clock Multiplier PLL has acquired lock to the reference clock input.
24	RAM_SWP_OVR	O	RAM Sweep Over, Digital Output (Active High). A high on this pin indicates that the RAM sweep profile has completed.
25 to 27, 31 to 39, 42 to 44, 48	D[15:0]	I	Parallel Input Bus (Active High).
49, 50	F[1:0]	I	Modulation Format Pins. Digital input to determine the modulation format.
40	PDCLK	O	Parallel Data Clock. This is the digital output (clock). The parallel data clock provides a timing signal for aligning data at the parallel inputs.
41	TxENABLE	I	Transmit Enable. Digital input (active high). In burst mode communications, a high on this pin indicates new data for transmission. In continuous mode, this pin remains high.
52 to 54	PROFILE[2:0]	I	Profile Select Pins. Digital inputs (active high). Use these pins to select one of eight phase/frequency profiles for the DDS. Changing the state of one of these pins transfers the current contents of all I/O buffers to the corresponding registers. State changes should be set up on the SYNC_CLK pin.
55	SYNC_CLK	O	Output Clock Divided-By-Four. A digital output (clock). Many of the digital inputs on the chip, such as I/O_UPDATE and PROFILE[2:0], need to be set up on the rising edge of this signal.

Pin No.	Mnemonic	I/O[1]	Description
59	I/O_UPDATE	I/O	Input/Output Update. Digital input (active high). A high on this pin transfers the contents of the I/O buffers to the corresponding internal registers.
60	OSK	I	Output Shift Keying. Digital input (active high). When the OSK features are placed in either manual or automatic mode, this pin controls the OSK function. In manual mode, it toggles the multiplier between 0 (low) and the programmed amplitude scale factor (high). In automatic mode, a low sweeps the amplitude down to zero, a high sweeps the amplitude up to the amplitude scale factor.
61	DROVER	O	Digital Ramp Over. Digital output (active high). This pin switches to Logic 1 whenever the digital ramp generator reaches its programmed upper or lower limit.
62	DRCTL	I	Digital Ramp Control. Digital input (active high). This pin controls the slope polarity of the digital ramp generator. See the Digital Ramp Generator (DRG) section for more details. If not using the digital ramp generator, connect this pin to Logic 0.
63	DRHOLD	I	Digital Ramp Hold. Digital input (active high). This pin stalls the digital ramp generator in its present state. See the Digital Ramp Generator (DRG) section for more details. If not using a digital ramp generator, connect this pin to Logic 0.
67	SDIO	I/O	Serial Data Input/Output. Digital input/output (active high). This pin can be either unidirectional or bidirectional (default), depending on the configuration settings. In bidirectional serial port mode, this pin acts as the serial data input and output. In unidirectional mode, it is an input only.
68	SDO	O	Serial Data Output. Digital output (active high). This pin is only active in unidirectional serial data mode. In this mode, it functions as the output. In bidirectional mode, this pin is not operational and should be left floating.
69	SCLK	I	Serial Data Clock. Digital clock (rising edge on write, falling edge on read). This pin provides the serial data clock for the control data path. Write operations to the AD9910 use the rising edge. Readback operations from the AD9910 use the falling edge.
70	$\overline{CS}$	I	Chip Select. Digital input (active low). This pin allows the AD9910 to operate on a common serial bus for the control data path. Bringing this pin low enables the AD9910 to detect serial clock rising/falling edges. Bringing this pin high causes the AD9910 to ignore input on the serial data pins.
71	I/O_RESET	I	Input/Output Reset. Digital input (active high). This pin can be used when a serial I/O communication cycle fails (see the I/O_RESET—Input/Output Reset section for details). When not used, connect this pin to ground.
80	$\overline{IOUT}$	O	Open-Drain DAC Complementary Output Source. Analog output (current mode). Connect through a 50 Ω resistor to AGND.
81	IOUT	O	Open-Drain DAC Output Source. Analog output (current mode). Connect through a 50 Ω resistor to AGND.
84	DAC_RSET	O	Analog Reference Pin. This pin programs the DAC output full-scale reference current. Attach a 10 kΩ resistor to AGND.
90	REF_CLK	I	Reference Clock Input. Analog input. When the internal oscillator is engaged, this pin can be driven by either an external oscillator or connected to a crystal. See the REF_CLK/ Overview section for more details.
91	$\overline{REF\_CLK}$	I	Reference Clock Input. Analog input. See the REF_CLK/ Overview section for more details.
94	REFCLK_OUT	O	Crystal Output. Analog output. See the REF_CLK/ Overview section for more details.
95	XTAL_SEL	I	Crystal Select (1.8 V Logic). Analog input (active high). Driving the XTAL_SEL pin high, the AVDD (1.8V) pin enables the internal oscillator to be used with a crystal resonator. If unused, connect it to AGND.
EPAD	Exposed Paddle (EPAD)		The EPAD should be soldered to ground.

[1] I = input, O = output.

TYPICAL PERFORMANCE CHARACTERISTICS

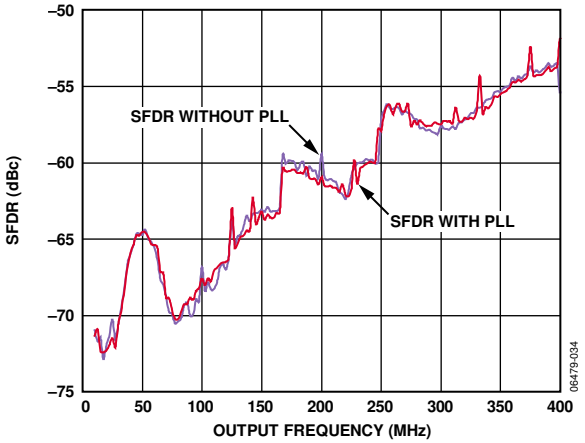


Figure 6. Wideband SFDR vs. Output Frequency (PLL with Reference Clock = 15.625 MHz × 64)

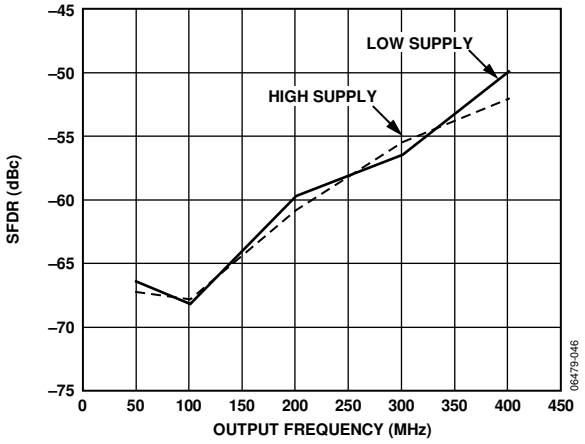


Figure 7. Wideband SFDR vs. Output Frequency and Supply (±5%), REFCLK = 1 GHz

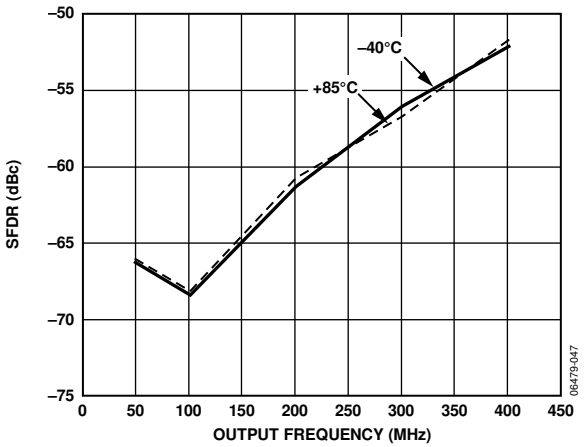


Figure 8. Wideband SFDR vs. Output Frequency and Temperature, REFCLK = 1 GHz

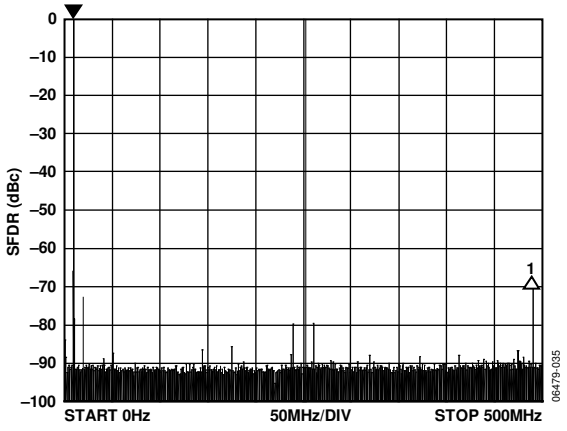


Figure 9. Wideband SFDR at 10 MHz, REFCLK = 1 GHz

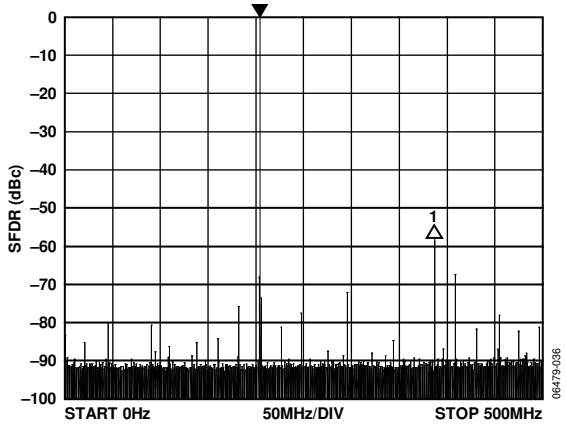


Figure 10. Wideband SFDR at 204 MHz, REFCLK = 1 GHz

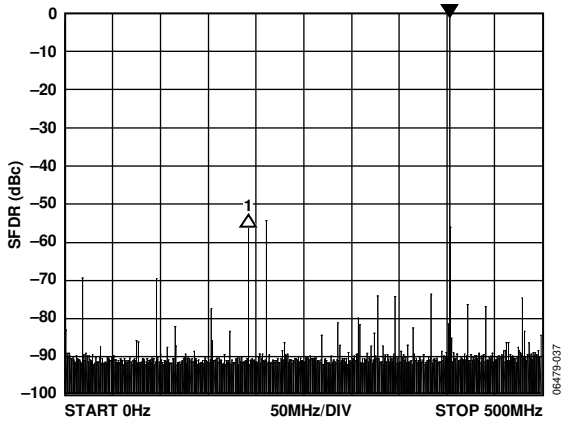


Figure 11. Wideband SFDR at 403 MHz, REFCLK = 1 GHz

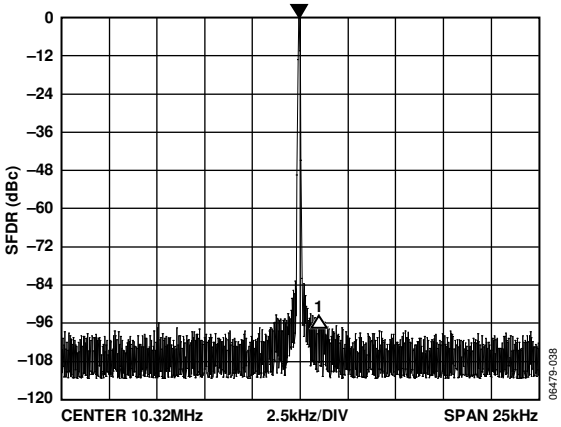


Figure 12. Narrow-Band SFDR at 10.32 MHz, REFCLK = 1 GHz

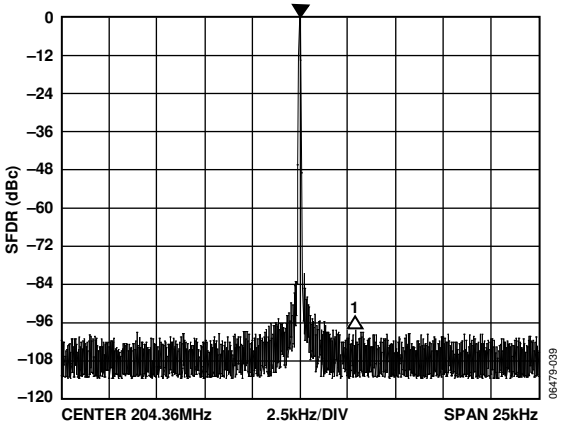


Figure 13. Narrow-Band SFDR at 204.36 MHz, REFCLK = 1 GHz

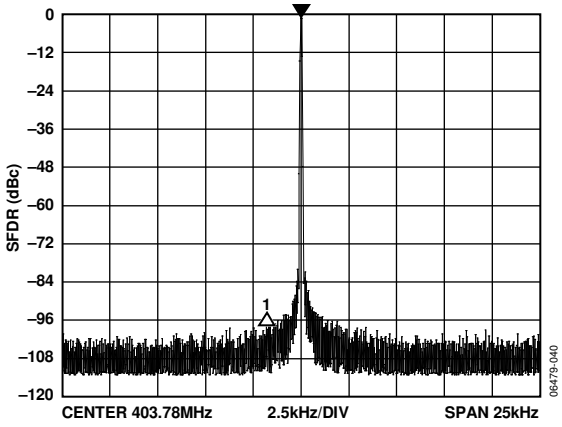


Figure 14. Narrow-Band SFDR at 403.78 MHz, REFCLK = 1 GHz

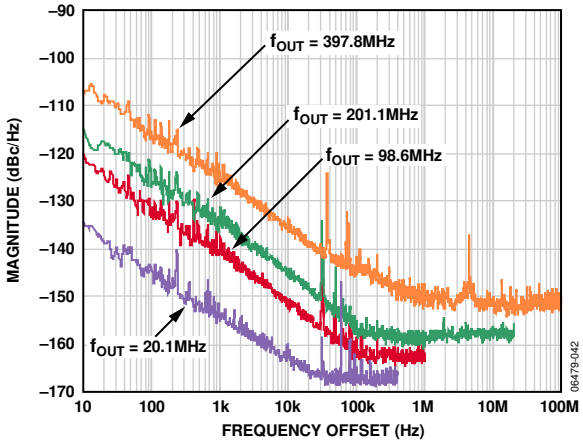


Figure 15. Residual Phase Noise Plot, 1 GHz Operation with PLL Disabled

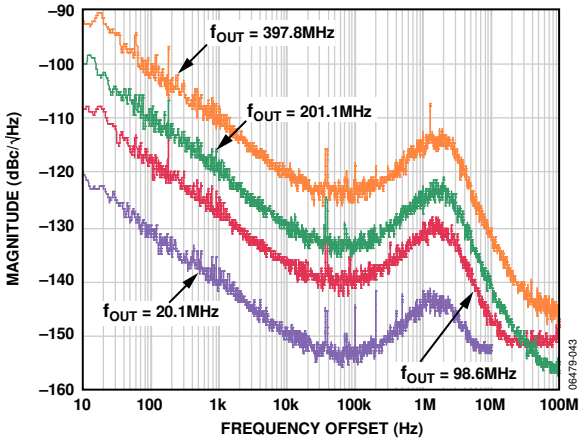


Figure 16. Residual Phase Noise,
1 GHz Operation Using a 50 MHz Reference Clock with 20× PLL Multiplier

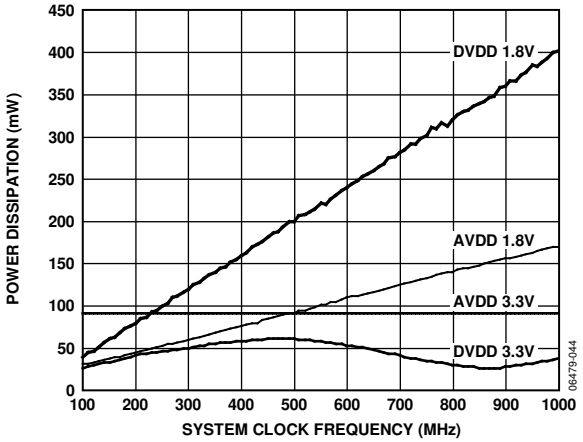


Figure 17. Power Dissipation vs. System Clock Frequency (PLL Disabled)

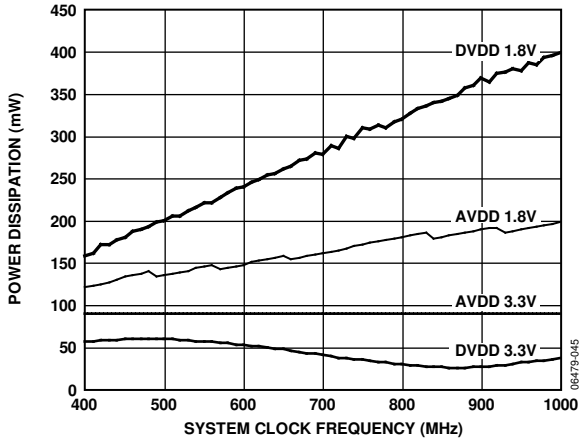


Figure 18. Power Dissipation vs. System Clock Frequency (PLL Enabled)

APPLICATION CIRCUITS

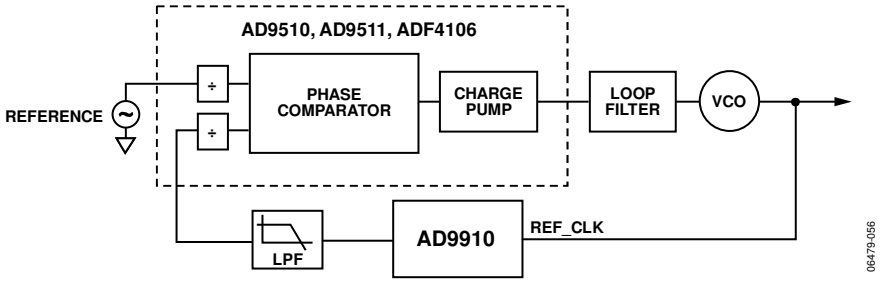


Figure 19. DDS in PLL Feedback Locking to Reference, Offering Fine Frequency and Delay Adjust Tuning

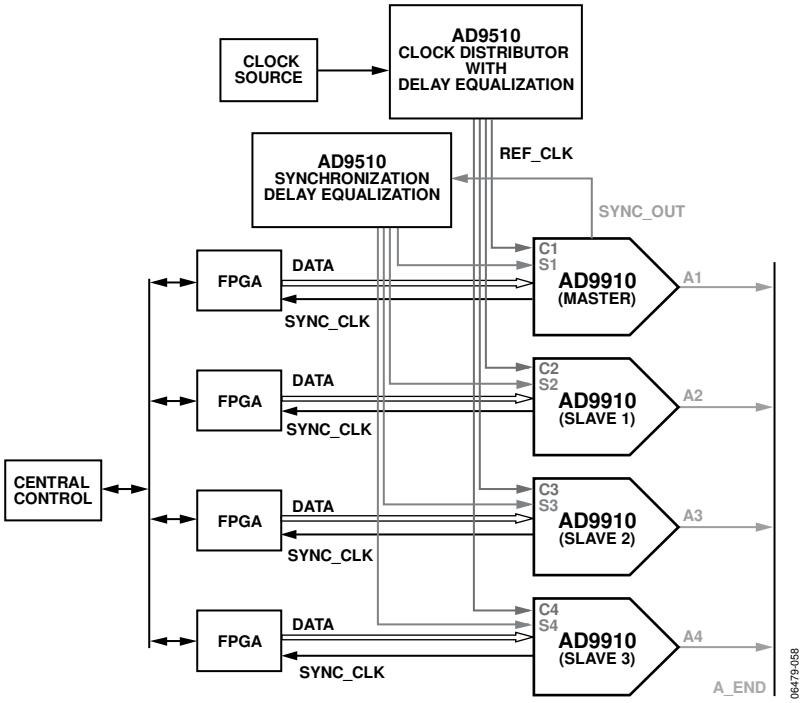


Figure 20. Synchronizing Multiple Devices to Increase Channel Capacity Using the AD9510 as a Clock Distributor for the Reference and Synchronization Clock

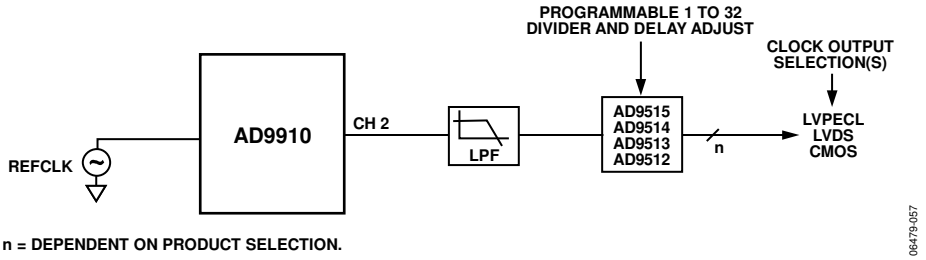


Figure 21. Clock Generation Circuit Using the AD9512/AD9513/AD9514/AD9515 Series of Clock Distribution Chips

THEORY OF OPERATION

- The AD9910 has four modes of operation.
- Single tone
- RAM modulation
- Digital ramp modulation
- Parallel data port modulation

The modes relate to the data source used to supply the DDS with its signal control parameters: frequency, phase, or amplitude. The partitioning of the data into different combinations of frequency, phase, and amplitude is handled automatically based on the mode and/or specific control bits.

In single tone mode, the DDS signal control parameters come directly from the programming registers associated with the serial I/O port. In RAM modulation mode, the DDS signal control parameters are stored in the internal RAM and played back upon command. In digital ramp modulation mode, the DDS signal control parameters are delivered by a digital ramp generator. In parallel data port modulation mode, the DDS signal control parameters are driven directly into the parallel port.

The various modulation modes generally operate on only one of the DDS signal control parameters (two in the case of the polar modulation format). The unmodulated DDS signal control parameters are stored in their appropriate programming registers and automatically route to the DDS based on the selected mode.

A separate output shift keying (OSK) function is also available. This function employs a separate digital linear ramp generator that only affects the amplitude parameter of the DDS. The OSK function has priority over the other data sources that can drive the DDS amplitude parameter. As such, no other data source can drive the DDS amplitude when the OSK function is enabled.

Although the various modes (including the OSK function) are described independently, they can be enabled simultaneously. This provides an unprecedented level of flexibility for generating complex modulation schemes. However, to avoid multiple data sources from driving the same DDS signal control parameter, the device has a built-in priority protocol (see Table 5 in the Mode Priority section).

SINGLE TONE MODE

In single tone mode, the DDS signal control parameters are supplied directly from the programming registers. A profile is an independent register that contains the DDS signal control parameters. Eight profile registers are available.

Each profile is independently accessible. Use the three external profile pins (PROFILE[2:0]) to select the desired profile. A change in the state of the profile pins with the next rising edge on SYNC_CLK updates the DDS with the parameters specified by the selected profile.

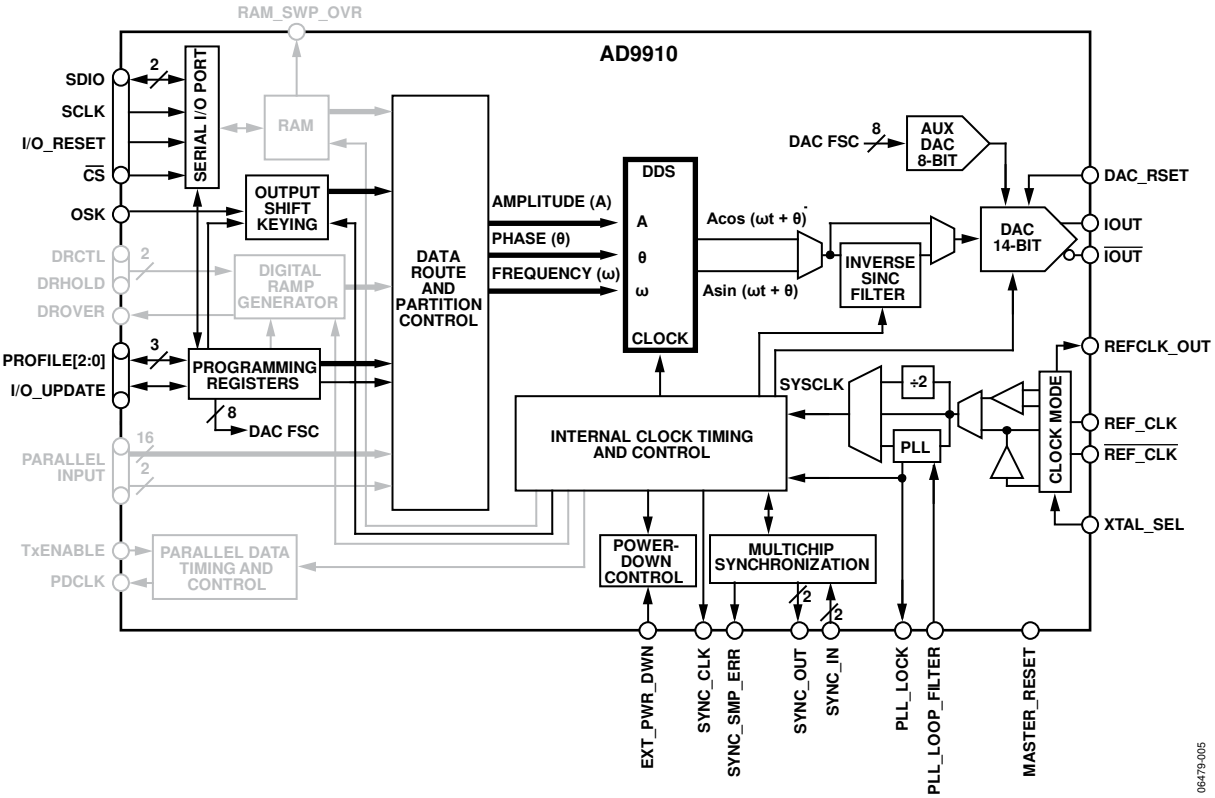


Figure 22. Single Tone Mode

RAM MODULATION MODE

The RAM modulation mode (see Figure 23) is activated via the RAM enable bit and assertion of the I/O_UPDATE pin (or a profile change). In this mode, the modulated DDS signal control parameters are supplied directly from RAM.

The RAM consists of 32-bit words and is 1024 words deep. Coupled with a sophisticated internal state machine, the RAM provides a very flexible method for generating arbitrary, time dependent waveforms. A programmable timer controls the rate at which words are extracted from the RAM for delivery to the DDS. Thus, the programmable timer establishes a sample rate at which 32-bit samples are supplied to the DDS.

The selection of the specific DDS signal control parameters that serve as the destination for the RAM samples is also programmable through eight independent RAM profile registers. Select a particular profile using the three external profile pins (PROFILE[2:0]). A change in the state of the profile pins with the next rising edge on SYNC_CLK activates the selected RAM profile.

In RAM modulation mode, the ability to generate a time dependent amplitude, phase, or frequency signal enables modulation of any one of the parameters controlling the DDS carrier signal. Furthermore, a polar modulation format is available that partitions each RAM sample into a magnitude and phase component; 16 bits are allocated to phase and 14 bits are allocated to magnitude.

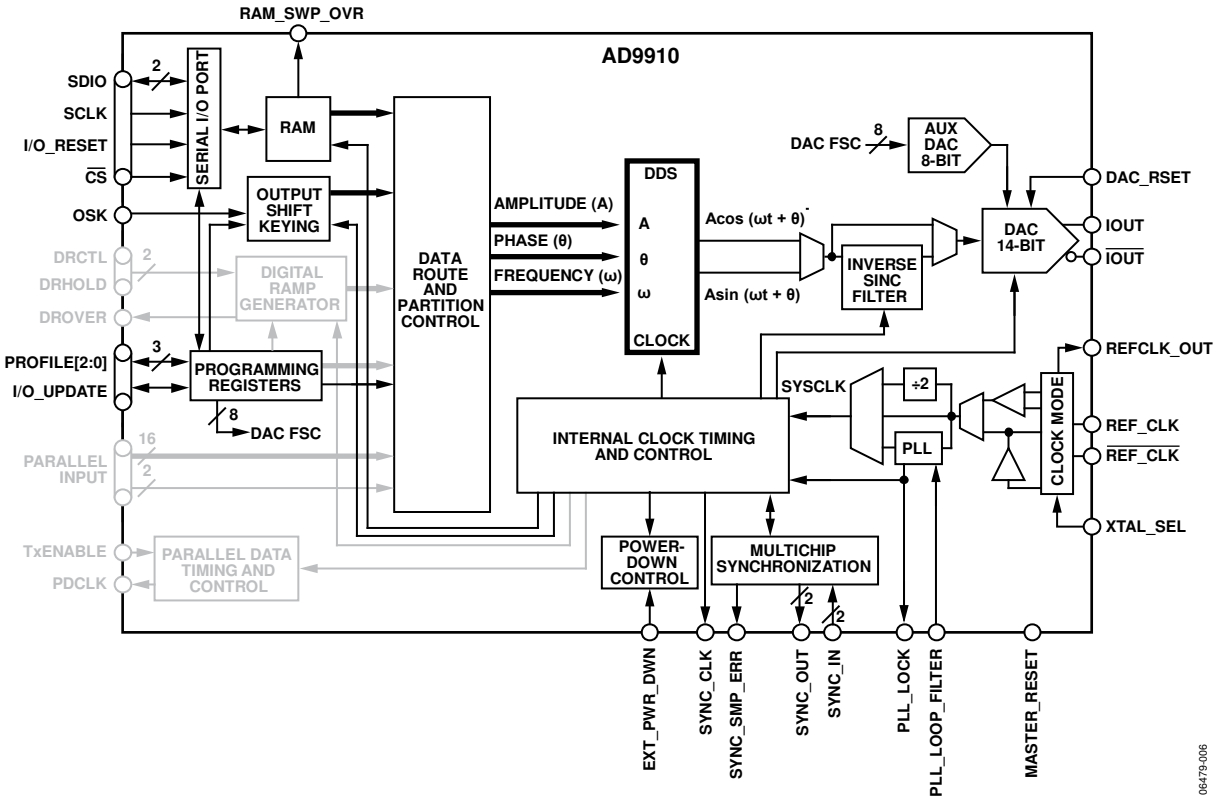


Figure 23. RAM Modulation Mode

DIGITAL RAMP MODULATION MODE

In digital ramp modulation mode (see Figure 24), the modulated DDS signal control parameter is supplied directly from the digital ramp generator (DRG). The ramp generation parameters are controlled through the serial I/O port.

The ramp generation parameters allow the user to control both the rising and falling slopes of the ramp. The upper and lower boundaries of the ramp, the step size and step rate of the rising portion of the ramp, and the step size and step rate of the falling portion of the ramp are all programmable.

The ramp is digitally generated with 32-bit output resolution. The 32-bit output of the DRG can be programmed to represent frequency, phase, or amplitude. When programmed to represent frequency, all 32 bits are used. However, when programmed to represent phase or amplitude, only the 16 MSBs or 14 MSBs, respectively, are used.

The ramp direction (rising or falling) is externally controlled by the DRCTL pin. An additional pin (DRHOLD) allows the user to suspend the ramp generator in its present state.

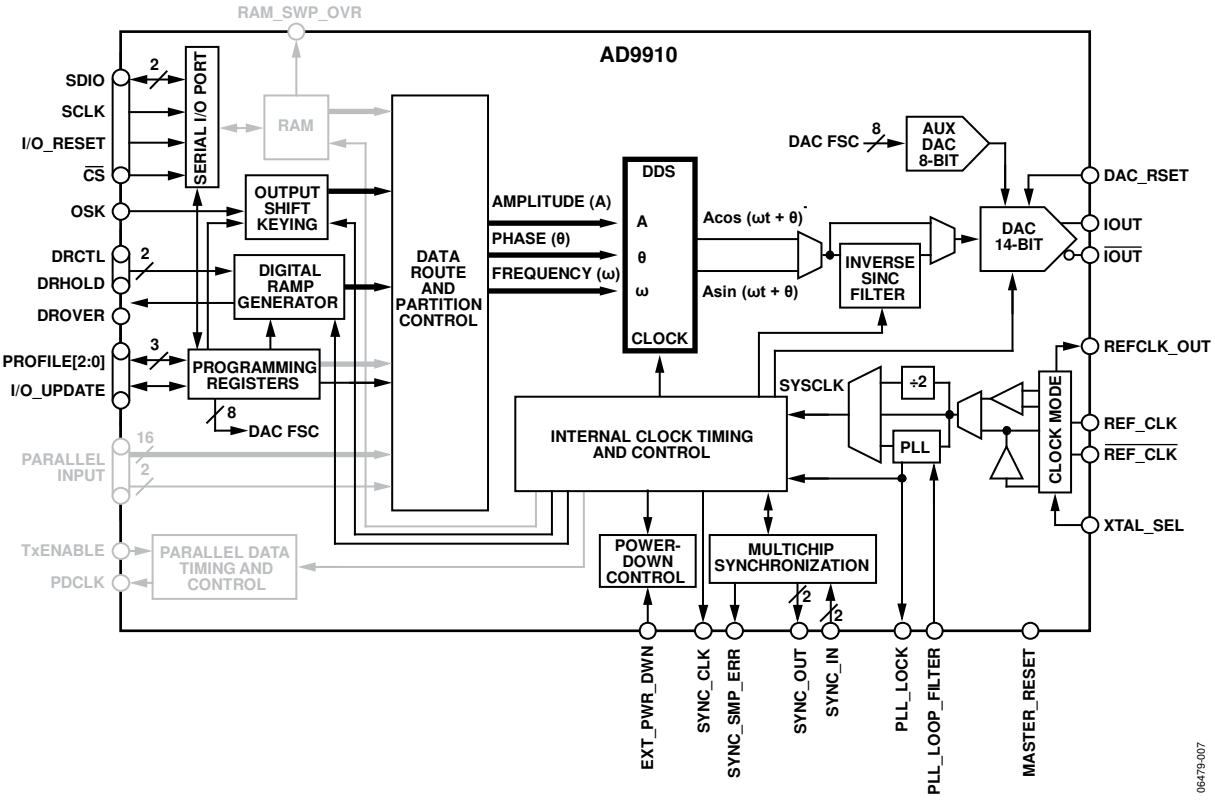


Figure 24. Digital Ramp Modulation Mode

PARALLEL DATA PORT MODULATION MODE

In parallel data port modulation mode (see Figure 25), the modulated DDS signal control parameter(s) are supplied directly from the 18-bit parallel data port.

The data port is partitioned into two sections. The 16 MSBs make up a 16-bit data-word (D[15:0] pins) and the two LSBs make up a 2-bit destination word (F[1:0] pins). The destination word defines how the 16-bit data-word is applied to the DDS signal control parameters. Table 4 defines the relationship between the destination bits, the partitioning of the 16-bit data-word, and the destination of the data (in terms of the DDS signal control parameters). Formatting of the 16-bit data-word is unsigned binary, regardless of the destination.

When the destination bits indicate that the data-word is destined as a DDS frequency parameter, the 16-bit data-word serves as an offset to the 32-bit frequency tuning word in the FTW register. This means that the 16-bit data-word must somehow be properly aligned with the 32-bit word in the FTW register. This is accomplished by means of the 4-bit FM gain word in the programming registers. The FM gain word allows the user to apply a weighting factor to the 16-bit data-word. In the default state (0), the 16-bit data-word and the 32-bit word in the FTW register are LSB aligned. Each increment in the value of the FM gain word shifts the 16-bit data-word to the left relative to the 32-bit word in the FTW register, increasing the influence of the 16-bit data-word on the frequency defined by the FTW register by a factor of two. The FM gain word effectively controls the frequency range spanned by the data-word.

Parallel Data Clock (PDCLK)

The AD9910 generates a clock signal on the PDCLK pin that runs at ¼ of the DAC sample rate (the sample rate of the parallel data port). PDCLK serves as a data clock for the parallel port. By default, each rising edge of PDCLK is used to latch the 18 bits of user-supplied data into the data port. The edge polarity can be changed through the PDCLK invert bit. Furthermore, the PDCLK output signal can be switched off using the PDCLK enable bit. However, even though the output signal is switched off, it continues to operate internally using the internal PDCLK timing to capture the data at the parallel port. Note that PDCLK is Logic 0 when disabled.

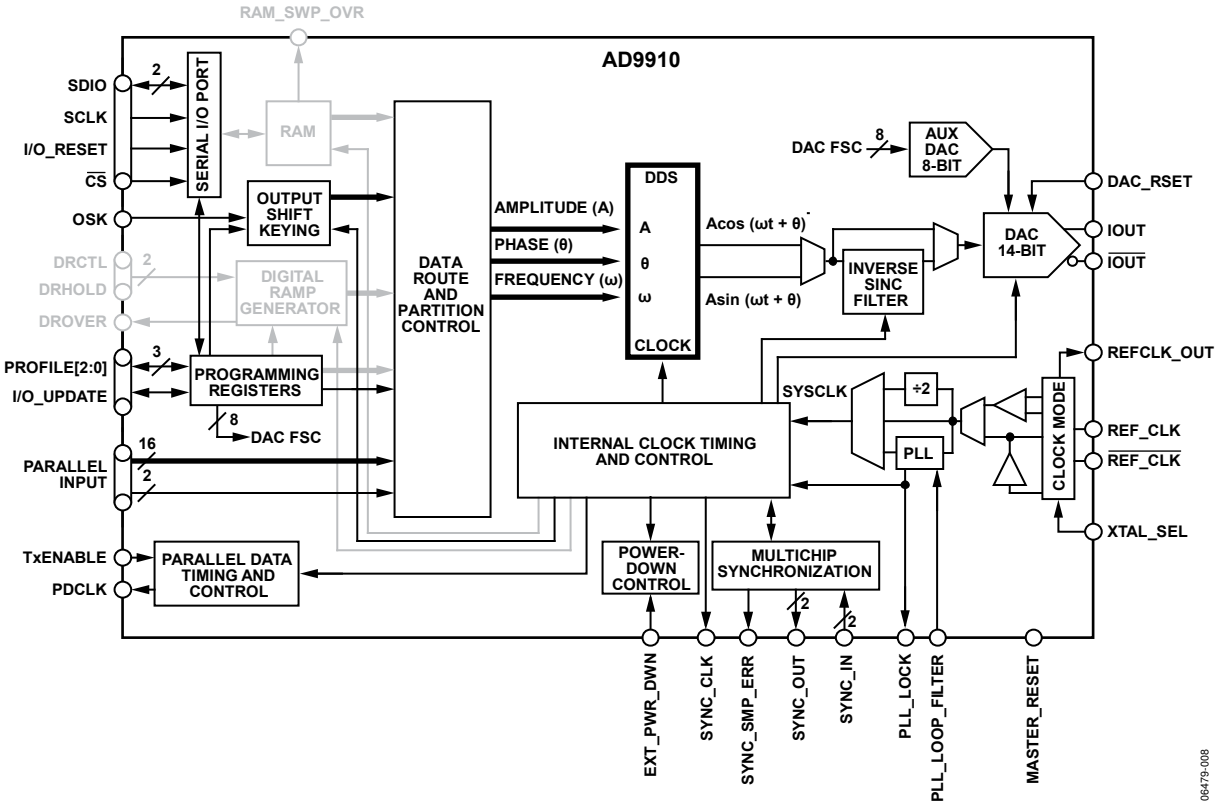


Figure 25. Parallel Data Port Modulation Mode

Table 4. Parallel Port Destination Bits

F[1:0]	D[15:0]	Parameter(s)	Comments
00	D[15:2]	14-bit amplitude parameter (unsigned integer)	Amplitude scales from 0 to $1 - 2^{-14}$. D[1:0] are not used.
01	D[15:0]	16-bit phase parameter (unsigned integer)	Phase offset ranges from 0 to $2\pi(1 - 2^{-16})$ radians.
10	D[15:0]	32-bit frequency parameter (unsigned integer)	The alignment of the 16-bit data-word with the 32-bit frequency parameter is controlled by a 4-bit FM gain word in the programming registers.
11	D[15:8]	8-bit amplitude (unsigned integer)	The MSB of the data-word amplitude aligns with the MSB of the DDS 14-bit amplitude parameter. The six LSBs of the DDS amplitude parameter are assigned from Bits[5:0] of the ASF register. The resulting 14-bit word scales the amplitude from 0 to $1 - 2^{-14}$.
	D[7:0]	8-bit phase (unsigned integer)	The MSB of the data-word phase aligns with the MSB of the 16-bit phase parameter of the DDS. The eight LSBs of the DDS phase parameter are assigned from Bits[7:0] of the POW register. The resulting 16-bit word offsets the phase from 0 to $2\pi(1 - 2^{-16})$ radians.

Transmit Enable (TxENABLE)

The AD9910 also accepts a user-generated signal applied to the TxENABLE pin that acts as a gate for the user-supplied data. By default, TxENABLE is considered true for Logic 1 and false for Logic 0. However, the logical behavior of this pin can be reversed using the TxENABLE invert bit. When TxENABLE is true, the device latches data into the device on the expected edge of PDCLK (based on the PDCLK invert bit). When TxENABLE is false, even though the PDCLK may continue to operate, the device ignores the data supplied to the port. Furthermore, when the TxENABLE pin is held false, the device internally clears the 16-bit data-words, or it retains the last value present on the data port prior to TxENABLE switching to the false state (based on the setting of the data assembler hold last value bit).

Alternatively, instead of operating the TxENABLE pin as a gate, the user can drive the TxENABLE pin with a clock signal operating at the parallel port data rate. When driven by a clock signal, the transition from the false to true state must meet the required setup and hold time on each cycle to ensure proper operation. The TxENABLE and PDCLK timing is shown in Figure 26.

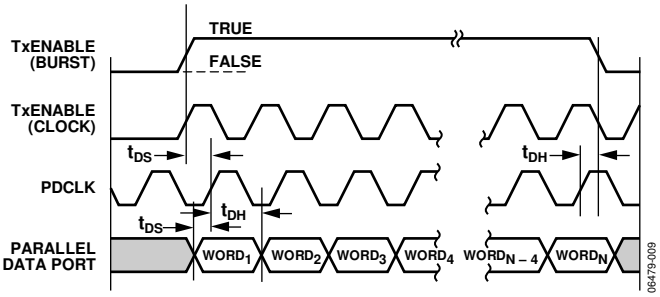


Figure 26. PDCLK and TxENABLE Timing Diagram

MODE PRIORITY

The three different modulation modes generate frequency, phase, and/or amplitude data destined for the DDS signal control parameters. In addition, the OSK function generates amplitude data destined for the DDS. Each of these functions is independently invoked using the appropriate control bit via the serial I/O port.

The ability to activate each of these functions independently makes it possible to have multiple data sources attempting to drive the same DDS signal control parameter. To avoid contention, the AD9910 has a built-in priority system. Table 5 summarizes the priority for each of the DDS signal control parameters. The rows of Table 5 list data sources for a particular DDS signal control parameter in descending order of precedence. For example, if both the RAM and the parallel port are enabled and both are programmed for frequency as the destination, then the DDS frequency parameter is driven by the RAM and not the parallel data port.

Table 5. Data Source Priority

	DDS Signal Control Parameters					
	Frequency		Phase		Amplitude	
Priority	Data Source	Conditions	Data Source	Conditions	Data Source	Conditions
Highest Priority	RAM	RAM enabled and data destination is frequency	RAM	RAM enabled and data destination is phase or polar	OSK generator	OSK enabled (auto mode)
	DRG	DRG enabled and data destination is frequency	DRG	DRG enabled and data destination is phase	ASF register	OSK enabled (manual mode)
	Parallel data port and FTW register	Parallel data port enabled and data destination is frequency	Parallel data port	Parallel data port enabled and data destination is phase	RAM	RAM enabled and data destination is amplitude or polar
	FTW register	RAM enabled and data destination is phase, amplitude, or polar	Parallel data port concatenated with the POW register LSBs	Parallel data port enabled and data destination is polar	DRG	DRG enabled and data destination is amplitude
	FTW in active single tone profile register	DRG enabled and data destination is phase or amplitude	POW register	RAM enabled and destination is frequency or amplitude	Parallel data port	Parallel data port enabled and data destination is amplitude
	FTW in active single tone profile register	Parallel data port enabled and data destination is phase, amplitude, or polar	POW in active single tone profile register	DRG enabled and data destination is frequency or amplitude	Parallel data port concatenated with the ASF register LSBs	Parallel data port enabled and data destination is polar
	FTW in active single tone profile register	None	POW in active single tone profile register	Parallel data port enabled and data destination is frequency or amplitude	ASF in active single tone profile register	Enable amplitude scale from single tone profiles bit (CFR2[24]) set
Lowest Priority			POW in active single tone profile register	None	No amplitude scaling	None

FUNCTIONAL BLOCK DETAIL

DDS CORE

The direct digital synthesizer (DDS) block generates a reference signal (sine or cosine based on CFR1[16], the select DDS sine output bit). The parameters of the reference signal (frequency, phase, and amplitude) are applied to the DDS at its frequency, phase offset, and amplitude control inputs, as shown in Figure 27.

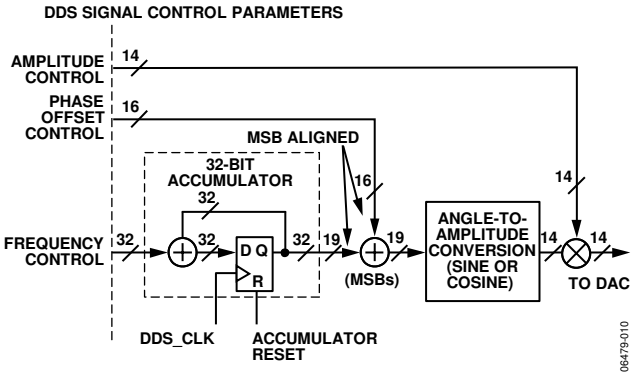


Figure 27. DDS Block Diagram

The output frequency (f_{OUT}) of the AD9910 is controlled by the frequency tuning word (FTW) at the frequency control input to the DDS. The relationship among f_{OUT}, FTW, and f_{SYSCLK} is given by

$$f_{OUT} = \left(\frac{FTW}{2^{32}}\right) f_{SYSCLK} \quad (1)$$

where *FTW* is a 32-bit integer ranging in value from 0 to 2,147,483,647 ($2^{31} - 1$), which represents the lower half of the full 32-bit range. This range constitutes frequencies from dc to Nyquist (that is, ½ f_{SYSCLK}).

The FTW required to generate a desired value of f_{OUT} is found by solving Equation 1 for FTW, as given in Equation 2.

$$FTW = \text{round}\left(2^{32}\left(\frac{f_{OUT}}{f_{SYSCLK}}\right)\right) \quad (2)$$

where the round(*x*) function rounds the argument (the value of x) to the nearest integer. This is required because the FTW is constrained to be an integer value. For example, for f_{OUT} = 41 MHz and f_{SYSCLK} = 122.88 MHz, then FTW = 1,433,053,867 (0x556AAAAB).

Programming an FTW greater than 2^{31} produces an aliased image that appears at a frequency given by

$$f_{OUT} = \left(1 - \frac{FTW}{2^{32}}\right) f_{SYSCLK} \quad (\text{for FTW} \geq 2^{31})$$

The relative phase of the DDS signal can be digitally controlled by means of a 16-bit phase offset word (POW). The phase offset is applied prior to the angle-to-amplitude conversion block internal to the DDS core. The relative phase offset (Δθ) is given by

$$\Delta\theta = \begin{vmatrix} 2\pi\left(\frac{POW}{2^{16}}\right) \\ 360\left(\frac{POW}{2^{16}}\right) \end{vmatrix}$$

where the upper quantity is for the phase offset expressed as radian units and the lower quantity as degrees. To find the POW value necessary to develop an arbitrary Δθ, solve the previous equation for POW and round the result (in a manner similar to that described previously for finding an arbitrary FTW).

The relative amplitude of the DDS signal can be digitally scaled (relative to full scale) by means of a 14-bit amplitude scale factor (ASF). The amplitude scale value is applied at the output of the angle-to-amplitude conversion block internal to the DDS core. The amplitude scale is given by

$$Amplitude\ Scale = \begin{vmatrix} \frac{ASF}{2^{14}} \\ 20\log\left(\frac{ASF}{2^{14}}\right) \end{vmatrix} \quad (3)$$

where the upper quantity is amplitude expressed as a fraction of full scale and the lower quantity is expressed in decibels relative to full scale. To find the ASF value necessary for a particular scale factor, solve Equation 3 for ASF and round the result (in a manner similar to that described previously for finding an arbitrary FTW).

When the AD9910 is programmed to modulate any of the DDS signal control parameters, the maximum modulation sample rate is ¼ f_{SYSCLK}. This means that the modulation signal exhibits images at multiples of ¼ f_{SYSCLK}. The impact of these images must be considered when using the device as a modulator.

14-BIT DAC OUTPUT

The AD9910 incorporates an integrated 14-bit, current output DAC. The output current is delivered as a balanced signal using two outputs. The use of balanced outputs reduces the potential amount of common-mode noise present at the DAC output, offering the advantage of an increased signal-to-noise ratio. An external resistor (R_{SET}) connected between the DAC_RSET pin and AGND establishes the reference current. The full-scale output current of the DAC (I_{OUT}) is produced as a scaled version of the reference current (see the Auxiliary DAC section). The recommended value of R_{SET} is 10 kΩ.

Attention should be paid to the load termination to keep the output voltage within the specified compliance range; voltages developed beyond this range cause excessive distortion and can damage the DAC output circuitry.