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500 MSPS Direct Digital Synthesizer with 10-Bit DAC

Data Sheet

AD9911

FEATURES

Patented SpurKiller technology
Multitone generation
Test-tone modulation
Up to 800 Mbps data throughput
Matched latencies for frequency/phase/amplitude changes
Linear frequency/phase/amplitude sweeping capability
Up to 16 levels of FSK, PSK, ASK
Programmable DAC full-scale current
32-bit frequency tuning resolution
14-bit phase offset resolution
10-bit output amplitude-scaling resolution
Software-/hardware-controlled power-down
Multiple device synchronization
Selectable 4× to 20× REF_CLK multiplier (PLL)
Selectable REF_CLK crystal oscillator
56-lead LFCSP

APPLICATIONS

Agile local oscillator
Test and measurement equipment
Commercial and amateur radio exciter
Radar and sonar
Test-tone generation
Fast frequency hopping
Clock generation

GENERAL DESCRIPTION

The AD9911 is a complete direct digital synthesizer (DDS). This device includes a high speed DAC with excellent wideband and narrowband spurious-free dynamic range (SFDR) as well as three auxiliary DDS cores without assigned digital-to-analog converters (DACs). These auxiliary channels are used for spur reduction, multitone generation, or test-tone modulation.

The AD9911 is the first DDS to incorporate SpurKiller technology and multitone generation capability. Multitone mode enables the generation up to four concurrent carriers; frequency, phase and amplitude can be independently programmed. Multitone generation can be used for system tests, such as inter-modulation distortion and receiver blocker sensitivity. SpurKilling enables customers to improve SFDR performance by reducing the magnitude of harmonic components and/or the aliases of those harmonic components.

Test-tone modulation efficiently enables sine wave modulation of amplitude on the output signal using one of the auxiliary DDS cores.

The AD9911 can perform modulation of frequency, phase, or amplitude (FSK, PSK, ASK). Modulation is implemented by storing profiles in the register bank and applying data to the profile pins. In addition, the AD9911 supports linear sweep of frequency, phase, or amplitude for applications such as radar and instrumentation.

(continued on Page 3)

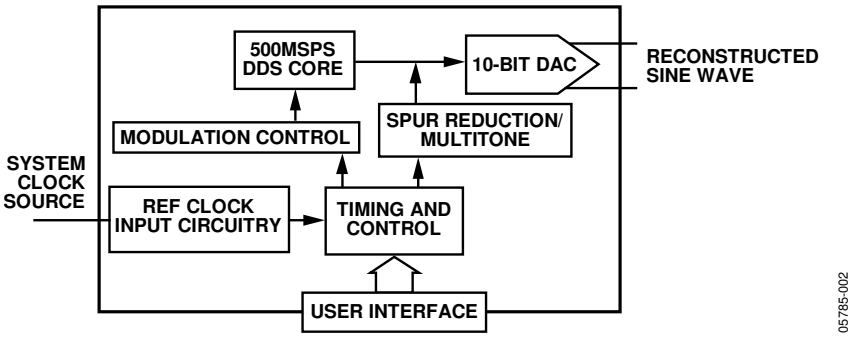

Figure 1. Basic Block Diagram

Rev. A **Document Feedback**

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AD9911* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9911 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1389: Recommended Rework Procedure for the Lead Frame Chip Scale Package (LFCSP)
- AN-237: Choosing DACs for Direct Digital Synthesis
- AN-280: Mixed Signal Circuit Technologies
- AN-342: Analog Signal-Handling for High Speed and Accuracy
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-419: A Discrete, Low Phase Noise, 125 MHz Crystal Oscillator for the AD9850
- AN-423: Amplitude Modulation of the AD9850 Direct Digital Synthesizer
- AN-543: High Quality, All-Digital RF Frequency Modulation Generation with the ADSP-2181 and the AD9850 DDS
- AN-557: An Experimenter's Project:
- AN-587: Synchronizing Multiple AD9850/AD9851 DDS-Based Synthesizers
- AN-605: Synchronizing Multiple AD9852 DDS-Based Synthesizers
- AN-621: Programming the AD9832/AD9835
- AN-632: Provisionary Data Rates Using the AD9951 DDS as an Agile Reference Clock for the ADN2812 Continuous-Rate CDR
- AN-769: Generating Multiple Clock Outputs from the AD9540
- AN-772: A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)
- AN-823: Direct Digital Synthesizers in Clocking Applications Time
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-843: Measuring a Loudspeaker Impedance Profile Using the AD5933
- AN-847: Measuring a Grounded Impedance Profile Using the AD5933
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design
- AN-927: Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)

- AN-939: Super-Nyquist Operation of the AD9912 Yields a High RF Output Signal
- AN-953: Direct Digital Synthesis (DDS) with a Programmable Modulus

Data Sheet

- AD9911: 500 MSPS Direct Digital Synthesizer with 10-Bit DAC Data Sheet

Product Highlight

- Introducing Digital Up/Down Converters: VersaCOMM™ Reconfigurable Digital Converters

Technical Books

- A Technical Tutorial on Digital Signal Synthesis, 1999

REFERENCE DESIGNS

- CN0109

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

Technical Articles

- 400-MSample DDSs Run On Only +1.8 VDC
- ADI Buys Korean Mobile TV Chip Maker
- Basics of Designing a Digital Radio Receiver (Radio 101)
- DDS Applications
- DDS Circuit Generates Precise PWM Waveforms
- DDS Design
- DDS Device Produces Sawtooth Waveform
- DDS Device Provides Amplitude Modulation
- DDS IC Initiates Synchronized Signals
- DDS IC Plus Frequency-To-Voltage Converter Make Low-Cost DAC
- DDS Simplifies Polar Modulation
- Digital Potentiometers Vary Amplitude In DDS Devices
- Digital Up/Down Converters: VersaCOMM™ White Paper
- Digital Waveform Generator Provides Flexible Frequency Tuning for Sensor Measurement
- Improved DDS Devices Enable Advanced Comm Systems
- Integrated DDS Chip Takes Steps To 2.7 GHz
- Simple Circuit Controls Stepper Motors
- Speedy A/Ds Demand Stable Clocks
- Synchronized Synthesizers Aid Multichannel Systems
- The Year of the Waveform Generator
- Two DDS ICs Implement Amplitude-shift Keying
- Video Portables and Cameras Get HDMI Outputs

DESIGN RESOURCES

- AD9911 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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REVISION HISTORY

11/2016—Rev. 0 to Rev. A

Changes to Figure 43 Caption ... 25
Updated Outline Dimensions ... 41

5/2006—Revision 0: Initial Version

GENERAL DESCRIPTION

The DDS acts as a high resolution frequency divider with the REF_CLK as the input and the DAC providing the output. The REF_CLK input can be driven directly or used in combination with an integrated REF_CLK multiplier (PLL). The REF_CLK input also features an oscillator circuit to support an external crystal as the REF_CLK source. The crystal can be used in combination with the REF_CLK multiplier.

The AD9911 I/O port offers multiple configurations to provide significant flexibility. The I/O port offers an SPI-compatible mode of operation that is virtually identical to the SPI operation found in earlier Analog Devices DDS products.

Flexibility is provided by four data pins (Pin SDIO_0, Pin SDIO_1, Pin SDIO_2, and Pin SDIO_3) that allow four programmable modes of I/O operation.

The DAC output is supply referenced and must be terminated into AVDD by a resistor and an AVDD center-tapped transformer. The DAC has its own programmable reference to enable different full-scale currents.

The DDS core (the AVDD pins and the DVDD pins) is powered by a 1.8 V supply. The digital I/O interface (SPI) operates at 3.3 V and requires that the Pin DVDD_I/O (Pin 49) be connected to 3.3 V.

FUNCTIONAL BLOCK DIAGRAM

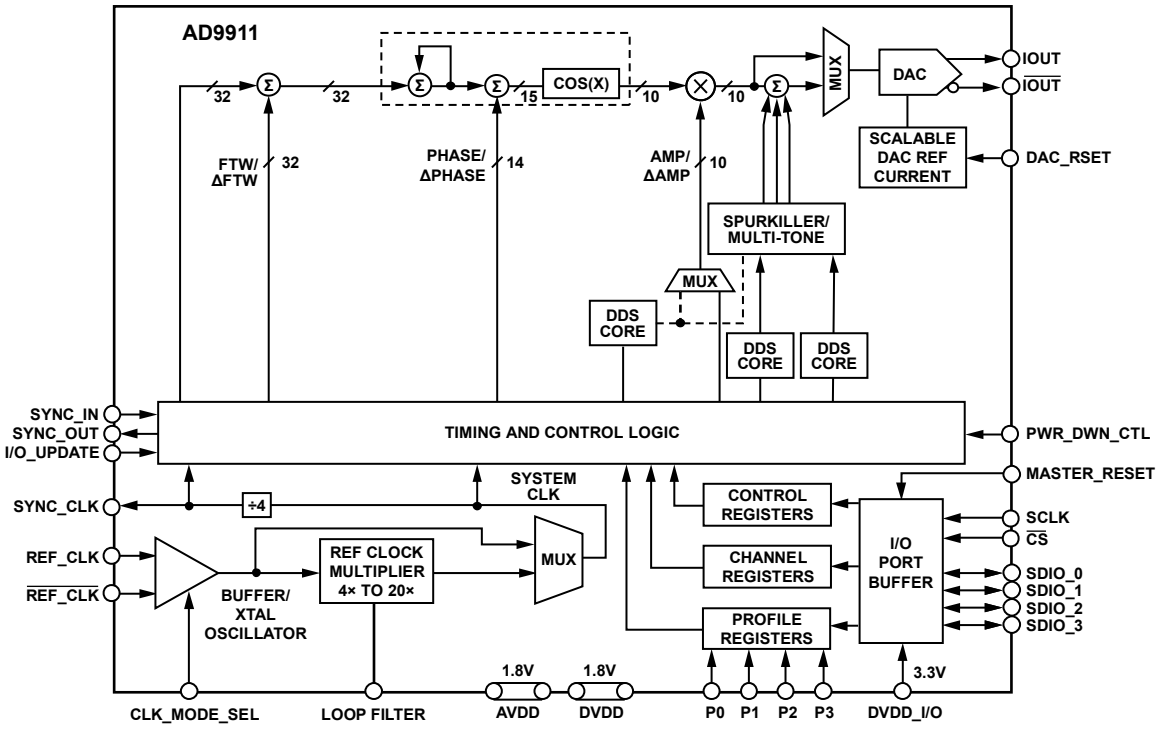

Figure 2. Functional Block Diagram

SPECIFICATIONS

AVDD and DVDD = 1.8 V ± 5%; DVDD_I/O = 3.3 V ± 5%; R_{SET} = 1.91 kΩ; external reference clock frequency = 500 MSPS (REF_CLK multiplier bypassed), unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REF CLOCK INPUT CHARACTERISTICS					
Frequency Range					
REF_CLK Multiplier Bypassed	1		500	MHz	
REF_CLK Multiplier Enabled	10		125	MHz	
Internal VCO Output Frequency Range VCO Gain Bit Set[1]	255		500	MHz	
Internal VCO Output Frequency Range VCO Gain Bit Cleared	100		160	MHz	
Crystal REF_CLK Source Range	20		30	MHz	
Input Power Sensitivity	−5		+3	dBm	Measured at the pin (single-ended)
Input Voltage Bias Level		1.15		V	
Input Capacitance		2		pF	
Input Impedance		1500		Ω	
Duty Cycle with REF_CLK Multiplier Bypassed	45		55	%	
Duty Cycle with REF_CLK Multiplier Enabled	35		65	%	
CLK Mode Select (Pin 24) Logic 1 V	1.25		1.8	V	1.8 V digital input logic
CLK Mode Select (Pin 24) Logic 0 V			0.5	V	1.8 V digital input logic
DAC OUTPUT CHARACTERISTICS					Must be referenced to AVDD
Full-Scale Output Current		10		mA	10 mA is set by R_{SET} = 1.91 kΩ
Gain Error	−10		+10	%FS	
Output Current Offset		1	25	μA	
Differential Nonlinearity		±0.5		LSB	
Integral Nonlinearity		±1.0		LSB	
Output Capacitance		3		pF	
Voltage Compliance Range	AVDD – 0.50		AVDD + 0.50	V	
WIDEBAND SFDR					The frequency range for wideband SFDR is defined as dc to Nyquist
1 MHz to 20 MHz Analog Output		−65		dBc	
20 MHz to 60 MHz Analog Output		−62		dBc	
60 MHz to 100 MHz Analog Output		−59		dBc	
100 MHz to 150 MHz Analog Output		−56		dBc	
150 t MHz to 200 MHz Analog Output		−53		dBc	
WIDEBAND SFDR Improvement Spur Reduction Enabled					Programs devices on an individual basis to enable spur reduction. See the SpurKiller/Multitone Mode section.
60 MHz to 100 MHz Analog Output		8		dBc	
100 MHz to 150 MHz Analog Output		15		dBc	
150 MHz to 200 MHz Analog Output		12		dBc	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
NARROWBAND SFDR					
1.1 MHz Analog Output (±10 kHz)		−90		dBc	
1.1 MHz Analog Output (±50 kHz)		−88		dBc	
1.1 MHz Analog Output (±250 kHz)		−86		dBc	
1.1 MHz Analog Output (±1 MHz)		−85		dBc	
15.1 MHz Analog Output (±10 kHz)		−90		dBc	
15.1 MHz Analog Output (±50 kHz)		−87		dBc	
15.1 MHz Analog Output (±250 kHz)		−85		dBc	
15.1 MHz Analog Output (±1 MHz)		−83		dBc	
40.1 MHz Analog Output (±10 kHz)		−90		dBc	
40.1 MHz Analog Output (±50 kHz)		−87		dBc	
40.1 MHz Analog Output (±250 kHz)		−84		dBc	
40.1 MHz Analog Output (±1 MHz)		−82		dBc	
75.1 MHz Analog Output (±10 kHz)		−87		dBc	
75.1 MHz Analog Output (±50 kHz)		−85		dBc	
75.1 MHz Analog Output (±250 kHz)		−83		dBc	
75.1 MHz Analog Output (±1 MHz)		−82		dBc	
100.3 MHz Analog Output (±10 kHz)		−87		dBc	
100.3 MHz Analog Output (±50 kHz)		−85		dBc	
100.3 MHz Analog Output (±250 kHz)		−83		dBc	
100.3 MHz Analog Output (±1 MHz)		−81		dBc	
200.3 MHz Analog Output (±10 kHz)		−87		dBc	
200.3 MHz Analog Output (±50 kHz)		−85		dBc	
200.3 MHz Analog Output (±250 kHz)		−83		dBc	
200.3 MHz Analog Output (±1 MHz)		−81		dBc	
PHASE NOISE CHARACTERISTICS					
Residual Phase Noise @ 15.1 MHz (f_{OUT})					
1 kHz Offset		−150		dBc/Hz	
10 kHz Offset		−159		dBc/Hz	
100 kHz Offset		−165		dBc/Hz	
1 MHz Offset		−165		dBc/Hz	
Residual Phase Noise @ 40.1 MHz (f_{OUT})					
1 kHz Offset		−142		dBc/Hz	
10 kHz Offset		−151		dBc/Hz	
100 kHz Offset		−160		dBc/Hz	
1 MHz Offset		−162		dBc/Hz	
Residual Phase Noise @ 75.1 MHz (f_{OUT})					
1 kHz Offset		−135		dBc/Hz	
10 kHz Offset		−146		dBc/Hz	
100 kHz Offset		−154		dBc/Hz	
1 MHz Offset		−157		dBc/Hz	
Residual Phase Noise @ 100.3 MHz (f_{OUT})					
1 kHz Offset		−134		dBc/Hz	
10 kHz Offset		−144		dBc/Hz	
100 kHz Offset		−152		dBc/Hz	
1 MHz Offset		−154		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Residual Phase Noise @ 15.1 MHz (f_{OUT}) with REF_CLK Multiplier Enabled 5×					
1 kHz Offset		–139		dBc/Hz	
10 kHz Offset		–149		dBc/Hz	
100 kHz Offset		–153		dBc/Hz	
1 MHz Offset		–148		dBc/Hz	
Residual Phase Noise @ 40.1 MHz (f_{OUT}) with REF_CLK Multiplier Enabled 5×					
1 kHz Offset		–130		dBc/Hz	
10 kHz Offset		–140		dBc/Hz	
100 kHz Offset		–145		dBc/Hz	
1 MHz Offset		–139		dBc/Hz	
Residual Phase Noise @ 75.1 MHz (f_{OUT}) with REF_CLK Multiplier Enabled 5×					
1 kHz Offset		–123		dBc/Hz	
10 kHz Offset		–134		dBc/Hz	
100 kHz Offset		–138		dBc/Hz	
1 MHz Offset		–132		dBc/Hz	
Residual Phase Noise @ 100.3 MHz(f_{OUT}) with REF_CLK Multiplier Enabled 5×					
1 kHz Offset		–120		dBc/Hz	
10 kHz Offset		–130		dBc/Hz	
100 kHz Offset		–135		dBc/Hz	
1 MHz Offset		–129		dBc/Hz	
Residual Phase Noise @ 15.1 MHz (f_{OUT}) with REF_CLK Multiplier Enabled 20×					
1 kHz Offset		–127		dBc/Hz	
10 kHz Offset		–136		dBc/Hz	
100 kHz Offset		–139		dBc/Hz	
1 MHz Offset		–138		dBc/Hz	
Residual Phase Noise @ 40.1 MHz (f_{OUT}) with REF_CLK Multiplier Enabled 20×					
1 kHz Offset		–117		dBc/Hz	
10 kHz Offset		–128		dBc/Hz	
100 kHz Offset		–132		dBc/Hz	
1 MHz Offset		–130		dBc/Hz	
Residual Phase Noise @ 75.1 MHz (f_{OUT}) with REF_CLK Multiplier Enabled 20×					
1 kHz Offset		–110		dBc/Hz	
10 kHz Offset		–121		dBc/Hz	
100 kHz Offset		–125		dBc/Hz	
1 MHz Offset		–123		dBc/Hz	
Residual Phase Noise @ 100.3 MHz (f_{OUT}) with REF_CLK Multiplier Enabled 20×					
1 kHz Offset		–107		dBc/Hz	
10 kHz Offset		–119		dBc/Hz	
100 kHz Offset		–121		dBc/Hz	
1 MHz Offset		–119		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
I/O PORT TIMING CHARACTERISTICS					
Maximum Frequency Clock (SCLK)			200	MHz	
Minimum SCLK Pulse Width Low (t_{PWL})	1.6			ns	
Minimum SCLK Pulse Width High (t_{PWH})	2.2			ns	
Minimum Data Set-Up Time (t_{DS})	2.2			ns	
Minimum Data Hold Time	0			ns	
Minimum CSB Set-Up Time (t_{PRE})	1.0			ns	
Minimum Data Valid Time for Read Operation	12			ns	
MISCELLANEOUS TIMING CHARACTERISTICS					
Master_Reset Minimum Pulse Width	1				Minimum pulse width = 1 sync clock period
I/O_Update Minimum Pulse Width	1				Minimum pulse width = 1 sync clock period
Minimum Set-Up Time (I/O_Update to SYNC_CLK)	4.8			ns	Rising edge to rising edge
Minimum Hold Time (I/O_Update to SYNC_CLK)	0			ns	Rising edge to rising edge
Minimum Set-Up Time (Profile Inputs to SYNC_CLK)	5.4			ns	
Minimum Hold Time (Profile Inputs to SYNC_CLK)	0			ns	
Minimum Set-Up Time (SDIO Inputs to SYNC_CLK)	2.5			ns	
Minimum Hold Time (SDIO Inputs to SYNC_CLK)	0			ns	
Propagation Delay Between REF_CLK and SYNC_CLK	2.25	3.5	5.5	ns	
CMOS LOGIC INPUT					
V_{IH}	2.0			V	
V_{IL}			0.8	V	
Logic 1 Current		3	12	µA	
Logic 0 Current		−12		µA	
Input Capacitance		2		pF	
CMOS LOGIC OUTPUTS (1 mA Load)					
V_{OH}	2.7			V	
V_{OL}			0.4	V	
POWER SUPPLY					
Total Power Dissipation—Single-Tone Mode		241		mW	Dominated by supply variation
Total Power Dissipation—With Sweep Accumulator		241		mW	Dominated by supply variation
Total Power Dissipation—3 Spur Reduction/Multitone Channels Active		351		mW	Dominated by supply variation
Total Power Dissipation—Test-Tone Modulation		264		mW	Dominated by supply variation
Total Power Dissipation—Full Power Down		1.8		mW	
IAVDD—Single-Tone Mode		73		mA	
IAVDD— Sweep Accumulator, REF_CLK Multiplier, and 10-Bit Output Scalar Enabled		73		mA	
IDVDD—Single-Tone Mode		50		mA	
IDVDD—Sweep Accumulator, REF_CLK Multiplier, and 10-Bit Output Scalar Enabled		50		mA	
IDVDD_I/O		40		mA	IDVDD = read
IDVDD_I/O		30		mA	IDVDD = write
IAVDD Power-Down Mode		0.7		mA	
IDVDD Power-Down Mode		1.1		mA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DATA LATENCY (PIPELINE DELAY) SINGLE-TONE MODE[2, 3]					
Frequency, Phase, and Amplitude Words to DAC Output with Matched Latency Enabled	29			SYSCLK cycles	
Frequency Word to DAC Output with Matched Latency Disabled	29			SYSCLK cycles	
Phase Offset Word to DAC Output with Matched Latency Disabled	25			SYSCLK cycles	
Amplitude Word to DAC Output with Matched Latency Disabled	17			SYSCLK cycles	
DATA LATENCY (PIPELINE DELAY) MODULATION MODE[4]					
Frequency Word to DAC Output	34			SYSCLK Cycles	
Phase Offset Word to DAC Output	29			SYSCLK Cycles	
Amplitude Word to DAC Output	21			SYSCLK Cycles	
DATA LATENCY (PIPELINE DELAY) LINEAR SWEEP MODE[4]					
Frequency Rising/Falling Delta Tuning Word to DAC Output	41			SYSCLK Cycles	
Phase Offset Rising/Falling Delta Tuning Word to DAC Output	37			SYSCLK Cycles	
Amplitude Rising/Falling Delta Tuning Word to DAC Output	29			SYSCLK Cycles	

[1] For the VCO frequency range of 160 MHz to 255 MHz, the appropriate setting for the VCO gain bit is dependent upon supply, temperature and process. Therefore, in a production environment this frequency band must be avoided.
[2] Data latency is reference to the I/O_UPDATE pin.
[3] Data latency is fixed and the units are system clock (SYSCLK) cycles
[4] Data latency is referenced to a profile change.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Maximum Junction Temperature	150°C
DVDD_I/O (Pin 49)	4 V
AVDD, DVDD	2 V
Digital Input Voltage (DVDD_I/O = 3.3 V)	−0.7 V to +4 V
Digital Output Current	5 mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−40°C to +85°C
Lead Temperature (10 sec Soldering)	300°C
θ_{JA}	21°C/W
θ_{JC}	2°C/W

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

EQUIVALENT INPUT AND OUTPUT CIRCUITS

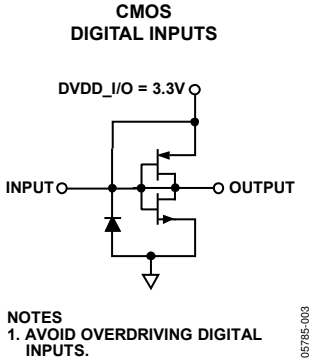

Figure 3. CMOS Digital Inputs

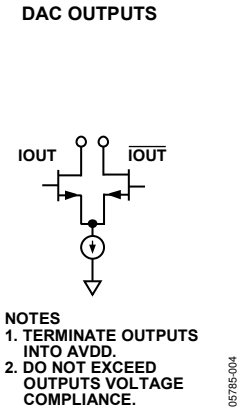

Figure 4. DAC Outputs

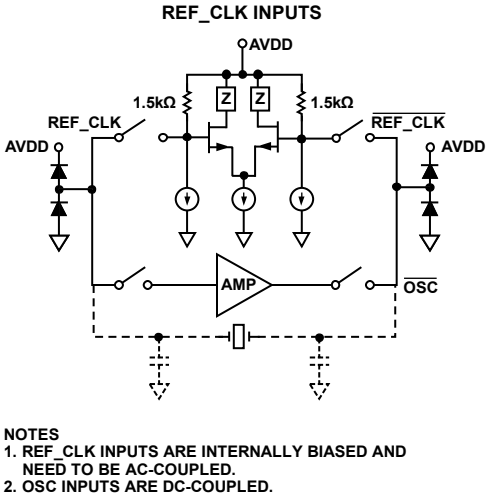

Figure 5. REF_CLK Inputs

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

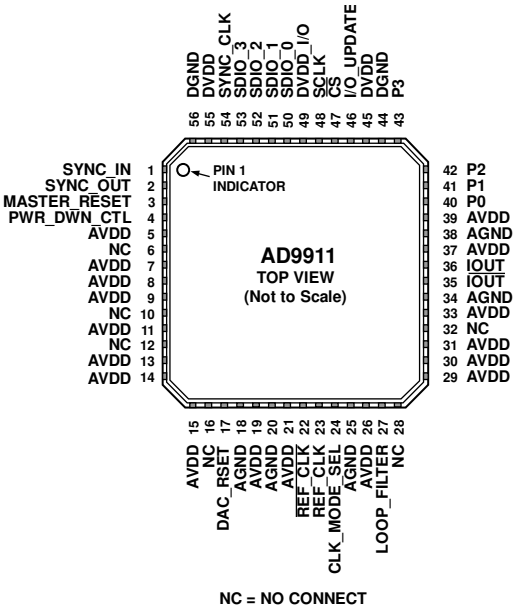

Figure 6. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	I/O	Description
1	SYNC_IN	I	Synchronizes Multiple AD9911 Devices. Connects to the SYNC_OUT pin of the master AD9911 device.
2	SYNC_OUT	O	Synchronizes Multiple AD9911 Devices. Connects to the SYNC_IN pin of the slave AD9911 device.
3	MASTER_RESET	I	Active High Reset Pin. Asserting this pin forces the internal registers to the default state shown in the Register Map section.
4	PWR_DWN_CTL	I	External Power-Down Control. See the Power Down Functions section for details.
5, 7, 8, 9, 11, 13, 14, 15, 19, 21, 26, 29, 30, 31, 33, 37, 39	AVDD	I	Analog Power Supply Pins (1.8 V).
18, 20, 25, 34, 38	AGND	I	Analog Ground Pins.
45, 55	DVDD	I	Digital Power Supply Pins (1.8 V).
44, 56	DGND	I	Digital Power Ground Pins.
35	$\overline{\text{IOUT}}$	O	Complementary DAC Output. Terminates into AVDD.
36	IOUT	O	True DAC Output. Terminates into AVDD.
17	DAC_RSET	I	Establishes the Reference Current for the DAC. A 1.91 kΩ resistor (nominal) is connected from Pin 17 to AGND.
22	$\overline{\text{REF\_CLK}}$	I	Complementary Reference Clock/Oscillator Input. When the REF_CLK is operated in single-ended mode, this pin should be decoupled to AVDD or AGND with a 0.1 µF capacitor.
23	REF_CLK	I	Reference Clock/Oscillator Input. When the REF_CLK operates in single-ended mode, Pin 23 is the input. See the Modes of Operation section for the reference clock configuration.
24	CLK_MODE_SEL	I	Control Pin for the Oscillator. CAUTION: Do not drive this pin beyond 1.8 V. When high (1.8 V), the oscillator is enabled to accept a crystal as the REF_CLK source. When low, the oscillator is bypassed.
27	LOOP_FILTER	I	Connects to the External Zero Compensation Network of the PLL Loop Filter. Typically, the network consists of a 0 Ω resistor in series with a 680 pF capacitor tied to AVDD.

Pin No.	Mnemonic	I/O	Description
6, 10, 12, 16, 28, 32	NC	N/A	No Connection. Analog Devices recommends leaving these pins floating.
40, 41, 42, 43	P0, P1, P2, P3	I	These data pins are used for modulation (FSK, PSK, ASK), start/stop for the sweep accumulator, and ramping up/down the output amplitude. Any toggle of these data inputs is equivalent to an I/O_UPDATE. The data is synchronous to the SYNC_CLK (Pin 54). The data inputs must meet the set-up and hold time requirements to the SYNC_CLK. This guarantees a fixed pipeline delay of data to the DAC output; otherwise, a ±1 SYNC_CLK period of uncertainty occurs. The functionality of these pins is controlled by profile pin configuration (PPC) bits in Register FR1 <12:14>.
46	I/O_UPDATE	I	A rising edge triggers data transfer from the I/O port buffer to active registers. I/O_UPDATE is synchronous to the SYNC_CLK (Pin 54). I/O_UPDATE must meet the set-up and hold time requirements to the SYNC_CLK to guarantee a fixed pipeline delay of data to DAC output. If not, a ±1 SYNC_CLK period of uncertainty occurs. The minimum pulse width is one SYNC_CLK period.
47	$\overline{CS}$	I	The active low chip select allows multiple devices to share a common I/O bus (SPI).
48	SCLK	I	Data Clock for I/O Operations. Data bits are written on the rising edge of SCLK and read on the falling edge of SCLK.
49	DVDD_I/O	I	3.3 V Digital Power Supply for SPI Port and Digital I/O.
50	SDIO_0	I/O	Data pin SDIO_0 is dedicated to the I/O port only.
51, 52, 53	SDIO_1, SDIO_2, SDIO_3	I/O	Data pins SDIO_1:3 can be used for the I/O port or to initiate a ramp up/ramp down (RU/RD) of the DAC output amplitude.
54	SYNC_CLK	O	The SYNC_CLK, which runs at ¼ the system clock rate, can be disabled. I/O_UPDATE and profile changes (Pin 40 to Pin 43) are synchronous to the SYNC_CLK. To guarantee a fixed pipeline delay of data to DAC output, I/O_UPDATE and profile changes (Pin 40 to Pin 43) must meet the set-up and hold time requirements to the rising edge of SYNC_CLK. If not, a ±1 SYNC_CLK period of uncertainty exists.

TYPICAL PERFORMANCE CHARACTERISTICS

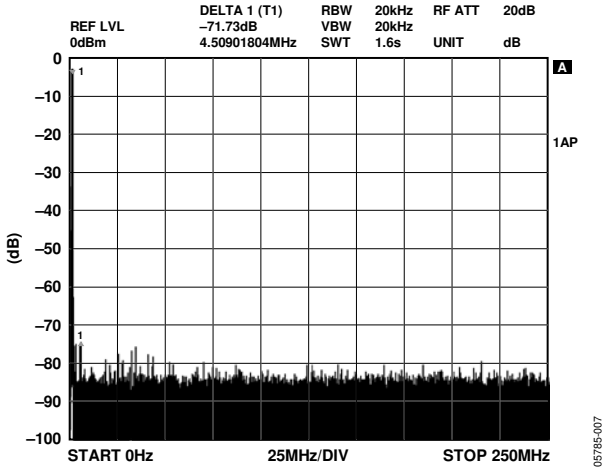

Figure 7. f_{OUT} = 1.1 MHz, f_{CLK} = 500 MSPS, Wideband SFDR

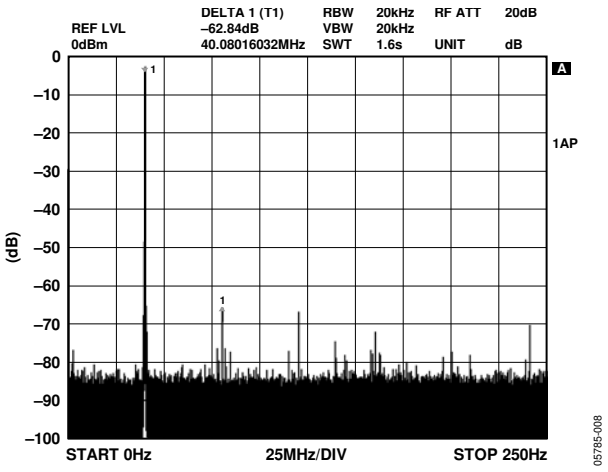

Figure 8. f_{OUT} = 40.1 MHz, f_{CLK} = 500 MSPS, Wideband SFDR

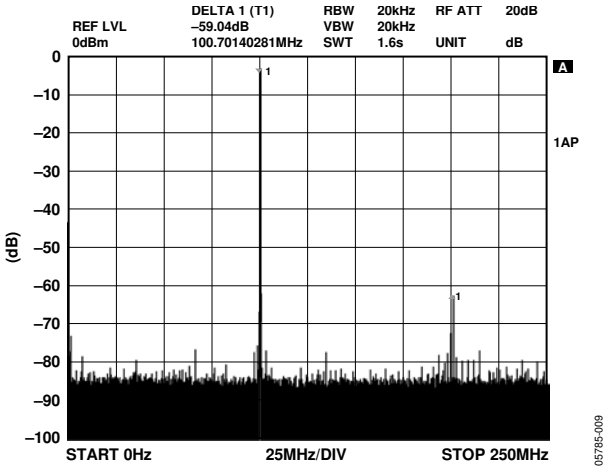

Figure 9. f_{OUT} = 100.3 MHz, f_{CLK} = 500 MSPS, Wideband SFDR

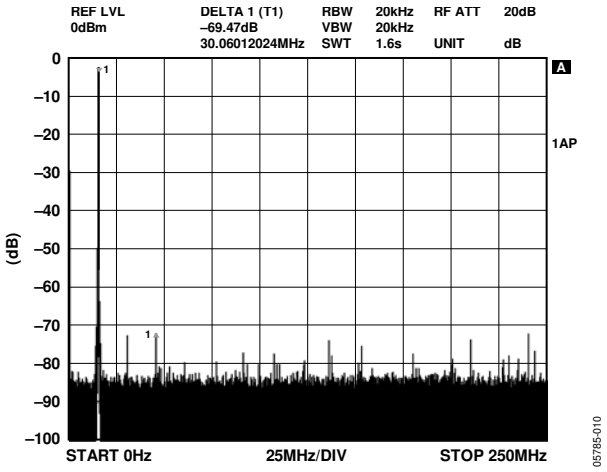

Figure 10. f_{OUT} = 15.1 MHz, f_{CLK} = 500 MSPS, Wideband SFDR

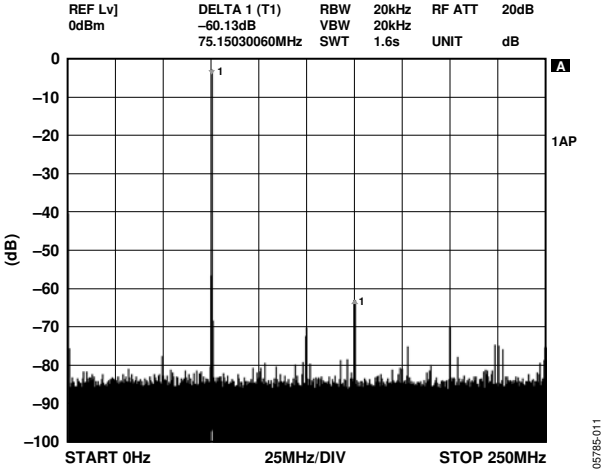

Figure 11. f_{OUT} = 75.1 MHz, f_{CLK} = 500 MSPS, Wideband SFDR

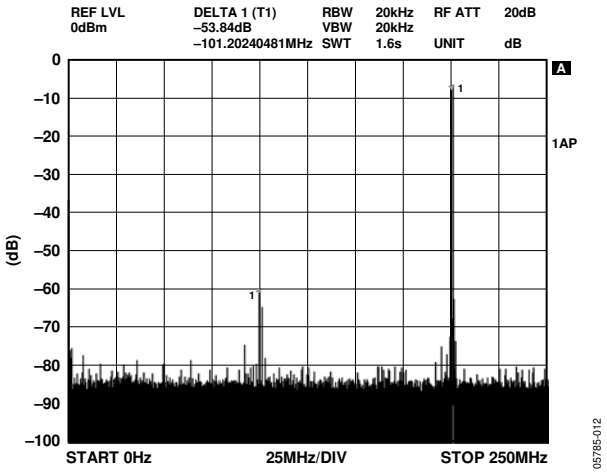

Figure 12. f_{OUT} = 200.3 MHz, f_{CLK} = 500 MSPS, Wideband SFDR

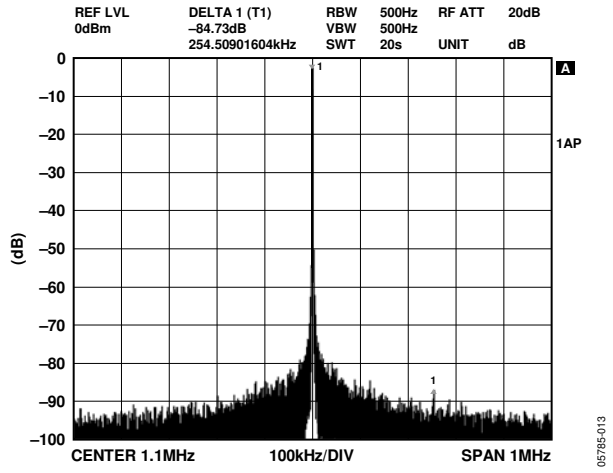

Figure 13. f_{OUT} = 1.1 MHz, f_{CLK} = 500 MSPS, NBSFDR, ±1 MHz

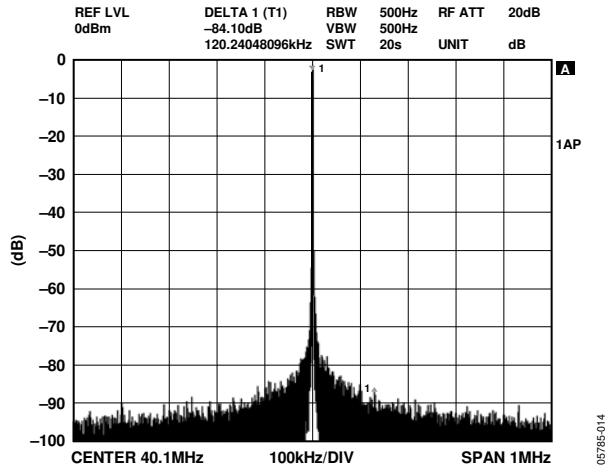

Figure 14. f_{OUT} = 40.1 MHz, f_{CLK} = 500 MSPS, NBSFDR, ±1 MHz

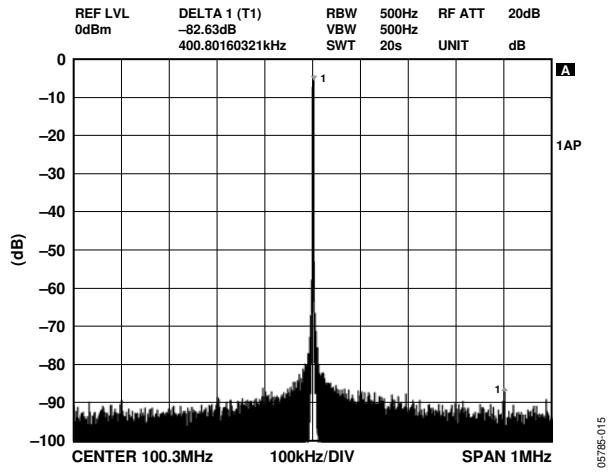

Figure 15. f_{OUT} = 100.3 MHz, f_{CLK} = 500 MSPS, NBSFDR, ±1 MHz

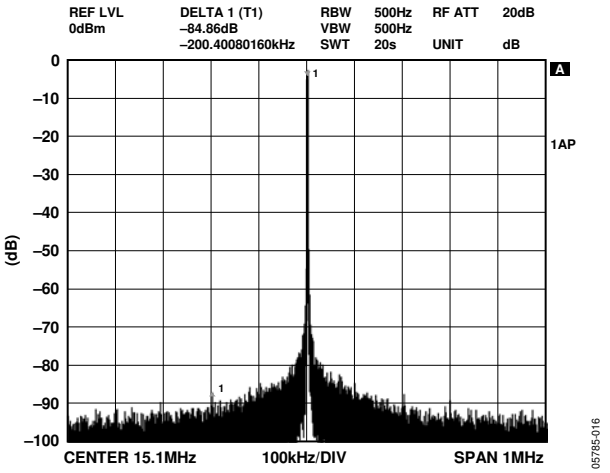

Figure 16. f_{OUT} = 15.1 MHz, f_{CLK} = 500 MSPS, NBSFDR, ±1 MHz

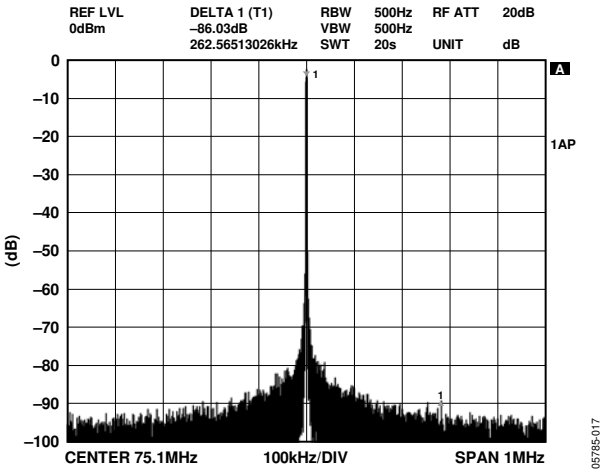

Figure 17. f_{OUT} = 75.1 MHz, f_{CLK} = 500 MSPS, NBSFDR, ±1 MHz

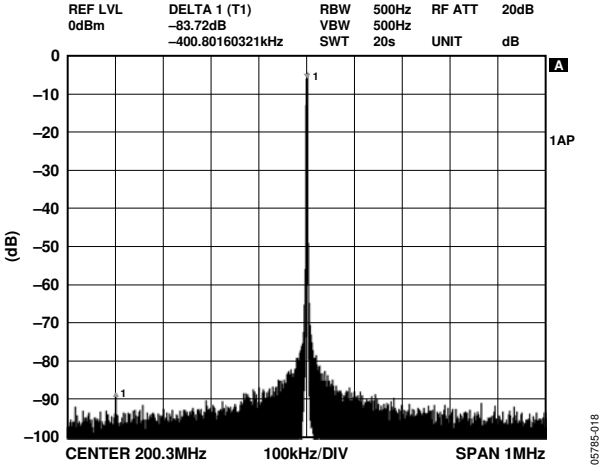

Figure 18. f_{OUT} = 200.3MHz, f_{CLK} = 500 MSPS, NBSFDR, ±1 MHz

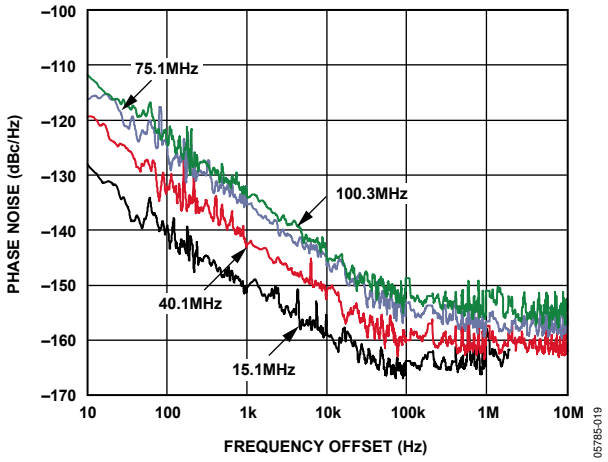

Figure 19. Residual Phase Noise (SSB) with f_{OUT} = 15.1 MHz, 40.1 MHz, 75.1 MHz, 100.3 MHz, f_{CLK} = 500 MHz with REF_CLK Multiplier Bypassed

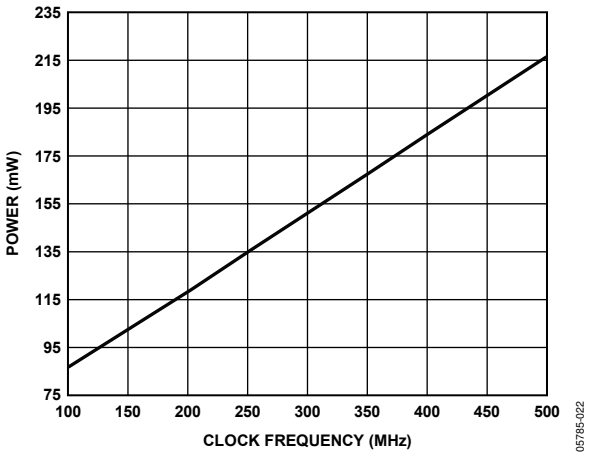

Figure 22. Power vs. System Clock Frequency

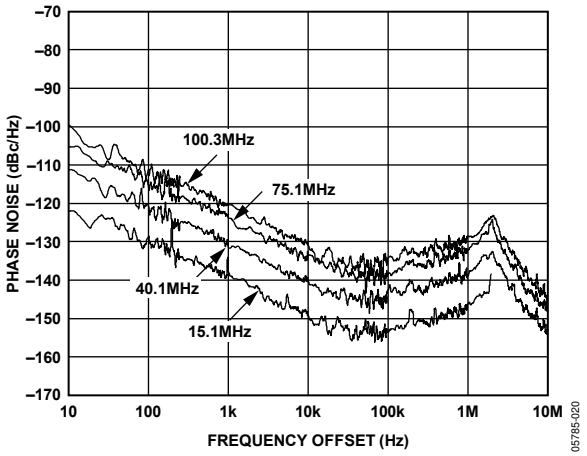

Figure 20. Residual Phase Noise (SSB) with f_{OUT} = 15.1 MHz, 40.1 MHz, 75.1 MHz, 100.3 MHz, f_{CLK} = 500 MHz with REF_CLK Multiplier = 5×

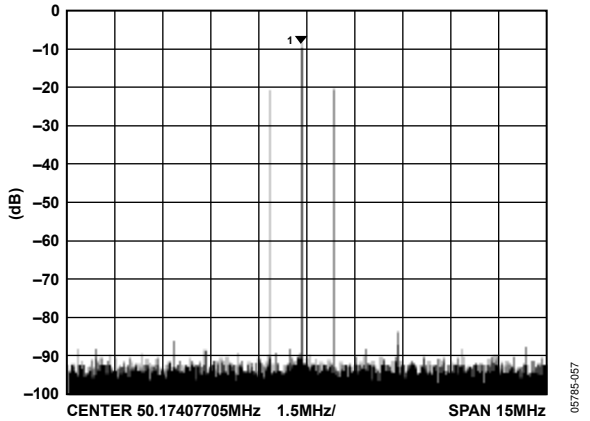

Figure 23. Amplitude Modulation Using Primary Channel (CH1 = 50 MHz) and One Auxiliary Channel (CH0 = 1 MHz)

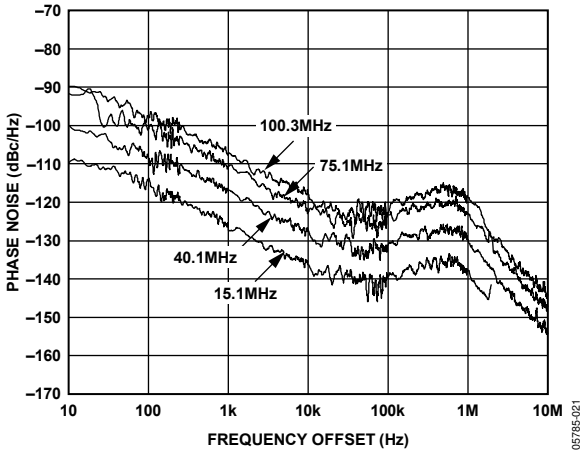

Figure 21. Residual Phase Noise(SSB) with f_{OUT} = 15.1 MHz, 40.1 MHz, 75.1 MHz, 100.3 MHz, f_{CLK} = 500 MHz with REF_CLK Multiplier = 20×

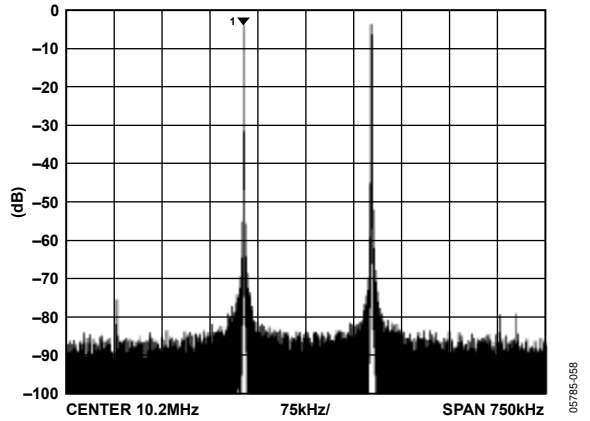

Figure 24. Two-Tone Generation Using Primary Channel (CH1 = 10.1 MHz) and One Auxiliary Channel (CH0 = 10.3 MHz)

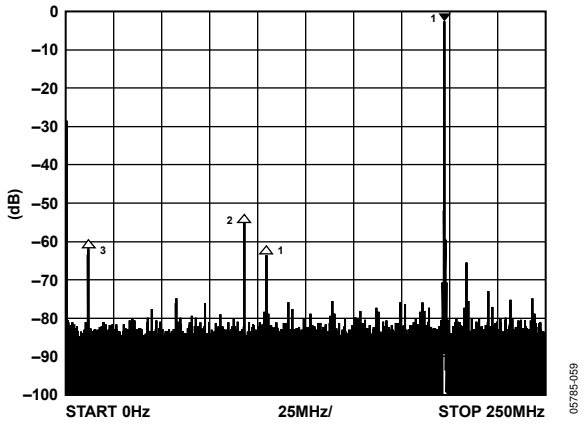

Figure 25. SpurKiller Disabled and Three Spurs Identified

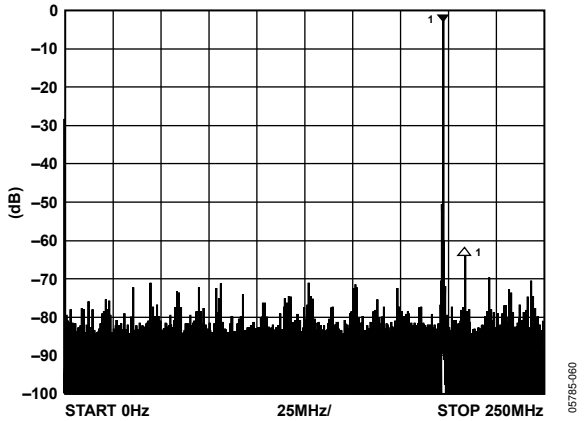

Figure 26. SpurKiller Enabled with Three Spurs Reduced (see Figure 25)

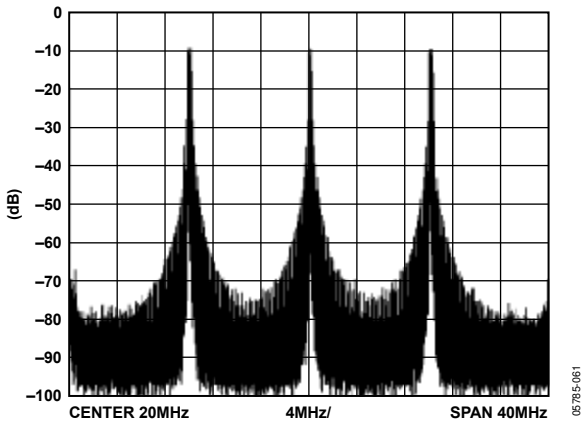

Figure 27. Three Auxiliary Channels Perform Two-Level FSK with Profile Pins. The three carriers are set to 10 MHz, 20 MHz, and 30 MHz using all three auxiliary channels.

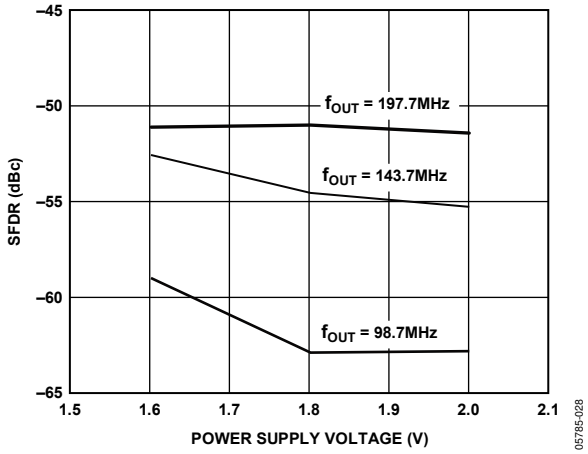

Figure 28. SFDR vs. Supply Voltage (AVDD)

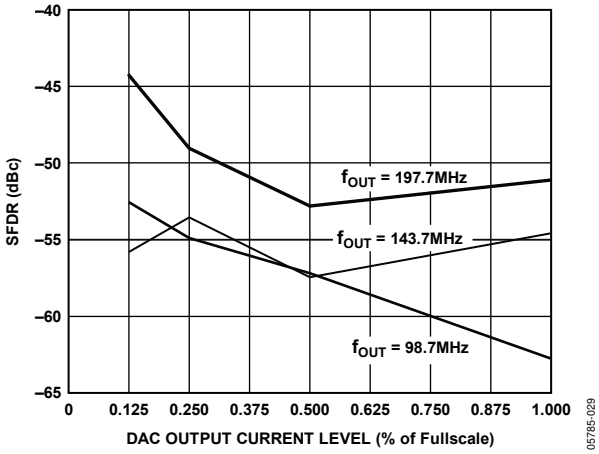

Figure 29. SFDR vs. DAC Output Current

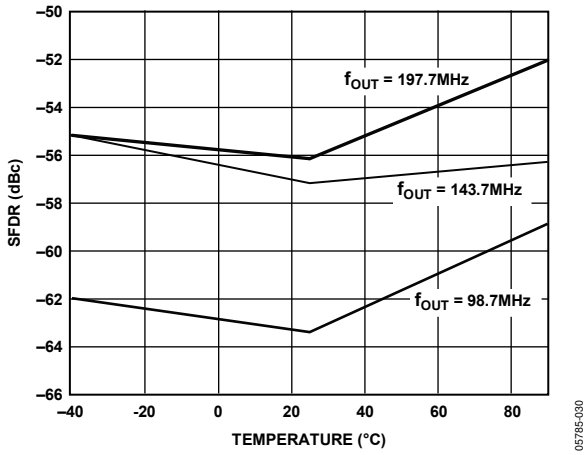

Figure 30. SFDR vs. Temperature

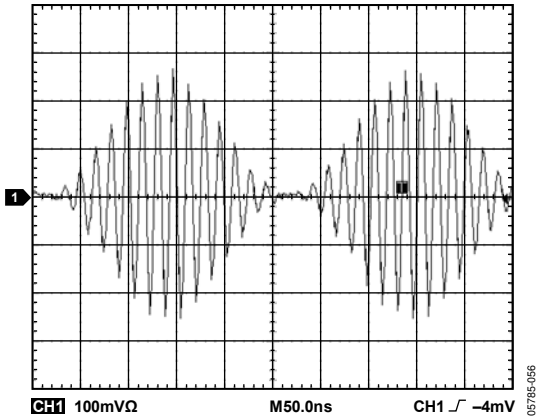

Figure 31. Primary Channel (62 MHz) 100% Amplitude Modulated by CH0 (4 MHz)

APPLICATION CIRCUITS

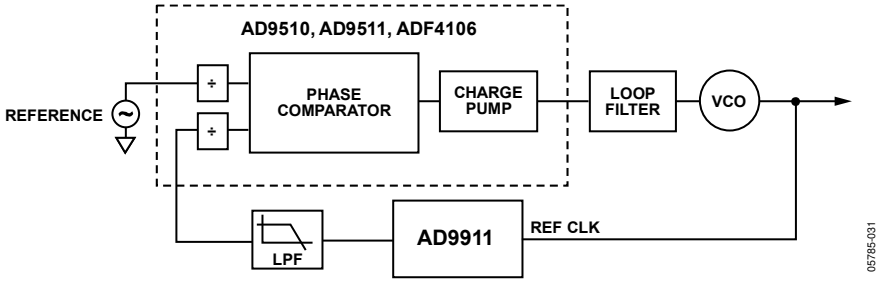

Figure 32. DDS in PLL Feedback Locking to Reference Offering Fine Frequency and Delay Adjust Tuning

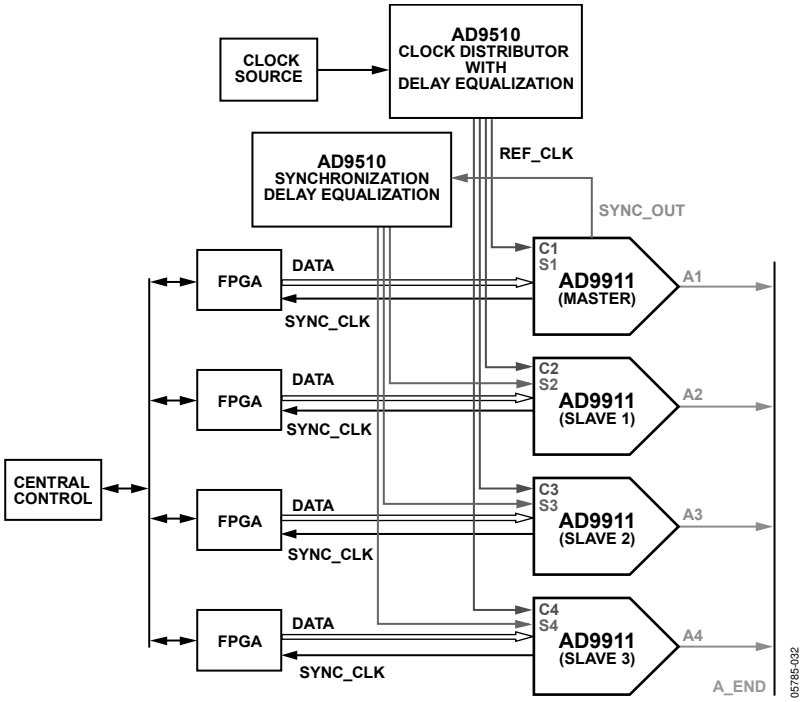

Figure 33. Synchronizing Multiple Devices to Increase Channel Capacity Using the AD9510 as a Clock Distributor for the Reference and SYNC Clock

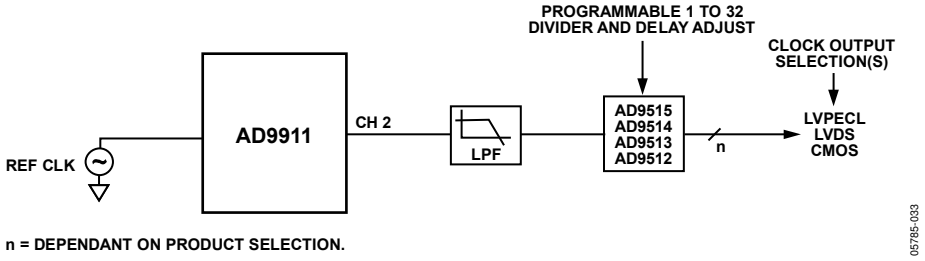

Figure 34. Clock Generation Circuit Using the AD951x Series of Clock Distribution Chips

THEORY OF OPERATION

PRIMARY DDS CORE

The AD9911 has one complete DDS (Channel 1) that consists of a 32-bit phase accumulator, a phase-to-amplitude converter, and 10-bit DAC. Together, these digital blocks generate a sine wave when the phase accumulator is clocked and the phase increment value (frequency tuning word) is greater than 0. The phase-to-amplitude converter translates phase information to amplitude information by a cos (θ) operation.

The output frequency (f_O) of the DDS is a function of the rollover rate of the phase accumulator. The exact relationship is shown in the following equation:

$$f_O = \frac{(FTW)(f_S)}{2^{32}} \; with \; 0 \le FTW \le 2^{31}$$

where:
f_S = the system clock rate.
FTW = the frequency tuning word.
2^{32} represents the capacity of the phase accumulator'.

The DDS core architecture also supports the capability to phase offset the output signal. This is performed by the channel phase offset word (CPOW). The CPOW is a 14-bit register that stores a phase offset value. This value is added to the output of the phase accumulator to offset the current phase of the output signal. The exact value of phase offset is given by the following equation:

$$\Phi = \left(\frac{CPOW}{2^{14}} \right) \times 360°$$

SPURKILLER/MULTITONE MODE AND TEST-TONE MODULATION

The AD9911 is equipped with three auxiliary DDS cores (Channel 0, Channel 2, and Channel 3). Because these channels do not have a DAC, there is no direct output. Instead, these channels are designed to implement either spur reduction/ multiple tones or test-tone modulation on the output spectrum for Channel 1.

When using multitone mode, the device can output up to four distinct carriers concurrently. This is possible via the summing node for all four DDS cores. The frequency, phase and amplitude of each tone is adjustable. The maximum amplitude of the auxiliary channels is −12 db below the primary channel's maximum amplitude to prevent overdriving the DAC input. The primary channel's amplitude can be adjusted down to achieve equal amplitude for all carriers.

When using SpurKiller mode, up to three spurs in the output spectrum for Channel 1 are reducible (one per auxiliary channel). To match an exact frequency using the three channels, the spur must be harmonically related to the fundamental frequency or the tuning word for Channel 1. A nonharmonic spur may be impossible to match frequency.

Spur reduction is not as effective at lower fundamental frequencies where SFDR performance is already very good. The benefits of SpurKiller channels are virtually nonexistent when the output frequency is less than 20% of the sampling frequency.

Test-tone modulation is similar to amplitude modulation options of a signal generator. For test-tone modulation, auxiliary DDS Channel 0 is assigned to implement amplitude sinusoidal modulated waveforms of the primary channel. This function is programmed using internal registers.

D/A CONVERTER

The AD9911 incorporates a 10-bit current output DAC. The DAC converts a digital code (amplitude) into a discrete analog quantity. The DAC current outputs can be modeled as a current source with high output impedance (typically 100 kΩ). Unlike many DACs, these current outputs require termination into AVDD via a resistor or a center-tapped transformer for expected current flow.

The DAC has complementary outputs that provide a combined full-scale output current (I_{OUT} + I_{OUTB}). The outputs always sink current.

The full-scale current is controlled by means of an external resistor (R_{SET}) and the scalable DAC current control bits discussed in the Modes of Operation section. The Resistor R_{SET} is connected between the DAC_RSET pin and analog ground (AGND). The full-scale current is inversely proportional to the resistor value as follows:

$$I_{OUT} = \frac{18.91}{R_{SET}}$$

Limiting the output to 10 mA with an R_{SET} of 1.9 kΩ provides optimal spurious-free dynamic range (SFDR) performance. The DAC output voltage compliance range is AVDD + 0.5 V to AVDD − 0.5 V. Voltages developed beyond this range can cause excessive harmonic distortion. Proper attention should be paid to the load termination to keep the output voltage within its compliance range. Exceeding this range could damage the DAC output circuitry.

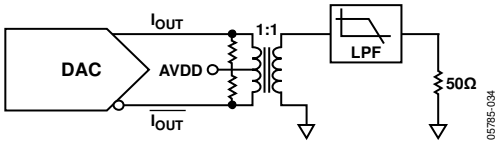

Figure 35. Typical DAC Output Termination Configuration

MODES OF OPERATION

SINGLE-TONE MODE

To configure the AD9911 in single-tone mode, the auxiliary DDS cores (CH0, CH2, and CH3) must be disabled by using the channel enable bits and digital powering down (CSR bit <7>) the three auxiliary DDS cores. Only CH1 remains enabled. See the Register Maps section for a description of the channel enable bits in the channel select register or CSR (Register 0x00). The channel enable bits are enabled or disabled immediately after the CSR data byte is written. An I/O_UPDATE is not required for channel enable bits.

The two main registers used in this mode, Register 0x04 and Register 0x05, contain the frequency tuning word and the phase offset word for CH1. The following is a basic protocol to program a frequency tuning word and/or phase offset word for CH1.

1. Power up the AD9911 and issue a master reset. A master reset places the part in single-bit mode for serial programming operations (refer to the I/O Modes of Operation section). The frequency tuning word and phase offset word for CH1 defaults to 0.
2. Disable CH0, CH2, CH3 and enable CH1 using the channel enable bits in Register 0x00.
3. Using the I/O port, program the desired frequency tuning word (Register 0x04) and/or the phase offset word (Register 0x05) for CH1.
4. Send an I/O update signal. CH1 should output its programmed frequency and/or phase offset value, after a pipeline delay (see Table 1).

Single-Tone Mode—Matched Pipeline Delay

In single-tone mode, the AD9911 offers matched pipeline delay to the DAC input for all frequency, phase, and amplitude changes. The result is that frequency, phase, and amplitude changes arrive at the DAC input simultaneously. The feature is enabled by asserting the match pipeline delay bit found in the channel function register (CSR) (Register 0x03). This feature is available in single-tone mode only.

SPURKILLER/MULTITONE MODE

For both SpurKiller and multitone mode, the frequency, phase and amplitude settings of the auxiliary channels and the primary channel use Register 0x04 Bits <31:0> for frequency and Register 0x05 Bits <13:0> for phase. Note the channel enable bits in the CSR register must be use to distinguish the content of each channel. See the I/O Port section for details.

For multitone mode, the digital content of the three auxiliary DDS channels are summed with the primary channel. Each tone can be individually programmed for frequency, phase and amplitude as well as individually modulated using the profile pins in shift-keying modulation. See Figure 24 and Figure 27 for examples.

Note the data align bits in Register 0x03 Bits <18:16>, provide a coarse amplitude adjust setting for the auxiliary channels. These bits default to clear; for multitone mode these bit should typically be set.

For SpurKiller mode, the digital contents of the three auxiliary DDS channels are attenuated and summed with the primary channel. In this manner, harmonic spurs from the DAC can be reduced. This is accomplished by matching the frequency of the harmonic component, the amplitude, and the phase (180° offset) of the desired spur on one of the SpurKiller channels.

Bench level observations and manipulation are required to establish the optimal parameter settings for the SpurKiller channel(s). The parameters are dependent on the fundamental frequency and system clock frequency. The repeatability of these settings on a unit-to-unit basis depends directly on the SFDR variation of the DAC. The DAC on the AD9911 has enough part-to-part SFDR variation that using a set of fixed programming values across multiple devices will not consistently improve SFDR.

Spur reduction performance on an individual device is stable over supply and temperature. The SpurKiller/multitone mode configuration is illustrated in Figure 36.

The amplitude of the auxiliary channels uses coarse and fine adjustments to match the amplitude of the targeted spur. The coarse adjust is implemented via the data align bits in Register 0x03 Bits <18:16>. The approximate amplitude of the auxiliary channel is programmable between −60 dB and −12 dB compared to the full-scale fundamental, per the following equation:

$$AMP = -60\text{ dB} + (D \times 6\text{ dB})$$

where AMP is the amplitude and D is the decimal value (0-7) of the data align bits

For fine amplitude adjustments, the 10-bit output scalar (multiplier) of the auxiliary channel in Register 0x06 Bit <0:9> is used. The multiplier is enabled by Register 0x06 Bit <12>.

A single active SpurKiller channel targeting the second harmonic is expressed as

$$f_{OUT} = A \times \cos(\omega t + \Phi_1) + B \times \cos(2\omega t + \Phi_2) + B \times \cos(2\omega t + \Phi_2 + 180°) + (\text{all other spurious components})$$

where $B \times \cos(2\omega t + \Phi_2 + 180°)$ represents the fundamental tone of the SpurKiller channel.

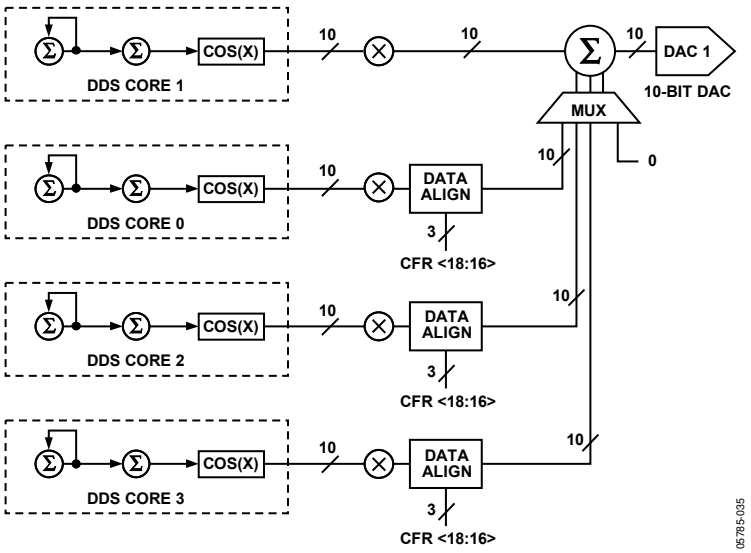

Figure 36. SpurKiller/Multitone Mode Configuration

TEST-TONE MODE

Test-tone mode enables sinusoidal amplitude modulation of the carrier (CH1). Setting Bit 2 in Register 0x01 enables test-tone mode. Auxiliary CH2 and CH3 should both be disabled using the channel enable bits (CSR Bit <7>). The frequency of modulation is set using the frequency tuning word (Register 0x04 Bits <31:0>) of auxiliary CH0. Auxiliary CH0 output scalar (Register 0x06 Bits <0:9>) sets the magnitude of the modulating signal. See Figure 37 for a diagram of the test-tone mode configuration.

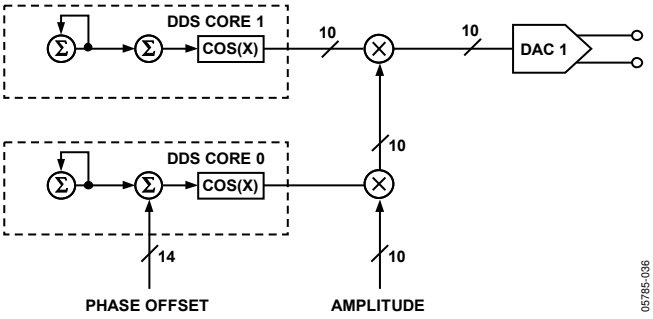

Figure 37. Test-Tone Mode Configuration

REFERENCE CLOCK MODES

The AD9911 supports several methods for generating the internal system clock. An on-chip oscillator circuit is available for initiating the low frequency reference signal by connecting a crystal to the clock input pins. The system clock can also be generated using the internal, PLL-based reference clock multiplier, allowing the part to operate with a low frequency clock source while still providing a high sample rate for the DDS and DAC. For best phase noise performance, a clean, stable clock with a high slew rate is required.

Enabling the PLL allows multiplication of the reference clock frequency from 4× to 20×, in integer steps. The PLL multiplication value is 5-bits located in the Function Register 1 (FR1) Bits <22:18>. For further information, refer to the Register Map section.

When FR1 <22:18> is programmed with values ranging from 4 to 20 (decimal), the clock multiplier is enabled. The integer value in the register represents the multiplication factor. The system clock rate with the clock multiplier enabled is equal to the reference clock rate times the multiplication factor. If FR1 <22:18> is programmed with a value less than 4 or greater than 20, the clock multiplier is disabled. Note that the output frequency of the PLL has a restricted frequency range. There is a VCO gain bit that must be set appropriately. The VCO gain bit (FR1<23>) defines two ranges (low/high) of frequency output. See the Register Map section for configuration directions and defaults.

The charge pump current in the PLL defaults to 75 μA, which typically produces the best phase noise characteristics. Increasing charge pump current typically degrades phase noise, but decreases the lock time and alters the loop bandwidth. The charge pump control bits (FR1 <17:16>) function is described in the Register Map section.

To enable the on-chip oscillator for crystal operation, drive CLK_MODE_SEL (Pin 24) high. The CLKMODESEL pin is considered an analog input, operating on 1.8 V logic. With the on-chip oscillator enabled, connection of an external crystal to the REF_CLK and REF_CLKB inputs is made producing a low frequency reference clock. The crystal frequency must be in the range of 20 MHz to 30 MHz. summarizes the clock mode options. See the Register Maps section for more details.

Table 4.

CLK_MODE_SEL Pin 24	FR1 <22:18> PLL, Bits = M	Oscillator Enabled	System Clock (f_{SYSCLK})	Min/Max Frequency Range (MHz)
High = 1.8 V Logic	4 ≤ M ≤ 20	Yes	$f_{SYSCLK} = f_{OSC} \times M$	$100 < f_{SYSCLK} < 500$
High = 1.8 V Logic	M < 4 or M > 20	Yes	$f_{SYSCLK} = f_{OSC}$	$20 < f_{SYSCLK} < 30$
Low	4 ≤ M ≤ 20	No	$f_{SYSCLK} = f_{REF\ CLK} \times M$	$100 < f_{SYSCLK} < 500$
Low	M < 4 or M > 20	No	$f_{SYSCLK} = f_{REF\ CLK}$	$0 < f_{SYSCLK} < 500$

Reference Clock Input Circuitry

The reference clock input circuitry has two modes of operation. The first mode (logic low) configures the circuitry as an input buffer. In this mode, the reference clock must be ac-coupled to the input due to internal dc biasing. This mode supports either differential or single-ended configurations. If single-ended mode is desired, the complementary reference clock input (Pin 23) should be decoupled to AVDD or AGND via a 0.1 µF capacitor. The following three figures exemplify common reference clock configurations for the AD9911.

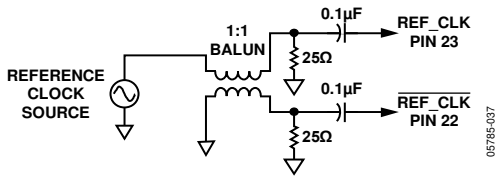

Figure 38. Typical Reference Clock Configuration for Sine Wave Source

The reference clock inputs can also support an LVPECL or PECL driver as the reference clock source.

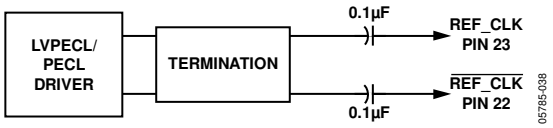

Figure 39. Typical Reference Clock Configuration for LVPECL/PECL Source

For external crystal operation, both clock inputs must be dc-coupled via the crystal leads and bypassed. Figure 40 shows the configuration when a crystal is used.

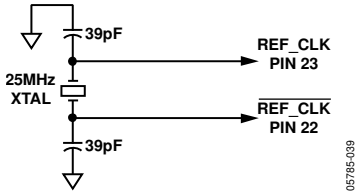

Figure 40. Crystal Configuration for Reference Clock Source

SCALABLE DAC REFERENCE CURRENT CONTROL MODE

Set the full-scale output current using bits CFR <9:8>, as shown in Table 5.

Table 5.

CFR <9:8>		LSB Current State
1	1	Full-scale
0	1	Half-scale
1	0	Quarter-scale
0	0	Eighth-scale

POWER-DOWN FUNCTIONS

The AD9911 supports pin-controlled power-down plus numerous software selectable power-down modes. Software controlled power-down allows the input clock circuitry, DAC, and the digital logic (for the primary and auxiliary DDS cores) to be individually powered.

When the PWR_DWN_CTL input pin is high, the AD9911 enters power-down mode based on the FR1 <6> bit. When the PWR_DWN_CTL input pin is low, the individual power-down bits (CFR <7:4>) control the power-down modes of operation. See the Control Register Descriptions section for further details.

SHIFT KEYING MODULATION

The AD9911 can perform 2-/4-/8- or 16-level modulation of frequency, phase, or amplitude (FSK, PSK, ASK) by applying data to the profile pins. SYNC_CLK must be enabled when performing FSK, PSK, or ASK, while the auxiliary DDS cores must be disabled. Digital power down (CSR Bit <7>) of the auxiliary channels is recommended.

In addition, the AD9911 has the ability to ramp up or ramp down the output amplitude before, during, or after a modulation (FSK, PSK only) sequence. This is accomplished by using the 10-bit output scalar. Profile pins or SDIO_1:3 pins can be configured to initiate the ramp up/ramp down (RU/RD) operation. See the Output Amplitude Control section for further details.

In modulation mode, a set of control bits (CFR<23:22>) determines the type (frequency, phase, or amplitude) of modulation. The primary channel (CH1) has 16 profile registers. Register Address 0x0A through Register Address 0x18 are profile registers for modulation of frequency, phase, or amplitude. Register 0x04, Register 0x05, and Register 0x06 are dedicated registers for frequency, phase, and amplitude, respectively.

These registers contain the initial frequency, phase offset and amplitude word. Frequency modulation is 32-bit resolution, phase modulation is 14 bit, and amplitude is 10 bit. When modulating phase or amplitude, the word value must be MSB-aligned in the profile registers; excess bits are ignored. In

modulation mode, bits CFR <23:22> and FR1 <9:8> configure the modulation type and level. See Table 6 and Table 7 for settings. Note that the linear sweep enable bit must be set to Logic 0 in modulation mode.

Table 6.

CFR <23:22>		CFR <14>	Description
0	0	x	Modulation disabled
0	1	0	Amplitude modulation
1	0	0	Frequency modulation
1	1	0	Phase modulation

Table 7.

FR1 <9:8>		Description
0	0	2-level modulation
0	1	4-level modulation
1	0	8-level modulation
1	1	16-level modulation

When both modulation and the RU/RD feature are desired, unused profile pins or SDIO pins can be assigned. SDIO pins can only be used for RU/RD.

Table 8.

RU/RD Bits FR1 <11:10>		Description
0	0	RU/RD disabled.
0	1	Profile Pin 2 and Pin 3 configured for RU/RD operation.
1	0	Profile Pin 3 configured for RU/RD operation.
1	1	SDIO Pin 1, Pin 2, and Pin 3 configured for RU/RD operation. Forces the I/O to be used only in 1-bit mode.

If profile pins are used for RU/RD, Logic 0 sets for ramp up and Logic 1 sets for ramp down.

To support RU/RD flexibility, it is necessary to assign the profile pins and/or SDIO Pin 1 to Pin 3 to CH1 operation. This is controlled by the profile pin configuration (PPC) or PPC bits (FR1 <14:12>). The modulation descriptions that follow include data pin assignment. In the modulation descriptions, an "x" indicates that it does not matter.

2-Level Modulation—No RU/RD

Modulation level bits are set to 00 (2-level). AFP bits are set to the desired modulation. RU/RD bits and the linear sweep bit are disabled. Table 9 displays how the profile pins are assigned.

Table 9. 2-Level Modulation—No RU/RD

Bits FR1<14:12>			P0	P1	P2	P3
x	x	x	N/A	CH1	N/A	N/A

As shown in Table 9, only Profile Pin P1 can be used to modulate CH1. If Pin P1 is Logic 0 and FSK modulation is desired, then Profile Register 0 (Register 0x04) frequency is chosen. If Pin P1 is Logic 1, then Profile Register 1 (Register 0x0A) frequency is chosen.

4-Level Modulation—No RU/RD

Modulation level bits are set to 01 (4-level). AFP bits are set to the desired modulation. RU/RD bits and the linear sweep bit are disabled. Table 10 displays how the profile pins are assigned.

Table 10. 4-Level Modulation—No RU/RD

Profile Pin Configuration (PPC) Bits FR1 <14:12>			P0	P1	P2	P3
0	1	1	CH1	CH1	N/A	N/A

For this condition, the profile register chosen is based on the 2 bit value presented to profile pins <P0:P1>. For example, if PPC = 011 and <P0:P1>= 11, then the contents of Profile Register 3 (Register 0x0C) are presented to CH1 output.

8-Level Modulation—No RU/RD

Modulation level bits are set to 10 (8-level). AFP bits are set to the desired modulation. RU/RD bits and the linear sweep bit are disabled. Table 11 shows the assignment of profile pins and channels.

Table 11. 8-Level Modulation—No RU/RD

Profile Pin Config. Bits FR1 <14:12>			P0	P1	P2	P3
x	0	1	CH1	CH1	CH1	x

For this condition, the profile register (1 of 8) chosen is based on the 3-bit value presented to the Profile Pin P0 to Pin P2. For example, if PPC = x01 and <P0:P2> = 111, then the contents of Profile Register 7 (Register 0x10) are presented to CH1 output.

16-Level Modulation—No RU/RD

Modulation level bits are set to 11 (16-level). AFP bits are set to the desired modulation. RU/RD bits and the linear sweep bit are disabled. Table 12 displays how the profile pins and channels are assigned.

Table 12. 16-Level Modulation—No RU/RD

Profile Pin Config. (PPC) Bits FR1 <14:12>			P0	P1	P2	P3
x	0	1	CH1	CH1	CH1	CH1

For these conditions, the profile register chosen is based on the 4-bit value presented to Profile Pin P0 to Pin P3. For example, if PPC = x01 and <P0:P3>= 1110, then the contents of Profile Register 14 (Register 0x17) are presented to CH1 output.

2-Level Modulation Using Profile Pins for RU/RD

When the RU/RD bits = 01, either Profile Pin P2 or Pin P3 are available for RU/RD. Note that only a modulation level of two is available when RU/RD bits = 01. See Table 13 for available pin assignments.

Table 13. 2-Level Modulation—RU/RD

Profile Pin Config. Bits FR1<14:12>			P0	P1	P2	P3
0	0	0	N/A	CH1	N/A	CH1 RU/RD
0	1	1	CH1	N/A	CH1 RU/RD	N/A

8-Level Modulation Using a Profile Pin for RU/RD

When the RU/RD bits = 10, Profile Pin P3 is available for RU/RD. Note that only a modulation level of eight is available when the RU/RD bits = 10. See Table 14 for available pin assignments.

Table 14. 8-Level Modulation—RU/RD

Profile Pin Config. Bits FR1 <14:12>			P0	P1	P2	P3
x	0	1	CH1	CH1	CH1	CH1 RU/RD

SHIFT KEYING MODULATION USING SDIO PINS FOR RU/RD

For RU/RD bits = 11, SDIO Pin 1, Pin 2, and Pin 3 are available for RU/RD. In this mode, modulation levels of 2, 4, and 16 are available. Note that the I/O port can only be used in 1-bit serial mode.

Table 15. 2-Level Modulation Using SDIO Pins for RU/RD

Profile Pin Config. Bits FR1 <14:12>			P0	P1	P2	P3
x	x	x	N/A	CH1	N/A	N/A

In this case, the SDIO pins can be used for the RU/RD function, as described in Table 16.

Table 16. SDIO Pins

1	2	3	Description
0	1	0	Triggers the ramp-up function for CH1
0	1	1	Triggers the ramp-down function for CH1

4-Level Modulation Using SDIO Pins for RU/RD

For RU/RD = 11 (SDIO Pin 1 and Pin 2 are available for RU/RD), the modulation level is set to four. See Table 17 for pin assignments, including SDIO pin assignments.

Table 17.

Profile Pin Config. Bits (FR1<14:12>)			P0	P1	P2	P3	SDIO_1	SDIO_2	SDIO_3
0	0	0	N/A	N/A	CH1	CH1	N/A	CH1 RU/RD	N/A
0	1	1	CH1	CH1	N/A	N/A	CH1 RU/RD	N/A	N/A

For the configuration shown in Table 17, the profile register is chosen based on the 2-bit value presented to <P0:P1> or <P2:P3>. For example, if PPC = 011, <P0:P1> = 11, then the contents of Profile Register 3 (Register 0x0C) are presented to CH1 output. SDIO Pin 1 and Pin 2 provide the RU/RD function.

16-Level Modulation Using SDIO Pins for RU/RD

RU/RD = 11 (SDIO Pin 1 available for RU/RD) and the level is set to 16. See the pin assignment shown in Table 18.

Table 18.

Profile Pin Config. Bits (FR1<14:12>)			P0	P1	P2	P3	SDIO_1	SDIO_2	SDIO_3
x	0	1	CH1	CH1	CH1	CH1	CH1 RU/RD	N/A	N/A

For the configuration shown in Table 18, the profile register is chosen based on the 4-bit value presented to <P0:P3>. For example, if PPC = x01 and <P0:P3> = 1101, then the contents of Profile Register 13 (Register 0x16) are presented to CH1 output. The SDIO_1 pin provides the RU/RD function.

LINEAR SWEEP (SHAPED) MODULATION MODE

Linear sweep enables the user to sweep frequency, phase, or amplitude from a starting point (S0) to an endpoint (E0). The purpose of linear sweep mode is to provide better bandwidth containment compared to direct modulation mode by enabling more gradual, user-defined changes between S0 and E0. Note that SYNC_CLK must be enabled when using Linear Sweep while the auxiliary DDS cores must be disabled. Digital power down (CSR bit <7>) of the auxiliary channels is recommended. Figure 41 depicts the linear sweep block diagram.

In linear sweep mode, S0 is loaded into Profile Register 0 (Profile 0 is represented by Register 0x04, Register 0x05, or Register 0x06, depending on the parameter being swept) and E0 is always loaded into Profile Register 1 (Register 0x0A). If E0 is configured for frequency sweep, the resolution is 32-bits. For phase sweep, the resolution is 14 bits and for amplitude sweep, the resolution is 10 bits. When sweeping phase or amplitude, the word value must be MSB-aligned in Profile Register 1; unused bits are ignored. Profile Pin1 triggers and controls the direction (up/down) of the linear sweep for frequency, phase, or amplitude.

The AD9911 can be programmed to ramp up or ramp down the output amplitude (using the 10-bit output scalar) before and after a linear sweep. If the RU/RD feature is desired, profile pins or SDIO_1:3 pins can be configured to control the RU/RD operation. For further details, refer to the Output Amplitude Control section. To enable linear sweep mode, AFP bits (CFR <23:22>), modulation level bits (FR1 <9:8>), and the linear sweep enable bit (CFR <14>) must be programmed. The AFP bits determine the type of linear sweep to be performed (see Table 19). The modulation level bits must be set to 00 (2-level).

Table 19.

AFP CFR <23:22>		Linear Sweep Enable CFR <14>	Description
0	0	1	N/A
0	1	1	Amplitude sweep
1	0	1	Frequency sweep
1	1	1	Phase sweep