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1 GSPS Direct Digital Synthesizer with 14-Bit DAC

AD9912

FEATURES

- 1 GSPS internal clock speed (up to 400 MHz output directly)
- Integrated 1 GSPS 14-bit DAC
- 48-bit frequency tuning word with 4 µHz resolution
- Differential HSTL comparator
- Flexible system clock input accepts either crystal or external reference clock
- On-chip low noise PLL REFCLK multiplier
- 2 SpurKiller channels
- Low jitter clock doubler for frequencies up to 750 MHz
- Single-ended CMOS comparator; frequencies of <150 MHz
- Programmable output divider for CMOS output
- Serial I/O control
- Excellent dynamic performance
- Software controlled power-down
- Available in two 64-lead LFCSP packages
- Residual phase noise @ 250 MHz
  - 10 Hz offset: −113 dBc/Hz
  - 1 kHz offset: −133 dBc/Hz
  - 100 kHz offset: −153 dBc/Hz
  - 40 MHz offset: −161 dBc/Hz

APPLICATIONS

- Agile LO frequency synthesis
- Low jitter, fine tune clock generation
- Test and measurement equipment
- Wireless base stations and controllers
- Secure communications
- Fast frequency hopping

GENERAL DESCRIPTION

The AD9912 is a direct digital synthesizer (DDS) that features an integrated 14-bit digital-to-analog converter (DAC). The AD9912 features a 48-bit frequency tuning word (FTW) that can synthesize frequencies in step sizes no larger than 4 µHz. Absolute frequency accuracy can be achieved by adjusting the DAC system clock.

The AD9912 also features an integrated system clock phase-locked loop (PLL) that allows for system clock inputs as low as 25 MHz.

The AD9912 operates over an industrial temperature range, spanning −40°C to +85°C.

BASIC BLOCK DIAGRAM

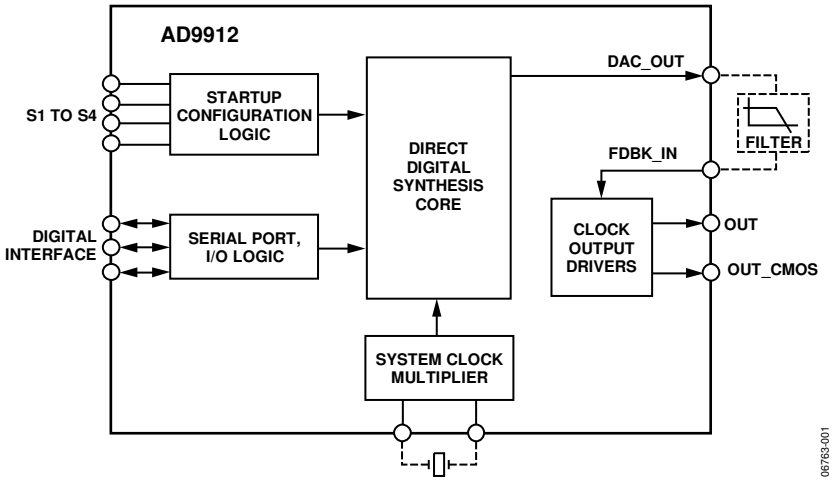

Figure 1.

Rev. F

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9912 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1389: Recommended Rework Procedure for the Lead Frame Chip Scale Package (LFCSP)
- AN-1396: How to Predict the Frequency and Magnitude of the Primary Phase Truncation Spur in the Output Spectrum of a Direct Digital Synthesizer (DDS)
- AN-237: Choosing DACs for Direct Digital Synthesis
- AN-280: Mixed Signal Circuit Technologies
- AN-342: Analog Signal-Handling for High Speed and Accuracy
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-419: A Discrete, Low Phase Noise, 125 MHz Crystal Oscillator for the AD9850
- AN-423: Amplitude Modulation of the AD9850 Direct Digital Synthesizer
- AN-543: High Quality, All-Digital RF Frequency Modulation Generation with the ADSP-2181 and the AD9850 DDS
- AN-557: An Experimenter's Project:
- AN-587: Synchronizing Multiple AD9850/AD9851 DDS-Based Synthesizers
- AN-605: Synchronizing Multiple AD9852 DDS-Based Synthesizers
- AN-621: Programming the AD9832/AD9835
- AN-632: Provisionary Data Rates Using the AD9951 DDS as an Agile Reference Clock for the ADN2812 Continuous-Rate CDR
- AN-769: Generating Multiple Clock Outputs from the AD9540
- AN-772: A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)
- AN-823: Direct Digital Synthesizers in Clocking Applications Time
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-843: Measuring a Loudspeaker Impedance Profile Using the AD5933
- AN-847: Measuring a Grounded Impedance Profile Using the AD5933
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design

- AN-927: Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)
- AN-939: Super-Nyquist Operation of the AD9912 Yields a High RF Output Signal
- AN-953: Direct Digital Synthesis (DDS) with a Programmable Modulus

Data Sheet

- AD9912: 1 GSPS Direct Digital Synthesizer with 14-Bit DAC Data Sheet

Product Highlight

- Introducing Digital Up/Down Converters: VersaCOMM™ Reconfigurable Digital Converters

Technical Books

- A Technical Tutorial on Digital Signal Synthesis, 1999

User Guides

- UG-475: Evaluating the AD9912 1 GSPS Direct Digital Synthesizer with 14-Bit DAC

TOOLS AND SIMULATIONS

- AD9912 IBIS Models

REFERENCE DESIGNS

- CN0109

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

Technical Articles

- 400-MSample DDSs Run On Only +1.8 VDC
- ADI Buys Korean Mobile TV Chip Maker
- Basics of Designing a Digital Radio Receiver (Radio 101)
- DDS Applications
- DDS Circuit Generates Precise PWM Waveforms
- DDS Design
- DDS Device Produces Sawtooth Waveform
- DDS Device Provides Amplitude Modulation
- DDS IC Initiates Synchronized Signals
- DDS IC Plus Frequency-To-Voltage Converter Make Low-Cost DAC
- DDS Simplifies Polar Modulation
- Digital Potentiometers Vary Amplitude In DDS Devices
- Digital Up/Down Converters: VersaCOMM™ White Paper
- Digital Waveform Generator Provides Flexible Frequency Tuning for Sensor Measurement
- Improved DDS Devices Enable Advanced Comm Systems
- Integrated DDS Chip Takes Steps To 2.7 GHz
- Simple Circuit Controls Stepper Motors
- Speedy A/Ds Demand Stable Clocks
- Synchronized Synthesizers Aid Multichannel Systems
- The Year of the Waveform Generator
- Two DDS ICs Implement Amplitude-shift Keying
- Video Portables and Cameras Get HDMI Outputs

DESIGN RESOURCES

- AD9912 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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6/10—Rev. E to Rev. F

Changed Default Value of Register 0x003 to 0x19 (Table 12).....31

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11/09—Rev. C to Rev. D

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10/07—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V ± 5%, AVDD3 = 3.3 V ± 5%, DVDD = 1.8 V ± 5%, DVDD_I/O = 3.3 V ± 5%, AVSS = 0 V, DVSS = 0 V, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
DVDD_I/O (Pin 1)	3.135	3.30	3.465	V	
DVDD (Pin 3, Pin 5, Pin 7)	1.71	1.80	1.89	V	
AVDD3 (Pin 14, Pin 46, Pin 47, Pin 49)	3.135	3.30	3.465	V	
AVDD3 (Pin 37)	1.71	3.30	3.465	V	Pin 37 is typically 3.3 V but can be set to 1.8 V
AVDD (Pin 11, Pin 19, Pin 23 to Pin 26, Pin 29, Pin 30, Pin 36, Pin 42, Pin 44, Pin 45, Pin 53)	1.71	1.80	1.89	V	
SUPPLY CURRENT					See also the Total Power Dissipation specifications
I_{AVDD3} (Pin 37)		8	9.6	mA	CMOS output driver at 3.3 V, 50 MHz, with 5 pF load
I_{AVDD3} (Pin 46, Pin 47, Pin 49)		26	31	mA	DAC output current source, f_S = 1 GSPS
I_{AVDD} (Pin 11, Pin 19, Pin 23 to Pin 26, Pin 29, Pin 30, Pin 36, Pin 42, Pin 44, Pin 45)		113	136	mA	Aggregate analog supply, with system clock PLL, HSTL output driver, and S-divider enabled
I_{AVDD} (Pin 53)		40	48	mA	DAC power supply
I_{DVDD} (Pin 3, Pin 5, Pin 7)		205	246	mA	Digital core (SpurKiller off)
$I_{DVDD\_I/O}$ (Pin 1, Pin 14[1])		2	3	mA	Digital I/O (varies dynamically)
LOGIC INPUTS (Except Pin 32)					Pin 9, Pin 10, Pin 54, Pin 55, Pin 58 to Pin 61, Pin 63, Pin 64
Input High Voltage (V_{IH})	2.0		DVDD_I/O	V	
Input Low Voltage (V_{IL})	DVSS		0.8	V	
Input Current (I_{INH}, I_{INL})		±60	±200	µA	At V_{IN} = 0 V and V_{IN} = DVDD_I/O
Maximum Input Capacitance (C_{IN})		3		pF	
CLKMODESEL (Pin 32) LOGIC INPUT					Pin 32 only
Input High Voltage (V_{IH})	1.4		AVDD	V	
Input Low Voltage (V_{IL})	AVSS		0.4	V	
Input Current (I_{INH}, I_{INL})		−18	−50	µA	At V_{IN} = 0 V and V_{IN} = AVDD
Maximum Input Capacitance (C_{IN})		3		pF	
LOGIC OUTPUTS					Pin 62 and the following bidirectional pins: Pin 9, Pin 10, Pin 54, Pin 55, Pin 63
Output High Voltage (V_{OH})	2.7		DVDD_I/O	V	I_{OH} = 1 mA
Output Low Voltage (V_{OL})	DVSS		0.4	V	I_{OL} = 1 mA
FDBK_IN INPUT					Pin 40, Pin 41
Input Capacitance		3		pF	
Input Resistance	18	22	26	kΩ	Differential
Differential Input Voltage Swing	225			mV p-p	Equivalent to 112.5 mV swing on each leg; must be ac-coupled

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYSTEM CLOCK INPUT					System clock inputs should always be ac-coupled (both single-ended and differential)
SYSCLK PLL Bypassed					
Input Capacitance		1.5		pF	Single-ended, each pin
Input Resistance	2.4	2.6	2.9	kΩ	Differential
Internally Generated DC Bias Voltage[2]	0.93	1.17	1.38	V	
Differential Input Voltage Swing	632			mV p-p	Equivalent to 316 mV swing on each leg
SYSCLK PLL Enabled					
Input Capacitance		3		pF	Single-ended, each pin
Input Resistance	2.4	2.6	2.9	kΩ	Differential
Internally Generated DC Bias Voltage[2]	0.93	1.17	1.38	V	
Differential Input Voltage Swing	632			mV p-p	Equivalent to 316 mV swing on each leg
Crystal Resonator with SYSCLK PLL Enabled					
Motional Resistance		9	100	Ω	25 MHz, 3.2 mm × 2.5 mm AT cut
CLOCK OUTPUT DRIVERS					
HSTL Output Driver					
Differential Output Voltage Swing	1080	1280	1480	mV	Output driver static, see Figure 27 for output swing vs. frequency
Common-Mode Output Voltage[2]	0.7	0.88	1.06	V	
CMOS Output Driver					Output driver static, see Figure 28 and Figure 29 for output swing vs. frequency
Output Voltage High (V_{OH})	2.7			V	I_{OH} = 1 mA, Pin 37 = 3.3 V
Output Voltage Low (V_{OL})			0.4	V	I_{OL} = 1 mA, Pin 37 = 3.3 V
Output Voltage High (V_{OH})	1.4			V	I_{OH} = 1 mA, Pin 37 = 1.8 V
Output Voltage Low (V_{OL})			0.4	V	I_{OL} = 1 mA, Pin 37 = 1.8 V
TOTAL POWER DISSIPATION					
DDS Only		637	765	mW	Power-on default, except SYSCLK PLL bypassed and CMOS driver off; SYSCLK = 1 GHz; HSTL driver off; spur reduction off; f_{OUT} = 200 MHz
DDS with Spur Reduction On		686	823	mW	Same as "DDS Only" case, except both spur reduction channels on
DDS with HSTL Driver Enabled		657	788	mW	Same as "DDS Only" case, except HSTL driver enabled
DDS with CMOS Driver Enabled		729	875	mW	Same as "DDS Only" case, except CMOS driver and S-divider enabled and at 3.3 V; CMOS f_{OUT} = 50 MHz (S-divider = 4)
DDS with HSTL and CMOS Drivers Enabled		747	897	mW	Same as "DDS Only" case, except both HSTL and CMOS drivers enabled; S-divider enabled and set to 4; CMOS f_{OUT} = 50 MHz
DDS with SYSCLK PLL Enabled		648	777	mW	Same as "DDS Only" case, except 25 MHz on SYCLK input and PLL multiplier = 40
Power-Down Mode		13	16	mW	Using either the power-down and enable register or the PWRDOWN pin

[1] Pin 14 is in the AVDD3 group, but it is recommended that Pin 14 be tied to Pin 1.
[2] AVSS = 0 V.

AC SPECIFICATIONS

f_S = 1 GHz, DAC R_{SET} = 10 kΩ, unless otherwise noted. Power supply pins within the range specified in the DC Specifications section.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FDBK_IN INPUT					Pin 40, Pin 41
Input Frequency Range	10		400	MHz	
Minimum Differential Input Level	225			mV p-p	−12 dBm into 50 Ω; must be ac-coupled
	40			V/µs	
SYSTEM CLOCK INPUT					Pin 27, Pin 28
SYSCLK PLL Bypassed					
Input Frequency Range	250		1000	MHz	Maximum f_{OUT} is 0.4 × f_{SYSCLK}
Duty Cycle	45		55	%	
Minimum Differential Input Level	632			mV p-p	Equivalent to 316 mV swing on each leg
SYSCLK PLL Enabled					
VCO Frequency Range, Low Band	700		810	MHz	When in the range, use the low VCO band exclusively
VCO Frequency Range, Auto Band	810		900	MHz	When in the range, use the VCO auto band select
VCO Frequency Range, High Band	900		1000	MHz	When in the range, use the high VCO band exclusively
Maximum Input Rate of System Clock PFD			200	MHz	
Without SYSCLK PLL Doubler					
Input Frequency Range	11		200	MHz	
Multiplication Range	4		66		Integer multiples of 2, maximum PFD rate and system clock frequency must be met
Minimum Differential Input Level	632			mV p-p	Equivalent to 316 mV swing on each leg
With SYSCLK PLL Doubler					
Input Frequency Range	6		100	MHz	
Multiplication Range	8		132		Integer multiples of 8
Input Duty Cycle		50		%	Deviating from 50% duty cycle may adversely affect spurious performance
Minimum Differential Input Level	632			mV p-p	Equivalent to 316 mV swing on each leg
Crystal Resonator with SYSCLK PLL Enabled					
Crystal Resonator Frequency Range	10		50	MHz	AT cut, fundamental mode resonator
Maximum Crystal Motional Resistance			100	Ω	See the SYSCLK Inputs section for recommendations
CLOCK DRIVERS					
HSTL Output Driver					
Frequency Range	20		725	MHz	See Figure 27 for maximum toggle rate
Duty Cycle	48		52	%	
Rise Time/Fall Time (20% to 80%)		115	165	ps	100 Ω termination across OUT/OUTB, 2 pF load
Jitter (12 kHz to 20 MHz)		1.5		ps	f_{OUT} = 155.52 MHz, 50 MHz system clock input (see Figure 12 through Figure 14 for test conditions)
HSTL Output Driver with 2× Multiplier					
Frequency Range	400		725	MHz	
Duty Cycle	45		55	%	
Rise Time/Fall Time (20% to 80%)		115	165	ps	100 Ω termination across OUT/OUTB, 2 pF load
Subharmonic Spur Level		−35		dBc	Without correction
Jitter (12 kHz to 20 MHz)		1.6		ps	f_{OUT} = 622.08 MHz, 50 MHz system clock input (see Figure 15 for test conditions)
CMOS Output Driver (AVDD3/Pin 37) @ 3.3 V					
Frequency Range	0.008		150	MHz	See Figure 29 for maximum toggle rate; the S-divider should be used for low frequencies because the FDBK_IN minimum frequency is 10 MHz
Duty Cycle	45	55	65	%	With 20 pF load and up to 150 MHz
Rise Time/Fall Time (20% to 80%)		3	4.6	ns	With 20 pF load

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CMOS Output Driver (AVDD3/Pin 37) @ 1.8 V					
Frequency Range	0.008		40	MHz	See Figure 28 for maximum toggle rate
Duty Cycle	45	55	65	%	With 20 pF load and up to 40 MHz
Rise Time/Fall Time (20% to 80%)		5	6.8	ns	With 20 pF load
DAC OUTPUT CHARACTERISTICS					
DCO Frequency Range (1st Nyquist Zone)	0		450	MHz	DAC lower limit is 0 Hz; however, the minimum slew rate for FDBK_IN dictates the lower limit if using CMOS or HSTL outputs
Output Resistance		50		Ω	Single-ended (each pin internally terminated to AVSS)
Output Capacitance		5		pF	
Full-Scale Output Current		20	31.7	mA	Range depends on DAC R_{SET} resistor
Gain Error	−10		+10	% FS	
Output Offset			0.6	µA	
Voltage Compliance Range	AVSS − 0.50	+0.5	AVSS + 0.50	V	Outputs connected to a transformer whose center tap is grounded
Wideband SFDR					See the Typical Performance Characteristics section
20.1 MHz Output		−79		dBc	0 MHz to 500 MHz
98.6 MHz Output		−67		dBc	0 MHz to 500 MHz
201.1 MHz Output		−61		dBc	0 MHz to 500 MHz
398.7 MHz Output		−59		dBc	0 MHz to 500 MHz
Narrow-Band SFDR					See the Typical Performance Characteristics section
20.1 MHz Output		−95		dBc	±250 kHz
98.6 MHz Output		−96		dBc	±250 kHz
201.1 MHz Output		−91		dBc	±250 kHz
398.7 MHz Output		−86		dBc	±250 kHz
DIGITAL TIMING SPECIFICATIONS					
Time Required to Enter Power-Down		15		µs	
Time Required to Leave Power-Down		18		µs	
Reset Assert to High-Z Time for S1 to S4 Configuration Pins		60		ns	Time from rising edge of RESET to high-Z on the S1, S2, S3, S4 configuration pins
SERIAL PORT TIMING SPECIFICATIONS					
SCLK Clock Rate ($1/t_{CLK}$)		25	50	MHz	Refer to Figure 56 for all write-related serial port parameters; maximum SCLK rate for readback is governed by t_{DV}
SCLK Pulse Width High, t_{HIGH}	8			ns	
SCLK Pulse Width Low, t_{LOW}	8			ns	
SDO/SDIO to SCLK Setup Time, t_{DS}	1.93			ns	
SDO/SDIO to SCLK Hold Time, t_{DH}	1.9			ns	
SCLK Falling Edge to Valid Data on SDIO/SDO, t_{DV}			11	ns	Refer to Figure 54
CSB to SCLK Setup Time, t_S	1.34			ns	
CSB to SCLK Hold Time, t_H	−0.4			ns	
CSB Minimum Pulse Width High, t_{PWH}	3			ns	
IO_UPDATE Pin Setup Time (from SCLK Rising Edge of the Final Bit)	t_{CLK}			sec	t_{CLK} = period of SCLK in Hz
IO_UPDATE Pin Hold Time	t_{CLK}			sec	t_{CLK} = period of SCLK in Hz
PROPAGATION DELAY					
FDBK_IN to HSTL Output Driver		2.8		ns	
FDBK_IN to HSTL Output Driver with 2× Frequency Multiplier Enabled		7.3		ns	
FDBK_IN to CMOS Output Driver		8.0		ns	S-divider bypassed
FDBK_IN Through S-Divider to CMOS Output Driver		8.6		ns	
Frequency Tuning Word Update: IO_UPDATE Pin Rising Edge to DAC Output		$60/f_S$		ns	f_S = system clock frequency in GHz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Analog Supply Voltage (AVDD)	2 V
Digital Supply Voltage (DVDD)	2 V
Digital I/O Supply Voltage (DVDD_I/O)	3.6 V
DAC Supply Voltage (AVDD3 Pins)	3.6 V
Maximum Digital Input Voltage	−0.5 V to DVDD_I/O + 0.5 V
Storage Temperature	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
64-Lead LFCSP	25.2	13.9	1.7	°C/W typical

Note that the exposed pad on the bottom of package must be soldered to ground to achieve the specified thermal performance. See the Typical Performance Characteristics section for more information.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

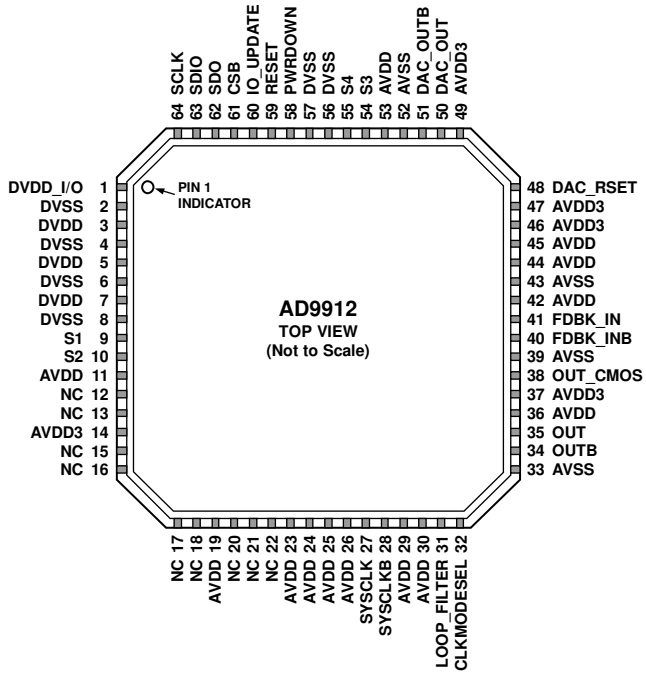

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
1	I	Power	DVDD_I/O	I/O Digital Supply.
2, 4, 6, 8	I	Power	DVSS	Digital Ground. Connect to ground.
3, 5, 7	I	Power	DVDD	Digital Supply.
9, 10, 54, 55	I/O	3.3 V CMOS	S1, S2, S3, S4	Start-Up Configuration Pins. These pins are configured under program control and do not have internal pull-up/pull-down resistors.
11, 19, 23 to 26, 29, 30, 36, 42, 44, 45, 53	I	Power	AVDD	Analog Supply. Connect to a nominal 1.8 V supply.
12, 13, 15, 16, 17, 18, 20, 21, 22			NC	No Connect. These unused pins can be left unconnected.
14, 46, 47, 49	I	Power	AVDD3	Analog Supply. Connect to a nominal 3.3 V supply.
27	I	Differential input	SYSCLK	System Clock Input. The system clock input has internal dc biasing and should always be ac-coupled, except when using a crystal. Single-ended 1.8 V CMOS can also be used, but it may introduce a spur caused by an input duty cycle that is not 50%. When using a crystal, tie the CLKMODESEL pin to AVSS, and connect crystal directly to this pin and Pin 28.
28	I	Differential input	SYSCLKB	Complementary System Clock. Complementary signal to the input provided on Pin 27. Use a 0.01 µF capacitor to ground on this pin if the signal provided on Pin 27 is single-ended.
31	O		LOOP_FILTER	System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter must be constructed and attached to this pin. This pin should be pulled down to ground with 1 kΩ resistor when the system clock PLL is bypassed. See Figure 46 for a diagram of the system clock PLL loop filter.

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
32	I	1.8 V CMOS	CLKMODESEL	Clock Mode Select. Set to GND when connecting a crystal to the system clock input (Pin 27 and Pin 28). Pull up to 1.8 V when using either an oscillator or an external clock source. This pin can be left unconnected when the system clock PLL is bypassed. (See the SYSCLK Inputs section for details on the use of this pin.)
33, 39, 43, 52	O	GND	AVSS	Analog Ground. Connect to ground.
34	O	1.8 V HSTL	OUTB	Complementary HSTL Output. See the Specifications and Primary 1.8 V Differential HSTL Driver sections for details.
35	O	1.8 V HSTL	OUT	HSTL Output. See the Specifications and Primary 1.8 V Differential HSTL Driver sections for details.
37	I	Power	AVDD3	Analog Supply for CMOS Output Driver. This pin is normally 3.3 V but can be 1.8 V. This pin should be powered even if the CMOS driver is not used. See the Power Supply Partitioning section for power supply partitioning.
38	O	3.3 V CMOS	OUT_CMOS	CMOS Output. See the Specifications section and the Output Clock Drivers and 2× Frequency Multiplier section. This pin is 1.8 V CMOS if Pin 37 is set to 1.8 V.
40	I	Differential input	FDBK_INB	Complementary Feedback Input. When using the HSTL and CMOS outputs, this pin is connected to the filtered DAC_OUTB output. This internally biased input is typically ac-coupled, and when configured as such, can accept any differential signal whose single-ended swing is at least 400 mV.
41	I	Differential input	FDBK_IN	Feedback Input. In standard operating mode, this pin is connected to the filtered DAC_OUT output.
48	O	Current set resistor	DAC_RSET	DAC Output Current Setting Resistor. Connect a resistor (usually 10 kΩ) from this pin to GND. See the Digital-To-Analog (DAC) Output section.
50	O	Differential output	DAC_OUT	DAC Output. This signal should be filtered and sent back on-chip through the FDBK_IN input. This pin has an internal 50 Ω pull-down resistor.
51	O	Differential output	DAC_OUTB	Complementary DAC Output. This signal should be filtered and sent back on-chip through the FDBK_INB input. This pin has an internal 50 Ω pull-down resistor.
56, 57		Power	DVSS	Digital Ground. Connect to ground.
58	I	3.3 V CMOS	PWRDOWN	Power-Down. When this active high pin is asserted, the device becomes inactive and enters the full power-down state. This pin has an internal 50 kΩ pull-down resistor.
59	I	3.3 V CMOS	RESET	Chip Reset. When this active high pin is asserted, the chip goes into reset. Note that on power-up, a 10 µs reset pulse is internally generated when the power supplies reach a threshold and stabilize. This pin should be grounded with a 10 kΩ resistor if not used.
60	I	3.3 V CMOS	IO_UPDATE	I/O Update. A logic transition from 0 to 1 on this pin transfers data from the I/O port registers to the control registers (see the Write section). This pin has an internal 50 kΩ pull-down resistor.
61	I	3.3 V CMOS	CSB	Chip Select. Active low. When programming a device, this pin must be held low. In systems where more than one AD9912 is present, this pin enables individual programming of each AD9912. This pin has an internal 100 kΩ pull-up resistor.
62	O	3.3 V CMOS	SDO	Serial Data Output. When the device is in 3-wire mode, data is read on this pin. There is no internal pull-up/pull-down resistor on this pin.
63	I/O	3.3 V CMOS	SDIO	Serial Data Input/Output. When the device is in 3-wire mode, data is written via this pin. In 2-wire mode, data reads and writes both occur on this pin. There is no internal pull-up/pull-down resistor on this pin.
64	I	3.3 V CMOS	SCLK	Serial Programming Clock. Data clock for serial programming. This pin has an internal 50 kΩ pull-down resistor.
Exposed Die Pad	O	GND	EPAD	Analog Ground. The exposed die pad on the bottom of the package provides the analog ground for the part; this exposed pad must be connected to ground for proper operation.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD, AVDD3, and DVDD at nominal supply voltage; DAC R_{SET} = 10 kΩ, unless otherwise noted. See Figure 26 for 1 GHz reference phase noise used for generating these plots.

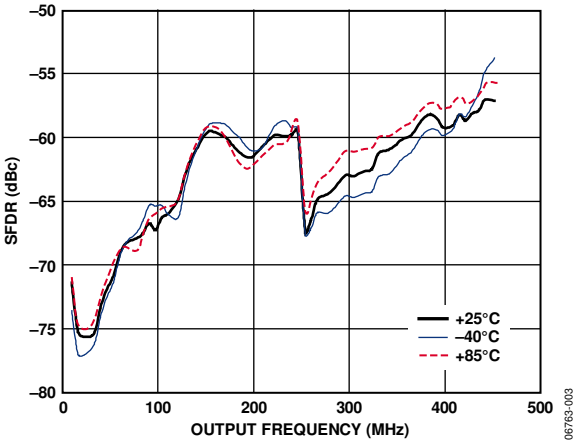

Figure 3. Wideband SFDR vs. Output Frequency at −40°C, +25°C, and +85°C, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

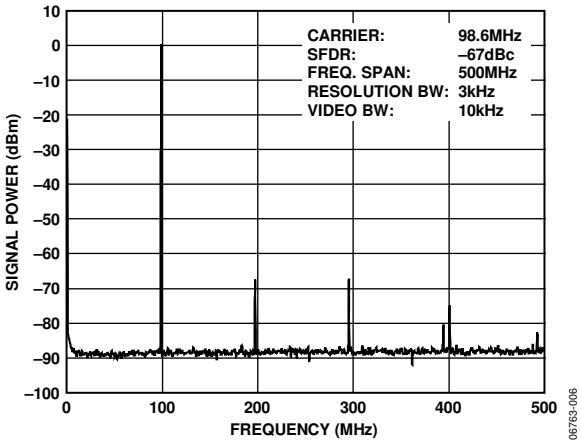

Figure 6. Wideband SFDR at 98.6 MHz, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

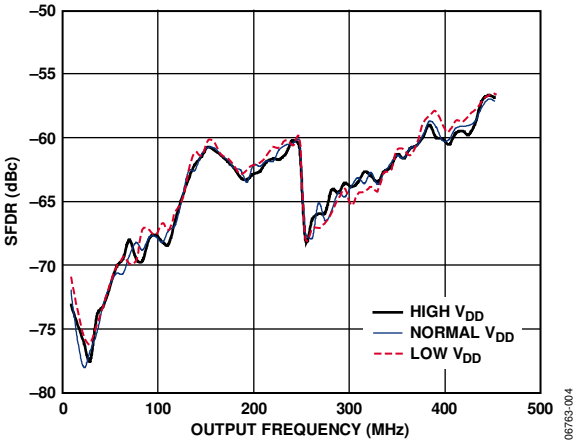

Figure 4. Variation of Wideband SFDR vs. Frequency over DAC Power Supply Voltage, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

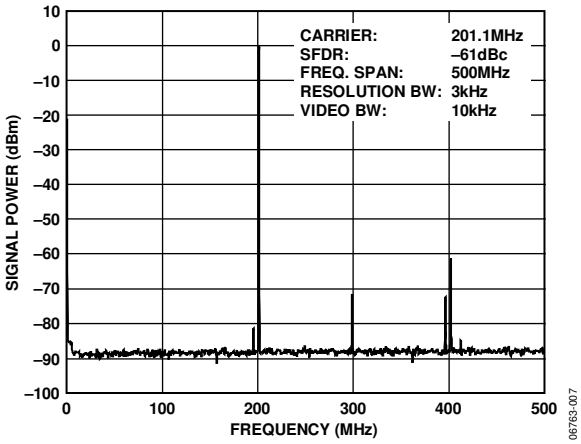

Figure 7. Wideband SFDR at 201.1 MHz, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

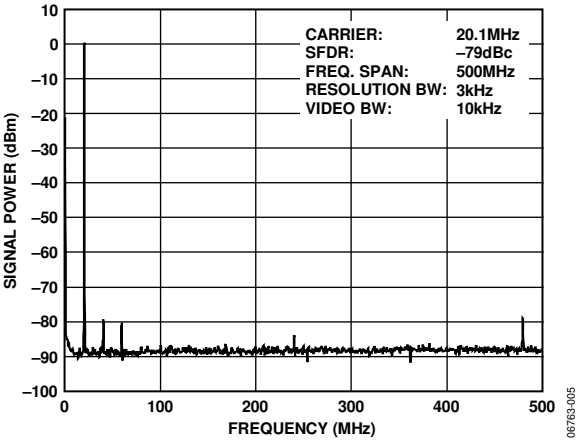

Figure 5. Wideband SFDR at 20.1 MHz, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

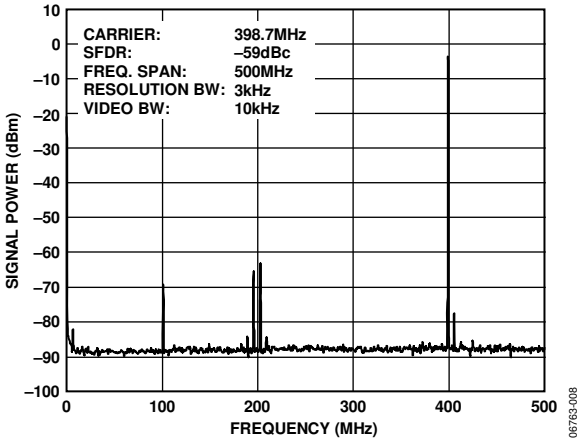

Figure 8. Wideband SFDR at 398.7 MHz, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

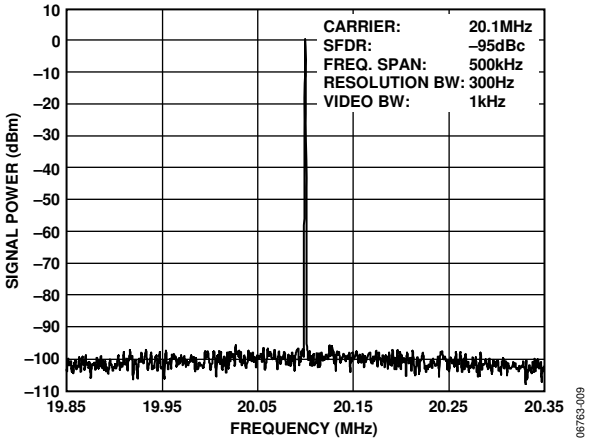

Figure 9. Narrow-Band SFDR at 20.1 MHz, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

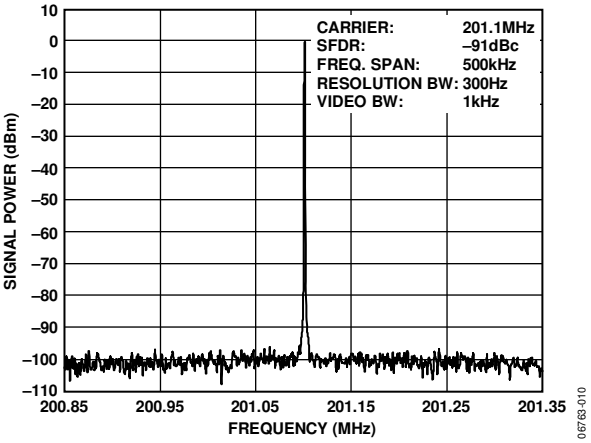

Figure 10. Narrow-Band SFDR at 201.1 MHz, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

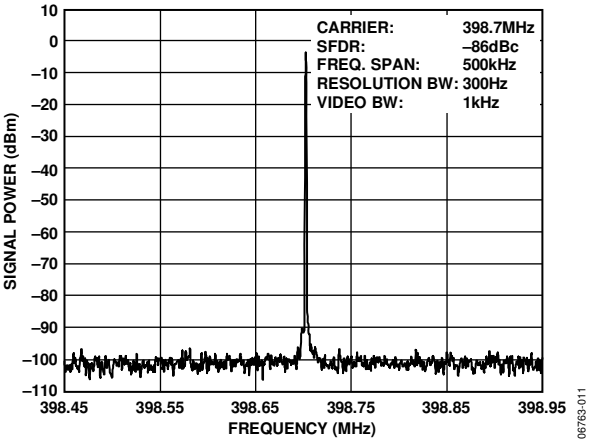

Figure 11. Narrow-Band SFDR at 398.7 MHz, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

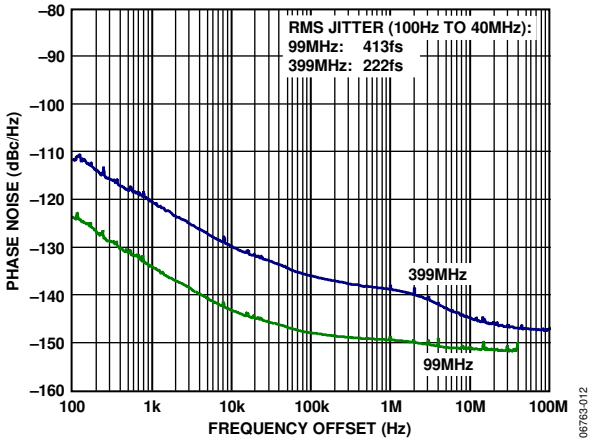

Figure 12. Absolute Phase Noise Using HSTL Driver, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

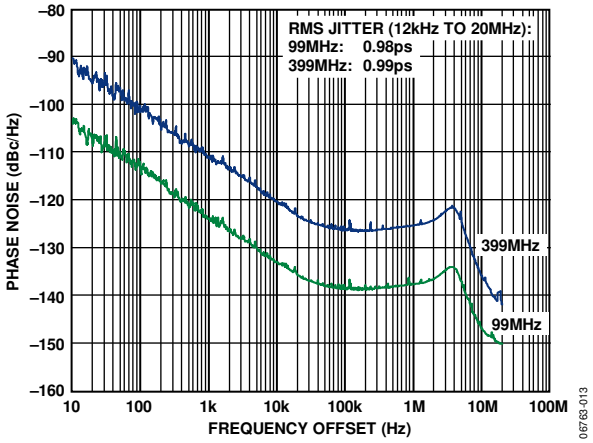

Figure 13. Absolute Phase Noise Using HSTL Driver, SYSCLK = 1 GHz (SYSCLK PLL Driven by Rohde & Schwarz SMA100 Signal Generator at 83.33 MHz)

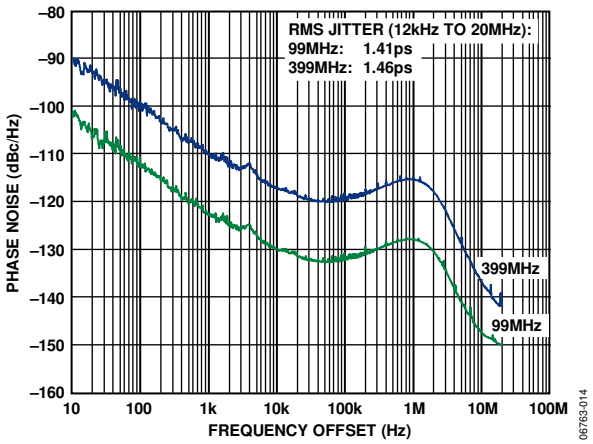

Figure 14. Absolute Phase Noise Using HSTL Driver, SYSCLK = 1 GHz (SYSCLK PLL Driven by Rohde & Schwarz SMA100 Signal Generator at 25 MHz)

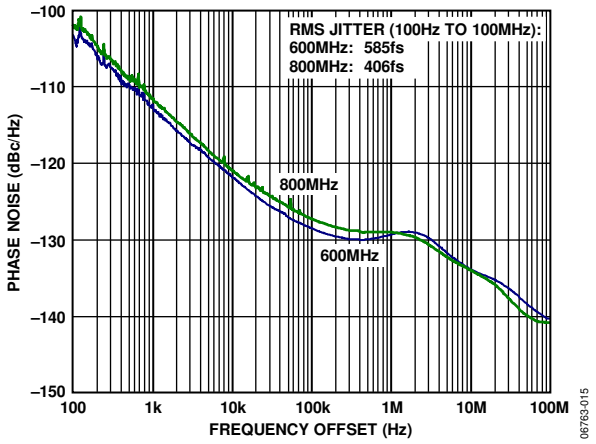

Figure 15. Absolute Phase Noise Using HSTL Driver, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed), HSTL Output Doubler Enabled

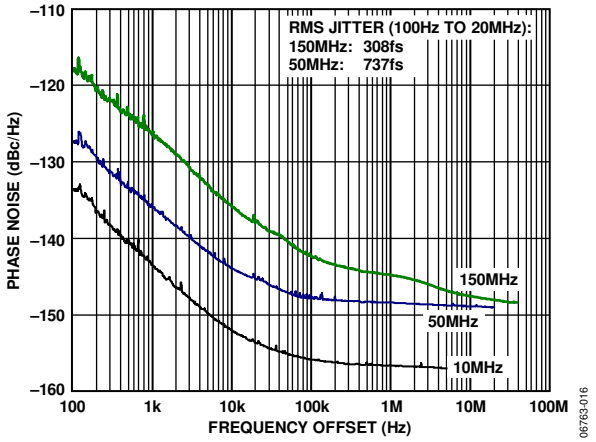

Figure 16. Absolute Phase Noise Using CMOS Driver at 3.3 V, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed) DDS Run at 200 MSPS for 10 MHz Plot

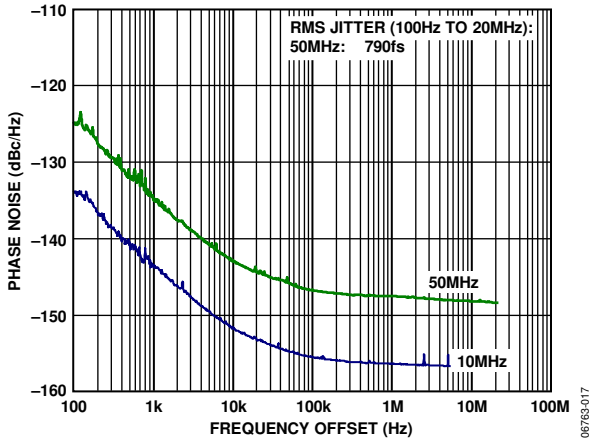

Figure 17. Absolute Phase Noise Using CMOS Driver at 1.8 V, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

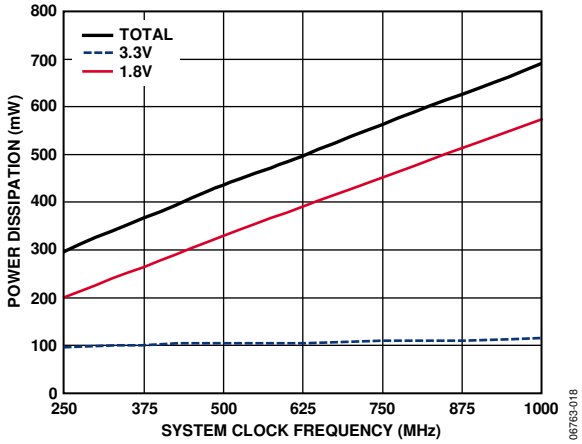

Figure 18. Power Dissipation vs. System Clock Frequency (SYSCLK PLL Bypassed), $f_{OUT} = f_{SYSCLK}/5$, HSTL Driver On, CMOS Driver On, SpurKiller Off

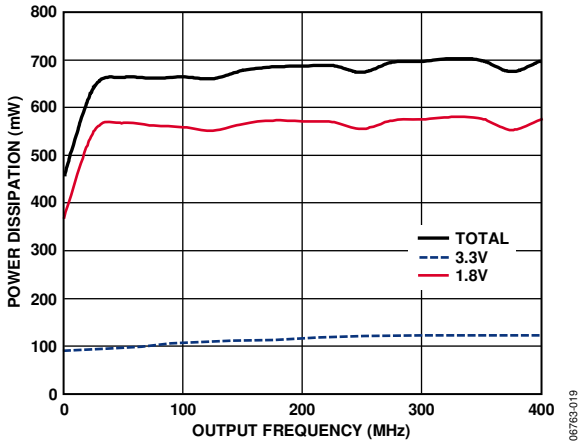

Figure 19. Power Dissipation vs. Output Frequency SYSCLK = 1 GHz (SYSCLK PLL Bypassed), HSTL Driver On, CMOS Driver On, SpurKiller Off

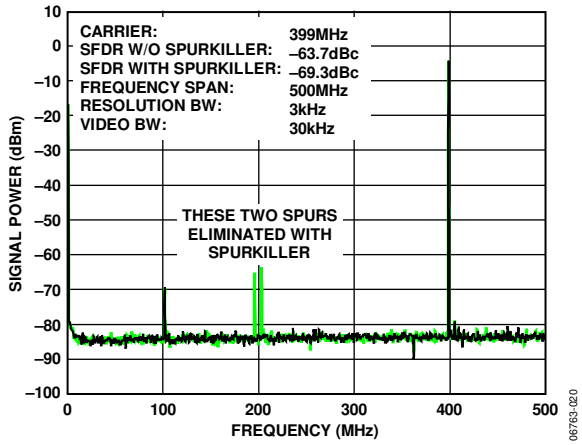

Figure 20. SFDR Comparison With and Without SpurKiller, SYSCLK = 1 GHz, f_{OUT} = 400 MHz

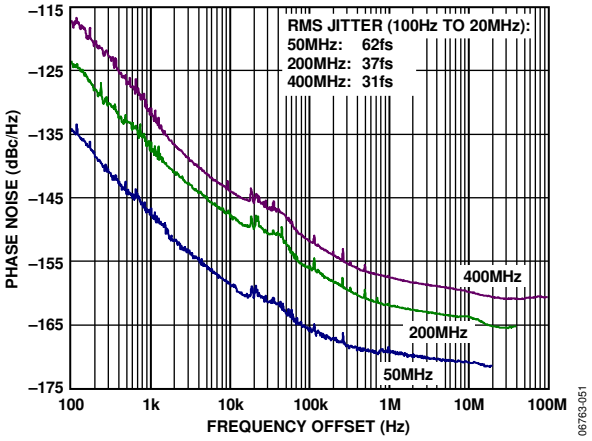

Figure 21. Absolute Phase Noise of Unfiltered DAC Output, f_{OUT} = 50 MHz, 200 MHz, and 400 MHz, SYSCLK Driven by a 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

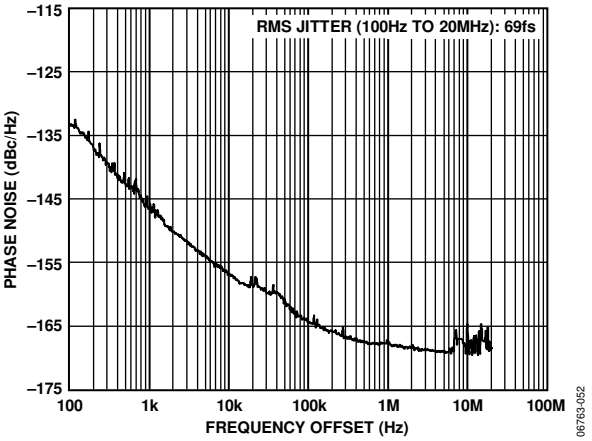

Figure 22. Absolute Phase Noise of Unfiltered DAC Output, f_{OUT} = 63 MHz, SYSCLK Driven by a 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

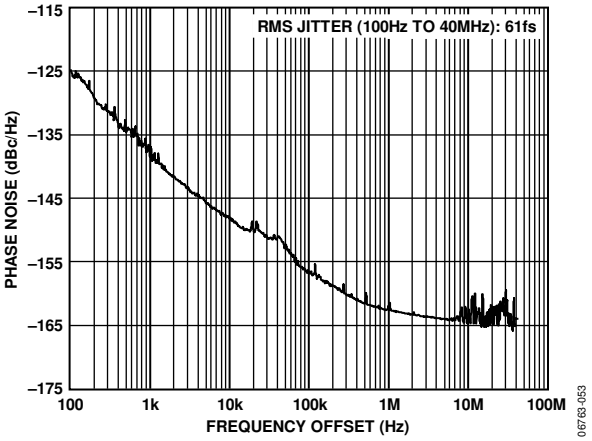

Figure 23. Absolute Phase Noise of Unfiltered DAC Output, f_{OUT} = 171 MHz, SYSCLK Driven by a 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

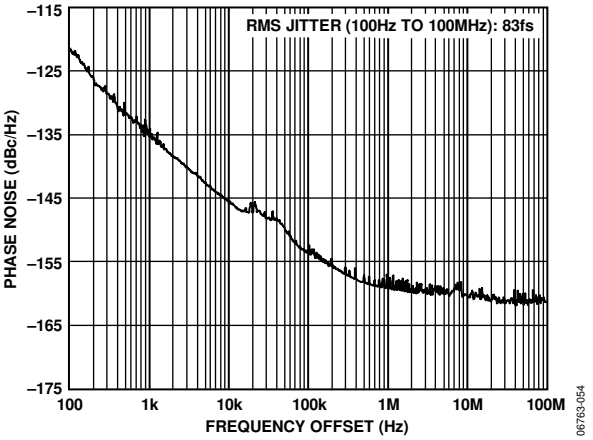

Figure 24. Absolute Phase Noise of Unfiltered DAC Output, f_{OUT} = 258.3 MHz, SYSCLK Driven by a 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

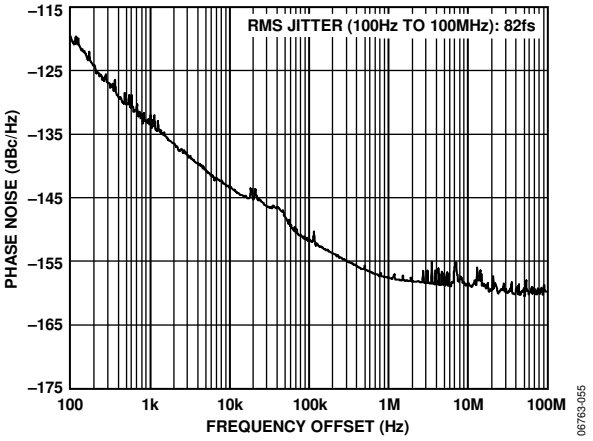

Figure 25. Absolute Phase Noise of Unfiltered DAC Output, f_{OUT} = 311.6 MHz, SYSCLK Driven by a 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

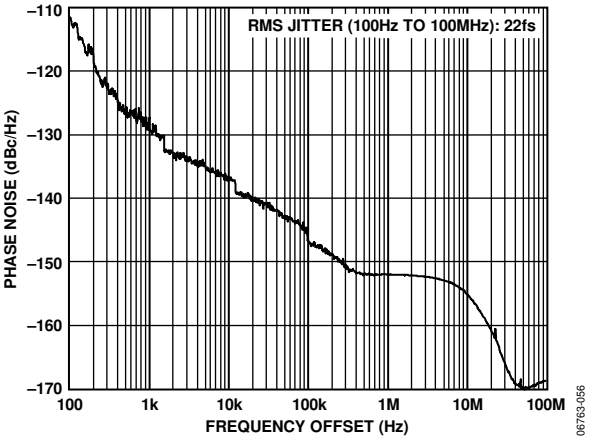

Figure 26. Absolute Phase Noise of 1 GHz Reference Used for Performance Plots; Wenzel Components Used: 100 MHz Oscillator, LNBA-13-24 Amp, LNOM 100-5 Multiplier, LNDD 500-14 Diode Doubler

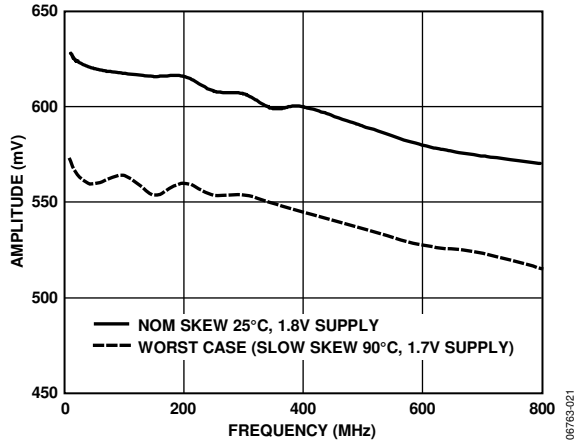

Figure 27. HSTL Output Driver Single-Ended Peak-to-Peak Amplitude vs. Toggle Rate (100 Ω Across Differential Pair)

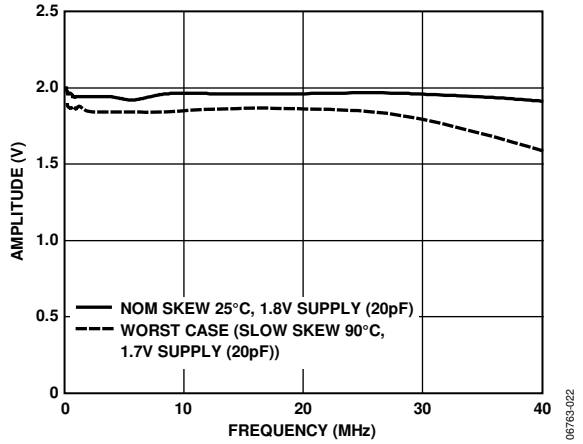

Figure 28. CMOS Output Driver Peak-to-Peak Amplitude vs. Toggle Rate (AVDD3 = 1.8 V) with 20 pF Load

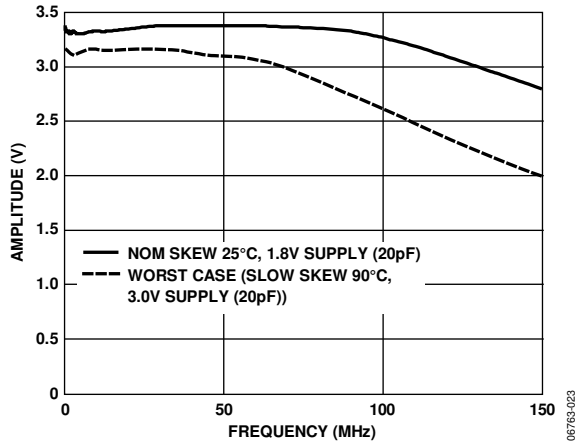

Figure 29. CMOS Output Driver Peak-to-Peak Amplitude vs. Toggle Rate (AVDD3 = 3.3 V) with 20 pF Load

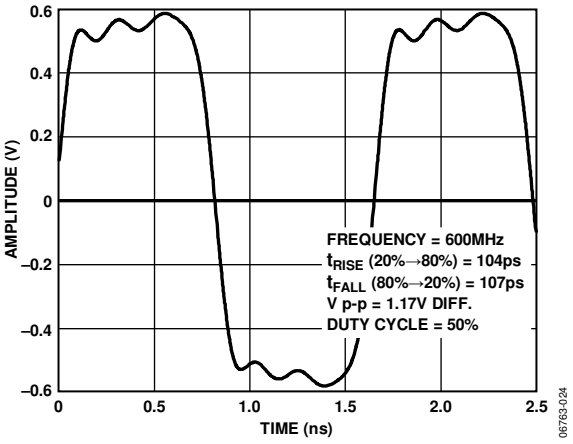

Figure 30. Typical HSTL Output Waveform, Nominal Conditions, DC-Coupled, Differential Probe Across 100 Ω load

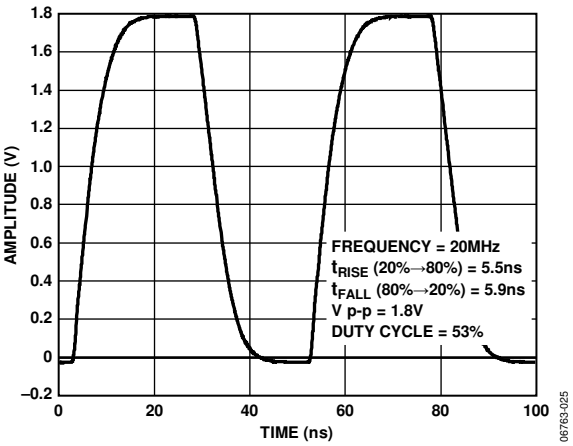

Figure 31. Typical CMOS Output Driver Waveform (@ 1.8 V), Nominal Conditions, Estimated Capacitance = 5 pF

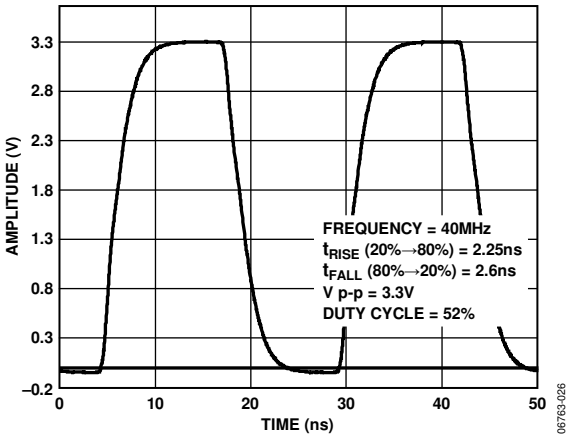

Figure 32. CMOS Output Driver Waveform (@ 3.3 V), Nominal Conditions, Estimated Capacitance = 5 pF

INPUT/OUTPUT TERMINATION RECOMMENDATIONS

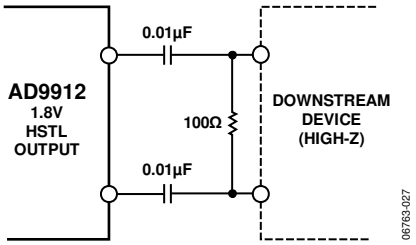

Figure 33. AC-Coupled HSTL Output Driver

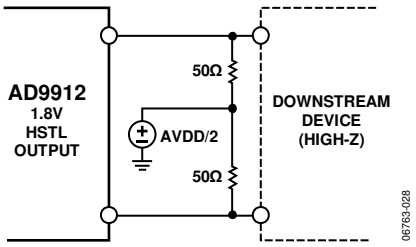

Figure 34. DC-Coupled HSTL Output Driver

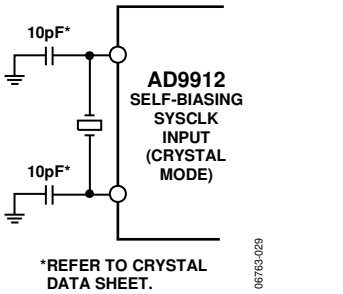

Figure 35. SYSCLK Input, Xtal

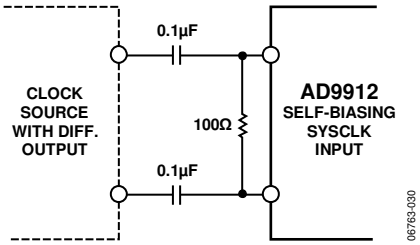

Figure 36. SYSCLK Differential Input, Non-Xtal

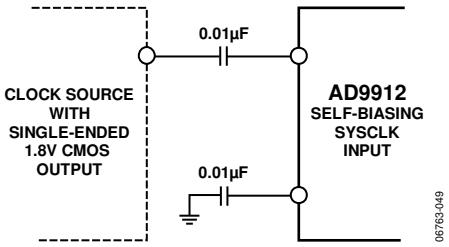

Figure 37. SYSCLK Single-Ended Input, Non-Xtal

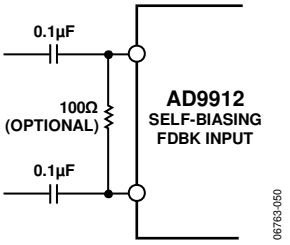

Figure 38. FDBK_IN Input

THEORY OF OPERATION

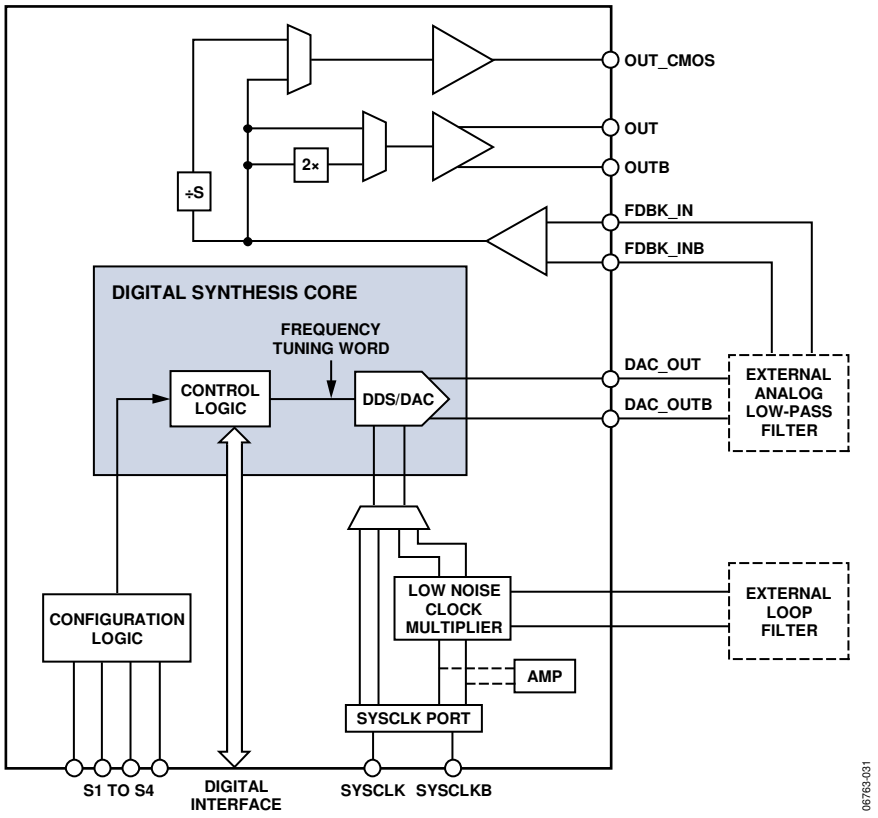

Figure 39. Detailed Block Diagram

OVERVIEW

The AD9912 is a high performance, low noise, 14-bit DDS clock synthesizer with integrated comparators for applications desiring an agile, finely tuned square or sinusoidal output signal. A digitally controlled oscillator (DCO) is implemented using a direct digital synthesizer (DDS) with an integrated output DAC, clocked by the system clock.

A bypassable PLL-based frequency multiplier is present, enabling use of an inexpensive, low frequency source for the system clock. For best jitter performance, the system clock PLL should be bypassed, and a low noise, high frequency system clock should be provided directly. Sampling theory sets an upper bound for the DDS output frequency at 50% of f_S (where f_S is the DAC sample rate), but a practical limitation of 40% of f_S is generally recommended to allow for the selectivity of the required off-chip reconstruction filter.

The output signal from the reconstruction filter can be fed back to the AD9912 to be processed through the output circuitry.

The output circuitry includes HSTL and CMOS output buffers, as well as a frequency doubler for applications that need frequencies above the Nyquist level of the DDS.

The AD9912 also offers preprogrammed frequency profiles that allow the user to generate frequencies without programming the part. The individual functional blocks are described in the following sections.

DIRECT DIGITAL SYNTHESIZER (DDS)

The frequency of the sinusoid generated by the DDS is determined by a frequency tuning word (FTW), which is a digital (that is, numeric) value. Unlike an analog sinusoidal generator, a DDS uses digital building blocks and operates as a sampled system. Thus, it requires a sampling clock (f_S) that serves as the fundamental timing source of the DDS. The accumulator behaves as a modulo-2^{48} counter with a programmable step size that is determined by the frequency tuning word (FTW). A block diagram of the DDS is shown in Figure 40.

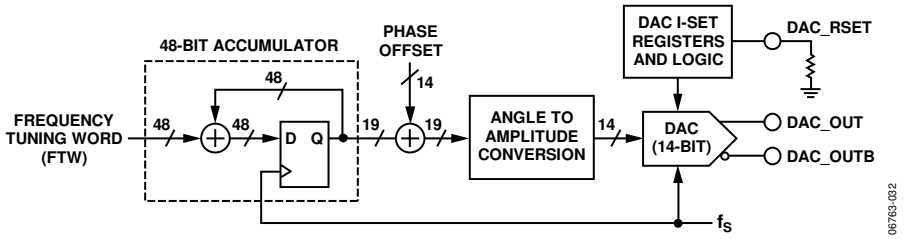

Figure 40. DDS Block Diagram

The input to the DDS is a 48-bit FTW that provides the accumulator with a seed value. On each cycle of f_S, the accumulator adds the value of the FTW to the running total of its output. For example, given an FTW = 5, the accumulator increments the count by 5 sec on each f_S cycle. Over time, the accumulator reaches the upper end of its capacity (2^{48} in this case) and then rolls over, retaining the excess. The average rate at which the accumulator rolls over establishes the frequency of the output sinusoid. The following equation defines the average rollover rate of the accumulator and establishes the output frequency (f_{DDS}) of the DDS:

$$f_{DDS} = \left(\frac{FTW}{2^{48}}\right) f_S$$

Solving this equation for FTW yields

$$FTW = \text{round}\left[2^{48}\left(\frac{f_{DDS}}{f_S}\right)\right]$$

For example, given that f_S = 1 GHz and f_{DDS} = 19.44 MHz, then FTW = 5,471,873,547,255 (0x04FA05143BF7).

The relative phase of the sinusoid can be controlled numerically, as well. This is accomplished using the phase offset function of the DDS (a programmable 14-bit value (Δphase); see the I/O Register Map section). The resulting phase offset, ΔΦ (radians), is given by

$$\Delta\Phi = 2\pi\left(\frac{\Delta phase}{2^{14}}\right)$$

DIGITAL-TO-ANALOG (DAC) OUTPUT

The output of the digital core of the DDS is a time series of numbers representing a sinusoidal waveform. This series is translated to an analog signal by means of a digital-to-analog converter (DAC).

The DAC outputs its signal to two pins driven by a balanced current source architecture (see the DAC output diagram in Figure 41). The peak output current derives from a combination of two factors. The first is a reference current (I_{DAC_REF}) that is established at the DAC_RSET pin, and the second is a scale factor that is programmed into the I/O register map.

The value of I_{DAC_REF} is set by connecting a resistor (R_{DAC_REF}) between the DAC_RSET pin and ground. The DAC_RSET pin is internally connected to a virtual voltage reference of 1.2 V nominal, so the reference current can be calculated by

$$I_{DAC\_REF} = \frac{1.2}{R_{DAC\_REF}}$$

Note that the recommended value of I_{DAC_REF} is 120 μA, which leads to a recommended value for R_{DAC_REF} of 10 kΩ.

The scale factor consists of a 10-bit binary number (FSC) programmed into the DAC full-scale current register in the I/O register map. The full-scale DAC output current (I_{DAC_FS}) is given by

$$I_{DAC\_FS} = I_{DAC\_REF}\left(72 + \frac{192FSC}{1024}\right)$$

Using the recommended value of R_{DAC_REF}, the full-scale DAC output current can be set with 10-bit granularity over a range of approximately 8.6 mA to 31.7 mA. 20 mA is the default value.

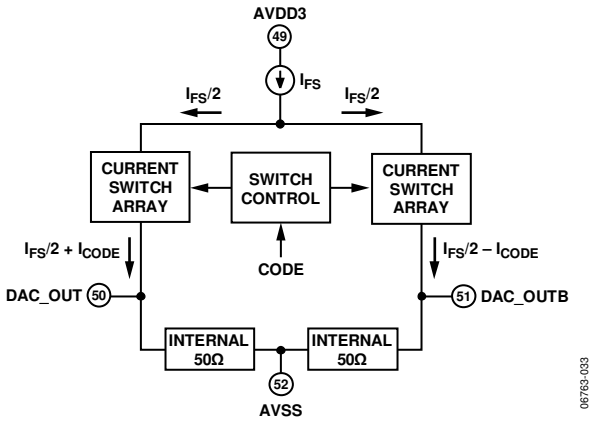

Figure 41. DAC Output

RECONSTRUCTION FILTER

The origin of the output clock signal produced by the AD9912 is the combined DDS and DAC. The DAC output signal appears as a sinusoid sampled at f_S. The frequency of the sinusoid is determined by the frequency tuning word (FTW) that appears at the input to the DDS. The DAC output is typically passed through an external reconstruction filter that serves to remove the artifacts of the sampling process and other spurs outside the filter bandwidth. If desired, the signal can then be brought back on-chip to be converted to a square wave that is routed internally to the output clock driver or the 2× DLL multiplier.

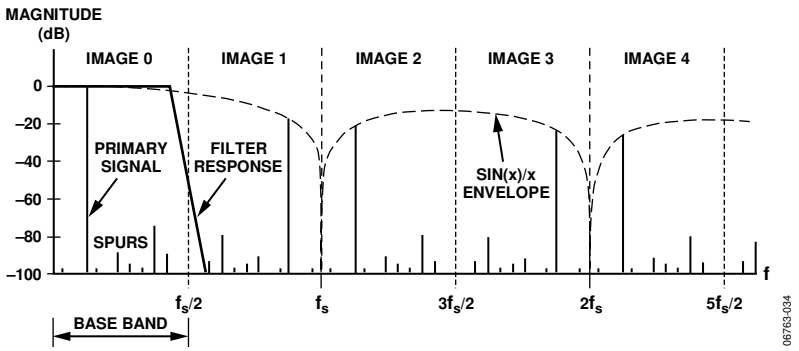

Figure 42. DAC Spectrum vs. Reconstruction Filter Response

Because the DAC constitutes a sampled system, its output must be filtered so that the analog waveform accurately represents the digital samples supplied to the DAC input. The unfiltered DAC output contains the (typically) desired baseband signal, which extends from dc to the Nyquist frequency ($f_S/2$). It also contains images of the baseband signal that theoretically extend to infinity. Notice that the odd images (shown in Figure 42) are mirror images of the baseband signal. Furthermore, the entire DAC output spectrum is affected by a sin(x)/x response, which is caused by the sample-and-hold nature of the DAC output signal.

For applications using the fundamental frequency of the DAC output, the response of the reconstruction filter should preserve the baseband signal (Image 0), while completely rejecting all other images. However, a practical filter implementation typically exhibits a relatively flat pass band that covers the desired output frequency plus 20%, rolls off as steeply as possible, and then maintains significant (though not complete) rejection of the remaining images. Depending on how close unwanted spurs are to the desired signal, a third-, fifth-, or seventh-order elliptic low-pass filter is common.

Some applications operate off an image above the Nyquist frequency, and those applications use a band-pass filter instead of a low-pass filter.

The design of the reconstruction filter has a significant impact on the overall signal performance. Therefore, good filter design and implementation techniques are important for obtaining the best possible jitter results.

FDBK_IN INPUTS

The FDBK_IN pins serve as the input to the comparators and output drivers of the AD9912. Typically, these pins are used to receive the signal generated by the DDS after it has been band-limited by the external reconstruction filter.

A diagram of the FDBK_IN input pins is provided in Figure 43, which includes some of the internal components used to bias the input circuitry. Note that the FDBK_IN input pins are internally biased to a dc level of ~1 V. Care should be taken to ensure that any external connections do not disturb the dc bias because this may significantly degrade performance.

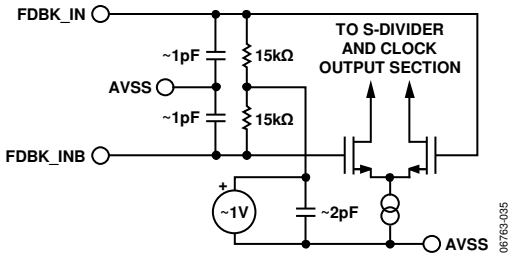

Figure 43. Differential FDBK_IN Inputs

SYSCLK INPUTS

Functional Description

An external time base connects to the AD9912 at the SYSCLK pins to generate the internal high frequency system clock (f_S).

The SYSCLK inputs can be operated in one of the following three modes:

- SYSCLK PLL bypassed
- SYSCLK PLL enabled with input signal generated externally
- Crystal resonator with SYSCLK PLL enabled

A functional diagram of the system clock generator is shown in Figure 44.

The SYSCLK PLL multiplier path is enabled by a Logic 0 (default) in the PD SYSCLK PLL bit (Register 0x0010, Bit 4) of the I/O register map. The SYSCLK PLL multiplier can be driven from the SYSCLK input pins by one of two means, depending on the logic level applied to the 1.8 V CMOS CLKMODESEL pin. When CLKMODESEL = 0, a crystal can be connected directly across the SYSCLK pins. When CLKMODESEL = 1, the maintaining amp is disabled, and an external frequency source (such as an oscillator or signal generator) can be connected directly to the SYSCLK input pins. Note that CLKMODESEL = 1 does not disable the system clock PLL.

The maintaining amp on the AD9912 SYSCLK pins is intended for 25 MHz, 3.2 mm × 2.5 mm AT cut fundamental mode crystals with a maximum motional resistance of 100 Ω. The following crystals, listed in alphabetical order, meet these criteria (as of the revision date of this data sheet):

- AVX/Kyocera CX3225SB
- ECS ECX-32
- Epson/Toyocom TSX-3225
- Fox FX3225BS
- NDK NX3225SA

Note that although these crystals meet the preceding criteria according to their data sheets, Analog Devices, Inc., does not guarantee their operation with the AD9912, nor does Analog Devices endorse one supplier of crystals over another.

When the SYSCLK PLL multiplier path is disabled, the AD9912 must be driven by a high frequency signal source (250 MHz to 1 GHz). The signal thus applied to the SYSCLK input pins becomes the internal DAC sampling clock (f_S) after passing through an internal buffer.

It is important to note that when bypassing the system clock PLL, the LOOP_FILTER pin (Pin 31) should be pulled down to the analog ground with a 1 kΩ resistor.

SYSCLK PLL Doubler

The SYSCLK PLL multiplier path offers an optional SYSCLK PLL doubler. This block comes before the SYSCLK PLL multiplier and acts as a frequency doubler by generating a pulse on each edge of the SYSCLK input signal. The SYSCLK PLL multiplier locks to the falling edges of this regenerated signal.

The impetus for doubling the frequency at the input of the SYSCLK PLL multiplier is that an improvement in overall phase noise performance can be realized. The main drawback is that the doubler output is not a rectangular pulse with a constant duty cycle even for a perfectly symmetric SYSCLK input signal. This results in a subharmonic appearing at the same frequency as the SYSCLK input signal, and the magnitude of the subharmonic can be quite large. When employing the doubler, care must be taken to ensure that the loop bandwidth of the SYSCLK PLL multiplier adequately suppresses the subharmonic.

The benefit offered by the doubler depends on the magnitude of the subharmonic, the loop bandwidth of the SYSCLK PLL multiplier, and the overall phase noise requirements of the specific application. In many applications, the AD9912 clock output is applied to the input of another PLL, and the subharmonic is often suppressed by the relatively narrow bandwidth of the downstream PLL.

Note that generally, the benefits of the SYSCLK PLL doubler are realized for SYSCLK input frequencies of 25 MHz and above.

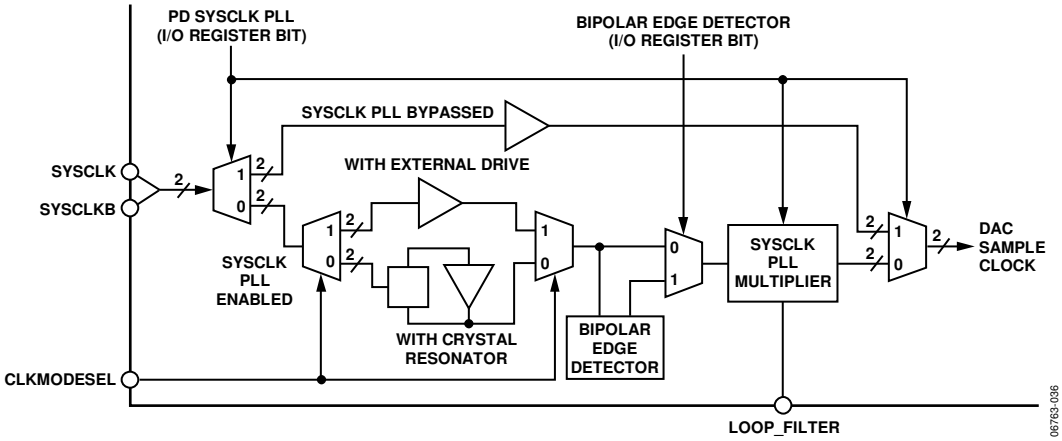

Figure 44. System Clock Generator Block Diagram

SYSCLK PLL Multiplier

When the SYSCLK PLL multiplier path is employed, the frequency applied to the SYSCLK input pins must be limited so as not to exceed the maximum input frequency of the SYSCLK PLL phase detector. A block diagram of the SYSCLK generator appears in Figure 45.

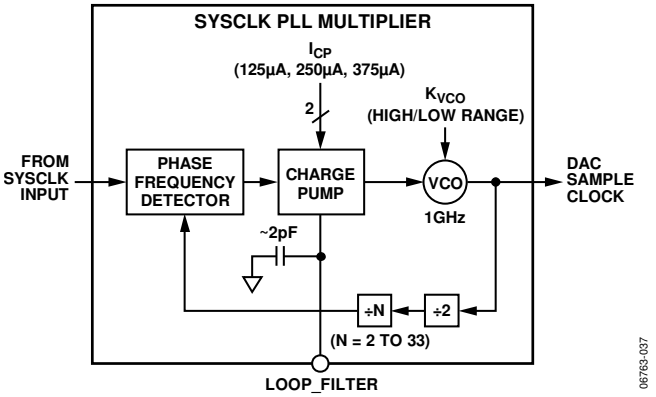

Figure 45. Block Diagram of the SYSCLK PLL

The SYSCLK PLL multiplier has a 1 GHz VCO at its core. A phase/frequency detector (PFD) and charge pump provide the steering signal to the VCO in typical PLL fashion. The PFD operates on the falling edge transitions of the input signal, which means that the loop locks on the negative edges of the reference signal. The charge pump gain is controlled via the I/O register map by selecting one of three possible constant current sources ranging from 125 µA to 375 µA in 125 µA steps. The center frequency of the VCO is also adjustable via the I/O register map and provides high/low gain selection. The feedback path from VCO to PFD consists of a fixed divide-by-2 prescaler followed by a programmable divide-by-N block, where $2 \leq N \leq 33$. This limits the overall divider range to any even integer from 4 to 66, inclusive. The value of N is programmed via the I/O register map via a 5-bit word that spans a range of 0 to 31, but the internal logic automatically adds a bias of 2 to the value entered, extending the range to 33. Care should be taken when choosing these values so as not to exceed the maximum input frequency of the SYSCLK PLL phase detector or SYSCLK PLL doubler. These values can be found in the AC Specifications section.

External Loop Filter (SYSCLK PLL)

The loop bandwidth of the SYSCLK PLL multiplier can be adjusted by means of three external components as shown in Figure 46. The nominal gain of the VCO is 800 MHz/V. The recommended component values (shown in Table 6) establish a loop bandwidth of approximately 1.6 MHz with the charge pump current set to 250 µA. The default case is N = 40, and it assumes a 25 MHz SYSCLK input frequency and generates an internal DAC sampling frequency (f_S) of 1 GHz.

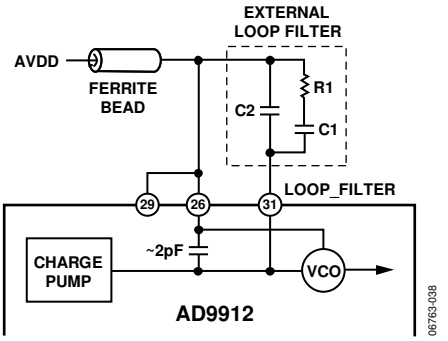

Figure 46. External Loop Filter for SYSCLK PLL

Table 6. Recommended Loop Filter Values for a Nominal 1.5 MHz SYSCLK PLL Loop Bandwidth

Multiplier	R1	Series C1	Shunt C2
<8	390 Ω	1 nF	82 pF
10	470 Ω	820 pF	56 pF
20	1 kΩ	390 pF	27 pF
40 (default)	2.2 kΩ	180 pF	10 pF
60	2.7 kΩ	120 pF	5 pF

Detail of SYSCLK Differential Inputs

A diagram of the SYSCLK input pins is provided in Figure 47. Included are details of the internal components used to bias the input circuitry. These components have a direct effect on the static levels at the SYSCLK input pins. This information is intended to aid in determining how best to interface to the device for a given application.

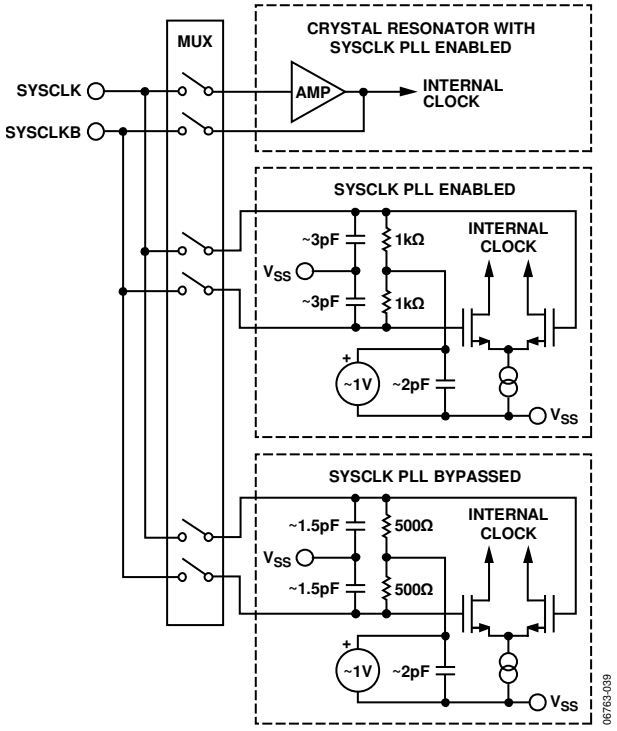

Figure 47. Differential SYSCLK Inputs

Note that the SYSCLK PLL bypassed and SYSCLK PLL enabled input paths are internally biased to a dc level of ~1 V. Care should be taken to ensure that any external connections do not disturb the dc bias because this may significantly degrade performance. Generally, it is recommended that the SYSCLK inputs be ac-coupled, except when using a crystal resonator.

OUTPUT CLOCK DRIVERS AND 2× FREQUENCY MULTIPLIER

There are two output drivers provided by the AD9912. The primary output driver supports differential 1.8 V HSTL output levels, while the secondary supports either 1.8 V or 3.3 V CMOS levels, depending on whether Pin 37 is driven at 1.8 V or 3.3 V.

The primary differential driver nominally provides an output voltage with 100 Ω load applied differentially. The source impedance of the driver is approximately 100 Ω for most of the output clock period; during transition between levels, the source impedance reaches a maximum of about 500 Ω. The driver is designed to support output frequencies of up to and beyond the OC-12 network rate of 622.08 MHz.

The output clock can also be powered down by a control bit in the I/O register map.

Primary 1.8 V Differential HSTL Driver

The DDS produces a sinusoidal clock signal that is sampled at the system clock rate. This DDS output signal is routed off chip where it is passed through an analog filter and brought back on chip for buffering and, if necessary, frequency doubling. Where possible, for the best jitter performance, it is recommended that the frequency doubler be bypassed.

The 1.8 V HSTL output should be ac-coupled, with 100 Ω termination at the destination. The driver design has low jitter injection for frequencies in the range of 50 MHz to 750 MHz. Refer to the AC Specifications section for the exact frequency limits.

2× Frequency Multiplier

The AD9912 can be configured (via the I/O register map) with an internal 2× delay-locked loop (DLL) multiplier at the input of the primary clock driver. The extra octave of frequency gain allows the AD9912 to provide output clock frequencies that exceed the range available from the DDS alone. These settings are found in Register 0x0010 and Register 0x0200.

The input to the DLL consists of the filtered DDS output signal after it has been squared up by an integrated clock receiver circuit. The DLL can accept input frequencies in the range of 200 MHz to 400 MHz.

Single-Ended CMOS Output

In addition to the high-speed differential output clock driver, the AD9912 provides an independent, single-ended output, CMOS clock driver that is very good for frequencies up to 150 MHz. The signal path for the CMOS clock driver can either include or bypass the CMOS output divider.

If the CMOS output divider is bypassed, the HSTL and CMOS drivers are the same frequency as the signal presented at the FDBK_IN pins. When using the CMOS output in this configuration, the DDS output frequency should be in the range of 30 MHz to 150 MHz. At low output frequencies (<30 MHz), the low slew rate of the DAC results in a higher noise floor. This can be remedied by running the DDS at 100 MHz or greater and using the CMOS divider. At an output frequency of 50 MHz, the best technique depends on the user's application. Running the DDS at 200 MHz, and using a CMOS divider of 4, results in a lower noise floor, but at the expense of close-in phase noise.

At frequencies greater than 150 MHz, the HSTL output should be used.

CMOS Output Divider (S-Divider)

The CMOS output divider is 16 bits cascaded with an additional divide-by-two. The divider is therefore capable of integer division from 1 to 65,535 (index of 1) or from 2 to 131,070 (index of 2). The divider is programmed via the I/O register map to trigger on either the rising (default) or falling edge of the feedback signal.

The CMOS output divider is an integer divider capable of handling frequencies well above the Nyquist limit of the DDS. The S-divider/2 bit (Register 0x0106, Bit 0) must be set when FDBK_IN is greater than 400 MHz.

Note that the actual output divider values equal the value stored in the output divider register minus one. Therefore, to have an output divider of one, the user writes zeros to the output divider register.

HARMONIC SPUR REDUCTION

The most significant spurious signals produced by the DDS are harmonically related to the desired output frequency of the DDS. The source of these harmonic spurs can usually be traced to the DAC, and the spur level is in the −60 dBc range. This ratio represents a level that is about 10 bits below the full-scale output of the DAC (10 bits down is 2^{-10}, or 1/1024).

Such a spur can be reduced by combining the original signal with a replica of the spur, but offset in phase by 180°. This idea is the foundation of the technique used to reduce harmonic spurs in the AD9912. Because the DAC has 14-bit resolution, a −60 dBc spur can be synthesized using only the lower 4 bits of the DAC full-scale range. That is, the 4 LSBs can create an output level that is approximately 60 dB below the full-scale level of the DAC (commensurate with a −60 dBc spur). This fact gives rise to a means of digitally reducing harmonic spurs or their aliased images in the DAC output spectrum by digitally adding a sinusoid at the input of the DAC with a similar magnitude as the offending spur, but shifted in phase to produce destructive interference.