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## FEATURES

- 50 mW at up to 250 MSPS internal clock speed**
- 100 MHz analog output**
- Integrated 10-bit DAC**
- 0.058 Hz or better frequency resolution**
- 0.022° phase tuning resolution**
- Programmable modulus in frequency equation**
- Phase noise  $\leq -135$  dBc per Hz @ 1 kHz offset (DAC output)**  
( $<115$  dBc per Hz when using on-board PLL multiplier)
- Excellent dynamic performance**  
 **$>80$  dB SFDR @ 100 MHz ( $\pm 100$  kHz offset)  $A_{OUT}$**
- Automatic linear frequency sweeping capability**
- 8 frequency or phase offset profiles**
- 1.8 V power supply**
- Software and hardware controlled power-down**
- Parallel and serial programming options**
- 32-lead LFCSP package**
- Optional PLL REF\_CLK multiplier**
- Internal oscillator (can be driven by a single crystal)**
- Phase modulation capability**

## APPLICATIONS

- Portable and handheld equipment**
- Agile LO frequency synthesis**
- Programmable clock generator**
- FM chirp source for radar and scanning systems**

## GENERAL DESCRIPTION

The AD9913 is a complete direct digital synthesizer (DDS) designed to meet the stringent power consumption limits of portable, handheld, and battery-powered equipment. The AD9913 features a 10-bit digital-to-analog converter (DAC) operating up to 250 MSPS. The AD9913 uses advanced DDS technology, coupled with an internal high speed, high performance DAC to form a complete, digitally-programmable, high frequency synthesizer capable of generating a frequency agile analog output sinusoidal waveform at up to 100 MHz.

The AD9913 provides fast frequency hopping and fine tuning resolution. The AD9913 also offers fine resolution phase offset control. Control words are loaded into the AD9913 through the serial or parallel I/O port. The AD9913 also supports a user-defined linear sweep mode of operation for generating highly linearized swept waveforms of frequency. To support various methods of generating a system clock, the AD9913 includes an oscillator, allowing a simple crystal to be used as the frequency reference, as well as a high speed clock multiplier to convert the reference clock frequency up to the full system clock rate. For power saving considerations, many of the individual blocks of the AD9913 can be powered down when not in use.

The AD9913 operates over the extended industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

## FUNCTIONAL BLOCK DIAGRAM

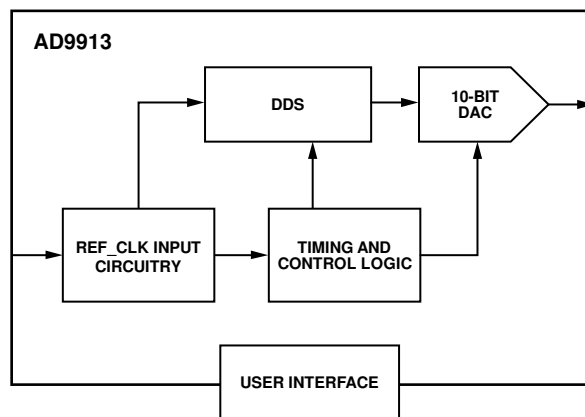


Figure 1.

# AD9913\* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

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## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- AD9913 Evaluation Board

## DOCUMENTATION

### Application Notes

- AN-1389: Recommended Rework Procedure for the Lead Frame Chip Scale Package (LFCSP)
  - AN-237: Choosing DACs for Direct Digital Synthesis
  - AN-280: Mixed Signal Circuit Technologies
  - AN-342: Analog Signal-Handling for High Speed and Accuracy
  - AN-345: Grounding for Low-and-High-Frequency Circuits
  - AN-419: A Discrete, Low Phase Noise, 125 MHz Crystal Oscillator for the AD9850
  - AN-423: Amplitude Modulation of the AD9850 Direct Digital Synthesizer
  - AN-543: High Quality, All-Digital RF Frequency Modulation Generation with the ADSP-2181 and the AD9850 DDS
  - AN-557: An Experimenter's Project:
  - AN-587: Synchronizing Multiple AD9850/AD9851 DDS-Based Synthesizers
  - AN-605: Synchronizing Multiple AD9852 DDS-Based Synthesizers
  - AN-621: Programming the AD9832/AD9835
  - AN-632: Provisionary Data Rates Using the AD9951 DDS as an Agile Reference Clock for the ADN2812 Continuous-Rate CDR
  - AN-769: Generating Multiple Clock Outputs from the AD9540
  - AN-772: A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)
  - AN-823: Direct Digital Synthesizers in Clocking Applications Time
  - AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
  - AN-843: Measuring a Loudspeaker Impedance Profile Using the AD5933
  - AN-847: Measuring a Grounded Impedance Profile Using the AD5933
  - AN-851: A WiMax Double Downconversion IF Sampling Receiver Design
  - AN-927: Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)
-

- 
- AN-939: Super-Nyquist Operation of the AD9912 Yields a High RF Output Signal
  - AN-953: Direct Digital Synthesis (DDS) with a Programmable Modulus

#### Data Sheet

- AD9913: Low Power 250 MSPS 10-Bit DAC 1.8 V CMOS Direct Digital Synthesizer Data Sheet

#### Product Highlight

- Introducing Digital Up/Down Converters: VersaCOMM™ Reconfigurable Digital Converters

#### Technical Books

- A Technical Tutorial on Digital Signal Synthesis, 1999

## TOOLS AND SIMULATIONS

- AD9913 IBIS Model

## REFERENCE DESIGNS

- CN0109

## REFERENCE MATERIALS

### Product Selection Guide

- RF Source Booklet

### Solutions Bulletins & Brochures

- Test & Instrumentation Solutions Bulletin, Volume 10, Issue 3

### Technical Articles

- 400-MSample DDSs Run On Only +1.8 VDC
- ADI Buys Korean Mobile TV Chip Maker
- Basics of Designing a Digital Radio Receiver (Radio 101)
- DDS Applications
- DDS Circuit Generates Precise PWM Waveforms
- DDS Design
- DDS Device Produces Sawtooth Waveform
- DDS Device Provides Amplitude Modulation
- DDS IC Initiates Synchronized Signals
- DDS IC Plus Frequency-To-Voltage Converter Make Low-Cost DAC
- DDS Simplifies Polar Modulation
- Digital Potentiometers Vary Amplitude In DDS Devices
- Digital Up/Down Converters: VersaCOMM™ White Paper
- Digital Waveform Generator Provides Flexible Frequency Tuning for Sensor Measurement
- Improved DDS Devices Enable Advanced Comm Systems
- Integrated DDS Chip Takes Steps To 2.7 GHz
- Simple Circuit Controls Stepper Motors
- Speedy A/Ds Demand Stable Clocks
- Synchronized Synthesizers Aid Multichannel Systems
- The Year of the Waveform Generator
- Two DDS ICs Implement Amplitude-shift Keying
- Video Portables and Cameras Get HDMI Outputs

## DESIGN RESOURCES

- AD9913 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all AD9913 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

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**TECHNICAL SUPPORT** 

Submit a technical question or find your regional support number.

**DOCUMENT FEEDBACK** 

Submit feedback for this data sheet.

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## REVISION HISTORY

### 8/2016—Rev. A to Rev. B

Changes to Table 7.....	20
Updated Outline Dimensions .....	32
Changes to Ordering Guide .....	32

### 6/2010—Rev. 0 to Rev. A

Added Digital Input Voltage to Table 2 .....	5
Added Exposed Pad Notation to Figure 3 and Table 3.....	5
Changes to Programmable Modulus Mode Section .....	14
Changes to Serial Programming Section.....	22

Changes to Data Write Operation Section.....	24
Added Register Update (I/O Update) section and Figure 35 ...	25
Added Endnote 1 to Table 9.....	26
Changes to Register Bit Descriptions Section and Bit 7 Description in Table 10.....	28
Changes to Table 15 and Table 16 .....	31
Added Exposed Pad Notation to Outline Dimensions .....	32

### 10/2007—Revision 0: Initial Version

## SPECIFICATIONS

### ELECTRICAL SPECIFICATIONS

AVDD (1.8 V), DVDD (1.8 V), and DVDD\_I/O = 1.8 V  $\pm$  5%, T = 25°C, R<sub>SET</sub> = 4.64 k $\Omega$ , DAC full-scale current = 2 mA, external reference clock frequency = 250 MHz with REF\_CLK multiplier disabled, unless otherwise noted.

Table 1.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
<b>REF_CLK INPUT CHARACTERISTICS</b>					
Frequency Range					
REF_CLK Multiplier	Disabled			250	MHz
	Enabled			250	MHz
REF_CLK Input Divider Frequency	Full temperature range			83	MHz
VCO Oscillation Frequency	VCO1	16		250	MHz
	VCO2	100		250	MHz
PLL Lock Time	25 MHz reference clock, 10 $\times$ PLL		60		$\mu$ s
External Crystal Mode			25		MHz
CMOS Mode	V <sub>IH</sub>	0.9			V
	V <sub>IL</sub>			0.65	V
Input Capacitance			3		pF
Input Impedance (Differential)			2.7		k $\Omega$
Input Impedance (Single-Ended)			1.35		k $\Omega$
Duty Cycle		45		55	%
REF_CLK Input Level		355		1000	mV p-p
<b>DAC OUTPUT CHARACTERISTICS</b>					
Full-Scale Output Current				4.6	mA
Gain Error		-14		-6	%FS
Output Offset				+0.1	$\mu$ A
Differential Nonlinearity		-0.4		+0.4	LSB
Integral Nonlinearity		-0.5		+0.5	LSB
AC Voltage Compliance Range			$\pm$ 400		mV
<b>SPURIOUS-FREE DYNAMIC RANGE</b>					
	Refer to Figure 6				
<b>SERIAL PORT TIMING CHARACTERISTICS</b>					
SCLK Frequency				32	MHz
SCLK Pulse Width	Low	17.5			ns
	High	3.5			ns
SCLK Rise/Fall Time			2		ns
Data Setup Time to SCLK		5.5			ns
Data Hold Time to SCLK		0			ns
Data Valid Time in Read Mode			22		ns
<b>PARALLEL PORT TIMING CHARACTERISTICS</b>					
PCLK Frequency				33	MHz
PCLK Pulse Width	Low	10			ns
	High	20			ns
PCLK Rise/Fall Time			2		ns
Address/Data Setup Time to PCLK		3.0			ns
Address/Data Hold Time to PCLK		0.3			ns
Data Valid Time in Read Mode			8		ns
<b>IO_UPDATE/PROFILE(2:0) TIMING</b>					
Setup Time to SYNC_CLK		0.5			ns
Hold Time to SYNC_CLK		1			SYNC_CLK cycles

Parameter	Conditions/Comments	Min	Typ	Max	Unit
<b>MISCELLANEOUS TIMING CHARACTERISTICS</b>					
Wake-Up Time <sup>1</sup>					
Fast Recovery Mode				1	SYSCCLK cycles <sup>2</sup>
Full Sleep Mode				60	μs
Reset Pulse Width High		5			SYSCCLK cycles
<b>DATA LATENCY (PIPELINE DELAY)</b>					
Frequency, Phase-to-DAC Output	Matched latency enabled		11		SYSCCLK cycles
Frequency-to-DAC Output	Matched latency disabled		11		SYSCCLK cycles
Phase-to-DAC Output	Matched latency disabled		10		SYSCCLK cycles
Delta Tuning Word-to-DAC Output (Linear Sweep)			14		SYSCCLK cycles
<b>CMOS LOGIC INPUTS</b>					
Logic 1 Voltage		1.2			V
Logic 0 Voltage				0.4	V
Logic 1 Current		-700		+700	nA
Logic 0 Current		-700		+700	nA
Input Capacitance			3		pF
<b>CMOS LOGIC OUTPUTS</b>					
	1 mA load				
Logic 1 Voltage		1.5			V
Logic 0 Voltage				0.125	V
<b>POWER SUPPLY CURRENT</b>					
DVDD (1.8 V) Pin Current Consumption				46.5	mA
DAC_CLK_AVDD (1.8 V)				4.7	mA
DAC_AVDD (1.8 V) Pin Current Consumption				6.2	mA
PLL_AVDD (1.8 V)				1.8	mA
CLK_AVDD (1.8 V) Pin Current Consumption				4.3	mA
<b>POWER CONSUMPTION</b>					
Single Tone Mode	PLL enabled, CMOS input		50	66.5	mW
	PLL disabled, differential input		57	70.5	mW
	PLL enabled, XTAL input		52	68.5	mW
Modulus Mode	PLL disabled			94.6	mW
Linear Sweep Mode	PLL disabled			98.4	mW
Power-Down					
Full				15	mW
Safe	PLL enabled			44.8	mW
PLL Modes					
VCO 1					
Differential Input Mode				11	mW
CMOS Input Mode				7.5	mW
Crystal Mode				5.4	mW
VCO 2					
Differential Input Mode				15	mW
CMOS Input Mode				11.5	mW
Crystal Mode				9.4	mW

<sup>1</sup> Refer to the Power-Down Features section.

<sup>2</sup> SYSCCLK cycle refers to the actual clock frequency used on-chip by the DDS. If the reference clock multiplier is used to multiply the external reference clock frequency, the SYSCCLK frequency is the external frequency multiplied by the reference clock multiplication factor. If the reference clock multiplier and divider are not used, the SYSCCLK frequency is the same as the external reference clock frequency.



## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Maximum Junction Temperature	150°C
AVDD, DVDD	2 V
Digital Input Voltage	-0.7 V to +2.2 V
Digital Output Current	5 mA
Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +105°C
Lead Temperature (Soldering, 10 sec)	300°C
$\theta_{JA}$	36.1°C/W
$\theta_{JC}$	4.2°C/W

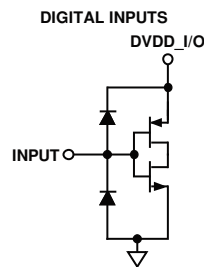
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION

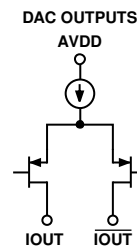


**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## EQUIVALENT CIRCUITS



AVOID OVERDRIVING DIGITAL INPUTS. FORWARD BIASING ESD DIODES MAY COUPLE DIGITAL NOISE ONTO POWER PINS.

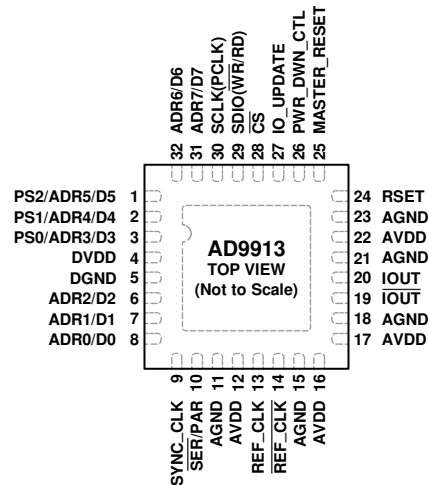


MUST TERMINATE OUTPUTS TO AGND FOR CURRENT FLOW. DO NOT EXCEED THE OUTPUT VOLTAGE COMPLIANCE RATING.

07002-010

Figure 2. Equivalent Input and Output Circuits

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



## NOTES

1. EXPOSED PAD SHOULD BE SOLDERED TO GROUND.

07002-003

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	I/O	Description
1	PS2/ADR5/D5	I/O	Multipurpose pin: Profile Select Pin (PS2) in Direct Switch Mode, Parallel Port Address Line (ADR5), and Data Line (D5) to program registers.
2	PS1/ADR4/D4	I/O	Multipurpose pin: Profile Select Pin (PS1) in Direct Switch Mode or Linear Sweeping Mode, Parallel Port Address Line (ADR4), and Data Line (D4) to program registers.
3	PS0/ADR3/D3	I/O	Multipurpose pin: Profile Select Pin (PS0) in Direct Switch Mode or Linear Sweeping Mode, Parallel Port Address Line (ADR3), and Data Line (D3) to program registers.
4	DVDD	I	Digital Power Supply (1.8 V).
5	DGND	I	Digital Ground.
6	ADR2/D2	I/O	Parallel Port Address Line 2 and Data Line 2.
7	ADR1/D1	I/O	Parallel Port Address Line 1 and Data Line 1.
8	ADR0/D0	I/O	Parallel Port Address Line 0 and Data Line 0.
9	SYNC_CLK	O	Clock Out. The profile pins [PS0:PS2] and the IO_UPDATE pin (Pin 27) should be set up to the rising edge of this signal to maintain constant pipe line delay through the device.
10	SER/PAR	I	Serial Port and Parallel Port Selection. Logic low = serial mode; logic high = parallel mode.
11, 15, 18, 21, 23	AGND	I	Analog Ground.
12, 16, 17, 22	AVDD	I	Analog Power Supply (1.8 V).
13	REF_CLK	I	Reference Clock Input. See the REF_CLK Overview section for more details.
14	REF_CLK	I	Complementary Reference Clock Input. See the REF_CLK Overview section for more details.
19	IOUT	O	Open Source DAC Complementary Output Source. Current mode. Connect through 50 $\Omega$ to AGND.
20	IOUT	O	Open Source DAC Output Source. Current mode. Connect through 50 $\Omega$ to AGND.
24	RSET	I	Analog Reference. This pin programs the DAC output full-scale reference current. Attach a 4.64 k $\Omega$ resistor to AGND.
25	MASTER_RESET	I	Master Reset, Digital Input (Active High). This pin clears all memory elements and reprograms registers to default values.

Pin No.	Mnemonic	I/O	Description
26	PWR_DWN_CTL	I	External Power-Down, Digital Input (Active High). A high level on this pin initiates the currently programmed power-down mode. See the Power-Down Features section for further details. If unused, tie to ground.
27	IO_UPDATE	I	I/O Update; Digital Input. A high on this pin indicates a transfer of the contents of the I/O buffers to the corresponding internal registers.
28	$\overline{\text{CS}}$	I	Chip Select for Serial and Parallel Port. Digital input (active low). Bringing this pin low enables the AD9913 to detect serial (SCLK) or parallel (PCLK) clock rising/falling edges. Bringing this pin high causes the AD9913 to ignore input on the data pins.
29	SDIO( $\overline{\text{WR}}$ /RD)	I/O	Bidirectional Data Line for Serial Port Operation and Write/Read Enable for Parallel Port Operation.
30	SCLK/PCLK	I	Input Clock for Serial and Parallel Port.
31	ADR7/D7	I/O	Parallel Port Address Line 7 and Data Line 7.
32	ADR6/D6	I/O	Parallel Port Address Line 6 and Data Line 6.
33	Exposed Paddle		The EPAD should be soldered to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

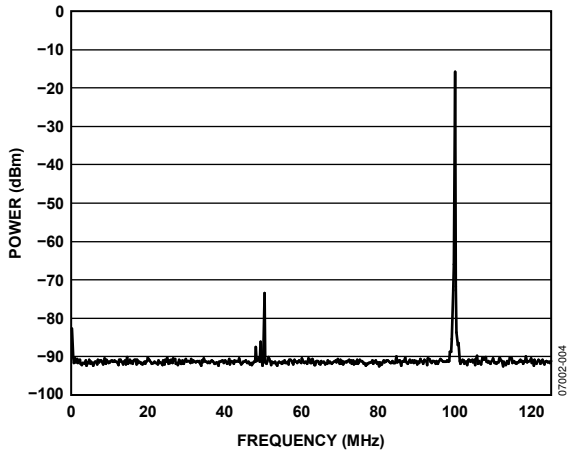


Figure 4. Wideband SFDR @ 99.76 MHz  $f_{OUT}$   
(250 MHz Clock, 4 mA DAC Full-Scale Current, PLL Bypassed)

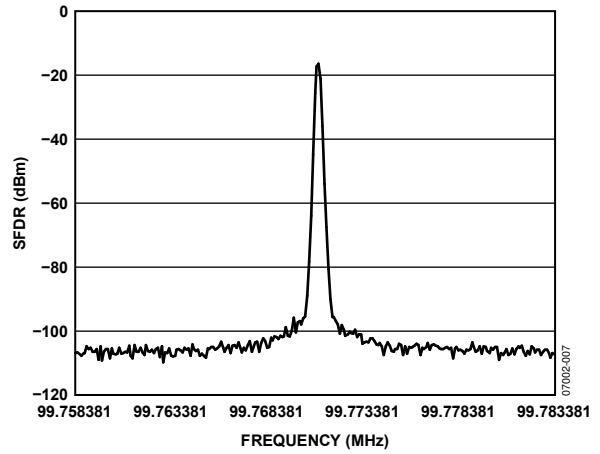


Figure 7. Narrow-Band SFDR @ 99.76 MHz  $f_{OUT}$   
(250 MHz Clock, 4 mA DAC Full-Scale Current, PLL Bypassed)

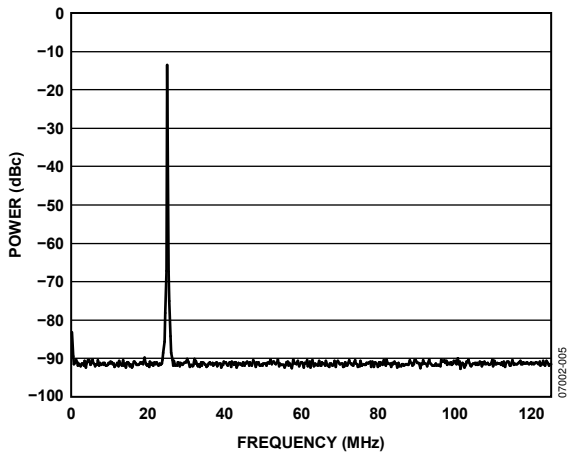


Figure 5. Wideband SFDR @ 25.14 MHz  $f_{OUT}$   
(250 MHz Clock, 4 mA DAC Full-Scale Current, PLL Bypassed)

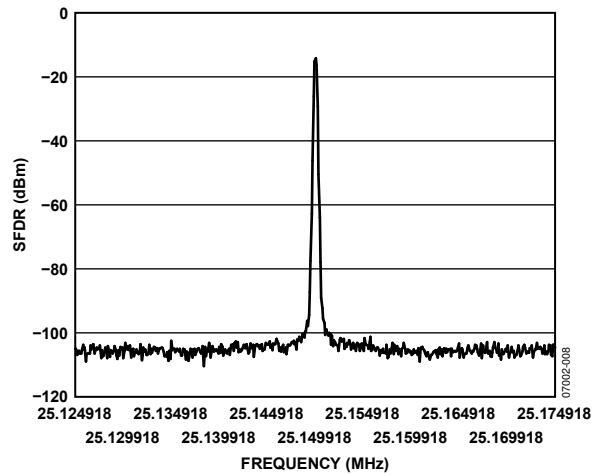


Figure 8. Narrow-Band SFDR @ 25.14 MHz  $f_{OUT}$   
(250 MHz Clock, 4 mA DAC Full-Scale Current, PLL Bypassed)

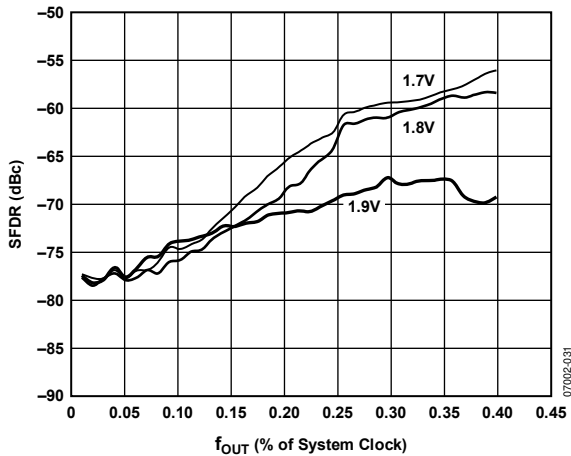


Figure 6. SFDR vs. Supply Variation  
(250 MHz Clock, 4 mA DAC Full-Scale Current, PLL Bypassed)

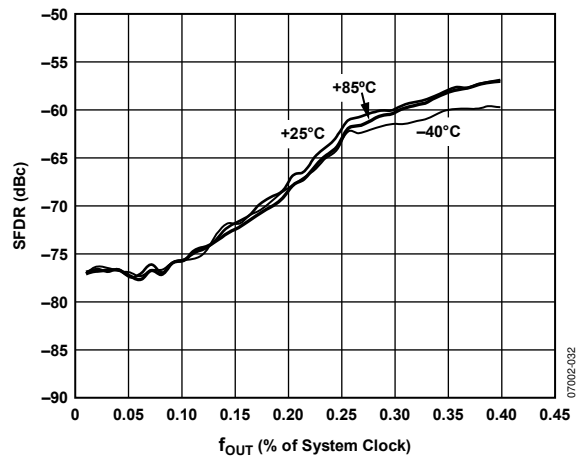


Figure 9. SFDR vs. Temperature  
(250 MHz Clock, 4 mA DAC Full-Scale Current, PLL Bypassed)

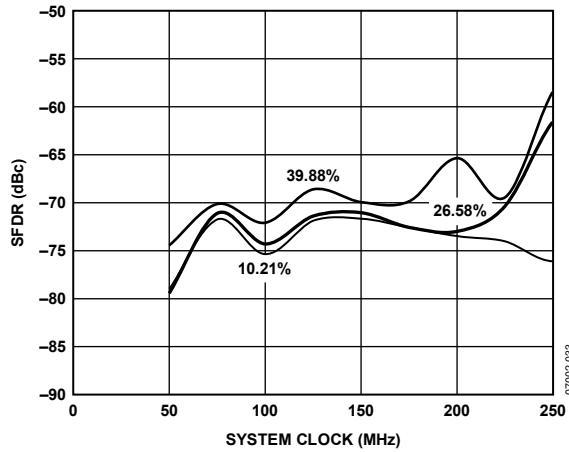


Figure 10. SFDR vs. System Clock Frequency (PLL Bypassed)

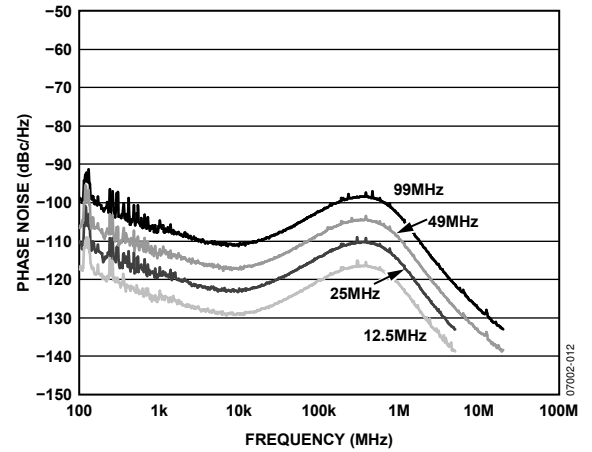


Figure 12. Absolute Phase Noise vs.  $f_{OUT}$  Using the Internal PLL (REF\_CLK 25 MHz  $\times$  10 = 250 MHz Using PLL)

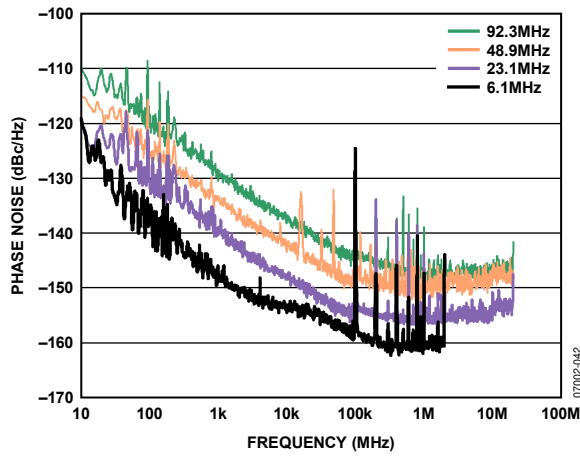


Figure 11. Residual Phase Noise vs.  $f_{OUT}$  (PLL Bypassed)

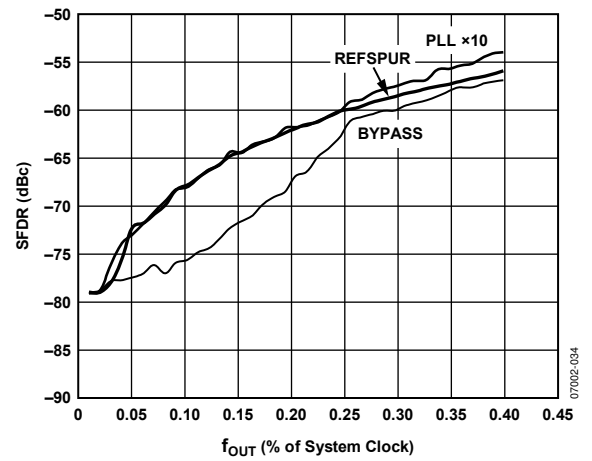


Figure 13. SFDR Without the Internal PLL (REF\_CLK = 25 MHz  $\times$  10 = 250 MHz Using PLL, 4 mA DAC Full-Scale Current)

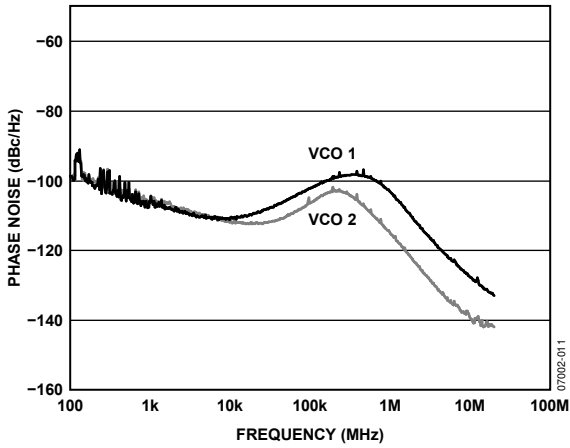


Figure 14. Absolute Phase Noise, VCO1 vs. VCO2

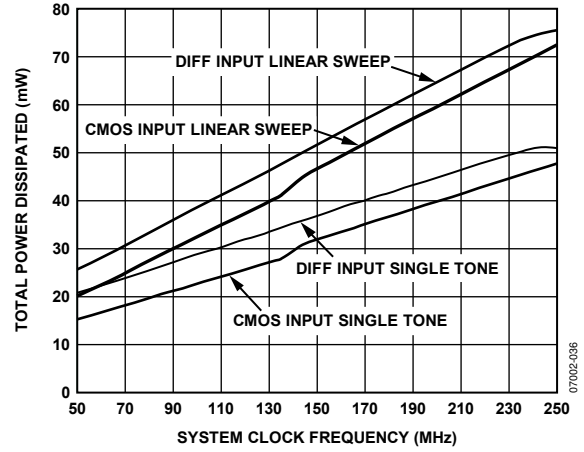


Figure 16. Power Dissipation vs. System Clock Frequency vs. Clock Input Mode

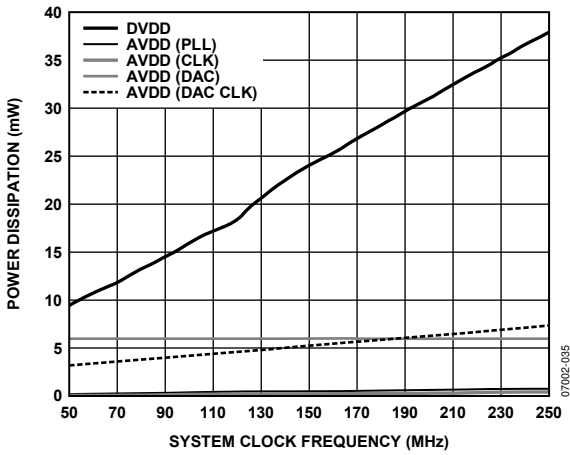


Figure 15. Power Supply Current Domains (CMOS Input Mode, 4 mA DAC Full-Scale Current, Single Tone)

APPLICATIONS CIRCUITS

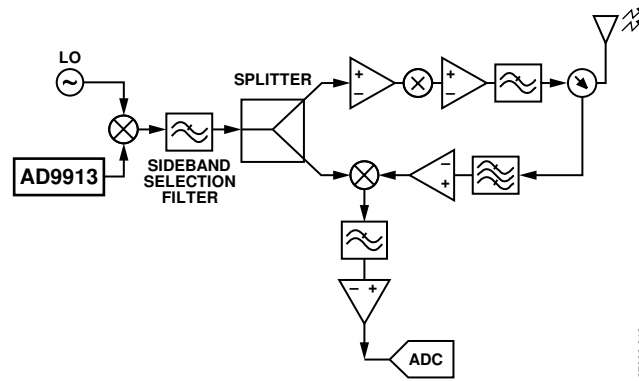


Figure 17. RFID Block Diagram (Only I-Channel of Receiver Shown)

07002-013

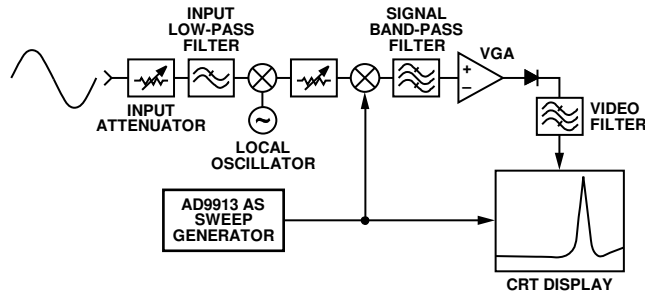


Figure 18. Handheld Spectrum Analyzer

07002-014

# THEORY OF OPERATION

## DDS CORE

The DDS block generates a reference signal (sine or cosine based on the selected DDS sine output bit). The parameters of the reference signal (frequency and phase), are applied to the DDS at its frequency and phase offset control inputs, as shown in Figure 19.

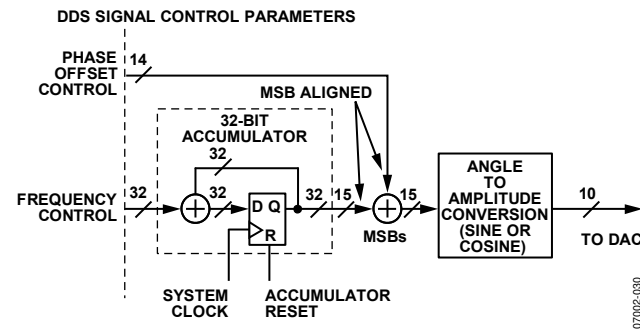


Figure 19. DDS Block Diagram

The output frequency ( $f_{OUT}$ ) of the AD9913 is controlled by the frequency tuning word (FTW) at the frequency control input to the DDS. In all modes except for programmable modulus, the relationship between  $f_{OUT}$ , FTW, and  $f_{SYSCLK}$  is:

$$f_{OUT} = \left( \frac{FTW}{2^{32}} \right) f_{SYSCLK} \quad (1)$$

where FTW is a 32-bit integer ranging in value from 0 to 2,147,483,647 ( $2^{31} - 1$ ), which represents the lower half of the full 32-bit range. This range constitutes frequencies from dc to Nyquist (that is,  $\frac{1}{2} f_{SYSCLK}$ ).

The FTW required to generate a desired value of  $f_{OUT}$  is found by solving Equation 1 for FTW as given in Equation 2

$$FTW = \text{round} \left( 2^{32} \left( \frac{f_{OUT}}{f_{SYSCLK}} \right) \right) \quad (2)$$

where the  $\text{round}(x)$  function rounds the argument (the value of  $x$ ) to the nearest integer. This is required because the FTW is constrained to be an integer value.

For applications where rounding to the nearest available frequency is not acceptable, programmable modulus mode enables additional options.

The relative phase of the DDS signal can be digitally controlled by means of a 14-bit phase offset word (POW). The phase offset is applied prior to the angle-to-amplitude conversion block internal to the DDS core. The relative phase offset ( $\Delta\theta$ ) is given by

$$\Delta\theta = \begin{cases} 2\pi \left( \frac{POW}{2^{14}} \right) \\ 360 \left( \frac{POW}{2^{14}} \right) \end{cases}$$

where the upper quantity is for the phase offset expressed as radian units and the lower quantity as degrees. To find the POW value necessary to develop an arbitrary  $\Delta\theta$ , solve the above equation for POW and round the result (in a manner similar to that described for finding an arbitrary FTW in Equation 1 and Equation 2).

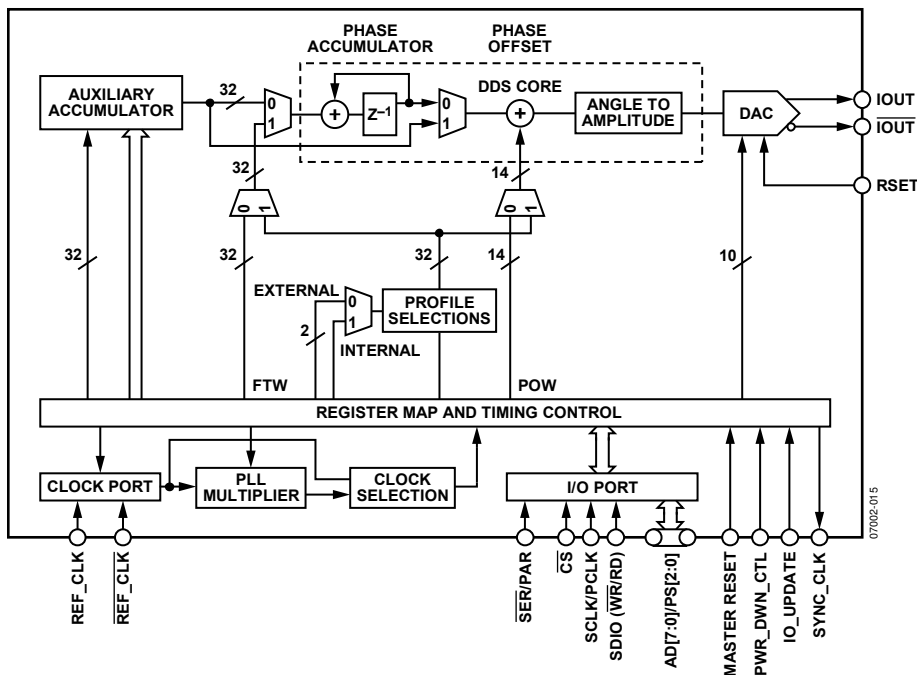


Figure 20. Detailed Block Diagram



## AUXILIARY ACCUMULATOR

In addition to the phase accumulator of the DDS, the AD9913 has an auxiliary accumulator. This accumulator can be configured to support either an automatic sweep of one of the programmable characteristics of the DDS output (frequency or phase), or it can be configured to implement a change in the denominator of the frequency equation given in the DDS Core section. For further details, refer to the Programmable Modulus Mode section.

## 10-BIT DAC

The AD9913 incorporates an integrated 10-bit, current output DAC. The output current is delivered as a balanced signal using two outputs. The use of balanced outputs reduces the potential amount of common-mode noise present at the DAC output, offering the advantage of an increased signal-to-noise ratio. An external resistor ( $R_{SET}$ ) connected between the RSET pin and AGND establishes the reference current. The full-scale output current of the DAC ( $I_{OUT}$ ) is produced as a scaled version of the reference current. The recommended value of  $R_{SET}$  is 4.62 k $\Omega$ .

The following equation computes the typical full-scale current with respect to the  $R_{set}$  resistor value and the gain control setting:

$$I_{OUT}(x, R_{SET}) = \frac{0.0206}{R_{SET}} \times (1 + x)$$

The DAC is designed to operate with full-scale current values up to 4.58 mA. Based on the equation and assuming a 4.62 k  $\Omega$  resistor value for  $R_{SET}$ , and  $x = 0x1FF$ , the nominal output current for the DAC is 2.28 mA.

Figure 17 shows the range of DAC output current vs. the DAC FS value assuming an  $R_{SET}$  value of 4.62 k $\Omega$ .

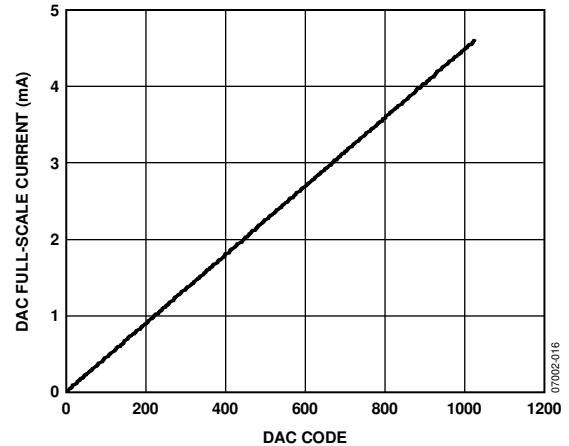


Figure 21. DAC Output Current vs. DAC FS Bits

Pay careful attention to the load termination to ensure that the output voltage remains within the specified compliance range; voltages developed beyond this range cause excessive distortion and can damage the DAC output circuitry.

## I/O PORT

The AD9913 I/O port can be configured as a synchronous serial communications port that allows easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O port is compatible with most synchronous transfer formats, including both the Motorola 6905/11 SPI and Intel 8051 SSR protocols. For faster programming requirements, a parallel mode is also provided.

## PROFILE SELECTIONS

The AD9913 supports the use of profiles, which consist of a group of eight registers containing pertinent operating parameters for a particular operating mode. Profiles enable rapid switching between parameter sets. Profile parameters are programmed via the I/O port. Once programmed, a specific profile is activated by means of Register CFR1 Bits [22:20], or three external profile select pins. The external profile pins option is only available in serial mode.

## MODES OF OPERATION

The AD9913 operates in four modes:

- Single tone
- Direct switch
- Programmable modulus
- Linear sweep

The modes relate to the data source used to supply the DDS with its signal control parameters: frequency, phase, or amplitude. The partitioning of the data into different combinations of frequency, phase, and amplitude is handled automatically based on the mode and/or specific control bits.

### SINGLE TONE MODE

Single tone mode is the default operational mode and is active when both the direct switch mode bit and the auxiliary accumulator enable bit are not set. This mode outputs a single frequency as programmed by the user in the frequency tuning word (FTW) register. A phase offset value is also available in single tone mode via the POW register.

### DIRECT SWITCH MODE

Direct switch mode enables FSK or PSK modulation. This mode simply selects the frequency or phase value programmed into the profile registers. Frequency or phase is determined by the destination bits in CFR1 [13:12]. Direct switch mode is enabled using the direct switch mode active bit in register CFR1 [16].

Two approaches are designed for switching between profile registers. The first is programming the internal profile control bits, CFR1 [22:20], to the desired value and issuing an IO\_UPDATE. The second approach, with higher data throughput, is achieved by changing the profile control pins [2:0]. Control bit CFR1 [27] is for selection between the two approaches. The default state uses the profile pins.

To perform 8-tone FSK or PSK, program the FTW word or phase offset word in each profile. The internal profile control bits or the profile pins are used for the FSK or PSK data.

Table 4 shows the relationship between the profile selection pin or bit approach.

**Table 4. Profile Selection**

Profile Pins PS [2:0] or CFR1 Bits [22:20]	Profile Selection
000	Profile 0
001	Profile 1
010	Profile 2
011	Profile 3
100	Profile 4
101	Profile 5
110	Profile 6
111	Profile 7

## PROGRAMMABLE MODULUS MODE

In programmable modulus mode, the auxiliary accumulator is used to alter the frequency equation of the DDS core, making it possible to implement fractions which are not restricted to a power of 2 in the denominator.

A standard DDS is restricted to powers of 2 as a denominator because the phase accumulator is a set of bits as wide as the frequency tuning word. When in programmable modulus mode, the frequency equation becomes

$$f_0 = (FTW)(f_s)/x \text{ with } 0 \leq FTW \leq 2^{31}$$

$$f_0 = f_s \times (1 - (FTW/x)) \text{ with } 2^{31} < FTW < 2^{32} - 1$$

where  $0 \leq x \leq 2^{32}$ .

When in programmable modulus mode, the auxiliary accumulator is set up to roll over before it reaches full capacity. Every time it rolls over, an extra LSB value is added to the phase accumulator. In order to determine the values that must be programmed in the registers, the user must define the desired output to sampling clock frequency as a ratio of integers (M/N, where N must not exceed  $2^{32}$ ).

Refer to the AN-953 Application Note for detailed steps of how to implement a programmable modulus. The AN-953 defines how to calculate the three required values (A, B, and X) used for programmable modulus. The following assigns the required values to the appropriate register.

- Register 0x06 [63:32] holds the B value.
- Register 0x06 [31:0] holds the X value.
- Register 0x07 [31:0] holds the A value.

### LINEAR SWEEP MODE

One purpose of linear sweep mode is to provide better bandwidth containment compared to direct switch mode by enabling more gradual, user-defined changes between a starting point (S0) to an endpoint (E0). The auxiliary accumulator enable bit is located in Register CFR1 [11]. Linear sweep uses the auxiliary accumulator to sweep frequency or phase from S0 to E0. A frequency or phase sweep is determined by the destination bits in CFR1 [13:12]. The trigger to initiate the sweep can be edge or level triggered. This is determined by Register CFR1 [9]. Note that, in level triggered mode, the sweep automatically repeats as long as the appropriate profile pin is held high.

In linear sweep mode, S0 and E0 (upper and lower limits) are loaded into the linear sweep parameter register (Register 0x06). If configured for frequency sweep, the resolution is 32-bits. For phase sweep, the resolution is 14 bits. When sweeping the phase, the word value must be MSB-aligned; unused bits are ignored. The profile pins or the internal profile bits trigger and control the direction (up/down) of the linear sweep for frequency or phase. Table 5 depicts the direction of the sweep.

**Table 5. Determining the Direction of the Linear Sweep**

Profile Pins [2:0] or CFR1 Bits [22:20]	Linear Sweep Mode
x00 <sup>1</sup>	Sweep off
x01 <sup>1</sup>	Ramp up
x10 <sup>1</sup>	Ramp down
x11 <sup>1</sup>	Bidirectional ramp

<sup>1</sup> x = don't care.

Note that if the part is used in parallel port programming mode, the sweep mode is only determined by the internal profile control bits, CFR1 [22:20]. If the part is used in serial port programming mode, either the internal profile control bits or the external profile select pins can work as the sweep control. CFR1 [27] selects between these two approaches.

**Setting the Slope of the Linear Sweep**

The slope of the linear sweep is set by the intermediate step size (delta tuning word) between S0 and E0 (see Figure 22) and the time spent (sweep ramp rate word) at each step. The resolution of the delta tuning word is 32 bits for frequency and 14 bits for phase. The resolution for the delta ramp rate word is 16 bits.

In linear sweep mode, the user programs a rising delta word (RDW, Register 0x07) and a rising sweep ramp rate (RSRR, Register 0x08). These settings apply when sweeping from S0 to E0. The falling delta word (FDW, Register 0x07) and falling sweep ramp rate (FSRR, Register 0x08) apply when sweeping from E0 to S0.

Note that if the auxiliary accumulator is allowed to overflow, an uncontrolled, continuous sweep operation occurs. To avoid this, the magnitude of the rising or falling delta word should be smaller than the difference between full-scale and the E0 value (full-scale – E0). For a frequency sweep, full-scale is  $2^{32} - 1$ . For a phase sweep, full-scale is  $2^{14} - 1$ .

Figure 22 displays a linear sweep up and then down. This depicts the dwell mode (see CRF1 [8]). If the no-dwell bit, CFR1 [8], is set, the sweep accumulator returns to 0 upon reaching E0.

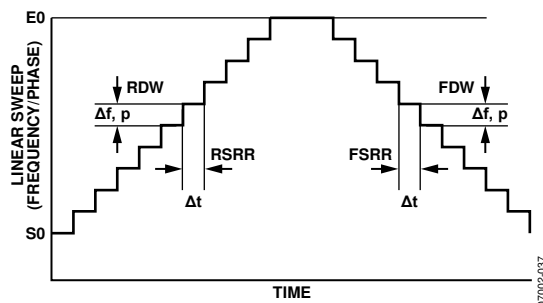


Figure 22. Linear Sweep Mode

For a piecemeal or a nonlinear transition between S0 and E0, the delta tuning words and ramp rate words can be reprogrammed during the transition.

The formulas for calculating the step size of RDW or FDW are

$$Frequency\ Step = \left( \frac{RDW}{2^{32}} \right) f_{SYSCLK} \quad (\text{MHz})$$

$$Phase\ Step = \left( \frac{\pi RDW}{2^{13}} \right) \quad (\text{radians})$$

$$Phase\ Step = \left( \frac{45 RDW}{2^{11}} \right) \quad (\text{degrees})$$

The formula for calculating delta time from RSRR or FSRR is

$$\Delta t = (RSRR) / f_{SYSCLK} \quad (\text{Hz})$$

At 250 MSPS operation, ( $f_{SYSCLK} = 250 \text{ MHz}$ ). The minimum time interval between steps is  $1/250 \text{ MHz} \times 1 = 4 \text{ ns}$ . The maximum time interval is  $(1/250 \text{ MHz}) \times 65,535 = 262 \mu\text{s}$ .

**Frequency Linear Sweep Example**

In linear sweep mode, when sweeping from low to high, the RDW is applied to the input of the auxiliary accumulator and the RSRR register is loaded into the sweep rate timer.

The RDW accumulates at the rate given by the ramp rate (RSRR) until the output equals the upper limit in the linear sweep parameter register (Register 0x06). The sweep is then complete.

When sweeping from high to low, the FDW is applied to the input of the auxiliary accumulator and the FSRR register is loaded into the sweep rate timer.

The FDW accumulates at the rate given by the ramp rate (FSRR) until the output equals the lower limit in the linear sweep parameter register value (Register 0x06). The sweep is then complete. A phase sweep works in the same manner with fewer bits.

To view sweep capabilities using the profile pins and the no-dwell bit, refer to Figure 23, Figure 24, and Figure 25.

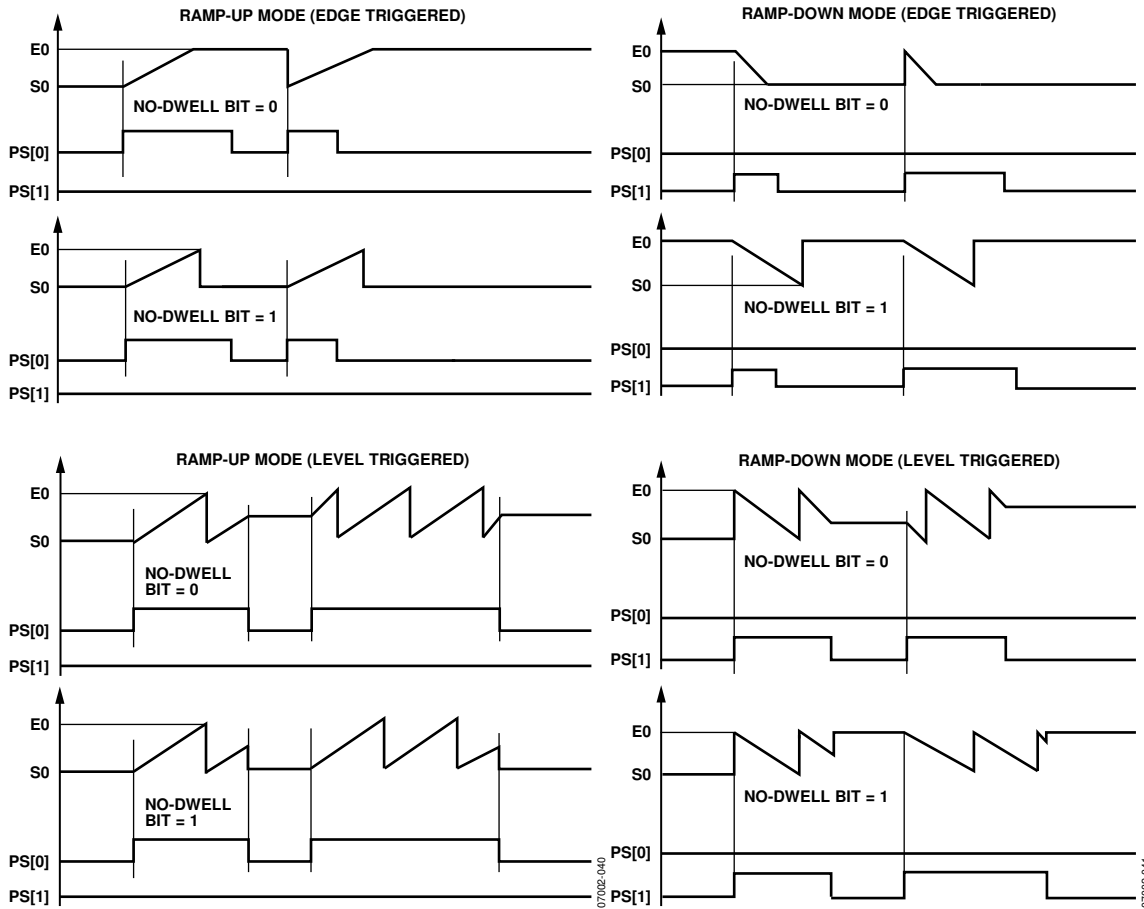


Figure 23. Display of Ramp-Up and Ramp-Down Capability Using the External Profile Pins

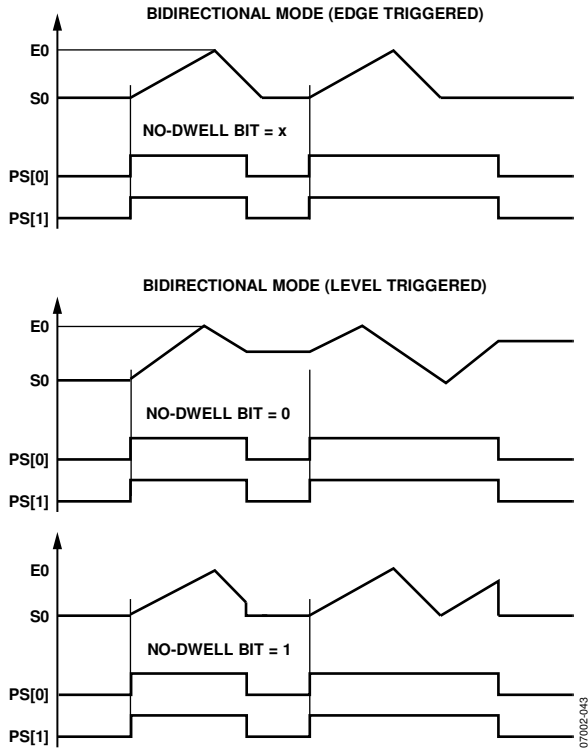


Figure 24. Display of Bidirectional Ramp Capability Using the External Profile Pins

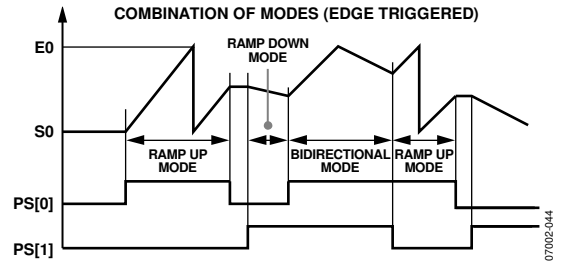


Figure 25. Combination of Sweep Modes Using the External Profile Pins

**Clear Functions**

The AD9913 allows for a programmable continuous zeroing of the sweep logic and the phase accumulator as well as clear-and-release, or automatic zeroing function. Each feature is individually controlled via bits in the control registers.

**Continuous Clear Bits**

The continuous clear bits are simply static control signals that hold the respective accumulator (and associated logic) at zero for the entire time the bit is active.

**Clear-and-Release Function**

The auto clear auxiliary accumulator bit, when active, clears and releases the auxiliary accumulator upon receiving an I/O\_UPDATE or change in profile bits.

The auto clear phase accumulator, when active, clears and releases the phase accumulator upon receiving a I/O\_UPDATE or a change in profile bits.

The automatic clearing function is repeated for every subsequent I/O\_UPDATE or change in profile bits until the control bit is cleared.

These bits are programmed independently and do not have to be active at the same time. For example, one accumulator may be using the clear and release function while the other is continuously cleared.

# CLOCK INPUT (REF\_CLK)

## REF\_CLK OVERVIEW

The AD9913 supports a number of options for producing the internal SYSCLK signal (that is, the DAC sample clock) via the REF\_CLK input pins. The REF\_CLK input can be driven directly from a differential or single-ended source, or it can accept a crystal connected across the two input pins. There is also an internal phase-locked loop (PLL) multiplier that can be independently enabled. The various input configurations are controlled by means of the control bits in the CFR2 [7:5] register.

Table 6. Clock Input Mode Configuration

CFR2 [7:5]	Mode Configuration
000	Differential Input, PLL Enabled
001	Differential Input, PLL Disabled (Default)
x10 <sup>1</sup>	XTAL Input, PLL Enabled
x11 <sup>1</sup>	XTAL Input, PLL Disabled
100	CMOS Input, PLL Enabled
101	CMOS Input PLL Disabled

<sup>1</sup> x = don't care.

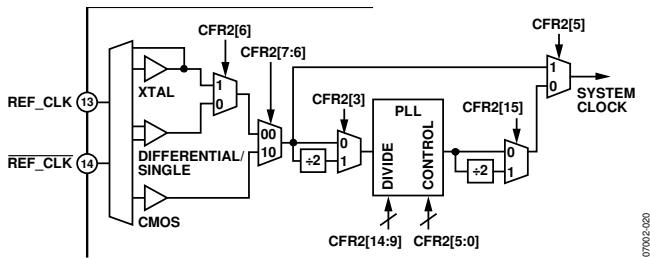


Figure 26. Internal Clock Path Functional Block Diagram

## CRYSTAL-DRIVEN REF\_CLK

When using a crystal at the REF\_CLK input, the resonant frequency should be approximately 25 MHz. Figure 27 shows the recommended circuit configuration.

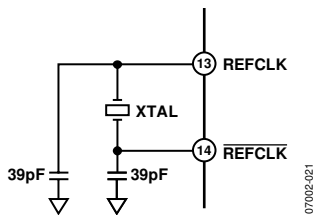


Figure 27. Crystal Connection Diagram

## DIRECT-DRIVEN REF\_CLK

When driving the REF\_CLK inputs directly from a signal source, either single-ended or differential signals can be used. With a differential signal source, the REF\_CLK pins are driven with complementary signals and ac-coupled with 0.1 μF capacitors. With a single-ended signal source, either a single-ended-to-differential conversion can be employed or the REF\_CLK input can be driven single-ended directly. In either case, 0.1 μF capacitors are used to ac couple both REF\_CLK

pins to avoid disturbing the internal dc bias voltage of ~1.35 V. See Figure 28 for more details.

The REF\_CLK input resistance is ~2.7 kΩ differential (~1.35 kΩ single-ended). Most signal sources have relatively low output impedances. The REF\_CLK input resistance is relatively high, therefore, its effect on the termination impedance is negligible and can usually be chosen to be the same as the output impedance of the signal source. The bottom two examples in Figure 28 assume a signal source with a 50 Ω output impedance.

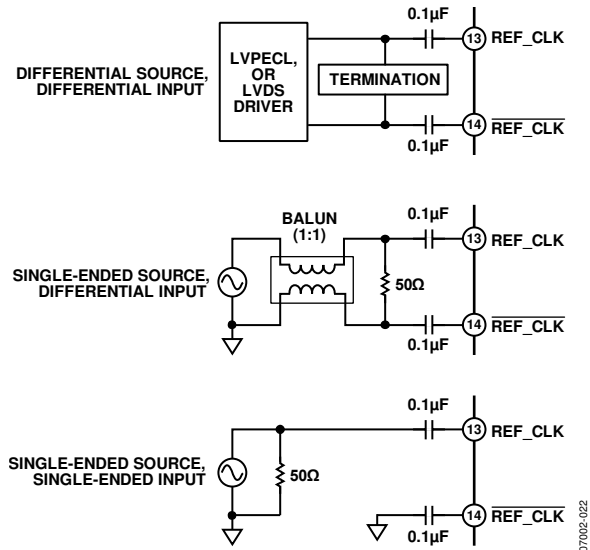


Figure 28. Direct Connection Diagram

## CMOS-DRIVEN REF\_CLK

This mode is enabled by writing CFR2 [7] to be true. In this state, the AD9913 must be driven at Pin 13 with the reference clock source. Additionally, it is recommended that Pin 14 in CMOS mode be tied to ground through a 10 kΩ resistor.

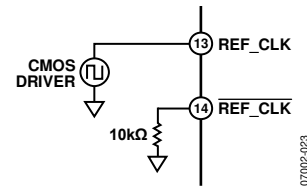


Figure 29. CMOS-Driven Diagram

## PHASE-LOCKED LOOP (PLL) MULTIPLIER

An internal phase-locked loop (PLL) provides users of the AD9913 the option to use a reference clock frequency that is lower than the system clock frequency. The PLL supports a wide range of programmable frequency multiplication factors (1× to 64×). See Table 7 for details on configuring the PLL multiplication factor. The PLL is also equipped with a PLL\_LOCK bit.

CFR2 [15:8] and CFR2 [5:1] control the PLL operation. Upon power-up, the PLL is off. To initialize the PLL, CFR2 [5] must be cleared and CFR2 [1] must be set. The function of CFR2 [1]

is to reset digital logic in the PLL circuit with an active low signal. The function of CFR2 [5] is to power up or power down the PLL.

CFR2 [4] is the PLL LO range bit. When operating the AD9913 with the PLL enabled, CFR2 [4] adjusts PLL loop filter components to allow low frequency reference clock inputs.

CFR2 [3] enables a divide-by-two circuit at the input of the PLL phase detector. If this bit is enabled the reference clock signal is divided by 2 prior to multiplication in the PLL. Refer to the electrical specifications for the maximum reference clock input frequency when utilizing the PLL with the divide by 2 circuit enabled. If the divide by 2 circuit is disabled and the PLL is enabled, then the maximum reference clock input frequency is one-half the maximum rate indicated in the electrical specifications table for the maximum input divider frequency.

The AD9913 PLL uses one of two VCOs for producing the system clock signal. CFR2 Bit 2 is a select bit that enables an alternative VCO in the PLL. The basic operation of the PLL is not affected by the state of this bit. The purpose of offering two VCOs is to provide performance options. The two VCOs have approximately the same gain characteristics, but differ in other aspects. The overall spurious performance, phase noise, and power consumption may change based on the setting of CFR2 Bit 2. It is important to consider that for either VCO, the minimum oscillation frequency must be satisfied, and that minimum oscillation frequency is significantly different between the two oscillators.

CFR2 [15:9], along with CFR2 [3], determine the multiplication of the PLL. CFR2 [15] enables a divider at the output of the

PLL. The bits CFR [14:9] control the feedback divider. The feedback divider is composed of two stages:  $\div N$  (1:31) selected by CFR2 [13:9];  $\div 1$  or  $\div 2$  selected by CFR2 [14].

Note that the same system clock frequency can be obtained with different combinations of CFR2 [15:9] and CFR2 [3]. One combination may work better in a given application either to run at lower power or to satisfy the VCOs minimum oscillation frequency

Note that the AD9913 maximum system clock frequency is 250 MHz. If the user intends to use high values for the PLL feedback divider ratio, then care should be taken that the system clock frequency does not exceed 250 MHz.

### PLL LOCK INDICATION

CFR2 [0] is a read-only bit that displays the status of the PLL lock signal.

When the AD9913 is programmed to use the PLL, there is some amount of time required for the loop to lock. While the loop is not locked, the chip system clock operates at the reference clock frequency presented to the part at the pins. Once the PLL lock signal goes high, the system clock frequency switches asynchronously to operate at the PLL output frequency. To maintain a system clock frequency with or without a locked loop if the PLL lock signal transitions low, the chip reverts to the reference clock signal while the loop attempts to acquire lock once again.

Table 7 describes how to configure the PLL multiplication factor using the appropriated register bits.

**Table 7. PLL Multiplication Factor Configuration**

CFR2 [13:9]	CFR2 [15:14], CFR2 [3]							
	= 000	= 001	= 100	= 101	= 010	= 011	= 110	= 111
00000	32	16	16	8	64	32	32	16
00001	1	0.5	0.5	0.25	2	1	1	0.5
00010	2	1	1	0.5	4	2	2	1
00011	3	1.5	1.5	0.75	6	3	3	1.5
00100	4	2	2	1	8	4	4	2
00101	5	2.5	2.5	1.25	10	5	5	2.5
00110	6	3	3	1.5	12	6	6	3
00111	7	3.5	3.5	1.75	14	7	7	3.5
01000	8	4	4	2	16	8	8	4
01001	9	4.5	4.5	2.25	18	9	9	4.5
01010	10	5	5	2.5	20	10	10	5
01011	11	5.5	5.5	2.75	22	11	11	5.5
01100	12	6	6	3	24	12	12	6
01101	13	6.5	6.5	3.25	26	13	13	6.5
01110	14	7	7	3.5	28	14	14	7
01111	15	7.5	7.5	3.75	30	15	15	7.5
10000	16	8	8	4	32	16	16	8
10001	17	8.5	8.5	4.25	34	17	17	8.5
10010	18	9	9	4.5	36	18	18	9
10011	19	9.5	9.5	4.75	38	19	19	9.5
10100	20	10	10	5	40	20	20	10
10101	21	10.5	10.5	5.25	42	21	21	10.5
10110	22	11	11	5.5	44	22	22	11
10111	23	11.5	11.5	5.75	46	23	23	11.5
11000	24	12	12	6	48	24	24	12
11001	25	12.5	12.5	6.25	50	25	25	12.5
11010	26	13	13	6.5	52	26	26	13
11011	27	13.5	13.5	6.75	54	27	27	13.5
11100	28	14	14	7	56	28	28	14
11101	29	14.5	14.5	7.25	58	29	29	14.5
11110	30	15	15	7.5	60	30	30	15
11111	31	15.5	15.5	7.75	62	31	31	15.5



## POWER-DOWN FEATURES

The AD9913 supports an externally controlled power-down feature as well as software programmable power-down bits consistent with other Analog Devices, Inc. DDS products.

The external PWR\_DWN\_CTL pin determines the power-down scheme. A low on this pin allows the user to power down DAC, PLL, input clock circuitry, and the digital section of the chip individually via the unique control bits, CFR1 [6:4]. In this mode, CFR1 [7] is inactive.

When the PWR\_DWN\_CTL is set, CFR1 [6:4] lose their meaning. At the same time, the AD9913 provides two different power-down modes based on the value of CFR1 [7]: a fast recovery power-down mode in which only the digital logic and the DAC digital logic are powered down, and a full power-down mode in which all functions are powered down. A significant amount of time is required to recover from power-down mode.

Table 11 indicates the logic level for each power-down bit that drives out of the AD9913 core logic to the analog section and the digital clock generation section of the chip for the external power-down operation.

**Table 8. Power-Down Controls**

Control	Mode Active	Description
PWR_DWN_CTL = 0 CFR1 [7] = don't care	Software Control	Digital power-down = CFR1 [6] DAC power-down = CFR1 [5] Input clock power-down = CFR1 [4]
PWRDWNCTL = 1 CFR1 [7] = 0	External Control, Fast recovery power-down mode	N/A
PWRDWNCTL = 1 CFR1 [7] = 1	External Control, Full power-down mode	N/A

## I/O PROGRAMMING

### SERIAL PROGRAMMING

The AD9913 serial port is a flexible, synchronous serial communications port allowing an easy interface to many industry standard microcontrollers and microprocessors.

The interface allows read/write access to all registers that configure the AD9913. MSB first or LSB first transfer formats are supported. The AD9913 serial interface port is configured as a single pin I/O (SDIO), which allows a two-wire interface. The AD9913 does not have a SDO pin for 3-wire operation.

With the AD9913, the instruction byte specifies read/write operation and the register address. Serial operations on the AD9913 occur only at the register level, not the byte level.

For the AD9913, the serial port controller recognizes the instruction byte register address and automatically generates the proper register byte address. In addition, the controller expects that all bytes of that register are accessed. It is a requirement that all bytes of a register be accessed during serial I/O operations.

There are two phases to a communication cycle with the AD9913. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9913, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9913 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the

upcoming data transfer is read or write and the serial address of the register being accessed.

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9913. The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9913 and the system controller. The number of bytes transferred during Phase 2 of the communication cycle is a function of the register accessed. For example, when accessing the Control Function Register 2, which is two bytes wide, Phase 2 requires that two bytes be transferred. If accessing one of the profile registers, which are six bytes wide, Phase 2 requires that six bytes be transferred. After transferring all data bytes per the instruction, the communication cycle is completed.

At the completion of any communication cycle, the AD9913 serial port controller expects the next eight rising SCLK edges to be the instruction byte of the next communication cycle.

All data input to the AD9913 is registered on the rising edge of SCLK. All data is driven out of the AD9913 on the falling edge of SCLK. Figure 30 through Figure 32 illustrate the general operation of serial ports.

Note that IO\_UPDATE is not shown in Figure 30 and Figure 31. The IO\_UPDATE transfers the contents of the write sequence to the active register. See the Register Update (I/O Update) section.

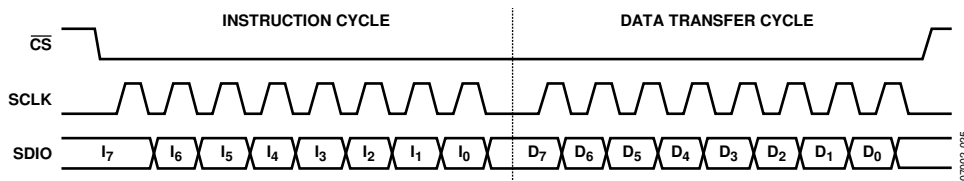


Figure 30. Serial Port Writing Timing—Clock Stall Low

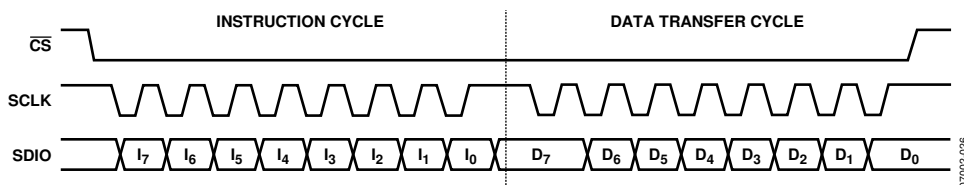


Figure 31. Serial Port Write Timing—Clock Stall High

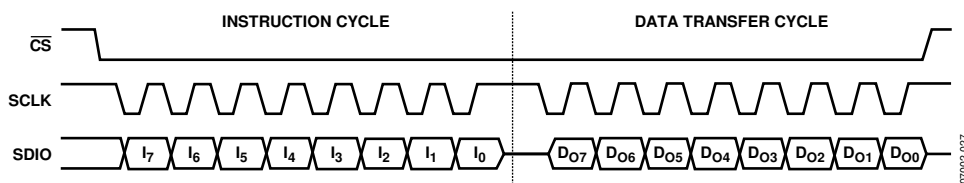


Figure 32. Two-Wire Serial Port Read Timing—Clock Stall High