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3.5 GSPS Direct Digital Synthesizer with 12-Bit DAC

Data Sheet

AD9914

FEATURES

- 3.5 GSPS internal clock speed
- Integrated 12-bit DAC
- Frequency tuning resolution to 190 pHz
- 16-bit phase tuning resolution
- 12-bit amplitude scaling
- Programmable modulus
- Automatic linear and nonlinear frequency sweeping capability
- 32-bit parallel datapath interface
- 8 frequency/phase offset profiles
- Phase noise: −128 dBc/Hz (1 kHz offset at 1396 MHz)
- Wideband SFDR < −50 dBc
- Serial or parallel input/output control
- 1.8 V/3.3 V power supplies
- Software and hardware controlled power-down
- 88-lead LFCSP package
- PLL REF CLK multiplier
- Phase modulation capability
- Amplitude modulation capability

APPLICATIONS

- Agile LO frequency synthesis
- Programmable clock generator
- FM chirp source for radar and scanning systems
- Test and measurement equipment
- Acousto-optic device drivers
- Polar modulator
- Fast frequency hopping

FUNCTIONAL BLOCK DIAGRAM

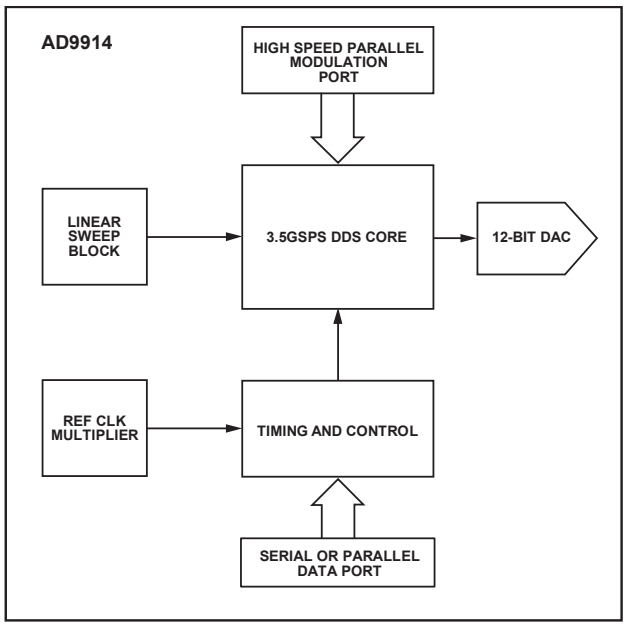

Figure 1.

Rev. F

Document Feedback

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- AD9914 Evaluation Board

DOCUMENTATION

Application Notes

- AN-953: Direct Digital Synthesis (DDS) with a Programmable Modulus

Data Sheet

- AD9914: 3.5 GSPS Direct Digital Synthesizer with 12-Bit DAC Data Sheet

User Guides

- AD9914/AD9915 Evaluation Board User Guide

TOOLS AND SIMULATIONS

- AD9914 IBIS Model

REFERENCE MATERIALS

Press

- Analog Devices Advances RF and Microwave Designs from Bits to Antenna and Back at IMS2012
- Analog Devices Unveils Industry's Fastest 12-bit, Direct Digital Synthesizers for Frequency-Agile Wireless Applications

Product Selection Guide

- RF Source Booklet

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- AD9914 Material Declaration
- PCN-PDN Information
- Quality And Reliability
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7/2012—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9914 is a direct digital synthesizer (DDS) featuring a 12-bit DAC. The AD9914 uses advanced DDS technology, coupled with an internal high speed, high performance DAC to form a digitally programmable, complete high frequency synthesizer capable of generating a frequency-agile analog output sinusoidal waveform at up to 1.4 GHz. The AD9914 enables fast frequency hopping and fine tuning resolution (64-bit capable using programmable modulus mode). The AD9914 also offers fast phase and amplitude hopping capability. The frequency tuning and control words are loaded into the AD9914 via a serial or parallel input/output port. The AD9914 also supports a user defined linear sweep mode of operation for generating linear swept waveforms of frequency, phase, or amplitude. A high speed, 32-bit parallel data input port is included, enabling high data rates for polar modulation schemes and fast reprogramming of the phase, frequency, and amplitude tuning words.

The AD9914 is specified to operate over the extended industrial temperature range (see the Absolute Maximum Ratings section).

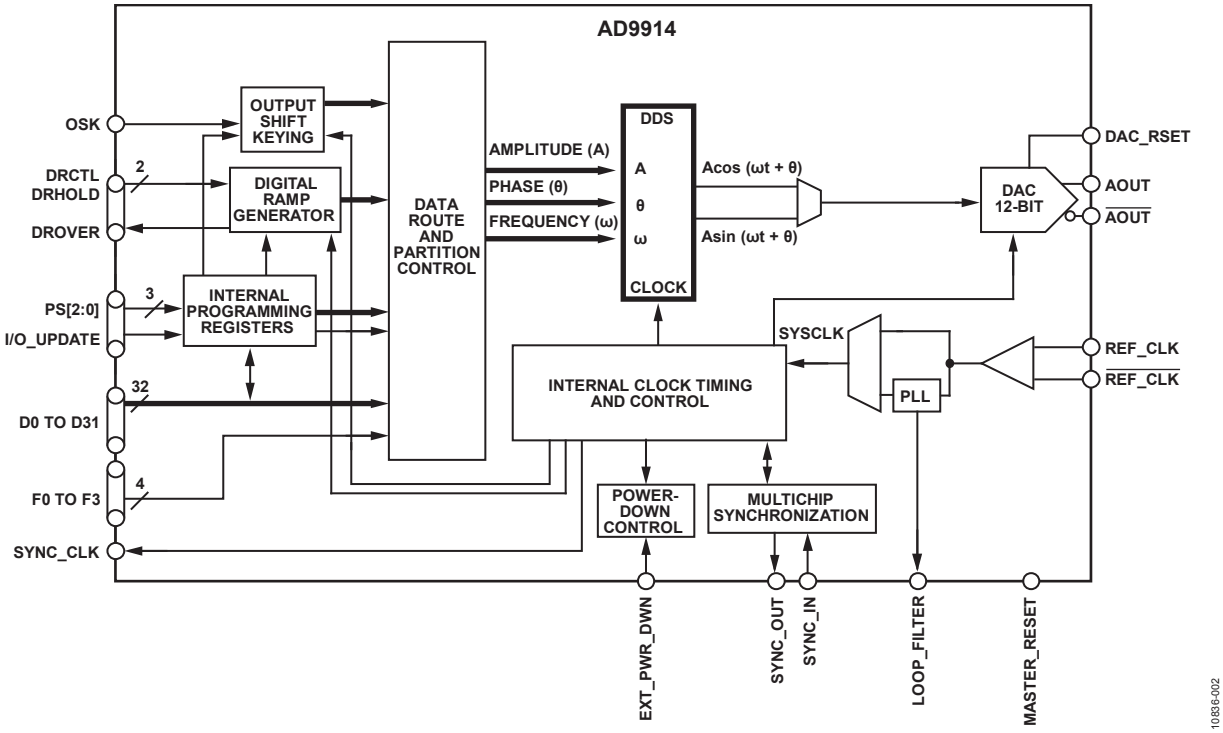


Figure 2. Detailed Block Diagram

SPECIFICATIONS

DC SPECIFICATIONS

AVDD (1.8 V) and DVDD (1.8 V) = 1.8 V ± 5%, AVDD (3.3 V) and DVDD_I/O (3.3 V) = 3.3 V ± 5%, T_A = 25°C, R_{SET} = 3.3 kΩ, I_{OUT} = 20 mA, external reference clock frequency = 3.5 GHz with reference clock (REF CLK) multiplier bypassed, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
DVDD_I/O	3.135	3.30	3.465	V	Pin 16, Pin 83
DVDD	1.71	1.80	1.89	V	Pin 6, Pin 23, Pin 73
AVDD (3.3 V)	3.135	3.30	3.465	V	Pin 34, Pin 36, Pin 39, Pin 40, Pin 43, Pin 47, Pin 50, Pin 52, Pin 53, Pin 60
AVDD (1.8 V)	1.71	1.80	1.89	V	Pin 32, Pin 56, Pin 57
SUPPLY CURRENT					See also the total power dissipation specifications
$I_{DVDD\_I/O}$			20	mA	Pin 16, Pin 83
I_{DVDD}			433	mA	Pin 6, Pin 23, Pin 73
$I_{AVDD(3.3V)}$			640	mA	Pin 34, Pin 36, Pin 39, Pin 40, Pin 43, Pin 47, Pin 50, Pin 52, Pin 53, Pin 60
$I_{AVDD(1.8V)}$			178	mA	Pin 32, Pin 56, Pin 57
TOTAL POWER DISSIPATION					
Base DDS Power, PLL Disabled		2392	3091	mW	3.5 GHz, single-tone mode, modules disabled, linear sweep disabled, amplitude scaler disabled
Base DDS Power, PLL Enabled		2237	2627	mW	2.5 GHz, single-tone mode, modules disabled, linear sweep disabled, amplitude scaler disabled
Linear Sweep Additional Power		28		mW	
Modulus Additional Power		20		mW	
Amplitude Scaler Additional Power		138		mW	Manual or automatic
Full Power-Down Mode		400	616	mW	Using either the power-down and enable register or the EXT_PWR_DWN pin
CMOS LOGIC INPUTS					
Input High Voltage (V_{IH})	2.0		DVDD_I/O	V	
Input Low Voltage (V_{IL})			0.8	V	
Input Current (I_{INH}, I_{INL})		±60	±200	µA	At V_{IN} = 0 V and V_{IN} = DVDD_I/O
Maximum Input Capacitance (C_{IN})		3		pF	
CMOS LOGIC OUTPUTS					
Output High Voltage (V_{OH})	2.7		DVDD_I/O	V	I_{OH} = 1 mA
Output Low Voltage (V_{OL})			0.4	V	I_{OL} = 1 mA
REF CLK INPUT CHARACTERISTICS					REF CLK inputs must always be ac-coupled (both single-ended and differential)
REF CLK Multiplier Bypassed					
Input Capacitance		1		pF	Single-ended, each pin
Input Resistance		1.4		kΩ	Differential
Internally Generated DC Bias Voltage		2		V	
Differential Input Voltage		0.8	1.5	V p-p	
REF CLK Multiplier Enabled					
Input Capacitance		1		pF	Single-ended, each pin
Input Resistance		1.4		kΩ	Differential
Internally Generated DC Bias Voltage		2		V	
Differential Input Voltage		0.8	1.5	V p-p	

AC SPECIFICATIONS

AVDD (1.8V) and DVDD (1.8V) = 1.8 V ± 5%, AVDD3 (3.3V) and DVDD_I/O (3.3V) = 3.3 V ± 5%, T_A = 25°C, R_{SET} = 3.3 kΩ, I_{OUT} = 20 mA, external reference clock frequency = 3.5 GHz with reference clock (REF CLK) multiplier bypassed, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REF CLK INPUT					Input frequency range
REF CLK Multiplier Bypassed					
Input Frequency Range	500		3500	MHz	Maximum f_{OUT} is 0.4 × f_{SYSCLK}
Duty Cycle	45		55	%	
Minimum Differential Input Level	632			mV p-p	Equivalent to 316 mV swing on each leg
System Clock (SYSCLK) PLL Enabled					
VCO Frequency Range	2400		2500	MHz	
VCO Gain (K_V)		60		MHz/V	
Maximum PFD Rate			125	MHz	
CLOCK DRIVERS					
SYNC_CLK Output Driver					
Frequency Range			146	MHz	
Duty Cycle	45	50	55	%	
Rise Time/Fall Time (20% to 80%)		650		ps	
SYNC_OUT Output Driver					10 pF load
Frequency Range			9.1	MHz	
Duty Cycle	33		66	%	CFR2 register, Bit 9 = 1
Rise Time (20% to 80%)		1350		ps	10 pF load
Fall Time (20% to 80%)		1670		ps	10 pF load
DAC OUTPUT CHARACTERISTICS					
Output Frequency Range (1st Nyquist Zone)	0		1750	MHz	
Output Resistance		50		Ω	Single-ended (each pin internally terminated to AVDD (3.3 V))
Output Capacitance		1		pF	
Full-Scale Output Current			20.48	mA	Range depends on DAC R_{SET} resistor
Gain Error	−10		+10	% FS	
Output Offset			0.6	µA	
Voltage Compliance Range	AVDD − 0.50		AVDD + 0.50	V	
Wideband SFDR					See the Typical Performance Characteristics section
101.1 MHz Output		−66		dBc	0 MHz to 1750 MHz
427.5 MHz Output		−65		dBc	0 MHz to 1750 MHz
696.5 MHz Output		−57		dBc	0 MHz to 1750 MHz
1396.5 MHz Output		−52		dBc	0 MHz to 1750 MHz
Narrow-Band SFDR					See the Typical Performance Characteristics section
100.5 MHz Output		−95		dBc	±500 kHz
427.5 MHz Output		−95		dBc	±500 kHz
696.5 MHz Output		−95		dBc	±500 kHz
1396.5 MHz Output		−92		dBc	±500 kHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL TIMING SPECIFICATIONS					
Time Required to Enter Power-Down		45		ns	Power-down mode loses DAC/PLL calibration settings
Time Required to Leave Power-Down		250		ns	Must recalibrate DAC/PLL
Minimum Master Reset time	24			SYSCLK cycles	
Maximum DAC Calibration Time (t_{CAL})			135	µs	See the DAC Calibration Output section for formula
Maximum PLL Calibration Time (t_{REF_CLK})			16	ms	PFD rate = 25 MHz
			8	ms	PFD rate = 50 MHz
Maximum Profile Toggle Rate			2	SYNC_CLK period	
PARALLEL PORT TIMING					
Write Timing					
Address Setup Time to $\overline{WR}$ Active	1			ns	
Address Hold Time to $\overline{WR}$ Inactive			0	ns	
Data Setup Time to $\overline{WR}$ Inactive	3.8			ns	
Data Hold Time to $\overline{WR}$ Inactive			0	ns	
$\overline{WR}$ Minimum Low Time			2.1	ns	
$\overline{WR}$ Minimum High Time			3.8	ns	
Minimum $\overline{WR}$ Time			10.5	ns	
Read Timing					
Address to Data Valid			92	ns	
Address Hold to $\overline{RD}$ Inactive			0	ns	
$\overline{RD}$ Active to Data Valid			69	ns	
$\overline{RD}$ Inactive to Data Tristate			50	ns	
$\overline{RD}$ Minimum Low Time			69	ns	
$\overline{RD}$ Minimum High Time			50	ns	
SERIAL PORT TIMING					
SCLK Clock Rate ($1/t_{CLK}$)			80	MHz	SCLK duty cycle = 50%
SCLK Pulse Width High, t_{HIGH}	1.5			ns	
SCLK Pulse Width Low, t_{LOW}	5.1			ns	
SDIO to SCLK Setup Time, t_{DS}	4.9			ns	
SDIO to SCLK Hold Time, t_{DH}			0	ns	
SCLK Falling Edge to Valid Data on SDIO/SDO, t_{DV}			78	ns	
$\overline{CS}$ to SCLK Setup Time, t_S	4			ns	
$\overline{CS}$ to SCLK Hold Time, t_H			0	ns	
$\overline{CS}$ Minimum Pulse Width High, t_{PWH}	4			ns	
DATA PORT TIMING					
D[31:0] Setup Time to SYNC_CLK	2			ns	
D[31:0] Hold Time to SYNC_CLK			0	ns	
F[3:0] Setup Time to SYNC_CLK	2			ns	
F[3:0] Hold Time to SYNC_CLK			0	ns	
IO_UPDATE Pin Setup Time to SYNC_CLK	2			ns	
IO_UPDATE Pin Hold Time to SYNC_CLK			0	ns	
Profile Pin Setup Time to SYNC_CLK	2			ns	
Profile Pin Hold Time to SYNC_CLK			0	ns	
DR_CTL/DR_HOLD Setup Time to SYNC_CLK	2			ns	
DR_CTL/DR_HOLD Hold Time to SYNC_CLK			0	ns	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DATA LATENCY (PIPELINE DELAY)					SYSCLK cycles = f_S = system clock frequency in GHz
Single Tone Mode or Profile Mode (Matched Latency Disabled)					
Frequency		318		SYSCLK cycles	OSK disabled
		342		SYSCLK cycles	OSK enabled
Phase		294		SYSCLK cycles	OSK disabled
		318		SYSCLK cycles	OSK enabled
Amplitude		102		SYSCLK cycles	OSK enabled
Single Tone Mode or Profile Mode (Matched Latency Enabled)					
Frequency		318		SYSCLK cycles	OSK disabled
		342		SYSCLK cycles	OSK enabled
Phase		318		SYSCLK cycles	OSK disabled
		342		SYSCLK cycles	OSK enabled
Amplitude		342		SYSCLK cycles	OSK enabled
Modulation Mode with 32-Bit Parallel Port (Matched Latency Disabled)					
Frequency		318		SYSCLK cycles	OSK disabled
		342		SYSCLK cycles	OSK enabled
Phase		294		SYSCLK cycles	OSK disabled
		318		SYSCLK cycles	OSK enabled
Amplitude		102		SYSCLK cycles	OSK enabled
Modulation Mode with 32-Bit Parallel Port (Matched Latency Enabled)					
Frequency		318		SYSCLK cycles	OSK disabled
		342		SYSCLK cycles	OSK enabled
Phase		318		SYSCLK cycles	OSK disabled
		342		SYSCLK cycles	OSK enabled
Amplitude		342		SYSCLK cycles	OSK enabled
Sweep Mode (Match Latency Disabled)					
Frequency		342		SYSCLK cycles	OSK disabled
		366		SYSCLK cycles	OSK enabled
Phase		318		SYSCLK cycles	OSK disabled
		342		SYSCLK cycles	OSK enabled
Amplitude		126		SYSCLK cycles	OSK enabled
Sweep Mode (Match Latency Enabled)					
Frequency		342		SYSCLK cycles	OSK disabled
		366		SYSCLK cycles	OSK enabled
Phase		342		SYSCLK cycles	OSK disabled
		366		SYSCLK cycles	OSK enabled
Amplitude		366		SYSCLK cycles	OSK enabled

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
AVDD (1.8 V), DVDD (1.8 V) Supplies	2 V
AVDD (3.3 V), DVDD_I/O (3.3 V) Supplies	4 V
Digital Input Voltage	−0.7 V to +4 V
Digital Output Current	5 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature	150°C
Lead Temperature (10 sec Soldering)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL PERFORMANCE

Table 4.

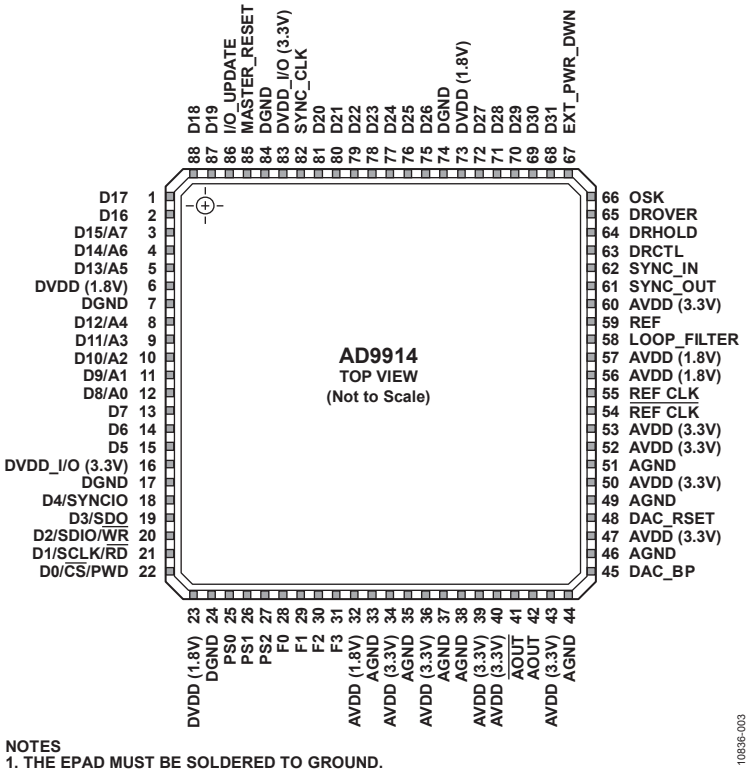
Symbol	Description	Value[1]	Unit
θ_{JA}	Junction-to-ambient thermal resistance (still air) per JEDEC JESD51-2	24.1	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance (1.0 m/sec airflow) per JEDEC JESD51-6	21.3	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance (2.0 m/sec air flow) per JEDEC JESD51-6	20.0	°C/W
θ_{JB}	Junction-to-board thermal resistance (still air) per JEDEC JESD51-8	13.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter (still air) per JEDEC JESD51-6	12.8	°C/W
θ_{JC}	Junction-to-case thermal resistance	2.21	°C/W
Ψ_{JT}	Junction-to-top-of-package characterization parameter (still air) per JEDEC JESD51-2	0.23	°C/W

[1] Results are from simulations. PCB is JEDEC multilayer. Thermal performance for actual applications requires careful inspection of the conditions in the application to determine if they are similar to those assumed in these calculations.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EPAD MUST BE SOLDERED TO GROUND.

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	I/O[1]	Description
1, 2, 13 to 15, 68 to 72, 75 to 81, 87, 88	D5 to D7, D16 to D31, D27 to D31	I/O	Parallel Port Pins. The 32-bit parallel port offers the option for serial or parallel programming of the internal registers. In addition, the parallel port can be configured to provide direct FSK, PSK, or ASK (or combinations thereof) modulation data. The 32-bit parallel port configuration is set by the state of the four function pins (F0 to F3).
3	D15/A7	I/O	Parallel Port Pin/Address Line. The state of the F0 to F3 function pins determines if this pin acts as a line for direct FSK, PSK, or ASK data or as an address line for programming the internal registers.
4	D14/A6	I/O	Parallel Port Pin/Address Line. The state of the F0 to F3 function pins determines if this pin acts as a line for direct FSK, PSK, or ASK data or as an address line for programming the internal registers.
5	D13/A5	I/O	Parallel Port Pin/Address Line. The state of the F0 to F3 function pins determines if this pin acts as a line for direct FSK, PSK, or ASK data or as an address line for programming the internal registers.
8	D12/A4	I/O	Parallel Port Pin/Address Line. The state of the F0 to F3 function pins determines if this pin acts as a line for direct FSK, PSK, or ASK data or as an address line for programming the internal registers.
9	D11/A3	I/O	Parallel Port Pin/Address Line. The state of the F0 to F3 function pins determines if this pin acts as a line for direct FSK, PSK, or ASK data or as an address line for programming the internal registers.
10	D10/A2	I/O	Parallel Port Pin/Address Line. Multipurpose pin depending on the state of the function pins (F0 to F3). The state of the F0 to F3 function pins determines if this pin acts as a line for direct FSK, PSK, or ASK data or as an address line for programming the internal registers.
11	D9/A1	I/O	Parallel Port Pin/Address Line. Multipurpose pin depending on the state of the function pins (F0 to F3). The state of the F0 to F3 function pins determines if this pin acts as a line for direct FSK, PSK, or ASK data or as an address line for programming the internal registers.

Pin No.	Mnemonic	I/O[1]	Description
12	D8/A0	I/O	Parallel Port Pin/Address Line. The state of the F0 to F3 function pins determines if this pin acts as a line for direct FSK, PSK, or ASK data or as an address line for programming the internal registers.
18	D4/SYNCIO	I	Parallel Port Pin/Serial Port Synchronization Pin. This pin is D4 for direct FSK, PSK, or ASK data. If serial mode is invoked via F0 to F3, this pin resets the serial port.
19	D3/SDO	I/O	Parallel Port Pin/Serial Data Output. This pin is D3 for direct FSK, PSK, or ASK data. If serial mode is invoked via F0 to F3, this pin is used for readback mode for serial operation.
20	D2/SDIO/$\overline{WR}$	I/O	Parallel Port Pin/Serial Data Input and Output/Write Input. This pin is D2 for direct FSK, PSK, or ASK data. If serial mode is invoked via F0 to F3, this pin is used for the SDIO for serial operation. If parallel mode is enabled, this pin is writes to change the values of the internal registers.
21	D1/SCLK/$\overline{RD}$	I	Parallel Port Pin/Serial Clock/Read Input. This pin is D1 for direct FSK, PSK, or ASK data. If serial mode is invoked via F0 to F3, this pin is used for SCLK for serial operation. If parallel mode is enabled, this pin reads back the value of the internal registers.
22	D0/$\overline{CS}$/PWD	I	Parallel Port Pin/Chip Select/Parallel Width. This pin is D0 for direct FSK, PSK, or ASK data. If serial mode is invoked via F0 to F3, this pin is used for the chip select for serial operation. If parallel mode is enabled, this pin sets either 8-bit data or16-bit data.
6, 23, 73	DVDD (1.8V)	I	Digital Core Supplies (1.8 V).
7, 17, 24, 74, 84	DGND	I	Digital Ground.
16, 83	DVDD_I/O (3.3V)	I	Digital Input/Output Supplies (3.3 V).
32, 56, 57	AVDD (1.8V)	I	Analog Core Supplies (1.8 V).
33, 35, 37, 38, 44, 46, 49, 51	AGND	I	Analog Ground.
34, 36, 39, 40, 43, 47, 50, 52, 53, 60	AVDD (3.3V)	I	Analog DAC Supplies (3.3 V).
25, 26, 27	PS0 to PS2	I	Profile Select Pins. Digital inputs (active high). Use these pins to select one of eight phase/frequency profiles for the DDS. Changing the state of one of these pins transfers the current contents of all input/output buffers to the corresponding registers. State changes must be set up on the SYNC_CLK pin (Pin 82).
28, 29, 30, 31	F0 to F3	I	Function Pins. Digital inputs. The state of these pins determines if a serial or parallel interface is used. In addition, the function pins determine how the 32-bit parallel data-word is partitioned for FSK, PSK, or ASK modulation mode.
41	$\overline{AOUT}$	O	DAC Complementary Output Source. Analog output (voltage mode). Internally connected through a 50 Ω resistor to AVDD (3.3 V).
42	AOUT	O	DAC Output Source. Analog output (voltage mode). Internally connected through a 50 Ω resistor to AVDD (3.3 V).
45	DAC_BP	I	DAC Bypass Pin. Provides access to the common control node of the DAC current sources. Connecting a capacitor between this pin and ground can improve noise performance at the DAC output.
48	DAC_RSET	O	Analog Reference. This pin programs the DAC output full-scale reference current. Connect a 3.3 kΩ resistor to AGND.
54	$\overline{REF\_CLK}$	I	Complementary Reference Clock Input. Analog input.
55	REF_CLK	I	Reference Clock Input. Analog input.
58	LOOP_FILTER	O	External PLL Loop Filter Node.
59	REF	O	Local PLL Reference Supply. Typically at 2.05 V.
61	SYNC_OUT	O	Digital Synchronization Output. This pin synchronizes multiple chips.
62	SYNC_IN	I	Digital Synchronization Input. This pin synchronizes multiple chips.
63	DRCTL	I	Ramp Control. Digital input (active high). This pin controls the sweep direction (up/down).
64	DRHOLD	I	Ramp Hold. Digital input (active high). Pauses the sweep when active.
65	DROVER	O	Ramp Over. Digital output (active high). This pin switches to Logic 1 when the digital ramp generator reaches the programmed upper or lower limit.
66	OSK	I	Output Shift Keying. Digital input (active high). When the OSK features are placed in either manual or automatic mode, this pin controls the OSK function. In manual mode, it toggles the multiplier between 0 (low) and the programmed amplitude scale factor (high). In automatic mode, a low sweeps the amplitude down to zero and a high sweeps the amplitude up to the amplitude scale factor.

Pin No.	Mnemonic	I/O[1]	Description
67	EXT_PWR_DWN	I	External Power-Down. Digital input (active high). A high level on this pin initiates the currently programmed power-down mode.
82	SYNC_CLK	O	Clock Output. Digital output. Many of the digital inputs on the chip, such as I/O_UPDATE, PS[2:0], and the parallel data port (D0 to D31), must be set up on the rising edge of this signal.
85	MASTER_RESET	I	Master Reset. Digital input (active high). Clears all memory elements and sets registers to default values.
86	I/O_UPDATE	I	Input/Output Update. Digital input (active high). A high on this pin transfers the contents of the input/output buffers to the corresponding internal registers.
	EPAD		Exposed Pad. The EPAD must be soldered to ground.

[1] I = input, O = output.

TYPICAL PERFORMANCE CHARACTERISTICS

Nominal supply voltage; DAC R_{SET} = 3.3 kΩ, T_A = 25°C, unless otherwise noted.

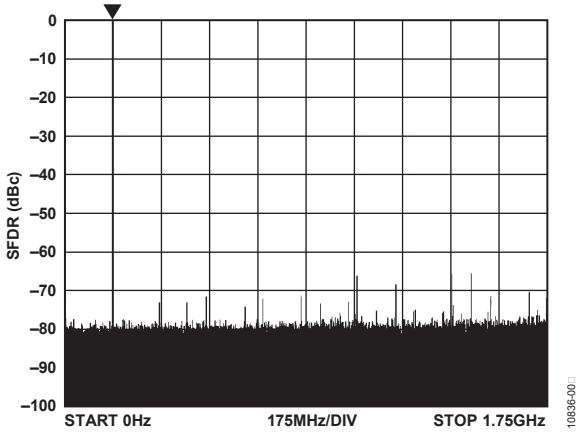


Figure 4. Wideband SFDR at 171.5 MHz SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

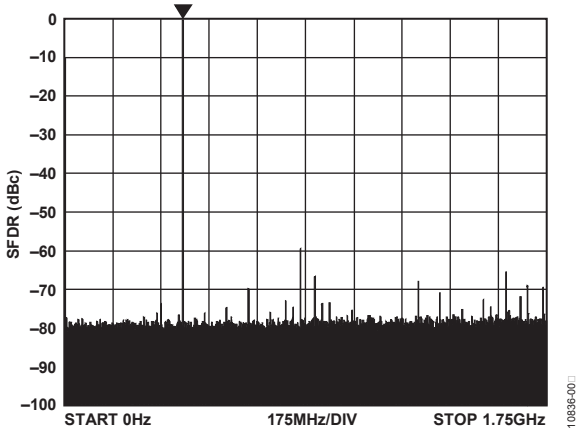


Figure 5. Wideband SFDR at 427.5 MHz SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

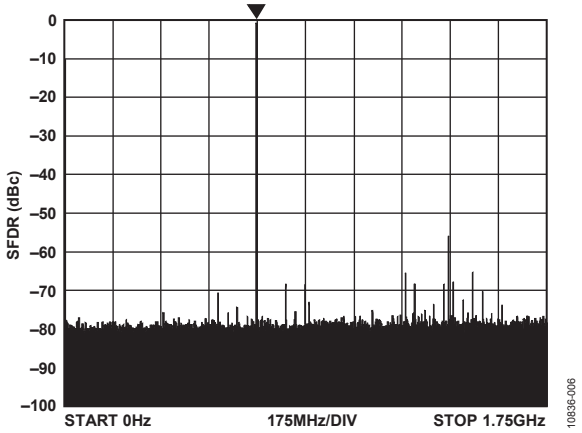


Figure 6. Wideband SFDR at 696.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

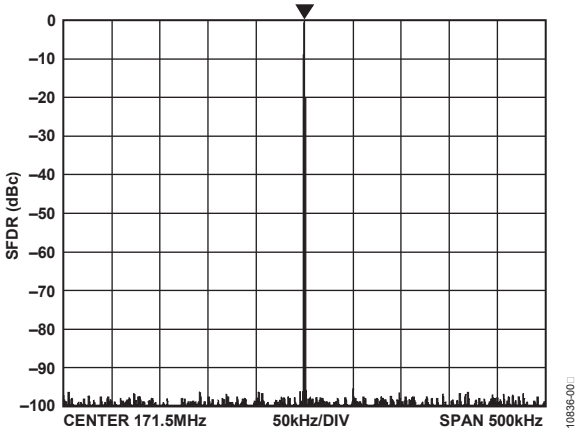


Figure 7. Narrow-Band SFDR at 171.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

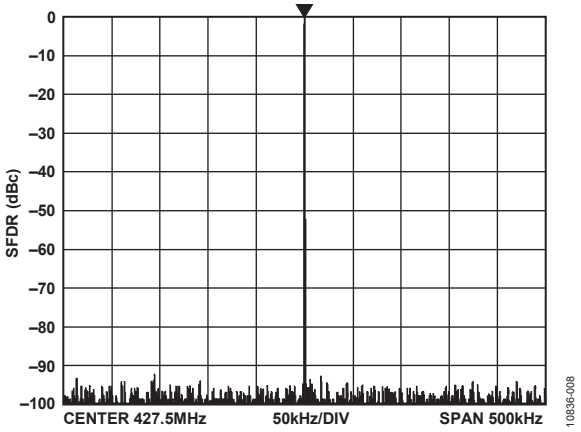


Figure 8. Narrow-Band SFDR at 427.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

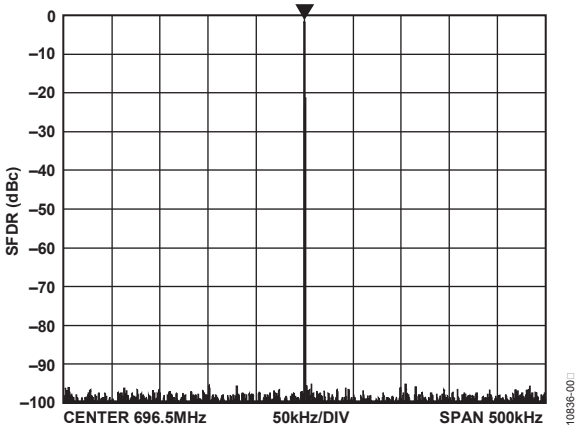


Figure 9. Narrow-Band SFDR at 696.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

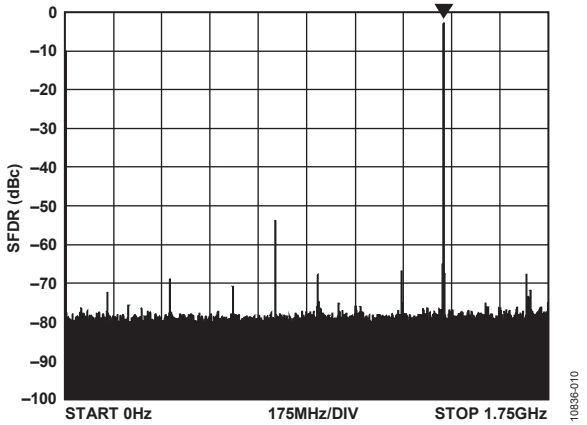


Figure 10. Wideband SFDR at 1396.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

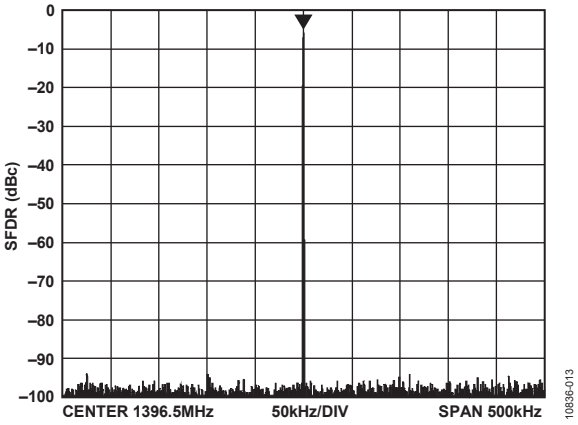


Figure 13. Narrow-Band SFDR at 1396.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

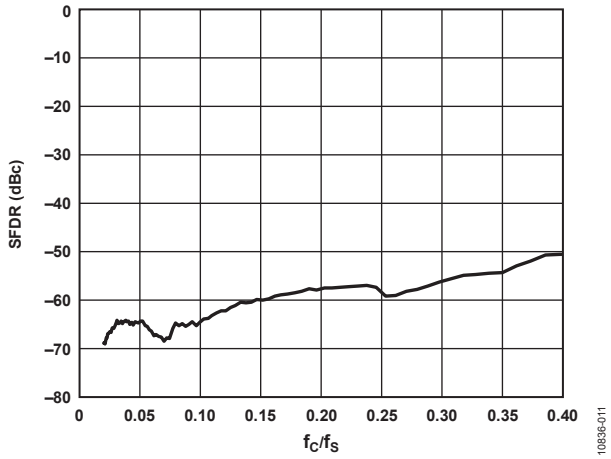


Figure 11. Wideband SFDR vs. Normalized f_{OUT} SYSCLK = 3.5 GHz

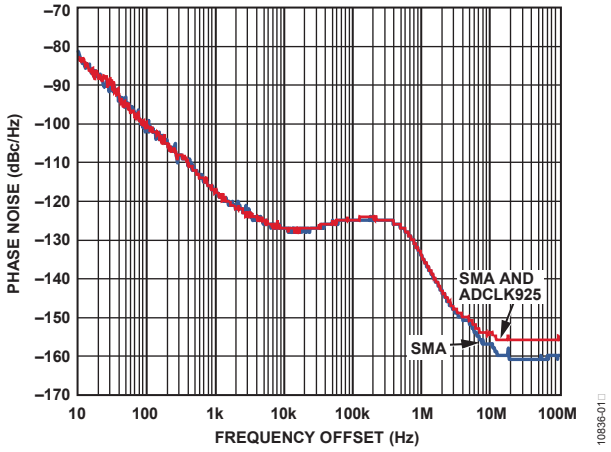


Figure 14. Absolute Phase Noise of REF CLK Source Driving AD9914 Rohde & Schwarz SMA100 Signal Generator at 3.5 GHz Buffered by Series ADCLK925

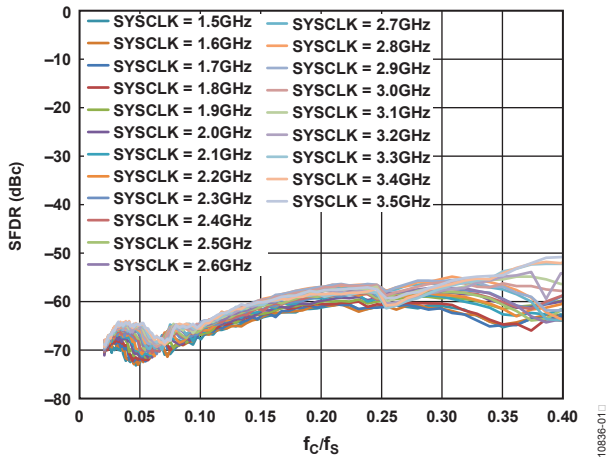


Figure 12. Wideband SFDR vs. Normalized f_{OUT}, SYSCLK = 2.5 GHz to 3.5 GHz

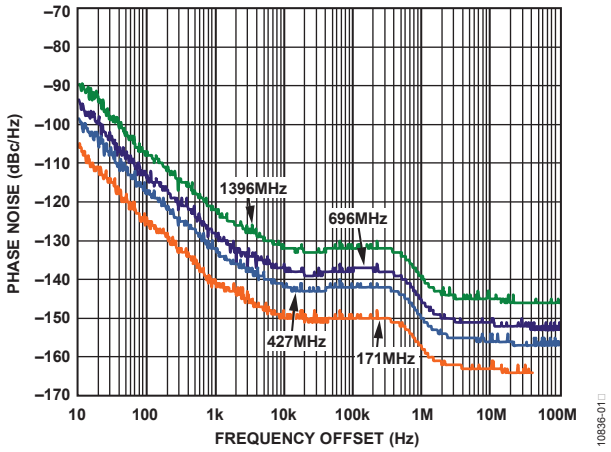


Figure 15. Absolute Phase Noise Curves of DDS Output at 3.5 GHz Operation

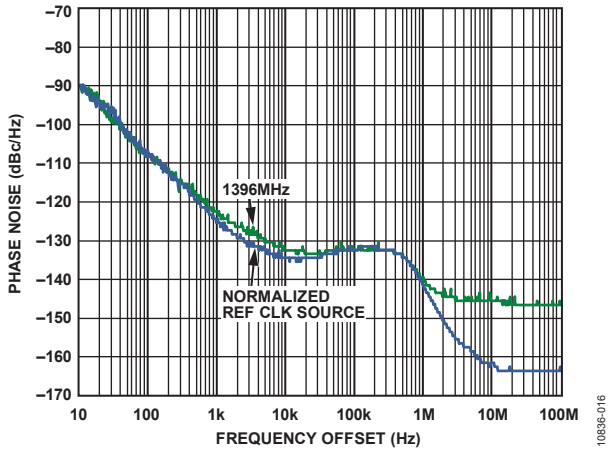


Figure 16. Absolute Phase Noise Curves of Normalized REF CLK Source to DDS Output at 1396 MHz (SYSCLK = 3.5 GHz)

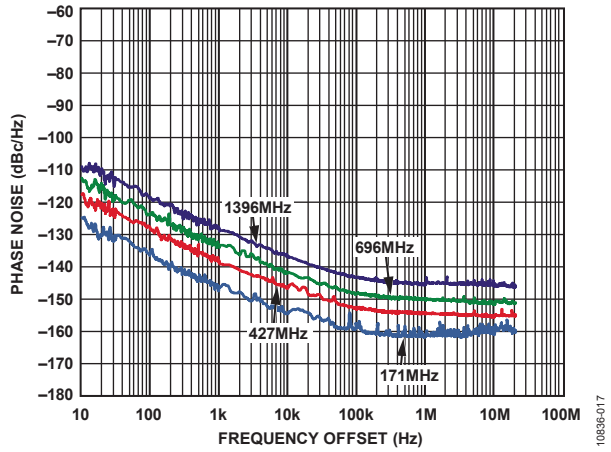


Figure 17. Residual Phase Noise Curves

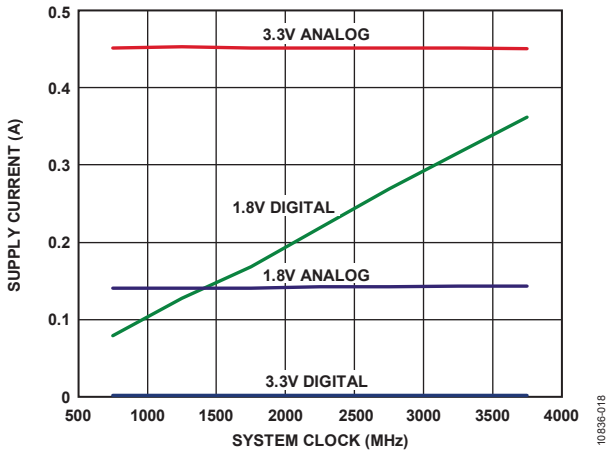


Figure 18. Power Supply Current vs. SYSCLK

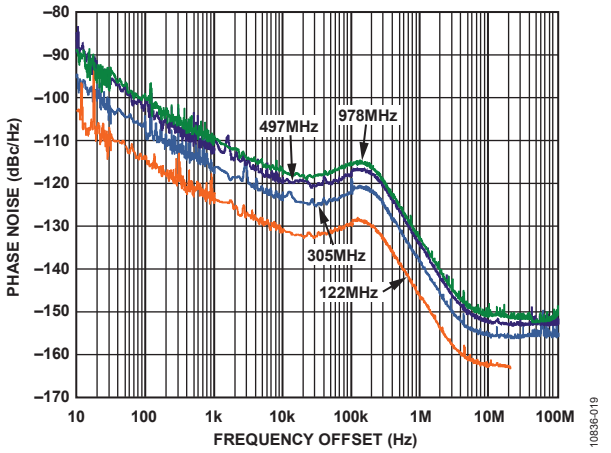


Figure 19. Absolute Phase Noise Curves of DDS Output Using Internal PLL at 2.5 GHz Operation

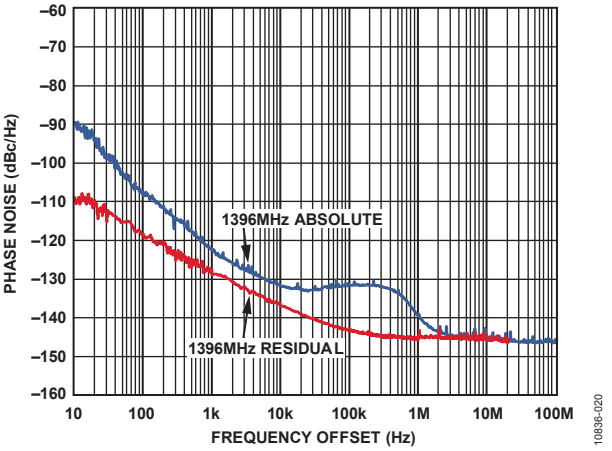


Figure 20. Residual PN vs. Absolute PN Measurement Curves at 1396 MHz

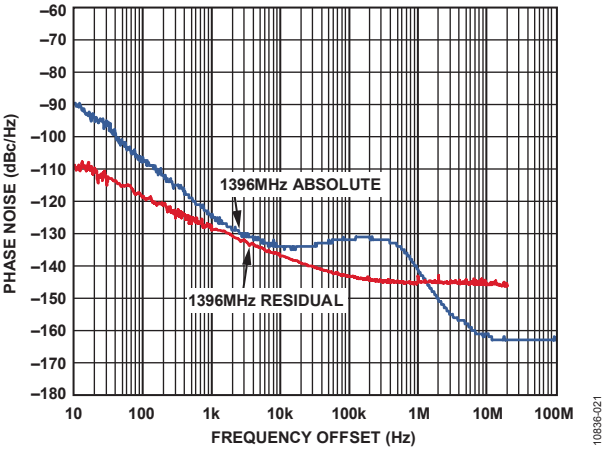


Figure 21. Residual Phase Noise vs. Normalized Absolute REF CLK Source Phase Noise at 1396 MHz

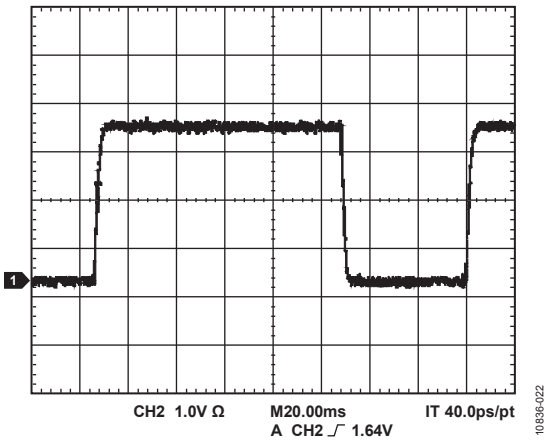


Figure 22. SYNC_OUT (f_{SYSCLK}/384)

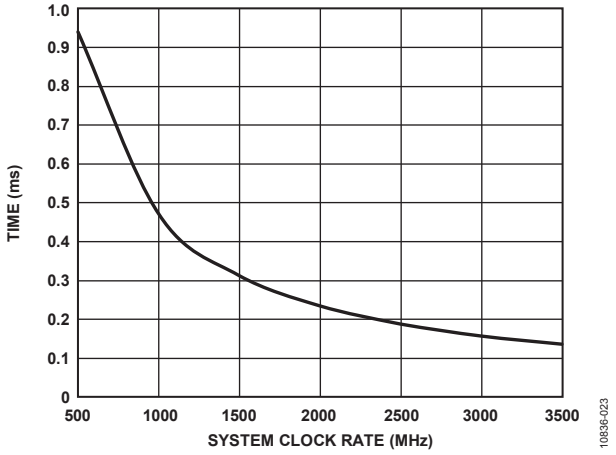


Figure 23. DAC Calibration Time vs. SYSCLK Rate. See the DAC Calibration Output Section for Formula.

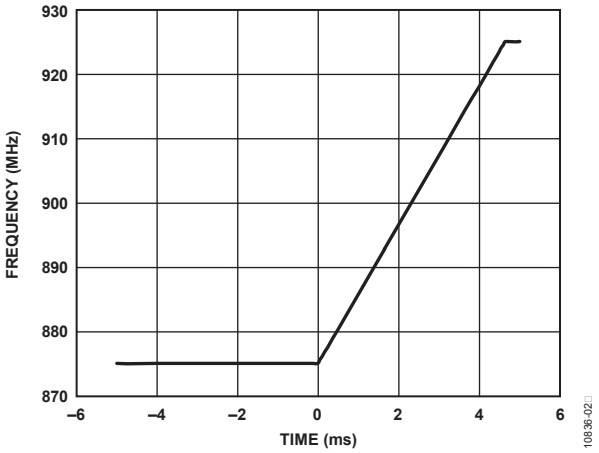


Figure 24. Measured Rising Linear Frequency Sweep

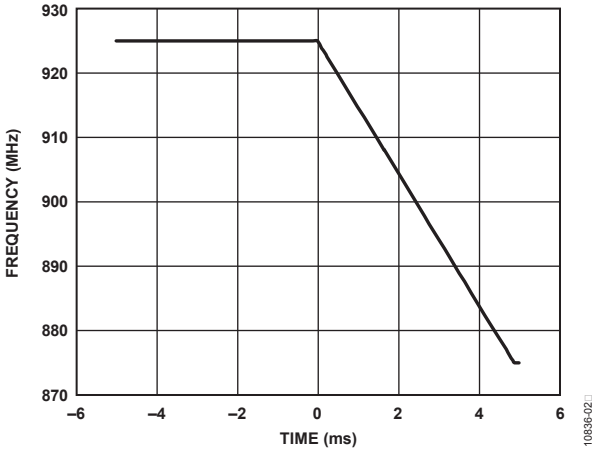


Figure 25. Measured Falling Linear Frequency Sweep

EQUIVALENT CIRCUITS

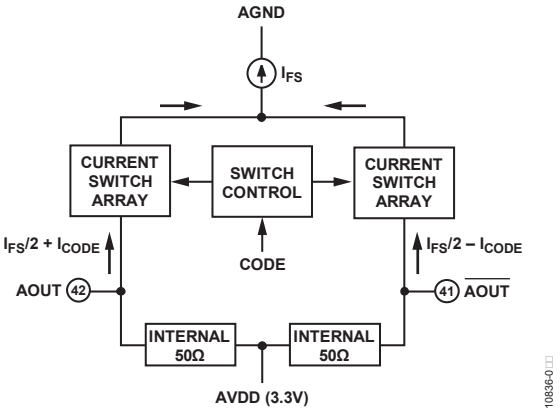


Figure 26. DAC Output

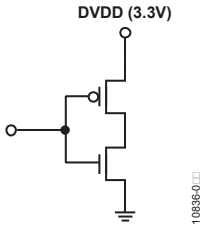


Figure 28. CMOS Input

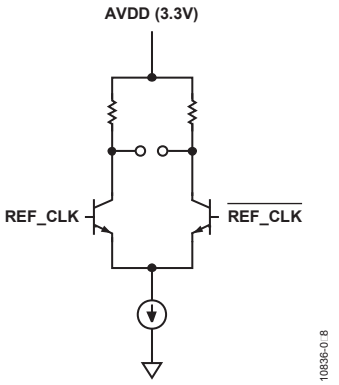


Figure 27. REF CLK input

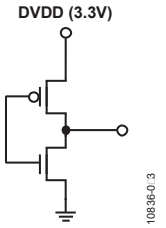


Figure 29. CMOS Output

THEORY OF OPERATION

The AD9914 has five modes of operation.

- Single tone
- Profile modulation
- Digital ramp modulation (linear sweep)
- Parallel data port modulation
- Programmable modulus mode

The modes define the data source supplies the DDS with the signal control parameters: frequency, phase, or amplitude. The partitioning of the data into different combinations of frequency, phase, and amplitude is established based on the mode and/or specific control bits and function pins.

Although the various modes are described independently, they can be enabled simultaneously. This provides an unprecedented level of flexibility for generating complex modulation schemes. However, to avoid multiple data sources from driving the same DDS signal control parameter, the device has a built-in priority protocol.

In single tone mode, the DDS signal control parameters come directly from the profile programming registers. In digital ramp modulation mode, the DDS signal control parameters are delivered by a digital ramp generator. In parallel data port modulation mode, the DDS signal control parameters are driven directly into the parallel port.

The various modulation modes generally operate on only one of the DDS signal control parameters (two in the case of the polar modulation format via the parallel data port). The unmodulated DDS signal control parameters are stored in programming registers and automatically routed to the DDS based on the selected mode.

A separate output shift keying (OSK) function is also available. This function employs a separate digital linear ramp generator that affects only the amplitude parameter of the DDS. The OSK function has priority over the other data sources that can drive the DDS amplitude parameter. As such, no other data source can drive the DDS amplitude when the OSK function is enabled.

SINGLE TONE MODE

In single tone mode, the DDS signal control parameters are supplied directly from the profile programming registers. A profile is an independent register that contains the DDS signal control parameters. Eight profile registers are available. Note that the profile pins must select the desired register.

PROFILE MODULATION MODE

Each profile is independently accessible. For FSK, PSK, or ASK modulation, use the three external profile pins (PS[2:0]) to select the desired profile. A change in the state of the profile pins with the next rising edge on SYNC_CLK updates the DDS with the parameters specified by the selected profile. Therefore, the profile change must meet the setup and hold times to the SYNC_CLK rising edge. Note that amplitude control must also be enabled using the OSK enable bit in the CFR1 register (0x00[8]).

DIGITAL RAMP MODULATION MODE

In digital ramp modulation mode, the modulated DDS signal control parameter is supplied directly from the digital ramp generator (DRG). The ramp generation parameters are controlled through the serial or parallel input/output port.

The ramp generation parameters allow the user to control both the rising and falling slopes of the ramp. The upper and lower boundaries of the ramp, the step size and step rate of the rising portion of the ramp, and the step size and step rate of the falling portion of the ramp are all programmable.

The ramp is digitally generated with 32-bit output resolution. The 32-bit output of the DRG can be programmed to affect frequency, phase, or amplitude. When programmed for frequency, all 32 bits are used. However, when programmed for phase or amplitude, only the 16 MSBs or 12 MSBs, respectively, are used.

The ramp direction (rising or falling) is externally controlled by the DRCTL pin. An additional pin (DRHOLD) allows the user to suspend the ramp generator in the present state. Note that amplitude control must also be enabled using the OSK enable bit in Register CFR1.

PARALLEL DATA PORT MODULATION MODE

In parallel data port modulation mode, the modulated DDS signal control parameter(s) are supplied directly from the 32-bit parallel data port. The function pins define how the 32-bit data-word is applied to the DDS signal control parameters. Formatting of the 32-bit data-word is unsigned binary, regardless of the destination.

Parallel Data Clock (SYNC_CLK)

The AD9914 generates a clock signal on the SYNC_CLK pin that runs at 1/24 of the DAC sample rate (the sample rate of the parallel data port). SYNC_CLK serves as a data clock for the parallel port.

PROGRAMMABLE MODULUS MODE

In programmable modulus mode, the DRG is used as an auxiliary accumulator to alter the frequency equation of the DDS core, making it possible to implement fractions that are not restricted to a power of 2 in the denominator. A standard DDS is restricted to powers of 2 as a denominator because the phase accumulator is a set of bits as wide as the frequency tuning word (FTW).

When in programmable modulus mode, however, the frequency equation is:

$$f_0 = (f_S)(FTW + A/B)/2^{32}$$

where $f_0/f_S < ½$, $0 \le FTW < 2^{31}$, $2 \le B \le 2^{32} - 1$, and $A < B$.

This equation implies a modulus of $B \times 2^{32}$ (rather than 2^{32}, in the case of a standard DDS). Furthermore, because B is programmable, the result is a DDS with a programmable modulus.

When in programmable modulus mode, the 32-bit auxiliary accumulator operates in a way that allows it to roll over at a value other than the full capacity of 2^{32}. That is, it operates with a modified modulus based on the programmable value of B. With each roll over of the auxiliary accumulator, a value of 1 LSB adds to the current accumulated value of the 32-bit phase accumulator. This behavior changes the modulus of the phase accumulator to B × 2^{32} (instead of 2^{32}), allowing it to synthesize the desired f_0.

To determine the programmable modulus mode register values for FTW, A, and B, the user must first define f_0/f_S as a ratio of relatively prime integers, M/N. That is, having converted f_0 and f_S to integers, M and N, reduce the fraction, M/N, to the lowest terms. Then, divide M × 232 by N. The integer part of this division operation is the value of FTW (Register 0x04[31:0]). The remainder, Y, of this division operation is

$$Y = (2^{32} \times M) - (FTW \times N)$$

The value of Y facilitates the determination of A and B by taking the fraction, Y/N, and reducing it to the lowest terms. Then, the numerator of the reduced fraction is A (Register 0x06[31:0]) and the denominator is the B (Register 0x05[31:0]).

For example, synthesizing precisely 300 MHz with a 1 GHz system clock is not possible with a standard DDS. It is possible, however, using programmable modulus as follows.

First, express f_0/f_S as a ratio of integers:

300,000,000/1,000,000,000

Reducing this fraction to lowest terms yields 3/10; therefore, M = 3 and N = 10. FTW is the integer part of (M × 2^{32})/N, or (3 × 2^{32})/10, which is 1,288,490,188 (0x4CCCCCCC in 32-bit hexadecimal notation). The remainder, Y, of (3 × 2^{32})/10, is (2^{32} × 3) − (1,288,490,188 × 10), which is 8. Therefore, Y/N is 8/10, which reduces to 4/5. Therefore, A = 4 and B = 5 (0x00000004 and 0x00000005 in 32-bit hexadecimal notation, respectively). Programming the AD9914 with these values of FTW, A, and B results in an output frequency that is exactly 3/10 of the system clock frequency.

MODE PRIORITY

The ability to activate each mode independently makes it possible to have multiple data sources attempting to drive the same DDS signal control parameter (frequency, phase, and amplitude). To avoid contention, the AD9914 has a built-in priority system. Table 6 summarizes the priority for each of the DDS modes. The data source column in Table 6 lists data sources for a particular DDS signal control parameter in descending order of precedence. For example, if the profile mode enable bit and the parallel data port enable bit (0x01[23:22]) are set to Logic 1 and both are programmed to source the frequency tuning word to DDS output, the profile modulation mode has priority over the parallel data port modulation mode.

Table 6. Data Source Priority

	DDS Signal Control Parameters	
Priority	**Data Source**	**Conditions**
Highest Priority	Programmable modulus	If programmable modulus mode is used to output frequency only, no other data source can control the output frequency in this mode. Note that the DRG is used in conjunction with programmable modulus mode; therefore, the DRG cannot be used to sweep phase or amplitude in programmable modulus mode. If output phase offset control is desired, enable profile mode and use the profile registers and profile pins accordingly to control output phase adjustment. If output amplitude control is desired, enable profile mode and use the profile registers and profile pins accordingly to control output amplitude adjustment. Note that the OSK enable bit must be set to control the output amplitude.
	DRG	The digital ramp modulation mode is the next highest priority mode. If the DRG is enabled to sweep output frequency, phase, or amplitude, the two parameters not being swept can be controlled independently via the profile mode.
	Profiles	The profile modulation mode is the next highest priority mode. Profile mode can control all three parameters independently, if desired.
Lowest Priority	Parallel port	Parallel data port modulation has the lowest priority but the most flexibility as far as changing any parameter at the high rate. See the Programming and Function Pins section.

FUNCTIONAL BLOCK DETAIL

DDS CORE

The direct digital synthesizer (DDS) block generates a reference signal (sine or cosine based on Register 0x00, Bit 16, the enable sine output bit). The parameters of the reference signal (frequency, phase, and amplitude) are applied to the DDS at the frequency, phase offset, and amplitude control inputs, as shown in Figure 30.

The output frequency (f_{OUT}) of the AD9914 is controlled by the frequency tuning word (FTW) at the frequency control input to the DDS. The relationship among f_{OUT}, FTW, and f_{SYSCLK} is given by

$$f_{OUT} = \left(\frac{FTW}{2^{32}}\right) f_{SYSCLK} \quad (1)$$

where *FTW* is a 32-bit integer ranging in value from 0 to 2,147,483,647 ($2^{31} - 1$), which represents the lower half of the full 32-bit range. This range constitutes frequencies from dc to Nyquist (that is, ½ f_{SYSCLK}).

The FTW required to generate a desired value of f_{OUT} is found by solving Equation 1 for FTW, as given in Equation 2.

$$FTW = \text{round}\left(2^{32}\left(\frac{f_{OUT}}{f_{SYSCLK}}\right)\right) \quad (2)$$

where the round(*x*) function rounds the argument (the value of x) to the nearest integer. This is required because the FTW is constrained to be an integer value. For example, for f_{OUT} = 41 MHz and f_{SYSCLK} = 122.88 MHz, FTW = 1,433,053,867 (0x556AAAAB).

Programming an FTW greater than 2^{31} produces an aliased image that appears at a frequency given by

$$f_{OUT} = \left(1 - \frac{FTW}{2^{32}}\right) f_{SYSCLK}$$

for FTW ≥ 2^{31}

The relative phase of the DDS signal can be digitally controlled by means of a 16-bit phase offset word (POW). The phase offset is applied prior to the angle to amplitude conversion block internal to the DDS core. The relative phase offset (Δθ) is given by

$$\Delta\theta = \begin{vmatrix} 2\pi\left(\frac{POW}{2^{16}}\right) \\ 360\left(\frac{POW}{2^{16}}\right) \end{vmatrix}$$

where the upper quantity is for the phase offset expressed as radian units and the lower quantity as degrees.

To find the POW value necessary to develop an arbitrary Δθ, solve the preceding equation for POW and round the result (in a manner similar to that described previously for finding an arbitrary FTW).

The relative amplitude of the DDS signal can be digitally scaled (relative to full scale) by means of a 12-bit amplitude scale factor (ASF). The amplitude scale value is applied at the output of the angle to amplitude conversion block internal to the DDS core. The amplitude scale is given by

$$Amplitude\ Scale = \begin{vmatrix} \frac{ASF}{2^{12}} \\ 20\log\left(\frac{ASF}{2^{12}}\right) \end{vmatrix} \quad (3)$$

where the upper quantity is amplitude expressed as a fraction of full scale and the lower quantity is expressed in decibels relative to full scale.

To find the ASF value necessary for a particular scale factor, solve Equation 3 for ASF and round the result (in a manner similar to that described previously for finding an arbitrary FTW).

When the AD9914 is programmed to modulate any of the DDS signal control parameters, the maximum modulation sample rate is 1/24 f_{SYSCLK}. This means that the modulation signal exhibits images at multiples of 1/24 f_{SYSCLK}. The impact of these images must be considered when using the device as a modulator.

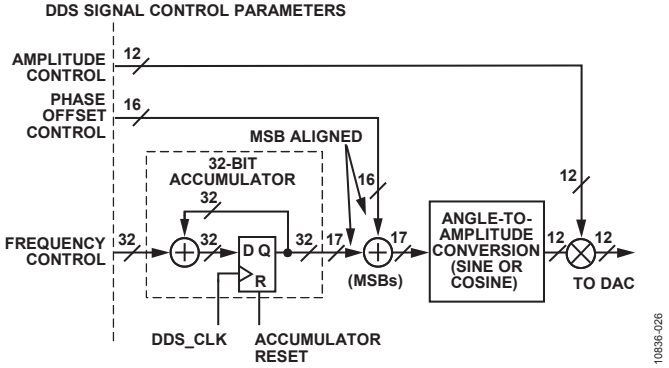


Figure 30. DDS Block Diagram

12-BIT DAC OUTPUT

The AD9914 incorporates an integrated 12-bit, current output DAC. The output current is delivered as a balanced signal using two outputs. The use of balanced outputs reduces the potential amount of common-mode noise present at the DAC output, offering the advantage of an increased signal-to-noise ratio. An external resistor (R_{SET}) connected between the DAC_RSET pin and AGND establishes the reference current. The recommended value of R_{SET} is 3.3 kΩ.

Attention must be paid to the load termination to keep the output voltage within the specified compliance range; voltages developed beyond this range cause excessive distortion and can damage the DAC output circuitry.

DAC CALIBRATION OUTPUT

The DAC CAL enable bit in the CFR4 control register (0x03[24]) must be manually set and then cleared after each power-up and every time the REF CLK or internal system clock is changed. This initiates an internal calibration routine to optimize the setup and hold times for internal DAC timing. Failure to calibrate may degrade performance and even result in loss of functionality. The length of time to calibrate the DAC clock is calculated from the following equation:

$$t_{CAL} = \frac{469{,}632}{f_S}$$

RECONSTRUCTION FILTER

The DAC output signal appears as a sinusoid sampled at f_S. The frequency of the sinusoid is determined by the frequency tuning word (FTW) that appears at the input to the DDS. The DAC output is typically passed through an external reconstruction filter that serves to remove the artifacts of the sampling process and other spurs outside the filter bandwidth.

Because the DAC constitutes a sampled system, the output must be filtered so that the analog waveform accurately represents the digital samples supplied to the DAC input. The unfiltered DAC output contains the desired baseband signal, which extends from dc to the Nyquist frequency ($f_S/2$). It also contains images of the baseband signal that theoretically extend to infinity. Notice that the odd numbered images (shown in Figure 31) are mirror images of the baseband signal. Furthermore, the entire DAC output spectrum is affected by a sin(x)/x response, which is caused by the sample-and-hold nature of the DAC output signal.

For applications using the fundamental frequency of the DAC output, the response of the reconstruction filter must preserve the baseband signal (Image 0), while completely rejecting all other images. However, a practical filter implementation typically exhibits a relatively flat pass band that covers the desired output frequency plus 20%, rolls off as steeply as possible, and then maintains significant (though not complete) rejection of the remaining images. Depending on how close unwanted spurs are to the desired signal, a third-, fifth-, or seventh-order elliptic low-pass filter is common.

Some applications operate from an image above the Nyquist frequency, and those applications use a band-pass filter instead of a low-pass filter. The design of the reconstruction filter has a significant impact on the overall signal performance. Therefore, good filter design and implementation techniques are important for obtaining the best possible jitter results.

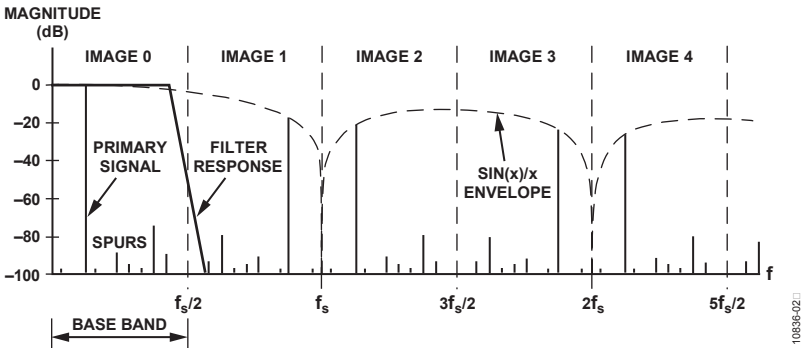


Figure 31. DAC Spectrum vs. Reconstruction Filter Response

CLOCK INPUT (REF_CLK/$\overline{\text{REF\_CLK}}$)

REF_CLK/$\overline{\text{REF\_CLK}}$ Overview

The AD9914 supports a number of options for producing the internal SYSCLK signal (that is, the DAC sample clock) via the REF_CLK/$\overline{\text{REF\_CLK}}$ input pins. The REF_CLK input can be driven directly from a differential or single-ended source. There is also an internal phase-locked loop (PLL) multiplier that can be independently enabled. However, the PLL limits the SYSCLK signal between 2.4 GHz and 2.5 GHz operation. A differential signal is recommended when the PLL is bypassed. A block diagram of the REF_CLK functionality is shown in Figure 32. Figure 32 also shows how the CFR3 control bits are associated with specific functional blocks.

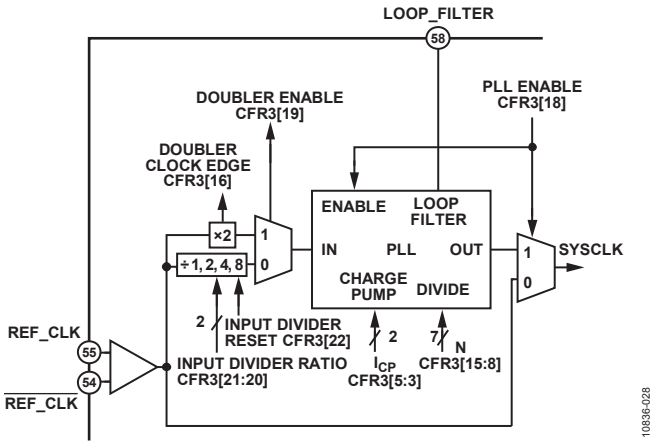


Figure 32. REF_CLK Block Diagram

The PLL enable bit chooses between the PLL path or the direct input path. When the direct input path is selected, the REF_CLK/$\overline{\text{REF\_CLK}}$ pins must be driven by an external signal source (single-ended or differential). Input frequencies up to 3.5 GHz are supported.

Direct Driven REF_CLK/$\overline{\text{REF\_CLK}}$

With a differential signal source, the REF_CLK/$\overline{\text{REF\_CLK}}$ pins are driven with complementary signals and ac-coupled with 0.1 µF capacitors. With a single-ended signal source, either a single-ended-to-differential conversion can be employed or the REF_CLK input can be driven single-ended directly. In either case, 0.1 µF capacitors ac couples both REF_CLK/ $\overline{\text{REF\_CLK}}$ pins to avoid disturbing the internal dc bias voltage of ~1.35 V. See Figure 33 for more details.

The REF_CLK/$\overline{\text{REF\_CLK}}$ input resistance is ~2.5 kΩ differential (~1.2 kΩ single-ended). Most signal sources have relatively low output impedances. The REF_CLK/$\overline{\text{REF\_CLK}}$ input resistance is relatively high; therefore, the effect on the termination impedance is negligible and can usually be chosen to be the same as the output impedance of the signal source. The bottom two examples in Figure 33 assume a signal source with a 50 Ω output impedance.

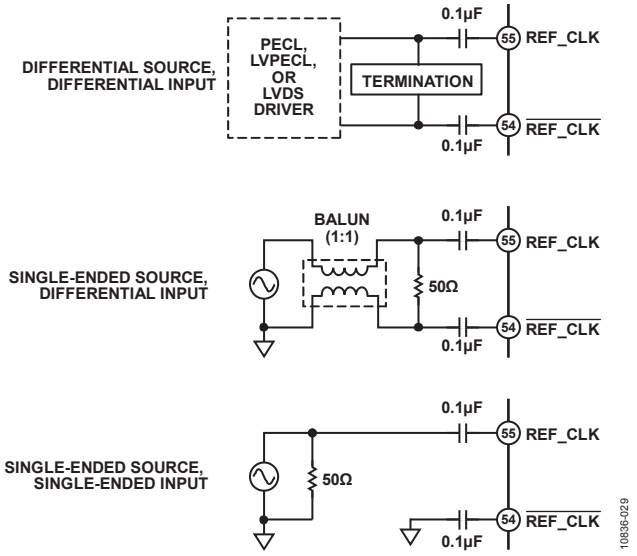


Figure 33. Direct Connection Diagram

Phase-Locked Loop (PLL) Multiplier

An internal PLL provides the option to use a reference clock frequency that is significantly lower than the system clock frequency. The PLL supports a wide range of programmable even frequency multiplication factors (20× to 510×) as well as a programmable charge pump current and external loop filter components (connected via the PLL LOOP_FILTER pin). These features add an extra layer of flexibility to the PLL, allowing optimization of phase noise performance and flexibility in frequency plan development. The PLL is also equipped with a PLL lock bit indicator (0x1B[24]).

The PLL output frequency range (f_{SYSCLK}) is constrained to the range of 2.4 GHz ≤ f_{SYSCLK} ≤ 2.5 GHz by the internal VCO.

VCO Calibration

When using the PLL to generate the system clock, VCO calibration is required to tune the VCO appropriately and achieve good performance. When the reference input signal is stable, the VCO cal enable bit in the CFR1 register, 0x00[24], must be asserted. Subsequent VCO calibrations require that the VCO calibration bit be cleared prior to initiating another VCO calibration. VCO calibration must occur before DAC calibration to ensure optimal performance and functionality.

PLL Charge Pump/Total Feedback Divider

The charge pump current (I_{CP}) value is automatically chosen via the VCO calibration process and N value (N = 10 to 255) stored in Feedback Divider N[7:0] in the CFR3 register (0x02[15:8]). N values below 10 must be avoided.

Note that the total PLL multiplication value for the PLL is always 2N due to the fixed divide by 2 element in the feedback path. This is shown in Figure 34. This fixed divide by 2 element forces only even PLL multiplication.

To manually override the charge pump current value, the manual I_{CP} selection bit in CFR3 (0x02[6]) must be set to Logic 1. This provides the user with additional flexibility to optimize the PLL performance. Table 7 lists the bit settings vs. the nominal charge pump current.

Table 7. PLL Charge Pump Current

I_{CP} Bits (CFR3[5:3])	Charge Pump Current, I_{CP} (µA)
000	125
001	250
010	375
011	500 (default)
100	625
101	750
110	875
111	1000

Table 8. N Divider vs. Charge Pump Current

N Divider Range	Recommended Charge Pump Current, I_{CP} (µA)
10 to 15	125
16 to 23	250
24 to 35	375
36 to 43	500
44 to 55	625
56 to 63	750
64 to 79	875
80 to 100	1000

PLL Loop Filter Components

The loop filter is mostly internal to the device, as shown in Figure 34. The recommended external capacitor value is 560 pF. Because C_P and R_{PZ} are integrated, it is not recommended to adjust the loop bandwidth via the external capacitor value. The better option is to adjust the charge pump current even though it is a coarse adjustment.

For example, suppose the PLL is manually programmed such that I_{CP} = 375 µA, K_V = 60 MHz/V, and N = 25. This produces a loop bandwidth of approximately 250 kHz.

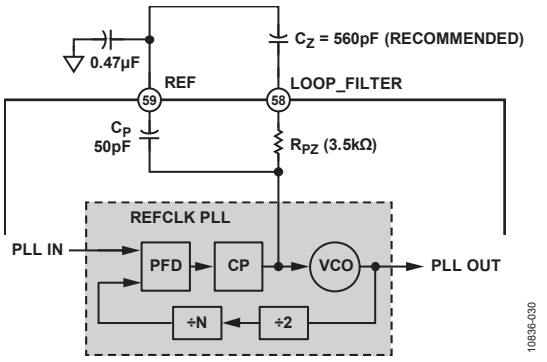


Figure 34. REF CLK PLL External Loop Filter

PLL LOCK INDICATION

When the PLL is in use, the PLL lock bit (0x1B[24])provides an active high indication that the PLL has locked to the REF CLK input signal.

OUTPUT SHIFT KEYING (OSK)

The OSK function (see Figure 35) allows the user to control the output signal amplitude of the DDS. The amplitude data generated by the OSK block has priority over any other functional block that is programmed to deliver amplitude data to the DDS. Therefore, the OSK data source, when enabled, overrides all other amplitude data sources.

The operation of the OSK function is governed by two CFR1 register bits, OSK enable (0x00[8]) and external OSK enable (0x00[9]), the external OSK pin, the profile pins, and the 12 bits of amplitude scale factor found in one of eight profile registers. The profile pins select the profile register containing the desired amplitude scale factor.

The primary control for the OSK block is the OSK enable bit (0x00[8]). When the OSK function is disabled, the OSK input controls and OSK pin are ignored.

The OSK pin functionality depends on the state of the external OSK enable bit and the OSK enable bit. When both bits are set to Logic 1 and the OSK pin is Logic 0, the output amplitude is forced to 0; otherwise, if the OSK pin is Logic 1, the output amplitude is set by the amplitude scale factor value in one of eight profile registers depending on the profile pin selection.

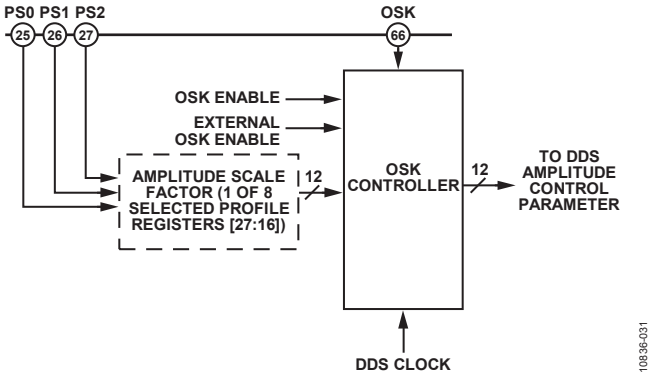


Figure 35. OSK Block Diagram

DIGITAL RAMP GENERATOR (DRG)

DRG Overview

To sweep phase, frequency, or amplitude from a defined start point to a defined endpoint, a completely digital ramp generator is included in the AD9914. The DRG makes use of eight control register bits, three external pins, and five 32-bit registers (see Figure 36).

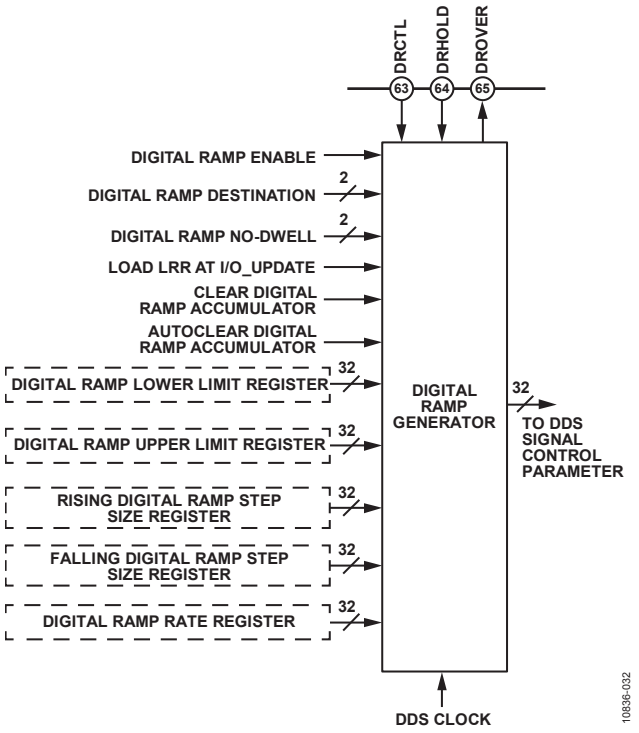


Figure 36. Digital Ramp Block Diagram

The primary control for the DRG is the digital ramp enable bit (0x01[19]). When disabled, the other DRG input controls are ignored and the internal clocks are shut down to conserve power.

The output of the DRG is a 32-bit unsigned data bus that can be routed to any one of the three DDS signal control parameters, as controlled by the two digital ramp destination bits in Control Function Register 2 according to Table 9. The 32-bit output bus is MSB-aligned with the 32-bit frequency parameter, the 16-bit phase parameter, or the 12-bit amplitude parameter, as defined by the destination bits. When the destination is phase or amplitude, the unused LSBs are ignored.

Table 9. Digital Ramp Destination

Digital Ramp Destination Bits (CFR2[21:20])	DDS Signal Control Parameter	Bits Assigned to DDS Parameter
00	Frequency	31:0
01	Phase	31:18
1x[1]	Amplitude	31:20

[1] x = don't care.

The ramp characteristics of the DRG are fully programmable. This includes the upper and lower ramp limits, and independent control of the step size and step rate for both the positive and negative slope characteristics of the ramp. A detailed block diagram of the DRG is shown in Figure 37.

The direction of the ramping function is controlled by the DRCTL pin. Logic 0 on this pin causes the DRG to ramp with a negative slope, whereas Logic 1 causes the DRG to ramp with a positive slope.

The DRG also supports a hold feature controlled via the DRHOLD pin. When this pin is set to Logic 1, the DRG is stalled at the last state; otherwise, the DRG operates normally. The DDS signal control parameters that are not the destination of the DRG are taken from the active profile.

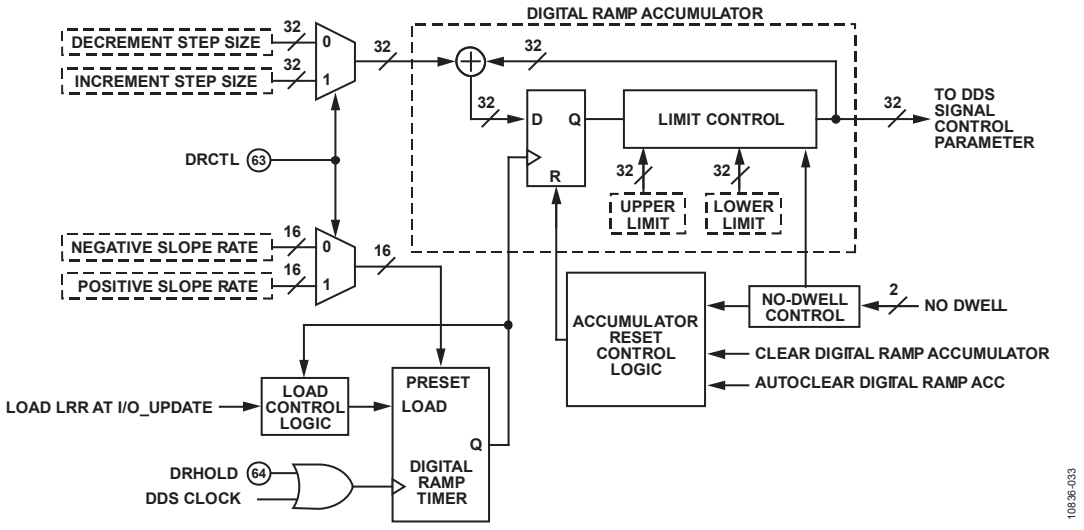


Figure 37. Digital Ramp Generator Detail

DRG Slope Control

The core of the DRG is a 32-bit accumulator clocked by a programmable timer. The time base for the timer is the DDS clock, which operates at 1/24 f_{SYSCLK}. The timer establishes the interval between successive updates of the accumulator. The positive (+Δt) and negative (−Δt) slope step intervals are independently programmable as given by

$$+\Delta t = \frac{24P}{f_{SYSCLK}}$$

$$-\Delta t = \frac{24N}{f_{SYSCLK}}$$

where *P* and *N* are the two 16-bit values stored in the 32-bit digital ramp rate register and control the step interval. N defines the step interval of the negative slope portion of the ramp. P defines the step interval of the positive slope portion of the ramp.

The step size of the positive ($STEP_P$) and negative ($STEP_N$) slope portions of the ramp are 32-bit values programmed into the 32-bit rising and falling digital ramp step size registers (0x06 and 0x07). Program each of the step sizes as an unsigned integer (the hardware automatically interprets $STEP_N$ as a negative value). The relationship between the 32-bit step size values and actual units of frequency, phase, or amplitude depend on the digital ramp destination bits. Calculate the actual frequency, phase, or amplitude step size by substituting $STEP_N$ or $STEP_P$ for M in the following equations as required:

$$Frequency\ Step = \left(\frac{M}{2^{32}}\right) f_{SYSCLK}$$

$$PhaseStep = \frac{\pi M}{2^{31}} \quad \text{(radians)}$$

$$PhaseStep = \frac{45M}{2^{29}} \quad \text{(degrees)}$$

$$Amplitude\ Step = \left(\frac{M}{2^{32}}\right) I_{FS}$$

Note that the frequency units are the same as those that represent f_{SYSCLK} (MHz, for example). The amplitude units are the same as those that represent I_{FS}, the full-scale output current of the DAC (mA, for example).

The phase and amplitude step size equations yield the average step size. Although the step size accumulates with 32-bit precision, the phase or amplitude destination exhibits only 16 bits or 12 bits, respectively. Therefore, at the destination, the actual phase or amplitude step is the accumulated 32-bit value truncated to 16 bits or 12 bits, respectively.

As described previously, the step interval is controlled by a 16-bit programmable timer. There are three events that can cause this timer to be reloaded prior to the expiration. One event occurs when the digital ramp enable bit transitions from cleared to set, followed by an input/output update. A second event is a change of state in the DRCTL pin. The third event is enabled using the load LRR at input/output update bit (0x00[15]).

DRG Limit Control

The ramp accumulator is followed by limit control logic that enforces an upper and lower boundary on the output of the ramp generator. Under no circumstances does the output of the DRG exceed the programmed limit values while the DRG is enabled. The limits are set through the 64-bit digital ramp limit register. Note that the upper limit value must be greater than the lower limit value to ensure normal operation.

DRG Accumulator Clear

The ramp accumulator can be cleared (that is, reset to 0) under program control. When the ramp accumulator is cleared, it forces the DRG output to the lower limit programmed into the digital ramp limit register.

With the limit control block embedded in the feedback path of the accumulator, resetting the accumulator is equivalent to presetting it to the lower limit value.