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12-Bit CCD Signal Processor with V-Driver and *Precision Timing* Generator

AD9920A

FEATURES

Integrated 19-channel V-driver
1.8 V AFETG core
24 programmable vertical clock signals
Correlated double sampler (CDS) with −3 dB, 0 dB, +3 dB, and +6 dB gain
12-bit, 40.5 MHz analog-to-digital converter (ADC)
Black level clamp with variable level control
Complete on-chip timing generator
***Precision Timing* core with ~400 ps resolution**
On-chip 3 V horizontal and RG drivers
General-purpose outputs (GPOs) for shutter and system support
On-chip sync generator with external sync input
On-chip 1.8 V low dropout (LDO) regulator
105-ball, 8 mm × 8 mm CSP_BGA package

APPLICATIONS

Digital still cameras

GENERAL DESCRIPTION

The AD9920A is a highly integrated charge-coupled device (CCD) signal processor for digital still camera applications. It includes a complete analog front end (AFE) with analog-to-digital conversion, combined with a full-function programmable timing generator and 19-channel vertical driver (V-driver). The timing generator is capable of supporting up to 24 vertical clock signals to control advanced CCDs. The on-chip V-driver supports up to 19 channels for use with six-field CCDs. A *Precision Timing*® core allows adjustment of high speed clocks with approximately 400 ps resolution at 40.5 MHz operation. The AD9920A also contains six GPOs that can be used for shutter and system functions.

The analog front end includes black level clamping, variable gain CDS, and a 12-bit ADC. The timing generator provides all the necessary CCD clocks: RG, H-clocks, V-clocks, sensor gate pulses, substrate clock, and substrate bias control.

The AD9920A is specified over an operating temperature range of −25°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

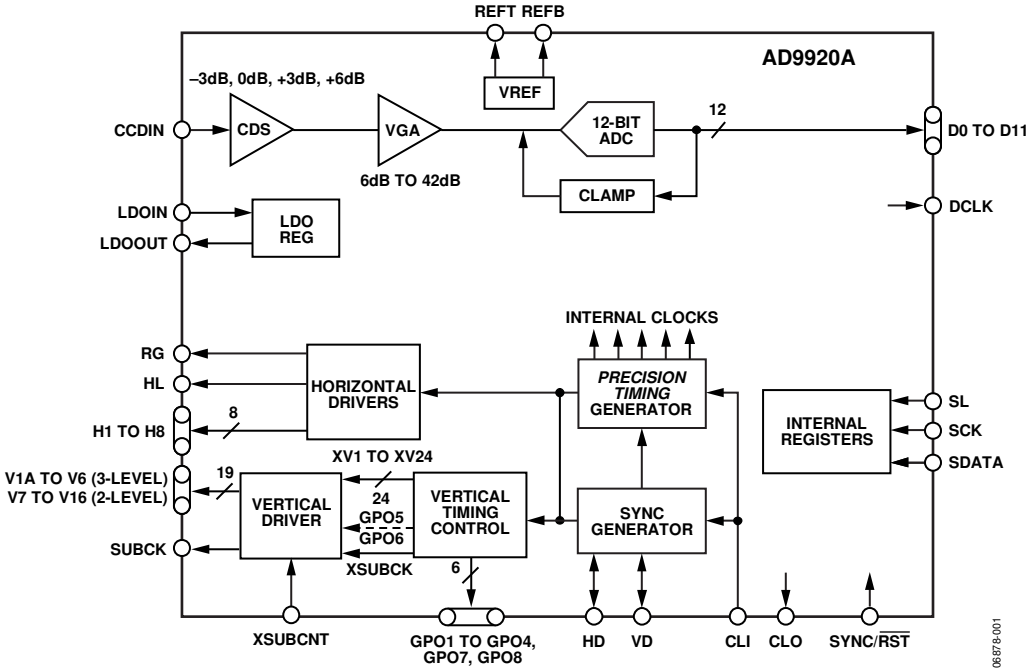

Figure 1.

Rev. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
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View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- AD9920A: 12-Bit CCD Signal Processor with V-Driver and *Precision Timing* Generator Data Sheet

DESIGN RESOURCES

- AD9920A Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9920A EngineerZone Discussions.

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Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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REVISION HISTORY

6/10—Rev. A to Rev. B

6/09—Revision A: Initial Version

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
TEMPERATURE RANGE					
Operating		−25		+85	°C
Storage		−65		+150	°C
POWER SUPPLY VOLTAGE INPUTS					
AVDD	AFE analog supply	1.6	1.8	2.0	V
TCVDD	Timing core supply	1.6	1.8	2.0	V
CLIVDD	CLI input supply	1.6	3.0	3.6	V
RGVDD	RG, HL driver supply	2.1	3.0	3.6	V
HVDD1 and HVDD2	H1 to H8 driver supplies	2.1	3.0	3.6	V
DVDD	Digital logic supply	1.6	1.8	2.0	V
DRVDD	Parallel data output driver supply	1.6	3.0	3.6	V
IOVDD	Digital I/O supply	1.6	3.0	3.6	V
V-DRIVER POWER SUPPLY VOLTAGES					
VDVDD	V-driver/logic supply	1.6	3.0	3.6	V
VH1, VH2	V-driver high supply	11.0	15.0	16.5	V
VL1, VL2	V-driver low supply	−8.5	−7.5	−5.5	V
VM1, VM2	V-driver midsupply	−1.5	0.0	+1.5	V
VLL	SUBCK low supply	−11.0	−7.5	−5.5	V
VH1, VH2 to VL1, VL2, VLL				23.5	V
VMM[1]	SUBCK midsupply	VLL	0.0	VDVDD	V
LDO[2]					
LDOIN	LDO supply input	2.5	3.0	3.6	V
Output Voltage		1.8	1.9	2.05	V
Output Current		60	100		mA
POWER SUPPLY CURRENTS—40.5 MHz OPERATION					
AVDD	1.8 V		27		mA
TCVDD	1.8 V		5		mA
CLIVDD	3 V		1.5		mA
RGVDD	3.3 V, 20 pF RG load, 20 pF HL load		10		mA
HVDD1 and HVDD2[3]	3.3 V, 480 pF total load on H1 to H8		59		mA
DVDD	1.8 V		9.5		mA
DRVDD	3 V, 10 pF load on each data output pin (D0 to D11)		6		mA
IOVDD	3 V, depends on load and output frequency of digital I/O		2		mA
POWER SUPPLY CURRENTS—STANDBY MODE OPERATION					
Standby1 Mode			20		mA
Standby2 Mode			5		mA
Standby3 Mode			1.5		mA
MAXIMUM CLOCK RATE (CLI)		40.5			MHz
MINIMUM CLOCK RATE (CLI)			10		MHz

[1] VMM must be greater than VLL and less than VDVDD.
[2] LDO should be used only for the AD9920A 1.8 V supplies, not for external circuitry.
[3] The total power dissipated by the HVDD (or RGVDD) can be approximated using the following equation:
Total HVDD Power = (C_L × *HVDD* × *Pixel Frequency*) × *HVDD*

DIGITAL SPECIFICATIONS

IOVDD = 1.6 V to 3.6 V, RGVDD = HVDD1 and HVDD2 = 2.7 V to 3.6 V, C_L = 20 pF, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS (IOVDD)						
High Level Input Voltage	V_{IH}		V_{DD} − 0.6			V
Low Level Input Voltage	V_{IL}				0.6	V
High Level Input Current	I_{IH}			10		µA
Low Level Input Current	I_{IL}			10		µA
Input Capacitance	C_{IN}			10		pF
LOGIC OUTPUTS (IOVDD, DRVDD)						
High Level Output Voltage	V_{OH}	I_{OH} = 2 mA	V_{DD} − 0.5			V
Low Level Output Voltage	V_{OL}	I_{OL} = 2 mA			0.5	V
RG and H-DRIVER OUTPUTS (HVDD1, HVDD2, and RGVDD)						
High Level Output Voltage	V_{OH}	Maximum current	V_{DD} − 0.5			V
Low Level Output Voltage	V_{OL}	Maximum current			0.5	V
Maximum H1 to H8 Output Current		Programmable	30			mA
Maximum HL and RG Output Current		Programmable	17			mA
Maximum Load Capacitance		Each output	60			pF
CLI INPUT		With CLO oscillator disabled				
High Level Input Voltage	V_{IHCLI}		CLIVDD/2 + 0.5			V
Low Level Input Voltage	V_{ILCLI}				CLIVDD/2 − 0.5	V

ANALOG SPECIFICATIONS

AVDD = 1.8 V, f_{CLI} = 40.5 MHz, typical timing specifications, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CDS[1]					
DC Restore	AVDD − 0.5 V	1.21	1.3	1.44	V
Allowable CCD Reset Transient	Limit is the lower of AVDD + 0.3 V or 2.2 V		0.5	0.8	V
CDS Gain Accuracy	VGA gain = 6.3 dB (Code 15, default value)				
−3 dB CDS Gain		−3.1	−2.6	−2.1	dB
0 dB CDS Gain		−0.6	−0.1	+0.4	dB
+3 dB CDS Gain		2.7	3.2	3.7	dB
+6 dB CDS Gain		5.2	5.7	6.2	dB
Maximum Input Range Before Saturation					
−3 dB CDS Gain			1.4		V p-p
0 dB CDS Gain			1.0		V p-p
+3 dB CDS Gain			0.7		V p-p
+6 dB CDS Gain			0.5		V p-p
Allowable OB Pixel Amplitude[1]					
0 dB CDS Gain (Default)		−100		+200	mV
+6 dB CDS Gain		−50		+100	mV
VARIABLE GAIN AMPLIFIER (VGA)					
Gain Control Resolution			1024		Steps
Gain Monotonicity			Guaranteed		
Gain Range					
Low Gain	VGA Code 15, default		6.3		dB
Maximum Gain	VGA Code 1023		42.4		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
BLACK LEVEL CLAMP					
Clamp Level Resolution			1024		Steps
Clamp Level	Measured at ADC output				
Minimum Clamp Level	Code 0		0		LSB
Maximum Clamp Level	Code 1023		255		LSB
ADC					
Resolution		12			Bits
Differential Nonlinearity (DNL)[2]			±0.5		LSB
No Missing Codes			Guaranteed		
Integral Nonlinearity (INL)[2]			±3.0		LSB
Full-Scale Input Voltage			2.0		V
VOLTAGE REFERENCE					
Reference Top Voltage (REFT)			1.4		V
Reference Bottom Voltage (REFB)			0.4		V
SYSTEM PERFORMANCE	Includes entire signal chain				
Gain Accuracy	0 dB CDS gain				
Low Gain	VGA Code 15 Gain = (0.0358 × code) + 5.76 dB	5.7	6.2	6.7	dB
Maximum Gain	VGA Code 1023	41.8	42.3	42.8	dB
Peak Nonlinearity, 1 V Input Signal[2]	6 dB VGA gain, 0 dB CDS gain applied		0.1	0.3	%
Total Output Noise[2]	AC-grounded input, 6 dB VGA gain applied		0.6		LSB rms
Power Supply Rejection (PSR)[2]	Measured with step change on supply		40		dB

[1] Input signal characteristics are defined as shown in Figure 2.
[2] See the Terminology section.

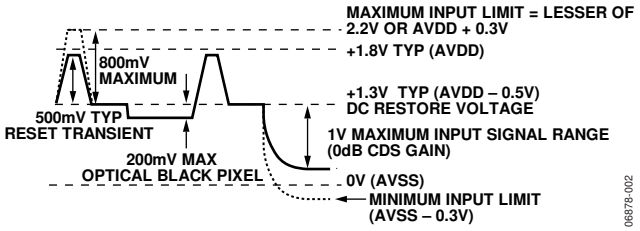


Figure 2. Input Signal Characteristics

TIMING SPECIFICATIONS

C_L = 20 pF, AVDD = DVDD = TCVDD = 1.8 V, f_{CLI} = 40.5 MHz, unless otherwise noted.

Table 4.

Parameter	Test Conditions/ Comments	Symbol	Min	Typ	Max	Unit
MASTER CLOCK	See Figure 18					
CLI Clock Period		t_{CONV}	24.7			ns
CLI High/Low Pulse Width			0.8 × t_{CONV}/2	t_{CONV}/2	1.2 × t_{CONV}/2	ns
Delay from CLI Rising Edge to Internal Pixel Position 0		t_{CLIDLY}		6		ns
SLAVE MODE SPECIFICATIONS	See Figure 105					
VD Falling Edge to HD Falling Edge		t_{VDHD}	0		VD period − t_{CONV}	ns
HD Falling Edge to CLI Rising Edge	Only valid if OSC_$\overline{RST}$ = 0	t_{HDCLI}	3		t_{CONV} − 2	ns
HD Falling Edge to CLO Rising Edge	Only valid if OSC_$\overline{RST}$ = 1	t_{HDCLO}	3		t_{CONV} − 2	ns
CLI Rising Edge to SHPLOC	Internal sample edge	t_{CLISHP}	3		t_{CONV} − 2	ns
AFE						
SHPLOC Sample Edge to SHDLOC Sample Edge	See Figure 23	t_{S1}	0.8 × t_{CONV}/2	t_{CONV}/2	t_{CONV} − t_{S2}	ns
SHDLOC Sample Edge to SHPLOC Sample Edge	See Figure 23	t_{S2}	0.8 × t_{CONV}/2	t_{CONV}/2	t_{CONV} − t_{S1}	ns
AFE Pipeline Delay	See Figure 26			16		Cycles
AFE CLPOB Pulse Width			2	20		Pixels
DATA OUTPUTS						
Output Delay from DCLK Rising Edge	See Figure 25	t_{OD}		1		ns
Pipeline Delay from SHP/SHD Sampling to Data Output				16		Cycles
SERIAL INTERFACE						
Maximum SCK Frequency	Must not exceed CLI frequency	f_{SCLK}	40.5			MHz
SL to SCK Setup Time		t_{LS}	10			ns
SCK to SL Hold Time		t_{LH}	10			ns
SDATA Valid to SCK Rising Edge Setup		t_{DS}	10			ns
SCK Falling Edge to SDATA Valid Hold		t_{DH}	10			ns
TIMING CORE SETTING RESTRICTIONS						
Inhibited Region for SHP Edge Location[1]	See Figure 23	t_{SHPINH}	50		62	Edge location
Inhibited Region for SHP or SHD with Respect to H-Clocks[2, 3, 4]	See Figure 23 and Figure 24					
RETIME = 0, MASK = 0		t_{SHDINH}	HxNEGLOC − 14		HxNEGLOC − 2	Edge location
RETIME = 0, MASK = 1		t_{SHDINH}	HxPOSLOC − 14		HxPOSLOC − 2	Edge location
RETIME = 1, MASK = 0		t_{SHPINH}	HxNEGLOC − 14		HxNEGLOC − 2	Edge location
RETIME = 1, MASK = 1		t_{SHPINH}	HxPOSLOC − 14		HxPOSLOC − 2	Edge location
Inhibited Region for DOUTPHASE Edge Location	See Figure 23	$t_{DOUTINH}$	SHDLOC + 1		SHDLOC + 12	Edge location

[1] Applies only to slave mode operation. The inhibited area for SHP is needed to meet the timing requirement for t_{CLISHP} for proper H-counter reset operation.
[2] When the HBLKRETIME bits (Address 0x35, Bits[3:0]) are enabled, the inhibit region for the SHD location changes to the inhibit region for the SHP location.
[3] When the HBLK masking polarity registers (V-sequence Register 0x18[24:21]) are set to 0, the H-edge reference becomes HxNEGLOC.
[4] The H-clock signals that have SHP/SHD inhibit regions depend on the HCLK mode: Mode 1 = H1; Mode 2 = H1, H2; Mode 3 = H1, H3; and 3-Phase Mode = Phase 1, Phase 2, and Phase 3.

VERTICAL DRIVER SPECIFICATIONS

VH1, VH2 = 12 V; VM1, VM2, VMM = 0 V; VL1, VL2, VLL = −6 V; C_L shown in load model; T_A = 25°C.

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
V1A TO V13		Simplified load conditions, 3000 pF to ground + 30 Ω in series, SRSW = VSS				
Delay Time, VL to VM and VM to VH	t_{PLM}, t_{PMH}			40		ns
Delay Time, VM to VL and VH to VM	t_{PML}, t_{PHM}			40		ns
Rise Time, VL to VM	t_{RLM}			150		ns
Rise Time, VM to VH	t_{RMH}			315		ns
Fall Time, VM to VL	t_{FML}			250		ns
Fall Time, VH to VM	t_{FHM}			165		ns
Output Currents						
At −7.25 V				10		mA
At −0.25 V				−22		mA
At +0.25 V				22		mA
At +14.75 V				−10		mA
R_{ON}					35	Ω
V14, V15, V16		Simplified load conditions, 3000 pF to ground + 30 Ω in series				
Delay Time, VL to VM	t_{PLM}			45		ns
Delay Time, VM to VL	t_{PML}			45		ns
Rise Time, VL to VM	t_{RLM}			345		ns
Fall Time, VM to VL	t_{FML}			280		ns
Output Currents						
At −7.25 V				10		mA
At −0.25 V				−7		mA
R_{ON}					55	Ω
SUBCK OUTPUT		Simplified load conditions, 1000 pF to ground				
Delay Time, VLL to VH	t_{PLH}			50		ns
Delay Time, VH to VLL	t_{PHL}			50		ns
Delay Time, VLL to VMM	t_{PLM}			50		ns
Delay Time, VMM to VH	t_{PMH}			50		ns
Delay Time, VH to VMM	t_{PHM}			50		ns
Delay Time, VMM to VLL	t_{PML}			50		ns
Rise Time, VLL to VH	t_{RLH}			50		ns
Rise Time, VLL to VMM	t_{RLM}			55		ns
Rise Time, VMM to VH	t_{RMH}			50		ns
Fall Time, VH to VLL	t_{FHL}			55		ns
Fall Time, VH to VMM	t_{FHM}			100		ns
Fall Time, VMM to VLL	t_{FML}			40		ns
Output Currents						
At −7.25 V				20		mA
At −0.25 V				−12		mA
At +0.25 V				12		mA
At +14.75 V				−20		mA
R_{ON}					35	Ω
SRCTL INPUT RANGE		Valid only when SRSW is high	0.8		VDVDD	V

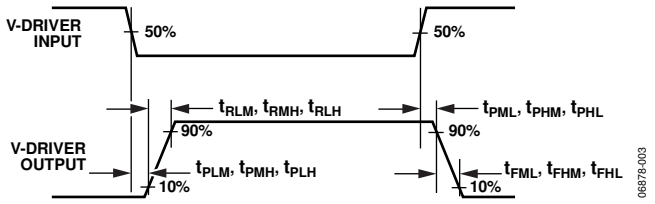


Figure 3. Definition of V-Driver Timing Specifications

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVDD to AVSS	−0.3 V to +2.2 V
TCVDD to TCVSS	−0.3 V to +2.2 V
HVDD1, HVDD2 to HVSS1, HVSS2	−0.3 V to +3.9 V
RGVDD to RGVSS	−0.3 V to +3.9 V
DVDD to DVSS	−0.3 V to +2.2 V
DRVDD to DRVSS/LDOVSS	−0.3 V to +3.9 V
IOVDD to IOVSS	−0.3 V to +3.9 V
VDVDD to VDVSS	−0.3 V to +3.9 V
CLIVDD to TCVSS	−0.3 V to +3.9 V
VH1, VH2 to VL1, VL2, VLL	−0.3 V to +25.0 V
VH1, VH2 to VDVSS	−0.3 V to +17.0 V
VL1, VL2 to VDVSS	−17.0 V to +0.3 V
VM1, VM2 to VDVSS	−6.0 V to +3.0 V
VLL to VDVSS	−17.0 V to +0.3 V
VMM to VDVSS	VLL − 0.3 V to VDVDD + 0.3 V
V1A to V16 to VDVSS	VLx − 0.3 V to VHx + 0.3 V
RG and HL Outputs to RGVSS	−0.3 V to RGVDD + 0.3 V
H1 to H8 Outputs to HVSSx	−0.3 V to HVDDx + 0.3 V
VDR_EN, XSUBCNT, SRCTL, SRSW to VDVSS	−0.3 V to VDVDD + 0.3 V
Digital Outputs to IOVSS	−0.3 V to IOVDD + 0.3 V
Digital Inputs to IOVSS	−0.3 V to IOVDD + 0.3 V
SCK, SL, SDATA to DVSS	−0.3 V to DVDD + 0.3 V
REFT, REFB, CCDIN to AVSS	−0.3 V to AVDD + 0.3 V
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	350°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	Unit
CSP_BGA (BC-105-1)	40.3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

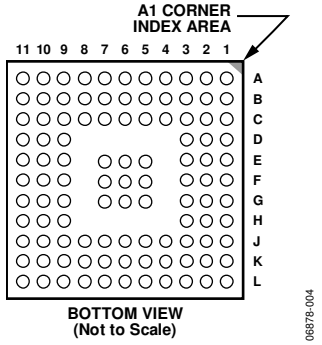


Figure 4. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
L6	AVDD	P	Analog Supply.
J7, K8	AVSS	P	Analog Supply Ground.
A10	DVDD	P	Digital Logic Supply.
A9	DVSS	P	Digital Logic Ground.
L5	CLIVDD	P	CLI Input Supply.
K6	TCVDD	P	Analog Timing Core Supply.
K4	TCVSS	P	Analog Timing Core Ground.
A2	DRVDD	P	Data Driver Supply.
B2	DRVSS/LDOVSS	P	Data Driver and LDO Ground.
E1	HVDD1	P	H-Driver Supply.
E2	HVSS1	P	H-Driver Ground.
G1	HVDD2	P	H-Driver Supply.
G2	HVSS2	P	H-Driver Ground.
J1	HVDD2	P	H-Driver Supply.
J2	HVSS2	P	H-Driver Ground.
L3	RGVDD	P	RG, HL Driver Supply.
K3	RGVSS	P	RG, HL Driver Ground.
B1	LDOIN	P	LDO 3.3 V Input.
C1	LDOOUT	P	LDO Output Voltage.
H11	IOVDD	P	Digital I/O Supply.
G11	IOVSS	P	Digital I/O Ground.
C11	VDVDD	P	V-Driver Logic Supply (3 V).
C10	VDVSS	P	V-Driver Ground.
E3	VM1	P	V-Driver Midsupply.
D3	VL1	P	V-Driver Low Supply.
C3	VH1	P	V-Driver High Supply.
J3	VH2	P	V-Driver High Supply.
H3	VL2	P	V-Driver Low Supply.
F3	VM2	P	V-Driver Midsupply.
G3	VMM	P	V-Driver Midsupply for SUBCK Output.
J4	VLL	P	V-Driver Low Supply for SUBCK Output.
L7	CCDIN	AI	CCD Signal Input.
K7	CCDGND	AI	CCD Ground.
C2	SRCTL	AI	Slew Rate Control Pin. Tie to VDVSS if not used.
L8	REFT	AO	Voltage Reference Top Bypass.
L9	REFB	AO	Voltage Reference Bottom Bypass.
D11	VD	DIO	Vertical Sync Pulse.
E10	HD	DIO	Horizontal Sync Pulse.

Pin No.	Mnemonic	Type[1]	Description
E11	SYNC/$\overline{\text{RST}}$	DO	SYNC Pin (Internal Pull-Up Resistor)/External Reset Input (Active Low).
K9	SL	DI	3-Wire Serial Load Pulse (Internal Pull-Up Resistor).
K10	SDATA	DI	3-Wire Serial Data.
L10	SCK	DI	3-Wire Serial Clock.
B11	VDR_EN	DI	Enable V-Outputs When High.
K11	XSUBCNT	DI	XSUBCNT Input to SUBCK Buffer.
C9	SRSW	DI	Slew Rate Control Enable. Tie to ground to disable.
J6	$\overline{\text{LEGEN}}$	DI	Legacy Mode Enable Bar. Tie to ground for legacy 18-channel mode.
J5	CLI	DI	Reference Clock Input.
K5	CLO	DO	Clock Output for Crystal.
F10	GPO1	DO	General-Purpose Output.
H9	GPO2	DO	General-Purpose Output.
G10	GPO3	DO	General-Purpose Output.
F11	GPO4	DO	General-Purpose Output.
H10	GPO7	DO	General-Purpose Output.
J11	GPO8	DO	General-Purpose Output.
B9	D0	DO	Data Output (LSB).
C6	D1	DO	Data Output.
C7	D2	DO	Data Output.
A8	D3	DO	Data Output.
A7	D4	DO	Data Output.
B7	D5	DO	Data Output.
B6	D6	DO	Data Output.
A6	D7	DO	Data Output.
A5	D8	DO	Data Output.
B4	D9	DO	Data Output.
A4	D10	DO	Data Output.
A3	D11	DO	Data Output (MSB).
B3	DCLK	DO	Data Clock Output.
D1	H1	DO	CCD Horizontal Clock.
D2	H2	DO	CCD Horizontal Clock.
F1	H3	DO	CCD Horizontal Clock.
F2	H4	DO	CCD Horizontal Clock.
H1	H5	DO	CCD Horizontal Clock.
H2	H6	DO	CCD Horizontal Clock.
K1	H7	DO	CCD Horizontal Clock.
K2	H8	DO	CCD Horizontal Clock.
L2	HL	DO	CCD Horizontal Clock.
L4	RG	DO	CCD Reset Gate Clock.
G9	V1A	VO3	CCD Vertical Transfer Clock. Three-level output (XV1 + XV16).
G6	V1B	VO3	CCD Vertical Transfer Clock. Three-level output (XV1 + XV17).
G5	V2A	VO3	CCD Vertical Transfer Clock. Three-level output (XV2 + XV18).
E9	V2B	VO3	CCD Vertical Transfer Clock. Three-level output (XV2 + XV19).
J9	V3A	VO3	CCD Vertical Transfer Clock. Three-level output (XV3 + XV20).
F6	V3B	VO3	CCD Vertical Transfer Clock. Three-level output. $\overline{\text{LEGEN}}$ is low, XV3 + XV21. $\overline{\text{LEGEN}}$ is high, XV23 + XV21.
F5	V4	VO3	CCD Vertical Transfer Clock. Three-level output (XV4 + XV22).
E5	V5	VO3	CCD Vertical Transfer Clock. Three-level output. $\overline{\text{LEGEN}}$ is low, XV5 + XV23. $\overline{\text{LEGEN}}$ is high, XV5 + GPO5.
D10	V6	VO3	CCD Vertical Transfer Clock. Three-level output. $\overline{\text{LEGEN}}$ is low, XV6 + XV24. $\overline{\text{LEGEN}}$ is high, XV6 + GPO6.
F9	V7	VO2	CCD Vertical Transfer Clock. Two-level output (XV7).
F7	V8	VO2	CCD Vertical Transfer Clock. Two-level output (XV8).

Pin No.	Mnemonic	Type[1]	Description
D9	V9	VO2	CCD Vertical Transfer Clock. Two-level output (XV9).
C4	V10	VO2	CCD Vertical Transfer Clock. Two-level output (XV10).
C5	V11	VO2	CCD Vertical Transfer Clock. Two-level output (XV11).
B5	V12	VO2	CCD Vertical Transfer Clock. Two-level output (XV12).
E6	V13	VO2	CCD Vertical Transfer Clock. Two-level output (XV13).
E7	V14	VO2	CCD Vertical Transfer Clock. Two-level output (XV14).
C8	V15	VO2	CCD Vertical Transfer Clock. Two-level output (XV15).
J8	V16	VO2	CCD Vertical Transfer Clock. Two-level output (XV24). Available only when $\overline{\text{LEGEN}}$ is high (19-channel mode).
G7	SUBCK	VO3	CCD Substrate Clock Output.
A1, A11, B8, B10, J10, L1, L11	NC		Not Internally Connected.

[1] AI = analog input; AO = analog output; DI = digital input; DO = digital output; DIO = digital input/output; P = power; VO2 = vertical driver output, two-level; VO3 = vertical driver output, three-level.

TYPICAL PERFORMANCE CHARACTERISTICS

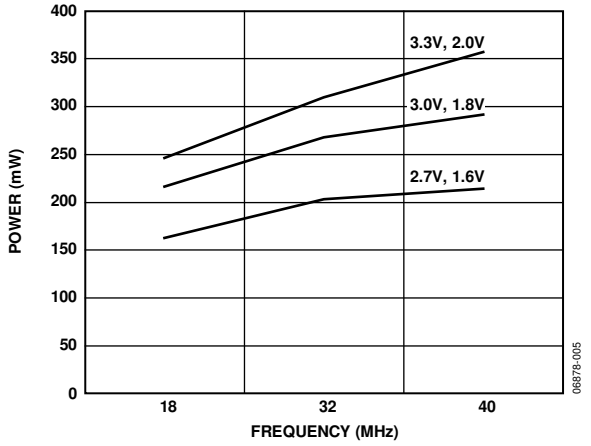


Figure 5. AFETG Power vs. Frequency (V-Driver Not Included); AVDD = TCVDD = DVDD = 1.8 V, All Other Supplies at 2.7 V, 3.0 V, or 3.3 V

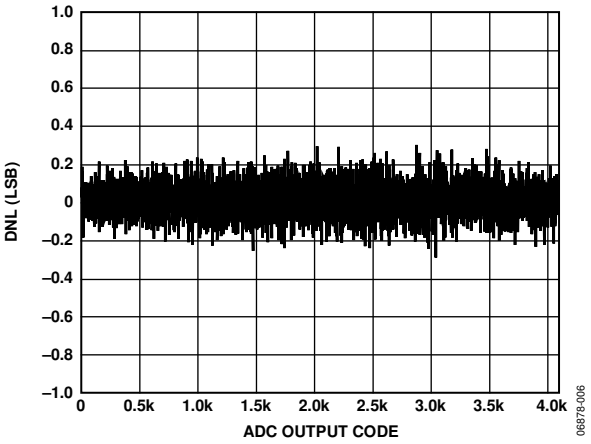


Figure 6. Typical Differential Nonlinearity (DNL) Performance

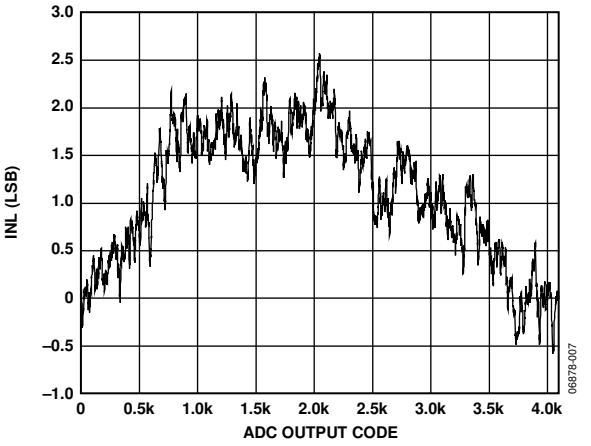


Figure 7. Typical System Integral Nonlinearity (INL) Performance

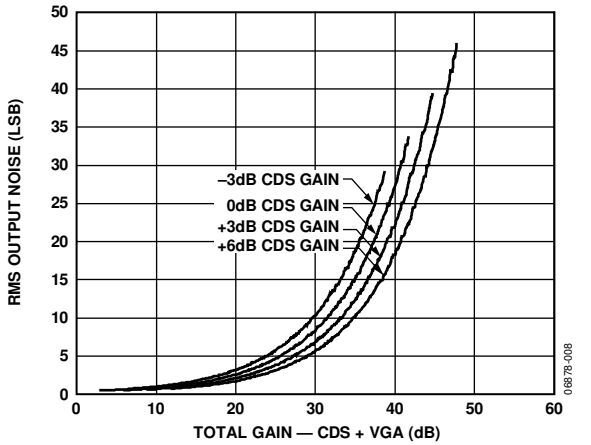


Figure 8. Output Noise vs. Total Gain (CDS + VGA)

EQUIVALENT CIRCUITS

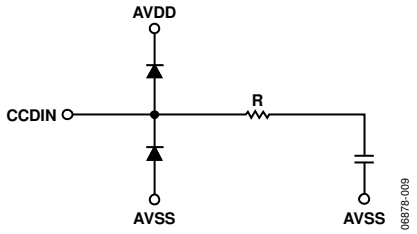


Figure 9. CCDIN

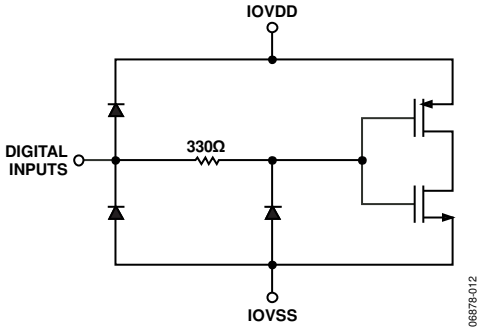


Figure 12. Digital Inputs

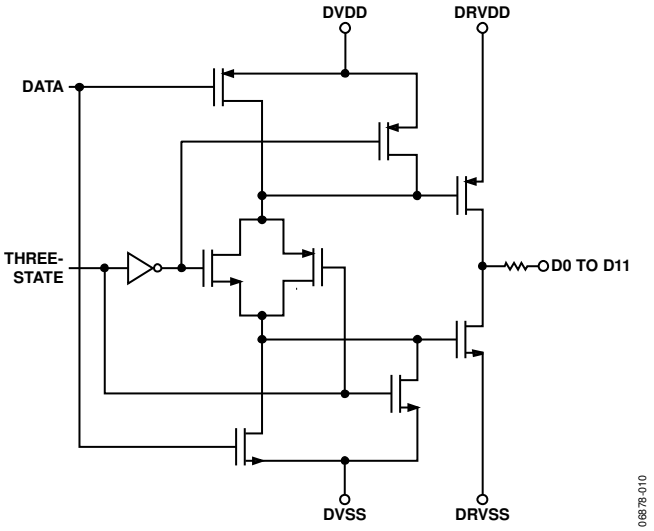


Figure 10. Digital Data Outputs

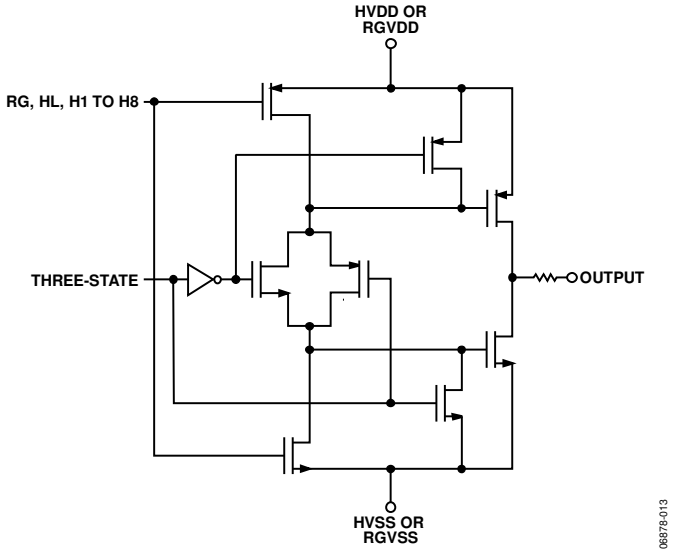


Figure 13. H1 to H8, HL, RG Drivers

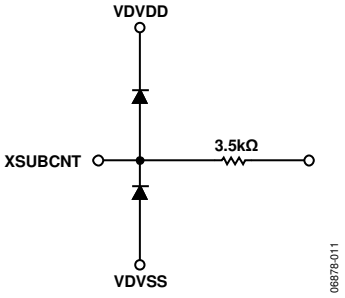


Figure 11. XSUBCNT

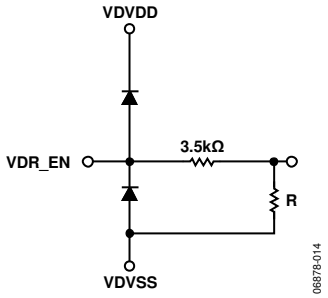


Figure 14. VDR_EN

TERMINOLOGY

Differential Nonlinearity (DNL)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed. No missing codes guaranteed to 12-bit resolution indicates that all 4096 codes, each for its respective input, must be present over all operating conditions.

Integral Nonlinearity (INL)
INL is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Peak Nonlinearity
Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the output of the AD9920A from a true straight line. The point used as zero scale occurs 0.5 LSB before the first code transition. Positive full scale is defined as a level 1 LSB and 0.5 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always appropriately amplified to fill the ADC full-scale range.

Power Supply Rejection (PSR)
The PSR is measured with a step change applied to the supply pins. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

Total Output Noise
The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage using the relationship

$$1\ \text{LSB} = (\textit{ADC Full Scale}/2^{n}\ \textit{Codes})$$

where n is the bit resolution of the ADC.

For the AD9920A, 1 LSB = 0.244 mV.

THEORY OF OPERATION

Figure 15 shows the typical system block diagram for the AD9920A in master mode. The CCD output is processed by the AD9920A AFE circuitry, which consists of a CDS, black level clamp, and ADC. The digitized pixel information is sent to the digital image processor chip, which performs the postprocessing and compression. To operate the CCD, all CCD timing parameters are programmed into the AD9920A from the system microprocessor through the 3-wire serial interface. From the master clock, CLI, provided by the image processor or external crystal, the AD9920A generates the CCD horizontal and vertical clocks and the internal AFE clocks. External synchronization is provided by a sync pulse from the microprocessor, which resets the internal counters and resyncs the VD and HD outputs.

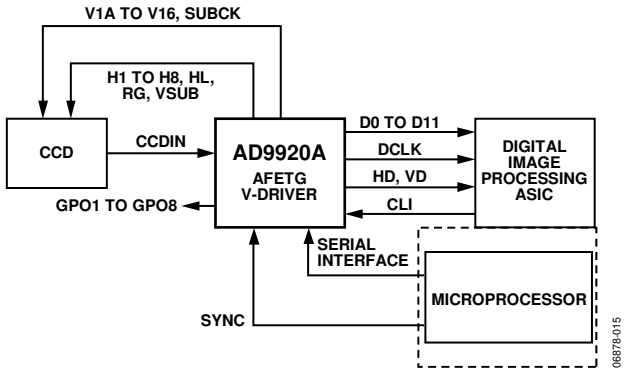


Figure 15. Typical System Block Diagram, Master Mode

Alternatively, the AD9920A can be operated in slave mode. In this mode, the VD and HD are provided externally from the image processor, and all AD9920A timing is synchronized with VD and HD.

The H-drivers for H1 to H8, HL, and RG are included in the AD9920A, allowing these clocks to be directly connected to the CCD. An H-driver voltage of up to 3.6 V is supported. V1A to V16 and SUBCK vertical clocks are included as well, allowing the AD9920A to provide all horizontal and vertical clocks necessary to clock data out of a CCD.

The AD9920A includes programmable general-purpose outputs (GPOs) that can trigger mechanical shutter and strobe (flash) circuitry.

Figure 16 and Figure 17 show the maximum horizontal and vertical counter dimensions for the AD9920A. All internal horizontal and vertical clocking is controlled by these counters, which specify line and pixel locations. Maximum HD length is 16,384 pixels per line, and maximum VD length is 8192 lines per field.

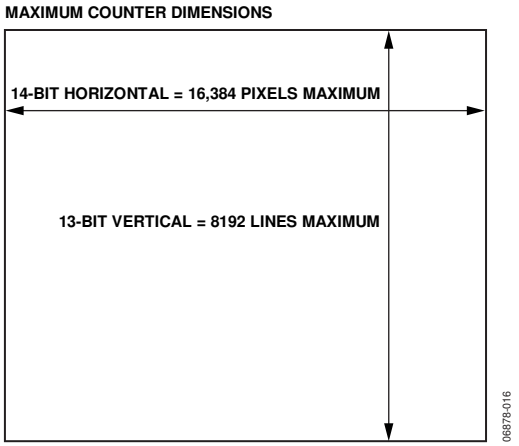


Figure 16. Vertical and Horizontal Counters

H-COUNTER BEHAVIOR IN SLAVE MODE

In the AD9920A, the internal H-counter holds at its maximum count of 16,383 instead of rolling over. This feature allows the AD9920A to be used in applications that contain a line length greater than 16,384 pixels. Although no programming values for the vertical and horizontal signals are available beyond 8191, the H, RG, and AFE clocking continues to operate, sampling the remaining pixels on the line.

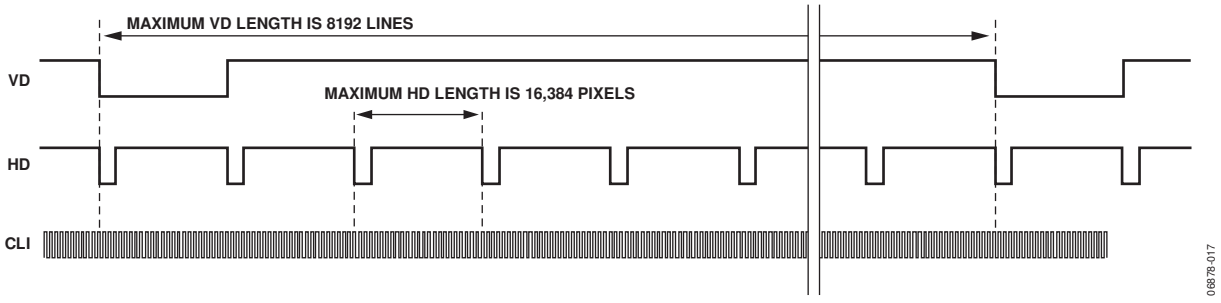


Figure 17. Maximum VD/HD Dimensions

HIGH SPEED *PRECISION TIMING* CORE

The AD9920A generates high speed timing signals using the flexible *Precision Timing* core. This core is the foundation for generating the timing used for both the CCD and the AFE; it includes the reset gate (RG), horizontal drivers (H1 to H8, HL), and SHP/SHD sample clocks. A unique architecture makes it routine for the system designer to optimize image quality by providing precise control over the horizontal CCD readout and the AFE correlated double sampling.

The high speed timing of the AD9920A operates the same way in either master or slave mode configuration. For more information on synchronization and pipeline delays, see the Power-Up Sequence for Master Mode section.

Timing Resolution

The *Precision Timing* core uses a 1× master clock input as a reference (CLI). This clock should be the same as the CCD pixel clock frequency. Figure 18 illustrates how the internal timing core divides the master clock period into 64 steps or edge positions. Using a 40.5 MHz CLI frequency, the edge resolution of the *Precision Timing* core is approximately 0.4 ns. If a 1× system clock is not available, it is possible to use a 2× reference clock by programming the CLIDIVIDE register (AFE Register Address 0x0D). The AD9920A then internally divides the CLI frequency by 2.

High Speed Clock Programmability

Figure 19 shows when the high speed clocks RG, H1 to H8, HL, SHP, and SHD are generated. The RG pulse has programmable rising and falling edges and can be inverted using the polarity control. Horizontal Clock H1 has programmable rising and falling edges and polarity control. In HCLK Mode 1, H3, H5, and H7 are equal to H1. H2, H4, H6, and H8 are always inverses of H1.

The edge location registers are each six bits wide, allowing the selection of all 64 edge locations. Figure 23 shows the default timing locations for all of the high speed clock signals.

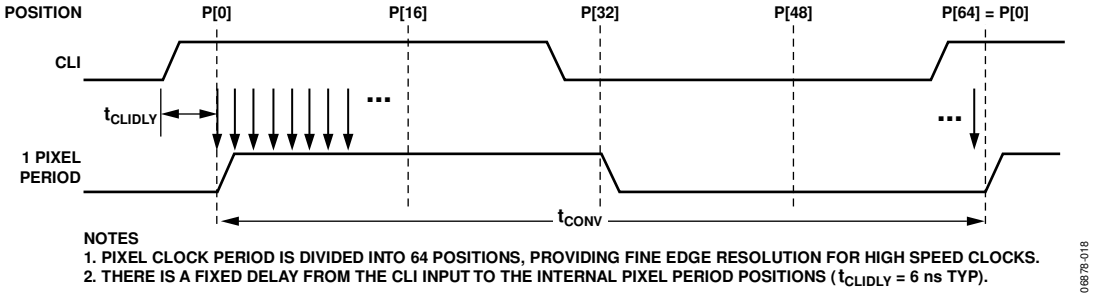


Figure 18. High Speed Clock Resolution from CLI, Master Clock Input

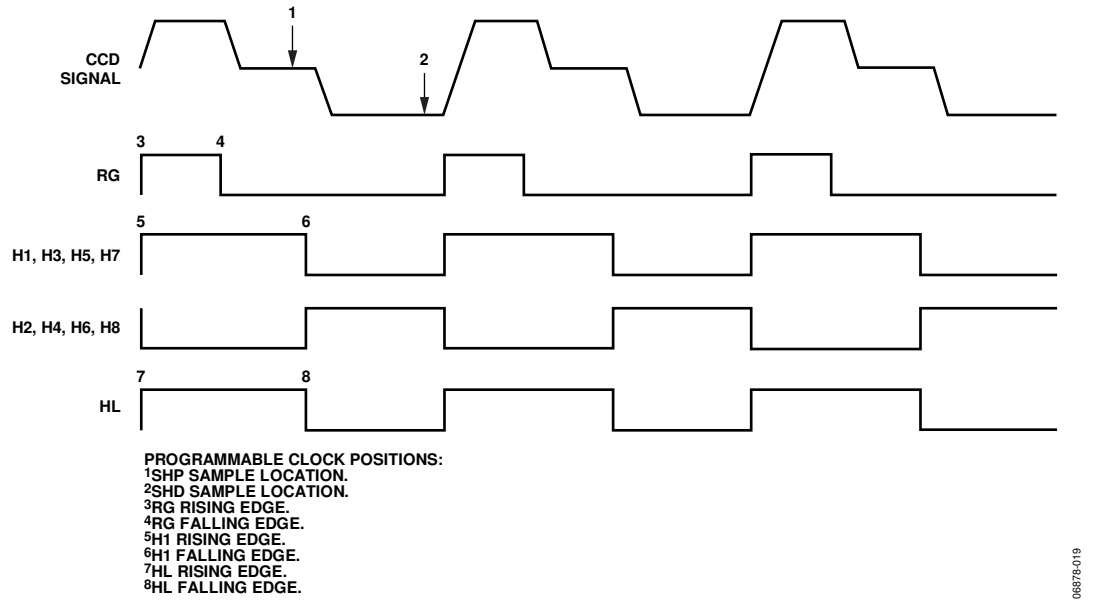


Figure 19. High Speed Clock Programmable Locations (HCLKMODE = 0x01)

H-Driver and RG Outputs

In addition to the programmable timing positions, the AD9920A features on-chip output drivers for the RG, HL, and H1 to H8 outputs. These drivers are powerful enough to drive the CCD inputs directly. The H-driver and RG current can be adjusted for optimum rise/fall time for a particular load by using the drive strength control registers (Address 0x36 and Address 0x37). The 3-bit drive setting for each H1 to H8 output is adjustable in 4.3 mA increments: 0 = off, 1 = 4.3 mA, 2 = 8.6 mA, 3 = 12.9 mA, 4 = 17.3 mA, 5 = 21.6 mA, 6 = 25.9 mA, and 7 = 30.2 mA.

The 3-bit drive settings for the HL and RG outputs are also adjustable in 4.3 mA increments, but with a maximum drive strength of 17.3 mA: 0 = off, 1 = 4.3 mA, 2 = 8.6 mA, 3 = 12.9 mA, 4 = 4.3 mA, 5 = 8.6 mA, 6 = 12.9 mA, and 7 = 17.3 mA.

As shown in Figure 19, when HCLK Mode 1 is used, the H2, H4, H6, and H8 outputs are inverses of the H1, H3, H5, and H7 outputs. Using the HCLKMODE register (Address 0x24, Bits[4:0]), it is possible to select a different configuration.

Table 10 shows a comparison of the different programmable settings for each HCLK mode. Figure 20 and Figure 21 show the settings for HCLK Mode 2 and HCLK Mode 3, respectively.

It is recommended that all H1 to H8 outputs on the AD9920A be used together for maximum flexibility in drive strength settings. A typical CCD with H1 and H2 inputs should have only the AD9920A H1, H3, H5, and H7 outputs connected together to drive the CCD H1 and should have only the AD9920A H2, H4, H6, and H8 outputs connected together to drive the CCD H2.

In 3-phase HCLK mode, only six of the HCLK outputs are used, with two outputs driving each of the three phases:

- H1 and H2 are connected to CCD Phase 1.
- H5 and H6 are connected to CCD Phase 2.
- H7 and H8 are connected to CCD Phase 3.

Table 9. Timing Core Register Parameters for H1, H2, HL, RG, SHP, and SHD

Parameter	Length (Bits)	Range	Description
Positive Edge	6	0 to 63 edge location	Positive edge location for H1, H2, HL, H3P1, and RG.
Negative Edge	6	0 to 63 edge location	Negative edge location for H1, H2, HL, H3P1, and RG.
Sampling Location	6	0 to 63 edge location	Sampling location for internal SHP and SHD signals.
Drive Strength	3	0 to 7 current steps	Drive current for H1 to H8, HL, and RG outputs (4.3 mA per step).

Table 10. HCLK Modes, Selected by Address 0x24, Bits[4:0]

HCLKMODE	Register Value	Description
Mode 1	0x01	H1 edges are programmable with H3 = H5 = H7 = H1, H2 = H4 = H6 = H8 = inverse of H1.
Mode 2	0x02	H1 edges are programmable with H3 = H5 = H7 = H1. H2 edges are programmable with H4 = H6 = H8 = H2.
Mode 3	0x04	H1 edges are programmable with H3 = H1 and H2 = H4 = inverse of H1. H5 edges are programmable with H7 = H5 and H6 = H8 = inverse of H5.
3-Phase Mode	0x10	H1 edges are programmable using Address 0x33 and H2 = H1 (Phase 1). H5 edges are programmable using Address 0x31 and H6 = H5 (Phase 2). H7 edges are programmable using Address 0x30 and H8 = H7 (Phase 3).
Invalid Selection	All other values	Invalid register settings. Do not use.

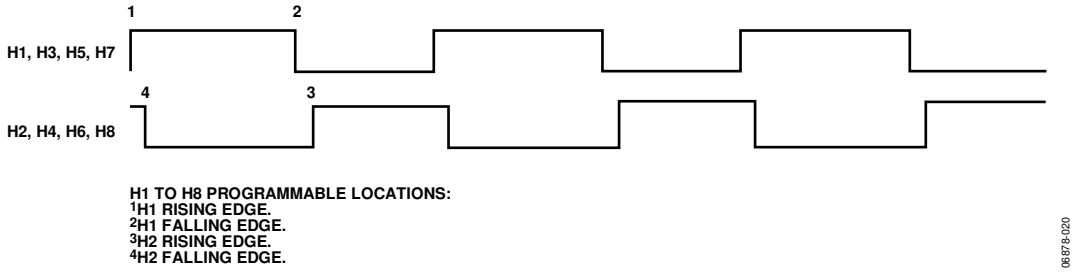


Figure 20. HCLK Mode 2 Operation

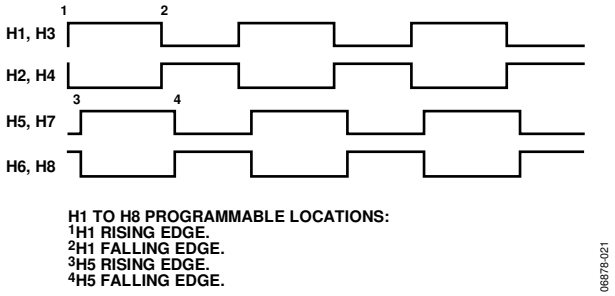


Figure 21. HCLK Mode 3 Operation

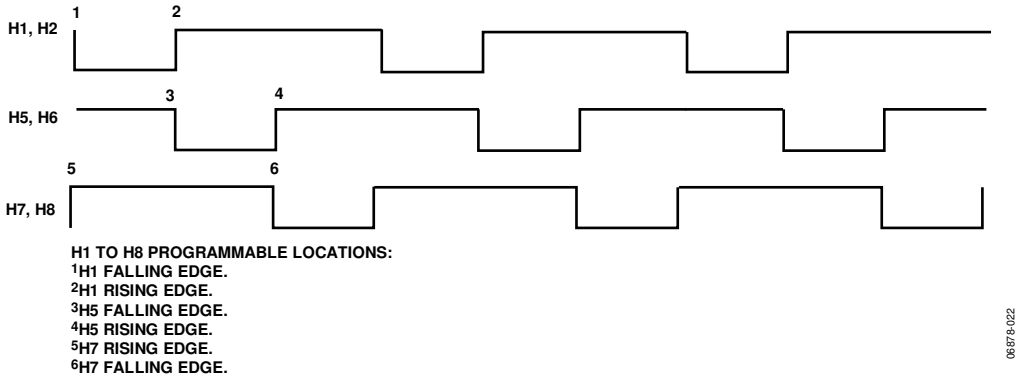
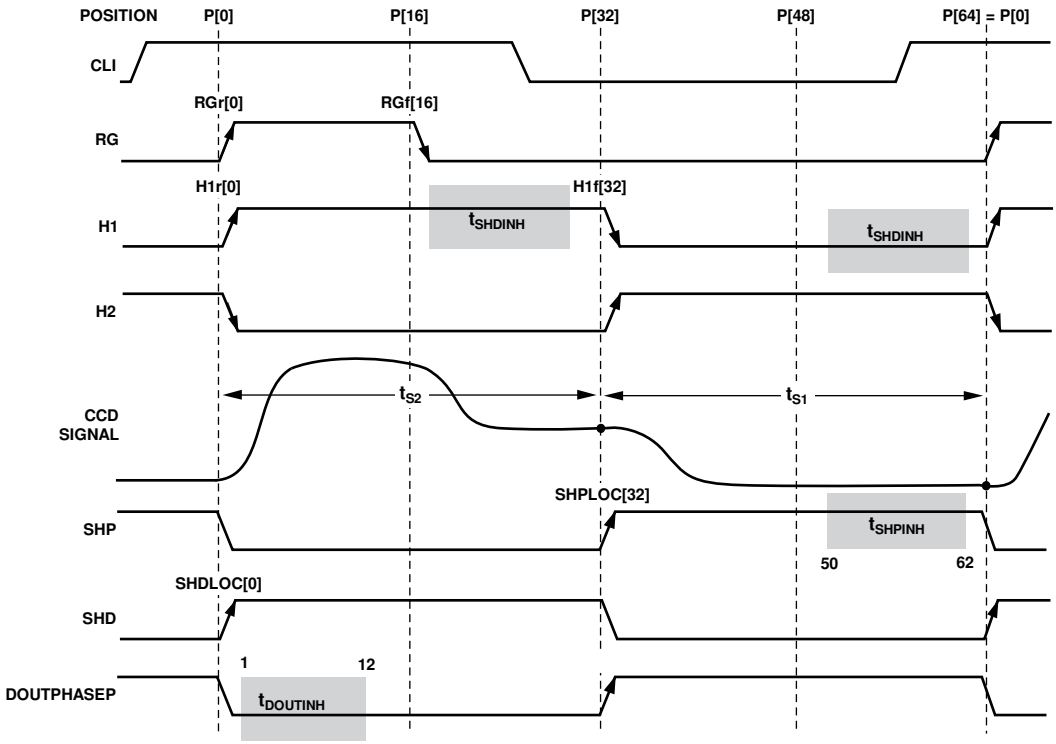
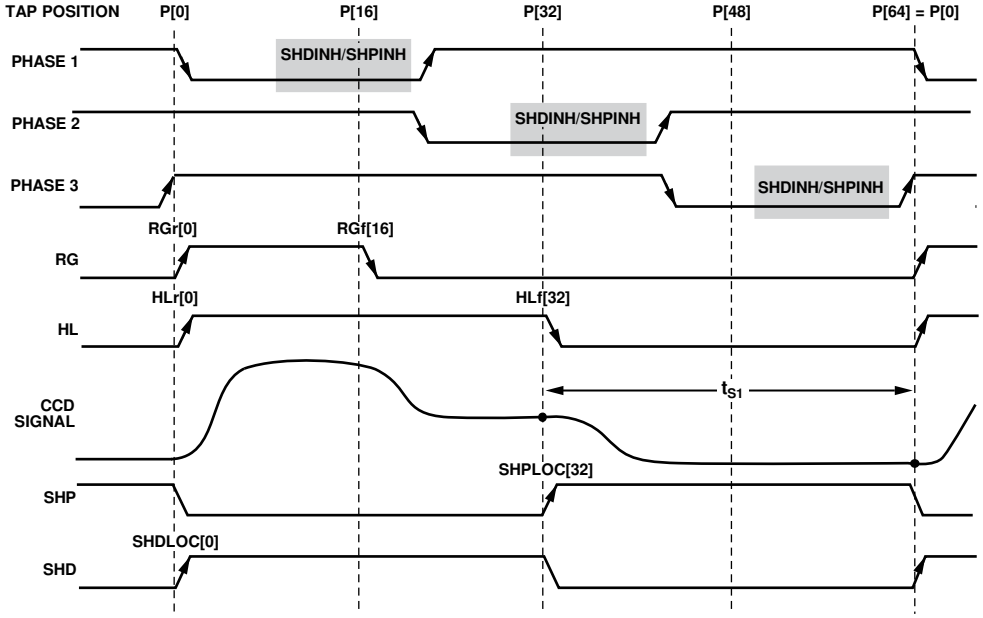


Figure 22. 3-Phase HCLK Mode Operation



NOTES
1. ALL SIGNAL EDGES ARE FULLY PROGRAMMABLE TO ANY OF THE 64 POSITIONS WITHIN ONE PIXEL PERIOD. TYPICAL POSITIONS FOR EACH SIGNAL ARE SHOWN. HCLK MODE 1 IS SHOWN.
2. CERTAIN POSITIONS SHOULD BE AVOIDED FOR EACH SIGNAL, SHOWN ABOVE AS INHIBIT REGIONS.
3. IF A SETTING IN THE INHIBIT REGION IS USED, AN UNSTABLE PIXEL SHIFT CAN OCCUR IN THE HBLK LOCATION OR AFE PIPELINE.
4. THE t_{SHPINH} AREA FROM 50 TO 62 ONLY APPLIES IN SLAVE MODE.
5. THE t_{SHDINH} AREA WILL APPLY TO EITHER H1 RISING OR FALLING EDGE, DEPENDING ON THE VALUE OF THE H1HBLK MASKING POLARITY.
6. THE t_{SHDINH} AREA CAN ALSO BE CHANGED TO A t_{SHPINH} AREA IF THE H1HBLKRETIME BIT = 1.

Figure 23. High Speed Timing Default Locations



NOTES
1. ALL SIGNAL EDGES ARE FULLY PROGRAMMABLE TO ANY OF THE 64 POSITIONS WITHIN ONE PIXEL PERIOD. TYPICAL POSITIONS FOR EACH SIGNAL ARE SHOWN USING 3-PHASE HBLK MODE.
2. THE RISING EDGE OF EACH HCLK PHASE HAS AN ASSOCIATED SHDINH.
3. WHEN THE HBLK RETIME BITS (0x35 [3:0]) ARE ENABLED, THE INHIBITED AREA BECOMES SHPINH.
4. WHEN THE HBLK MASK LEVEL FOR PHASE 1, 2, OR 3 IS CHANGED TO LOW, THE INHIBIT AREA IS REFERENCED TO THE HCLK FALLING EDGE, INSTEAD OF THE HCLK RISING EDGE.

Figure 24. High Speed Timing Typical Locations, 3-Phase HCLK Mode

DIGITAL DATA OUTPUTS

The AD9920A data output and DCLK phase are programmable using the DOUTPHASE registers (Address 0x39, Bits[13:0]). DOUTPHASEP (Bits[5:0]) selects any edge location from 0 to 63, as shown in Figure 25. DOUTPHASEN (Bits[13:8]) does not actually program the phase of the data outputs but is used internally and should always be programmed to a value of DOUTPHASEP plus 32 edges. For example, if DOUTPHASEP is set to 0, DOUTPHASEN should be set to 32 (0x20).

Normally, the data output and DCLK signals track in phase, based on the contents of the DOUTPHASE registers. The DCLK output phase can also be held fixed with respect to the data outputs by setting the DCLKMODE register high (Address 0x39, Bit 16). In this mode, the DCLK output remains at a fixed phase equal to a delayed version of CLI, and the data output phase remains programmable.

The pipeline delay through the AD9920A is shown in Figure 26. After the CCD input is sampled by SHD, there is a 16-cycle delay until the data is available.

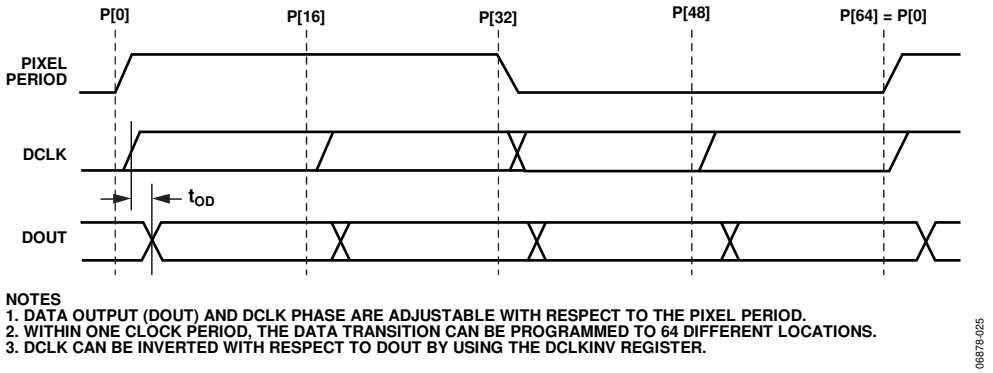


Figure 25. Digital Output Phase Adjustment Using DOUTPHASEP Register

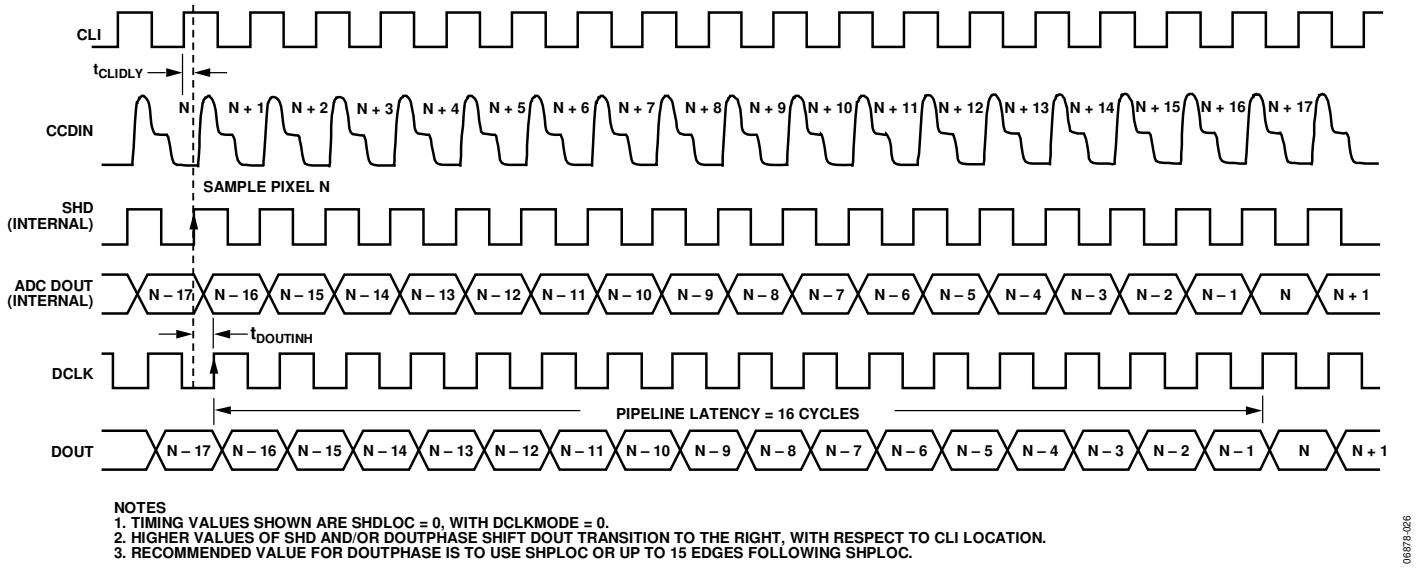


Figure 26. Digital Data Output Pipeline Delay

HORIZONTAL CLAMPING AND BLANKING

The horizontal clamping and blanking pulses of the AD9920A are fully programmable to suit a variety of applications. Individual control is provided for CLPOB, PBLK, and HBLK in the different regions of each field. This allows the dark pixel clamping and blanking patterns to be changed at each stage of the readout to accommodate different image transfer timing and high speed line shifts.

Individual CLPOB and PBLK Patterns

The AFE horizontal timing consists of CLPOB and PBLK, as shown in Figure 27. These two signals are programmed independently using the registers shown in Table 11. The start polarity for the CLPOB (or PBLK) signal is CLPOBPOL (PBLKPOL), and the first and second toggle positions of the pulse are CLPOBTOG1 (PBLKTOG1) and CLPOBTOG2 (PBLKTOG2). Both signals are active low and should be programmed accordingly.

A separate pattern for CLPOB and PBLK can be programmed for each vertical sequence. As described in the Vertical Timing Generation section, several V-sequences can be created, each containing a unique pulse pattern for CLPOB and PBLK.

Figure 57 shows how the sequence change positions divide the readout field into regions. By assigning a different V-sequence to each region, the CLPOB and PBLK signals can change with each change in the vertical timing.

CLPOB and PBLK Masking Areas

Additionally, the AD9920A allows the CLPOB and PBLK signals to be disabled in certain lines in the field without changing any of the existing CLPOB pattern settings.

To use CLPOB (or PBLK) masking, the CLPMASKSTART (PBLKMASKSTART) and CLPMASKEND (PBLKMASKEND) registers are programmed to specify the start and end lines in the field where the CLPOB (PBLK) patterns are ignored. The three sets of start and end registers allow up to three CLPOB (PBLK) masking areas to be created.

The CLPOB and PBLK masking registers are not specific to a certain V-sequence; they are always active for any existing field of timing. During operation, to disable the CLPOB masking feature, these registers must be set to the maximum value of 0x1FFF or a value greater than the programmed VD length.

Note that to disable CLPOB (or PBLK) masking during power-up, it is recommended that CLPMASKSTART (PBLKMASKSTART) be set to 8191 and that CLPMASKEND (PBLKMASKEND) be set to 0. This prevents any accidental masking caused by register update events.

Table 11. CLPOB and PBLK Pattern Registers

Register	Length (Bits)	Range	Description
CLPOBPOL	1	High/low	Starting polarity of CLPOB for each V-sequence.
PBLKPOL	1	High/low	Starting polarity of PBLK for each V-sequence.
CLPOBTOG1	13	0 to 8191 pixel location	First CLPOB toggle position within line for each V-sequence.
CLPOBTOG2	13	0 to 8191 pixel location	Second CLPOB toggle position within line for each V-sequence.
PBLKTOG1	13	0 to 8191 pixel location	First PBLK toggle position within line for each V-sequence.
PBLKTOG2	13	0 to 8191 pixel location	Second PBLK toggle position within line for each V-sequence.
CLPMASKSTART	13	0 to 8191 line location	CLPOB masking area—starting line within field (maximum of three areas).
CLPMASKEND	13	0 to 8191 line location	CLPOB masking area—ending line within field (maximum of three areas).
PBLKMASKSTART	13	0 to 8191 line location	PBLK masking area—starting line within field (maximum of three areas).
PBLKMASKEND	13	0 to 8191 line location	PBLK masking area—ending line within field (maximum of three areas).

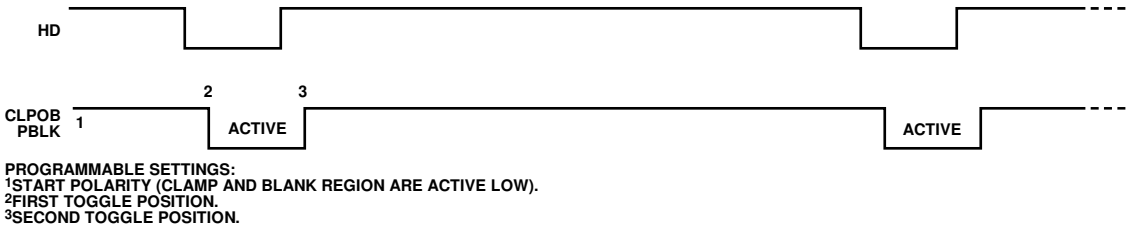


Figure 27. Clamp and Preblank Pulse Placement

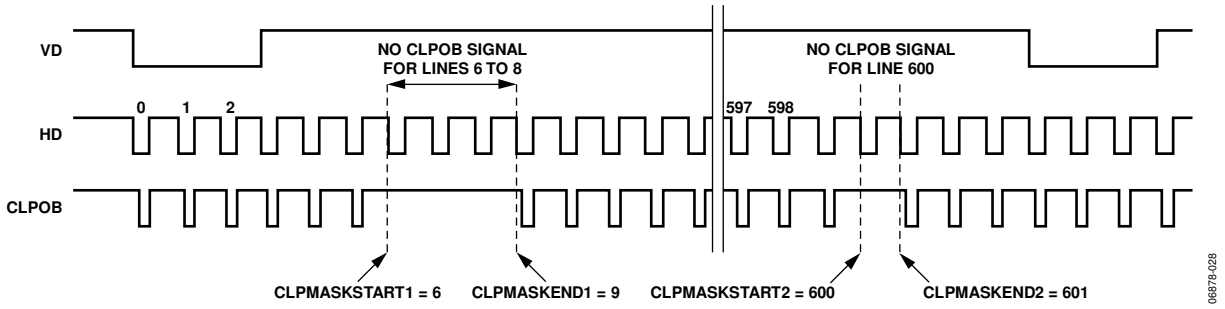


Figure 28. CLPOB Masking Example

Individual HBLK Patterns

The HBLK programmable timing shown in Figure 29 is similar to the timing of CLPOB and PBLK; however, there is no start polarity control. Only the toggle positions are used to designate the start and stop positions of the blanking period. Additionally, separate masking polarity controls for each H-clock phase designate the polarity of the horizontal clock signals during the blanking period. Setting HBLKMASK_H1 high sets H1—and, therefore, H3, H5, and H7—low during the blanking, as shown in Figure 30. As with the CLPOB and PBLK signals, HBLK registers are available in each V-sequence, allowing different blanking signals to be used with different vertical timing sequences.

The AD9920A supports two modes of HBLK operation. HBLK Mode 0 supports basic operation and pixel mixing HBLK operation. HBLK Mode 1 supports advanced HBLK operation.

The following sections describe each mode in detail. Register parameters are described in detail in Table 12.

HBLK Mode 0 Operation

There are six toggle positions available for HBLK. Normally, only two of the toggle positions are used to generate the standard HBLK interval. However, the additional toggle positions can be used to generate special HBLK patterns, as shown in Figure 31. The pattern in this example uses all six toggle positions to generate two extra groups of pulses during the HBLK interval. By changing the toggle positions, different patterns can be created.

Separate toggle positions are available for even and odd lines. If alternation is not needed, the same values should be loaded into the registers for even (HBLKTOGE) and odd (HBLKTOGO) lines.

Multiple repeats of the HBLK signal are enabled by setting the HBLKLEN and HBLKREP registers along with the six toggle positions (four are shown in Figure 32).

Generating HBLK Line Alternation

HBLK Mode 0 provides the ability to alternate different HBLK toggle positions on even and odd lines. HBLK line alternation can be used alone or in conjunction with V-pattern odd/even alternation (see the Generating Line Alternation for V-Sequences and HBLK section). Separate toggle positions are available for even and odd lines. If even/odd line alternation is not needed, the same values should be loaded into the registers for even (HBLKTOGE) and odd (HBLKTOGO) lines.