Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

CCD Signal Processor with V-Driver and *Precision Timing* Generator

AD9923A

FEATURES

Integrated 15-channel V-driver
12-bit, 36 MHz analog-to-digital converter (ADC)
Similar register map to the AD9923
5-field, 10-phase vertical clock support
Complete on-chip timing generator
***Precision Timing* core with <600 ps resolution**
Correlated double sampler (CDS)
6 dB to 42 dB 10-bit variable gain amplifier (VGA)
Black level clamp with variable level control
On-chip 3 V horizontal and RG drivers
2-phase and 4-phase H-clock modes
Electronic and mechanical shutter support
On-chip driver for external crystal
On-chip sync generator with external sync input
8 mm × 8 mm CSP_BGA package with 0.65 mm pitch

APPLICATIONS

Digital still cameras

GENERAL DESCRIPTION

The AD9923A is a complete 36 MHz front-end solution for digital still cameras and other CCD imaging applications. Similar to the AD9923 product, the AD9923A includes the analog front end (AFE), a fully programmable timing generator (TG), and a 15-channel vertical driver (V-driver). A *Precision Timing*™ core allows adjustment of high speed clocks with approximately 600 ps resolution at 36 MHz operation.

The on-chip V-driver supports up to 15 channels for use with 5-field, 10-phase CCDs.

The analog front end includes black level clamping, CDS, VGA, and a 12-bit ADC. The timing generator and V-driver provide all the necessary CCD clocks: RG, H-clocks, vertical clocks, sensor gate pulses, substrate clock, and substrate bias control. The internal registers are programmed using a 3-wire serial interface.

Packaged in an 8 mm × 8 mm CSP_BGA, the AD9923A is specified over an operating temperature range of −25°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

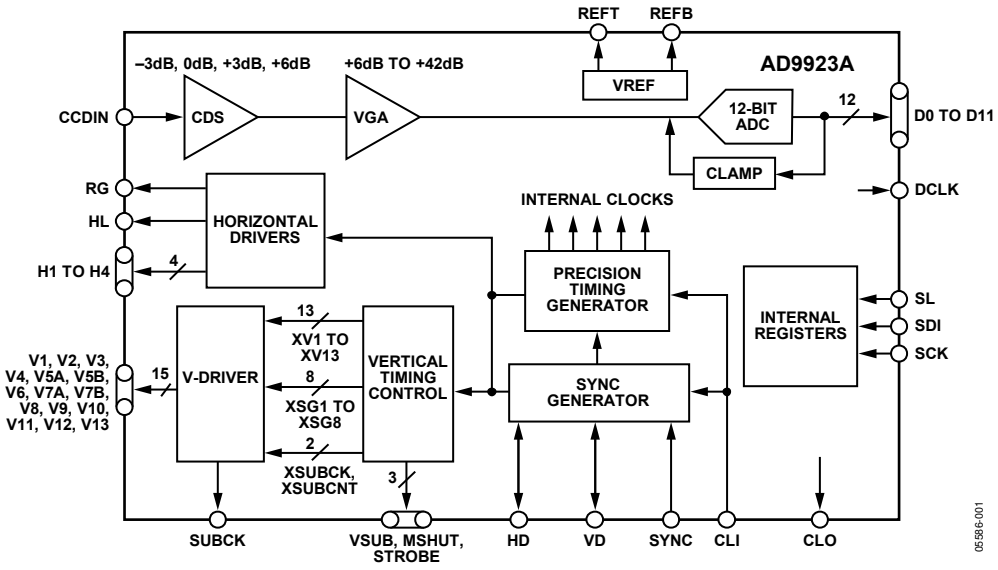


Figure 1.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

AD9923A* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- AD9923A: CCD Signal Processor with V-Driver and Precision Timing Generator Data Sheet

DESIGN RESOURCES

- AD9923A Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9923A EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

1/10—Rev. 0 to Rev. A

Changes to Table 6 ... 6
Added Table 8; Renumbered Sequentially ... 8
Changes to Individual HBLK Patterns Section ... 20
Changes to Table 13 ... 20
Change to SUBCK: High Precision Operation Section ... 45
Changes to Manual Control Section ... 49

10/06—Revision 0: Initial Version

SPECIFICATIONS

Table 1.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
TEMPERATURE RANGE					
Operating		−25		+85	°C
Storage		−65		+150	°C
AFETG POWER SUPPLY VOLTAGES					
AVDD	AFE analog supply	2.7	3.0	3.6	V
TCVDD	Timing Core Analog Supply	2.7	3.0	3.6	V
RGVDD	RG Driver	2.7	3.0	3.6	V
HVDD	HL, H1 to H4 Drivers	2.7	3.0	3.6	V
DRVDD	Data Output Drivers	2.7	3.0	3.6	V
DVDD	Digital	2.7	3.0	3.6	V
V-DRIVER POWER SUPPLY VOLTAGES					
VDD1, VDD2	V-Driver Logic	+2.7	+3.0	+3.6	V
VH1, VH2	V-Driver High Supply	+11.5	+15.0	+16.5	V
VL1, VL2	V-Driver Low Supply	−8.5	−7.5	−5.5	V
VM1, VM2	V-Driver Mid Supply	−1.5	0.0	+1.5	V
VLL	SUBCK Low Supply	−8.5	−7.5	−5.5	V
VMM	SUBCK Mid Supply	−4.0	0.0	+1.5	V
AFETG POWER DISSIPATION					
Total	36 MHz, 3.0 V supply, 400 pF total H-load, 20 pF RG load		335		mW
Standby 1 Mode			105		mW
Standby 2 Mode			1		mW
Standby 3 Mode			1		mW
Power from HVDD Only[1]			130		mW
Power from RGVDD Only			10		mW
Power from AVDD Only			75		mW
Power from TCVDD Only			40		mW
Power from DVDD Only			75		mW
Power from DRVDD Only			5		mW
V-DRIVER POWER DISSIPATION[2]	VH1, VH2 = +15 V; VL1, VL2 = −7.5 V; VM1, VM2 = 0 V; VDD1, VDD2 = 3.3 V; all V-driver inputs tied low				
VH1, VH2			5		mW
VL1, VL2			2.5		mW
VM1, VM2			0		mW
VDD1, VDD2			0.5		mW
MAXIMUM CLOCK RATE (CLI)		36			MHz

[1] The total power dissipated by the HVDD supply can be approximated using the equation

Total HVDD Power = [C_{LOAD} × *HVDD* × *Pixel Frequency*] × *HVDD*

Reducing the H-load and/or using a lower HVDD supply reduces the power dissipation. C_{LOAD} is the total capacitance seen by all H-outputs.

[2] V-driver power dissipation depends on the frequency of operation and the load they are driving. All inputs to the V-driver were tied low for the measurements in Table 1.

DIGITAL SPECIFICATIONS

DRVDD = 2.7 V to 3.6 V, C_L = 20 pF, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS						
High Level Input Voltage		V_{IH}	2.1			V
Low Level Input Voltage		V_{IL}			0.6	V
High Level Input Current		I_{IH}		10		µA
Low Level Input Current		I_{IL}		10		µA
Input Capacitance		C_{IN}		10		pF
LOGIC OUTPUTS	Powered by DVDD, DRVDD					
High Level Output Voltage	At I_{OH} = 2 mA	V_{OH}	DVDD − 0.5, DRVDD − 0.5			V
Low Level Output Voltage	At I_{OL} = 2 mA	V_{OL}			0.5	V

H-DRIVER SPECIFICATIONS

HVDD = RGVDD = 2.7 V to 3.6 V, C_L = 20 pF, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
RG and H-DRIVER OUTPUTS	RG, HL, and H1 to H4 powered by RGVDD, HVDD				
High Level Output Voltage	At maximum current	RGVDD − 0.5, HVDD − 0.5			V
Low Level Output Voltage	At maximum current			0.5	V
Maximum Output Current	Programmable	30			mA
Maximum Load Capacitance	For each output	100			pF

VERTICAL DRIVER SPECIFICATIONS

VDD1 = VDD2 = 3.3 V, VH1 = VH2 = 15 V, VM1 = VM2 = VMM = 0 V, VL1 = VL2 = VLL = −7.5 V, 25°C.

Table 4.

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
V-DRIVER OUTPUTS	Simplified load conditions, 3000 pF to ground					
Delay Time						
VL to VM and VM to VH	Rising edges	t_{PLM}, t_{PMH}		35		ns
VM to VL and VH to VM	Falling edges	t_{PML}, t_{PHM}		35		ns
Rise Time						
VL to VM		t_{RLM}		125		ns
VM to VH		t_{RMH}		260		ns
Fall Time						
VM to VL		t_{FML}		220		ns
VH to VM		t_{FHM}		125		ns
Output Currents						
at −7.25 V				+10		mA
at −0.25 V				−22		mA
at +0.25 V				+22		mA
at +14.75 V				−10		mA
R_{ON}					35	Ω
SUBCK OUTPUT	Simplified load conditions, 1000 pF to ground					
Delay Time						
VLL to VH		t_{PLH}		25		ns
VH to VLL		t_{PHL}		30		ns
VLL to VMM		t_{PLM}		25		ns

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
VMM to VH		t_{PMH}		25		ns
VH to VMM		t_{PHM}		30		ns
VMM to VLL		t_{PML}		25		ns
Rise Time						
VLL to VH		t_{RLH}		40		ns
VLL to VMM		t_{RLM}		45		ns
VMM to VH		t_{RMH}		30		ns
Fall Time						
VH to VLL		t_{FHL}		40		ns
VH to VMM		t_{FHM}		90		ns
VMM to VLL		t_{FML}		25		ns
Output Currents						
at −7.25 V				20		mA
at −0.25 V				12		mA
at +0.25 V				12		mA
at +14.75 V				20		mA
R_{ON}					35	Ω

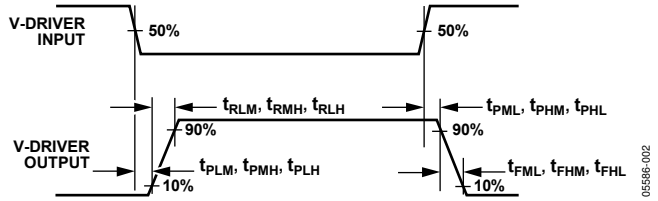


Figure 2. Definition of V-Driver Timing Specifications

ANALOG SPECIFICATIONS

AVDD = 3.0 V, f_{CLI} = 36 MHz, typical timing specifications, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
CDS	Input characteristics definition[1]				
Allowable CCD Reset Transient			0.5	1.2	V
CDS Gain Accuracy	VGA gain = 6 dB (Code 15, default value)				
−3 dB CDS Gain		−3	−2.5	−2	dB
0 dB CDS Gain	Default	0	+0.5	+1	dB
+3 dB CDS Gain		+3	+3.5	+4	dB
+6 dB CDS Gain		+5.5	+6	+6.5	dB
Maximum Input Range Before Saturation					
0 dB CDS Gain	Default setting		1.0		V p-p
−3 dB CDS Gain			1.4		V p-p
+6 dB CDS Gain			0.5		V p-p
Maximum CCD Black Pixel Amplitude	Positive offset definition[1]				
0 dB CDS Gain (Default)		−100		+200	mV
+6 dB CDS Gain		−50		+100	mV
VARIABLE GAIN AMPLIFIER (VGA)					
Gain Control Resolution			1024		Steps
Gain Monotonicity			Guaranteed		
Gain Range					
Minimum Gain (VGA Code 15)			6		dB
Maximum Gain (VGA Code 1023)			42		dB

Parameter	Conditions/Comments	Min	Typ	Max	Unit
BLACK LEVEL CLAMP	Measured at ADC output				
Clamp Level Resolution			1024		Steps
Minimum Clamp Level (Code 0)			0		LSB
Maximum Clamp Level (Code 1023)			255		LSB
ANALOG-TO-DIGITAL CONVERTER (ADC)					
Resolution		12			Bits
Differential Nonlinearity (DNL)		−1.0	±0.5	+1.0	LSB
No Missing Codes			Guaranteed		
Full-Scale Input Voltage			2.0		V
VOLTAGE REFERENCE					
Reference Top Voltage (REFT)			2.0		V
Reference Bottom Voltage (REFB)			1.0		V
SYSTEM PERFORMANCE	Includes entire signal chain				
Gain Accuracy					
Low Gain (VGA Code 15)	Default CDS gain (0 dB)	6.0	6.5	7.0	dB
Maximum Gain (VGA Code 1023)		42.0	42.5	43.0	dB
Peak Nonlinearity, 500 mV Input Signal	12 dB gain applied		0.1		%
Total Output Noise	AC-grounded input, 6 dB gain applied		1.0		LSB rms
Power Supply Rejection (PSR)	Measured with step change on supply		50		dB

[1] Input signal characteristics are defined as shown in Figure 3.

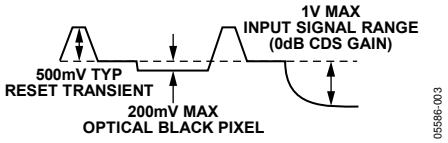


Figure 3. Signal Characteristics

TIMING SPECIFICATIONS

C_L = 20 pF, AVDD = DVDD = DRVDD = 3.0 V, f_{CLI} = 36 MHz, unless otherwise noted.

Table 6.

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
MASTER CLOCK, CLI						
CLI Clock Period		t_{CONV}	27.8			ns
CLI High/Low Pulse Width			11.2	13.9	16.6	ns
Delay from CLI Rising Edge to Internal Pixel Position 0		t_{CLIDLY}		6		ns
AFE CLPOB Pulse Width[1, 2]			2	20		Pixels
Allowable Region for HD Falling Edge to CLI Rising Edge	Only valid in slave mode	t_{HDCLI}	4		t_{CONV} − 2	ns
SHP Inhibit Region	Only valid in slave mode	t_{SHPINH}	30		39	Edge location
AFE SAMPLE LOCATION[1]						
SHP Sample Edge to SHD Sample Edge		t_{S1}	11.6	13.9		ns
DATA OUTPUTS						
Output Delay from DCLK Rising Edge[1]		t_{OD}		8		ns
Inhibited Area for DOUTPHASE Edge Location			SHD		SHD + 11	Edge location
Pipeline Delay from SHP/SHD Sampling to Data Output			16			Cycles
SERIAL INTERFACE						
Maximum SCK Frequency		f_{SCLK}	36			MHz
SL to SCK Setup Time		t_{LS}	10			ns
SCK to SL Hold Time		t_{LH}	10			ns
SDATA Valid to SCK Rising Edge Setup		t_{DS}	10			ns

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
SCK Falling Edge to SDATA Valid Hold		t_{DH}	10			ns
SCK Falling Edge to SDATA Valid Read		t_{DV}	10			ns
INHIBIT REGION FOR SHP AND SHD WITH RESPECT TO H-CLOCK EDGE LOCATION						
HxMASK = 0, HxRETIME = 0, HxPOLARITY = 0		t_{SHDINH}	HxPOS – 9		HxPOS – 18	Edge location
HxMASK = 0, HxRETIME = 0, HxPOLARITY = 1		t_{SHDINH}	HxNEG – 9		HxNEG – 18	Edge location
HxMASK = 0, HxRETIME = 1, HxPOLARITY = 0		t_{SHPINH}	HxPOS – 7		HxPOS – 16	Edge location
HxMASK = 0, HxRETIME = 1, HxPOLARITY = 1		t_{SHPINH}	HxNEG – 7		HxNEG – 16	Edge location
HxMASK = 1, HxRETIME = 0, HxPOLARITY = 0		t_{SHDINH}	HxNEG – 9		HxNEG – 18	Edge location
HxMASK = 1, HxRETIME = 0, HxPOLARITY = 1		t_{SHDINH}	HxPOS – 9		HxPOS – 18	Edge location
HxMASK = 1, HxRETIME = 1, HxPOLARITY = 0		t_{SHPINH}	HxNEG – 7		HxNEG – 16	Edge location
HxMASK = 1, HxRETIME = 1, HxPOLARITY = 1		t_{SHPINH}	HxPOS – 7		HxPOS – 16	Edge location

[1] Parameter is programmable.
[2] Minimum CLPOB pulse width is for functional operation only. Wider typical pulses are recommended to achieve good clamp performance.

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	To	Rating
AVDD	AVSS	−0.3 V to +3.9 V
TCVDD	TCVSS	−0.3 V to +3.9 V
HVDD	HVSS	−0.3 V to +3.9 V
RGVDD	RGVSS	−0.3 V to +3.9 V
DVDD	DVSS	−0.3 V to +3.9 V
DRVDD	DRVSS	−0.3 V to +3.9 V
VDD1, VDD2	VSS1, VSS2	−0.3 V to +6 V
VH1, VH2	VL1, VL2	−0.3 V to +25 V
VH1, VH2	VSS1, VSS2	−0.3 V to +17 V
VL1, VL2	VSS1, VSS2	−17 V to +0.3 V
VM1, VM2	VSS1, VSS2	−6 V to +6 V
VLL	VSS1, VSS2	−17 V to +0.3 V
VMM	VSS1, VSS2	−6 V to + VH
VDR_EN	VSS1, VSS2	−0.3 V to +6 V
V1 to V15	VSS1, VSS2	VL − 0.3 V to VH + 0.3 V
RG Output	RGVSS	−0.3 V to RGVDD + 0.3 V
H1 to H4 Output	HVSS	−0.3 V to HVDD + 0.3 V
Digital Outputs	DVSS	−0.3 V to DVDD + 0.3 V
Digital Inputs	DVSS	−0.3 V to DVDD + 0.3 V
SCK, SL, SDATA	DVSS	−0.3 V to DVDD + 0.3 V
REFT/REFB, CCDIN	AVSS	−0.3 V to AVDD + 0.3 V
Junction Temperature		150°C
Lead Temperature, 10 sec		350°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 8. Thermal Resistance

Package Type	θ_{JA}	Unit
CSP_BGA	40.3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

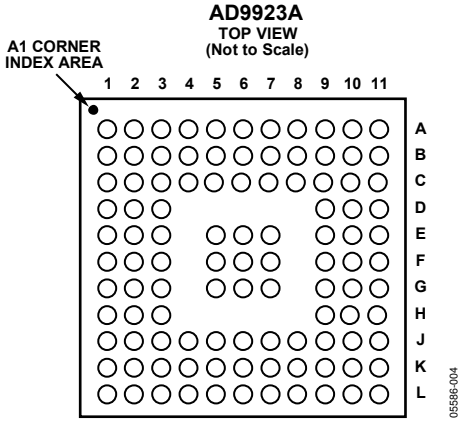


Figure 4. 105-Lead CSPBGA Package Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A7	AVDD	P	Analog Supply for AFE.
A1, A4, B2, B3, B4, B5, B6, B7	AVSS	P	Analog Ground for AFE.
B8	TCVDD	P	Analog Supply for Timing Core.
B9	TCVSS	P	Analog Ground for Timing Core.
E1	DVDD1	P	Digital Logic Power Supply 1.
F2	DVSS1	P	Digital Logic Ground 1.
K8, L7, L8	DVDD2	P	Digital Logic Power Supply 2.
K9	DVSS2	P	Digital Logic Ground 2.
D9	HVDD	P	H1 to H4, HL Driver Supply.
D10	HVSS	P	H1 to H4, HL Driver Ground.
B10	RGVDD	P	RG Driver Supply.
A10	RGVSS	P	RG Driver Ground.
L4	DRVDD	P	Data Output Driver Supply.
L5	DRVSS	P	Data Output Driver Ground.
J4	VDD1	P	V-Driver Logic Supply 1.
K5	VSS1	P	V-Driver Logic Ground 1.
L10	VDD2	P	V-Driver Logic Supply 2.
K10	VSS2	P	V-Driver Logic Ground 2.
F9	VH1	P	V-Driver High Supply 1.
D1	VH2	P	V-Driver High Supply 2.
E9	VL1	P	V-Driver Low Supply 1.
C1	VL2	P	V-Driver Low Supply 2.
C9	VM1	P	V-Driver Mid Supply 1.
D3	VM2	P	V-Driver Mid Supply 2.
F3	VLL	P	SUBCK Driver Low Supply.
E3	VMM	P	SUBCK Driver Mid Supply.
A6	CCDIN	AI	CCD Signal Input.
A5	CCDGND	AI	CCD Signal Ground.
A3	REFT	AO	Voltage Reference Top Bypass.
A2	REFB	AO	Voltage Reference Bottom Bypass.
C3	SL	DI	3-Wire Serial Load Pulse.
C2	SCK	DI	3-Wire Serial Clock.
B1	SDI	DI	3-Wire Serial Data Input.
G7	SYNC	DI	External System Synchronization Input.
E5	RSTB	DI	Reset Bar, Active Low Pulse.

Pin No.	Mnemonic	Type[1]	Description
A8	CLI	DI	Reference Clock Input (Master Clock).
A9	CLO	DO	Clock Output for Crystal.
F11	H1	DO	CCD Horizontal Clock 1.
E11	H2	DO	CCD Horizontal Clock 2.
D11	H3	DO	CCD Horizontal Clock 3.
C11	H4	DO	CCD Horizontal Clock 4.
B11	HL	DO	CCD Last Horizontal Clock.
C10	RG	DO	CCD Reset Gate Clock.
K6	VSUB	DO	CCD Substrate Bias.
F5	MSHUT	DO	Mechanical Shutter Pulse.
G5	STROBE	DO	Strobe Pulse.
G6	SUBCK	DO	CCD Substrate Clock (E Shutter).
F1	DCLK	DO	Data Clock Output.
G1	D0	DO	Data Output (LSB).
H3	D1	DO	Data Output.
H2	D2	DO	Data Output.
H1	D3	DO	Data Output.
J3	D4	DO	Data Output.
J2	D5	DO	Data Output.
J1	D6	DO	Data Output.
K3	D7	DO	Data Output.
K2	D8	DO	Data Output.
K1	D9	DO	Data Output.
L3	D10	DO	Data Output.
L2	D11	DO	Data Output (MSB).
D2	VD	DIO	Vertical Sync Pulse. Input in slave mode, output in master mode.
E2	HD	DIO	Horizontal Sync Pulse. Input in slave mode, output in master mode.
C8	V1	VO3	CCD Vertical Transfer Clock.
G10	V2	VO2	CCD Vertical Transfer Clock.
E7	V3	VO3	CCD Vertical Transfer Clock.
G9	V4	VO2	CCD Vertical Transfer Clock.
C4	V5A	VO3	CCD Vertical Transfer Clock.
C5	V5B	VO3	CCD Vertical Transfer Clock.
F10	V6	VO2	CCD Vertical Transfer Clock.
C6	V7A	VO3	CCD Vertical Transfer Clock.
C7	V7B	VO3	CCD Vertical Transfer Clock.
G11	V8	VO2	CCD Vertical Transfer Clock.
H11	V9	VO2	CCD Vertical Transfer Clock.
H10	V10	VO2	CCD Vertical Transfer Clock.
F6	V11	VO3	CCD Vertical Transfer Clock.
F7	V12	VO3	CCD Vertical Transfer Clock.
E10	V13	VO2	CCD Vertical Transfer Clock.
K11	VDR_EN	DI	V-Driver Output Enable pin.
J5	TEST0	DI	Test Input. Must be tied to VSS1 or VSS2.
J7	TEST1	DI	Test Input. Must be tied to VSS1 or VSS2.
J8	TEST3	DI	Test Input. Must be tied to VDD1 or VDD2.
A11, E6, H9, J6, J9, J10, J11, K4, K7, L1, L6, L9, L11, G2, G3	NC		No Connect.

[1] AI = analog input, AO = analog output, DI = digital input, DO = digital output, DIO = digital input/output, P = power, VO2 = Vertical Driver Output 2 level, VO3 = Vertical Driver Output 3 level.

TYPICAL PERFORMANCE CHARACTERISTICS

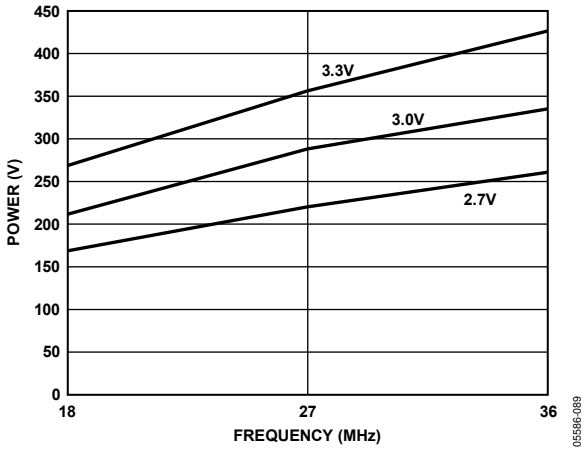


Figure 5. Power vs. Sample Rate

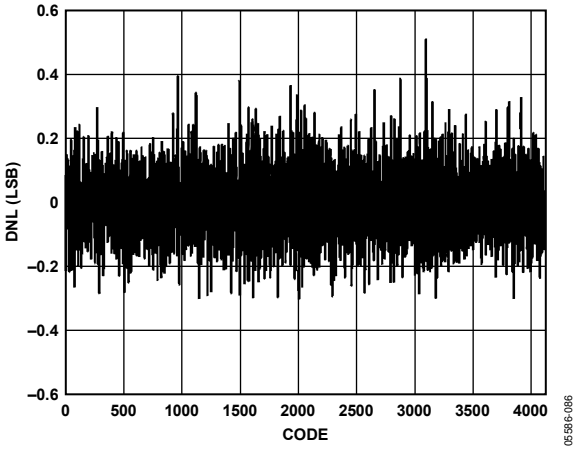


Figure 6. Typical DNL Performance

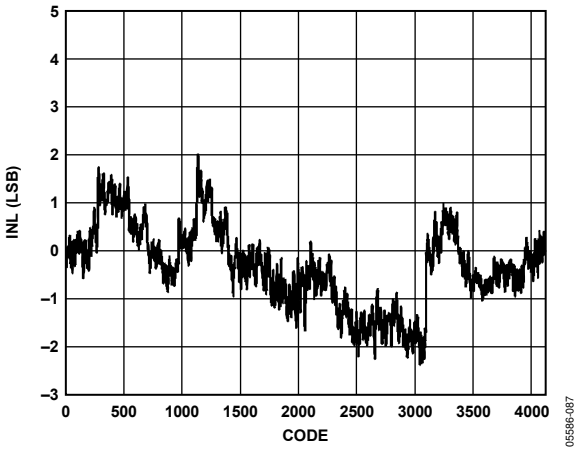


Figure 7. Typical INL Performance

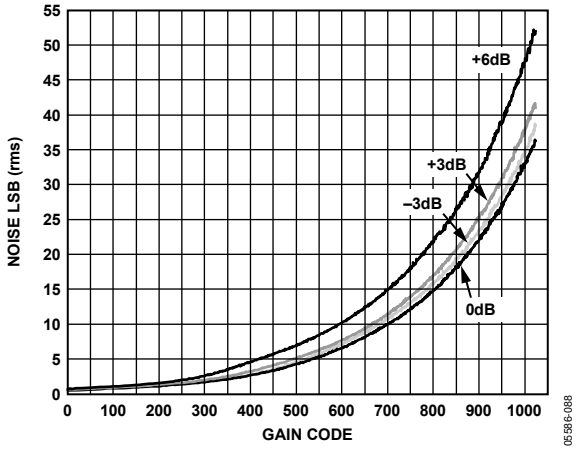


Figure 8. Output Noise vs. VGA Gain

EQUIVALENT CIRCUITS

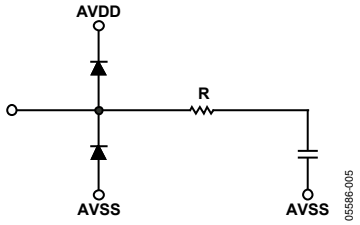


Figure 9. CCDIN, CCDGND

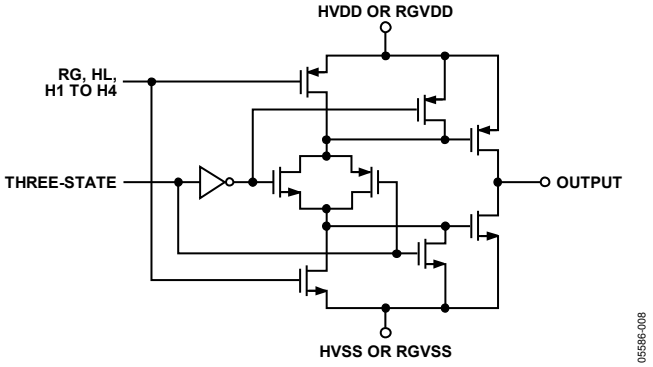


Figure 12. HL, H1 to H4, and RG Drivers

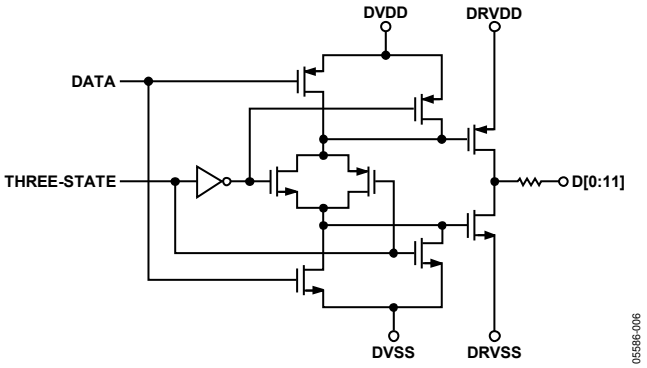


Figure 10. Digital Data Outputs

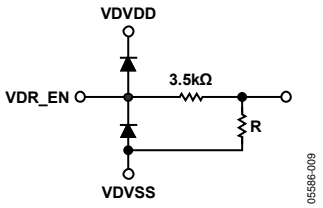


Figure 13. VDR_EN Input

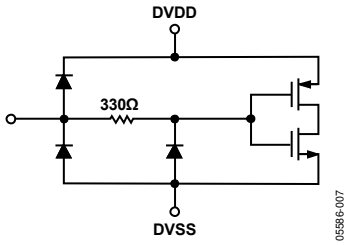


Figure 11. Digital Inputs

TERMINOLOGY

Differential Nonlinearity (DNL)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore, every code must have a finite width. No missing codes guaranteed to 12-bit resolution indicates that all 4096 codes, respectively, must be present over all operating conditions.

Integral Nonlinearity (INL)
The deviation of each code measured from a true straight line between the zero and full-scale values. The point used as zero scale occurs 0.5 LSB before the first code transition. Positive full scale is defined as a level 1.5 LSB beyond the last code transition. The deviation is measured from the middle of each output code to the true straight line.

Peak Nonlinearity
Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the AD9923A output from a true straight line. The point used as zero scale occurs 0.5 LSB before the first code transition. Positive full scale is defined as a level 1.5 LSB beyond the last code transition. The deviation is measured from the middle of each output code to the true straight line. The error is expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always appropriately gained up to fill the full-scale range of the ADC.

Total Output Noise
The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB, and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage, using the relationship

$$1\ LSB = (ADC\ full\ scale/2^{n}\ codes)$$

where n is the bit resolution of the ADC and *1 LSB* is 0.488 mV.

Power Supply Rejection (PSR)
The PSR is measured with a step change applied to the supply pins. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

THEORY OF OPERATION

Figure 14 shows the typical system block diagram for the AD9923A in master mode. The CCD output is processed by the AD9923A AFE circuitry, which consists of a CDS, VGA, black level clamp, and ADC. The digitized pixel information is sent to the digital image processor chip that performs the post-processing and compression. To operate the CCD, CCD timing parameters are programmed into the AD9923A from the system microprocessor through the 3-wire serial interface. The AD9923A generates the CCD horizontal, vertical, and the internal AFE clocks from the system master clock CLI. The CLI is provided by the image processor or external crystal. External synchronization is provided by a sync pulse from the microprocessor, which resets internal counters and resyncs the VD and HD outputs.

Alternatively, the AD9923A can be operated in slave mode, in which the VD and HD are provided externally from the image processor. In this mode, the AD9923A timing is synchronized with VD and HD.

The H-drivers for HL, H1 to H4, and RG are included in the AD9923A, allowing these clocks to be directly connected to the CCD. An H-driver voltage, HVDD, of up to 3.3 V is supported. An external V-driver is required for the vertical transfer clocks, the sensor gate pulses, and the substrate clock.

The AD9923A also includes programmable MSHUT and STROBE outputs that can be used to trigger mechanical shutter and strobe (flash) circuitry.

Figure 15 and Figure 16 show the maximum horizontal and vertical counter dimensions for the AD9923A. Internal horizontal and vertical clocking is controlled by these counters to specify line and pixel locations. The maximum HD length is 8192 pixels per line, and the maximum VD length is 4096 lines per field.

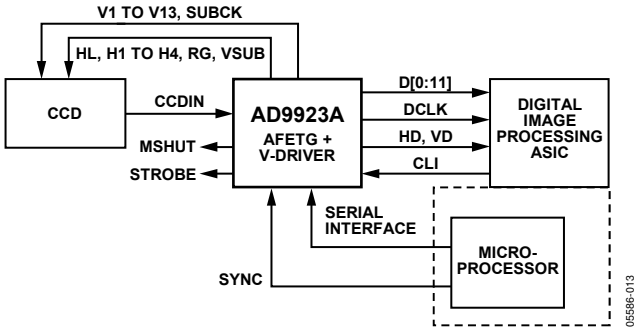


Figure 14. Typical System Block Diagram, Master Mode

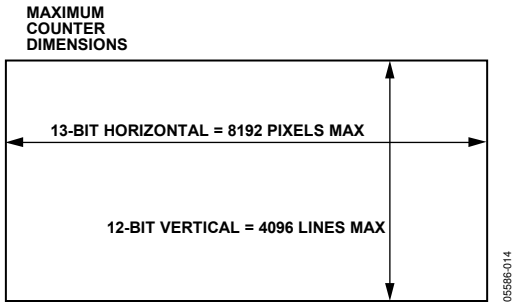


Figure 15. Vertical and Horizontal Counters

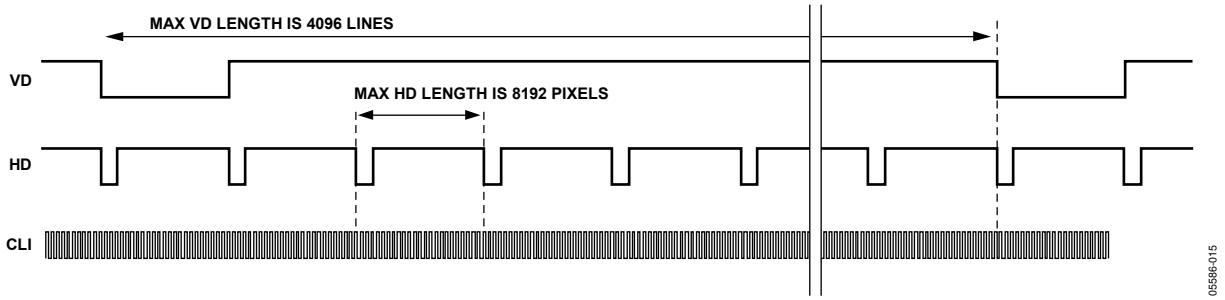


Figure 16. Maximum VD/HD Dimensions

PRECISION TIMING
HIGH SPEED TIMING GENERATION

The AD9923A generates high speed timing signals using the flexible *Precision Timing* core. This core is the foundation for generating the timing used for both the CCD and the AFE. It consists of the reset gate (RG), horizontal drivers (H1 to H4 and HL), and sample clocks (SHP and SHD). A unique architecture makes it routine for the system designer to optimize image quality by providing precise control over the horizontal CCD readout and the AFE-correlated double sampling.

The high speed timing of the AD9923A operates the same in master and slave modes. For more information on synchronization and pipeline delays, see the Power-Up and Synchronization in Slave Mode section.

Timing Resolution

The *Precision Timing* core uses a 1× master clock input (CLI) as a reference. The frequency of this clock should match the CCD pixel clock frequency. Figure 17 illustrates how the internal timing core divides the master clock period into 48 steps, or edge positions. Using a 36 MHz CLI frequency, the edge resolution of the *Precision Timing* core is approximately 0.6 ns. If a 1× system clock is not available, a 2× reference clock can be used by programming the CLIDIVIDE register (Address 0x30). The AD9923A then internally divides the CLI frequency by 2.

The AD9923A includes a master clock output (CLO) which is the inverse of CLI. This output is intended to be used as a crystal driver. A crystal can be placed between the CLI and CLO pins to generate the master clock for the AD9923A. For more information on using a crystal, see Figure 80.

High Speed Clock Programmability

Figure 18 shows how the RG, HL, H1 to H4, SHP, and SHD high speed clocks are generated. The RG pulse has programmable rising and falling edges and can be inverted using the polarity control. The HL, H1, and H3 horizontal clocks have programmable rising and falling edges and polarity control. The H2 and H4 clocks are inverses of the H1 and H3 clocks, respectively. Table 10 summarizes the high speed timing registers and their parameters. Figure 19 shows the typical 2-phase, H-clock operation, in which H3 and H4 are programmed for the same edge location as H1 and H2.

The edge location registers are six bits wide, but there are only 48 valid edge locations available. Therefore, the register values are mapped into four quadrants, each of which contains 12 edge locations. Table 11 shows the correct register values for the corresponding edge locations. Figure 20 shows the default timing locations for high speed clock signals.

H-Driver and RG Outputs

In addition to the programmable timing positions, the AD9923A features on-chip output drivers for the RG and H1 to H4 outputs. These drivers are powerful enough to directly drive the CCD inputs. The H-driver and RG current can be adjusted for optimum rise/fall times in a particular load by using the H1 to H4, HL, and RGDRV registers (Address 0x36). The 3-bit drive setting for each output can be adjusted in 4.1 mA increments, with the minimum setting of 0 equal to 0 mA or three-state, and the maximum setting of 7 equal to 30.1 mA.

As shown in Figure 18, Figure 19, and Figure 20, the H2 and H4 outputs are inverses of H1 and H3 outputs, respectively. The H1/H2 crossover voltage is approximately 50% of the output swing. The crossover voltage is not programmable.

Digital Data Outputs

The AD9923A data output and DCLK phase are programmable using the DOUTPHASE register (Address 0x38, Bits[5:0]). Any edge from 0 to 47 can be programmed, as shown in Figure 21. Normally, the DOUT and DCLK signals track in phase, based on the DOUTPHASE register contents. The DCLK output phase can also be held fixed with respect to the data outputs by setting the DCLKMODE register to high (Address 0x38, Bit[8]). In this mode, the DCLK output remains at a fixed phase equal to a delayed version of CLI, and the data output phase remains programmable. For more detail, see the Analog Front End Description/Operation section.

There is a fixed output delay from the DCLK rising edge to the DOUT transition, called t_{OD}. This delay can be programmed to four values between 0 ns and 12 ns, using the DOUTDELAY register (Address 0x38, Bits[10:9]). The default value is 8 ns.

The pipeline delay through the AD9923A is shown in Figure 22. After the CCD input is sampled by SHD, there is a 16-cycle delay before the data is available.

Table 10. Timing Core Register Parameters for HL, H1 to H4, RG, SHP/SHD

Parameter	Length (Bits)	Range	Description
Polarity	1	High/low	Polarity control for HL, H1, H3, and RG (0 = no inversion, 1 = inversion)
Positive Edge	6	0 to 47 edge location	Positive edge location for HL, H1, H3, and RG (H2/H4 are inverses of H1/H3, respectively)
Negative Edge	6	0 to 47 edge location	Negative edge location for HL, H1, H3, and RG (H2/H4 are inverses of H1/H3, respectively)
Sampling Location	6	0 to 47 edge location	Sampling location for internal SHP and SHD signals
Drive Strength	3	0 to 7 current steps	Drive current for HL, H1 to H4, and RG outputs (4.1 mA per step)

Table 11. *Precision Timing* Edge Locations

Quadrant	Edge Location (Decimal)	Register Value (Decimal)	Register Value (Binary)
I	0 to 11	0 to 11	000000 to 001011
II	12 to 23	16 to 27	010000 to 011011
III	24 to 35	32 to 43	100000 to 101011
IV	36 to 47	48 to 59	110000 to 111011

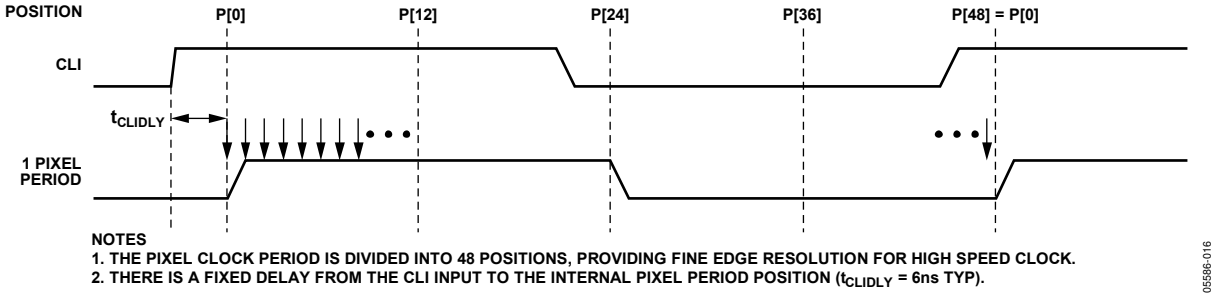


Figure 17. High Speed Clock Resolution from CLI Master Clock Input

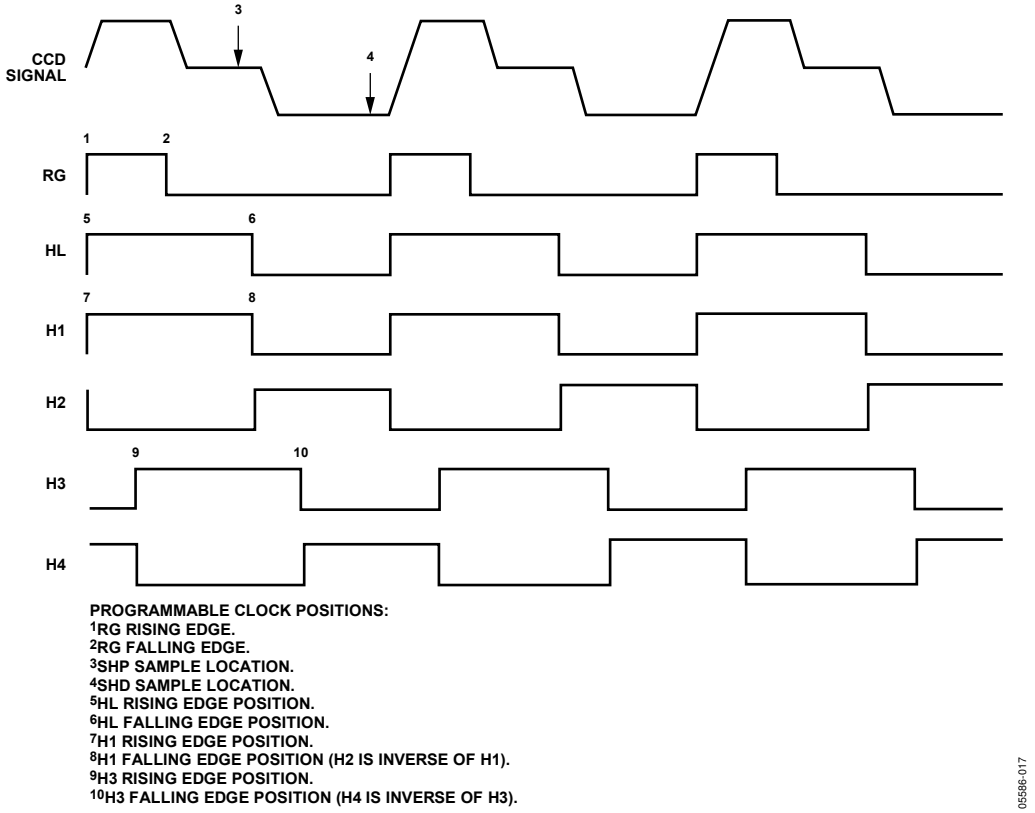
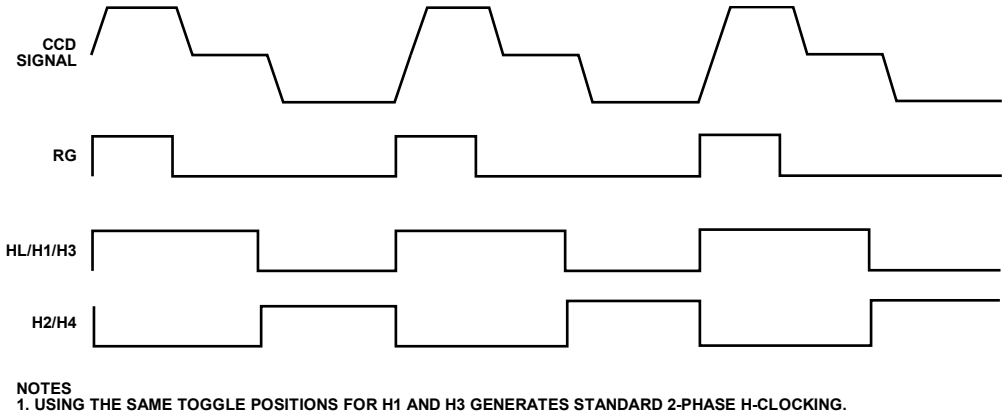
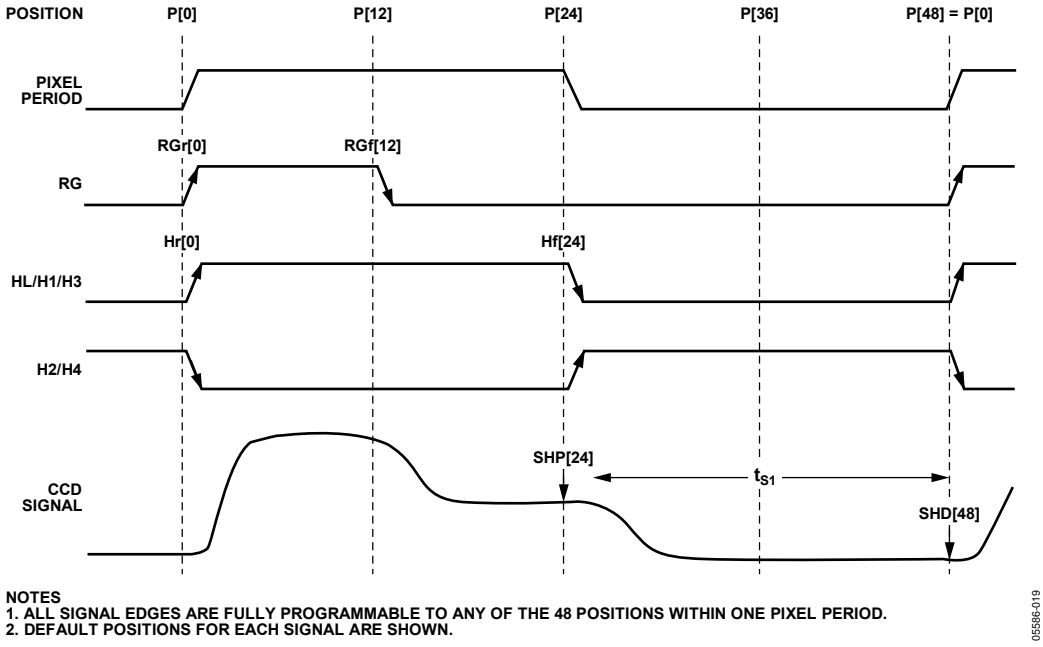


Figure 18. High Speed Clock Programmable Locations



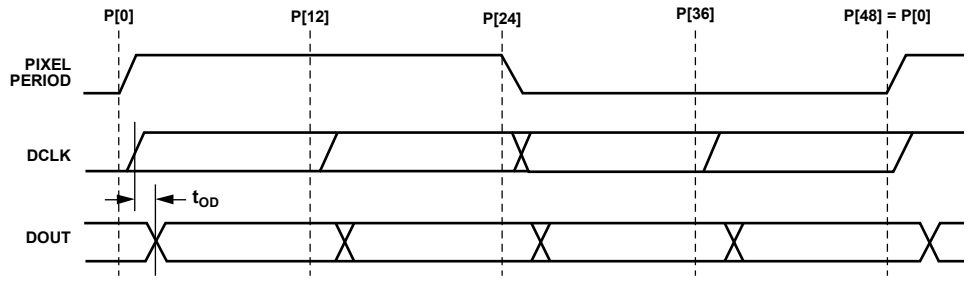
NOTES
1. USING THE SAME TOGGLE POSITIONS FOR H1 AND H3 GENERATES STANDARD 2-PHASE H-CLOCKING.

Figure 19. 2-Phase H-Clock Operation



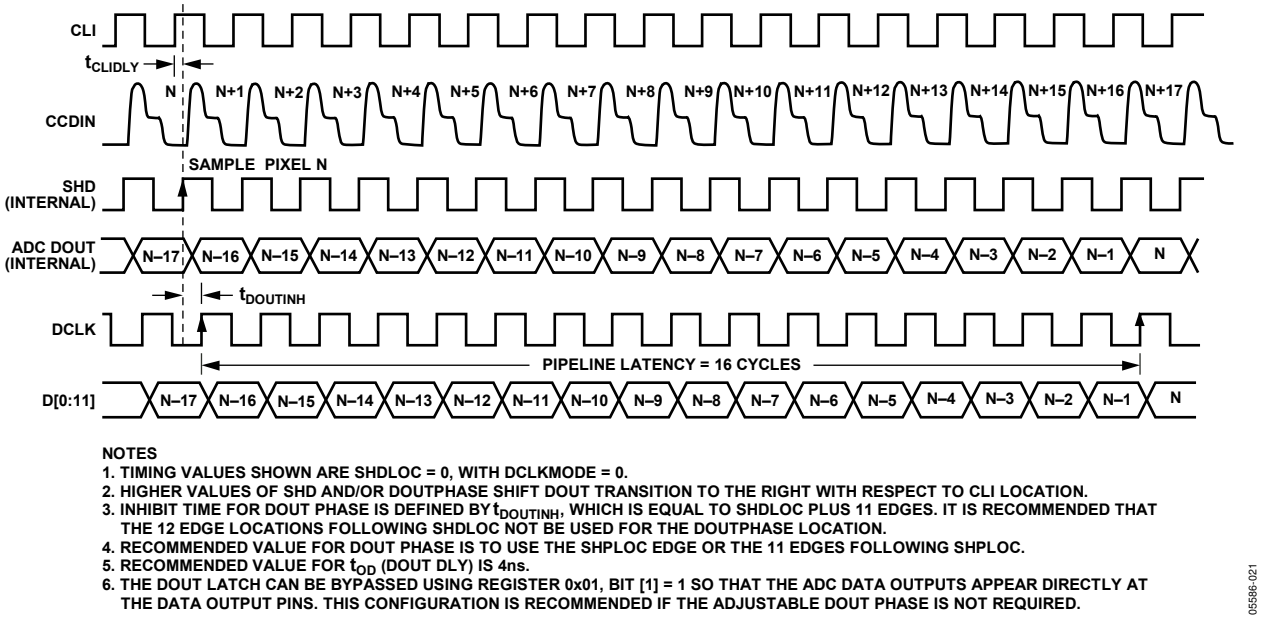
NOTES
1. ALL SIGNAL EDGES ARE FULLY PROGRAMMABLE TO ANY OF THE 48 POSITIONS WITHIN ONE PIXEL PERIOD.
2. DEFAULT POSITIONS FOR EACH SIGNAL ARE SHOWN.

Figure 20. High Speed Timing Default Locations



NOTES
1. DATA OUTPUT (DOUT) AND DCLK PHASE ARE ADJUSTABLE WITH RESPECT TO THE PIXEL PERIOD.
2. WITHIN 1 CLOCK PERIOD, THE DATA TRANSITION CAN BE PROGRAMMED TO 48 DIFFERENT LOCATIONS.
3. OUTPUT DELAY (t_{OD}) FROM DCLK RISING EDGE TO DOUT RISING EDGE IS PROGRAMMABLE.

Figure 21. Digital Output Phase Adjustment



NOTES
1. TIMING VALUES SHOWN ARE SHDLOC = 0, WITH DCLKMODE = 0.
2. HIGHER VALUES OF SHD AND/OR DOUTPHASE SHIFT DOUT TRANSITION TO THE RIGHT WITH RESPECT TO CLI LOCATION.
3. INHIBIT TIME FOR DOUT PHASE IS DEFINED BY $t_{DOUTINH}$, WHICH IS EQUAL TO SHDLOC PLUS 11 EDGES. IT IS RECOMMENDED THAT THE 12 EDGE LOCATIONS FOLLOWING SHDLOC NOT BE USED FOR THE DOUTPHASE LOCATION.
4. RECOMMENDED VALUE FOR DOUT PHASE IS TO USE THE SHPLOC EDGE OR THE 11 EDGES FOLLOWING SHPLOC.
5. RECOMMENDED VALUE FOR t_{OD} (DOUT DLY) IS 4ns.
6. THE DOUT LATCH CAN BE BYPASSED USING REGISTER 0x01, BIT [1] = 1 SO THAT THE ADC DATA OUTPUTS APPEAR DIRECTLY AT THE DATA OUTPUT PINS. THIS CONFIGURATION IS RECOMMENDED IF THE ADJUSTABLE DOUT PHASE IS NOT REQUIRED.

Figure 22. Digital Data Output Pipeline Delay

HORIZONTAL CLAMPING AND BLANKING

The AD9923A horizontal clamping and blanking pulses are fully programmable to suit a variety of applications. Individual controls are provided for CLPOB, PBLK, and HBLK during different regions of each field. This allows dark pixel clamping and blanking patterns to be changed at each stage of the readout to accommodate different image transfer timing and high speed line shifts.

Individual CLPOB and PBLK Patterns

The AFE horizontal timing consists of CLPOB and PBLK, as shown in Figure 23. These two signals are independently programmed using the registers in Table 12. SPOL is the start polarity for the signal, and TOG1 and TOG2 are the first and second toggle positions of the pulse. Both signals are active low and should be programmed accordingly.

A separate pattern for CLPOB and PBLK can be programmed for each V-sequence. As described in the Vertical Timing Generation section, several V-sequences can be created, each containing a unique pulse pattern for CLPOB and PBLK.

Figure 46 shows how the sequence change positions divide the readout field into regions. A different V-sequence can be assigned to each region, allowing the CLPOB and PBLK signals to change with each change in the vertical timing. Unused CLPOB and PBLK toggle positions should be set to 8191.

CLPOB and PBLK Masking Area

The AD9923A allows the CLPOB and/or PBLK signals to be disabled during certain lines in the field without changing the existing CLPOB and/or PBLK pattern settings.

To use CLPOB masking, the CLPMASKSTART and CLPMASKEND registers are programmed to specify the starting and ending lines in the field where the CLPOB patterns are ignored. There are three sets of CLPMASKSTART and CLPMASKEND registers, allowing up to three CLPOB masking areas to be created.

CLPOB masking registers are not specific to a given V-sequence; they are active for any existing field of timing. To disable the CLPOB masking feature, set these registers to the maximum value, 0xFFF (default value).

To use PBLK masking, the PBLKMASKSTART and PBLKMASKEND registers are programmed to specify the starting and ending lines in the field where the PBLK patterns are ignored. There are three sets of PBLKMASKSTART and PBLKMASKEND registers, allowing the creation of up to three PBLK masking areas.

PBLK masking registers are not specific to a given V-sequence; they are active for any existing field of timing. To disable the PBLK masking feature, set these registers to the maximum value, 0xFFF (default value).

Table 12. CLPOB and PBLK Pattern Registers

Register	Length (Bits)	Range	Description
CLPOBPOL	1	High/low	Starting polarity of CLPOB for each V-sequence
PBLKPOL	1	High/low	Starting polarity of PBLK for each V-sequence
CLPOBTOG1	13	0 to 8191 pixel location	First CLPOB toggle position within the line for each V-sequence
CLPOBTOG2	13	0 to 8191 pixel location	Second CLPOB toggle position within the line for each V-sequence
PBLKTOG1	13	0 to 8191 pixel location	First PBLK toggle position within the line for each V-sequence
PBLKBTOG2	13	0 to 8191 pixel location	Second PBLK toggle position within the line for each V-sequence
CLPMASKSTART	12	0 to 4095 line location	CLPOB masking area—starting line within the field (maximum of three areas)
CLPMASKEND	12	0 to 4095 line location	CLPOB masking area—ending line within the field (maximum of three areas)
PBLKMASKSTART	12	0 to 4095 line location	PBLK masking area—starting line within the field (maximum of three areas)
PBLKMASKEND	12	0 to 4095 line location	PBLK masking area—ending line within the field (maximum of three areas)

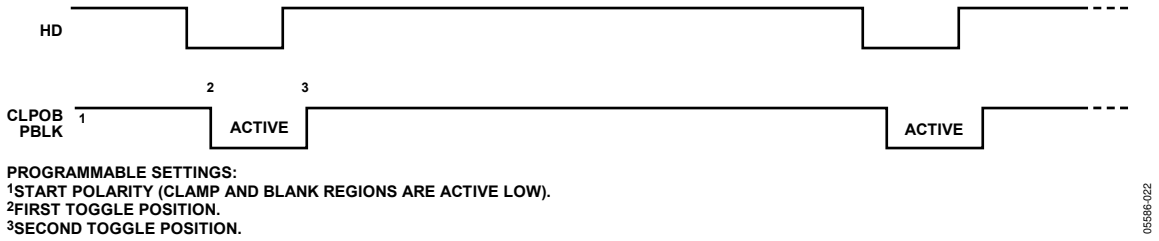


Figure 23. Clamp and Preblank Pulse Placement

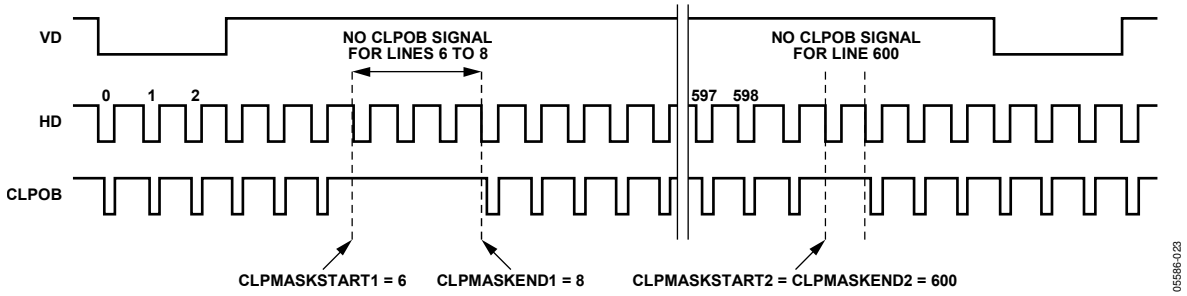


Figure 24. CLPOB Masking Example

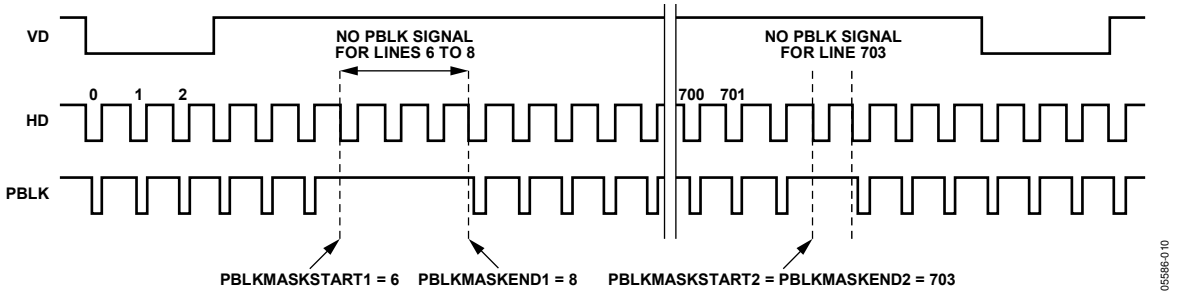


Figure 25. PBLK Masking Example

Individual HBLK Patterns

The HBLK programmable timing shown in Figure 26 is similar to CLPOB and PBLK; however, there is no start polarity control. Only the toggle positions are used to designate the start and end positions of the blanking period. Additionally, there is a polarity control register, HBLKMASK, that designates the polarity of the horizontal clock signals during the blanking period. Setting HBLKMASK high sets H1 = H3 = high and H2 = H4 = low during blanking, as shown in Figure 27. As with CLPOB and PBLK registers, HBLK registers are available in each V-sequence, allowing different blanking signals to be used with different vertical timing sequences.

Note that 8189 is the recommended setting for any unused HBLK toggle locations on the AD9923A, regardless of the setting for HBLKALT. 8190 and 8191 are not valid settings for HBLK toggle positions that are unused and causes undesired HBLK toggle activity.

Generating Special HBLK Patterns

There are six toggle positions available for HBLK. Normally, only two of the toggle positions are used to generate the standard HBLK interval. However, additional toggle positions can be used to generate special HBLK patterns, as shown in Figure 28. The pattern in this example uses all six toggle positions to generate two extra groups of pulses during the HBLK interval. By changing the toggle positions, different patterns can be created.

Table 13. HBLK Pattern Registers

Register	Length (Bits)	Range	Description
HBLKMASK	1	High/low	Masking polarity for H1, H3, HL (0 = mask low, 1 = mask high)
HBLKALT	3	0 to 7 alternation modes	Enables different odd/even alternation of HBLK toggle positions 0: disable alternation (HBLKTOGE1 to HBLKTOGE6 registers are used for each line) 1: TOGE1 and TOGE2 odd lines, TOGE3 to TOGE6 even lines 2: TOGE1 and TOGE2 even lines, TOGE3 to TOGE6 odd lines 3: TOGE1 to TOGE6 even lines, TOGO1 to TOGE6 odd lines (FREEZE/RESUME not available) 4 to 7: HBLKSTART, HBLKEND, HBLKLEN, and HBLKREP registers are used for each line
HBLKTOGE1	13	0 to 8189 pixel location	HBLK first toggle position (for even lines only when HBLKALT = 3)
HBLKTOGE2	13	0 to 8189 pixel location	HBLK second toggle position (for even lines only when HBLKALT = 3)
HBLKTOGE3	13	0 to 8189 pixel location	HBLK third toggle position (for even lines only when HBLKALT = 3)
HBLKTOGE4	13	0 to 8189 pixel location	HBLK fourth toggle position (for even lines only when HBLKALT = 3)
HBLKTOGE5	13	0 to 8189 pixel location	Fifth toggle position, even lines (HBLKSTART when HBLKALT = 4 to 7)
HBLKTOGE6	13	0 to 8189 pixel location	Sixth toggle position, even lines (HBLKEND when HBLKALT = 4 to 7)
HBLKLEN	13	0 to 8189 pixels	HBLK pattern length, only used when HBLKALT = 4 to 7
HBLKREP	8	0 to 255 repetitions	Number of HBLK pattern repetitions, only used when HBLKALT = 4 to 7
HBLKTOGO1	13	0 to 8189 pixel location	First toggle position for odd lines when HBLKALT = 3 (usually VREPA_3)
HBLKTOGO2	13	0 to 8189 pixel location	Second toggle position for odd lines when HBLKALT = 3 (usually VREPA_4)
HBLKTOGO3	13	0 to 8189 pixel location	Third toggle position for odd lines when HBLKALT = 3 (usually FREEZE1)
HBLKTOGO4	13	0 to 8189 pixel location	Fourth toggle position for odd lines when HBLKALT = 3 (usually RESUME1)
HBLKTOGO5	13	0 to 8189 pixel location	Fifth toggle position for odd lines when HBLKALT = 3 (usually FREEZE2)
HBLKTOGO6	13	0 to 8189 pixel location	Sixth toggle position for odd lines when HBLKALT = 3 (usually RESUME2)

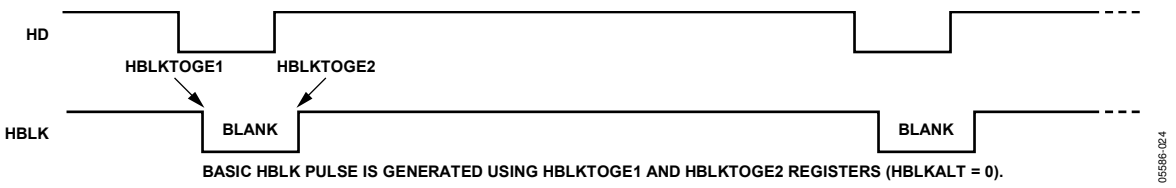


Figure 26. Typical Horizontal Blanking (HBLK) Pulse Placement

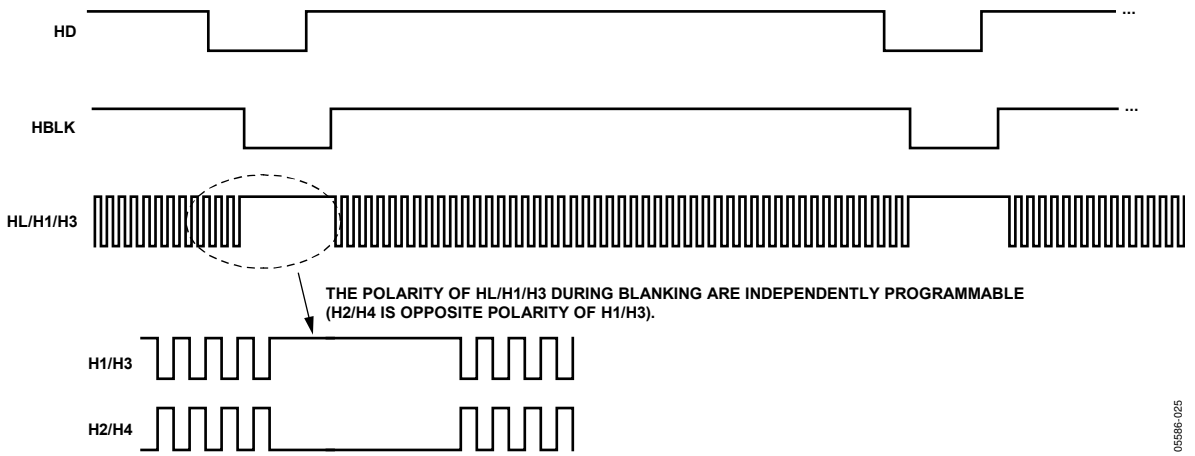


Figure 27. HBLK Masking Polarity Control

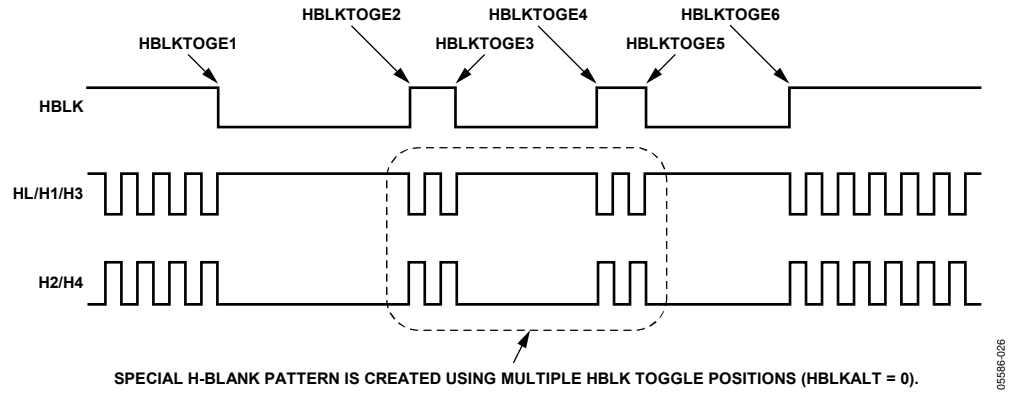
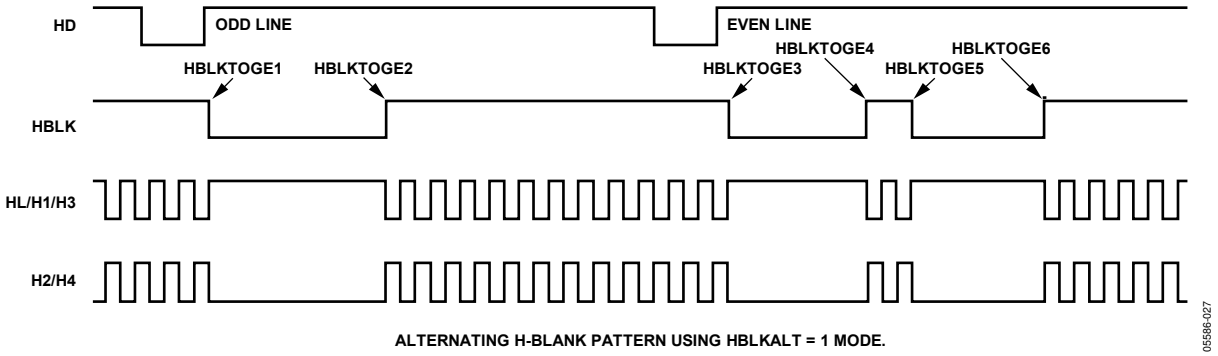


Figure 28. Using Multiple Toggle Positions for HBLK (HBLKALT = 0)

Generating HBLK Line Alternation

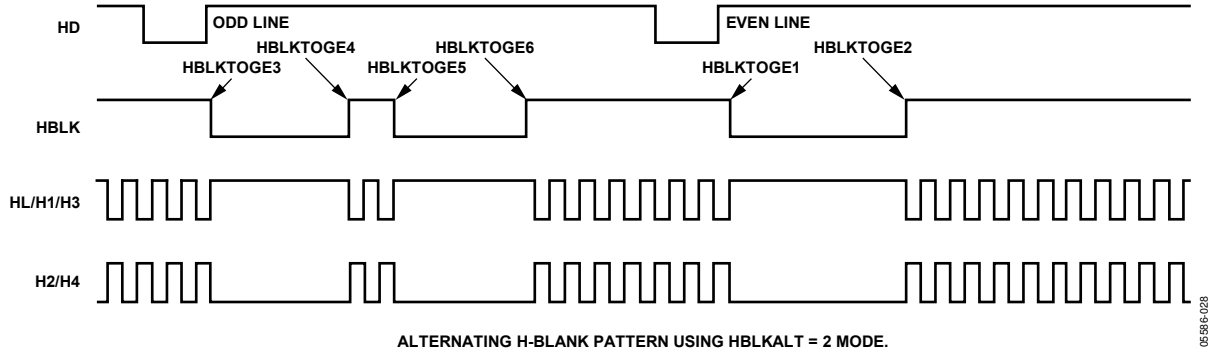
The AD9923A can alternate different HBLK toggle positions on odd and even lines. This feature can be used in conjunction with V-pattern odd/even alternation, or on its own. When 1 is written to the HBLKALT register, HBLKTOGE1 and HBLKTOGE2 are used on odd lines, and HBLKTOGE3 to HBLKTOGE6 are used on even lines. Writing 2 to the HBLKALT register gives the opposite result: HBLKTOGE1 and HBLKTOGE2 are used on even lines, and HBLKTOGE3 to HBLKTOGE6 are used on odd lines. When 3 is written to the HBLKALT register, all six even toggle positions, HBLKTOGE1 to HBLKTOGE6, are used on even lines. There are also six additional toggle positions, HBLKTOGO1 to HBLKTOGE6, for odd lines. These registers are normally used for VPAT Group A, VPAT Group B, and freeze/resume functions, but when HBLKALT = 3, these registers become the odd line toggle positions for HBLK.

Another HBLK feature is enabled by writing 4, 5, 6, or 7 to HBLKALT. In these modes, the HBLK pattern is generated using a different set of registers—HBLKSTART, HBLKEND, HBLKLEN, and HBLKREP—along with four toggle positions. This allows for multiple repeats of the HBLK signal, as shown in Figure 32.



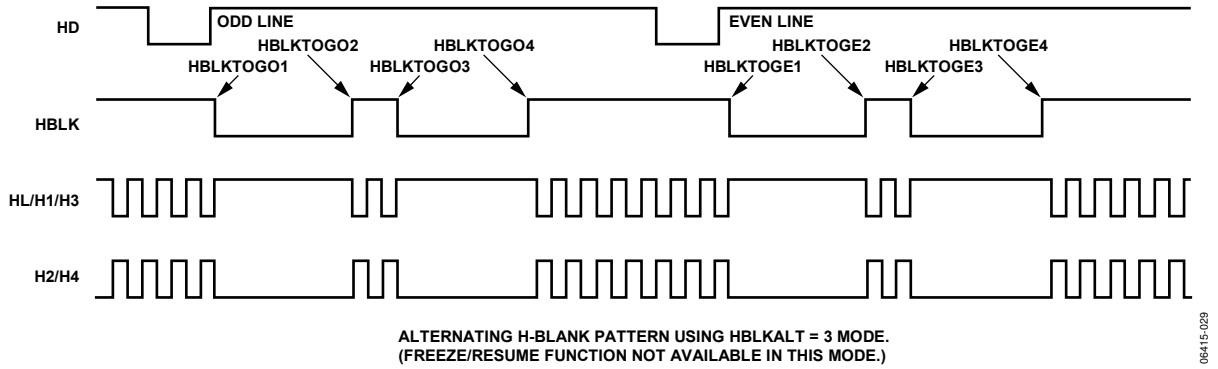
ALTERNATING H-BLANK PATTERN USING HBLKALT = 1 MODE.

Figure 29. HBLK Odd/Even Alternation Using HBLKALT = 1



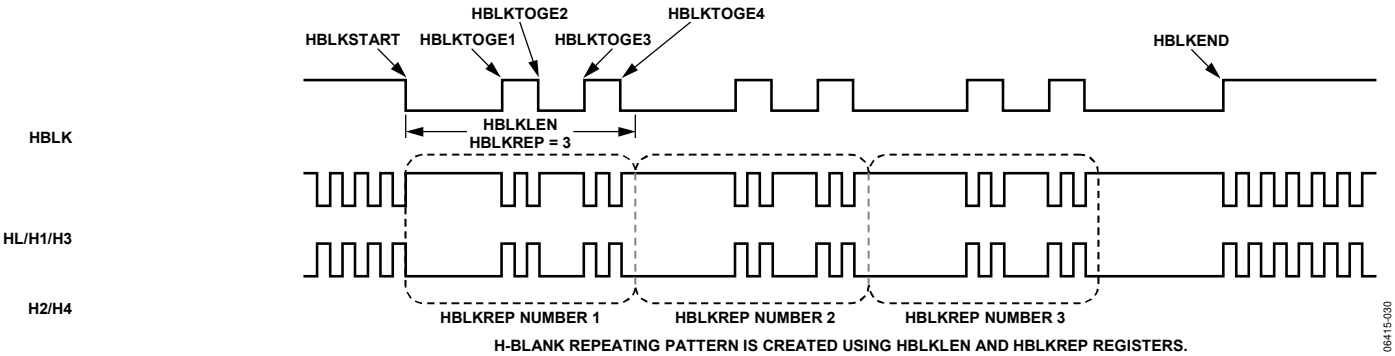
ALTERNATING H-BLANK PATTERN USING HBLKALT = 2 MODE.

Figure 30. HBLK Odd/Even Alternation Using HBLKALT = 2



ALTERNATING H-BLANK PATTERN USING HBLKALT = 3 MODE.
(FREEZE/RESUME FUNCTION NOT AVAILABLE IN THIS MODE.)

Figure 31. HBLK Odd/Even Alternation Using HBLKALT = 3



H-BLANK REPEATING PATTERN IS CREATED USING HBLKLEN AND HBLKREP REGISTERS.

Figure 32. HBLK Repeating Pattern Using HBLKALT = 4 to 7

Increasing H-Clock Width During HBLK

The AD9923A allows the H1 to H4 pulse width to be increased during the HBLK interval. The H-clock pulse width can increase by reducing the H-clock frequency (see Table 14).

The HBLKWIDTH register (Register 0x35, Bits[6:4]) is a 3-bit register that allows the H-clock frequency to be reduced by 1/2, 1/4, 1/6, 1/8, 1/10, 1/12, or 1/14. The reduced frequency only occurs for H1 to H4 pulses that are located within the HBLK area.

Horizontal Timing Sequence Example

Figure 33 shows an example of a CCD layout. The horizontal register contains 28 dummy pixels that occur on each line clocked from the CCD. In the vertical direction, there are 10 optical black (OB) lines at the front of the readout and two at the back of the readout. The horizontal direction has four OB pixels in the front and 48 OB pixels in the back.

Figure 34 shows the basic sequence layout to use during the effective pixel readout. The 48 OB pixels at the end of each line are used for CLPOB signals. PBLK is optional and it is often used to blank the digital outputs during the noneffective CCD pixels. HBLK is used during the vertical shift interval.

The HBLK, CLPOB, and PBLK parameters are programmed in the V-sequence registers. More elaborate clamping schemes can be used, such as adding a separate sequence to clamp during the entire line of OB pixels. This requires configuring a separate V-sequence for reading the OB lines.

The CLPMASKSTART and CLPMASKEND registers can be used to disable the CLPOB on a few lines without affecting the setup of the clamp sequences.

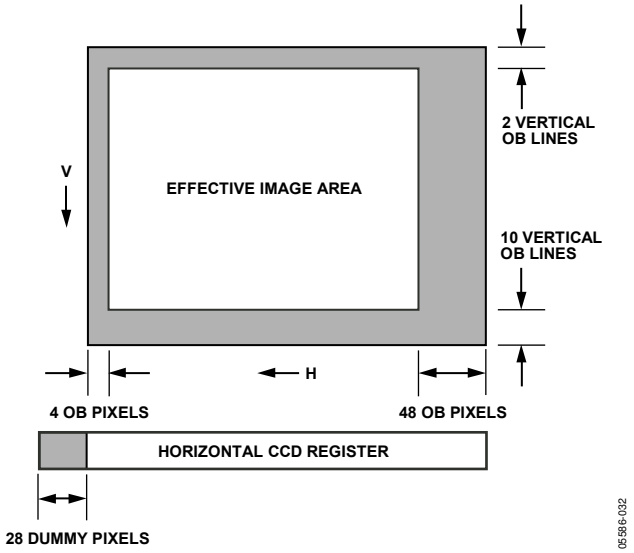


Figure 33. CCD Configuration Example

Table 14. HBLK Width Register

Register	Length (Bits)	Range	Description
HBLKWIDTH	3	1× to 1/14× pixel rate	Controls H1 to H4 width during HBLK as a fraction of pixel rate 0: same frequency as the pixel rate 1: 1/2 pixel frequency, that is, doubles the H1 to H4 pulse width 2: 1/4 pixel frequency 3: 1/6 pixel frequency 4: 1/8 pixel frequency 5: 1/10 pixel frequency 6: 1/12 pixel frequency 7: 1/14 pixel frequency

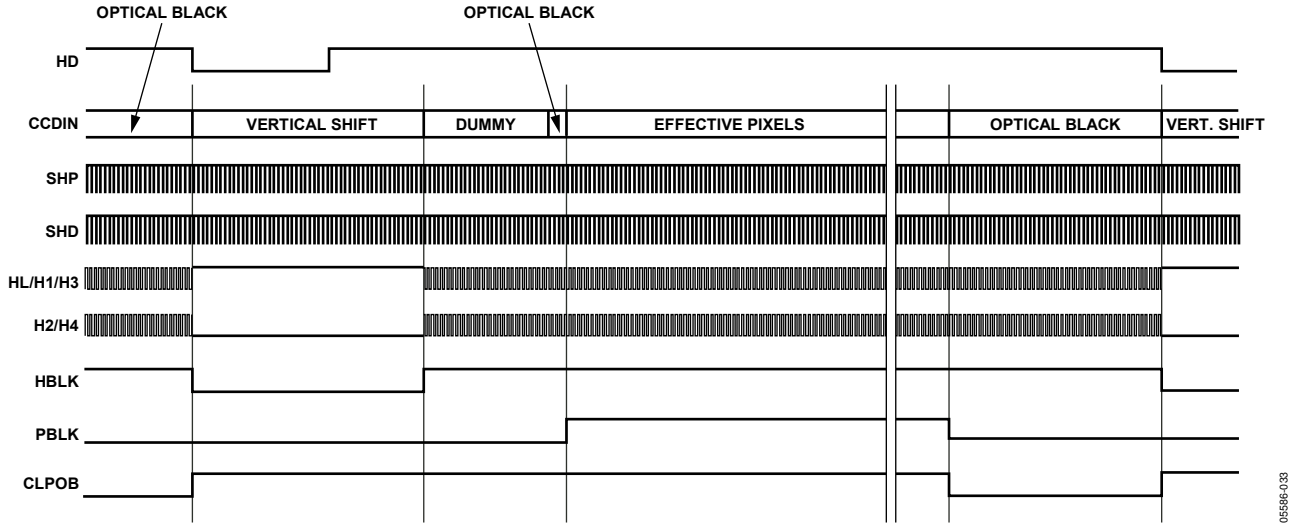


Figure 34. Horizontal Sequence Example

VERTICAL TIMING GENERATION

The AD9923A provides a very flexible solution for generating vertical CCD timing; it can support multiple CCDs and different system architectures. The 13-phase vertical transfer clocks, XV1 to XV13, are used to shift lines of pixels into the horizontal output register of the CCD. The AD9923A allows these outputs to be individually programmed into various readout configurations, using a four-step process as shown in Figure 35.

1. Use the vertical pattern group registers to create the individual pulse patterns for XV1 to XV13.
2. Use the V-pattern groups to build the sequences and add more information.
3. Construct the readout for an entire field by dividing the field into regions and assigning a sequence to each region. Each field can contain up to nine regions to accommodate different steps, such as high speed line shifts and unique vertical line transfers, of the readout. The total number of V-patterns, V-sequences, and fields are programmable and limited by the number of registers. High speed line shifts and unique vertical transfers are examples of the different steps required for readout.
4. Use the MODE register to combine fields in any order for various readout configurations.

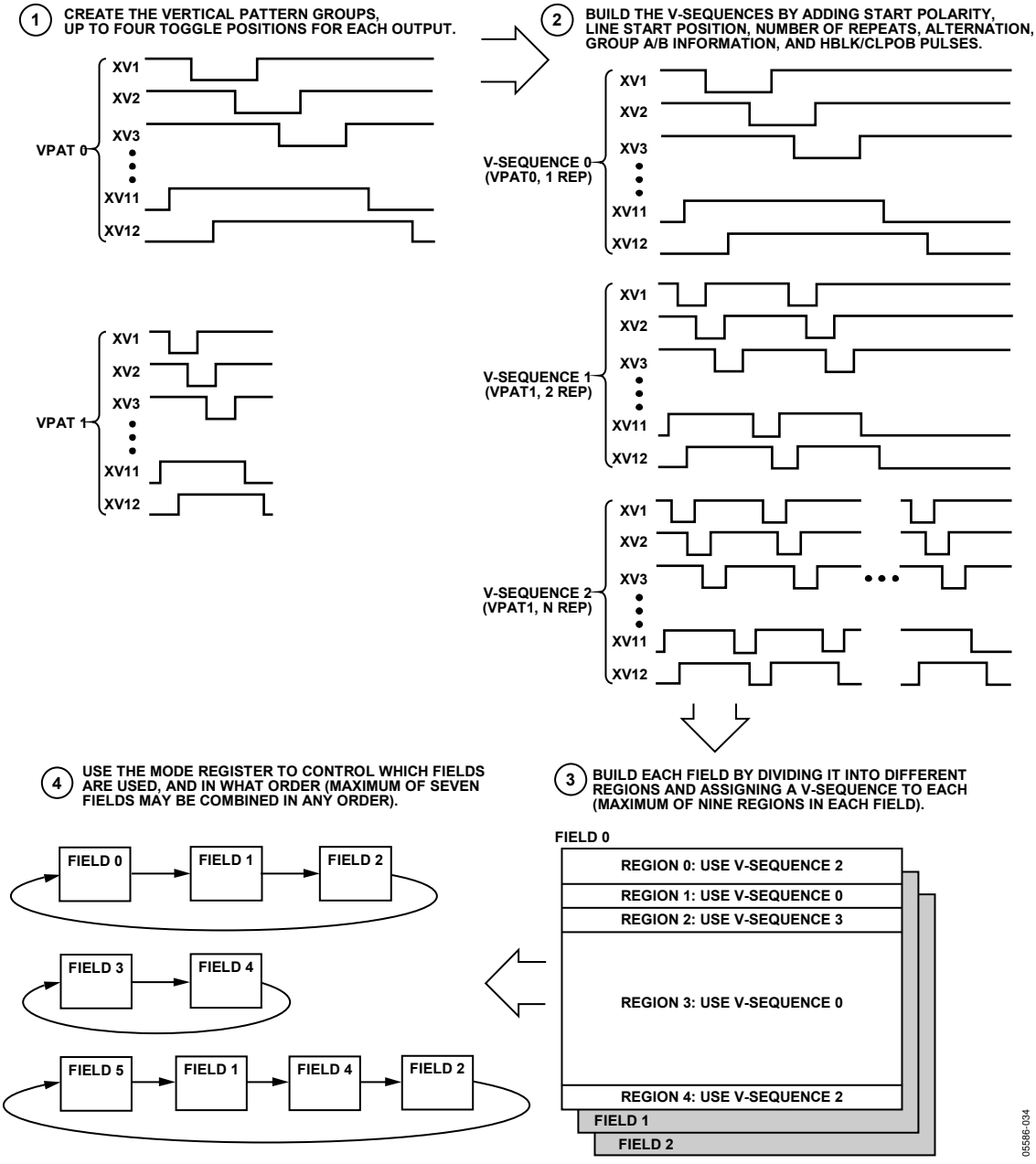


Figure 35. Summary of Vertical Timing Generation