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### FEATURES

**New AD9949A supports CCD line length > 4096 pixels**  
**Correlated double sampler (CDS)**  
**0 dB to 18 dB pixel gain amplifier (PxGA®)**  
**6 dB to 42 dB 10-bit variable gain amplifier (VGA)**  
**12-bit, 36 MSPS analog-to-digital converter (ADC)**  
**Black level clamp with variable level control**  
**Complete on-chip timing driver**  
*Precision Timing™* core with < 600 ps resolution  
**On-chip 3 V horizontal and RG drivers**  
**40-lead LFCSP package**

### APPLICATIONS

**Digital still cameras**  
**High speed digital imaging applications**

### GENERAL DESCRIPTION

The AD9949 is a highly integrated CCD signal processor for digital still camera applications. Specified at pixel rates of up to 36 MHz, the AD9949 consists of a complete analog front end with A/D conversion, combined with a programmable timing driver. The *Precision Timing* core allows adjustment of high speed clocks with < 600 ps resolution.

The analog front end includes black level clamping, CDS, PxGA, VGA, and a 36 MSPS, 12-bit ADC. The timing driver provides the high speed CCD clock drivers for RG and H1 to H4. Operation is programmed using a 3-wire serial interface.

Packaged in a space-saving, 40-lead LFCSP package, the AD9949 is specified over an operating temperature range of  $-20^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

### FUNCTIONAL BLOCK DIAGRAM

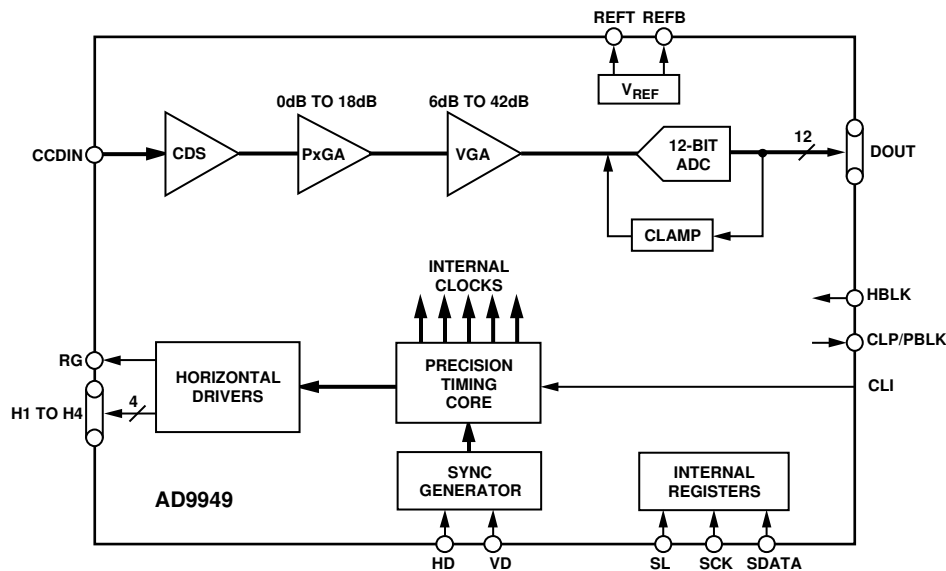


Figure 1.

### Rev. B

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## COMPARABLE PARTS

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## DOCUMENTATION

### Data Sheet

- AD9949: 12-Bit CCD Signal Processor with *Precision Timing*™ Core Data Sheet

## DESIGN RESOURCES

- AD9949 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

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## REVISION HISTORY

### 11/04—Data Sheet Changed from Rev. A to Rev. B

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### 9/04—Data Sheet Changed from Rev. 0 to Rev. A

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Changes to Terminology Section.....	9
Added H-Counter Behavior Section.....	12
Changes to Table 7.....	14

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Changes to Ordering Guide .....	35

### 5/03—Revision 0: Initial Version

## SPECIFICATIONS

### GENERAL SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating	-20		+85	°C
Storage	-65		+150	°C
MAXIMUM CLOCK RATE	36			MHz
POWER SUPPLY VOLTAGE				
AVDD, TCVDD (AFE, Timing Core)	2.7	3.0	3.6	V
HVDD (H1 to H4 Drivers)	2.7	3.0	3.6	V
RGVDD (RG Driver)	2.7	3.0	3.6	V
DRVDD (D0 to D11 Drivers)	2.7	3.0	3.6	V
DVDD (All Other Digital)	2.7	3.0	3.6	V
POWER DISSIPATION				
36 MHz, HVDD = RGVDD = 3 V, 100 pF H1 to H4 Loading <sup>1</sup>		320		mW
Total Shutdown Mode		1		mW

<sup>1</sup> The total power dissipated by the HVDD supply may be approximated using the equation  
 Total HVDD Power = (CLOAD x HVDD x Pixel Frequency) x HVDD x (Number of H – Outputs Used)  
 Reducing the H-loading, using only two of the outputs, and/or using a lower HVDD supply, reduces the power dissipation.

### DIGITAL SPECIFICATIONS

T<sub>MIN</sub> to T<sub>MAX</sub>, AVDD = DVDD = DRVDD = HVDD = RGVDD = 2.7 V, C<sub>L</sub> = 20 pF, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V <sub>IH</sub>	2.1			V
Low Level Input Voltage	V <sub>IL</sub>			0.6	V
High Level Input Current	I <sub>IH</sub>		10		μA
Low Level Input Current	I <sub>IL</sub>		10		μA
Input Capacitance	C <sub>IN</sub>		10		pF
LOGIC OUTPUTS					
High Level Output Voltage, I <sub>OH</sub> = 2 mA	V <sub>OH</sub>	2.2			V
Low Level Output Voltage, I <sub>OL</sub> = 2 mA	V <sub>OL</sub>			0.5	V
CLI INPUT					
High Level Input Voltage (TCVDD/2 + 0.5 V)	V <sub>IH-CLI</sub>	1.85			V
Low Level Input Voltage	V <sub>IL-CLI</sub>			0.85	V
RG AND H-DRIVER OUTPUTS					
High Level Output Voltage (RGVDD – 0.5 V and HVDD – 0.5 V)	V <sub>OH</sub>	2.2			V
Low Level Output Voltage	V <sub>OL</sub>			0.5	V
Maximum Output Current (Programmable)			30		mA
Maximum Load Capacitance		100			pF

# AD9949

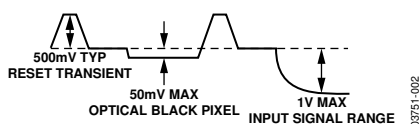
## ANALOG SPECIFICATIONS

$T_{MIN}$  to  $T_{MAX}$ ,  $AVDD = DVDD = 3.0\text{ V}$ ,  $f_{CLI} = 36\text{ MHz}$ , typical timing specifications, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Notes
<b>CDS</b>					
Gain		0		dB	
Allowable CCD Reset Transient <sup>1</sup>		500		mV	
Maximum Input Range before Saturation <sup>1</sup>	1.0			V p-p	
Maximum CCD Black Pixel Amplitude <sup>1</sup>		±50		mV	
<b>PIXEL GAIN AMPLIFIER (P×GA)</b>					
Gain Control Resolution		256		Steps	
Gain Monotonicity					
Minimum Gain		0		dB	
Maximum Gain		18		dB	
<b>VARIABLE GAIN AMPLIFIER (VGA)</b>					
Maximum Input Range	1.0			V p-p	
Maximum Output Range	2.0			V p-p	
Gain Control Resolution		1024		Steps	
Gain Monotonicity		Guaranteed			
Gain Range					
Minimum Gain (VGA Code 0)		6		dB	
Maximum Gain (VGA Code 1023)		42		dB	
<b>BLACK LEVEL CLAMP</b>					
Clamp Level Resolution		256		Steps	
Clamp Level					Measured at ADC output
Minimum Clamp Level (0)		0		LSB	
Maximum Clamp Level (255)		255		LSB	
<b>A/D CONVERTER</b>					
Resolution	12			Bits	
Differential Nonlinearity (DNL)	-1.0	±0.5	+1.0	LSB	
No Missing Codes		Guaranteed			
Integral Nonlinearity (INL)			8	LSB	
Full-Scale Input Voltage		2.0		V	
<b>VOLTAGE REFERENCE</b>					
Reference Top Voltage (REFT)		2.0		V	
Reference Bottom Voltage (REFB)		1.0		V	
<b>SYSTEM PERFORMANCE</b>					
VGA Gain Accuracy					Specifications include entire signal chain
Minimum Gain (Code 0)	5.0	5.5	6.0	dB	
Maximum Gain (Code 1023)	40.5	41.5	42.5	dB	
Peak Nonlinearity, 500 mV Input Signal		0.15	0.6	%	12 dB gain applied
Total Output Noise		0.8		LSB rms	AC grounded input, 6 dB gain applied
Power Supply Rejection (PSR)		50		dB	Measured with step change on supply

<sup>1</sup> Input signal characteristics defined as follows:



**TIMING SPECIFICATIONS**

$C_L = 20$  pF,  $f_{CLI} = 36$  MHz, unless otherwise noted.

**Table 4.**

Parameter	Symbol	Min	Typ	Max	Unit
MASTER CLOCK (CLI) (See Figure 16)					
CLI Clock Period	$t_{CLI}$	27.8			ns
CLI High/Low Pulse Width	$t_{ADC}$	11.2	13.9	16.6	ns
Delay from CLI to Internal Pixel Period Position	$t_{CLIDLy}$		6		ns
CLPOB PULSE WIDTH (PROGRAMMABLE) <sup>1</sup>	$t_{COB}$	2	20		Pixels
SAMPLE CLOCKS (See Figure 18)					
SHP Rising Edge to SHD Rising Edge	$t_{S1}$	12.5	13.9		ns
DATA OUTPUTS (See Figure 19 and Figure 20)					
Output Delay From Programmed Edge	$t_{OD}$		6		ns
Pipeline Delay			11		Cycles
SERIAL INTERFACE (SERIAL TIMING SHOWN IN Figure 14 and Figure 15)					
Maximum SCK Frequency	$f_{SCLK}$	10			MHz
SL to SCK Setup Time	$t_{LS}$	10			ns
SCK to SL Hold Time	$t_{LH}$	10			ns
SDATA Valid to SCK Rising Edge Setup	$t_{DS}$	10			ns
SCK Falling Edge to SDATA Valid Hold	$t_{DH}$	10			ns
SCK Falling Edge to SDATA Valid Read	$t_{DV}$	10			ns

<sup>1</sup> Minimum CLPOB pulse width is for functional operation only. Wider typical pulses are recommended to achieve low noise clamp reference.

## ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect to	Rating
AVDD and TCVDD	AVSS	-0.3 V to +3.9 V
HVDD and RGVDD	HVSS, RGVSS	-0.3 V to +3.9 V
DVDD and DRVDD	DVSS, DRVSS	-0.3 V to +3.9 V
Any VSS	Any VSS	-0.3 V to +0.3 V
Digital Outputs	DRVSS	-0.3 V to DRVDD + 0.3 V
CLPOB/PBLK and HBLK	DVSS	-0.3 V to DVDD + 0.3 V
SCK, SL, and SDATA	DVSS	-0.3 V to DVDD + 0.3 V
RG	RGVSS	-0.3 V to RGVDD + 0.3 V
H1 to H4	HVSS	-0.3 V to HVDD + 0.3 V
REFT, REFB, and CCDIN	AVSS	-0.3 V to AVDD + 0.3 V
Junction Temperature		150°C
Lead Temperature (10 s)		300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### THERMAL CHARACTERISTICS

#### Thermal Resistance

40-Lead LFCSP Package:  $\theta_{JA} = 27^{\circ}\text{C}/\text{W}^1$ .

<sup>1</sup>  $\theta_{JA}$  is measured using a 4-layer PCB with the exposed paddle soldered to the board.

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.





## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

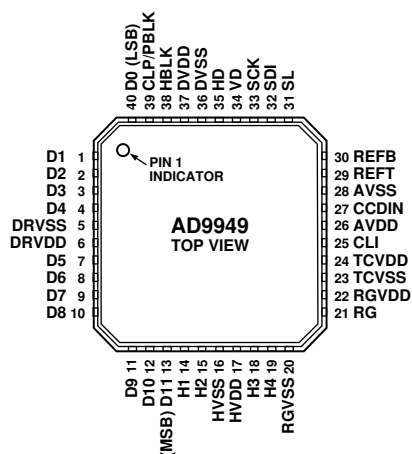


Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type <sup>1</sup>	Description
1 to 4	D1 to D4	DO	Data Outputs
5	DRVSS	P	Digital Driver Ground
6	DRVDD	P	Digital Driver Supply
7 to 13	D5 to D11	DO	Data Outputs (D11 is MSB)
14	H1	DO	CCD Horizontal Clock 1
15	H2	DO	CCD Horizontal Clock 2
16	HVSS	P	H1 to H4 Driver Ground
17	HVDD	P	H1 to H4 Driver Supply
18	H3	DO	CCD Horizontal Clock 3
19	H4	DO	CCD Horizontal Clock 4
20	RGVSS	P	RG Driver Ground
21	RG	DO	CCD Reset Gate Clock
22	RGVDD	P	RG Driver Supply
23	TCVSS	P	Analog Ground for Timing Core
24	TCVDD	P	Analog Supply for Timing Core
25	CLI	DI	Master Clock Input
26	AVDD	P	Analog Supply for AFE
27	CCDIN	AI	Analog Input for CCD Signal (Connect through Series 0.1 $\mu$ F Capacitor)
28	AVSS	P	Analog Ground for AFE
29	REFT	AO	Reference Top Decoupling (Decouple with 1.0 $\mu$ F to AVSS)
30	REFB	AO	Reference Bottom Decoupling (Decouple with 1.0 $\mu$ F to AVSS)
31	SL	DI	3-Wire Serial Load
32	SDI	DI	3-Wire Serial Data Input
33	SCK	DI	3-Wire Serial Clock
34	VD	DI	Vertical Sync Pulse
35	HD	DI	Horizontal Sync Pulse
36	DVSS	P	Digital Ground
37	DVDD	P	Digital Supply
38	HBLK	DI	Optional HBLK Input
39	CLP/PBLK	DO	CLPOB or PBLK Output
40	D0	DO	Data Output LSB

<sup>1</sup> Type: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power.

## TERMINOLOGY

### Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Thus, every code must have a finite width. No missing codes guaranteed to 12-bit resolution indicates that all 4096 codes, respectively, must be present over all operating conditions.

### Integral Nonlinearity (INL)

INL is the deviation of each individual code measured from a true straight line from zero to full scale. The point used as zero scale occurs 0.5 LSB before the first code transition. Positive full scale is defined as a level 1 LSB and 0.5 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line.

### Peak Nonlinearity

Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the output of the AD9949 from a straight line. The point used as zero scale occurs 0.5 LSB before the first code transition. Positive full scale is defined as a level 1 LSB and 0.5 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the straight line reference. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is appropriately gained up to fill the ADC's full-scale range.

### Total Output Noise

The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage, using the relationship

$$1 \text{ LSB} = (\text{ADC full scale}/2^n \text{ codes})$$

where  $n$  is the bit resolution of the ADC. For the AD9949, 1 LSB is approximately 0.488 mV.

### Power Supply Rejection (PSR)

The PSR is measured with a step change applied to the supply pins. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

# EQUIVALENT INPUT/OUTPUT CIRCUITS

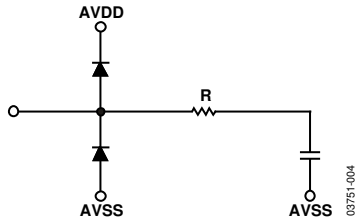


Figure 3. CCDIN (Pin 27)

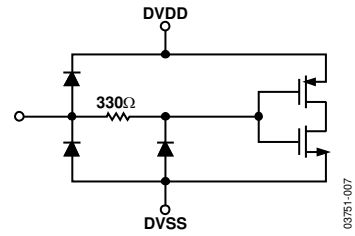


Figure 6. Digital Inputs (Pins 31 to 35, 38)

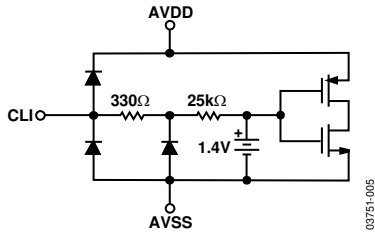


Figure 4. CLI (Pin 25)

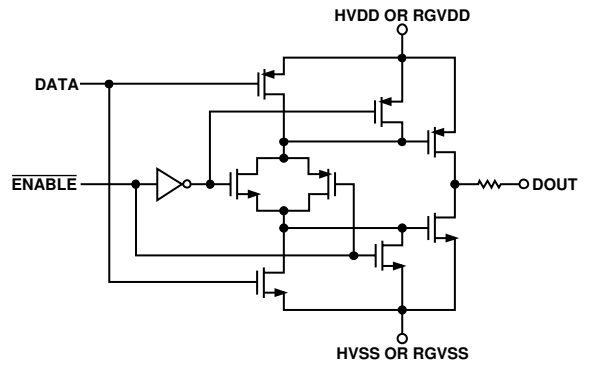


Figure 7. H1 to H4 and RG (Pins 14 to 15, 18 to 19, 21)

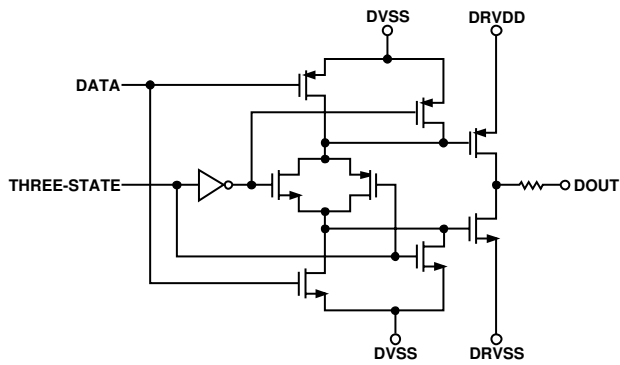


Figure 5. Data Outputs D0 to D11 (Pins 1 to 4, 7 to 13, 40)

TYPICAL PERFORMANCE CHARACTERISTICS

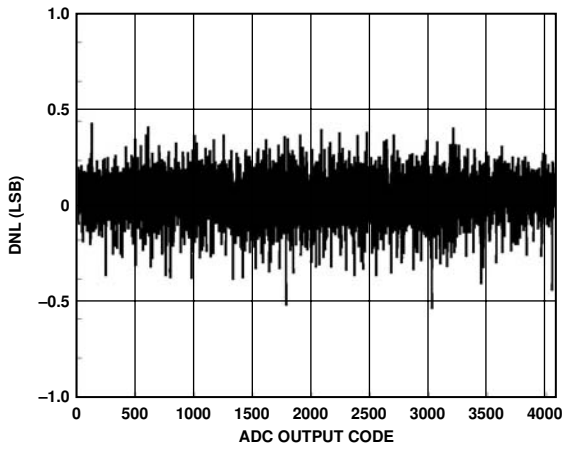


Figure 8. Typical DNL

03751-009

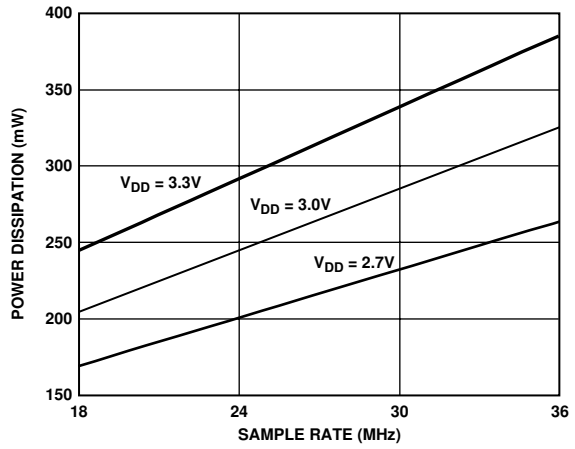


Figure 10. Power Curves

03751-011

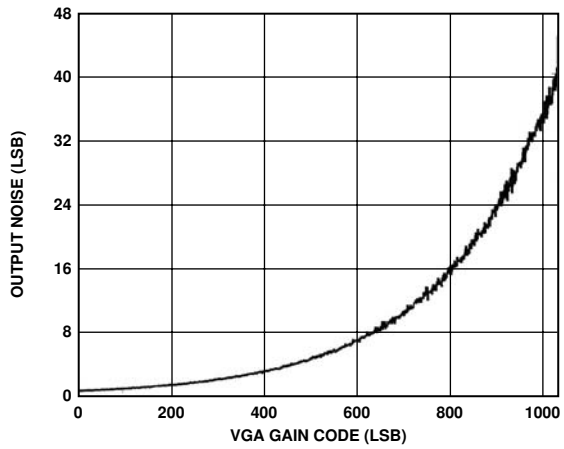


Figure 9. Output Noise vs. VGA Gain

03751-010

## SYSTEM OVERVIEW

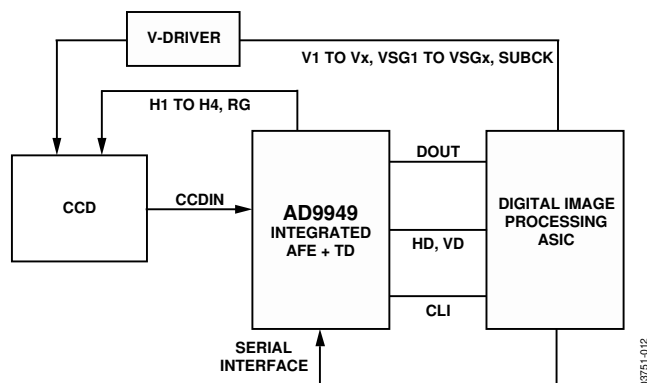


Figure 11. Typical Application

Figure 11 shows the typical system application diagram for the AD9949. The CCD output is processed by the AD9949's AFE circuitry, which consists of a CDS, a PxGA, a VGA, a black level clamp, and an ADC. The digitized pixel information is sent to the digital image processor chip where all postprocessing and compression occurs. To operate the CCD, CCD timing parameters are programmed into the AD9949 from the image processor through the 3-wire serial interface. From the system master clock, CLI, provided by the image processor, the AD9949 generates the high speed CCD clocks and all internal AFE clocks. All AD9949 clocks are synchronized with VD and HD. The AD9949's horizontal pulses (CLPOB, PBLK, and HBLK) are programmed and generated internally.

The H-drivers for H1 to H4 and RG are included in the AD9949, allowing these clocks to be directly connected to the CCD. The H-drive voltage of 3 V is supported in the AD9949.

Figure 12 shows the horizontal and vertical counter dimensions for the AD9949. All internal horizontal clocking is programmed using these dimensions to specify line and pixel locations.

## H-COUNTER BEHAVIOR

When the maximum horizontal count of 4096 pixels is exceeded, the H-counter in the AD9949 rolls over to zero and continues counting. It is, therefore, recommended that the maximum counter value not be exceeded.

However, the newer AD9949A version behaves differently. In the AD9949A, the internal H-counter holds at its maximum count of 4095 instead of rolling over. This feature allows the AD9949A to be used in applications containing a line length greater than 4096 pixels. Although no programmable values for the horizontal blanking or clamping are available beyond pixel 4095, the H, RG, and AFE clocking continues to operate, sampling the remaining pixels on the line.

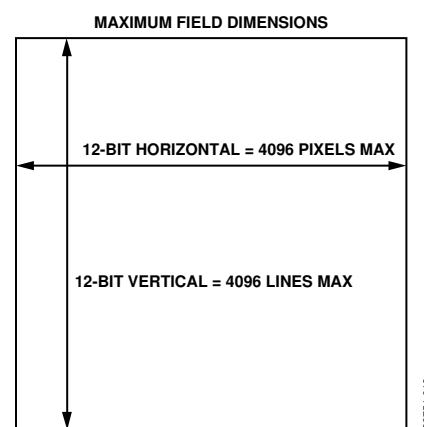


Figure 12. Vertical and Horizontal Counters

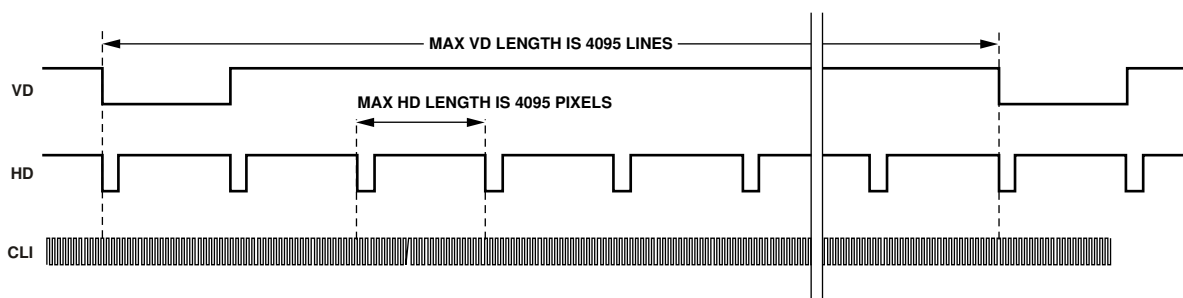
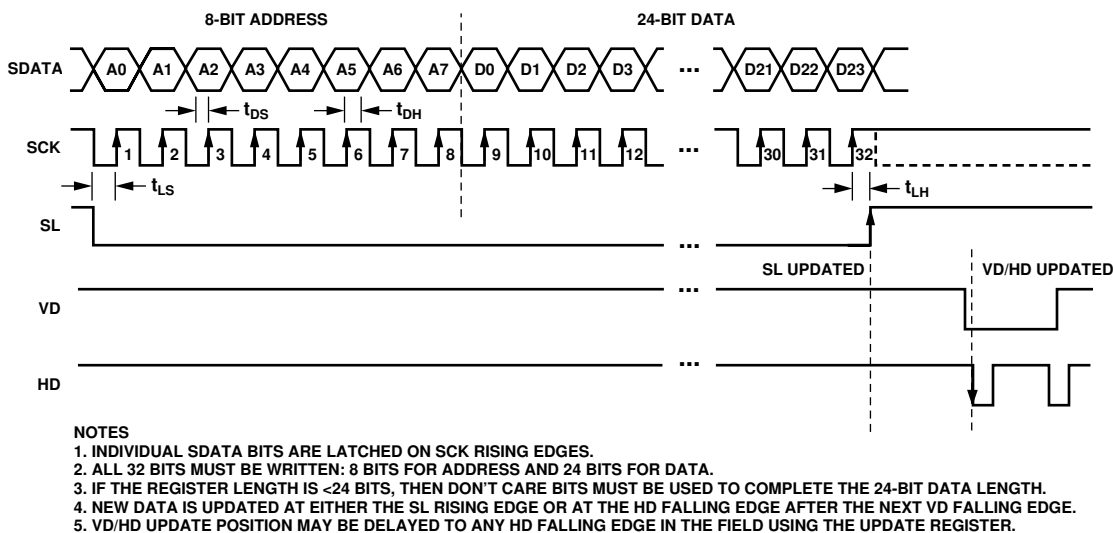


Figure 13. Maximum VD/HD Dimensions

## SERIAL INTERFACE TIMING

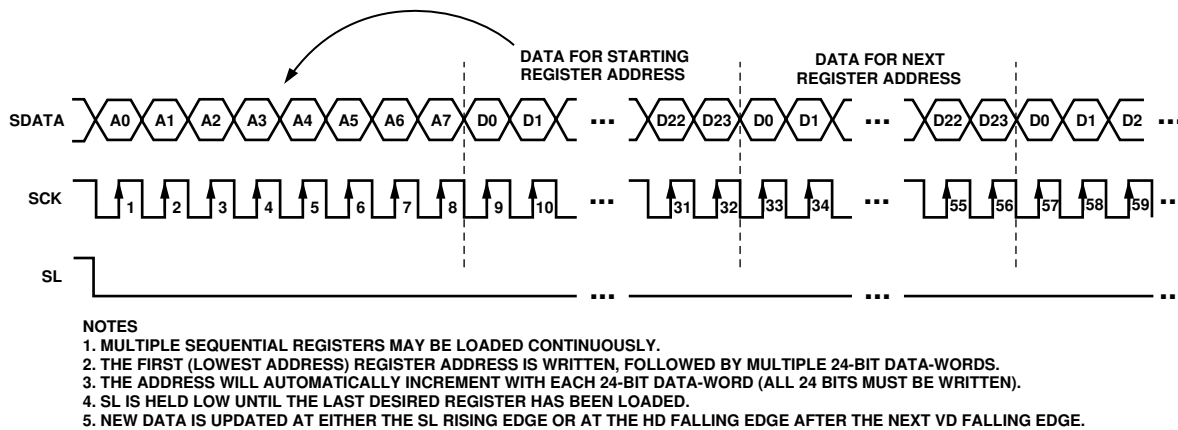
The AD9949's internal registers are accessed through a 3-wire serial interface. Each register consists of an 8-bit address and a 24-bit data-word. Both the 8-bit address and 24-bit data-word are written starting with the LSB. To write to each register, a 32-bit operation is required, as shown in Figure 14. Although many registers are less than 24 bits wide, all 24 bits must be written for each register. If the register is only 16 bits wide, then the upper eight bits may be filled with zeros during the serial write operation. If fewer than 24 bits are written, the register will not be updated with new data.

Figure 15 shows a more efficient way to write to the registers by using the AD9949's address auto-increment capability. Using this method, the lowest desired address is written first, followed by multiple 24-bit data-words. Each new 24-bit data-word is written automatically to the next highest register address. By eliminating the need to write each 8-bit address, faster register loading is achieved. Address auto-increment may be used starting with any register location and may be used to write to as few as two registers or as many as the entire register space.



03751-015

Figure 14. Serial Write Operation



03751-016

Figure 15. Continuous Serial Write Operation

## COMPLETE REGISTER LISTING

1. All addresses and default values are expressed in hexadecimal.
2. All registers are VD/HD updated as shown in Figure 14, except for the registers indicated in Table 7, which are SL updated.

**Table 7. SL Updated Registers**

<b>Register</b>	<b>Description</b>
OPRMODE	AFE Operation Modes
CTLMODE	AFE Control Modes
SW_RESET	Software Reset Bit
TGCORE_RSTB	Reset Bar Signal for Internal TG Core
PREVENTUPDATE	Prevents Update of Registers
VDHDEDGE	VD/HD Active Edge
FIELDVAL	Resets Internal Field Pulse
HBLKRETIME	Retimes the HBLK to Internal Clock
CLPBLKOUT	CLP/BLK Output Pin Select
CLPBLKEN	Enables CLP/BLK Output Pin
H1CONTROL	H1/H2 Polarity/Edge Control
RGCONTROL	RG Polarity/Edge Control
DRVCONTROL	RG and H1 to H4 Drive Current
SAMPCONTROL	SHP/SHD Sampling Edge Control
DOUPHASE	Data Output Phase Adjustment

# AD9949

Table 8. AFE Register Map

Address	Data Bit Content	Default Value	Name	Description
00	[11:0]	4	OPRMODE	AFE Operation Modes. (See Table 14.)
01	[9:0]	0	VGAGAIN	VGA Gain.
02	[7:0]	80	CLAMP LEVEL	Optical Black Clamp Level.
03	[11:0]	4	CTLMODE	AFE Control Modes. (See Table 15.)
04	[17:0]	0	PxGA GAIN01	PxGA Gain Registers for Color 0 [8:0] and Color 1 [17:9].
05	[17:0]	0	PxGA GAIN23	PxGA Gain Registers for Color 2 [8:0] and Color 3 [17:9].

Table 9. Miscellaneous Register Map

Address	Data Bit Content	Default Value	Name	Description
10	[0]	0	SW_RST	Software Reset. 1 = Reset all registers to default, then self-clear back to 0.
11	[0]	0	OUT_CONTROL	Output Control. 0 = Make all dc outputs inactive.
12	[0]	0	TGCORE_RSTB	Timing Core Reset Bar. 0 = Reset TG core. 1 = Resume operation.
13	[11:0]	0	UPDATE	Serial Update. Sets the line (HD) within the field to update serial data.
14	[0]	0	PREVENTUPDATE	Prevents the update of the VD updated registers. 1 = Prevent Update.
15	[0]	0	VDHDEDGE	VD/HD Active Edge. 0 = Falling Edge Triggered. 1 = Rising Edge Triggered.
16	[1:0]	0	FIELDVAL	Field Value Sync. 0 = Next Field 0. 1 = Next Field 1. 2/3 = Next Field 2.
17	[0]	0	HBLKRETIME	Retime HBLK to Internal H1 Clock. Preferred setting is 1. Setting to 1 adds one cycle delay to HBLK toggle positions.
18	[1:0]	0	CLPBLKOUT	CLP/BLK Pin Output Select. 0 = CLPOB. 1 = PBLK. 2 = HBLK. 3 = Low.
19	[0]	1	CLPBLKEN	Enable CLP/BLK Output. 1 = Enable.
1A	[0]	0	TEST MODE	Internal Test Mode. Should always be set high.



Table 10. CLPOB Register Map

Address	Data Bit Content	Default Value (Hex)	Name	Description
20	[3:0]	F	CLPOBPOL	Start Polarities for CLPOB Sequences 0, 1, 2, and 3.
21	[23:0]	FFFFFF	CLPOBTOG_0	Sequence 0. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
22	[23:0]	FFFFFF	CLPOBTOG_1	Sequence 1. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
23	[23:0]	FFFFFF	CLPOBTOG_2	Sequence 2. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
24	[23:0]	FFFFFF	CLPOBTOG_3	Sequence 3. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
25	[7:0]	0	CLPOBSCP0	CLPOB Sequence-Change Position 0 (Hard-Coded to 0).
26	[11:0]	FFF	CLPOBSPTR	CLPOB Sequence Pointers for Region 0 [1:0], 1 [3:2], 2[5:4], 3[7:6].
27	[11:0]	FFF	CLPOBSCP1	CLPOB Sequence-Change Position 1.
28	[11:0]	FFF	CLPOBSCP2	CLPOB Sequence-Change Position 2.
28	[11:0]	FFF	CLPOBSCP3	CLPOB Sequence-Change Position 3.

Table 11. PBLK Register Map

Address	Data Bit Content	Default Value (Hex)	Name	Description
30	[3:0]	F	PBLKPOL	Start Polarities for PBLK Sequences 0, 1, 2, and 3.
31	[23:0]	FFFFFF	PBLKTOG_0	Sequence 0. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
32	[23:0]	FFFFFF	PBLKTOG_1	Sequence 1. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
33	[23:0]	FFFFFF	PBLKTOG_2	Sequence 2. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
34	[23:0]	FFFFFF	PBLKTOG_3	Sequence 3. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
35	[7:0]	0	PBLKSCP0	PBLK Sequence-Change Position 0 (Hard-Coded to 0).
36	[11:0]	FFF	PBLKSPTR	PBLK Sequence Pointers for Region 0 [1:0], 1 [3:2], 2 [5:4], 3 [7:6].
37	[11:0]	FFF	PBLKSCP1	PBLK Sequence-Change Position 1.
38	[11:0]	FFF	PBLKSCP2	PBLK Sequence-Change Position 2.
38	[11:0]	FFF	PBLKSCP3	PBLK Sequence-Change Position 3.

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**Table 12. HBLK Register Map**

Address	Data Bit Content	Default Value (Hex)	Name	Description
40	[0]	0	HBLKDIR	HBLK Internal/External. 0 = Internal. 1 = External.
41	[0]	0	HBLKPOL	HBLK External Active Polarity. 0 = Active Low. 1 = Active High.
42	[0]	1	HBLKEXTMASK	HBLK External Masking Polarity. 0 = Mask H1 Low. 1 = Mask H1 High.
43	[3:0]	F	HBLKMASK	HBLK Internal Masking Polarity for Each Sequence 0 to 3. 0 = Mask H1 Low. 1 = Mask H1 High.
44	[23:0]	FFFFFF	HBLKTOG12_0	Sequence 0. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
45	[23:0]	FFFFFF	HBLKTOG34_0	Sequence 0. Toggle Position 3 [11:0] and Toggle Position 4 [23:12].
46	[23:0]	FFFFFF	HBLKTOG56_0	Sequence 0. Toggle Position 5 [11:0] and Toggle Position 6 [23:12].
47	[23:0]	FFFFFF	HBLKTOG12_1	Sequence 1. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
48	[23:0]	FFFFFF	HBLKTOG34_1	Sequence 1. Toggle Position 3 [11:0] and Toggle Position 4 [23:12].
49	[23:0]	FFFFFF	HBLKTOG56_1	Sequence 1. Toggle Position 5 [11:0] and Toggle Position 6 [23:12].
4A	[23:0]	FFFFFF	HBLKTOG12_2	Sequence 2. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
4B	[23:0]	FFFFFF	HBLKTOG34_2	Sequence 2. Toggle Position 3 [11:0] and Toggle Position 4 [23:12].
4C	[23:0]	FFFFFF	HBLKTOG56_2	Sequence 2. Toggle Position 5 [11:0] and Toggle Position 6 [23:12].
4D	[23:0]	FFFFFF	HBLKTOG12_3	Sequence 3. Toggle Position 1 [11:0] and Toggle Position 2 [23:12].
4E	[23:0]	FFFFFF	HBLKTOG34_3	Sequence 3. Toggle Position 3 [11:0] and Toggle Position 4 [23:12].
4F	[23:0]	FFFFFF	HBLKTOG56_3	Sequence 3. Toggle Position 5 [11:0] and Toggle Position 6 [23:12].
50	[7:0]	0	HBLKSCP0	HBLK Sequence-Change Position 0 (Hard-coded to 0).
51	[11:0]	FFF	HBLKSPTR	HBLK Sequence Pointers for Region 0 [1:0], 1 [3:2], 2 [5:4], 3 [7:6].
52	[11:0]	FFF	HBLKSCP1	HBLK Sequence-Change Position 1.
53	[11:0]	FFF	HBLKSCP2	HBLK Sequence-Change Position 2.
53	[11:0]	FFF	HBLKSCP3	HBLK Sequence-Change Position 3.

**Table 13. H1 to H2, RG, SHP, SHD Register Map**

Address	Data Bit Content	Default Value	Name	Description
60	[12:0]	01001	H1CONTROL	H1 Signal Control. Polarity [0](0 = Inversion, 1 = No Inversion). H1 Positive Edge Location [6:1]. H1 Negative Edge Location [12:7].
61	[12:0]	00801	RGCONTROL	RG Signal Control. Polarity [0](0 = Inversion, 1 = No Inversion). RG Positive Edge Location [6:1]. RG Negative Edge Location [12:7].
62	[14:0]	0	DRVCONTROL	Drive Strength Control for H1 [2:0], H2 [5:3], H3 [8:6], H4 [11:9], and RG [14:12]. Drive Current Values: 0 = Off, 1 = 4.3 mA, 2 = 8.6 mA, 3 = 12.9 mA, 4 = 17.2 mA, 5 = 21.5 mA, 6 = 25.8 mA, 7 = 30.1 mA.
63	[11:0]	00024	SAMPCONTROL	SHP/SHD Sample Control. SHP Sampling Location [5:0]. SHD Sampling Location [11:6].
64	[5:0]	0	DOUTPHASE	DOUT Phase Control.

Table 14. AFE Operation Register Detail

Address	Data Bit Content	Default Value	Name	Description
00	[1:0]	0	PWRDOWN	0 = Normal Operation. 1 = Reference Standby. 2/3 = Total Power-Down
	[2]	1	CLPENABLE	0 = Disable OB Clamp. 1 = Enable OB Clamp.
	[3]	0	CLPSPEED	0 = Select Normal OB Clamp Settling. 1 = Select Fast OB Clamp Settling.
	[4]	0	FASTUPDATE	0 = Ignore VGA Update. 1 = Very Fast Clamping when VGA Is Updated.
	[5]	0	PBLK_LVL	DOUT Value during PBLK. 0 = Blank to Zero. 1 = Blank to Clamp Level.
	[7:6]	0	TEST MODE	Test Operation Only. Set to zero.
	[8]	0	DCBYP	0 = Enable DC restore circuit. 1 = Bypass DC Restore Circuit during PBLK.
	[9]	0	TESTMODE	Test Operation Only. Set to zero.
	[11:10]	0	CDSGAIN	Adjustment of CDS Gain. 0 = 0 dB. 01 = -2 dB. 10 = -4 dB. 11 = 0 dB.

Table 15. AFE Control Register Detail

Address	Data Bit Content	Default Value	Name	Description
03	[1:0]	0	COLORSTEER	0 = Off. 1 = Progressive. 2 = Interlaced. 3 = Three Field.
	[2]	1	PxGAENABLE	0 = Disable PxGA. 1 = Enable PxGA.
	[3]	0	DOUTDISABLE	0 = Data Outputs Are Driven. 1 = Data Outputs Are Three-States.
	[4]	0	DOUTLATCH	0 = Latch Data Outputs with DOUT Phase. 1 = Output Latch Transparent.
	[5]	0	GRAYENCODE	0 = Binary Encode Data Outputs. 1 = Gray Encode Data Outputs.

## PRECISION TIMING HIGH SPEED TIMING GENERATION

The AD9949 generates flexible high speed timing signals using the *Precision Timing* core. This core is the foundation for generating the timing used for both the CCD and the AFE: the reset gate (RG), horizontal drivers (H1 to H4), and the SHP/SHD sample clocks. A unique architecture makes it routine for the system designer to optimize image quality by providing precise control over the horizontal CCD readout and the AFE correlated double sampling.

### TIMING RESOLUTION

The *Precision Timing* core uses a  $1 \times$  master clock input (CLI) as a reference. This clock should be the same as the CCD pixel clock frequency. Figure 16 illustrates how the internal timing core divides the master clock period into 48 steps or edge positions. Therefore, the edge resolution of the *Precision Timing* core is  $(t_{CLI}/48)$ . For more information on using the CLI input, refer to the Applications Information section.

### HIGH SPEED CLOCK PROGRAMMABILITY

Figure 17 shows how the high speed clocks, RG, H1 to H4, SHP, and SHD, are generated. The RG pulse has programmable rising and falling edges and may be inverted using the polarity control. The horizontal clocks H1 and H3 have programmable rising and falling edges and polarity control. The H2 and H4 clocks are always inverses of H1 and H3, respectively. Table 16 summarizes the high speed timing registers and their parameters.

Each edge location setting is 6 bits wide, but only 48 valid edge locations are available. Therefore, the register values are mapped into four quadrants, with each quadrant containing 12 edge locations. Table 17 shows the correct register values for the corresponding edge locations.

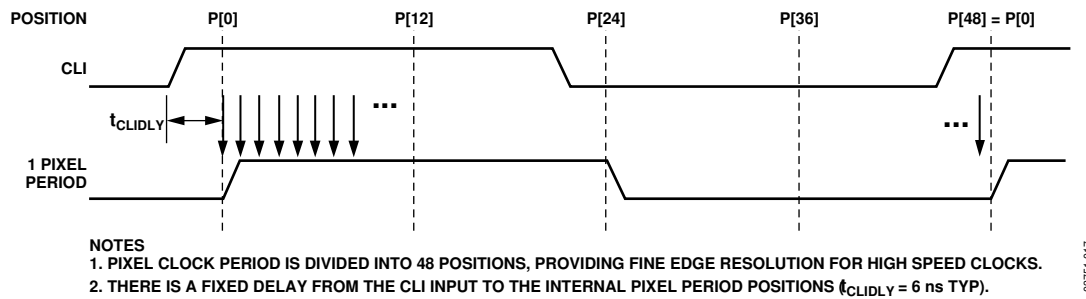


Figure 16. High Speed Clock Resolution from CLI Master Clock Input

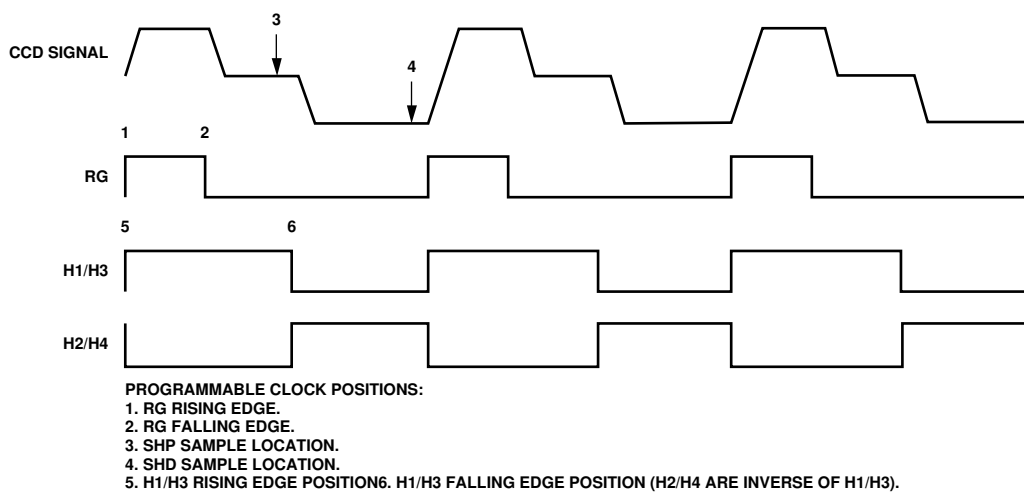


Figure 17. High Speed Clock Programmable Locations

Table 16. H1CONTROL, RGCONTROL, DRVCONTROL, and SAMPCONTROL Register Parameters

Parameter	Length	Range	Description
Polarity	1b	High/Low	Polarity Control for H1/H3 and RG (0 = No Inversion, 1 = Inversion).
Positive Edge	6b	0 to 47 Edge Location	Positive Edge Location for H1/H3 and RG.
Negative Edge	6b	0 to 47 Edge Location	Negative Edge Location for H1/H3 and RG.
Sample Location	6b	0 to 47 Sample Location	Sampling Location for SHP and SHD.
Drive Control	3b	0 to 7 Current Steps	Drive Current for H1 to H4 and RG Outputs, 0 to 7 Steps of 4.1 mA Each.
DOUT Phase	6b	0 to 47 Edge Location	Phase Location of Data Outputs with Respect to Pixel Period.

Table 17. Precision Timing Edge Locations

Quadrant	Edge Location (Decimal)	Register Value (Decimal)	Register Value (Binary)
I	0 to 11	0 to 11	000000 to 001011
II	12 to 23	16 to 27	010000 to 011011
III	24 to 35	32 to 43	100000 to 101011
IV	36 to 47	48 to 59	110000 to 111011

## H-DRIVER AND RG OUTPUTS

In addition to the programmable timing positions, the AD9949 features on-chip output drivers for the RG and H1 to H4 outputs. These drivers are powerful enough to directly drive the CCD inputs. The H-driver and RG driver current can be adjusted for optimum rise/fall time into a particular load by using the DRVCONTROL register (Address 0x62). The DRVCONTROL register is divided into five different 3-bit values, each one being adjustable in 4.1 mA increments. The minimum setting of 0 is equal to OFF or three-state, and the maximum setting of 7 is equal to 30.1 mA.

As shown in Figure 18, the H2/H4 outputs are inverses of H1/H3. The internal propagation delay resulting from the signal inversion is less than 1 ns, which is significantly less than the typical rise time driving the CCD load. This results in a H1/H2 crossover voltage at approximately 50% of the output swing. The crossover voltage is not programmable.

## DIGITAL DATA OUTPUTS

The AD9949 data output phase is programmable using the DOUTPHASE register (Address 0x64). Any edge from 0 to 47 may be programmed, as shown in Figure 19. The pipeline delay for the digital data output is shown in Figure 20.

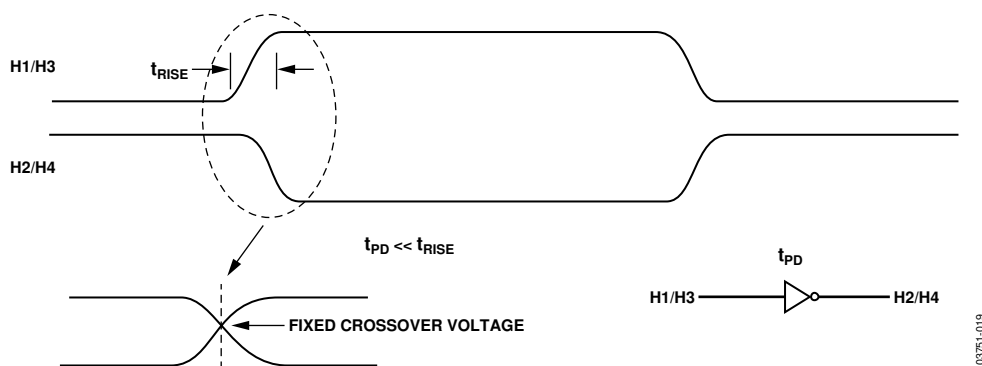
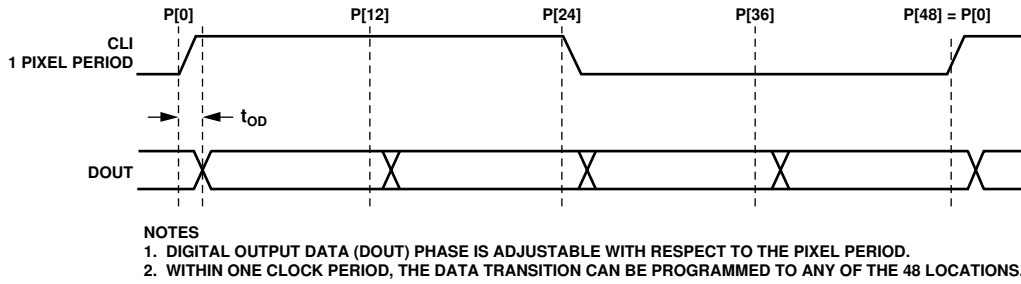
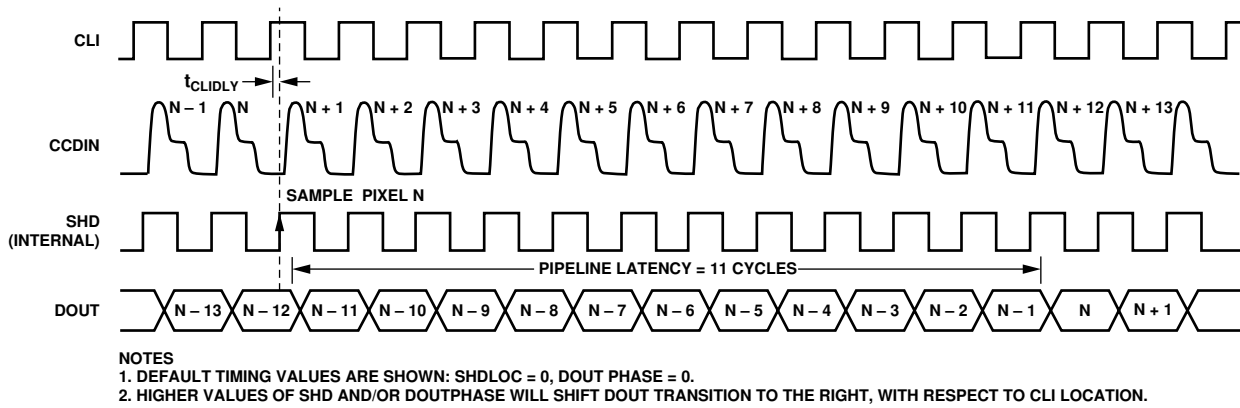


Figure 18. H-Clock Inverse Phase Relationship



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Figure 19. Digital Output Phase Adjustment



03751-021

Figure 20. Pipeline Delay for Digital Data Output

## HORIZONTAL CLAMPING AND BLANKING

The AD9949's horizontal clamping and blanking pulses are fully programmable to suit a variety of applications. Individual sequences are defined for each signal, which are then organized into multiple regions during image readout. This allows the dark pixel clamping and blanking patterns to be changed at each stage of the readout to accommodate different image transfer timing and high speed line shifts.

### INDIVIDUAL CLPOB AND PBLK SEQUENCES

The AFE horizontal timing consists of CLPOB and PBLK, as shown in Figure 21. These two signals are independently programmed using the parameters shown in Table 18. The start polarity, first toggle position, and second toggle position are fully programmable for each signal. The CLPOB and PBLK

signals are active low and should be programmed accordingly. Up to four individual sequences can be created for each signal.

### INDIVIDUAL HBLK SEQUENCES

The HBLK programmable timing shown in Figure 22 is similar to CLPOB and PBLK. However, there is no start polarity control. Only the toggle positions are used to designate the start and the stop positions of the blanking period. Additionally, there is a polarity control, HBLKMASK, which designates the polarity of the horizontal clock signals H1 to H4 during the blanking period. Setting HBLKMASK high sets H1 = H3 = low and H2 = H4 = high during the blanking, as shown in Figure 23. Up to four individual sequences are available for HBLK.

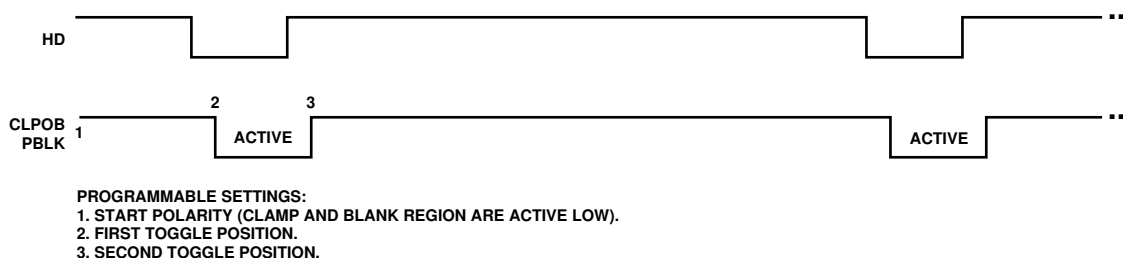


Figure 21. Clamp and Preblank Pulse Placement

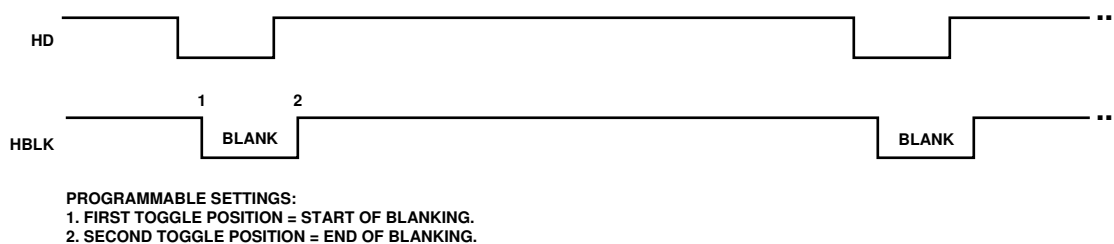


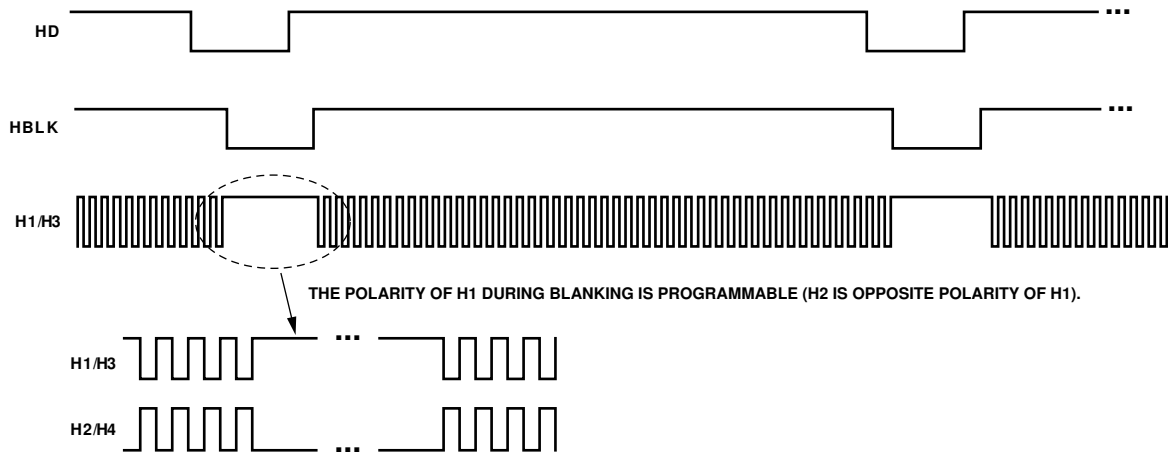
Figure 22. Horizontal Blanking (HBLK) Pulse Placement

Table 18. CLPOB and PBLK Individual Sequence Parameters

Parameter	Length	Range	Description
Polarity	1b	High/Low	Starting Polarity of Clamp and PBLK Pulses for Sequences 0 to 3.
Toggle Position 1	12b	0 to 4095 Pixel Location	First Toggle Position within the Line for Sequences 0 to 3.
Toggle Position 2	12b	0 to 4095 Pixel Location	Second Toggle Position within the Line for Sequences 0 to 3.

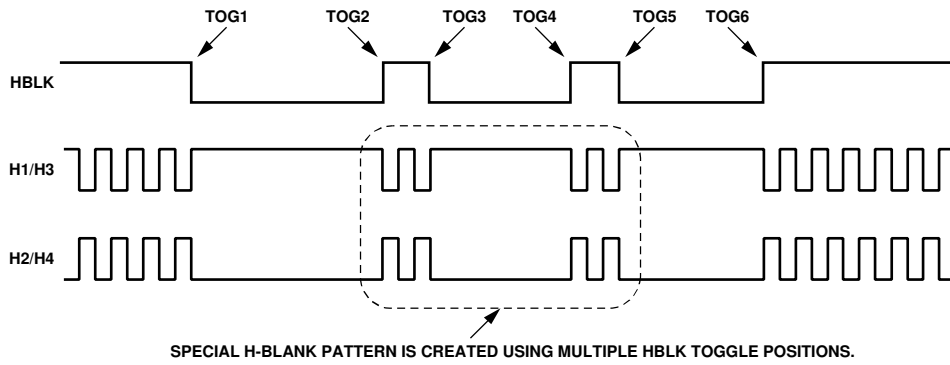
Table 19. HBLK Individual Sequence Parameters

Parameter	Length	Range	Description
HBLKMASK	1b	High/Low	Masking Polarity for H1 for Sequences 0 to 3 (0 = H1 Low, 1 = H1 High).
Toggle Position 1	12b	0 to 4095 Pixel Location	First Toggle Position within the Line for Sequences 0 to 3.
Toggle Position 2	12b	0 to 4095 Pixel Location	Second Toggle Position within the Line for Sequences 0 to 3.
Toggle Position 3	12b	0 to 4095 Pixel Location	Third Toggle Position within the Line for Sequences 0 to 3.
Toggle Position 4	12b	0 to 4095 Pixel Location	Fourth Toggle Position within the Line for Sequences 0 to 3.
Toggle Position 5	12b	0 to 4095 Pixel Location	Fifth Toggle Position within the Line for Sequences 0 to 3.
Toggle Position 6	12b	0 to 4095 Pixel Location	Sixth Toggle Position within the Line for Sequences 0 to 3.



03751-024

Figure 23. HBLK Masking Control



03751-025

Figure 24. Generating Special HBLK Patterns

**Table 20. Horizontal Sequence Control Parameters for CLPOB, PBLK, and HBLK**

Register	Length	Range	Description
SCP	12b	0 to 4095 Line Number	CLOB/PBLK/HBLK SCP to Define Horizontal Regions 0 to 3.
SPTR	2b	0 to 3 Sequence Number	Sequence Pointer for Horizontal Regions 0 to 3.



## GENERATING SPECIAL HBLK PATTERNS

Six toggle positions are available for HBLK. Normally, only two of the toggle positions are used to generate the standard HBLK interval. However, the additional toggle positions may be used to generate special HBLK patterns, as shown in Figure 24. The pattern in this example uses all six toggle positions to generate two extra groups of pulses during the HBLK interval. By changing the toggle positions, different patterns can be created.

## HORIZONTAL SEQUENCE CONTROL

The AD9949 uses sequence change positions (SCP) and sequence pointers (SPTR) to organize the individual horizontal sequences. Up to four SCPs are available to divide the readout into four separate regions, as shown in Figure 25. The SCP0 is always hard-coded to Line 0, and SCP1 to SCP3 are register programmable. During each region bounded by the SCP, the SPTR registers designate which sequence is used by each signal.

CLPOB, PBLK, and HBLK each have a separate set of SCPs. For example, CLPOBSCP1 defines Region 0 for CLPOB, and in that region any of the four individual CLPOB sequences may be selected with the CLPOBSPTR register. The next SCP defines a new region and in that region, each signal can be assigned to a different individual sequence. The sequence control registers are summarized in Table 20.

## EXTERNAL HBLK SIGNAL

The AD9949 can also be used with an external HBLK signal. Setting the HBLKDIR register (Address 0x40) to high disables the internal HBLK signal generation. The polarity of the external signal is specified using the HBLKPOL register, and the masking polarity of H1 is specified using the HBLKMASK register. Table 21 summarizes the register values when using an external HBLK signal.

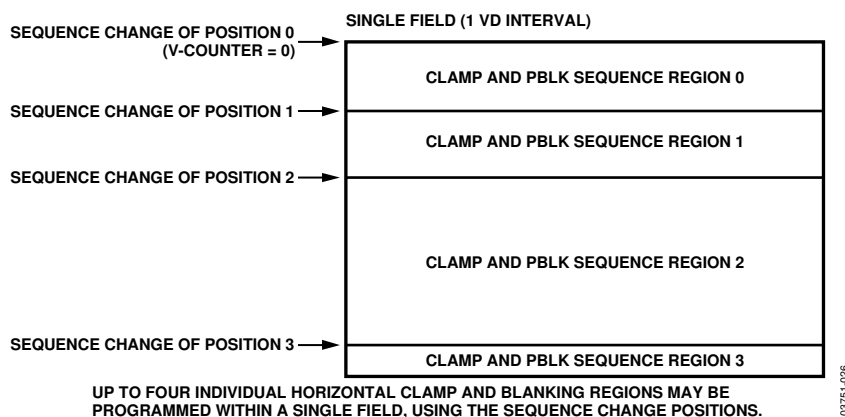


Figure 25. Clamp and Blanking Sequence Flexibility

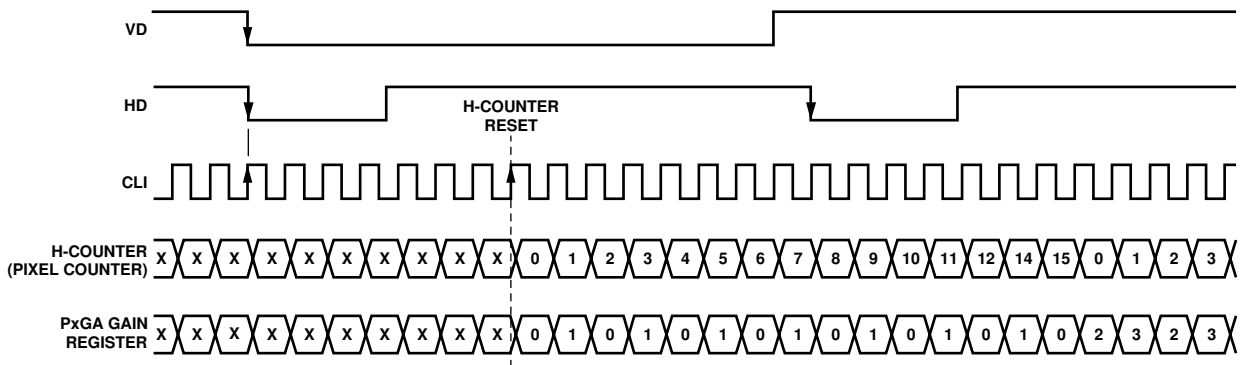
Table 21. External HBLK Register Parameters

Register	Length	Range	Description
HBLKDIR	1b	High/Low	Specifies HBLK Internally Generated or Externally Supplied. 1 = External.
HBLKPOL	1b	High/Low	External HBLK Active Polarity. 0 = Active Low. 1 = Active High.
HBLKEXTMASK	1b	High/Low	External HBLK Masking Polarity. 0 = Mask H1 Low. 1 = Mask H1 High.

## H-COUNTER SYNCHRONIZATION

The H-Counter reset occurs seven CLI cycles following the HD falling edge. The PxGA steering is synchronized with the reset of the internal H-Counter (see Figure 26).

As mentioned in the H-Counter Behavior section, the AD9949 H-counter rolls over to zero and continues counting when the maximum counter length is exceeded. The newer AD9949A product does not roll over but holds at its maximum value until the next HD rising edge occurs.



**NOTES**

1. INTERNAL H-COUNTER IS RESET 7 CLI CYCLES AFTER THE HD FALLING EDGE (WHEN USING VDHDEDGE = 0).
2. TYPICAL TIMING RELATIONSHIP: CLI RISING EDGE IS COINCIDENT WITH HD FALLING EDGE.
3. PxGA STEERING IS SYNCHRONIZED WITH THE RESET OF THE INTERNAL H-COUNTER (MOSAIC SEPARATE MODE IS SHOWN).

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Figure 26. H-Counter Synchronization