



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



## FEATURES

- 400 MSPS internal clock speed**
- Integrated 14-bit DAC**
- Programmable phase/amplitude dithering**
- 32-bit frequency tuning accuracy**
- 14-bit phase tuning accuracy**
- Phase noise better than  $-120$  dBc/Hz**
- Excellent dynamic performance**
  - >80 dB narrowband SFDR**
- Serial input/output (I/O) control**
- Ultrahigh speed analog comparator**
- Automatic linear and nonlinear frequency sweeping**
- 4 frequency/phase offset profiles**
- 1.8 V power supply**
- Software and hardware controlled power-down**
- 48-lead TQFP**
- Integrated 1024 word  $\times$  32-bit RAM**
- PLL-based REFCLK multiplier**
- Internal oscillator, can be driven by a single crystal**
- Phase modulation capability**
- Multichip synchronization**

## APPLICATIONS

- Agile LO frequency synthesis**
- Programmable clock generators**
- FM chirp source for radar and scanning systems**
- Automotive radars**
- Test and measurement equipment**
- Acousto-optic device drivers**

## GENERAL DESCRIPTION

The AD9954 is a direct digital synthesizer (DDS) that uses advanced technology, coupled with an internal high speed, high performance DAC to form a complete, digitally programmable, high frequency synthesizer capable of generating a frequency-agile analog output sinusoidal waveform at up to 160 MHz. The AD9954 enables fast frequency hopping coupled with fine tuning of both frequency (0.01 Hz or better) and phase (0.022° granularity).

The AD9954 is programmed via a high speed serial I/O port. The device includes static RAM to support flexible frequency sweep capability in several modes, plus a user-defined linear sweep mode of operation. Also included is an on-chip high speed comparator for applications requiring a square wave output. An on-chip oscillator and PLL circuitry provide users with multiple approaches to generate the device's system clock.

The AD9954 is specified to operate over the extended industrial temperature range (see Table 2).

## BASIC BLOCK DIAGRAM

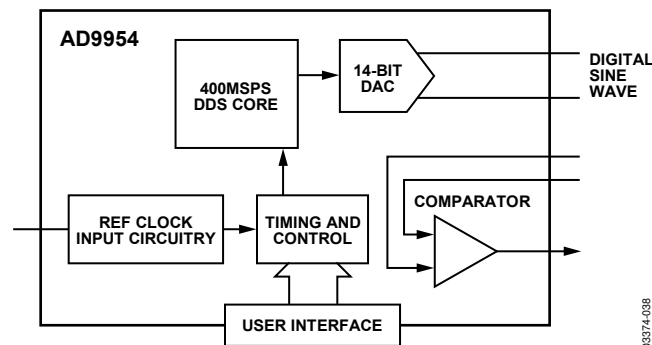


Figure 1.

# AD9954\* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

---

## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- AD9954 Evaluation Board

## DOCUMENTATION

### Application Notes

- AN-237: Choosing DACs for Direct Digital Synthesis
- AN-280: Mixed Signal Circuit Technologies
- AN-342: Analog Signal-Handling for High Speed and Accuracy
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-419: A Discrete, Low Phase Noise, 125 MHz Crystal Oscillator for the AD9850
- AN-423: Amplitude Modulation of the AD9850 Direct Digital Synthesizer
- AN-543: High Quality, All-Digital RF Frequency Modulation Generation with the ADSP-2181 and the AD9850 DDS
- AN-557: An Experimenter's Project:
- AN-587: Synchronizing Multiple AD9850/AD9851 DDS-Based Synthesizers
- AN-605: Synchronizing Multiple AD9852 DDS-Based Synthesizers
- AN-621: Programming the AD9832/AD9835
- AN-632: Provisionary Data Rates Using the AD9951 DDS as an Agile Reference Clock for the ADN2812 Continuous-Rate CDR
- AN-769: Generating Multiple Clock Outputs from the AD9540
- AN-823: Direct Digital Synthesizers in Clocking Applications Time
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-843: Measuring a Loudspeaker Impedance Profile Using the AD5933
- AN-847: Measuring a Grounded Impedance Profile Using the AD5933
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design
- AN-927: Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)
- AN-939: Super-Nyquist Operation of the AD9912 Yields a High RF Output Signal
- AN-953: Direct Digital Synthesis (DDS) with a Programmable Modulus

### Data Sheet

---

- 
- AD9954: 400 MSPS, 14-Bit, 1.8 V CMOS, Direct Digital Synthesizer Data Sheet

### Product Highlight

- Introducing Digital Up/Down Converters: VersaCOMM™ Reconfigurable Digital Converters

### Technical Books

- A Technical Tutorial on Digital Signal Synthesis, 1999

## TOOLS AND SIMULATIONS

- ADIsimDDS (Direct Digital Synthesis)
- AD9954 IBIS Models

## REFERENCE DESIGNS

- CN0109

## REFERENCE MATERIALS

### Product Selection Guide

- RF Source Booklet

### Technical Articles

- 400-MSample DDSs Run On Only +1.8 VDC
- ADI Buys Korean Mobile TV Chip Maker
- Basics of Designing a Digital Radio Receiver (Radio 101)
- DDS Applications
- DDS Circuit Generates Precise PWM Waveforms
- DDS Design
- DDS Device Produces Sawtooth Waveform
- DDS Device Provides Amplitude Modulation
- DDS IC Initiates Synchronized Signals
- DDS IC Plus Frequency-To-Voltage Converter Make Low-Cost DAC
- DDS Simplifies Polar Modulation
- Digital Potentiometers Vary Amplitude In DDS Devices
- Digital Up/Down Converters: VersaCOMM™ White Paper
- Digital Waveform Generator Provides Flexible Frequency Tuning for Sensor Measurement
- Improved DDS Devices Enable Advanced Comm Systems
- Integrated DDS Chip Takes Steps To 2.7 GHz
- Simple Circuit Controls Stepper Motors
- Speedy A/Ds Demand Stable Clocks
- Synchronized Synthesizers Aid Multichannel Systems
- The Year of the Waveform Generator
- Two DDS ICs Implement Amplitude-shift Keying
- Video Portables and Cameras Get HDMI Outputs

## DESIGN RESOURCES

- AD9954 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all AD9954 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

Submit feedback for this data sheet.

## TABLE OF CONTENTS

Features .....	1	Serial Interface Port Pin Descriptions .....	24
Applications .....	1	MSB/LSB Transfers .....	24
General Description .....	1	RAM I/O via Serial Port .....	24
Basic Block Diagram .....	1	Instruction Byte .....	25
Revision History .....	2	Register Maps and Descriptions .....	25
Functional Block Diagram .....	3	Control Register Bit Descriptions .....	29
Electrical Specifications .....	4	Other Register Descriptions .....	31
Absolute Maximum Ratings .....	7	Layout Considerations .....	32
Explanation of Test Levels .....	7	Detailed Programming Examples .....	33
ESD Caution .....	7	Single-Tone Mode .....	33
Pin Configuration and Function Descriptions .....	8	Linear Sweep Mode .....	33
Typical Performance Characteristics .....	10	RAM Mode .....	33
Theory of Operation .....	13	Suggested Application Circuits .....	35
Component Blocks .....	13	Evaluation Board Schematics .....	36
Modes of Operation .....	16	Outline Dimensions .....	39
Synchronization—Register Updates (I/O UPDATE) .....	21	Ordering Guide .....	39
Serial Port Operation .....	23		

## REVISION HISTORY

### 2/2017—Rev. B to Rev. C

Changes to Features Section .....	1
-----------------------------------	---

### 5/2009—Rev. A to Rev. B

Changes to Figure 29 and Figure 30 .....	24
Changes to Table 12 .....	26
Changes to Figure 34 .....	35
Updated Outline Dimensions .....	39
Changes to Ordering Guide .....	39

### 1/2007—Rev. 0 to Rev. A

Changes to Layout .....	Universal
Changes to Features, General Description, and Figure 1 .....	1
Changes to Figure 2 .....	3
Changes to Table 1 .....	4
Changes to Table 4 .....	8
Changes to Figure 5 to Figure 10 .....	10
Changes to Figure 12 .....	11
Changes to Figure 17 to Figure 18 Captions .....	12
Deleted Figure 19; Renumbered Sequentially .....	12
Added Table 5; Renumbered Sequentially .....	13
Changes to Component Block Section and Table 6 .....	13
Changes to Figure 20 .....	15

Changes to Modes of Operation Section and Table 8 .....	16
Changes to Table 9 .....	17
Changes to Synchronization; Register Updates (I/O UPDATE) Section and Figure 24 .....	21
Changes to Serial Port Operation Section .....	23
Changes to Serial Interface Port Pin Description Section, MSB/LSB Transfers Section, and RAM I/O Via Serial Port Section .....	24
Inserted Figure 29 and Figure 30; Renumbered Sequentially ..	24
Changes to Instruction Byte Section, Register Maps and Descriptions Section, and Table 12 .....	25
Changes to Table 13 .....	26
Changes to Table 14 .....	28
Added Single-Tone Mode Section, Linear Sweep Mode Section, Table 15, and RAM Mode Section .....	33
Added, and Table 16 .....	34
Inserted Figure 35 .....	36
Inserted Figure 36 .....	37
Inserted Figure 37 .....	38
Updated Outline Dimensions .....	39
Changes to Ordering Guide .....	39

### 10/2003—Revision 0: Initial Version

# FUNCTIONAL BLOCK DIAGRAM

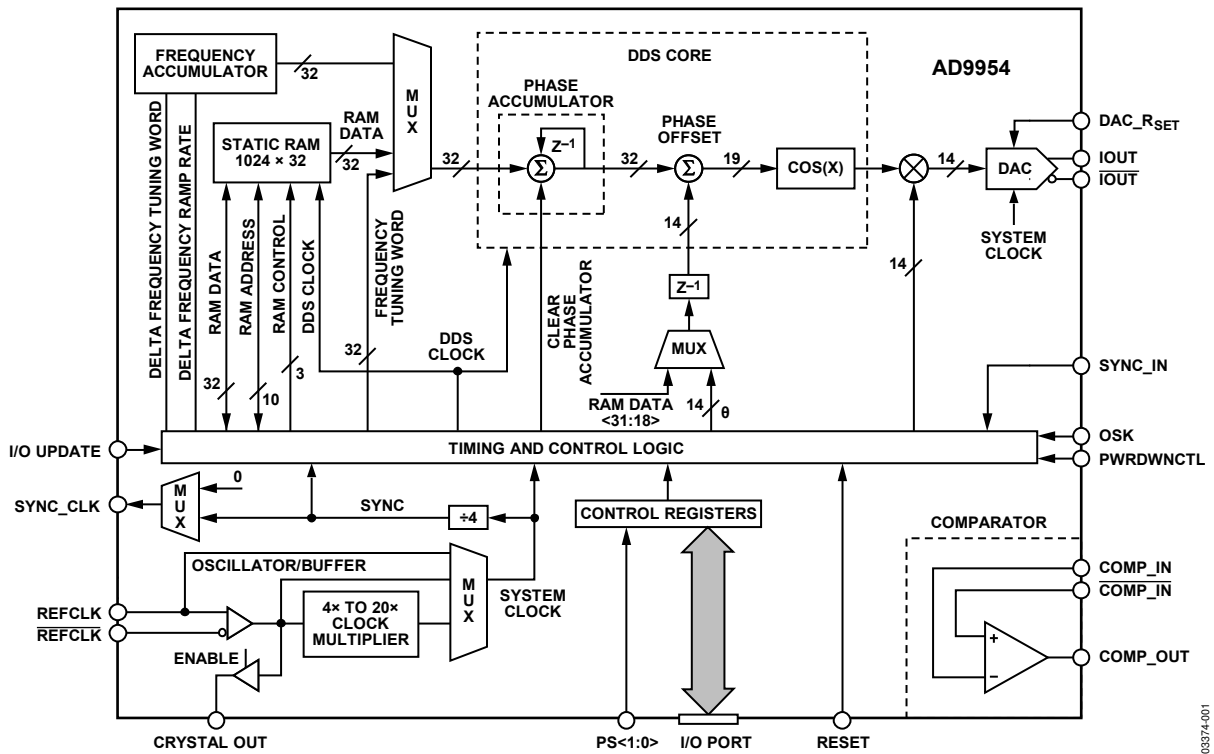


Figure 2.

033774-001

## ELECTRICAL SPECIFICATIONS

Unless otherwise noted, AVDD, DVDD = 1.8 V ± 5%, DVDD\_I/O = 3.3 V ± 5%, R<sub>SET</sub> = 3.92 kΩ, external reference clock frequency = 400 MHz. DAC output must be referenced to AVDD, not AGND.

Table 1.

Parameter	Temp	Test Level	Min	Typ	Max	Unit
<b>REF CLOCK INPUT CHARACTERISTICS</b>						
Frequency Range						
REFCLK Multiplier Disabled	Full	VI	1		400	MHz
REFCLK Multiplier Enabled at 4x	Full	VI	20		100	MHz
REFCLK Multiplier Enabled at 20x	Full	VI	4		20	MHz
Crystal Oscillator Operating Frequency	Full	IV	20		30	MHz
Input Capacitance	25°C	V		3		pF
Input Impedance	25°C	V		1.5		kΩ
Duty Cycle	25°C	V		50		%
Duty Cycle with REFCLK Multiplier Enabled	25°C	V	35		65	%
REFCLK Input Voltage Swing	Full	IV	100		1000	mV p-p
<b>DAC OUTPUT CHARACTERISTICS</b>						
Full-Scale Output Current	25°C		5	10	15	mA
Gain Error	25°C	I	-10		+10	%FS
Output Offset	25°C	I			0.6	μA
Differential Nonlinearity	25°C	V		1		LSB
Integral Nonlinearity	25°C	V		2		LSB
Output Capacitance	25°C	V		5		pF
Residual Phase Noise @ 1 kHz Offset, 40 MHz A <sub>OUT</sub>						
REFCLK Multiplier Enabled @ 20x	25°C	V		-105		dBc/Hz
REFCLK Multiplier Enabled @ 4x	25°C	V		-115		dBc/Hz
REFCLK Multiplier Disabled	25°C	V		-132		dBc/Hz
Voltage Compliance Range	25°C	I	AVDD - 0.5		AVDD + 0.5	V
<b>Wideband SFDR</b>						
1 MHz to 10 MHz Analog Out	25°C	V		73		dBc
10 MHz to 40 MHz Analog Out	25°C	V		67		dBc
40 MHz to 80 MHz Analog Out	25°C	V		62		dBc
80 MHz to 120 MHz Analog Out	25°C	V		58		dBc
120 MHz to 160 MHz Analog Out	25°C	V		52		dBc
<b>Narrow-Band SFDR</b>						
40 MHz Analog Out (±1 MHz)	25°C	V		87		dBc
40 MHz Analog Out (±250 kHz)	25°C	V		89		dBc
40 MHz Analog Out (±50 kHz)	25°C	V		91		dBc
40 MHz Analog Out (±10 kHz)	25°C	V		93		dBc
80 MHz Analog Out (±1 MHz)	25°C	V		85		dBc
80 MHz Analog Out (±250 kHz)	25°C	V		87		dBc
80 MHz Analog Out (±50 kHz)	25°C	V		89		dBc
80 MHz Analog Out (±10 kHz)	25°C	V		91		dBc
120 MHz Analog Out (±1 MHz)	25°C	V		83		dBc
120 MHz Analog Out (±250 kHz)	25°C	V		85		dBc
120 MHz Analog Out (±50 kHz)	25°C	V		87		dBc
120 MHz Analog Out (±10 kHz)	25°C	V		89		dBc
160 MHz Analog Out (±1 MHz)	25°C	V		81		dBc
160 MHz Analog Out (±250 kHz)	25°C	V		83		dBc
160 MHz Analog Out (±50 kHz)	25°C	V		85		dBc
160 MHz Analog Out (±10 kHz)	25°C	V		87		dBc

Parameter	Temp	Test Level	Min	Typ	Max	Unit
<b>COMPARATOR INPUT CHARACTERISTICS</b>						
Input Capacitance	25°C	V		3		pF
Input Resistance	25°C	IV		500		kΩ
Input Current	25°C	I		±12		μA
Hysteresis	25°C	IV	30		45	mV
<b>COMPARATOR OUTPUT CHARACTERISTICS</b>						
Logic 1 Voltage, High-Z Load	Full	VI	1.6			V
Logic 0 Voltage, High-Z Load	Full	VI			0.4	V
Propagation Delay	25°C	IV		3		ns
Output Duty-Cycle Error	25°C	IV		±5		%
Rise/Fall Time, 5 pF Load	25°C	IV			1	ns
Toggle Rate, High-Z Load	25°C	IV	200			MHz
Output Jitter <sup>1</sup>	25°C	IV			1	ps rms
<b>COMPARATOR NARROW-BAND SFDR</b>						
10 MHz to 160 MHz F <sub>OUT</sub>						
Measured over a 1 MHz BW	25°C	V		80		dBc
Measured over a 250 kHz BW	25°C	V		85		dBc
Measured over a 50 kHz BW	25°C	V		90		dBc
Measured over a 10 Hz BW	25°C	V		95		dBc
<b>TIMING CHARACTERISTICS</b>						
<b>Serial Control Bus</b>						
Maximum Frequency	Full	IV		25		Mbps
Minimum Clock Pulse Width Low	Full	IV	7			ns
Minimum Clock Pulse Width High	Full	IV	7			ns
Maximum Clock Rise/Fall Time	Full	IV		2		ns
Minimum Data Setup Time DVDD_I/O = 3.3 V	Full	IV	3			ns
Minimum Data Setup Time DVDD_I/O = 1.8 V	Full	IV	5			ns
Minimum Data Hold Time	Full	IV	0			ns
Maximum Data Valid Time	Full	IV		25		ns
Wake-Up Time <sup>2</sup>	Full	IV		1		ms
Minimum Reset Pulse Width High	Full	IV	5			SYSCLK cycles <sup>3</sup>
I/O UPDATE, PS0, PS1 to SYNC_CLK Setup Time, DVDD_I/O = 3.3 V	Full	I	4			ns
I/O UPDATE, PS0, PS1 to SYNC_CLK Setup Time, DVDD_I/O = 1.8 V	Full	I	6			ns
I/O UPDATE, PS0, PS1 to SYNC_CLK Hold Time	Full	I	0			ns
<b>Latency</b>						
I/O UPDATE to Frequency Change Prop Delay	25°C	IV	24			SYSCLK cycles
I/O UPDATE to Phase Offset Change Prop Delay	25°C	IV	24			SYSCLK cycles
I/O UPDATE to Amplitude Change Prop Delay	25°C	IV	16			SYSCLK cycles
PS0, PS1 to RAM Driven Frequency Change Prop Delay	25°C	IV	28			SYSCLK cycles
PS0, PS1 to RAM Driven Phase Change Prop Delay	25°C	IV	28			SYSCLK cycles
PS0 to Linear Frequency Sweep Prop Delay	25°C	IV	28			SYSCLK cycles



Parameter	Temp	Test Level	Min	Typ	Max	Unit
<b>CMOS LOGIC INPUTS</b>						
Logic 1 Voltage @ DVDD_I/O (Pin 43) = 1.8 V	25°C	I	1.25			V
Logic 0 Voltage @ DVDD_I/O (Pin 43) = 1.8 V	25°C	I			0.6	V
Logic 1 Voltage @ DVDD_I/O (Pin 43) = 3.3 V	25°C	I	2.2			V
Logic 0 Voltage @ DVDD_I/O (Pin 43) = 3.3 V	25°C	I			0.8	V
Logic 1 Current	25°C	V		3	12	μA
Logic 0 Current	25°C	V			12	μA
Input Capacitance	25°C	V		2		pF
<b>CMOS LOGIC OUTPUTS (1 mA Load) DVDD_I/O = 1.8 V</b>						
Logic 1 Voltage	25°C	I	1.35			V
Logic 0 Voltage	25°C	I			0.4	V
<b>CMOS LOGIC OUTPUTS (1 mA Load) DVDD_I/O = 3.3 V</b>						
Logic 1 Voltage	25°C	I	2.8			V
Logic 0 Voltage	25°C	I			0.4	V
<b>POWER CONSUMPTION (AVDD = DVDD = 1.8 V)</b>						
Single-Tone Mode (Comparator Off)	25°C	I		162	171	mW
With RAM or Linear Sweep Enabled	25°C	I		175	190	mW
With Comparator Enabled	25°C	I		180	190	mW
With RAM and Comparator Enabled	25°C	I		198	220	mW
Rapid Power-Down Mode	25°C	I		150	160	mW
Full-Sleep Mode	25°C	I		20	27	mW
<b>SYNCHRONIZATION FUNCTION<sup>4</sup></b>						
Maximum Sync Clock Rate (DVDD_I/O = 1.8 V)	25°C	VI	62.5			MHz
Maximum Sync Clock Rate (DVDD_I/O = 3.3 V)	25°C	VI	100			MHz
SYNC_CLK Alignment Resolution <sup>5</sup>	25°C	V		±1		SYSCLK cycles

<sup>1</sup> Represents the cycle-to-cycle residual jitter from the comparator alone.

<sup>2</sup> Wake-up time refers to the recovery from analog power-down modes (see section on Power-Down Modes of Operation). The primary limiting factor is the settling time of the PLL multiplier in the reference circuitry. The wake-up time assumes there is no capacitor on DAC BP and that the recommended PLL loop filter values are used.

<sup>3</sup> SYSCLK cycle refers to the clock frequency used on-chip to drive the DDS core. This is equal to the frequency of the reference source times the value of the PLL-based reference clock multiplier.

<sup>4</sup> SYNC\_CLK = ¼ SYSCLK rate. Be sure the high speed sync enable bit, CFR2<11>, is programmed appropriately.

<sup>5</sup> This parameter indicates that the digital synchronization feature cannot compensate for phase delays (timing skew) between system clock rising edges. If the system clock edges are aligned, the synchronization function should not increase the skew between the two edges.

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Maximum Junction Temperature	150°C
DVDD_I/O (Pin 43)	4 V
AVDD, DVDD	2 V
Digital Input Voltage (DVDD_I/O = 3.3 V)	-0.7 V to +5.25 V
Digital Input Voltage (DVDD_I/O = 1.8 V)	-0.7 V to +2.2 V
Digital Output Current	5 mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +105°C
Lead Temperature (10 sec Soldering)	300°C
$\theta_{JA}$	38°C/W
$\theta_{JC}$	15°C/W

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### EXPLANATION OF TEST LEVELS

- I 100% production tested.
- II 100% production tested at 25°C and sample tested at specified temperatures.
- III Sample tested only.
- IV Parameter is guaranteed by design and characterization testing.
- V Parameter is a typical value only.
- VI Devices are 100% production tested at 25°C and guaranteed by design and characterization testing for industrial operating temperature range.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

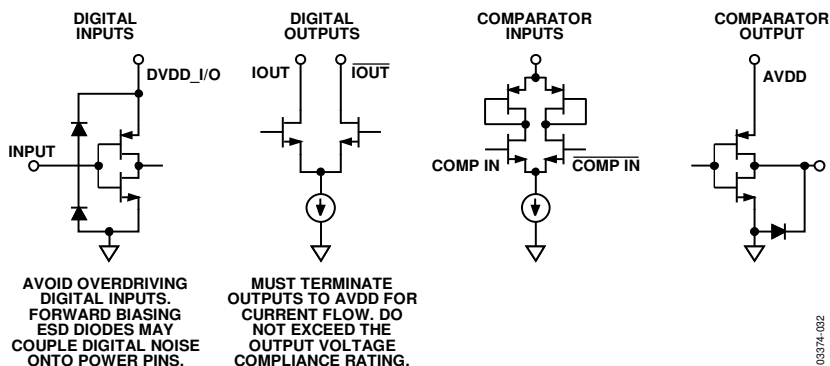


Figure 3. Equivalent Input and Output Circuits

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

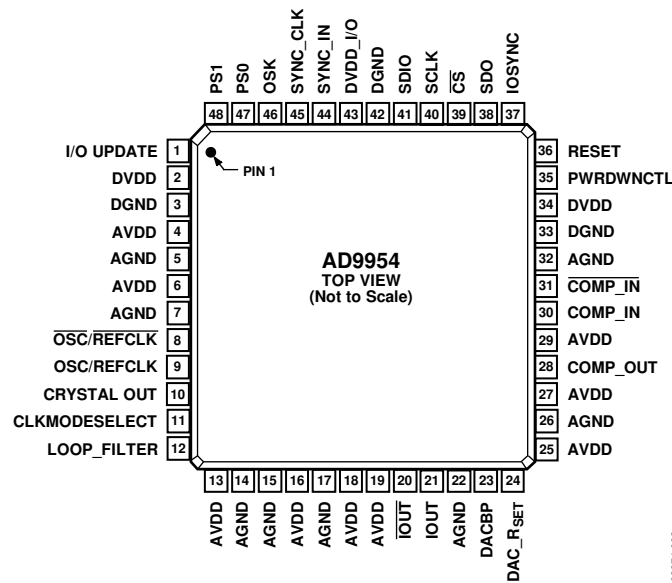


Figure 4. Pin Configuration

Note that the exposed paddle on the bottom of the package forms an electrical connection for the DAC and must be attached to analog ground. Note that Pin 43, DVDD\_I/O, can be powered to 1.8 V or 3.3 V. The DVDD pins (Pin 2 and Pin 34) must be powered to 1.8 V.

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	I/O	Description
1	I/O UPDATE	I	The rising edge transfers the contents of the internal buffer memory to the I/O registers. See Synchronization—Register Updates (I/O UPDATE) section for details.
2, 34	DVDD	I	Digital Power Supply Pins (1.8 V).
3, 33, 42	DGND	I	Digital Power Ground Pins.
4, 6, 13, 16, 18, 19, 25, 27, 29	AVDD	I	Analog Power Supply Pins (1.8 V).
5, 7, 14, 15, 17, 22, 26, 32	AGND	I	Analog Power Ground Pins.
8	OSC/REFCLK	I	Oscillator Input/Complementary Reference Clock. When the REFCLK port is operated in single-ended mode, REFCLK should be decoupled to AVDD with a 0.1 $\mu$ F capacitor.
9	OSC/REFCLK	I	Oscillator Input/Reference Clock. See Table 5 for details on the OSC/REFCLK operation.
10	CRYSTAL OUT	O	Output of the Oscillator Section.
11	CLKMODESELECT	I	Control Pin for the Oscillator Section (1.8 V logic only). See REFCLK Input section for detailed instructions.
12	LOOP_FILTER	I	This pin provides the connection for the external zero compensation network of the REFCLK multiplier's PLL loop filter. The network varies based on the multiplication value in the PLL loop. See Table 4 for details.
20	IOUT	O	Complementary DAC Output. Should be biased through a resistor to AVDD, not AGND.
21	IOUT	O	DAC Output. Should be biased through a resistor to AVDD, not AGND.
23	DACBP	I	DAC Band Gap Decoupling Pin. A 0.1 $\mu$ F capacitor to AGND is recommended.
24	DAC_RSET	I	A resistor (3.92 k $\Omega$ nominal) connected from AGND to DAC_RSET establishes the reference current for the DAC. See equation in DAC Output section.
28	COMP_OUT	O	Comparator Output.
30	COMP_IN	I	Comparator Input.

Pin No.	Mnemonic	I/O	Description
31	COMP_IN	I	Comparator Complementary Input.
35	PWRDWNCTL	I	Input Pin Used as an External Power-Down Control (see Table 9 for details).
36	RESET	I	Active High Hardware Reset Pin. Assertion of the RESET pin forces the AD9954 to the default state, as described in the right-hand column of Table 12, which is the I/O port register map.
37	IOSYNC	I	Asynchronous Active High Reset of the Serial Port Controller. When high, the current I/O operation is immediately terminated, enabling a new I/O operation to commence once IOSYNC is returned low. If unused, ground this pin; do not allow this pin to float.
38	SDO	O	See Serial Interface Port Pin Description section for details.
39	$\overline{CS}$	I	See Serial Interface Port Pin Description section for details.
40	SCLK	I	See Serial Interface Port Pin Description section for details.
41	SDIO	I/O	See Serial Interface Port Pin Description section for details.
43	DVDD_I/O	I	Digital Power Supply. This pin is for I/O cells only, 3.3 V.
44	SYNC_IN	I	Input Signal Used to Synchronize Multiple AD9954s. This input is connected to the SYNC_CLK output of a master AD9954.
45	SYNC_CLK	O	Clock Output Pin that Serves as a Synchronizer for External Hardware.
46	OSK	I	Input Pin Used to Control the Direction of the Shaped On-Off Keying Function When Programmed for Operation. OSK is synchronous to the SYNC_CLK pin. When OSK is disabled, this pin should be tied to DGND.
47, 48	PS0, PS1	I	Input Pins Used to Select One of the Internal Phase/Frequency Profiles. PS1 and PS0 are synchronous to the SYNC_CLK pin. Change on these pins triggers a transfer of the contents of the chosen internal buffer memory to the I/O registers (sends an internal I/O UPDATE).
<49>	AGND	I	The Exposed Paddle on the Bottom of the Package. It is a ground connection for the DAC and must be attached to AGND in any board layout.

TYPICAL PERFORMANCE CHARACTERISTICS

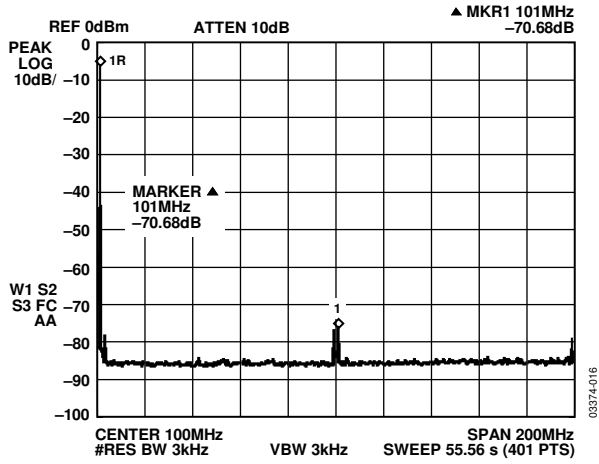


Figure 5.  $f_{OUT} = 1\text{ MHz}$ ,  $f_{CLK} = 400\text{ MSPS}$ , WBSFDR

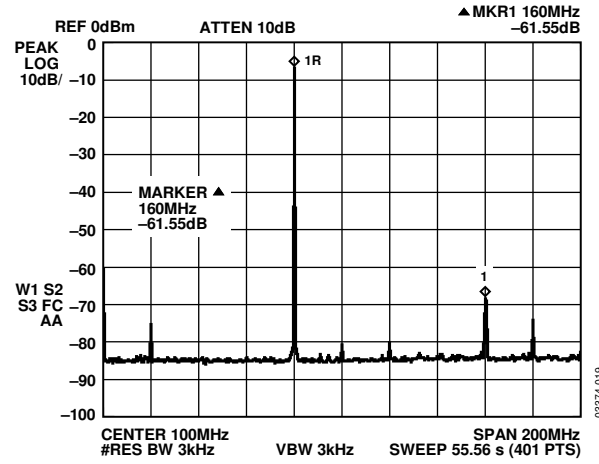


Figure 8.  $f_{OUT} = 80\text{ MHz}$ ,  $f_{CLK} = 400\text{ MSPS}$ , WBSFDR

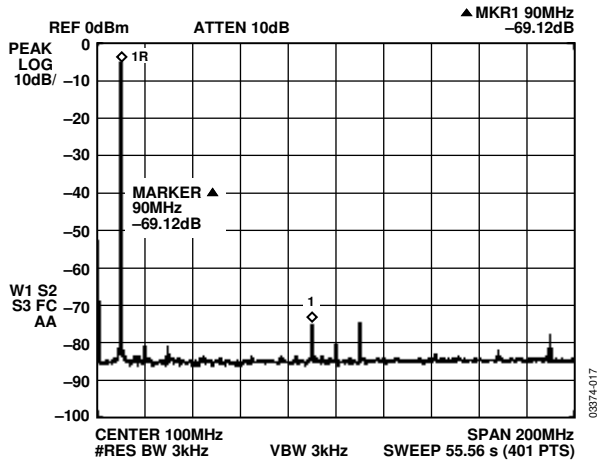


Figure 6.  $f_{OUT} = 10\text{ MHz}$ ,  $f_{CLK} = 400\text{ MSPS}$ , WBSFDR

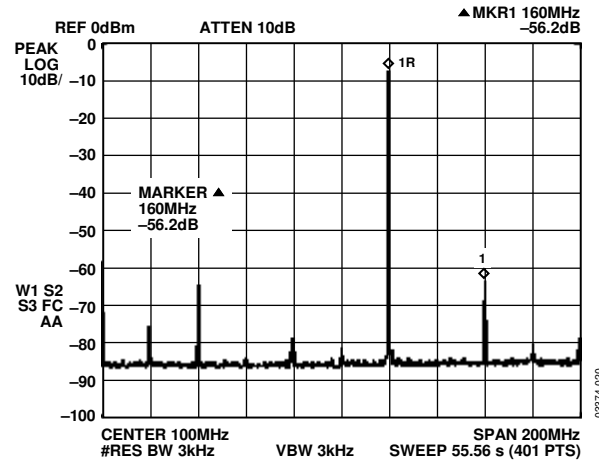


Figure 9  $f_{OUT} = 120\text{ MHz}$ ,  $f_{CLK} = 400\text{ MSPS}$ , WBSFDR

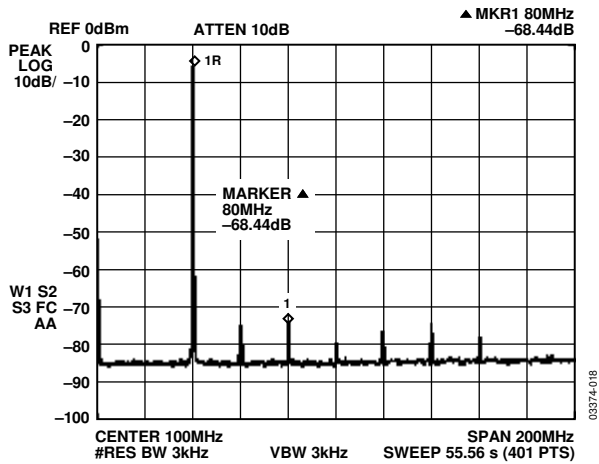


Figure 7.  $f_{OUT} = 40\text{ MHz}$ ,  $f_{CLK} = 400\text{ MSPS}$ , WBSFDR

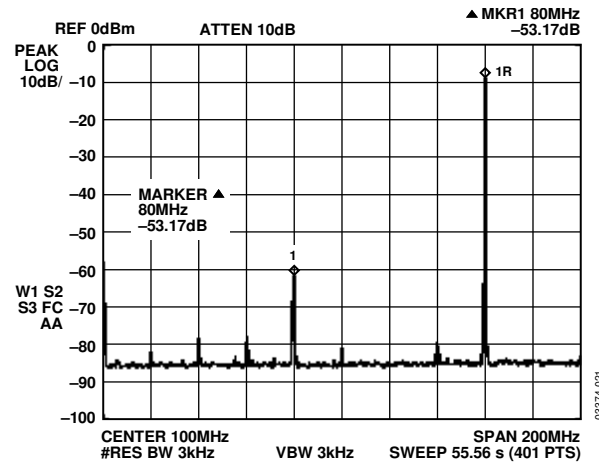


Figure 10.  $f_{OUT} = 160\text{ MHz}$ ,  $f_{CLK} = 400\text{ MSPS}$ , WBSFDR

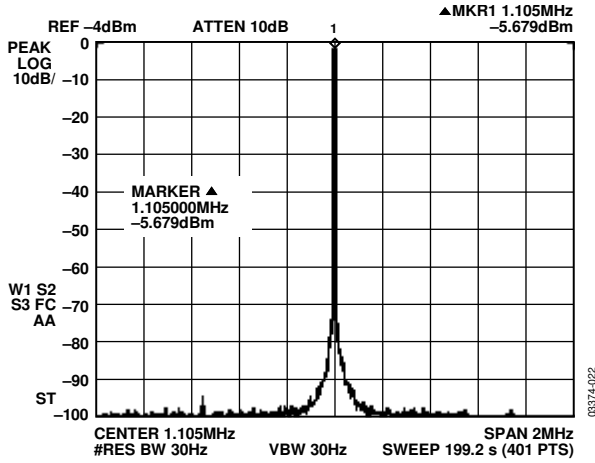


Figure 11.  $f_{OUT} = 1.1 \text{ MHz}$ ,  $f_{CLK} = 400 \text{ MSPS}$ , NBSFDR,  $\pm 1 \text{ MHz}$

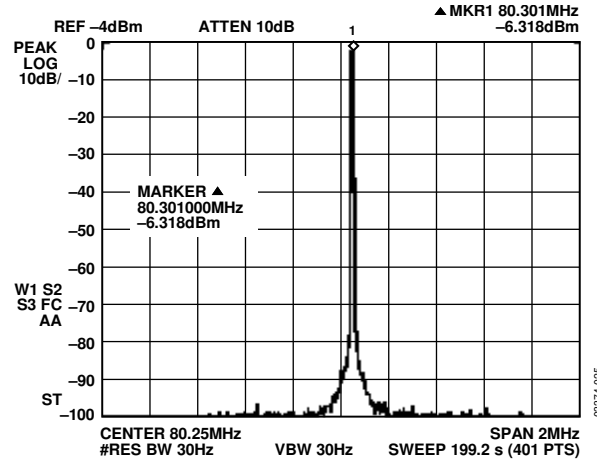


Figure 14.  $f_{OUT} = 80.3 \text{ MHz}$ ,  $f_{CLK} = 400 \text{ MSPS}$ , NBSFDR,  $\pm 1 \text{ MHz}$

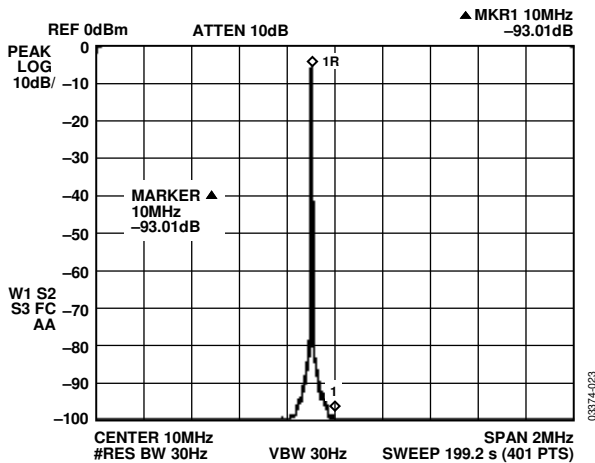


Figure 12.  $f_{OUT} = 9.5 \text{ MHz}$ ,  $f_{CLK} = 400 \text{ MSPS}$ , NBSFDR,  $\pm 1 \text{ MHz}$

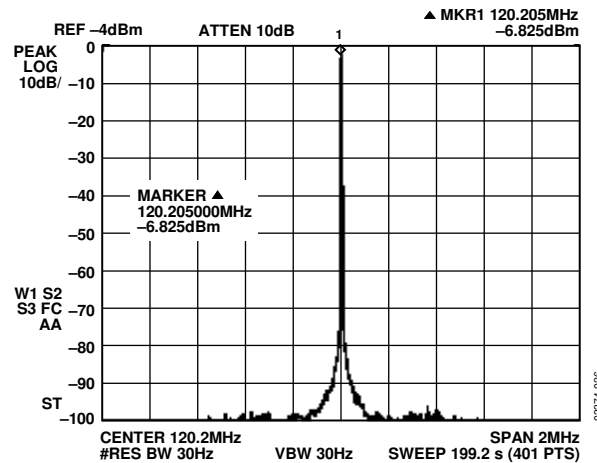


Figure 15.  $f_{OUT} = 120.2 \text{ MHz}$ ,  $f_{CLK} = 400 \text{ MSPS}$ , NBSFDR,  $\pm 1 \text{ MHz}$

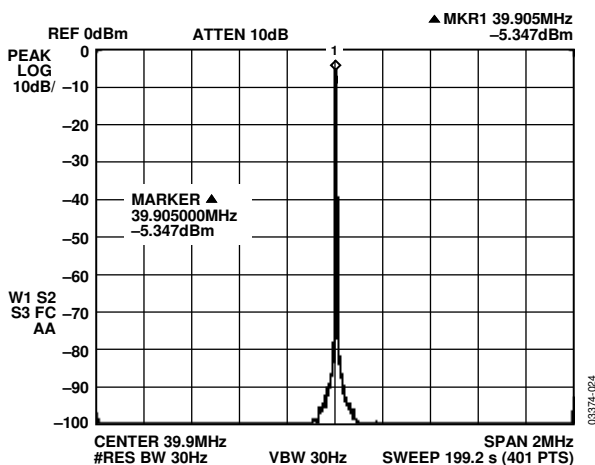


Figure 13.  $f_{OUT} = 39.9 \text{ MHz}$ ,  $f_{CLK} = 400 \text{ MSPS}$ , NBSFDR,  $\pm 1 \text{ MHz}$

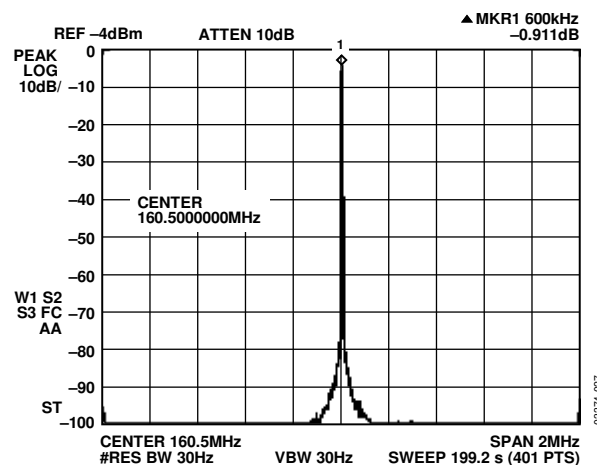


Figure 16.  $f_{OUT} = 160 \text{ MHz}$ ,  $f_{CLK} = 400 \text{ MSPS}$ , NBSFDR,  $\pm 1 \text{ MHz}$

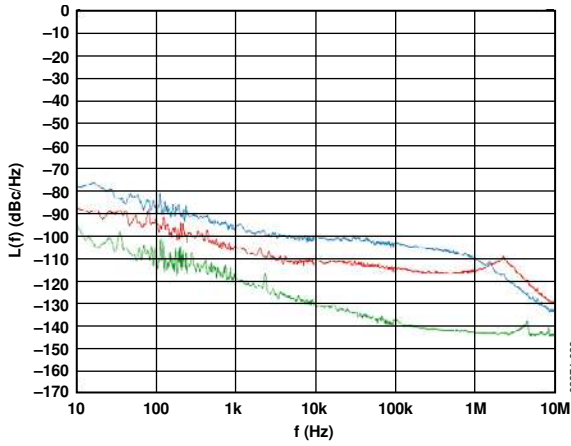


Figure 17. Residual Phase Noise with  $f_{OUT} = 159.5$  MHz,  $f_{CLK} = 400$  MSPS; PLL Bypassed (Green), PLL Set to 4x (Red), and PLL Set to 20x (Blue)

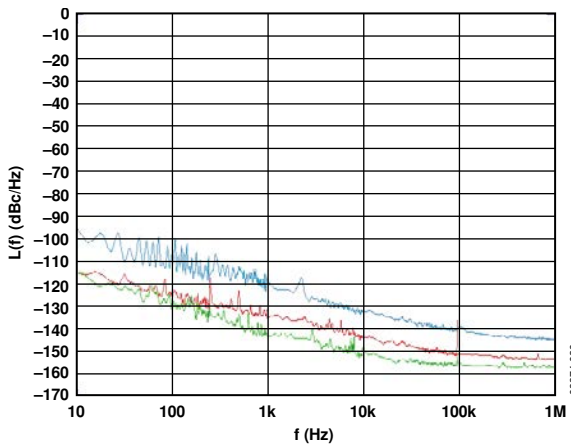


Figure 18. Residual Phase Noise with  $f_{OUT} = 9.5$  MHz,  $f_{CLK} = 400$  MSPS; PLL Bypassed (Green), PLL Set to 4x (Red), and PLL Set to 20x (Blue)

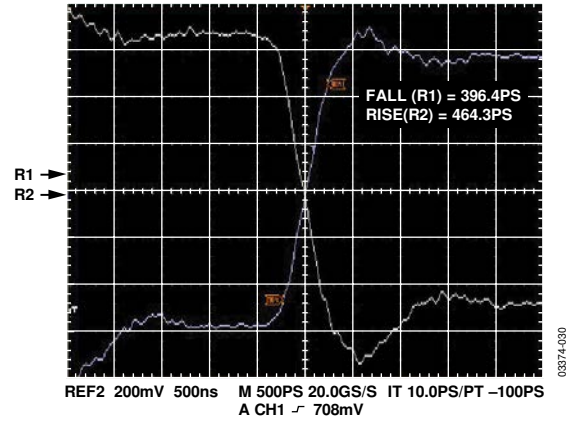


Figure 19. Comparator Rise and Fall Time at 160 MHz

## THEORY OF OPERATION

### COMPONENT BLOCKS

#### REFCLK Input

The AD9954 supports several methods for generating the internal system clock. An on-chip oscillator circuit is available for initiating the low frequency reference signal by connecting a crystal to the clock input pins. The system clock can be generated using an internal, PLL-based reference clock multiplier, allowing the part to operate with a low frequency clock source while still providing a high sample rate for the DDS and DAC. For best phase noise performance, a clean, stable clock with a high slew rate should be used to drive the REFCLK pin and bypass the multiplier.

The available modes are configured using the CLKMODESELECT pin, CFR1<4> and CFR2<7:3>. Note that the CLKMODESELECT pin is a 1.8 V logic only and does not apply to 3.3 V logic. Pulling CLKMODESELECT high enables the on-chip crystal oscillator circuit. With the on-chip oscillator enabled, users of the AD9954 connect an external crystal to the REFCLK and REFCLK inputs to produce a low frequency reference clock (see Table 1 for the crystal frequency range supported). The signal generated by the oscillator is buffered, and then delivered to the rest of the chip. This buffered signal is provided on the CRYSTAL OUT pin.

When the internal oscillator is disabled, an external oscillator must provide the REFCLK and/or REFCLK signals. For differential operation, these pins are driven with complementary signals. For single-ended operation, a 0.1  $\mu\text{F}$  capacitor should be connected between the unused pin and the analog power supply. With the capacitor in place, the clock input pin bias voltage is 1.35 V. Table 5 summarizes the clock modes of operation. Note the PLL multiplier is controlled via the CFR2<7:3> bits, independent of the CFR1<4> bit.

#### Clock Multiplier

An on-board PLL allows multiplication of the REFCLK frequency. The multiplication factor is set using CFR2<7:3>. When programmed for values ranging from 0x04 to 0x14 (decimal 4 to 20), the PLL multiplies the REFCLK input frequency by the programmed value. The user must consider the specified maximum frequency for the PLL when programming. If the multiplication factor is changed, the user must allocate time to allow the PLL to lock (approximately 1 ms).

The PLL is bypassed by programming a value outside the range of 4 to 20 (decimal). When bypassed, the PLL is shut down to conserve power.

The VCO in the PLL has a selectable frequency range. Use the VCO

range bit (CFR2<2>) to set the appropriate range.

The PLL in the clock multiplier has a loop filter comprised of on-chip components as well as external components. Recommended values for the external resistor/capacitor are provided in Table 4.

**Table 4. External Loop Filter Components for Clock Multiplier**

Multiply Value	Resistor Value	Capacitor Value ( $\mu\text{F}$ )
4 $\times$	0 $\Omega$	0.1
10 $\times$	1 k $\Omega$	0.1
20 $\times$	243 $\Omega$	0.01

#### DAC Output

Unlike many DACs, the DAC output on the AD9954 is referenced to AVDD, not AGND.

Two complementary outputs provide a combined full-scale output current ( $I_{\text{OUT}}$ ). Differential outputs reduce the amount of common-mode noise that may be present at the DAC output, resulting in a better signal-to-noise ratio. The full-scale current is controlled by means of an external resistor ( $R_{\text{SET}}$ ) connected between the DAC\_RSET pin and the DAC ground pin (Pin 49, the exposed paddle). The full-scale current is proportional to the resistor value by the equation

$$R_{\text{SET}} = (39.19/I_{\text{OUT}}) \Omega$$

The maximum full-scale output current of the combined DAC outputs is 15 mA. Limiting the output to 10 mA maximum provides the best spurious-free dynamic range (SFDR) performance. The DAC output compliance range is AVDD + 0.5 V to AVDD - 0.5 V. Voltages developed beyond this range result in excessive DAC distortion and could potentially damage the DAC output circuitry. Proper attention should be paid to the load termination to keep the output voltage within this compliance range.

**Table 5. Clock Input Modes of Operation**

CFR1<4>	CLKMODESELECT	CFR2<7:3>	Oscillator Enabled?	System Clock	Frequency Range (MHz)
Low	High	$4 \leq M \leq 20$	Yes	$f_{\text{CLK}} = f_{\text{OSC}} \times M$	$80 < f_{\text{CLK}} < 400$
Low	High	$M < 4$ or $M > 20$	Yes	$f_{\text{CLK}} = f_{\text{OSC}}$	$20 < f_{\text{CLK}} < 30$
Low	Low	$4 \leq M \leq 20$	No	$f_{\text{CLK}} = f_{\text{OSC}} \times M$	$80 < f_{\text{CLK}} < 400$
Low	Low	$M < 4$ or $M > 20$	No	$f_{\text{CLK}} = f_{\text{OSC}}$	$10 < f_{\text{CLK}} < 400$
High	X	X	No	$f_{\text{CLK}} = 0$	N/A



### Comparator

Some applications (for example, clocking) prefer a square-wave signal rather than a sine wave. In support of such applications, the AD9954 includes an on-chip comparator. The comparator has a bandwidth greater than 200 MHz and a common-mode input range of 1.3 V to 1.8 V. The comparator can be turned off to reduce power consumption using the comparator power-down bit, CFR1<6>.

### Frequency Accumulator

This block is used for linear sweep mode; transitioning from the start frequency (F0) to the terminal frequency (F1) is not instantaneous but instead is implemented in a swept or ramped fashion. This frequency ramping is accomplished by stepping through intermediate frequencies between F0 and F1.

The linear sweep block uses the falling and rising delta frequency tuning words, the falling and rising delta frequency ramp rates, and the frequency accumulator. The Linear Sweep Enable Bit CFR1<21> enables the linear sweep block. The linear sweep no dwell bit establishes the action to be performed upon reaching the terminal frequency in a sweep. See the Modes of Operation section for more details.

### DDS Core

The output frequency ( $f_o$ ) of the DDS is a function of the frequency of system clock (SYSCLK), the value of the frequency tuning word (FTW), and the capacity of the phase accumulator ( $2^{32}$ , in this case). The exact relationship is given below with  $f_s$  defined as the frequency of SYSCLK.

$$f_o = (FTW)(f_s)/2^{32} \text{ with } 0 \leq FTW \leq 2^{31}$$

$$f_o = f_s \times (1 - (FTW/2^{32})) \text{ with } 2^{31} < FTW < 2^{32} - 1$$

Each system clock cycle, the FTW is added to the value previously held in the phase accumulator. The value at the output of the phase accumulator is then summed with a user-defined, 14-bit phase offset value (POW). The most significant 19 bits of that summation are then translated to an amplitude value via the cos(x) functional block. Truncation of the LSBs is implemented to reduce the power consumption of the DDS core. This truncation does not reduce frequency resolution.

In certain applications, it is desirable to have the ability to force the output signal to zero phase. Simply setting the FTW to 0 does not accomplish this; it only stalls the core at its current phase value. A control bit is provided to force the phase accumulator output to zero.

At power-up, the clear phase accumulator bit is set to Logic 1, but the buffer memory for this bit is cleared (Logic 0). Therefore, upon power-up, the phase accumulator remains clear until the first I/O UPDATE is issued. I/O UPDATE transfers data from the input buffers to the active control registers. See the Functionality of the SYNC\_CLK and I/O UPDATE section for more details.

### Frequency Tuning Word Mux

As shown in Figure 2, there are three sources for the FTW

that are fed to the DDS core as the seed value for the phase accumulator: a frequency accumulator, the static RAM, and the registers of the control logic.

For applications where a static output frequency or more than four predefined output frequencies need to be switched between, in some variable or undefined order, the primary method of setting the FTW is by programming the desired value into the FTW0 register.

For applications where up to four specific sets of FTWs, or predefined series of FTWs are needed, the on-board RAM can be programmed with the desired FTWs, and the profile pins can be used to toggle between those sets/series.

For applications where a steady sweeping of frequency is desired, a second frequency accumulator is provided. The seed value and minimum/maximum numbers for the frequency accumulator are user programmable, although certain rules must be followed to avoid overflowing that accumulator.

### Phase Offset Word Mux

As shown in Figure 2, there are two sources for the POW that are fed to the DDS core as an adder to the output of the phase accumulator: the static RAM and the registers of the control logic. Using this feature enables synchronization of the DDS output to other system signals as well as phase modulation.

For applications where a static output phase or more than four predefined output phases need to be switched between, in some variable or undefined order, the primary method of setting the POW is by programming the desired value into the POW0 register.

For applications where up to four specific sets of POWs, or predefined series of POWs are needed, the on-board RAM can be programmed with the desired POWs, and the profile pins can be used to toggle between those sets/series.

The phase offset formula is

$$\Phi = \left( \frac{\text{POW}}{2^{14}} \right) \times 360^\circ$$

A digital delay block exists in the phase offset programming path to ensure matched latency with changes to the frequency tuning word. This enables users to easily program the device to change from one combined phase/frequency combination to another smoothly and seamlessly.

### Continuous and Clear-and-Release Frequency and Phase Accumulator Clear Functions

The AD9954 allows for a continuous zeroing of the frequency sweep logic and the phase accumulator as well as a clear and release or automatic zeroing function. The auto clear bits are CFR1<14:13>. The continuous clear bits are CFR1<11:10>.

**Clear-and-Release Function**

When set for auto clearing, the corresponding accumulator is cleared and then begins to accumulate again upon receipt of an I/O update or change on one of the profile pins. This is repeated for every subsequent I/O update or change on one of the profile pins until the appropriate autoclear control bit is cleared. It is perfectly valid to have one accumulator set to autoclearing and the other set to continuous clear.

**Amplitude Control Options**

**Shaped On-Off Keying**

The shaped on-off keying function is enabled/disabled using the OSK enable bit (CFR1<25>). This function allows the user to control the ramp-up and ramp-down time when turning the DAC on or off. This function is primarily used in burst transmissions of digital data to reduce the adverse spectral impact of short, abrupt bursts of data.

Both auto and manual shaped on-off keying modes are supported. CFR1<24> is used to select between auto and manual on-off keying modes. Figure 20 shows the block diagram of the OSK circuitry.

**Autoshaped On-Off Keying Mode Operation**

When autoshaped on-off keying mode is enabled, a single-scale factor is internally generated and applied to the multiplier input for scaling the output of the DDS core block (see Figure 20). The scale factor is the output of a 14-bit counter that increments/decrements at a rate determined by the contents of the 8-bit output ramp rate register. The scale factor increments if the OSK pin is high and decrements if the OSK pin is low. The scale factor is an unsigned value; all 0s multiply the DDS core output by 0 (decimal), and 0x3FFF multiplies the DDS core output by 16,383 (decimal).

Table 6 details the increment/decrement step size of the internally generated scale factor per the ASF<15:14> bits.

Note that the maximum amplitude allowed is limited by the

contents of the amplitude scale factor register, allowing the user to ramp to a value less than full scale.

**Table 6. Autoscale Factor Internal Step Size**

ASF<15:14> (Binary)	Increment/Decrement Size
00	1
01	2
10	4
11	8

**OSK Ramp Rate Timer**

The OSK ramp rate timer is a loadable down counter, which generates the clock signal to the 14-bit counter that generates the internal scale factor. The ramp rate timer is loaded with the value of the autoscale factor register (ASFR) every time the counter reaches 1 (decimal). This load and countdown operation continues for as long as the timer is enabled, unless the timer is forced to load before reaching a count of 1.

If the load ARR control bit (CFR1<26>) is set, the ramp rate timer is loaded upon an I/O update, upon a change in profile input, or upon reaching a value of 1. The ramp timer can be loaded before reaching a count of 1 by three methods.

The first method is by toggling the OSK pin or sending a rising edge to the I/O UPDATE pin (or changing the state of a profile pin). For this method, the ASFR value is loaded into the ramp rate timer, which then proceeds to count down as normal.

The second method is if the load ARR control bit (CFR1<26>) is set and an I/O update (or change in profile) is issued.

The last method is by setting the sweep enable bit. This switches from inactive autoshaped on-off keying mode to the active autoshaped on-off keying mode.

**Manual Shaped On-Off Keying Mode Operation**

When configured for manual shaped on-off keying, the content of the ASFR sets the scale factor for the data path

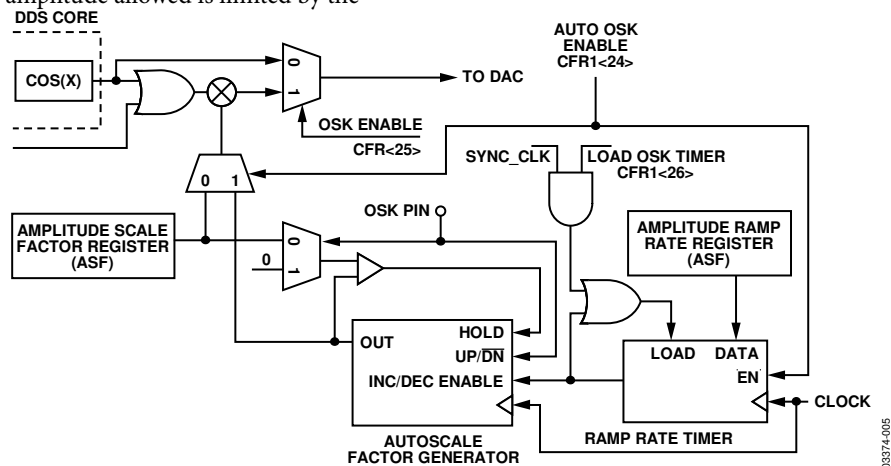


Figure 20. On-Off Shaped Keying, Block Diagram

## MODES OF OPERATION

### Single-Tone Mode

In single-tone mode, the DDS core uses a static tuning word. Whatever value is stored in FTW0 is supplied to the phase accumulator. This value can only be changed manually by writing a new value to FTW0 and then by issuing an I/O update. Phase adjustments are made using the phase offset register.

### RAM-Controlled Modes of Operation

Three important points apply to the RAM-controlled modes:

- The user must ensure that the beginning address is lower than the final address.
- Changing profiles or issuing an I/O update automatically terminates the current sweep and starts the next sweep, unless otherwise stated.
- Setting the RAM destination bit true such that the RAM output drives the phase offset adder is valid. While the sections that follow describe frequency sweeps, phase sweep operation is also available. The RAM destination bit (CFR1<30>) controls whether the RAM output drives the phase accumulator (frequency) or the phase offset adder (phase).

The AD9954 offers five modes of RAM-controlled operation (see Table 7).

**Table 7. RAM Modes of Operation**

RSCW<7:5> (Binary)	Mode	Notes
000	Direct Switch	No sweeping, profiles valid, no dwell ignored
001	Ramp Up	Sweeping, profiles valid, no-dwell valid
010	Bidirectional Ramp	Sweeping, PS0 is a direction control pin, no-dwell ignored
011	Continuous Bidirectional Ramp	Sweeping, profiles valid, no-dwell ignored
100	Continuous Recirculation	Sweeping, profiles valid, no-dwell ignored
101, 110, 111	Invalid mode	Default to direct switch

### Direct Switch Mode

Direct switch mode enables frequency shift keying (FSK) or phase shift keying (PSK) modulation. The AD9954 is programmed for direct switch using the RAM enable bit (CFR1<31>) and programming the RAM segment mode control bits of each desired profile to 000(b). This mode simply reads the RAM contents at the RAM segment beginning address for the current profile. No address ramping occurs in this mode.

To perform 4-tone shift keying, the user programs each RAM segment control word for direct switch mode and a unique beginning address value. Program the RAM enable and RAM destination bits (CFR1<31:30>) to enable the RAM and direct the RAM output to be the FTW (FSK) or the POW (PSK). The PS1 and PS0 inputs are the 4-tone FSK/PSK data inputs. When the profile is changed, the data stored at the new profile is loaded into either the phase accumulator (FSK) or the phase offset adder (PSK). When set for PSK, Bits<17:0> of the RAM output are unused when the RAM destination bit is set. Two-tone shift keying only uses one profile pin.

### Ramp-Up Mode

Ramp-up mode, in conjunction with the segmented RAM capability, allows up to four different sweep profiles to be programmed into the AD9954. The AD9954 is programmed for ramp-up mode by enabling the RAM using the RAM enable bit (CFR1<31>) and programming the RAM mode control bits of each profile to be used to 001(b).

When a sweep is initiated (via an I/O update or change in profile bits), the RAM address generator loads the RAM segment beginning address bits of the current RSCW, driving the RAM output from this address, and the ramp rate timer loads the RAM segment address ramp rate bits. When the ramp rate timer finishes a cycle, the RAM address generator increments to the next address, the timer reloads the ramp rate bits and begins a new countdown cycle. This sequence continues until the RAM address generator has incremented to an address equal to the RAM segment final address bits of the current RSCW. At this point, the next state is dependent upon whether no-dwell mode is active. See the no-dwell bit (CFR1<2>) in the register maps (see Table 12 and Table 13).

In this mode, asymmetrical FSK modulation can be implemented by configuring the RAM for two segments, and using the PS0 pin as the data input.

### Bidirectional Ramp Mode

Bidirectional ramp mode allows the AD9954 to offer a symmetrical sweep between two frequencies using the PS0 signal as the control input. The AD9954 is programmed for bidirectional ramp mode using the RAM enable bit (CFR1<31>) and programming the RAM segment mode control bits of each desired profile to 010(b). PS1 input is ignored; the PS0 input is the ramp direction indicator. The memory is not segmented, using only one beginning and one final address. The address registers for controlling RAM are located in the RAM segment control word (RSCW) associated with Profile 0.

Upon entering this mode (via an I/O update or changing the PS0 pin), the RAM address generator loads the RAM segment beginning address bits of RSCW0 and the ramp rate timer loads the RAM segment address ramp rate bits. The RAM drives data from the beginning address, and the ramp rate timer begins counting down to 1. When the timer reaches zero, the RAM address is incremented if PS0 is high and decrements if PS0 is low. Toggling the PS0 pin does not cause the device to generate an internal I/O update; transfers of data from the I/O buffers to the internal registers are only initiated by a rising edge on the I/O UPDATE pin.

RAM address control is now a function of the PS0 input. When polarity of the PS0 bit is changed, the RAM address generator increments/decrements to the next address and the ramp rate timer is reloaded. As in the ramp-up mode, this sequence continues until the RAM address generator has incremented/decremented to an address equal to the final/beginning address as long as the PS0 input remains high/low. Once the final/beginning address is reached, the sweep stalls until the polarity on PS0 is changed.

All data in the RAM segment control words associated with Profile 1, Profile 2, and Profile 3 are ignored. Only the information in the RAM segment control word for Profile 0 is used to control the RAM.

### Continuous Bidirectional Ramp Mode

Continuous bidirectional ramp mode allows the AD9954 to offer an automatic, symmetrical sweep between two frequencies. The AD9954 is programmed for continuous bidirectional ramp mode using the RAM enable bit (CFR1<31>) and programming the RAM segment mode control bits of each desired profile to 011(b). In general, this mode is identical in control to the bidirectional ramp mode, except the ramp up and down is automatic (no external control via the PS0 input), and switching profiles are valid. This mode enables generation of an automatic saw tooth sweep characteristic.

Upon entering this mode (via an I/O update or changing the PS1 or PS0 pins), the RAM address generator loads the RAM segment beginning address bits of the current RSCW and the ramp rate timer loads the RAM segment address ramp rate bits. The RAM drives data from the beginning address, and the ramp rate timer begins counting down to 1. When the ramp rate timer completes the countdown, the RAM address generator increments to the next address, and the timer reloads the ramp rate bits and continues counting down. This continues until the RAM address generator has incremented to an address equal to the RAM segment final address bits of the current RSCW. Upon reaching this final address, the RAM address generator begins decrementing each time the ramp rate timer completes a countdown cycle until it reaches the RAM segment beginning address. Upon reaching the beginning address, the entire sequence repeats until a new mode is selected.

### Continuous Recirculation Mode

Continuous recirculation mode allows the AD9954 to offer an automatic, continuous unidirectional sweep between two frequencies. The AD9954 is programmed for continuous recirculation mode using the RAM enable bit (CFR1<31>) and programming the RAM segment mode control bits of each desired profile to 100(b).

Upon entering this mode (via an I/O update or changing Pin PS1 or Pin PS0), the RAM address generator loads the RAM segment beginning address bits of the current RSCW and the ramp rate timer loads the RAM segment address ramp rate bits. The RAM drives data from the beginning address, and the ramp rate timer begins to count down to 1. When the ramp rate timer completes a cycle, the RAM address generator increments to the next address, and the timer reloads the ramp rate bits and continues counting down. This sequence continues until the RAM address generator has incremented to an address equal to the RAM segment final address bits of the current RSCW. Upon reaching this terminal address, the RAM address generator reloads the RAM segment beginning address bits and the sequence repeats until a new mode is selected.

### Internal Profile Control

The AD9954 offers a mode in which a composite frequency sweep can be built with software-programmable timing control. Internal profile control capability disengages the PS1 pin and the PS0 pin and enables the AD9954 to take control of switching between profiles. Modes are defined that allow continuous or single-burst profile switches for three combinations of profile selection bits (see Table 8). Internal profile control mode is engaged using Bits CFR1<29:27> per Table 8 Internal profile control is only valid when the device is operating in RAM mode. There is no internal profile control for linear sweeping operations.

When the internal profile control mode is engaged, the RAM segment mode control bits are ignored; the device operates all profiles in ramp-up mode. Switching between profiles occurs when the RAM address generator has exhausted the memory contents for the current profile.

Table 8. Internal Profile Control

CFR1<29:27> (Binary)	Mode Description
000	Internal control inactive
001	Internal control active, single-burst, activate Profile 0, then Profile 1, then stop
010	Internal control active, single-burst, activate Profile 0, then Profile 1, then Profile 2, then stop
011	Internal control active, single-burst, activate Profile 0, then Profile 1, then Profile 2, then Profile 3, then stop
100	Internal control active, continuous, activate Profile 0, then Profile 1, then Loop Starting 0
101	Internal control active, continuous, activate Profile 0, then Profile 1, then Profile 2, then Loop Starting 0
110	Internal control active, continuous, activate Profile 0, then Profile 1, then Profile 2, then Profile 3, and then Loop Starting 0
111	Invalid

A single-burst mode is one in which the composite sweep is executed once. For example, assume the device is programmed for ramp-up mode and the CFR1<29:27> bits are written to Logic 010(b). Upon receiving an I/O update, the internal control logic signals the device to begin executing the ramp-up mode sequence for Profile 0. Upon reaching the RAM segment final address value for Profile 0, the device jumps to the beginning address of Profile 1 and begins executing that ramp-up sequence. Upon reaching the RAM segment final address value for Profile 1, the device jumps to the beginning address of Profile 2 and begins executing that ramp-up sequence. When the RAM segment final address value for Profile 2 is reached, the sequence is over and the composite sweep has completed. Issuing another I/O update restarts the burst process.

A continuous internal profile control mode is one in which the composite sweep is continuously executed for as long as the device is programmed into that mode. Using the previous example, except programming the CFR1<29:27> bits to Logic 101(b), the operation would be identical until the RAM segment final address value for Profile 2 is reached. At this point, instead of stopping the sequence, the device jumps back to the beginning address of Profile 0 and continues sweeping.

### Linear Sweep Mode

The AD9954 is placed in linear sweep mode using the Linear Sweep Enable Bit CR1<21>. PS1 must be tied low. When in linear sweep mode, the AD9954 output frequency ramps up from a starting frequency, programmed by FTW0 to a finishing frequency FTW1, or down from FTW1 to FTW0. The delta frequency tuning words and the ramp rate word determine the rate of this ramping. The Linear Sweep No-Dwell Bit CFR1<2> controls the behavior of the device upon reaching the final frequency.

When PS0 is high, the 32-bit rising delta frequency tuning word (RDFTW) is the seed value for the frequency accumulator, it

ramps from FTW0 to FTW1 and the RSRR register is loaded into the sweep rate timer. When the timer counts down to one, the frequency accumulator cycles once, increasing by the seed value. This accumulation of the RDFTW at the rate given by the ramp rate (RSRR) continues until the output of the frequency adder is equal to the FTW1 register value, or PS0 is pulled low.

When PS0 is low, the 32-bit falling delta frequency tuning word (FDFTW) is the seed value for the frequency accumulator, it ramps down from FTW1 to FTW0 and the FSRR register is loaded into the sweep rate timer. When the timer counts down to one, the frequency accumulator cycles once, decreasing by the seed value. This accumulation of the FDFTW at the rate given by the ramp rate (FSRR) continues until the output of the frequency adder is equal to the FTW0 register value, or PS0 is pulled high.

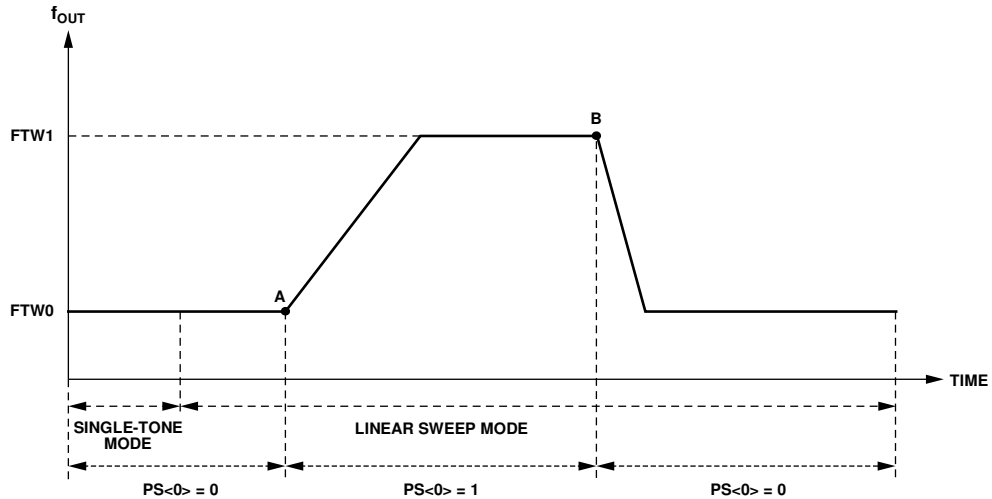
Pin PS0 controls the direction of the sweep, rising to FTW1 or falling to FTW0. Upon reaching the destination frequency, the AD9954 linear sweep function either holds at the destination frequency until the state on PS0 is changed or immediately returns to the initial frequency, FTW0, depending on the state of the Linear Sweep No-Dwell Bit CFR1<02>. While operating in linear sweep mode, toggling PS0 does not cause the device to generate an internal I/O update. When PS0 is acting as the sweep direction indicator, any transfer of data from the I/O buffers to the internal registers can only be initiated by a rising edge on the I/O UPDATE pin.

The linear sweep function of the AD9954 requires the lowest frequency to be loaded into the FTW0 register and the highest frequency into the FTW1 register. For piece-wise, nonlinear frequency transitions, it is necessary to reprogram the registers while the frequency transition is in process.

After a reset, the device is initially in single-tone mode. The programming steps to operate in linear sweep mode are:

1. PS1:0 = 00.
2. Set the linear sweep enable bit (CFR1<21>) and set or clear the linear sweep no-dwell bit (CFR1<2>) as desired.
3. Program the rising and falling delta frequency tuning words and ramp rate values.
4. Program the lower and higher output frequencies into the FTW0 and FTW1 registers, respectively.
5. Apply an I/O update to move this data into the registers (the instantaneous output frequency is FTW0).
6. Change the PS0 input as desired to sweep between the lower to higher frequency and back.

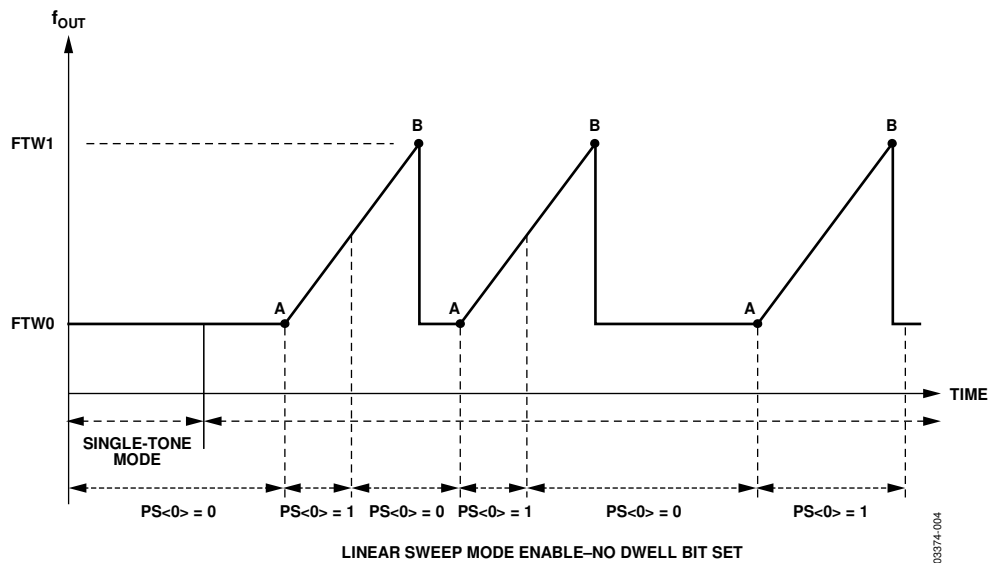
Figure 21 depicts a typical frequency ramping operation. The device initially powers up in single-tone mode. The profile inputs are low, setting FTW0 as the seed value for the phase accumulator. The user then writes to the linear sweep enable bit, the rising and falling delta frequency tuning words, and ramp rates via the serial port (Point A in Figure 21. In this example, the linear sweep no-dwell bit is cleared (CFR1<2>).



AT POINT A: LOAD RISING RAMP RATE REGISTER, APPLY RISING DFTW.  
 AT POINT B: LOAD FALLING RAMP RATE REGISTER, APPLY FALLING DFTW.

Figure 21. Linear Sweep Frequency Plan

03374-003



LINEAR SWEEP MODE ENABLE-NO DWELL BIT SET  
 Figure 22. Linear Sweep Using No-Dwell Frequency Plan

03374-004

**Linear Sweep No-Dwell Feature**

See CFR1<2> in the register maps (see Table 12 and Table 13) for general details of the no-dwell mode. Figure 22 depicts the linear sweep mode operation when the linear sweep no-dwell bit is set. The Label A points indicate where a rising edge on PS0 is detected; the Label B points indicate where the AD9954 has determined  $f_{OUT}$  has reached the terminal frequency and automatically returns to the starting frequency. Note that in this mode, only sweeps from FTW0 to FTW1 using the positive linear sweep control word are supported. Toggling PS0 from 1 to 0 neither initiates a falling sweep when the no-dwell bit is set, nor interrupts a positive sweep already underway.

**Resetting the Ramp Rate Timer**

The ramp timer can be reset before reaching a count of 1 by three methods.

Method one is by changing the PS0 input pin. When the PS0 input pin toggles from 0 to 1, the RSRRW value is loaded into the ramp rate timer, which then proceeds to countdown as normal. When the PS0 input pin toggles from 0 to 1, the falling sweep ramp rate word (FSRRW) value is loaded into the ramp rate timer, which then proceeds to countdown as normal.

The second method uses the LOAD SRR @ I/O UD bit (CFR1<15>), see Table 12 for details.

The last method in which the sweep ramp rate timer can be reset is changing from inactive linear sweep mode to active linear sweep mode using the linear sweep enable bit (CFR1<21>).

For methods two and three, the ramp rate timer loads a value determined by the state of PS0 (0 = FSRRW, 1 = RSRRW).

#### **Power-Down Functions of the AD9954**

The AD9954 supports an externally controlled (or hardware) power-down feature as well as software-programmable power-down bits capable of individually powering down specific unused circuit blocks.

Software-controlled power-down enables individual powering down of the DAC, comparator, PLL, input clock circuitry, and

the digital logic (CFR1<7:4>). With the exception of CFR1<6>, these bits are superseded when the externally controlled power-down pin (PWRDWNCTL) is high. External power-down control is supported on the AD9954 via the PWRDWNCTL input pin. When the PWRDWNCTL input pin is high, the AD9954 enters a power-down mode based on the CFR1<3> bit. When the PWRDWNCTL input pin is low, it operates normally. See CFR1<3> in Table 12 for details.

Table 9 details the logic level for each power-down bit that drives out of the AD9954 core logic to the analog section and the digital clock generation section of the chip for the external power-down operation.

**Table 9. Power-Down Control Functions**

<b>Control</b>	<b>Mode Active</b>	<b>Description</b>
PWRDWNCTL = 0, CFR1<3> don't care	Software control	Digital power-down = CFR1<7> Comparator power-down = CFR1<6> DAC power-down = CFR1<5> Clock input power-down = CFR1<4>
PWRDWNCTL = 1, CFR1<3> = 0	External control, fast recovery power-down mode	Digital power-down = 1'b1 Comparator power-down = 1'b0 or CFR1<6> DAC power-down = 1'b0 Clock input power-down = 1'b0
PWRDWNCTL = 1, CFR1<3> = 1	External control, full power-down mode	Digital power-down = 1'b1 Comparator power-down = 1'b1 DAC power-down = 1'b1 Clock input power-down = 1'b1

**SYNCHRONIZATION—REGISTER UPDATES (I/O UPDATE)**

**Functionality of the SYNC\_CLK and I/O UPDATE**

Data into the AD9954 is synchronous to the SYNC\_CLK signal (supplied externally to the user on the SYNC\_CLK pin). The I/O UPDATE pin is sampled on the rising edge of the SYNC\_CLK.

Internally, SYSCLK is fed to a divide-by-four frequency divider to produce the SYNC\_CLK signal. The SYNC\_CLK signal is made available to the system on the SYNC\_CLK pin. This enables synchronization of external hardware with the device’s internal clocks. This is accomplished by providing the SYNC\_CLK signal as an output that external hardware can then use to synchronize against.

The I/O update signal coupled with SYNC\_CLK is used to transfer internal buffer contents into the control registers. The combination of the SYNC\_CLK pin and the I/O UPDATE pin provides the user with constant latency relative to SYSCLK and ensures phase continuity of the analog output signal when a new tuning word or phase offset value is asserted.

Figure 23 and Figure 24 demonstrate an I/O update timing cycle and synchronization.

Synchronization logic notes include the following:

- The I/O update signal is edge detected to generate a single-cycle clock signal that drives the register bank flops. The I/O update signal has no constraints on duty cycle. The minimum low time on I/O update is one SYNC\_CLK clock cycle.
- The I/O UPDATE pin is set up and held around the rising edge of SYNC\_CLK. Setup and hold time specifications can be found in Table 2.

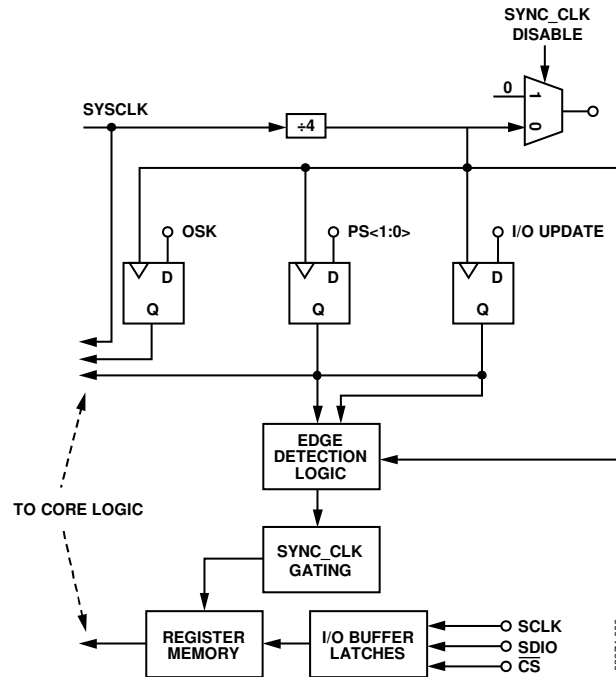
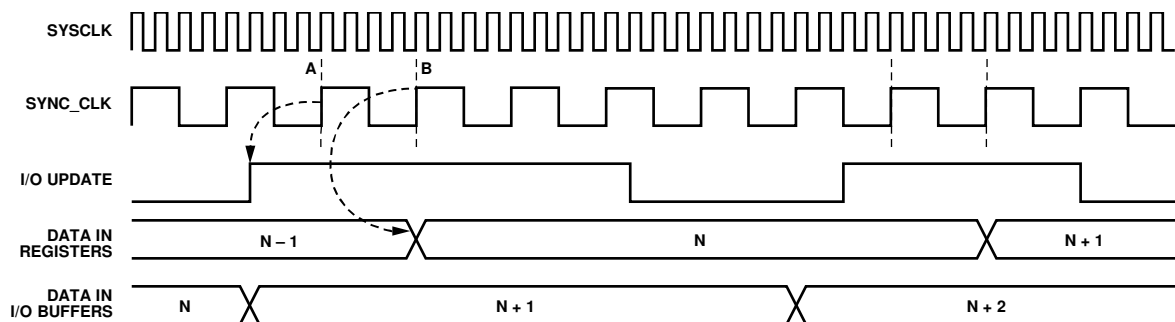


Figure 23. I/O Synchronization Block Diagram



THE DEVICE REGISTERS AN I/O UPDATE AT POINT A. THE DATA IS TRANSFERRED FROM THE ASYNCHRONOUSLY LOADED I/O BUFFERS AT POINT B.

Figure 24. I/O Synchronization Timing Diagram



### **Synchronizing Multiple AD9954s**

There are three modes of synchronization available to the user: an automatic synchronization mode, a software-controlled manual synchronization mode, and a hardware-controlled manual synchronization mode. The following requirements apply to all modes. First, all units must share a common clock source. Trace lengths and path impedance of the clock tree must be designed to keep the phase delay of the different clock branches as closely matched as possible. Second, the I/O update signal's rising edge must be provided synchronously to all devices being synchronized. Finally, the DVDD\_I/O supply should be set to 3.3 V for all devices that are to be synchronized. AVDD and DVDD should be left at 1.8 V.

In automatic synchronization mode, one device is chosen as a master, the other device(s) is slaved to this master. All slaves automatically synchronize their internal clocks to the SYNC\_CLK output signal of the master device. Use the automatic synchronization bit (CFR1<23>) to configure each slave. Connect the SYNC\_IN input(s) to the master SYNC\_CLK output. Slave devices continuously update the phase relationship of their SYNC\_CLK until it is in phase with the SYNC\_IN input. The high speed sync enhancement enable bit (CFR2<11>) must be programmed correctly.

In software manual synchronization mode, the user can force the device to advance the SYNC\_CLK rising edge one SYSCLK cycle ( $\frac{1}{4}$  SYNC\_CLK period). Manual synchronization mode is established using the slave device's software manual synchronization bit (CFR1<22>). See the bit description in Table 12 for more details.

In hardware manual synchronization mode, the SYNC\_IN input pin is configured such that it now advances the rising edge of the SYNC\_CLK signal each time the device detects a rising edge on the SYNC\_IN pin. Hardware manual synchronization mode is established using the hardware manual synchronization bit (CFR2<10>). See the bit description in Table 12 for more details.

### **Using a Single Crystal to Drive Multiple AD9954 Clock Inputs**

The AD9954 crystal oscillator output signal is available on the CRYSTAL OUT pin, enabling one crystal to drive multiple AD9954s. To drive multiple AD9954s with one crystal, the CRYSTAL OUT pin of the AD9954 using the external crystal should be connected to the REFCLK input of the other AD9954.

The CRYSTAL OUT pin must be enabled using the CRYSTAL OUT Pin Active Bit CFR2<9>. The drive strength of the CRYSTAL OUT pin is fairly low; therefore, the signal should be buffered if multiple loads are being driven.

### **RAM**

The AD9954 incorporates a block of SRAM. The RAM is a bidirectional single port. Read and write operations cannot occur simultaneously. Write operations to the serial I/O port take precedence; therefore, if an attempt to write to RAM is made during a read operation, the read operation is halted. The RAM is configurable using the RAM Segment Control Word<7:5> and data in the control function register.

Using the RAM enable bit (CFR1<31>), the RAM output can be enabled to drive the input to either the phase accumulator or the phase offset adder; the RAM destination bit (CFR1<30>) sets the routing. When the RAM output drives the phase accumulator, the phase offset word (POW, Address 0x05) drives the phase-offset adder. Conversely, when the RAM output drives the phase-offset adder, the frequency tuning word (FTW, Address 0x04) drives the phase accumulator. When CFR1<31> disables the RAM, it is inactive unless being written to via the serial port. The RAM is mapped into one of four profiles determined by the PS1 and PS0 input pins. Note that these profiles may overlap. For example, Profile 0 may use RAM Address Location 0 to Address Location 12, and Profile 1 may use RAM Address Location 5 to Address Location 20, and so forth.

All RAM write or read operations to/from the RAM are controlled by the PS1 and PS0 input pins and the respective RAM segment control word. To write to the RAM, a RAM segment must be defined in a RAM segment control word. The RAM segment that was defined must then be selected by use of the profile select pins, PS0 and PS1. With the correct RAM segment selected, the special instruction byte of 0xB0 should be sent. When the instruction byte to write to the RAM is sent to the part, the serial port controller immediately polls the corresponding RAM segment control word. From this register, the serial port controller makes note of the start address and the stop address. It then calculates how many entries there are in the segment, and how many bytes of data to expect. After sending the special instruction byte of 0xB0, the user must send all RAM entries for the currently selected profile to the part.

For example, consider a case where RAM Segment 2 begins at Address 21 and ends at Address 120. First, write to RAM Segment Control Word 2 with a starting address of 21, with a stop address of 120, and specify a ramp rate and a mode of operation. Next, set PS1 to 1 and PS0 to 0 to select RAM Segment 2 and then send the instruction byte of 0xB0. The part is now ready to put the first 32-bit word into the RAM at Address 21, to expect 100 32-bit words, and to store the last one at Address 120. It automatically controls sending the data from the serial port to the correct RAM address. Therefore, precede sending 100 32-bit words of data to the part. After the 3200th SCLK cycle, the write operation is complete, and all 100 words are stored in the RAM, from Address 21 to Address 120.

**Serial I/O Port**

The AD9954 serial port is a flexible, synchronous, serial communications port that easily interfaces to many industry-standard microcontrollers and microprocessors. The serial I/O port is compatible with most synchronous transfer formats, including both the Motorola 6905/11 SPI® and Intel® 8051 SSR protocols.

The interface accesses all registers that configure the AD9954. MSB first and LSB first transfer formats are supported. In addition, the AD9954's serial interface port can be configured as a single pin I/O (SDIO), which allows a 2-wire interface, or two unidirectional pins for in/out (SDIO/SDO), which enables a 3-wire interface. Two optional pins, IOSYNC and  $\overline{CS}$ , provide further flexibility for system design with the AD9954.

**SERIAL PORT OPERATION**

With the AD9954, the instruction byte specifies read/write operation and register address. Serial operations on the AD9954 only occur at the register level, they do not occur on the byte level. For the AD9954, the serial port controller recognizes the instruction byte register address and automatically generates the proper register byte address. In addition, the controller expects to access all bytes of that register. It is a requirement that all bytes of a register be accessed during serial I/O operations, with one exception; the IOSYNC function can be used to abort an I/O operation, thereby allowing less than all bytes to be accessed.

There are two phases to a communication cycle with the AD9954. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9954, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9954 serial port controller with information regarding Phase 2, the data transfer cycle. The instruction byte defines whether the upcoming data transfer is a read or a write and the serial address of the register being accessed.

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9954. The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9954 and the system controller. The number of bytes transferred during Phase 2 of the communication cycle is a function of the register being accessed. For example, when accessing the Control Function Register 2, which is three bytes wide, Phase 2 requires that three bytes be transferred. If accessing the frequency tuning word, which is four bytes wide, four bytes must be transferred. After transferring all data bytes per the instruction byte, the communication cycle is complete.

At the completion of any communication cycle, the AD9954 serial port controller expects the next eight rising SCLK edges to be the instruction byte of the next communication cycle. All data input to the AD9954 is registered on the rising edge of SCLK. All data is driven out of the AD9954 on the falling edge of SCLK. Figure 25 through Figure 28 are provided to aid in understanding the general operation of the AD9954 serial port.

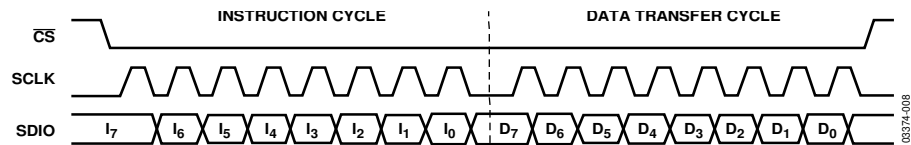


Figure 25. Serial Port Write Timing—Clock Stall Low

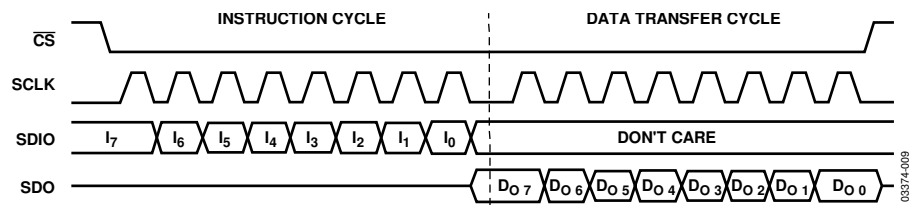


Figure 26. 3-Wire Serial Port Read Timing—Clock Stall Low

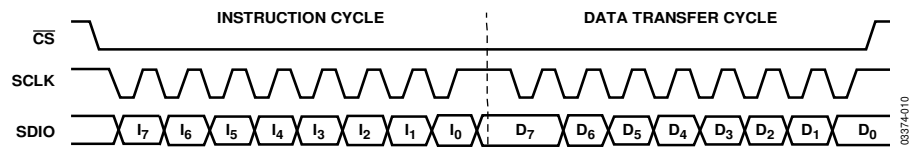


Figure 27. Serial Port Write Timing—Clock Stall High