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2.7 GHz DDS-Based *Agile*RF™ Synthesizer

AD9956

FEATURES

- 400 MSPS internal DDS clock speed
- 48-bit frequency tuning word
- 14-bit programmable phase offset
- Integrated 14-bit DAC
  - Excellent dynamic performance
  - Phase noise ≤ 135 dBc/Hz @ 1 KHz offset
  - −80 dB SFDR @ 160 MHz (±100 KHz offset I_{OUT})
- 25 Mb/s write-speed serial I/O control
- 200 MHz phase frequency detector inputs
- 655 MHz programmable input dividers for the phase frequency detector (÷M, ÷N) {M, N = 1..16} (bypassable)
- Programmable RF divider (÷R) {R = 1, 2, 4, 8} (bypassable)
- 8 phase/frequency profiles
- 1.8 V supply for device operation
- 3.3 V supply for I/O and charge pump
- Software controlled power-down
- 48-lead LFCSP package
- Automatic linear frequency sweeping capability (in DDS)
- Programmable charge pump current (up to 4 mA)
- Phase modulation capability
- Multichip synchronization
- Dual-mode PLL lock detect
- 655 MHz CML-mode PECL-compliant driver

APPLICATIONS

- Agile LO frequency synthesis
- FM chirp source for radar and scanning systems
- Automotive radars
- Test and measurement equipment
- Acousto-optic device drivers

FUNCTIONAL BLOCK DIAGRAM

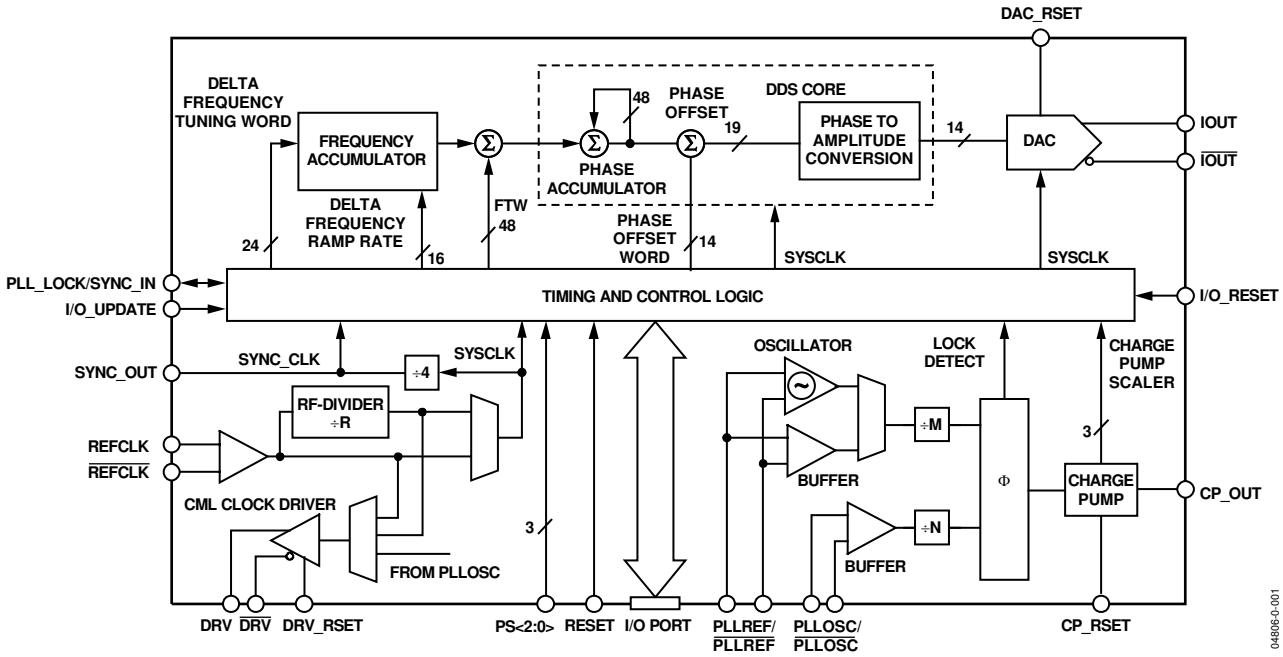

Figure 1.

Rev. A

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9956 Evaluation Board

DOCUMENTATION

Application Notes

- AN-237: Choosing DACs for Direct Digital Synthesis
- AN-280: Mixed Signal Circuit Technologies
- AN-342: Analog Signal-Handling for High Speed and Accuracy
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-419: A Discrete, Low Phase Noise, 125 MHz Crystal Oscillator for the AD9850
- AN-423: Amplitude Modulation of the AD9850 Direct Digital Synthesizer
- AN-543: High Quality, All-Digital RF Frequency Modulation Generation with the ADSP-2181 and the AD9850 DDS
- AN-557: An Experimenter's Project:
- AN-587: Synchronizing Multiple AD9850/AD9851 DDS-Based Synthesizers
- AN-605: Synchronizing Multiple AD9852 DDS-Based Synthesizers
- AN-621: Programming the AD9832/AD9835
- AN-632: Provisionary Data Rates Using the AD9951 DDS as an Agile Reference Clock for the ADN2812 Continuous-Rate CDR
- AN-769: Generating Multiple Clock Outputs from the AD9540
- AN-823: Direct Digital Synthesizers in Clocking Applications Time
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-843: Measuring a Loudspeaker Impedance Profile Using the AD5933
- AN-847: Measuring a Grounded Impedance Profile Using the AD5933
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design
- AN-927: Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)
- AN-939: Super-Nyquist Operation of the AD9912 Yields a High RF Output Signal
- AN-953: Direct Digital Synthesis (DDS) with a Programmable Modulus

Data Sheet

- AD9956: 400 MSPS 14-Bit DAC 48-Bit FTW 1.8 V CMOS DDS Based AgileRF™ Synthesizer Data Sheet

Product Highlight

- Introducing Digital Up/Down Converters: VersaCOMM™ Reconfigurable Digital Converters

TOOLS AND SIMULATIONS

- ADIsimDDS (Direct Digital Synthesis)
- AD9956 IBIS Models

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

Technical Articles

- 400-MSample DDSs Run On Only +1.8 VDC
- ADI Buys Korean Mobile TV Chip Maker
- Basics of Designing a Digital Radio Receiver (Radio 101)
- DDS Applications
- DDS Circuit Generates Precise PWM Waveforms
- DDS Design
- DDS Device Produces Sawtooth Waveform
- DDS Device Provides Amplitude Modulation
- DDS IC Initiates Synchronized Signals
- DDS IC Plus Frequency-To-Voltage Converter Make Low-Cost DAC
- DDS Simplifies Polar Modulation
- Digital Potentiometers Vary Amplitude In DDS Devices
- Digital Up/Down Converters: VersaCOMM™ White Paper
- Digital Waveform Generator Provides Flexible Frequency Tuning for Sensor Measurement
- Improved DDS Devices Enable Advanced Comm Systems
- Integrated DDS Chip Takes Steps To 2.7 GHz
- Simple Circuit Controls Stepper Motors
- Speedy A/Ds Demand Stable Clocks
- Synchronized Synthesizers Aid Multichannel Systems
- The Year of the Waveform Generator
- Two DDS ICs Implement Amplitude-shift Keying
- Video Portables and Cameras Get HDMI Outputs

DESIGN RESOURCES

- AD9956 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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TABLE OF CONTENTS

REVISION HISTORY

9/04—Data Sheet Changed from Rev. 0 to Rev. A

Changes to the Pin Configuration 11
Changes to the Pin Function Descriptions 12
Changes to Table 5 24
Changes to CFR2<15:12> PLLREF Divider Control Bits (÷N) 31
Changes to CFR2<11:8> PLLREF Divider Control Bits (÷M) 31
Changes to Ordering Guide 32

7/04—Revision: Initial Version

PRODUCT OVERVIEW

The AD9956 is Analog Devices' newest *Agile*RF synthesizer. The device is comprised of DDS and PLL circuitry. The DDS features a 14-bit DAC operating at up to 400 MSPS and a 48-bit frequency tuning word (FTW). The PLL circuitry includes a phase frequency detector with scaleable 200 MHz inputs (divider inputs operate up to 655 MHz) and digital control over the charge pump current. The device also includes a 655 MHz CML-mode PECL-compliant driver with programmable slew rates. The AD9956 uses advanced DDS technology, an internal high speed, high performance DAC, and an advanced phase frequency detector/charge pump combination, which, when used with an external VCO, enables the synthesis of digitally programmable, frequency-agile analog output sinusoidal waveforms up to 2.7 GHz. The AD9956 is designed to provide fast frequency hopping and fine tuning resolution (48-bit frequency tuning word). Information is loaded into the AD9956 via a serial I/O port that has a device write-speed of 25 Mb/s. The AD9956 DDS block also supports a user-defined linear sweep mode of operation.

The AD9956 is specified to operate over the extended automotive range of −40°C to +125°C.

SPECIFICATIONS

AVDD = DVDD = 1.8 V ± 5%; DVDD_I/O = CP_VDD = 3.3 V ± 5% (@ T_A = 25°C) DAC_R_{SET} = 3.92 kΩ, CP_R_{SET} = 3.09 kΩ, DRV_R_{SET} = 4.02 kΩ, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RF DIVIDER (REFCLK) INPUT SECTION (÷R)					
RF Divider Input Range	1		2700	MHz	DDS SYSCLK not to exceed 400 MSPS
Input Capacitance (DC)		3		pF	
Input Impedance (DC)		1500		Ω	
Input Duty Cycle	42	50	58	%	
Input Power/Sensitivity	−10		+4	dBm	Single-ended, into a 50 Ω load[1]
Input Voltage Level	350		1000	mV p-p	
PHASE FREQUENCY DETECTOR/CHARGE PUMP					
PLLREF Input					
Input Frequency[2]					
÷M Set to Divide by at Least 4			655	MHz	
÷M Bypassed			200	MHz	
Input Voltage Levels	200	450	600	mV p-p	
Input Capacitance			10	pF	
Input Resistance		1500		Ω	
PLLOSC Input					
Input Frequency					
÷N Set to Divide by at Least 4			655	MHz	
÷N Bypassed			200	MHz	
Input Voltage Levels	200	450	600	mV p-p	
Input Capacitance			10	pF	
Input Resistance		1500		Ω	
Charge Pump Source/Sink Maximum Current			4	mA	
Charge Pump Source/Sink Accuracy	−15		+5	%	
Charge Pump Source/Sink Matching	−5		+5	%	
Charge Pump Output Compliance Range[3]	0.5		CP_VDD – 0.5	V	
PLL_LOCK Drive Strength		2		mA	
PHASE FREQUENCY DETECTOR NOISE FLOOR					
@ 50 kHz PFD Frequency		149		dBc/Hz	
@ 2 MHz PFD Frequency		133		dBc/Hz	
@ 100 MHz PFD Frequency		116		dBc/Hz	
@ 200 MHz PFD Frequency		113		dBc/Hz	
CML OUTPUT DRIVER (DRV)					
Differential Output Voltage Swing[4]		720		mV	50 Ω load to supply, both lines
Maximum Toggle Rate	655			MHz	
Common-Mode Output Voltage		1.75		V	
Output Duty Cycle	42	50	58	%	
Output Current					
Continuous[5]		7.2		mA	
Rising Edge Surge		20.9		mA	
Falling Edge Surge		13.5		mA	
Output Rise Time		250		ps	100 Ω terminated, 5 pF load

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS (SDI/O, I/O_RESET, RESET, I/O_UPDATE, PS0 to PS2, SYNC_IN)					
V_{IH}, Input High Voltage	2.0			V	
V_{IL}, Input Low Voltage			0.8	V	
I_{INH}, I_{INL} Input Current		±1	±5	µA	
C_{IN}, Maximum Input Capacitance		3		pF	
LOGIC OUTPUTS (SDO, SYNC_OUT, PLL_LOCK)[6]					
V_{OH}, Output High Voltage	2.7			V	
V_{OH}, Output Low Voltage			0.4	V	
I_{OH}	100			µA	
I_{OL}	100			µA	
POWER CONSUMPTION					
Total Power Consumed, All Functions On			400	mW	
IAVDD			85	mA	
IDVDD			45	mA	
IDVDD_I/O			20	mA	
ICP_VDD			15	mA	
Power-Down Mode		80		mW	
WAKE-UP TIME (from Power-Down Mode)					
Digital Power-Down (CFR1<7>)		12		ns	
DAC Power-Down (CFR2<39>)		7		µs	
RF Divider Power-Down (CFR2<23>)		400		ns	
Clock Driver Power-Down (CFR2<20>)		6		µs	
Charge Pump Full Power-Down (CFR2<4>)		10		µs	
Charge Pump Quick Power-Down (CFR2<3>)		150		ns	
DAC OUTPUT CHARACTERISTICS					
Resolution		14		Bits	
Full-Scale Output Current		10	15	mA	
Gain Error	−10		+10	% FS	
Output Offset			0.6	µA	
Output Capacitance		5		pF	
Voltage Compliance Range	AVDD − 0.50		AVDD + 0.50	V	
Wideband SFDR (DC to Nyquist)					
10 MHz Analog Out		−64		dBc	
40 MHz Analog Out		−62		dBc	
80 MHz Analog Out		−60		dBc	
120 MHz Analog Out		−55		dBc	
160 MHz Analog Out		−55		dBc	
Narrowband SFDR					
10 MHz Analog Out (±1 MHz)		−89		dBc	
10 MHz Analog Out (±250 kHz)		−91		dBc	
10 MHz Analog Out (±50 kHz)		−93		dBc	
40 MHz Analog Out (±1 MHz)		−87		dBc	
40 MHz Analog Out (±250 kHz)		−89		dBc	
40 MHz Analog Out (±50 kHz)		−91		dBc	
80 MHz Analog Out (±1 MHz)		−85		dBc	
80 MHz Analog Out (±250 kHz)		−87		dBc	
80 MHz Analog Out (±50 kHz)		−89		dBc	
120 MHz Analog Out (±1 MHz)		−83		dBc	
120 MHz Analog Out (±250 kHz)		−85		dBc	
120 MHz Analog Out (±50 kHz)		−87		dBc	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
160 MHz Analog Out (±1 MHz)		−81		dBc	
160 MHz Analog Out (±250 kHz)		−83		dBc	
160 MHz Analog Out (±50 kHz)		−85		dBc	
DAC Residual Phase Noise					
19.7 MHz F_{OUT}					
@ 10 Hz Offset		125		dBc/Hz	
@ 100 Hz Offset		135		dBc/Hz	
@ 1 kHz Offset		143		dBc/Hz	
@ 10 kHz Offset		152		dBc/Hz	
@ 100 kHz Offset		158		dBc/Hz	
>1 MHz Offset		163		dBc/Hz	
51.84 MHz F_{OUT}					
@ 10 Hz Offset		119		dBc/Hz	
@ 100 Hz Offset		125		dBc/Hz	
@ 1 kHz Offset		132		dBc/Hz	
@ 10 kHz Offset		142		dBc/Hz	
@ 100 kHz Offset		150		dBc/Hz	
>1 MHz Offset		155		dBc/Hz	
105.3 MHz Analog Out					
@ 10 Hz Offset		105		dBc/Hz	
@ 100 Hz Offset		115		dBc/Hz	
@ 1 kHz Offset		122		dBc/Hz	
@ 10 kHz Offset		131		dBc/Hz	
@ 100 kHz Offset		139		dBc/Hz	
>1 MHz Offset		142		dBc/Hz	
155.52 MHz Analog Out					
@ 10 Hz Offset		105		dBc/Hz	
@ 100 Hz Offset		110		dBc/Hz	
@ 1 kHz Offset		119		dBc/Hz	
@ 10 kHz Offset		127		dBc/Hz	
@ 100 kHz Offset		135		dBc/Hz	
>1 MHz Offset		142		dBc/Hz	
CRYSTAL OSCILLATOR (ON PLLREF INPUT)					
Operating Range	20	25	30	MHz	
Residual Phase Noise (@ 25 MHz)					
@ 10 Hz Offset		95		dBc/Hz	
@ 100 Hz Offset		120		dBc/Hz	
@ 1 kHz Offset		137		dBc/Hz	
@ 10 kHz Offset		156		dBc/Hz	
@ 100 kHz Offset		164		dBc/Hz	
>1 MHz Offset		170		dBc/Hz	
DIGITAL TIMING SPECIFICATIONS					
$\overline{CS}$ to SCLK Setup Time TPRE	6			ns	
Period of SCLK (Write Speed) TSCLKW	40			ns	
Period of SCLK (Read Speed) TSCLKR		400		ns	
Serial Data Setup Time TDSU	6.5			ns	
Serial Data Hold Time TDHLD	0			ns	
TDV Data Valid Time TDV	40			ns	
I/O Update to SYNC_CLK Setup Time TUD	7			ns	
PS<2:0> to SYNC_CLK Setup Time TPS	7			ns	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Latencies/Pipeline Delays[7]					
I/O Update to DAC Frequency Change		33		SYSCLK Cycles	
I/O Update to DAC Phase Change		33		SYSCLK Cycles	
PS<2:0> to DAC Frequency Change		29		SYSCLK Cycles	
PS<2:0> to DAC Phase Change		29		SYSCLK Cycles	
I/O Update to CP_OUT Scaler Change		4		SYSCLK Cycles	
I/O Update to Frequency Accumulator Step Size Change		4		SYSCLK Cycles	
I/O Update to Frequency Accumulator Ramp Rate Change		4		SYSCLK Cycles	
RF DIVIDER/CML DRIVER EQUIVALENT INTRINSIC TIME JITTER					
F_{IN} = 414.72 MHz, F_{OUT} = 51.84 MHz					
BW = 12 kHz –> 400 kHz		136		f_S rms	OC1, RF Divider R = 8
F_{IN} = 1244.16 MHz, F_{OUT} = 155.52 MHz					
BW = 12 kHz –> 1.3 MHz		101		f_S rms	OC3, RF Divider R = 8
F_{IN} = 2488.32 MHz, F_{OUT} = 622.08 MHz					
BW = 12 kHz –> 5 MHz		108		f_S rms	OC12, RF Divider R = 4
RF DIVIDER/CML DRIVER RESIDUAL PHASE NOISE					
F_{IN} = 157.6 MHz, F_{OUT} = 19.7 MHz					RF Divider R = 8
@ 10 Hz		–115		dBc/Hz	
@ 100 Hz		–126		dBc/Hz	
@ 1 kHz		–134		dBc/Hz	
@ 10 kHz		–143		dBc/Hz	
@ 100 kHz		–150		dBc/Hz	
> 1 MHz		–151		dBc/Hz	
F_{IN} = 1240 MHz, F_{OUT} = 155 MHz					RF Divider R = 8
@ 10 Hz		–111		dBc/Hz	
@ 100 Hz		–122		dBc/Hz	
@ 1 kHz		–129		dBc/Hz	
@ 10 kHz		–138		dBc/Hz	
@ 100 kHz		–146		dBc/Hz	
@ 1 MHz		–150		dBc/Hz	
>3 MHz		–153		dBc/Hz	
F_{IN} = 2488MHz, F_{OUT} = 622 MHz					RF Divider R = 4
@ 10 Hz		–97		dBc/Hz	
@ 100 Hz		–110		dBc/Hz	
@ 1 kHz		–120		dBc/Hz	
@ 10 kHz		–126		dBc/Hz	
@ 100 kHz		–136		dBc/Hz	
@ 1 MHz		–141		dBc/Hz	
>3 MHz		–144		dBc/Hz	
TOTAL SYSTEM TIME JITTER FOR 622 MHz CLOCK					See the Loop Measurement Conditions section
12 kHz to 5 MHz Bandwidth		0.7		ps rms	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TOTAL SYSTEM JITTER AND PHASE NOISE FOR 105.33 MHz ADC CLOCK GENERATION CIRCUIT					See the Loop Measurement Conditions section
Converter Limiting Jitter		0.53		ps rms	
Resultant SNR		67		dB	
Phase Noise of Fundamental					
@ 10 Hz Offset		−75		dBc/Hz	
@ 100 Hz Offset		−87		dBc/Hz	
@ 1 kHz Offset		−93		dBc/Hz	
@ 10 kHz Offset		−105		dBc/Hz	
@ 100 kHz Offset		−145		dBc/Hz	
@ ≥1 MHz Offset		−152		dBc/Hz	

[1] The input impedance of the REFCLK input is 1500 Ω. However, in order to provide matching on the clock line, an external 50 Ω load is used.
[2] Driving the PLLREF input buffer, the crystal oscillator section of this input stage performs up to only 30 MHz.
[3] The charge pump output compliance range is functionally 0.2 V to (CP_VDD − 0.2 V). The value listed here is the compliance range for 5% matching.
[4] Measured as peak-to-peak from DRV to $\overline{\text{DRV}}$.
[5] For a 4.02 kΩ resistor from DRV_RSET to GND.
[6] Assumes a 1 mA load.
[7] I/O_UPDATE/PS<2:0> are detected by the AD9956 synchronous to the rising edge of SYNC_CLK. Each latency measurement is from the first SYNC_CLK rising edge after the I/O_UPDATE/PS<2:0> state change.

LOOP MEASUREMENT CONDITIONS

622 MHz OC-12 Clock

VCO = Sirenza 190-640T

Reference = Wenzel 500-10116 (30.3 MHz)

Loop Filter = 10 kHz BW, 60° Phase Margin

C1 = 170 nF, R1 = 14.4 Ω, C2 = 5.11 µF, R2 = 89.3 Ω, C3 Omitted

CP_OUT = 4 mA (Scaler = ×8)

÷R = 2, ÷M = 1, ÷N = 1

105 MHz Converter Clock

VCO = Sirenza 190-845T

Reference = Wenzel 500-10116 (30.3 MHz)

Loop Filter = 10 kHz BW, 45° Phase Margin

C1 = 117 nF, R1 = 28 Ω, C2 = 1.6 µF, R2 = 57.1 Ω, C3 = 53.4 nF

CP_OUT = 4 mA (Scaler = ×8)

÷R = 8, ÷M = 1, ÷N = 1

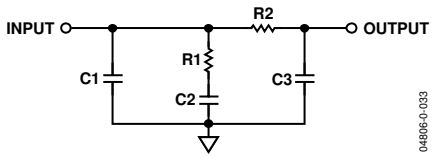


Figure 2. Generic Loop Filter

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Analog Supply Voltage (AVDD)	2 V
Digital Supply Voltage (DVDD)	2 V
Digital I/O Supply Voltage (DVDD_I/0)	3.6 V
Charge Pump Supply Voltage (CPVDD)	3.6 V
Maximum Digital Input Voltage	−0.5 V to DVDD_I/O + 0.5 V
Storage Temperature	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C
Thermal Resistance (θ_{JA})	26°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

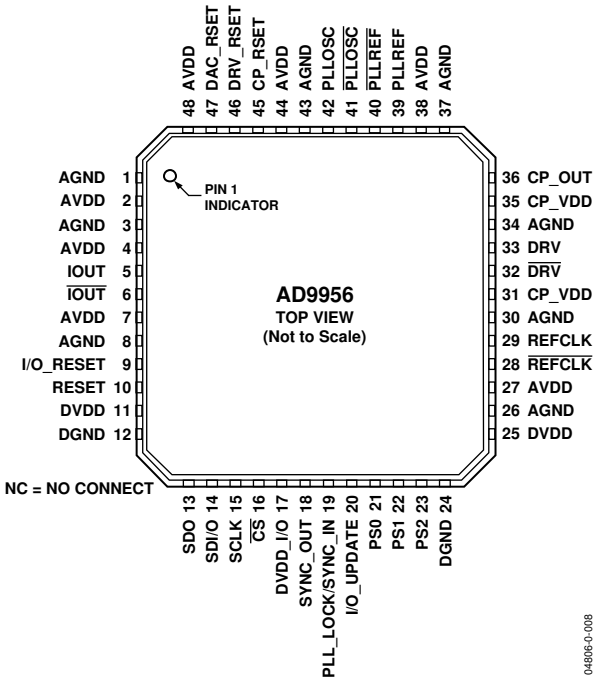


Figure 3. 48-Lead LFCSP Pin Configuration

Note that the exposed paddle on this package is an electrical connection (Pin 49) as well as a thermal enhancement. For the device to function properly, the paddle MUST be attached to analog ground.

Table 3. 48-Lead LFCSP Pin Function Description

Pin No.	Mnemonic	Description
1, 3, 8, 26, 30, 34, 37, 43, 49	AGND	Analog Ground.
2, 4, 7, 27, 38, 44, 48	AVDD	Analog Core Supply (1.8 V).
5	IOUT	DAC Analog Output.
6	$\overline{\text{IOUT}}$	DAC Analog Complementary Output.
9	I/O_RESET	Resets the serial port when synchronization is lost in communications but does not reset the device itself (ACTIVE HIGH). When not being used, this pin should be forced low, because it floats to the threshold value.
10	RESET	Master RESET. Clears all accumulators and returns all registers to their default values (ACTIVE HIGH).
11, 25	DVDD	Digital Core Supply (1.8 V).
12, 24	DGND	Digital Ground.
13	SDO	Serial Data Output. Used only when device is programmed for 3-wire serial data mode.
14	SDI/O	Serial Data I/O. When the part is programmed for 3-wire serial data mode, this is input only; in 2-wire mode, it serves as both the input and output.
15	SCLK	Serial Data Clock. Provides the clock signal for the serial data port.
16	$\overline{\text{CS}}$	Active Low Signal That Enables Shared Serial Busses. When brought high, the serial port ignores the serial data clocks.
17	DVDD_I/O	Digital Interface Supply (3.3 V).
18	SYNC_OUT	Synchronization Clock Output.
19	PLL_LOCK/SYNC_IN	Bidirectional Dual Function Pin. Depending on device programming, it is either the DDS' synchronization input (allows alignment of multiple subclocks) or the PLL lock detect output signal.
20	I/O_UPDATE	This input pin, when set high, transfers the data from the I/O buffers to the internal registers on the rising edge of the internal SYNC_CLK, which can be observed on SYNC_OUT.
21 to 23	PS0 to PS2	Profile Select Pins. Specify one of eight frequency tuning word/phase offset word profiles. In linear sweep mode, PS0 determines the state of the sweep. In linear sweep no dwell mode, PS0 is a trigger that initiates the sweep. PS1 and PS2 have no function during linear sweep mode or linear sweep no dwell mode.
28	$\overline{\text{REFCLK}}$	RF Divider and DDS REFCLK Complementary Input.
29	REFCLK	RF Divider and DDS REFCLK Input.
32	$\overline{\text{DRV}}$	CML Driver Complementary Output.
33	DRV	CML Driver Output.
31, 35	CP_VDD	Charge Pump Supply Pin (3.3 V). To minimize noise on the charge pump, isolate this supply from DVDD_I/O.
36	CP_OUT	Charge Pump Output.
39	PLLREF	Phase Frequency Detector Reference Input.
40	$\overline{\text{PLLREF}}$	Phase Frequency Detector Reference Complementary Input.
41	$\overline{\text{PLLOSC}}$	Phase Frequency Detector Oscillator (Feedback) Complementary Input.
42	PLLOSC	Phase Frequency Detector Oscillator (Feedback) Input.
45	CP_RSET	Charge Pump Current Set (Program Charge Pump Current with a Resistor to AGND).
46	DRV_RSET	CML Driver Output Current Set (Program CML Output Current with a Resistor to AGND).
47	DAC_RSET	DAC Output Current Set (Program DAC Output Current with a Resistor to AGND).

Note that the exposed paddle on this package is an electrical connection (Pin 49) as well as a thermal enhancement. In order for the device to function properly, the paddle MUST be attached to analog ground.

TYPICAL PERFORMANCE CHARACTERISTICS

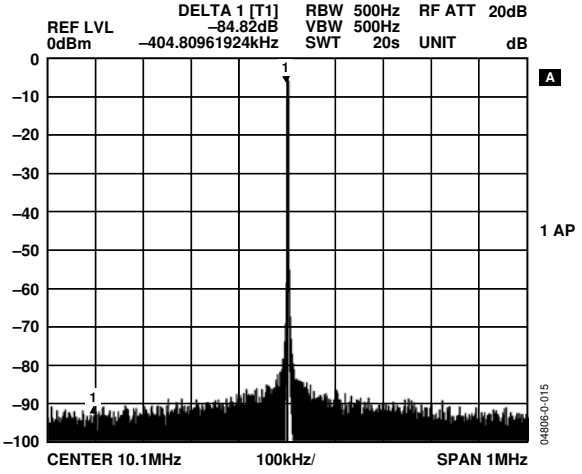


Figure 4. AD9956 DAC Performance: 400 MSPS Clock, 10 MHz F_{OUT}, 1 MHz Span

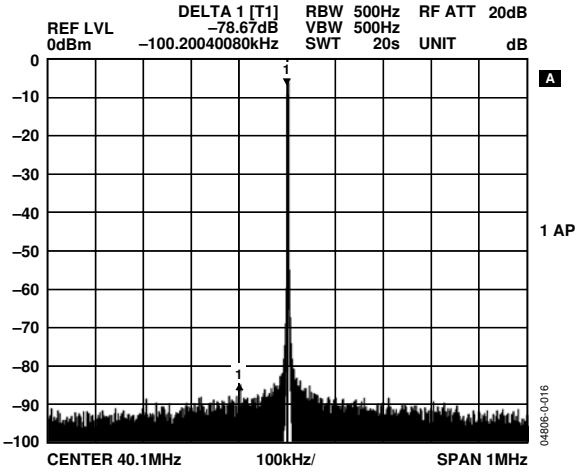


Figure 5. AD9956 DAC Performance: 400 MSPS Clock, 40 MHz F_{OUT}, 1 MHz Span

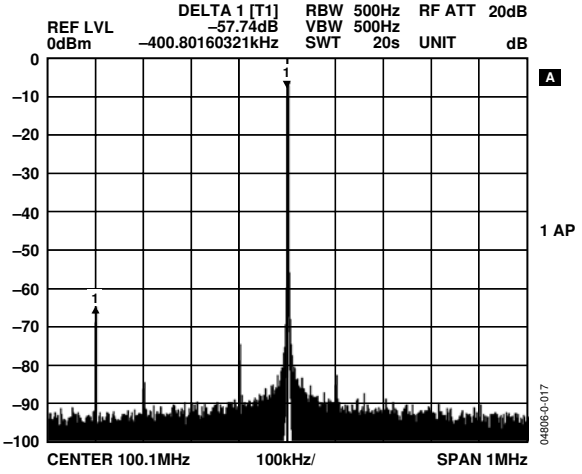


Figure 6. AD9956 DAC Performance: 400 MSPS Clock, 100 MHz F_{OUT}, 1 MHz Span

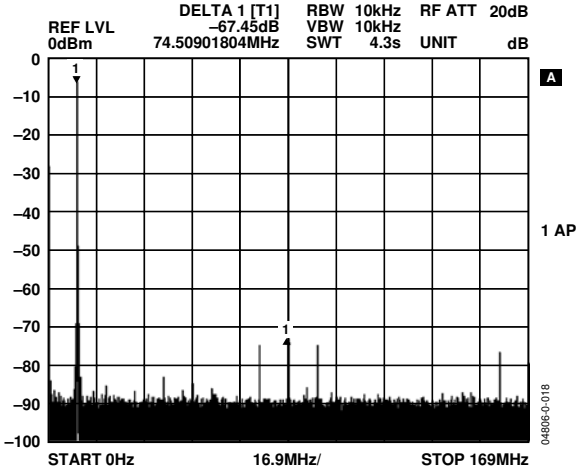


Figure 7. AD9956 DAC Performance: 400 MSPS Clock, 10 MHz F_{OUT}, 200 MHz Span

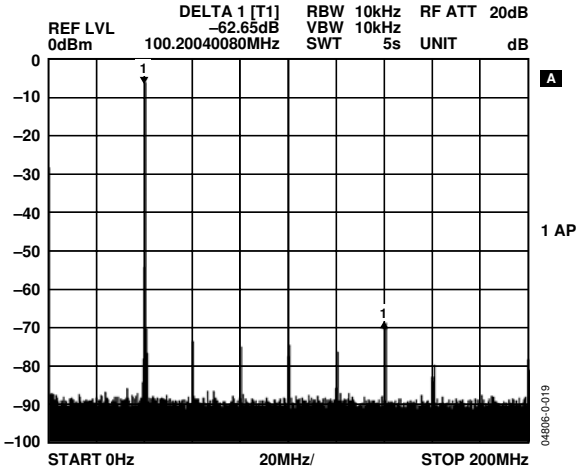


Figure 8. AD9956 DAC Performance: 400 MSPS Clock, 40 MHz F_{OUT}, 200 MHz Span

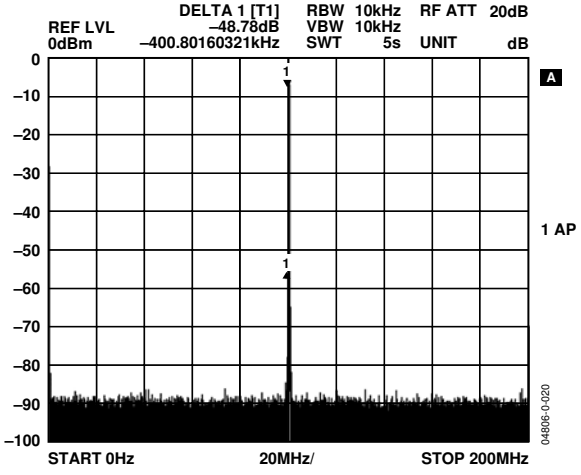


Figure 9. AD9956 DAC Performance: 400 MSPS Clock, 100 MHz F_{OUT}, 200 MHz Span

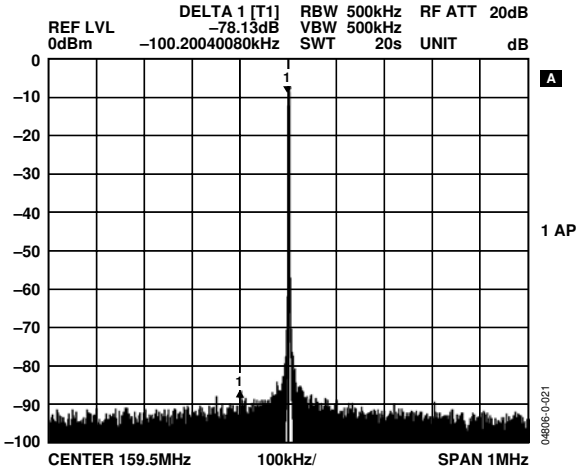


Figure 10. AD9956 DAC Performance: 400 MSPS Clock, 160 MHz F_{OUT}, 1 MHz Span

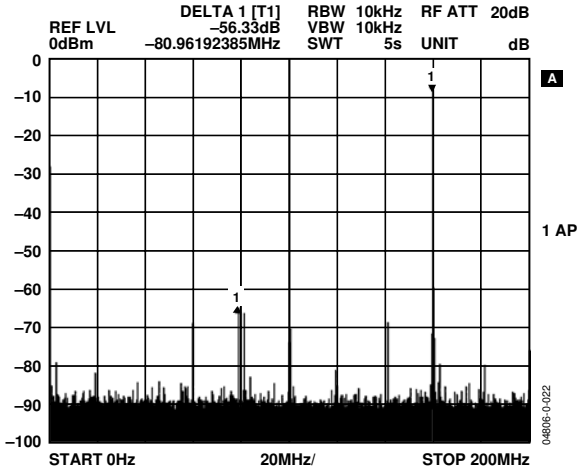


Figure 13. AD9956 DAC Performance: 400 MSPS Clock, 160 MHz F_{OUT}, 200 MHz Span

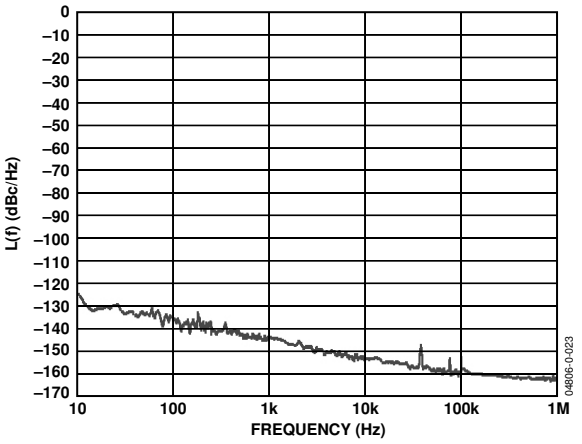


Figure 11. AD9956 DDS/DAC Residual Phase Noise 400 MHz Clock, 10 MHz Output

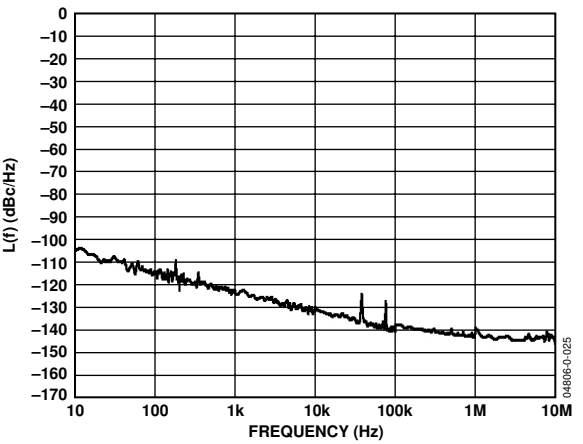


Figure 14. AD9956 DDS/DAC Residual Phase Noise 400 MHz Clock, 103 MHz Output

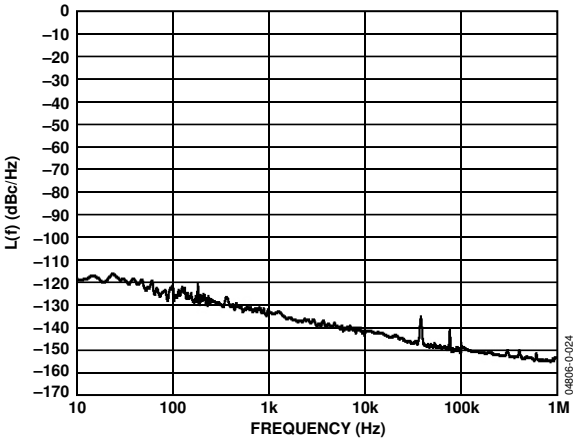


Figure 12. AD9956 DDS/DAC Residual Phase Noise 400 MHz Clock, 40 MHz Output

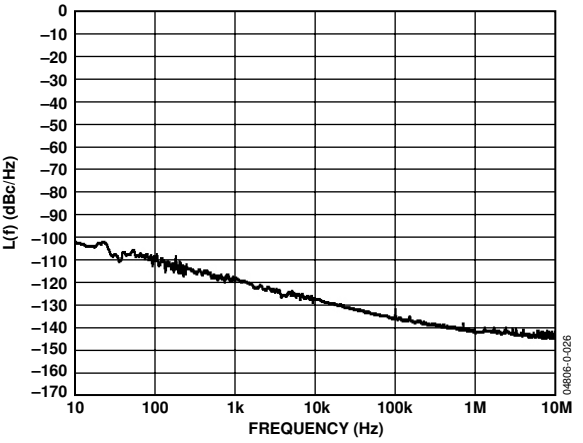


Figure 15. AD9956 DDS/DAC Residual Phase Noise 400 MHz Clock, 159 MHz Output

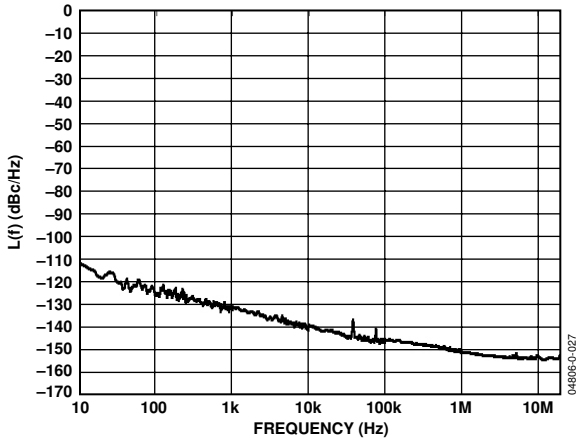


Figure 16. RF Divider and CML Driver Residual Phase Noise (840 MHz In, 105 MHz Out)

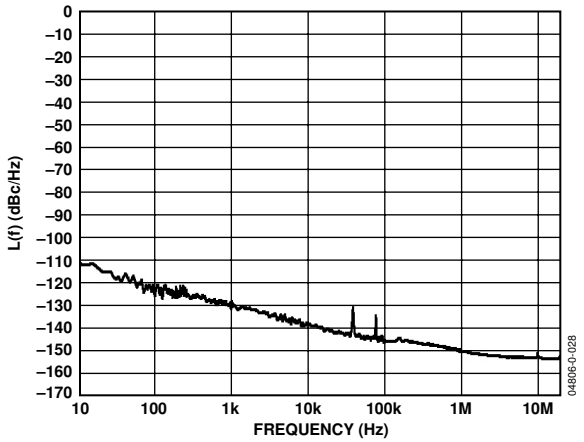


Figure 17. RF Divider and CML Driver Residual Phase Noise (1240 MHz In, 155 MHz Out)

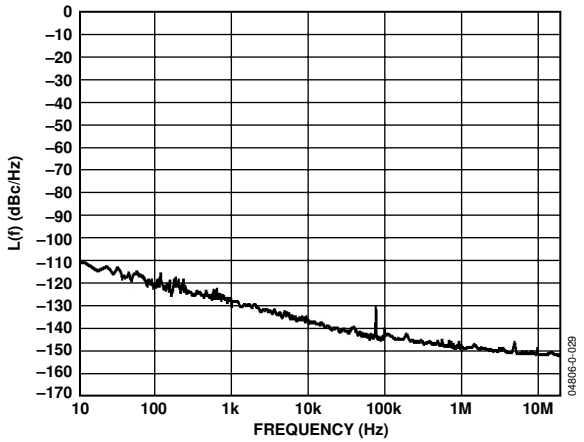


Figure 18. RF Divider and CML Driver Residual Phase Noise (1680 MHz In, 210 MHz Out)

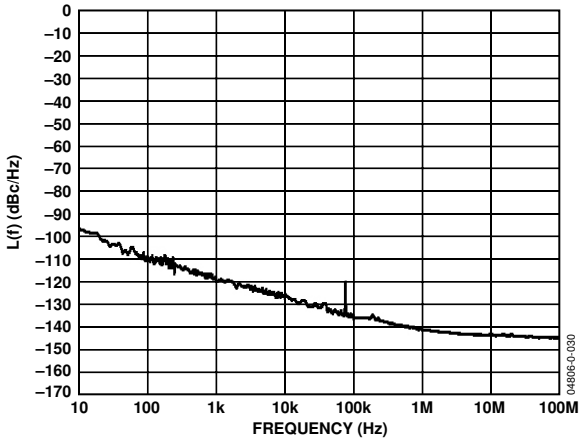


Figure 19. RF Divider and CML Driver Residual Phase Noise (2488 MHz In, 622 MHz Out)

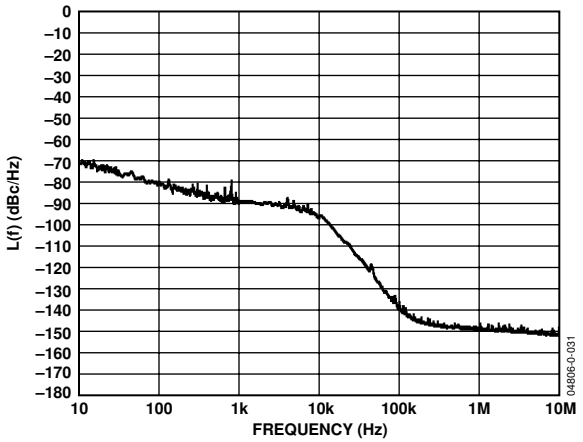


Figure 20. Total System Phase Noise for 105 MHz Converter Clock

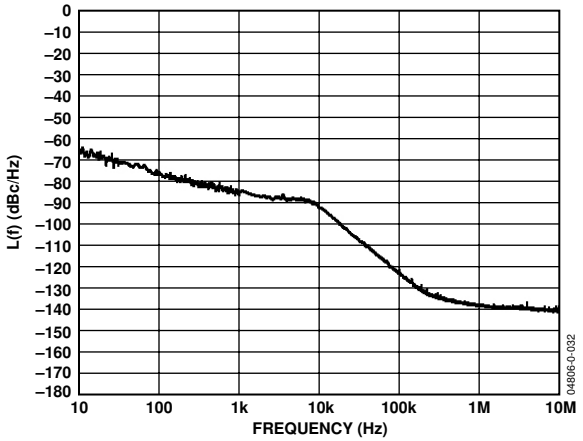


Figure 21. Total System Phase Noise for 622 MHz OC-12 Clock

TYPICAL APPLICATION CIRCUITS

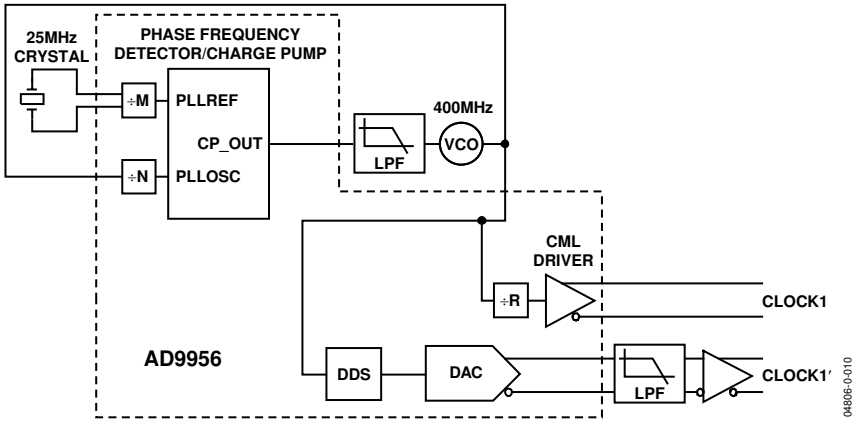


Figure 22. Dual-Clock Configuration

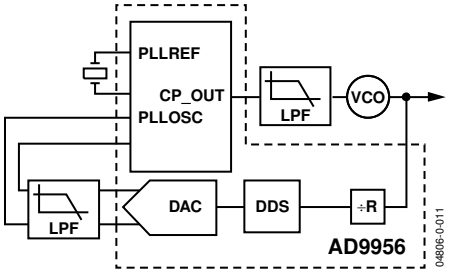


Figure 23. Fractional-Divider Loop

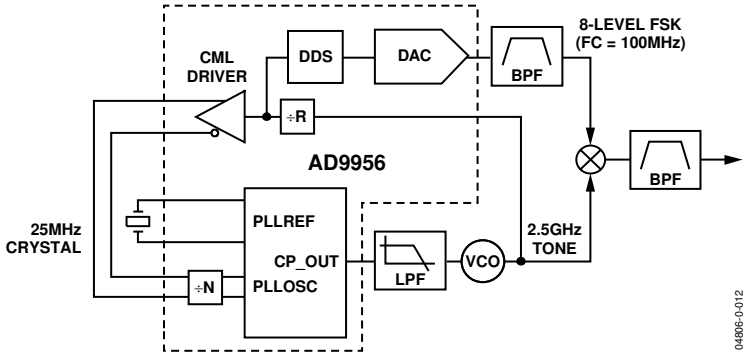


Figure 24. LO and Baseband Modulation Generation

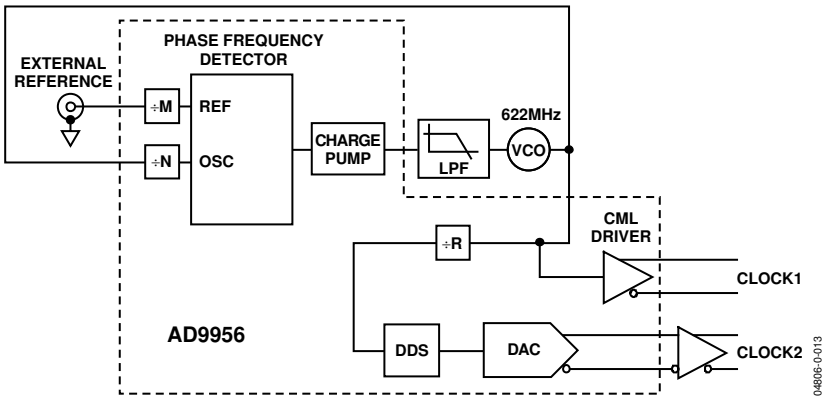


Figure 25. Optical Networking Clock

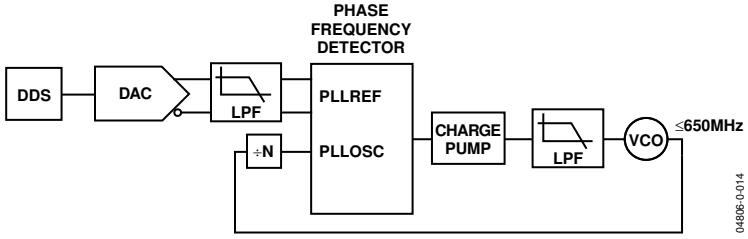


Figure 26. Direct Upconversion

APPLICATION CIRCUIT EXPLANATIONS

Dual-Clock Configuration

In this loop, M = 1, N = 16, and R = 4. The DDS tuning word is also equal to ¼ so that the frequency of CLOCK 1' equals the frequency of CLOCK 1. Phase adjustments in the DDS provide a 14-bit programmable rising edge skew capability of CLOCK 1' with respect to CLOCK 1 (see Figure 22).

Fractional-Divider Loop

This loop offers the precise frequency division (48-bit) of the DDS in the feedback path as well as the frequency sweeping capability of the DDS. Programming the DDS to sweep from 24 MHz to 25 MHz sweeps the output of the VCO from 2.7 GHz to 2.6 GHz. The reference in this case is a simple crystal (see Figure 23).

LO and Baseband Modulation Generation

Using the AD9956's PLL section to generate an LO and the DDS portion to generate a modulated baseband, this circuit uses an external mixer to perform some simple modulation at RF frequencies (see Figure 24).

Optical Networking Clock

This is the AD9956 configured as an optical networking clock. The loop can be used to generate a 622 MHz clock for OC12. The DDS can be programmed to output 8 kHz to serve as a base reference for other circuits in the subsystem (see Figure 25).

Direct Upconversion

The AD9956 is configured to use the DDS as a precision reference to the PLL loop. Since the VCO is < 655 MHz, it can be fed straight into the phase frequency detector feedback input (with the divider enabled), as seen in Figure 26.

GENERAL DESCRIPTION

DDS CORE

The DDS can create digital phase relationships by clocking a 48-bit accumulator. The incremental value loaded into the accumulator, known as the frequency tuning word, controls the overflow rate of the accumulator. Similar to a sine wave completing a 2π radian revolution, the overflow of the accumulator is cyclical in nature and generates a base frequency according to the following equation.

$$f_o = \frac{FTW \times (f_s)}{2^{48}} \qquad \{0 \le FTW \le 2^{47}\}$$

The instantaneous phase of the sine wave is, therefore, the output of the phase accumulator block. This signal can be phase-offset by programming an additive digital phase added to each and every phase sample coming out of the accumulator.

These instantaneous phase values are then piped through a phase-to-amplitude conversion (sometimes called an angle-to-amplitude conversion or AAC) block. This algorithm follows a COS(x) relationship where *x* is the phase coming out of the phase offset block, normalized to 2π.

Finally, the amplitude words are piped to a 14-bit DAC. Because the DAC is a sampled data system, the output is a reconstructed sine wave that needs to be filtered to take high frequency images out of the spectrum. The DAC is a current-steering DAC that is AVDD referenced. To get a measurable voltage output, the DAC outputs must terminate through a load resistor to AVDD, typically 50 Ω. At positive full scale, IOUT sinks no current and the voltage drop across the load resistor is zero. However, the $\overline{\text{IOUT}}$ output sinks the DAC's programmed full-scale output current, causing the maximum output voltage to drop across the load resistor. At negative full-scale, the situation is reversed and IOUT sinks the full-scale current (and generates the maximum drop across the load resistor). At the same time, $\overline{\text{IOUT}}$ sinks no current (and generates no voltage drop). At midscale, the outputs sink equal amounts of current, generating equal voltage drops.

PLL CIRCUITRY

The AD9956 includes an RF divider (divide-by-R), a phase frequency detector, and a programmable output current charge pump. Incorporating these blocks together, users can generate many useful circuits for frequency synthesis. A few simple examples are shown in the Typical Application Circuits.

The RF divider accepts differential or single-ended signals up to 2.7 GHz. The RF divider also supplies the SYSCLK input to the DDS. Because the DDS operates up to only 400 MSPS, device function requires that for any RF input signal > 400 MHz, the RF divider be engaged. The RF divider can be programmed to take values of 1, 2, 4, or 8. The ratio for the divider is programmed in the control register. The output of the divider can be routed to the input of the on-chip CML driver. For lower frequency input signals, it is possible to use the divider to divide the input signal to the CML driver and use the undivided input of the divider as the SYSCLK input to the DDS, or vice versa. In all cases, the clock to the DDS should not exceed 400 MSPS.

The on-chip phase frequency detector has two differential inputs, PLLREF (the reference input) and PLLOSC (the feedback or oscillator input). These differential inputs can be driven by single-ended signals; however, when doing so, tie the unused input through a 100 pF capacitor to the analog supply (AVDD). The maximum speed of the phase frequency detector inputs is 200 MHz. Each of the inputs has a buffer and a divider (÷M on PLLREF and ÷N on PLLOSC) that operates at up to 655 MHz. If the signal exceeds 200 MHz, however, the divider must be used. The dividers are programmed through the control registers and take any integer value between 1 and 16.

The PLLREF input also has the option of engaging an in-line oscillator circuit. Engaging this circuit means that the PLLREF input can be driven with a crystal in the of 20 MHz ≤ PLLREF ≤ 30 MHz range.

The charge pump outputs a current in response to an error signal generated in the phase frequency detector. The output current is programmed through by placing a resistor (CP_R_{SET}) from the CP_RSET pin to ground. The value is dictated by the following equation:

$$CP\_OUT = \frac{1.55}{CP\_R_{SET}}$$

This sets the charge pump's reference output current. Also, a programmable scaler multiplies this base value by any integer from 1 to 8, programmable through the CP current scale bits in the Control Function Register 2, CFR2<2:0>.

CML DRIVER

For clocking applications, an on-chip current mode logic (CML) driver is included. This CML driver generates very low jitter clock edges. The outputs of the CML driver are current outputs and drives PECL levels when terminated into a 100 Ω load. The base output current of the driver is programmed by attaching a resistor from the DRV_RSET pin to ground (nominally 4.02 kΩ for a continuous current of 7.2 mA). An optional on-chip current programming resistor is enabled by setting a bit in the control register. The rising edge and falling edge slew rates are independently programmable to help control overshoot and ringing through the application of surge current during rising edge transitions and falling edge transitions (see Figure 27). There is a default surge current of 7.6 mA on the rising edge and 4.05 mA on the falling edge. Bits in the control register enable additional rising edge and falling edge surge current, as well disable the default surge current (see the Control Function Register Descriptions section for details). The CML driver can be driven by the

- RF divider input
- RF divider output
- PLLOSC input

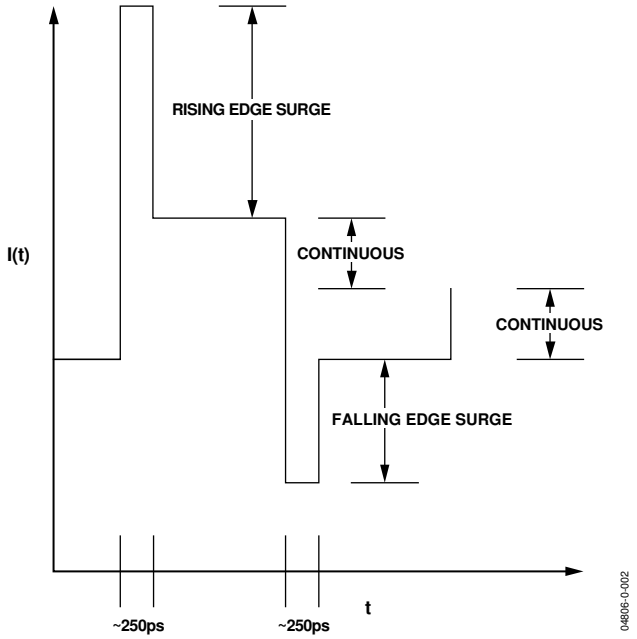


Figure 27. Rising Edge and Falling Edge Surge Current Output of the CML Clock Driver, as Opposed to the Steady State Continuous Current

MODES OF OPERATION

DDS MODES OF OPERATION

Single-Tone Mode

This is the default mode of operation for the DDS core. The phase accumulator runs at a fixed frequency, as per the active profile's tuning word. Likewise, any phase offset applied to the signal is a static value, which comes from the phase offset word of the active profile. The device has eight different phase/frequency profiles, each with its own 48-bit frequency tuning word and 14-bit phase offset word. Profiles are selected by applying their digital value on the profile-select pins (PS2, PS1, and PS0). It is impossible to use the phase offset of one profile and the frequency tuning word of another.

Linear Sweep Mode

This mode is entered by setting the linear sweep enable bit in the control register (CFR1<17> = 1) but leaving the linear sweep no dwell bit clear (CFR1<16> = 0). When the part is in linear sweep mode, the frequency accumulator ramps the output frequency of the device from a programmed lower frequency to a programmed upper frequency or from the upper frequency to the lower frequency. The lower frequency is set by the frequency tuning word stored in Profile 0, and the upper frequency is set by the frequency tuning word stored in Profile 1.

The combinational logic within the frequency accumulator requires that the value stored at FTW0 must always be less than the value stored in FTW. The direction of the sweep (sweep up to FTW1, sweep down to FTW0) is controlled by the PS0 pin. A high state on this pin tells the part to sweep up to FTW1. A low state on this pin tells the part to sweep down to FTW0. The frequency accumulator requires four values, which are stored in the register map. First, it requires an incremental frequency value that tells the frequency accumulator how big of a frequency step to take each time it takes a step when ramping up. This value is stored in the rising delta frequency tuning word (RDFTW). The second value required is the rate at which the frequency accumulator should increment, that is, how often it should take a step. This value is stored in the rising sweep ramp rate word (RSRR). The RSRR value specifies the number of SYNC_CLK cycles the frequency accumulator should count between steps. The third and fourth values are the falling ramp equivalents, the falling delta frequency tuning word (FDFTW) and the falling sweep ramp rate (FSRR).

When operating in the linear sweep default mode, combinational logic ensures that the part never ramps up past FTW1, even if the next RDFTW increments the frequency past FTW1. Once it reaches FTW1, as long as the PS0 pin stays high, the frequency remains at FTW1. Likewise, the internal logic ensures that the part never ramps down past FTW0, even if the next RDFTW increments the frequency past FTW0. During a sweep down (PS0 = 0), once the part reaches FTW0, as long as the PS0 pin stays low, the frequency remains at FTW0.

If a sweep is interrupted and the state of the PS0 pin is changed during the midst of a sweep, the part begins sweeping in the new direction at the rate dictated by the relevant delta frequency tuning word and sweep ramp rate word. For example, if the part is programmed to sweep from 100 MHz to 140 MHz and to take 1 kHz steps every 1000 sync clock cycles (rising and falling sweep words are the same), it would take four seconds to complete a sweep. If the PS0 has been low for a very long time (more than four seconds), changing the PS0 pin to high starts a sweep up to 140 MHz. If after two seconds (not enough time for a full sweep in this example) the PS0 pin is brought low again, the part begins sweeping down from the current value, roughly 120 MHz.

Linear Sweep No Dwell Mode

This mode is entered by setting the linear sweep enable bit and the linear sweep no dwell bit in the control register (CFR<17:16> =1). When the part is in linear sweep no dwell mode, the frequency accumulator ramps the output frequency of the device from a programmed lower frequency to a programmed upper frequency. Upon reaching the upper frequency, the accumulator returns to the lower frequency directly, without ramping back down. Unlike the default mode of the linear sweep, this mode uses only the rising delta frequency tuning word (RDFTW) and the rising sweep ramp rate (RSRR). The operation is still controlled by the PS0 pin. In this mode, however, it acts as a trigger for the sweep, not a direction bit. Once a PS0 low-to-high transition is detected, the part completes the entire sweep, regardless of whether or not the PS0 pin is changed back to low during the sweep. After the sweep is completed, another sweep may be initiated by applying another rising edge on the PS0 pin. This means that the PS0 pin needs to be brought low prior to the next sweep.

SYNCHRONIZATION MODES FOR MULTIPLE DEVICES

In a DDS system, the SYNC_CLK is derived internally off the master system clock, SYSCLK, with a ÷4 divider. Because the divider does not power up to a known state, it is possible for multiple devices in a system to have staggered clock-phase relationships. This is because each device could potentially generate the SYNC_CLK rising edge from any one of four rising edges of SYSCLK. This ambiguity can be resolved by employing digital synchronization logic to control the phase relationships of the derived clocks among different devices in the system. It is important to note that the synchronization functions included on the AD9956 control only the timing relationships among different digital clocks. They do not compensate for the analog timing skew on the system clock due to mismatched phase relationships on the input clock, REFCLK. Figure 28 illustrates this concept.

Automatic Synchronization

In automatic synchronization mode, the device is placed into slave mode and automatically aligns the internal SYNC_CLK to a master SYNC_CLK signal, supplied on the SYNC_IN input. When this bit is enabled, the PLL_LOCK is not available as an output, however, an out-of-lock condition can be detected by reading Control Function Register 1 and checking the status of the PLL_LOCK_ERROR bit, CFR1<24>. The automatic synchronization function is enabled by setting the Control Function Register 1 automatic synchronization bit, CFR1<3>. To employ this function at higher clock rates (SYNC_CLK > 62.5 MHz and SYSCLK > 250 MHz), the high speed sync enable bit (CFR1<0>) should be set as well.

Manual Synchronization, Hardware Controlled

In this mode, the user controls the timing relationship of the SYNC_CLK with respect to SYSCLK. When hardware manual synchronization is enabled, the PLL_LOCK/ SYNC_IN pin becomes a digital input. For each and every rising edge detected on the SYNC_IN input, the device advances the SYNC_IN rising edge by one SYSCLK period. When this bit is enabled, the PLL_LOCK is not available as an output. However, an out-of-lock condition can be detected by reading Control Function Register 1 and checking the status of the PLL Lock Error bit, CFR1<24>. This synchronization function is enabled by setting the hardware manual synchronization enable bit, CFR1<1>.

Manual Synchronization, Software Controlled

In this mode, the user controls the timing relationship between SYNC_CLK and SYSCLK through software programming. When the software manual synchronization bit (CFR1<2>) is set high, the SYNC_CLK is advanced by one SYSCLK cycle. Once this operation is complete, the bit is cleared. The user can set this bit repeatedly to advance the SYNC_CLK rising edge multiple times. Because the operation does not use the PLL_LOCK/ SYNC_IN pin as a SYNC_IN input, the PLL_LOCK signal can be monitored on the PLL_LOCK pin during this operation.

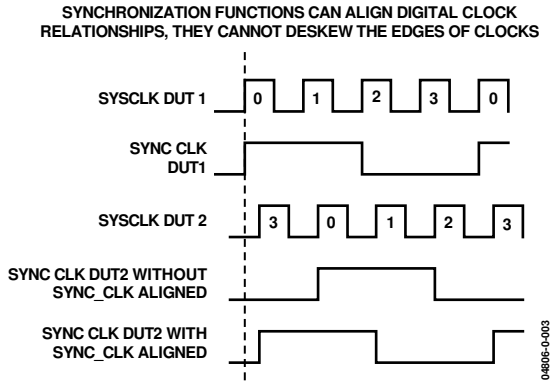


Figure 28. Synchronization Functions: Capabilities and Limitations

SERIAL PORT OPERATION

An AD9956 serial data-port communication cycle has two phases. Phase 1 is the instruction cycle, which is the writing of an instruction byte to the AD9956, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9956 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write and the serial address of the register being accessed.

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9956. The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9956 and the system controller. The number of bytes transferred during Phase 2 of the communication cycle is a function of the register being accessed. For example, when accessing Control Function Register 2, which is four bytes wide, Phase 2 requires that four bytes be transferred. If accessing a frequency tuning word, which is six bytes wide, Phase 2 requires that six bytes be transferred. After transferring all data bytes per the instruction, the communication cycle is completed.

At the completion of any communication cycle, the AD9956 serial port controller expects the next eight rising SCLK edges to be the instruction byte of the next communication cycle. All data input to the AD9956 is registered on the rising edge of SCLK. All data is driven out of the AD9956 on the falling edge of SCLK. Figure 29 through Figure 32 are useful in understanding the general operation of the AD9956 serial port.

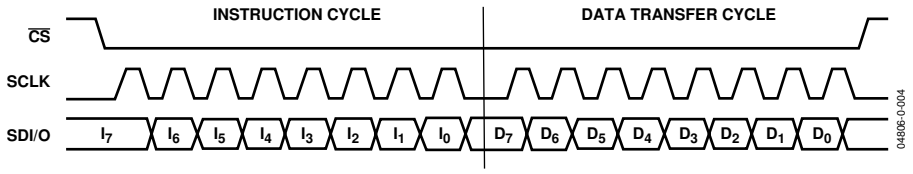


Figure 29. Serial Port Write Timing—Clock Stall Low

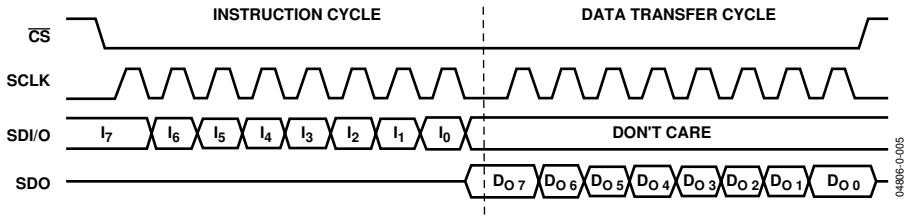


Figure 30. 3-Wire Serial Port Read Timing—Clock Stall Low

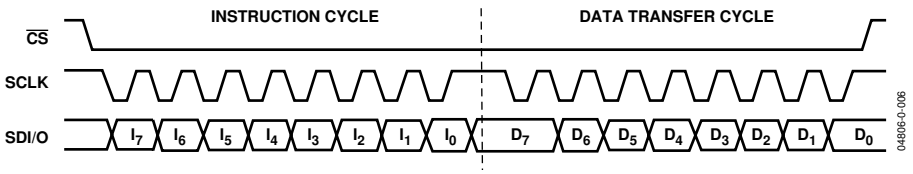


Figure 31. Serial Port Write Timing—Clock Stall High

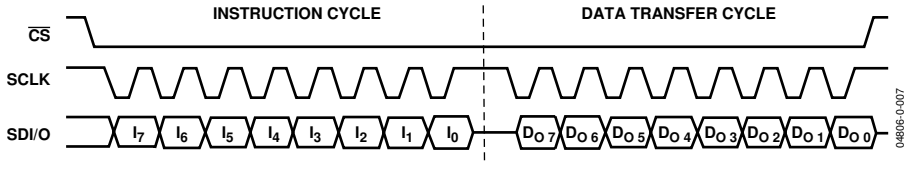


Figure 32. 2-Wire Serial Port Read Timing—Clock Stall High

INSTRUCTION BYTE

The instruction byte contains the following information:

Table 4.

D7	D6	D5	D4	D3	D2	D1	D0
R/Wb	X	X	A4	A3	A2	A1	A0

R/Wb—Bit 7 of the instruction byte determines whether a read or write data transfer occurs after the instruction byte write. Logic 1 indicates a read operation. Logic 0 indicates a write operation.

X, X—Bits 6 and 5 of the instruction byte are Don't Care.

A4 to A0—Bits 4 to 0 of the instruction byte determine which register is accessed during the data transfer portion of the communications cycle.

SERIAL INTERFACE PORT PIN DESCRIPTION

SCLK—Serial Clock. The serial clock pin is used to synchronize data to and from the AD9956 and to run the internal state machines. The SCLK maximum frequency is 25 MHz.

$\overline{CS}$—Chip Select Bar. $\overline{CS}$ is an active low input that allows more than one device on the same serial communications line. The SDO and SDI/O pins go to a high impedance state when this input is high. If driven high during any communications cycle, that cycle is suspended until $\overline{CS}$ is reactivated low. Chip select can be tied low in systems that maintain control of SCLK.

SDI/O—Serial Data Input/Output. Data is always written to the AD9956 on this pin. However, this pin can be used as a bidirectional data line. CFR1<7> controls the configuration of this pin. The default value (0) configures the SDI/O pin as bidirectional.

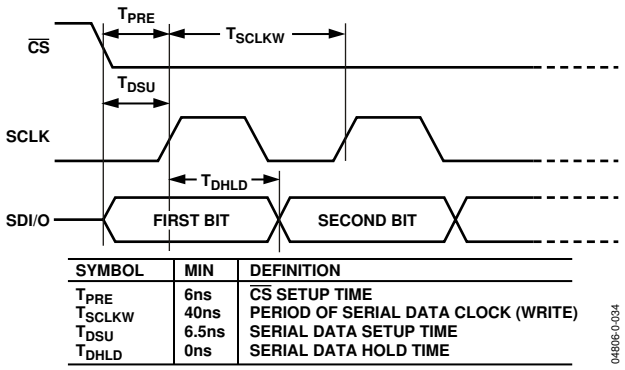
SDO—Serial Data Out. Data is read from this pin for protocols that use separate lines for transmitting and receiving data. When the AD9956 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

I/O_RESET—A high signal on this pin resets the I/O port state machines without affecting the addressable registers' contents. An active high input on the I/O_RESET pin causes the current communication cycle to abort. After I/O_RESET returns low (0), another communication cycle can begin, starting with the instruction byte write. Note that when not in use, this pin should be forced low, because it floats to the threshold value.

MSB/LSB TRANSFERS

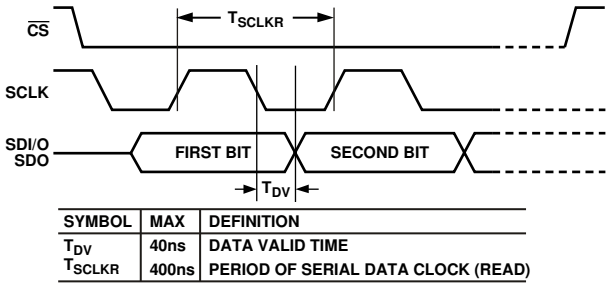
The AD9956 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by the LSB first bit in Control Register 1 (CFR1<15>). The default value of this bit is low (MSB first). When CFR1 <15> is set high, the AD9956 serial port is in LSB first format. The instruction byte must be written in the format indicated by CFR1 <15>. If the AD9956 is in LSB first mode, the instruction byte must be written from least significant bit to most significant bit. However, the instruction byte phase of the communications cycle still precedes the data transfer cycle.

For MSB first operation, all data written to (read from) the AD9956 are in MSB first order. If the LSB mode is active, all data written to (read from) the AD9956 are in LSB first order.



SYMBOL	MIN	DEFINITION
T_{PRE}	6ns	$\overline{CS}$ SETUP TIME
T_{SCLKW}	40ns	PERIOD OF SERIAL DATA CLOCK (WRITE)
T_{DSU}	6.5ns	SERIAL DATA SETUP TIME
T_{DHLD}	0ns	SERIAL DATA HOLD TIME

Figure 33. Timing Diagram for Data Write to AD9956



SYMBOL	MAX	DEFINITION
T_{DV}	40ns	DATA VALID TIME
T_{SCLKR}	400ns	PERIOD OF SERIAL DATA CLOCK (READ)

Figure 34. Timing Diagram for Data Read to AD9956