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1 GSPS Quadrature Digital Upconverter with 18-Bit I/Q Data Path and 14-Bit DAC

Data Sheet **AD9957**

FEATURES

1 GSPS internal clock speed (up to 400 MHz analog output)
Integrated 1 GSPS 14-bit DAC
250 MSPS input data rate
Phase noise ≤ −125 dBc/Hz (400 MHz carrier @ 1 kHz offset)
Excellent dynamic performance >80 dB narrow-band SFDR
8 programmable profiles for shift keying
Sin(x)/(x) correction (inverse sinc filter)
Reference clock multiplier
Internal oscillator for a single crystal operation
Software and hardware controlled power-down
Integrated RAM
Phase modulation capability
Multichip synchronization
Easy interface to Blackfin SPORT
Interpolation factors from 4× to 252×
Interpolation DAC mode
Gain control DAC
Internal divider allows references up to 2 GHz
1.8 V and 3.3 V power supplies
100-lead TQFP_EP package

APPLICATIONS

HFC data, telephony, and video modems
Wireless base station transmissions
Broadband communications transmissions
Internet telephony

GENERAL DESCRIPTION

The AD9957 functions as a universal I/Q modulator and agile upconverter for communications systems where cost, size, power consumption, and dynamic performance are critical. The AD9957 integrates a high speed, direct digital synthesizer (DDS), a high performance, high speed, 14-bit digital-to-analog converter (DAC), clock multiplier circuitry, digital filters, and other DSP functions onto a single chip. It provides baseband upconversion for data transmission in a wired or wireless communications system.

The AD9957 is the third offering in a family of quadrature digital upconverters (QDUCs) that includes the AD9857 and AD9856. It offers performance gains in operating speed, power consumption, and spectral performance. Unlike its predecessors, it supports a 16-bit serial input mode for I/Q baseband data. The device can alternatively be programmed to operate either as a single tone, sinusoidal source or as an interpolating DAC.

The reference clock input circuitry includes a crystal oscillator, a high speed, divide-by-two input, and a low noise PLL for multiplication of the reference clock frequency.

The user interface to the control functions includes a serial port easily configured to interface to the SPORT of the Blackfin® DSP and profile pins to enable fast and easy shift keying of any signal parameter (phase, frequency, or amplitude).

FUNCTIONAL BLOCK DIAGRAM

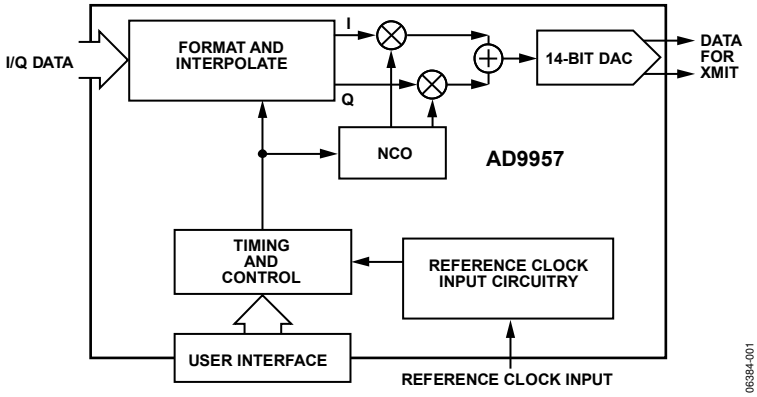

Figure 1.

Rev. D
Document Feedback

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AD9957* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD9957 Evaluation Board

DOCUMENTATION

Application Notes

- AN-0996: The Advantages of Using a Quadrature Digital Upconverter (QDUC) in Point-to-Point Microwave Transmit Systems
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-922: Digital Pulse-Shaping Filter Basics
- AN-924: Digital Quadrature Modulator Gain

Data Sheet

- AD9957: 1 GSPS Quadrature Digital Upconverter with 18-Bit IQ Data Path and 14-Bit DAC Data Sheet

User Guides

- UG-208: Evaluation Board User Guide for AD9957

TOOLS AND SIMULATIONS

- AD9957 IBIS Model

REFERENCE MATERIALS

Technical Articles

- Improved DDS Devices Enable Advanced Comm Systems

DESIGN RESOURCES

- AD9957 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD9957 EngineerZone Discussions.

SAMPLE AND BUY

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TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

AVDD (1.8V) and DVDD (1.8V) = 1.8 V ± 5%, AVDD (3.3V) = 3.3 V ± 5%, DVDD_I/O (3.3V) = 3.3 V ± 5%, T = 25°C, R_{SET} = 10 kΩ, I_{OUT} = 20 mA, external reference clock frequency = 1000 MHz with REFCLK multiplier disabled, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REF_CLK INPUT CHARACTERISTICS					
Frequency Range					
REFCLK Multiplier	Disabled	60		1000[1]	MHz
	Enabled	3.2		60	MHz
Maximum REFCLK Input Divider Frequency	Full temperature range	1500	1900		MHz
Minimum REFCLK Input Divider Frequency	Full temperature range		25	35	MHz
External Crystal			25		MHz
Input Capacitance			3		pF
Input Impedance (Differential)			2.8		kΩ
Input Impedance (Single-Ended)			1.4		kΩ
Duty Cycle	REFCLK multiplier disabled	45		55	%
	REFCLK multiplier enabled	40		60	%
REF_CLK Input Level	Single-ended	50		1000	mV p-p
	Differential	100		2000	mV p-p
REFCLK MULTIPLIER VCO GAIN CHARACTERISTICS					
VCO Gain (K_V) @ Center Frequency	VCO0 range setting		429		MHz/V
	VCO1 range setting		500		MHz/V
	VCO2 range setting		555		MHz/V
	VCO3 range setting		750		MHz/V
	VCO4 range setting		789		MHz/V
	VCO5 range setting[2]		850		MHz/V
REFCLK_OUT CHARACTERISTICS					
Maximum Capacitive Load			20		pF
Maximum Frequency			25		MHz
DAC OUTPUT CHARACTERISTICS					
Full-Scale Output Current		8.6	20	31.6	mA
Gain Error		−10		+10	%FS
Output Offset				2.3	µA
Differential Nonlinearity			0.8		LSB
Integral Nonlinearity			1.5		LSB
Output Capacitance			5		pF
Residual Phase Noise	@ 1 kHz offset, 20 MHz A_{OUT}				
REFCLK Multiplier	Disabled		−152		dBc/Hz
	Enabled @ 20×		−140		dBc/Hz
	Enabled @ 100×		−140		dBc/Hz
AC Voltage Compliance Range		−0.5		+0.5	V
SPURIOUS-FREE DYNAMIC RANGE (SFDR SINGLE TONE)					
f_{OUT} = 20.1 MHz			−70		dBc
f_{OUT} = 98.6 MHz			−69		dBc
f_{OUT} = 201.1 MHz			−61		dBc
f_{OUT} = 397.8 MHz			−54		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE SPECTRAL DENSITY (NSD)					
Single Tone					
f_{OUT} = 20.1 MHz			−167		dBm/Hz
f_{OUT} = 98.6 MHz			−162		dBm/Hz
f_{OUT} = 201.1 MHz			−157		dBm/Hz
f_{OUT} = 397.8 MHz			−151		dBm/Hz
TWO-TONE INTERMODULATION DISTORTION (IMD)	I/Q rate = 62.5 MSPS; 16× interpolation				
f_{OUT} = 25 MHz			−82		dBc
f_{OUT} = 50 MHz			−78		dBc
f_{OUT} = 100 MHz			−73		dBc
MODULATOR CHARACTERISTICS					
Input Data					
Error Vector Magnitude	2.5 Msymbols/s, QPSK, 4× oversampled		0.53		%
	270.8333 ksymbols/s, GMSK, 32× oversampled		0.77		%
	2.5 Msymbols/s, 256-QAM, 4× oversampled		0.35		%
WCDMA—FDD (TM1), 3.84 MHz Bandwidth, 5 MHz Channel Spacing					
Adjacent Channel Leakage Ratio (ACLR)	IF = 143.88 MHz		−78		dBc
Carrier Feedthrough			−78		dBc
SERIAL PORT TIMING CHARACTERISTICS					
Maximum SCLK Frequency			70		Mbps
Minimum SCLK Pulse Width	Low	4			ns
	High	4			ns
Maximum SCLK Rise/Fall Time			2		ns
Minimum Data Setup Time to SCLK		5			ns
Minimum Data Hold Time to SCLK		0			ns
Maximum Data Valid Time in Read Mode				11	ns
I/O_UPDATE/PROFILE<2:0>/RT TIMING CHARACTERISTICS					
Minimum Pulse Width	High	1			SYNC_CLK cycle
Minimum Setup Time to SYNC_CLK		1.75			ns
Minimum Hold Time to SYNC_CLK		0			ns
I/Q INPUT TIMING CHARACTERISTICS					
Maximum PDCLK Frequency			250		MHz
Minimum I/Q Data Setup Time to PDCLK		1.75			ns
Minimum I/Q Data Hold Time to PDCLK		0			ns
Minimum TxEnable Setup Time to PDCLK		1.75			ns
Minimum TxEnable Hold Time to PDCLK		0			ns
MISCELLANEOUS TIMING CHARACTERISTICS					
Wake-Up Time[3]			1		
Fast Recovery Mode			8		SYSCLK cycles[4]
Full Sleep Mode				150	µs
Minimum Reset Pulse Width High			5		SYSCLK cycles[4]
DATA LATENCY (PIPELINE DELAY)					
Data Latency Single Tone Mode					
Frequency, Phase-to-DAC Output			79		SYSCLK cycles[4]

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS LOGIC INPUTS					
Voltage					
Logic 1		2.0			V
Logic 0				0.8	V
Current					
Logic 1			90	150	µA
Logic 0			90	150	µA
Input Capacitance			2		pF
XTAL_SEL INPUT					
Logic 1 Voltage		1.25			V
Logic 0 Voltage				0.6	V
Input Capacitance			2		pF
CMOS LOGIC OUTPUTS	1 mA load				
Voltage					
Logic 1		2.8			V
Logic 0				0.4	V
POWER SUPPLY CURRENT					
DVDD_I/O (3.3V) Pin Current Consumption	QDUC mode		16		mA
DVDD (1.8V) Pin Current Consumption	QDUC mode		610		mA
AVDD (3.3V) Pin Current Consumption	QDUC mode		28		mA
AVDD (1.8V) Pin Current Consumption	QDUC mode		105		mA
POWER CONSUMPTION					
Single Tone Mode			800		mW
Continuous Modulation	8× interpolation		1400	1800	mW
Inverse Sinc Filter Power Consumption			150	200	mW
Full Sleep Mode			12	40	mW

[1] The system clock is limited to 750 MHz maximum in BFI mode.
[2] The gain value for VCO range Setting 5 is measured at 1000 MHz.
[3] Wake-up time refers to the recovery from analog power-down modes. The longest time required is for the Reference Clock Multiplier PLL to relock to the reference.
[4] SYSCLK cycle refers to the actual clock frequency used on-chip by the DDS. If the reference clock multiplier is used to multiply the external reference clock frequency, the SYSCLK frequency is the external frequency multiplied by the reference clock multiplication factor. If the reference clock multiplier and divider are not used, the SYSCLK frequency is the same as the external reference clock frequency.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
AVDD (1.8V), DVDD (1.8V) Supplies	2 V
AVDD (3.3V), DVDD_I/O (3.3V) Supplies	4 V
Digital Input Voltage	−0.7 V to +4 V
XTAL_SEL	−0.7 V to +2.2 V
Digital Output Current	5 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
θ_{JA}	22°C/W
θ_{JC}	2.8°C/W
Maximum Junction Temperature	150°C
Lead Temperature, Soldering (10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

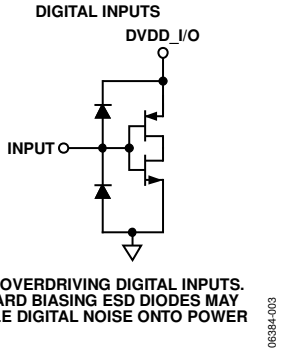

Figure 2. Equivalent Input Circuit

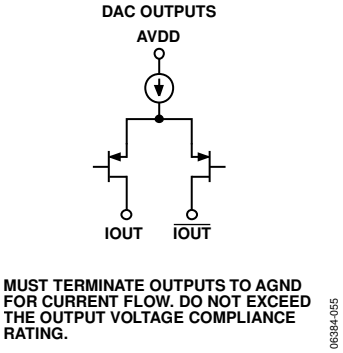

Figure 3. Equivalent Output Circuit

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

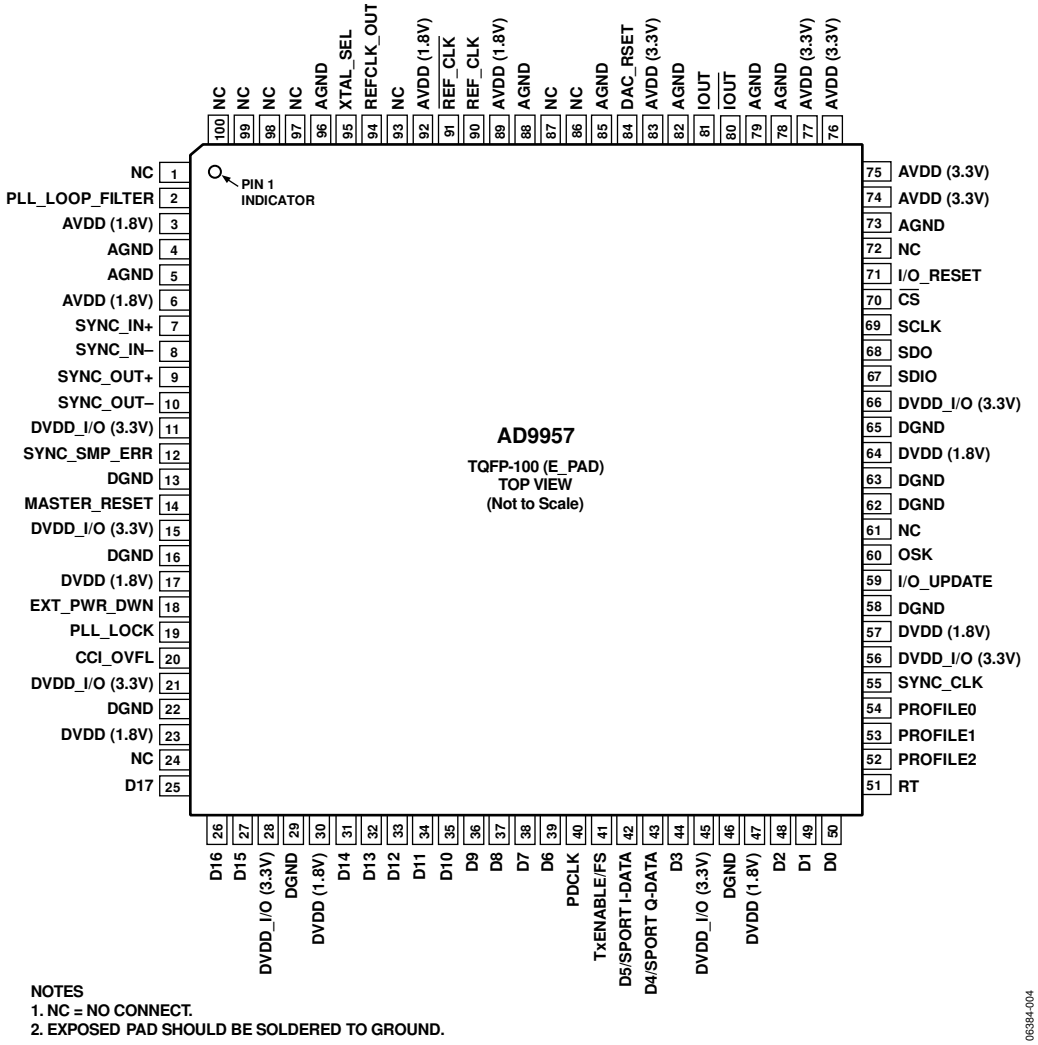

Figure 4. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	I/O[1]	Description
1, 24, 61, 72, 86, 87, 93, 97 to 100	NC		Not Connected. Allow the device pin to float.
2	PLL_LOOP_FILTER	I	PLL Loop Filter Compensation. See External PLL Loop Filter Components section.
3, 6, 89, 92	AVDD (1.8V)	I	Analog Core VDD. 1.8 V analog supplies.
74 to 77, 83	AVDD (3.3V)	I	Analog DAC VDD. 3.3 V analog supplies.
17, 23, 30, 47, 57, 64	DVDD (1.8V)	I	Digital Core VDD. 1.8 V digital supplies.
11, 15, 21, 28, 45, 56, 66	DVDD_I/O (3.3V)	I	Digital Input/Output VDD. 3.3 V digital supplies.
4, 5, 73, 78, 79, 82, 85, 88, 96	AGND	I	Analog Ground.
13, 16, 22, 29, 46, 58, 62, 63, 65	DGND	I	Digital Ground.
7	SYNC_IN+	I	Synchronization Signal, Digital Input (Rising Edge Active). Synchronization signal from external master to synchronize internal subclocks. See the Synchronization of Multiple Devices section.
8	SYNC_IN–	I	Synchronization Signal, Digital Input (Falling Edge Active). Synchronization signal from external master to synchronize internal subclocks. See the Synchronization of Multiple Devices section.
9	SYNC_OUT+	O	Synchronization Signal, Digital Output (Rising Edge Active). Synchronization signal from internal device subclocks to synchronize external slave devices. See the Synchronization of Multiple Devices section.
10	SYNC_OUT–	O	Synchronization Signal, Digital Output (Falling Edge Active). Synchronization signal from internal device subclocks to synchronize external slave devices. See the Synchronization of Multiple Devices section.
12	SYNC_SMP_ERR	O	Synchronization Sample Error, Digital Output (Active High). A high on this pin indicates that the AD9957 did not receive a valid sync signal on SYNC_IN+/SYNC_IN–. See the Synchronization of Multiple Devices section.
14	MASTER_RESET	I	Master Reset, Digital Input (Active High). This pin clears all memory elements and sets registers to default values.
18	EXT_PWR_DWN	I	External Power-Down, Digital Input (Active High). A high level on this pin initiates the currently programmed power-down mode. See the Power-Down Control section for further details. If unused, tie to ground.
19	PLL_LOCK	O	PLL Lock, Digital Output (Active High). A high on this pin indicates that the clock multiplier PLL has acquired lock to the reference clock input.
20	CCI_OVFL	O	CCI Overflow Digital Output, Active High. A high on this pin indicates a CCI filter overflow. This pin remains high until the CCI overflow condition is cleared.
25 to 27, 31 to 39, 42 to 44, 48 to 50	D<17:0>	I/O	Parallel Data Input Bus (Active High). These pins provide the interleaved, 18-bit, digital, I and Q vectors for the modulator to upconvert. Also used for a GPIO port in Blackfin interface mode.
42	SPORT I-DATA	I	I-Data Serial Input. In Blackfin interface mode, this pin serves as the I-data serial input.
43	SPORT Q-DATA	I	Q-Data Serial Input. In Blackfin interface mode, this pin serves as the Q-data serial input.
40	PDCLK	O	Parallel Data Clock, Digital Output (Clock). See the Signal Processing section for details.
41	TxENABLE/FS	I	Transmit Enable, Digital Input (Active High). See the Signal Processing section for details. In Blackfin interface mode, this pin serves as the FS input to receive the RFS output signal from the Blackfin.
51	RT	I	RAM Trigger, Digital Input (Active High). This pin provides control for the RAM amplitude scaling function. When this function is engaged, a high sweeps the amplitude from the beginning RAM address to the end. A low sweeps the amplitude from the end RAM address to the beginning. If unused, connect to ground or supply.
52 to 54	PROFILE<2:0>	I	Profile Select Pins, Digital Inputs (Active High). These pins select one of eight phase/frequency profiles for the DDS core (single tone or carrier tone). Changing the state of one of these pins transfers the current contents of all I/O buffers to the corresponding registers. Set up state changes to the SYNC_CLK pin.
55	SYNC_CLK	O	Output System Clock/4, Digital Output (Clock). Set up the I/O_UPDATE and PROFILE<2:0> pins to the rising edge of this signal.

Pin No.	Mnemonic	I/O[1]	Description
59	I/O_UPDATE	I/O	Input/Output Update; Digital Input Or Output (Active High), Depending on the Internal I/O Update Active Bit. A high on this pin indicates a transfer of the contents of the I/O buffers to the corresponding internal registers.
60	OSK	I	Output Shift Keying, Digital Input (Active High). When using OSK (manual or automatic), this pin controls the OSK function. See the Output Shift Keying (OSK) section of the data sheet for details. When not using OSK, tie this pin high.
67	SDIO	I/O	Serial Data Input/Output, Digital Input/Output (Active High). This pin can be either unidirectional or bidirectional (default), depending on configuration settings. In bidirectional serial port mode, this pin acts as the serial data input and output. In unidirectional, it is an input only.
68	SDO	O	Serial Data Output, Digital Output (Active High). This pin is only active in unidirectional serial data mode. In this mode, it functions as the output. In bidirectional mode, this pin is not operational and must be left floating.
69	SCLK	I	Serial Data Clock. Digital clock (rising edge on write, falling edge on read). This pin provides the serial data clock for the control data path. Write operations to the AD9957 use the rising edge. Readback operations from the AD9957 use the falling edge.
70	$\overline{CS}$	I	Chip Select, Digital Input (Active Low). Bringing this pin low enables the AD9957 to detect serial clock rising/falling edges. Bringing this pin high causes the AD9957 to ignore input on the serial data pins.
71	I/O_RESET	I	Input/Output Reset. Digital input (active high). This pin can be used when a serial I/O communication cycle fails (see the I/O_RESET—Input/Output Reset section for details). When not used, connect this pin to ground.
80	$\overline{IOUT}$	O	Open-Source DAC Complementary Output Source. Analog output, current mode. Connect through 50 Ω to AGND.
81	IOUT	O	Open-Source DAC Output Source. Analog output, current mode. Connect through 50 Ω to AGND.
84	DAC_RSET	O	Analog Reference Pin. This pin programs the DAC output full-scale reference current. Attach a 10 kΩ resistor to AGND.
90	REF_CLK	I	Reference Clock Input. Analog input. See the REFCLK Overview section for more details.
91	$\overline{REF\_CLK}$	I	Complementary Reference Clock Input. Analog input. See the REFCLK Overview section for more details.
94	REFCLK_OUT	O	Reference Clock Output. Analog output. See the REFCLK Overview section for more details.
95	XTAL_SEL	I	Crystal Select (1.8 V Logic). Analog input (active high). Driving the XTAL_SEL pin high enables the internal oscillator to be used with a crystal resonator. If unused, connect it to AGND.
(EPAD)	Exposed Pad (EPAD)		The EPAD should be soldered to ground.

[1] I is input, O is output.

TYPICAL PERFORMANCE CHARACTERISTICS

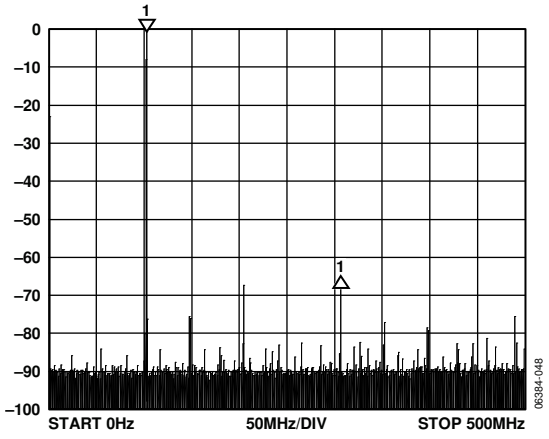

Figure 5. 15.625 kHz Quadrature Tone, Carrier = 102 MHz, CCI = 16, f_S = 1 GHz

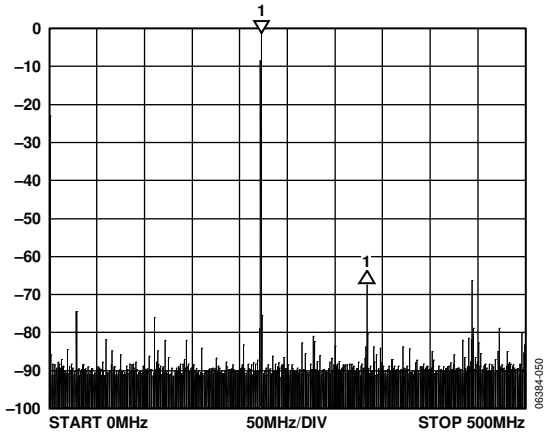

Figure 6. 15.625 kHz Quadrature Tone, Carrier = 222 MHz, CCI = 16, f_S = 1 GHz

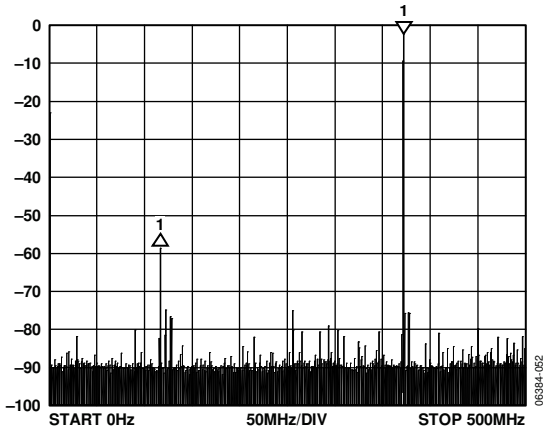

Figure 7. 15.625 kHz Quadrature Tone, Carrier = 372 MHz, CCI = 16, f_S = 1 GHz

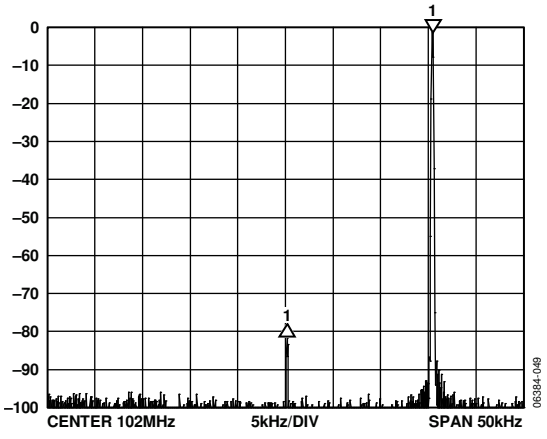

Figure 8. Narrow-Band View of Figure 5 (with Carrier and Lower Sideband Suppression)

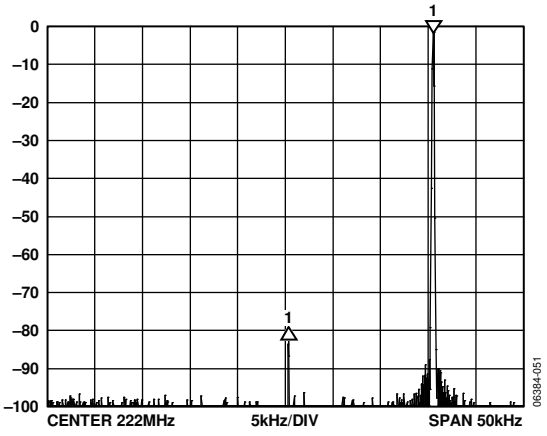

Figure 9. Narrow-Band View of Figure 6 (with Carrier And Lower Sideband Suppression)

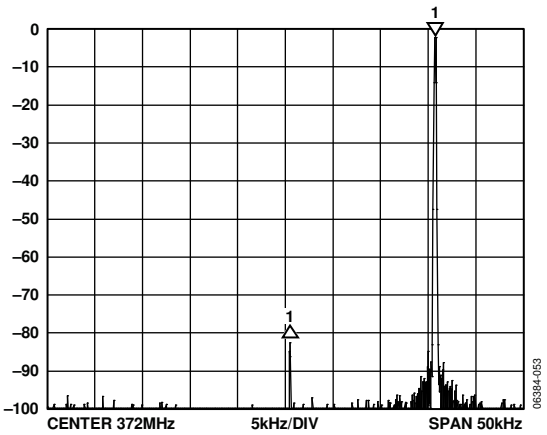

Figure 10. Narrow-Band View of Figure 7 (with Carrier and Lower Sideband Suppression)

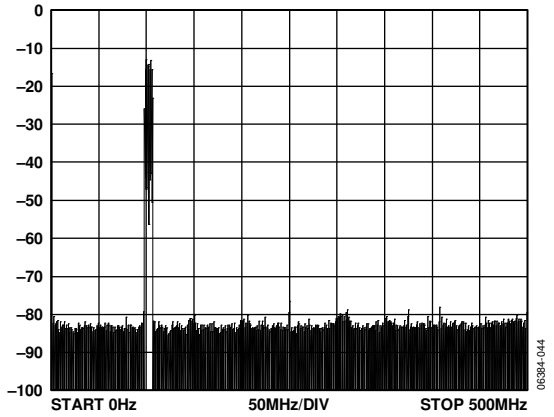

Figure 11. QPSK, 7.8125 Msymbols/s, 4x Oversampled Raised Cosine, $\alpha = 0.25$, CCI = 8, Carrier = 102 MHz, $f_S = 1$ GHz

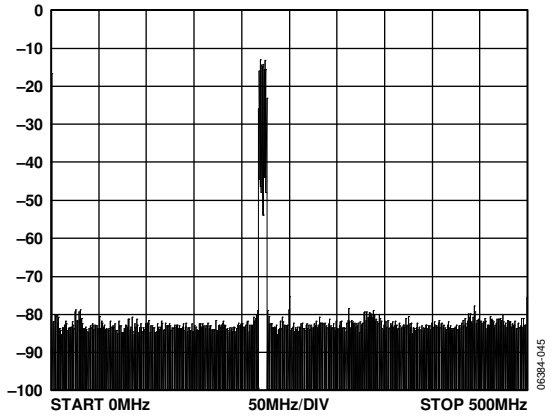

Figure 12. QPSK, 7.8125 Msymbols/s, 4x Oversampled Raised Cosine, $\alpha = 0.25$, CCI = 8, Carrier = 222 MHz, $f_S = 1$ GHz

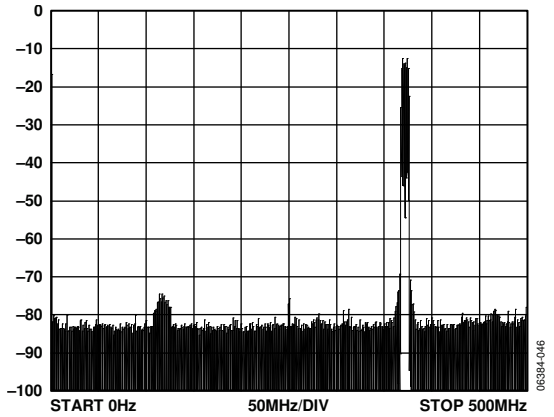

Figure 13. QPSK, 7.8125 Msymbols/s, 4x Oversampled Raised Cosine, $\alpha = 0.25$, CCI = 8, Carrier = 372 MHz, $f_S = 1$ GHz

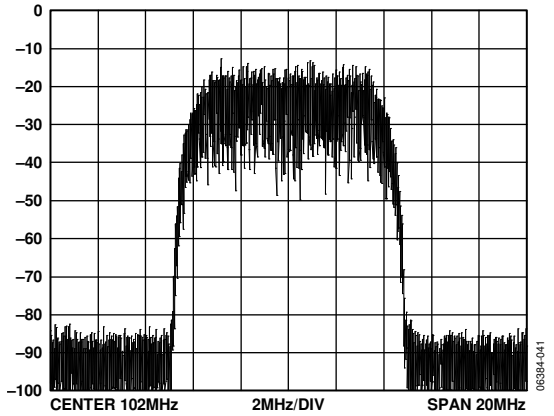

Figure 14. Narrow-Band View of Figure 11

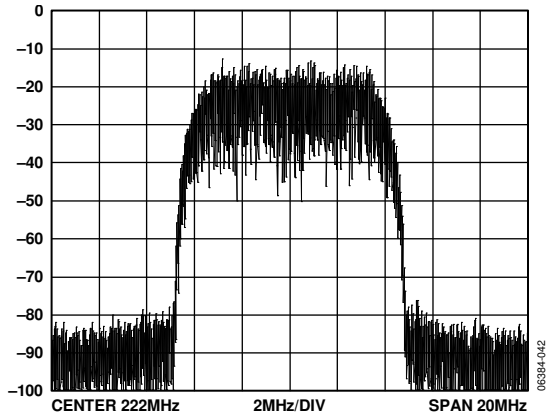

Figure 15. Narrow-Band View of Figure 12

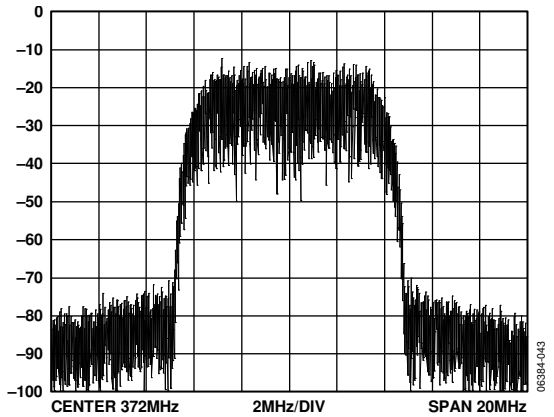

Figure 16. Narrow-Band View of Figure 13

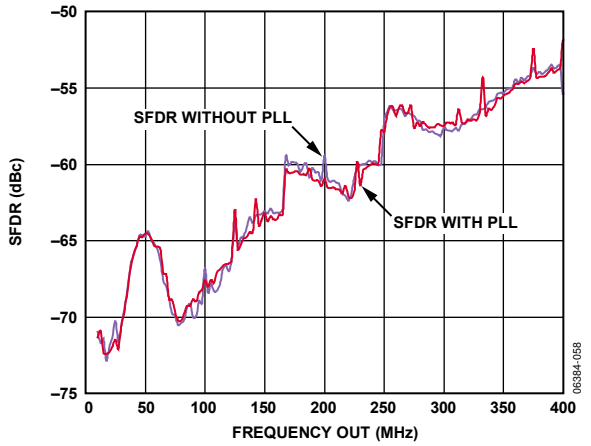

Figure 17. Wideband SFDR vs. Output Frequency in Single Tone Mode, PLL with REFCLK = 15.625 MHz × 64

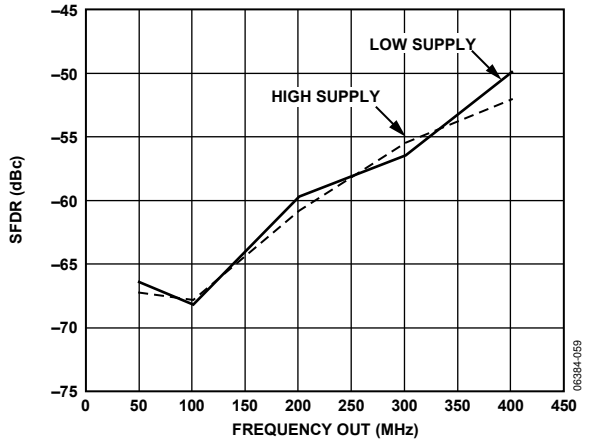

Figure 18. SFDR vs. Output Frequency and Supply (±5%) in Single Tone Mode, REFCLK = 1 GHz

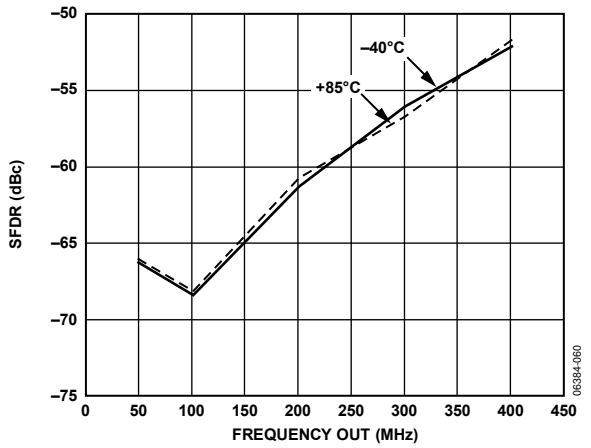

Figure 19. SFDR vs. Frequency and Temperature in Single Tone Mode, REFCLK = 1 GHz

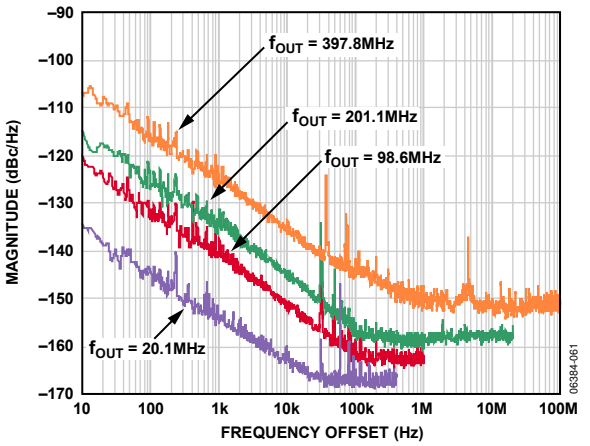

Figure 20. Residual Phase Noise, System Clock = 1 GHz

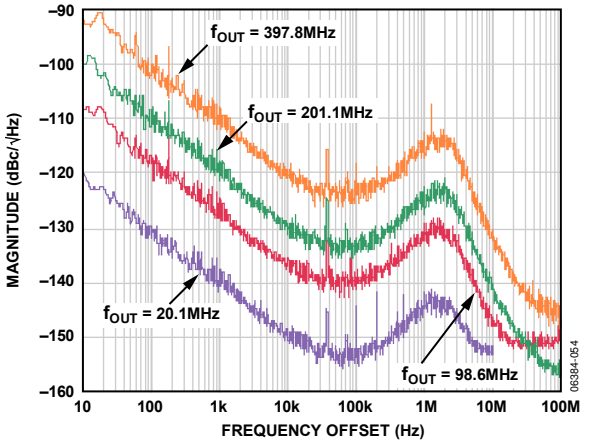

Figure 21. Residual Phase Noise Using the REFCLK Multiplier, REFCLK = 50 MHz with 20x Multiplication, System Clock = 1 GHz

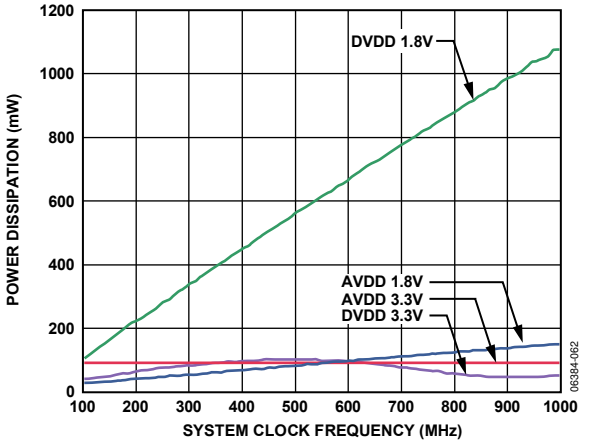

Figure 22. Power Dissipation vs. System Clock (PLL Disabled)

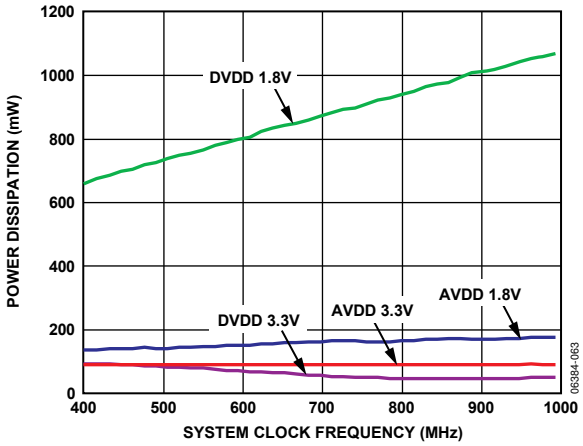

Figure 23. Power Dissipation vs. System Clock (PLL Enabled)

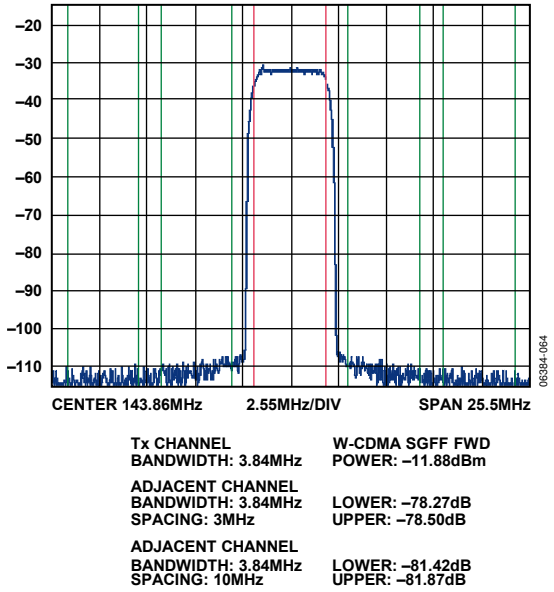

Figure 24. Typical ACLR for Wideband CDMA

MODES OF OPERATION

OVERVIEW

The AD9957 has three basic operating modes.

- Quadrature modulation (QDUC) mode (default)
- Interpolating DAC mode
- Single tone mode

The active mode is selected via the operating mode bits in Control Function Register 1 (CFR1). Single tone mode allows the device to operate as a sinusoidal generator with the DDS driving the DAC directly.

Interpolating DAC mode bypasses the DDS, allowing the user to deliver baseband data to the device at a sample rate lower than that of the DAC. An internal chain of rate interpolation filters the user data and upsamples to the DAC sample rate. Combined, the filters provide for programmable rate interpolation while suppressing spectral images and retaining the original baseband spectrum.

QDUC mode employs both the DDS and the rate interpolation filters. In this case, two parallel banks of rate interpolation filters allow baseband processing of in-phase and quadrature (I/Q) signals with the DDS providing the carrier signal to be modulated by the baseband signals. A detailed block diagram of the AD9957 is shown in Figure 25.

The inverse sinc filter is available in all three modes.

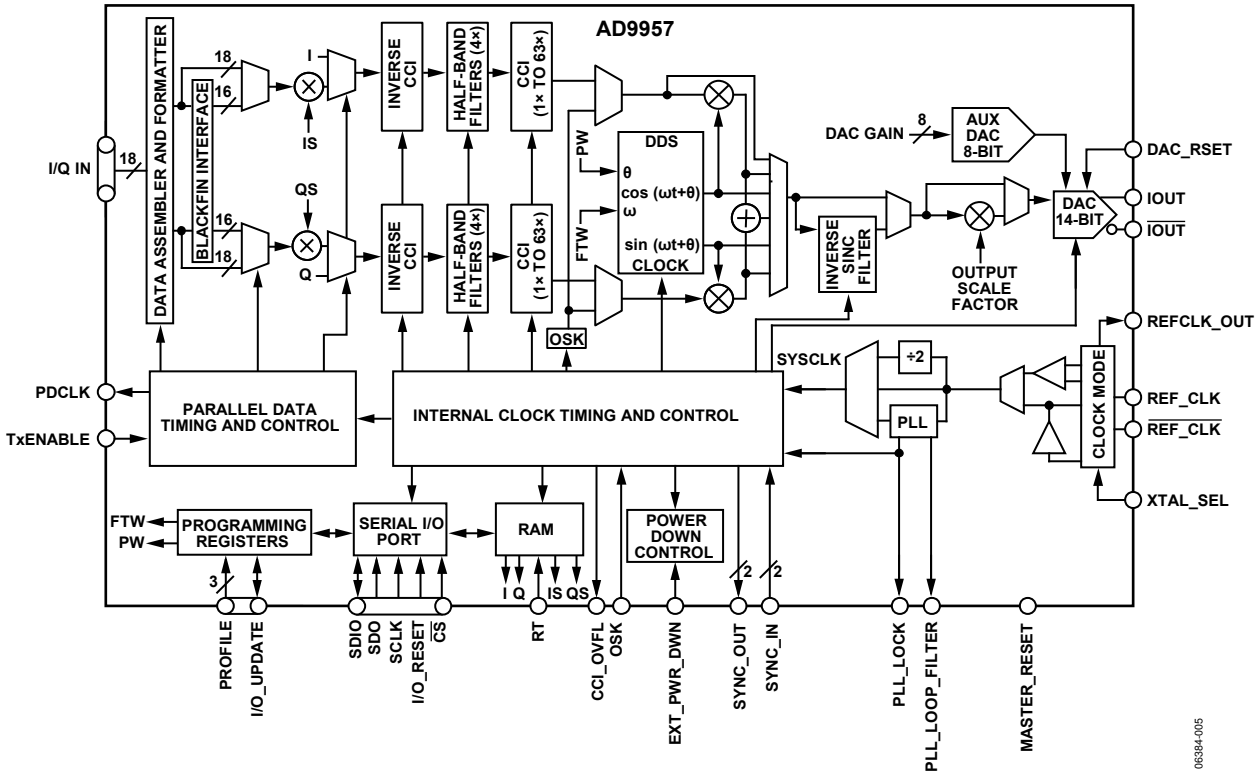

Figure 25. Detailed Block Diagram

QUADRATURE MODULATION MODE

A block diagram of the AD9957 operating in QDUC mode is shown in Figure 26; grayed items are inactive. The parallel input accepts 18-bit I- and Q-words in time-interleaved fashion. That is, an 18-bit I-word is followed by an 18-bit Q-word, then the next 18-bit I-word, and so on. One 18-bit I-word and one 18-bit Q-word together comprise one internal sample. The data assembler and formatter de-interleave the I- and Q-words so that each sample propagates along the internal data pathway in parallel fashion. Both I and Q data paths are active; the parallel data clock (PDCLK) serves to synchronize the input of I/Q data to the AD9957.

The PROFILE and I/O_UPDATE pins are also synchronous to the PDCLK.

The DDS core provides a quadrature (sine and cosine) local oscillator signal to the quadrature modulator, where the interpolated I and Q samples are multiplied by the respective phase of the carrier and summed together, producing a quadrature modulated data stream. This data stream is routed through the inverse sinc filter (optionally), and the output scaling multiplier. Then it is applied to the 14-bit DAC to produce the quadrature modulated analog output signal.

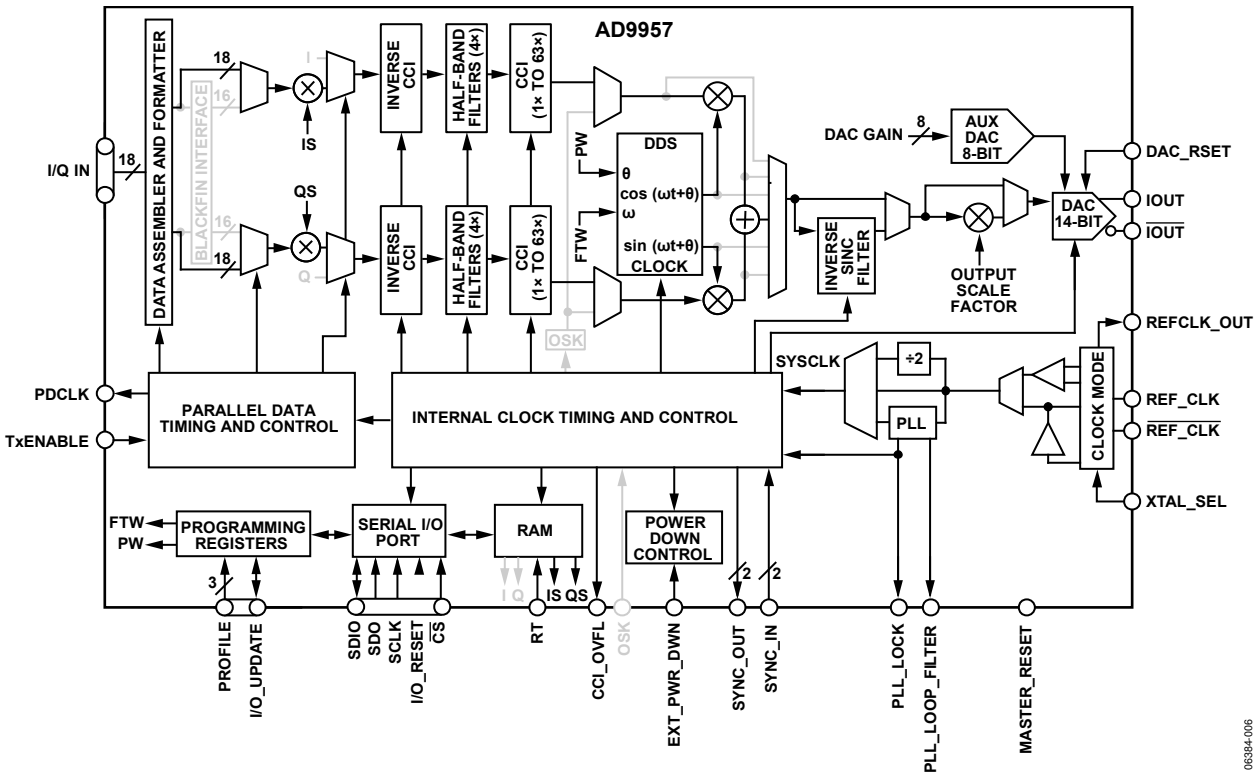

Figure 26. Quadrature Modulation Mode

BLACKFIN INTERFACE (BFI) MODE

A subset of the QDUC mode is the Blackfin interface (BFI) mode, shown in Figure 27; grayed items are inactive. In this mode, a separate I and Q serial bit stream is applied to the baseband data port instead of parallel data-words. The two serial inputs provide for 16-bit I- and Q-words (unlike the 18-bit words in normal QDUC mode). The serial bit streams are delivered to the Blackfin interface. The Blackfin interface converts the 16-bit serial data into 16-bit parallel data to propagate down the signal processing chain.

The Blackfin interface includes an additional pair of half-band filters in both I and Q signal paths (not shown explicitly in the diagram). The two half-band filters increase the interpolation of the baseband data by a factor of four, relative to the normal QDUC mode.

The synchronization of the serial data occurs through the PDCLK signal. In BFI mode, the PDCLK signal is effectively the bit clock for the serial data.

Note that the system clock is limited to 750 MHz in BFI mode.

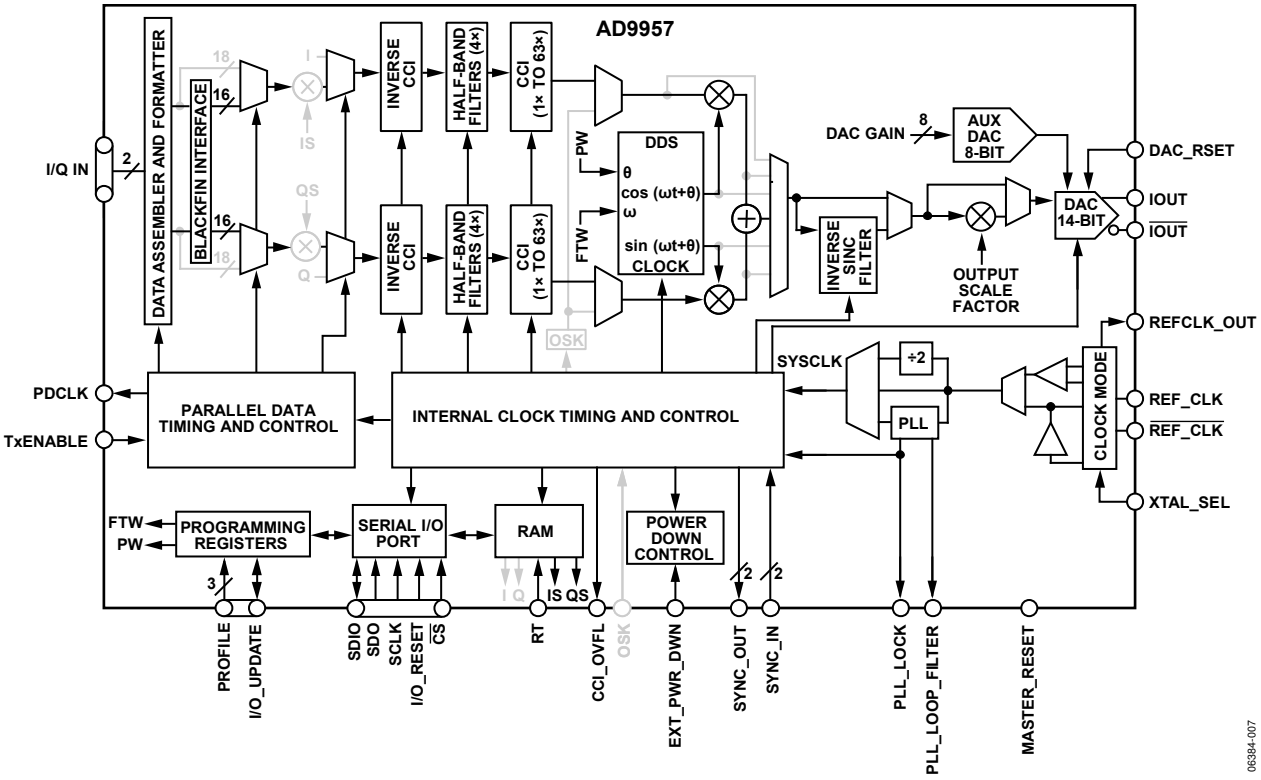

Figure 27. Quadrature Modulation Mode, Blackfin Interface

INTERPOLATING DAC MODE

A block diagram of the AD9957 operating in interpolating DAC mode is shown in Figure 28; grayed items are inactive. In this mode, the Q data path, DDS, and modulator are all disabled; only the I data path is active.

As in quadrature modulation mode, the PDCLK pin functions as a clock, synchronizing the input of data to the AD9957.

No modulation takes place in the interpolating DAC mode; therefore, the spectrum of the data supplied at the parallel port remains at baseband. However, a sample rate conversion takes place based on the programmed interpolation rate. The interpolation hardware processes the signal, effectively performing an oversample with a zero-stuffing operation. The original input spectrum remains intact and the images that otherwise would occur from the sample rate conversion process are suppressed by the interpolation signal chain.

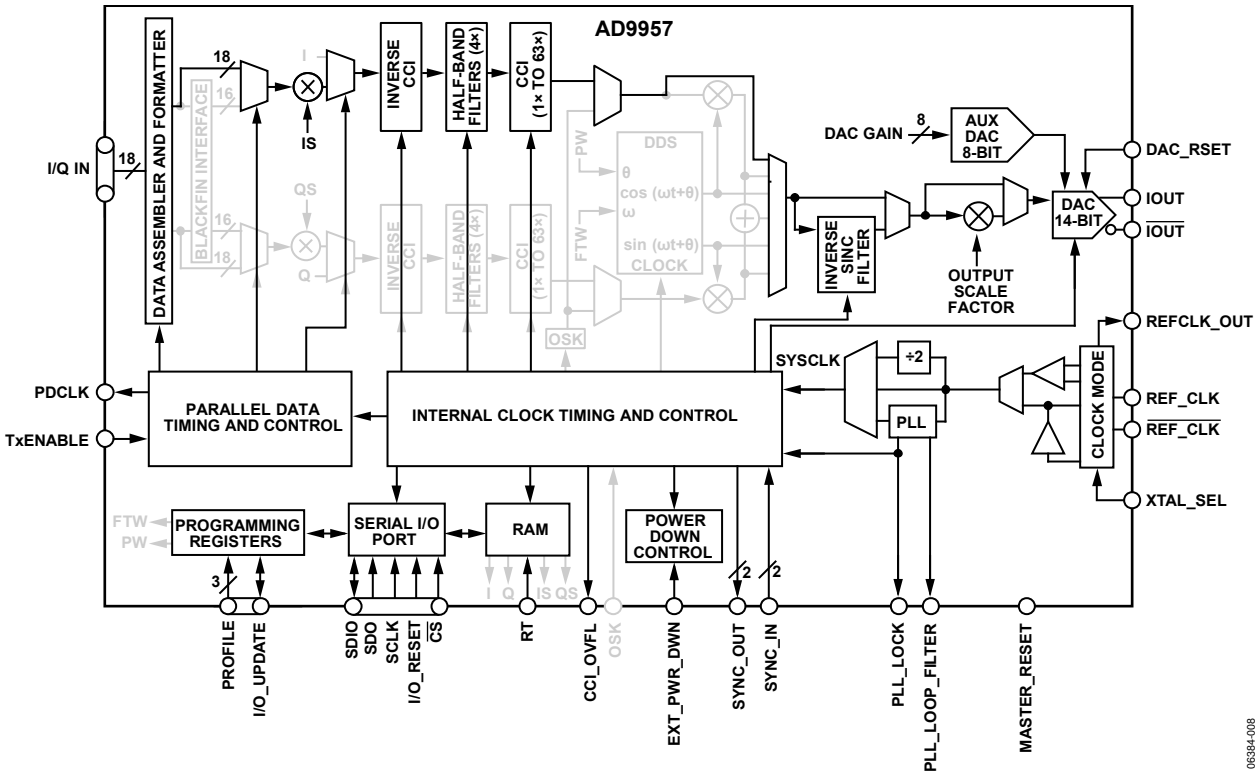

Figure 28. Interpolating DAC Mode

SINGLE TONE MODE

A block diagram of the AD9957 operating in single tone mode is shown in Figure 29; grayed items are inactive. In this mode, both I and Q data paths are disabled from the 18-bit parallel data port up to, and including, the modulator. The internal DDS core produces a single frequency signal based on the programmed tuning word. The user may select either the cosine or sine output of the DDS. The sinusoid at the DDS output can be scaled using a 14-bit amplitude scale factor (ASF) and optionally routed through the inverse sinc filter.

Single tone mode offers the output shift keying (OSK) function. It provides the ability to ramp the amplitude scale factor between zero and an arbitrary preset value over a programmable time interval.

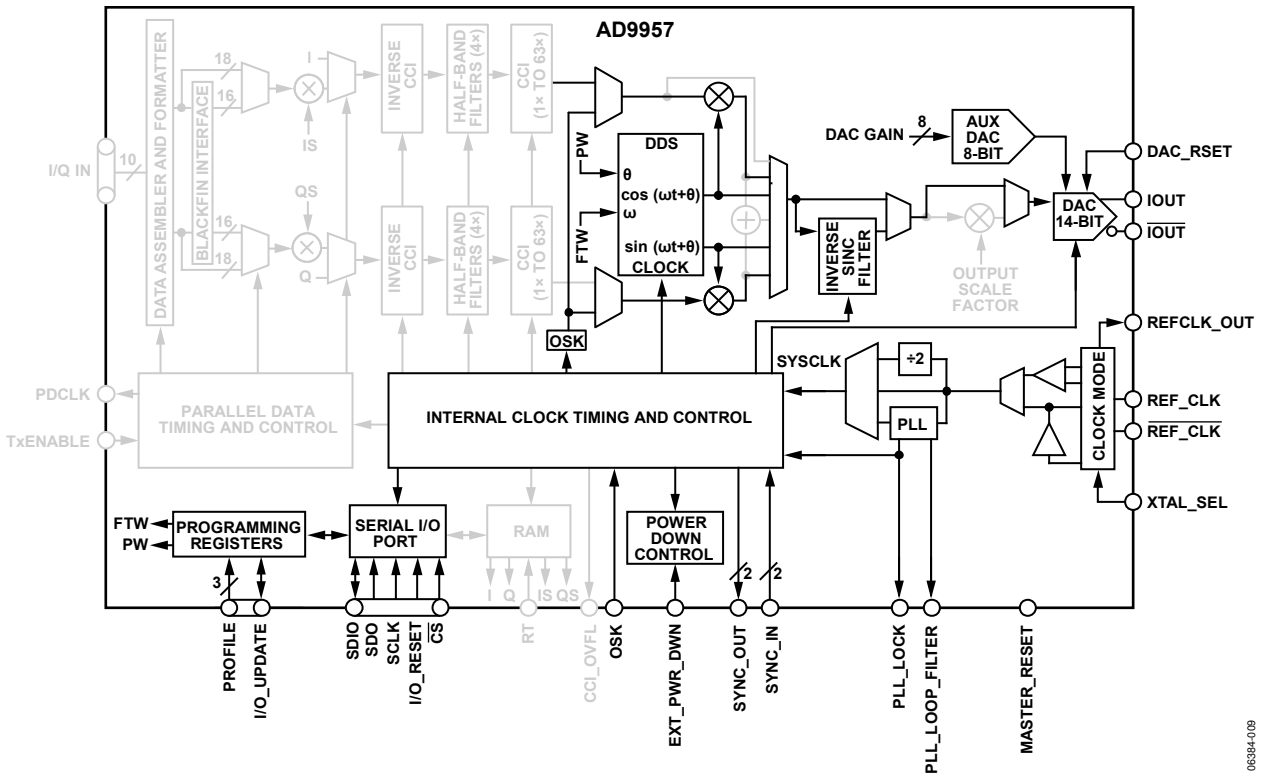

Figure 29. Single Tone Mode

SIGNAL PROCESSING

For a better understanding of the operation of the AD9957, it is helpful to follow the signal path in quadrature modulation mode from the parallel data port to the output of the DAC, examining the function of each block (see Figure 26).

The internal system clock (SYSCLK) signal that generates from the timing source provided to the REF_CLK pins provides all timing within the AD9957.

PARALLEL DATA CLOCK (PDCLK)

The AD9957 generates a signal on the PDCLK pin, which is a clock signal that runs at the sample rate of the parallel data port. PDCLK serves as a data clock for the parallel port in QDUC and interpolating DAC modes; in BFI mode, it is a bit clock. Normally, the device uses the rising edges on PDCLK to latch the user-supplied data into the data port. Alternatively, the PDCLK Invert bit selects the falling edges as the active edges. Furthermore, the PDCLK enable bit is used to switch off the PDCLK signal. Even when the output signal is turned off via the PDCLK enable bit, PDCLK continues to operate internally. The device uses PDCLK internally to capture parallel data. Note that PDCLK is Logic 0 when disabled.

In QDUC mode, the AD9957 expects alternating I- and Q-data-words at the parallel port (see Figure 31). Each active edge of PDCLK captures one 18-bit word; therefore, there are two PDCLK cycles per I/Q pair. In BFI mode, the AD9957 expects two serial bit streams, each segmented into 16-bit words with PDCLK indicating each new bit. In either case, the output clock rate is f_{PDCLK} as explained in the Input Data Assembler section.

In QDUC applications that require a consistent timing relationship between the internal SYSCLK signal and the PDCLK signal, the PDCLK rate control bit is used to slightly alter the operation of PDCLK. When this bit is set, the PDCLK rate is reduced by a factor of two. This causes rising edges on PDCLK to latch incoming I-words and falling edges to latch incoming Q-words. Again, the edge polarity assignment is reversible via the PDCLK Invert bit.

TRANSMIT ENABLE PIN (TxENABLE)

The AD9957 accepts a user-generated signal applied to the TxENABLE pin that gates the user supplied data. Polarity of the TxENABLE pin is set using the TxENABLE invert bit (see the Register Map section for details). When TxENABLE is true, the device latches data into the device on the expected edge of PDCLK (based on the PDCLK invert bit). When TxENABLE is false, the device ignores the data supplied to the port, even though the PDCLK may continue to operate. Furthermore, when the TxENABLE pin is held false, then the device either forces the 18-bit data-words to Logic 0s, or it retains the last value present on the data port prior to TxENABLE switching to the false state (see the data assembler hold last value bit in the Register Map section).

Alternatively, rather than operating the TxENABLE pin as a gate for framing bursts of data, it can be driven with a clock signal operating at the parallel port data rate. When driven by a clock signal, the transition from the false to true state must meet the required setup and hold times on each cycle to ensure proper operation.

In QDUC mode, on the false-to-true edge of TxENABLE, the device is ready to receive the first I-word. The first I-word is latched into the device coincident with the active edge of PDCLK. The next active edge of PDCLK latches in a Q-word, and so on, until TxENABLE is returned to a static false state. The user may reverse the ordering of the I- and Q-words via the Q-First Data Pairing bit. Furthermore, the user must ensure that an even number of data words are delivered to the device as it must capture both an I- and a Q-word before the data is processed along the signal chain.

In interpolating DAC mode, TxENABLE operation is similar to QDUC mode, but without the need for I/Q data pairing; the even-number-of-PDCLK-cycles rule does not apply.

In BFI mode, operation of the TxENABLE pin is similar except that instead of the false-to-true edge marking the first I-word, it marks the first I and Q bits in a serial frame. The user must ensure that all 16-bits of a serial frame are delivered because the device must capture a full 16-bit I- and Q-word before the data is processed along the signal chain.

The timing relationships between TxENABLE, PDCLK, and DATA are shown in Figure 30, Figure 31, and Figure 32.

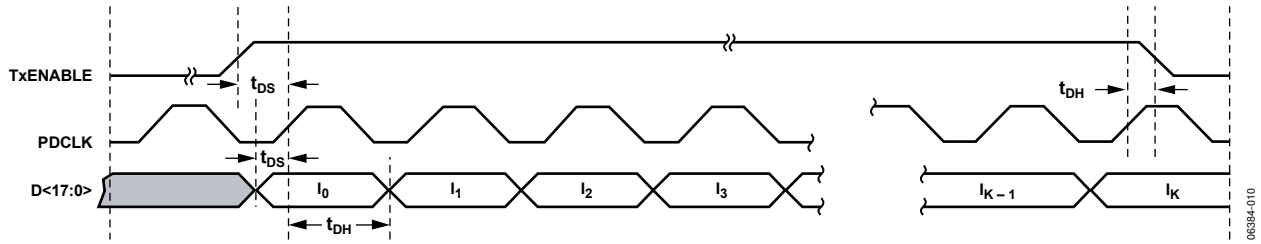

Figure 30. 18-Bit Parallel Port Timing Diagram—Interpolating DAC Mode

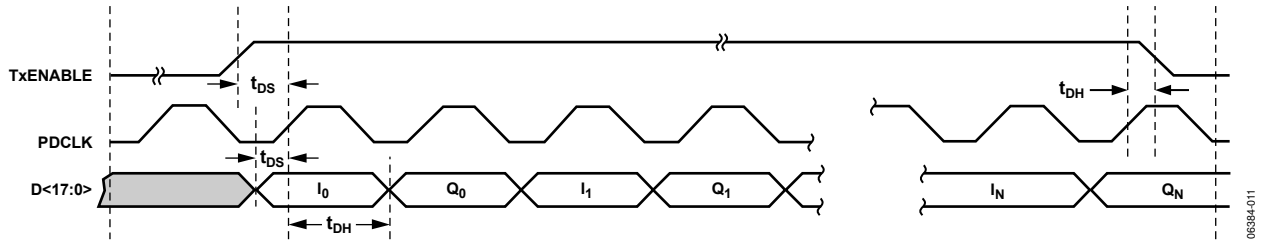

Figure 31. 18-Bit Parallel Port Timing Diagram—Quadrature Modulation Mode

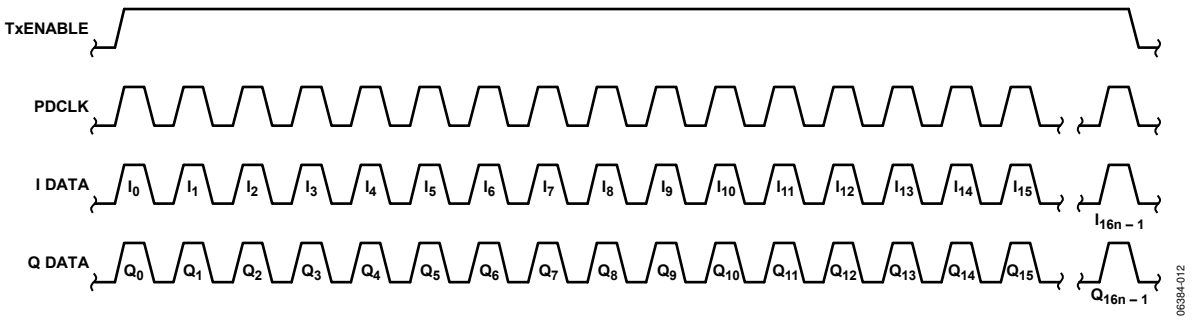

Figure 32. Dual Serial I/Q Bit Stream Timing Diagram, BFI Mode

INPUT DATA ASSEMBLER

The input to the AD9957 is an 18-bit parallel data port in QDUC mode or interpolating DAC mode. In BFI mode, it operates as a dual serial data port.

In QDUC mode, it is assumed that two consecutive 18-bit words represent the real (I) and imaginary (Q) parts of a complex number of the form, I + jQ. The 18-bit words are supplied to the input of the AD9957 at a rate of

$$f_{PDCLK} = \frac{f_{SYSCLK}}{2R} \text{ for QDUC mode}$$

where:
f_{SYSCLK} (for all of the PDCLK equations in this section) is the sample rate of the DAC.
R (for all of the PDCLK equations in this section) is the interpolation factor of the programmable interpolation filter.

When the PDCLK rate control bit is active in QDUC mode, however, the frequency of PDCLK becomes

$$f_{PDCLK} = \frac{f_{SYSCLK}}{4R} \text{ with PDCLK rate control active}$$

In the interpolating DAC mode, the rate of PDCLK is the same as QDUC mode with the PDCLK rate control bit active, that is,

$$f_{PDCLK} = \frac{f_{SYSCLK}}{4R} \text{ for interpolating DAC mode}$$

In BFI mode, the 18-bit parallel input converts to a dual serial input that is, one pin is assigned as the serial input for the I-words and one pin is assigned as the serial input for the Q-words. The other 16 pins are not used. Furthermore, each I- and Q-word has a 16-bit resolution. f_{PDCLK} is the bit rate of the I- and Q-data streams and is given by

$$f_{PDCLK} = \frac{f_{SYSCLK}}{R} \text{ for BFI mode}$$

Encoding and pulse shaping of symbols must be implemented before the data is presented to the input of the AD9957. Data delivered to the input of the AD9957 may be formatted as either twos complement or offset binary (see the Data Format bit in Table 13). In BFI mode, the bit sequence order can be set to either MSB-first or LSB-first (via the Blackfin Bit Order bit).

INVERSE CCI FILTER

The inverse cascaded comb integrator (CCI) filter predistorts the data, compensating for the slight attenuation gradient imposed by the CCI filter (see the Programmable Interpolating Filter section). Data entering the first half-band filter occupies a maximum bandwidth of ½ f_{IQ} as defined by Nyquist (where f_{IQ} is the sample rate at the input of the first half-band filter); see Figure 33.

If the CCI filter is used, the in-band attenuation gradient can pose a problem for applications requiring an extremely flat pass band. For example, if the spectrum of the data supplied to the AD9957 occupies a significant portion of the ½ f_{DATA} region, the higher frequencies of the data spectrum are slightly more attenuated than the lower frequencies (the worst-case overall droop from f = 0 to ½ f_{DATA} is <0.8 dB). The inverse CCI filter has a response characteristic that is the inverse of the CCI filter response over the ½ f_{IQ} region.

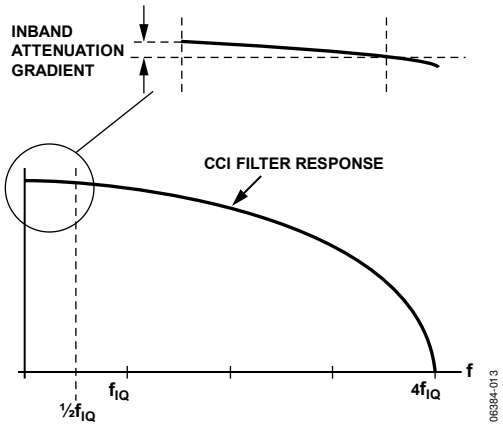

Figure 33. CCI Filter Response

The product of the two responses yields an extremely flat pass band (±0.05 dB over the baseband Nyquist bandwidth) eliminating the in-band attenuation gradient introduced by the CCI filter. The cost is a slight attenuation of the input signal (approximately 0.5 dB for a CCI interpolation rate of 2, and 0.8 dB for higher interpolation rates).

The inverse CCI filter can be bypassed using the appropriate bit in the register map; it is automatically bypassed if the CCI interpolation rate is 1×. When bypassed, power to the stage turns off to reduce power consumption.

FIXED INTERPOLATOR (4×)

This block is a fixed 4× rate interpolator, implemented as a cascade of two half-band filters. Together, the sampling rate of these two filters increases by a factor of four while preserving the spectrum of the baseband signal applied at the input. Both are linear phase filters; virtually no phase distortion is introduced within their pass bands. Their combined insertion loss is 0.01 dB, preserving the relative amplitude of the input signal.

The filters are designed to deliver a composite performance that yields a usable pass band of 40% of the input sample rate. Within that pass band, ripple does not exceed 0.002 dB peak-to-peak. The stop band extends from 60% to 340% of the input sample rate and offers a minimum of 85 dB attenuation. Figure 34 and Figure 35 show the composite response of the two half-band filters.

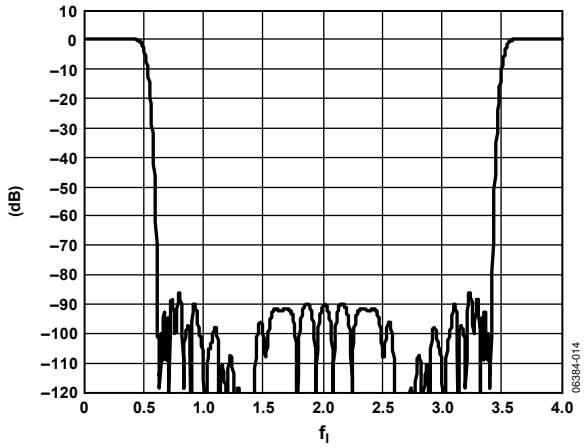

Figure 34. Half-Band 1 and Half-Band 2 Composite Response (Frequency Scaled to Input Sample Rate of Half-Band 1)

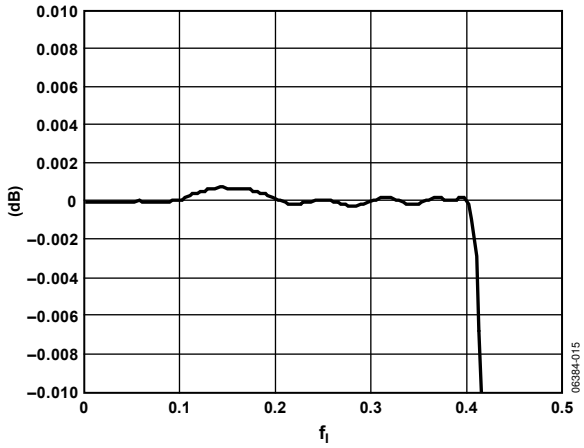

Figure 35. Composite Pass-Band Detail (Frequency Scaled to Input Sample Rate of Half-Band 1)

In BFI mode, there are two additional half-band filters resident, yielding a total fixed interpolation factor of 16×. The extra BFI filters use the same filter tap coefficient values as the QDUC half-band filters, but their data pathway is 16 bits (instead of 18 bits as with the QDUC half-band filters). As such, baseband quantization noise is higher in BFI mode.

Knowledge of the frequency response of the half-band filters is essential to understanding their impact on the spectral properties of the input signal. This is especially true when using the quadrature modulator to upconvert a baseband signal containing complex data symbols that have been pulse shaped.

Consider that a complex symbol is represented by a real (I) and an imaginary (Q) component, thus requiring two digital words to represent a single complex sample of the form I + jQ. The sample rate associated with a sequence of complex symbols is referred to as f_{SYMBOL}. If pulse shaping is applied to the symbols, the sample rate must be increased by some integer factor, M (a consequence of the pulse shaping process). This new sample rate (f_{IQ}) is related to the symbol rate by

$$f_{IQ} = Mf_{SYMBOL}$$

where f_{IQ} is the rate at which complex samples must be supplied to the input of the first half-band filter in both (I and Q) signal paths. This rate should not be confused with the rate at which data is supplied to the AD9957.

Typically, pulse shaping is applied to the baseband symbols via a filter having a raised cosine response. In such cases, an excess bandwidth factor (α, $0 \le \alpha \le 1$) is used to modify the bandwidth of the data. For α = 0, the data bandwidth corresponds to $f_{SYMBOL}/2$; for α = 1, the data bandwidth extends to f_{SYMBOL}. Figure 36 shows the relationship between α, the bandwidth of the raised cosine response, and the response of the first half-band filter.

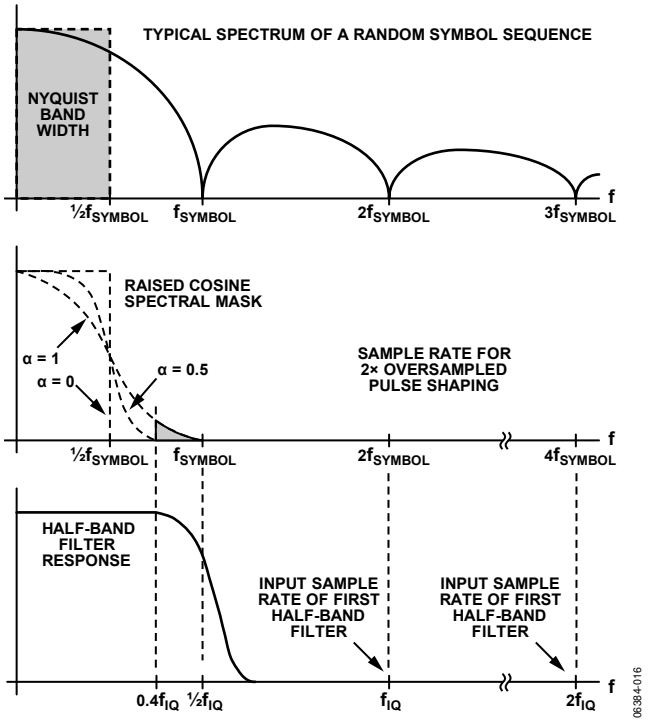

Figure 36. Effect of the Excess Bandwidth Factor (α)

The responses in Figure 36 reflect the specific case of M = 2 (the interpolation factor for the pulse shaping operation). Increasing Factor M shifts the location of the f_{IQ} point on the half-band response portion of the diagram to the right, as it must remain aligned with the corresponding Mf_{SYMBOL} point on the frequency axis of the raised cosine spectral diagram. However, if f_{IQ} shifts to the right, so does the half-band response, proportionally.

The result is that the raised cosine spectral mask always lies within the flat portion (dc to 0.4 f_{IQ}) of the pass band response of the first half-band filter, regardless of the choice of α so long as M > 2. Therefore, for M > 2, the first half-band filter has absolutely no negative impact on the spectrum of the baseband signal when raised cosine pulse shaping is employed. For the case of M = 2, a problem can arise. This is highlighted by the shaded area in the tail of the α = 1 trace on the raised cosine spectral mask diagram. Notice that this portion of the raised cosine spectral mask extends beyond the flat portion of the half-band response and causes unwanted amplitude and phase distortion as the signal passes through the first half-band filter. To avoid this, simply ensure that $\alpha \le 0.6$ when M = 2.

PROGRAMMABLE INTERPOLATING FILTER

The programmable interpolator is implemented as a low-pass CCI filter. It is programmable by a 6-bit control word, giving a range of 2× to 63× interpolation.

The programmable interpolator is bypassed when programmed for an interpolation factor of 1. When bypassed, power to the stage is removed and the inverse CCI filter is also bypassed, because its compensation is not needed.

The output of the programmable interpolator is the data from the 4× interpolator further upsampled by the CCI filter, according to the rate chosen by the user. This results in the upsampling of the input data by a factor of 8× to 252× in steps of four.

The transfer function of the CCI interpolating filter is

$$H(f) = \left(\sum_{k=0}^{R-1} e^{-j(2\pi fk)} \right)^5 \quad (1)$$

where *R* is the programmed interpolation factor, and *f* is the frequency normalized to f_{SYSCLK}.

Note that minimum R requirements exist depending on the mode and frequency of f_{SYSCLK}. The minimum R setting is defined under the follo wing conditions.

QDUC Mode

If f_{SYSCLK} is between 500 MSPS to 1 GSPS, then the minimum R is 2.

If f_{SYSCLK} is less than 500 MSPS, then the minimum R is 1.

BFI Mode

If f_{SYSCLK} is between 500 MSPS to 750 MSPS, then the minimum R is 3.

If f_{SYSCLK} is between 250 MSPS to 500 MSPS, then the minimum R is 2.

If f_{SYSCLK} is less than 250 MSPS, then the minimum R is 1.