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ANALOG DEVICES

2-Channel, 500 MSPS DDS with 10-Bit DACs

Data Sheet **AD9958**

FEATURES

- 2 synchronized DDS channels @ 500 MSPS
- Independent frequency/phase/amplitude control between channels
- Matched latencies for frequency/phase/amplitude changes
- Excellent channel-to-channel isolation (>72 dB)
- Linear frequency/phase/amplitude sweeping capability
- Up to 16 levels of frequency/phase/amplitude modulation (pin-selectable)
- 2 integrated 10-bit digital-to-analog converters (DACs)
- Individually programmable DAC full-scale currents
- 0.12 Hz or better frequency tuning resolution
- 14-bit phase offset resolution
- 10-bit output amplitude scaling resolution
- Serial I/O port interface (SPI) with 800 Mbps data throughput
- Software-/hardware-controlled power-down
- Dual supply operation (1.8 V DDS core/3.3 V serial I/O)
- Multiple device synchronization
- Selectable 4× to 20× REFCLK multiplier (PLL)
- Selectable REFCLK crystal oscillator
- 56-lead LFCSP

APPLICATIONS

- Agile local oscillators
- Phased array radars/sonars
- Instrumentation
- Synchronized clocking
- RF source for AOTF
- Single-side band suppressed carriers
- Quadrature communications

FUNCTIONAL BLOCK DIAGRAM

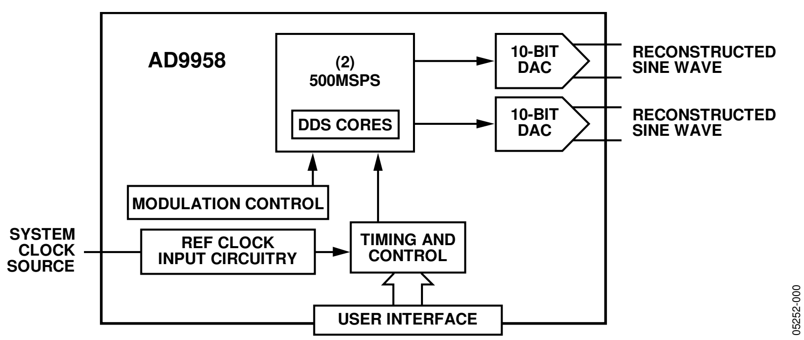

Figure 1.

Rev. C Document Feedback

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AD9958* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

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EVALUATION KITS

- AD9958 Evaluation Board

DOCUMENTATION

Application Notes

- AN-237: Choosing DACs for Direct Digital Synthesis
- AN-280: Mixed Signal Circuit Technologies
- AN-342: Analog Signal-Handling for High Speed and Accuracy
- AN-345: Grounding for Low-and-High-Frequency Circuits
- AN-419: A Discrete, Low Phase Noise, 125 MHz Crystal Oscillator for the AD9850
- AN-423: Amplitude Modulation of the AD9850 Direct Digital Synthesizer
- AN-543: High Quality, All-Digital RF Frequency Modulation Generation with the ADSP-2181 and the AD9850 DDS
- AN-557: An Experimenter's Project:
- AN-587: Synchronizing Multiple AD9850/AD9851 DDS-Based Synthesizers
- AN-605: Synchronizing Multiple AD9852 DDS-Based Synthesizers
- AN-621: Programming the AD9832/AD9835
- AN-632: Provisionary Data Rates Using the AD9951 DDS as an Agile Reference Clock for the ADN2812 Continuous-Rate CDR
- AN-769: Generating Multiple Clock Outputs from the AD9540
- AN-823: Direct Digital Synthesizers in Clocking Applications Time
- AN-837: DDS-Based Clock Jitter Performance vs. DAC Reconstruction Filter Performance
- AN-851: A WiMax Double Downconversion IF Sampling Receiver Design
- AN-927: Determining if a Spur is Related to the DDS/DAC or to Some Other Source (For Example, Switching Supplies)
- AN-939: Super-Nyquist Operation of the AD9912 Yields a High RF Output Signal
- AN-953: Direct Digital Synthesis (DDS) with a Programmable Modulus

Data Sheet

- AD9958: 2-Channel 500 MSPS DDS with 10-Bit DACs Data Sheet

Product Highlight

- Introducing Digital Up/Down Converters: VersaCOMM™ Reconfigurable Digital Converters

TOOLS AND SIMULATIONS

- ADIsimDDS (Direct Digital Synthesis)

REFERENCE DESIGNS

- CN0109
- CN0186

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

Technical Articles

- 400-MSample DDSs Run On Only +1.8 VDC
- ADI Buys Korean Mobile TV Chip Maker
- Basics of Designing a Digital Radio Receiver (Radio 101)
- DDS Applications
- DDS Circuit Generates Precise PWM Waveforms
- DDS Design
- DDS Device Produces Sawtooth Waveform
- DDS Device Provides Amplitude Modulation
- DDS IC Initiates Synchronized Signals
- DDS IC Plus Frequency-To-Voltage Converter Make Low-Cost DAC
- DDS Simplifies Polar Modulation
- Digital Potentiometers Vary Amplitude In DDS Devices
- Digital Up/Down Converters: VersaCOMM™ White Paper
- Digital Waveform Generator Provides Flexible Frequency Tuning for Sensor Measurement
- Improved DDS Devices Enable Advanced Comm Systems
- Integrated DDS Chip Takes Steps To 2.7 GHz
- Simple Circuit Controls Stepper Motors
- Speedy A/Ds Demand Stable Clocks
- Synchronized Synthesizers Aid Multichannel Systems
- The Year of the Waveform Generator
- Two DDS ICs Implement Amplitude-shift Keying
- Video Portables and Cameras Get HDMI Outputs

DESIGN RESOURCES

- AD9958 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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DOCUMENT FEEDBACK

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9/2005—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9958 consists of two DDS cores that provide independent frequency, phase, and amplitude control on each channel. This flexibility can be used to correct imbalances between signals due to analog processing, such as filtering, amplification, or PCB layout related mismatches. Because both channels share a common system clock, they are inherently synchronized. Synchronization of multiple devices is supported.

The AD9958 can perform up to a 16-level modulation of frequency, phase, or amplitude (FSK, PSK, ASK). Modulation is performed by applying data to the profile pins. In addition, the AD9958 also supports linear sweep of frequency, phase, or amplitude for applications such as radar and instrumentation.

The AD9958 serial I/O port offers multiple configurations to provide significant flexibility. The serial I/O port offers an SPI-compatible mode of operation that is virtually identical to the SPI operation found in earlier Analog Devices, Inc., DDS products. Flexibility is provided by four data pins (SDIO_0/SDIO_1/SDIO_2/SDIO_3) that allow four programmable modes of serial I/O operation.

The AD9958 uses advanced DDS technology that provides low power dissipation with high performance. The device incorporates two integrated, high speed 10-bit DACs with excellent wideband and narrow-band SFDR. Each channel has a dedicated 32-bit frequency tuning word, 14 bits of phase offset, and a 10-bit output scale multiplier.

The DAC outputs are supply referenced and must be terminated into AVDD by a resistor or an AVDD center-tapped transformer. Each DAC has its own programmable reference to enable different full-scale currents for each channel.

The DDS acts as a high resolution frequency divider with the REFCLK as the input and the DAC providing the output. The REFCLK input source is common to both channels and can be driven directly or used in combination with an integrated REFCLK multiplier (PLL) up to a maximum of 500 MSPS. The PLL multiplication factor is programmable from 4 to 20, in integer steps. The REFCLK input also features an oscillator circuit to support an external crystal as the REFCLK source. The crystal must be between 20 MHz and 30 MHz. The crystal can be used in combination with the REFCLK multiplier.

The AD9958 comes in a space-saving 56-lead LFCSP package. The DDS core (AVDD and DVDD pins) is powered by a 1.8 V supply. The digital I/O interface (SPI) operates at 3.3 V and requires the pin labeled DVDD_I/O (Pin 49) be connected to 3.3 V.

The AD9958 operates over the industrial temperature range of −40°C to +85°C.

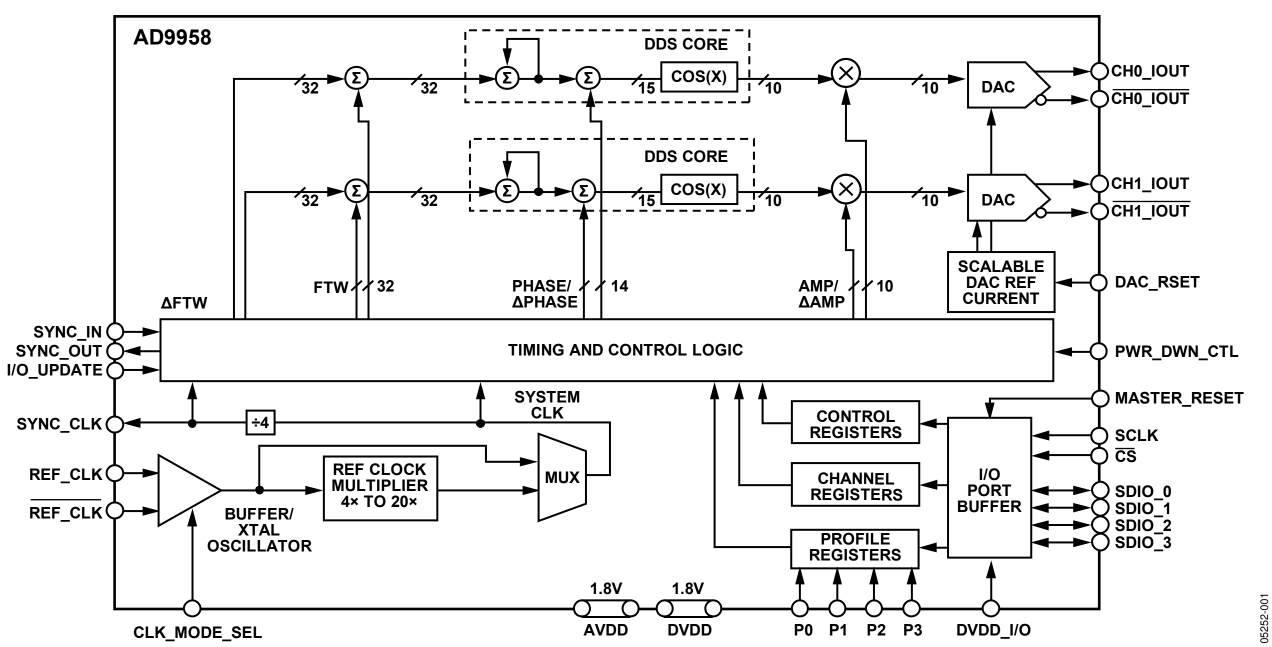


Figure 2. Detailed Block Diagram

SPECIFICATIONS

AVDD and DVDD = 1.8 V ± 5%; DVDD_I/O = 3.3 V ± 5%; T = 25°C; R_{SET} = 1.91 kΩ; external reference clock frequency = 500 MSPS (REFCLK multiplier bypassed), unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE CLOCK INPUT CHARACTERISTICS					See Figure 34 and Figure 35
Frequency Range					
REFCLK Multiplier Bypassed	1		500	MHz	
REFCLK Multiplier Enabled	10		125	MHz	
Internal VCO Output Frequency Range					
VCO Gain Control Bit Set High[1]	255		500	MHz	
VCO Gain Control Bit Set Low[1]	100		160	MHz	
Crystal REFCLK Source Range	20		30	MHz	
Input Level	200		1000	mV	Measured at each pin (single-ended)
Input Voltage Bias Level		1.15		V	
Input Capacitance		2		pF	
Input Impedance		1500		Ω	
Duty Cycle with REFCLK Multiplier Bypassed	45		55	%	
Duty Cycle with REFCLK Multiplier Enabled	35		65	%	
CLK Mode Select (Pin 24) Logic 1 Voltage	1.25		1.8	V	1.8 V digital input logic
CLK Mode Select (Pin 24) Logic 0 Voltage			0.5	V	1.8 V digital input logic
DAC OUTPUT CHARACTERISTICS					Must be referenced to AVDD
Resolution			10	Bits	
Full-Scale Output Current	1.25		10	mA	
Gain Error	−10		+10	% FS	
Channel-to-Channel Output Amplitude Matching Error	−2.5		+2.5	%	
Output Current Offset		1	25	µA	
Differential Nonlinearity		±0.5		LSB	
Integral Nonlinearity		±1.0		LSB	
Output Capacitance		3		pF	
Voltage Compliance Range	AVDD − 0.50		AVDD + 0.50	V	
Channel-to-Channel Isolation	72			dB	DAC supplies tied together (see Figure 19)
WIDEBAND SFDR					The frequency range for wideband SFDR is defined as dc to Nyquist
1 MHz to 20 MHz Analog Output		−65		dBc	
20 MHz to 60 MHz Analog Output		−62		dBc	
60 MHz to 100 MHz Analog Output		−59		dBc	
100 MHz to 150 MHz Analog Output		−56		dBc	
150 MHz to 200 MHz Analog Output		−53		dBc	
NARROW-BAND SFDR					
1.1 MHz Analog Output (±10 kHz)		−90		dBc	
1.1 MHz Analog Output (±50 kHz)		−88		dBc	
1.1 MHz Analog Output (±250 kHz)		−86		dBc	
1.1 MHz Analog Output (±1 MHz)		−85		dBc	
15.1 MHz Analog Output (±10 kHz)		−90		dBc	
15.1 MHz Analog Output (±50 kHz)		−87		dBc	
15.1 MHz Analog Output (±250 kHz)		−85		dBc	
15.1 MHz Analog Output (±1 MHz)		−83		dBc	
40.1 MHz Analog Output (±10 kHz)		−90		dBc	
40.1 MHz Analog Output (±50 kHz)		−87		dBc	
40.1 MHz Analog Output (±250 kHz)		−84		dBc	
40.1 MHz Analog Output (±1 MHz)		−82		dBc	
75.1 MHz Analog Output (±10 kHz)		−87		dBc	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
75.1 MHz Analog Output (±50 kHz)		−85		dBc	
75.1 MHz Analog Output (±250 kHz)		−83		dBc	
75.1 MHz Analog Output (±1 MHz)		−82		dBc	
100.3 MHz Analog Output (±10 kHz)		−87		dBc	
100.3 MHz Analog Output (±50 kHz)		−85		dBc	
100.3 MHz Analog Output (±250 kHz)		−83		dBc	
100.3 MHz Analog Output (±1 MHz)		−81		dBc	
200.3 MHz Analog Output (±10 kHz)		−87		dBc	
200.3 MHz Analog Output (±50 kHz)		−85		dBc	
200.3 MHz Analog Output (±250 kHz)		−83		dBc	
200.3 MHz Analog Output (±1 MHz)		−81		dBc	
PHASE NOISE CHARACTERISTICS					
Residual Phase Noise @ 15.1 MHz (f_{OUT})					
@ 1 kHz Offset		−150		dBc/Hz	
@ 10 kHz Offset		−159		dBc/Hz	
@ 100 kHz Offset		−165		dBc/Hz	
@ 1 MHz Offset		−165		dBc/Hz	
Residual Phase Noise @ 40.1 MHz (f_{OUT})					
@ 1 kHz Offset		−142		dBc/Hz	
@ 10 kHz Offset		−151		dBc/Hz	
@ 100 kHz Offset		−160		dBc/Hz	
@ 1 MHz Offset		−162		dBc/Hz	
Residual Phase Noise @ 75.1 MHz (f_{OUT})					
@ 1 kHz Offset		−135		dBc/Hz	
@ 10 kHz Offset		−146		dBc/Hz	
@ 100 kHz Offset		−154		dBc/Hz	
@ 1 MHz Offset		−157		dBc/Hz	
Residual Phase Noise @ 100.3 MHz (f_{OUT})					
@ 1 kHz Offset		−134		dBc/Hz	
@ 10 kHz Offset		−144		dBc/Hz	
@ 100 kHz Offset		−152		dBc/Hz	
@ 1 MHz Offset		−154		dBc/Hz	
Residual Phase Noise @ 15.1 MHz (f_{OUT}) with REFCLK Multiplier Enabled 5×					
@ 1 kHz Offset		−139		dBc/Hz	
@ 10 kHz Offset		−149		dBc/Hz	
@ 100 kHz Offset		−153		dBc/Hz	
@ 1 MHz Offset		−148		dBc/Hz	
Residual Phase Noise @ 40.1 MHz (f_{OUT}) with REFCLK Multiplier Enabled 5×					
@ 1 kHz Offset		−130		dBc/Hz	
@ 10 kHz Offset		−140		dBc/Hz	
@ 100 kHz Offset		−145		dBc/Hz	
@ 1 MHz Offset		−139		dBc/Hz	
Residual Phase Noise @ 75.1 MHz (f_{OUT}) with REFCLK Multiplier Enabled 5×					
@ 1 kHz Offset		−123		dBc/Hz	
@ 10 kHz Offset		−134		dBc/Hz	
@ 100 kHz Offset		−138		dBc/Hz	
@ 1 MHz Offset		−132		dBc/Hz	
Residual Phase Noise @ 100.3 MHz (f_{OUT}) with REFCLK Multiplier Enabled 5×					
@ 1 kHz Offset		−120		dBc/Hz	
@ 10 kHz Offset		−130		dBc/Hz	
@ 100 kHz Offset		−135		dBc/Hz	
@ 1 MHz Offset		−129		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Residual Phase Noise @ 15.1 MHz (f_{OUT}) with REFCLK Multiplier Enabled 20×					
@ 1 kHz Offset		−127		dBc/Hz	
@ 10 kHz Offset		−136		dBc/Hz	
@ 100 kHz Offset		−139		dBc/Hz	
@ 1 MHz Offset		−138		dBc/Hz	
Residual Phase Noise @ 40.1 MHz (f_{OUT}) with REFCLK Multiplier Enabled 20×					
@ 1 kHz Offset		−117		dBc/Hz	
@ 10 kHz Offset		−128		dBc/Hz	
@ 100 kHz Offset		−132		dBc/Hz	
@ 1 MHz Offset		−130		dBc/Hz	
Residual Phase Noise @ 75.1 MHz (f_{OUT}) with REFCLK Multiplier Enabled 20×					
@ 1 kHz Offset		−110		dBc/Hz	
@ 10 kHz Offset		−121		dBc/Hz	
@ 100 kHz Offset		−125		dBc/Hz	
@ 1 MHz Offset		−123		dBc/Hz	
Residual Phase Noise @ 100.3 MHz (f_{OUT}) with REFCLK Multiplier Enabled 20×					
@ 1 kHz Offset		−107		dBc/Hz	
@ 10 kHz Offset		−119		dBc/Hz	
@ 100 kHz Offset		−121		dBc/Hz	
@ 1 MHz Offset		−119		dBc/Hz	
SERIAL PORT TIMING CHARACTERISTICS					
Maximum Frequency Serial Clock (SCLK)			200	MHz	
Minimum SCLK Pulse Width Low (t_{PWL})	1.6			ns	
Minimum SCLK Pulse Width High (t_{PWH})	2.2			ns	
Minimum Data Setup Time (t_{DS})	2.2			ns	
Minimum Data Hold Time	0			ns	
Minimum $\overline{CS}$ Setup Time (t_{PRE})	1.0			ns	
Minimum Data Valid Time for Read Operation	12			ns	
MISCELLANEOUS TIMING CHARACTERISTICS					
MASTER_RESET Minimum Pulse Width	1				Min pulse width = 1 sync clock period
I/O_UPDATE Minimum Pulse Width	1				Min pulse width = 1 sync clock period
Minimum Setup Time (I/O_UPDATE to SYNC_CLK)	4.8			ns	Rising edge to rising edge
Minimum Hold Time (I/O_UPDATE to SYNC_CLK)	0			ns	Rising edge to rising edge
Minimum Setup Time (Profile Inputs to SYNC_CLK)	5.4			ns	
Minimum Hold Time (Profile Inputs to SYNC_CLK)	0			ns	
Minimum Setup Time (SDIO Inputs to SYNC_CLK)	2.5			ns	
Minimum Hold Time (SDIO Inputs to SYNC_CLK)	0			ns	
Propagation Time Between REF_CLK and SYNC_CLK	2.25	3.5	5.5	ns	
Profile Pin Toggle Rate			2	Sync clocks	
CMOS LOGIC INPUTS					
V_{IH}	2.0			V	
V_{IL}			0.8	V	
Logic 1 Current		3	12	µA	
Logic 0 Current		−12		µA	
Input Capacitance		2		pF	
CMOS LOGIC OUTPUTS					1 mA load
V_{OH}	2.7			V	
V_{OL}			0.4	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
Total Power Dissipation—Both Channels On, Single-Tone Mode		315	380	mW	Dominated by supply variation
Total Power Dissipation—Both Channels On, with Sweep Accumulator		350	420	mW	Dominated by supply variation
Total Power Dissipation—Full Power-Down		13		mW	
I_{AVDD}—Both Channels On, Single-Tone Mode		90	105	mA	
I_{AVDD}—Both Channels On, Sweep Accumulator, REFCLK Multiplier, and 10-Bit Output Scalar Enabled		95	110	mA	
I_{DVDD}—Both Channels On, Single-Tone Mode		60	70	mA	
I_{DVDD}—Both Channels On, Sweep Accumulator, REFCLK Multiplier, and 10-Bit Output Scalar Enabled		70	80	mA	
$I_{DVDD\_I/O}$			22	mA	I_{DVDD} = read
			30	mA	I_{DVDD} = write
I_{AVDD} Power-Down Mode			2.5	mA	
I_{DVDD} Power-Down Mode			2.5	mA	
DATA LATENCY (PIPELINE DELAY) SINGLE-TONE MODE[2, 3]					
Frequency, Phase, and Amplitude Words to DAC Output with Matched Latency Enabled	29			SYSCLKs	
Frequency Word to DAC Output with Matched Latency Disabled	29			SYSCLKs	
Phase Offset Word to DAC Output with Matched Latency Disabled	25			SYSCLKs	
Amplitude Word to DAC Output with Matched Latency Disabled	17			SYSCLKs	
DATA LATENCY (PIPELINE DELAY) MODULATION MODE[3, 4]					
Frequency Word to DAC Output	34			SYSCLKs	
Phase Offset Word to DAC Output	29			SYSCLKs	
Amplitude Word to DAC Output	21			SYSCLKs	
DATA LATENCY (PIPELINE DELAY) LINEAR SWEEP MODE[3,4]					
Frequency Rising/Falling Delta-Tuning Word to DAC Output	41			SYSCLKs	
Phase Offset Rising/Falling Delta-Tuning Word to DAC Output	37			SYSCLKs	
Amplitude Rising/Falling Delta-Tuning Word to DAC Output	29			SYSCLKs	

[1] For the VCO frequency range of 160 MHz to 255 MHz, there is no guarantee of operation.
[2] Data latency is referenced to I/O_UPDATE.
[3] Data latency is fixed.
[4] Data latency is referenced to a profile change.

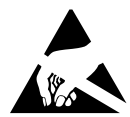
ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Maximum Junction Temperature	150°C
DVDD_I/O (Pin 49)	4 V
AVDD, DVDD	2 V
Digital Input Voltage (DVDD_I/O = 3.3 V)	−0.7 V to +4 V
Digital Output Current	5 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (10 sec Soldering)	300°C
θ_{JA}	21°C/W
θ_{JC}	2°C/W

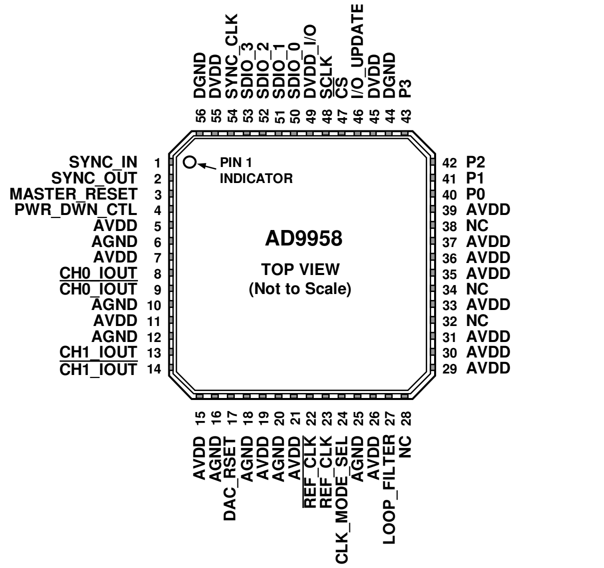
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED EPAD ON BOTTOM SIDE OF PACKAGE IS AN ELECTRICAL CONNECTION AND MUST BE SOLDERED TO GROUND.
2. PIN 49 IS DVDD_I/O AND IS TIED TO 3.3V.
3. NC = NO CONNECT.

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	I/O[1]	Description
1	SYNC_IN	I	Used to Synchronize Multiple AD9958 Devices. Connects to the SYNC_OUT pin of the master AD9958 device.
2	SYNC_OUT	O	Used to Synchronize Multiple AD9958 Devices. Connects to the SYNC_IN pin of the slave AD9958 devices.
3	MASTER_RESET	I	Active High Reset Pin. Asserting the MASTER_RESET pin forces the AD9958 internal registers to their default state, as described in the Register Maps and Bit Descriptions section.
4	PWR_DWN_CTL	I	External Power-Down Control.
5, 7, 11, 15, 19, 21, 26, 29, 30, 31, 33, 35, 36, 37, 39	AVDD	I	Analog Power Supply Pins (1.8 V).
6, 10, 12, 16, 18, 20, 25	AGND	I	Analog Ground Pins.
45, 55	DVDD	I	Digital Power Supply Pins (1.8 V).
44, 56	DGND	I	Digital Power Ground Pins.
8	CH0_IOUT	O	True DAC Output. Terminates into AVDD.
9	$\overline{\text{CH0\_IOUT}}$	O	Complementary DAC Output. Terminates into AVDD.
13	CH1_IOUT	O	True DAC Output. Terminates into AVDD.
14	$\overline{\text{CH1\_IOUT}}$	O	Complementary DAC Output. Terminates into AVDD.
17	DAC_RSET	I	Establishes the Reference Current for All DACs. A 1.91 kΩ resistor (nominal) is connected from Pin 17 to AGND.
22	$\overline{\text{REF\_CLK}}$	I	Complementary Reference Clock/Oscillator Input. When the REF_CLK is operated in single-ended mode, this pin should be decoupled to AVDD or AGND with a 0.1 µF capacitor.
23	REF_CLK	I	Reference Clock/Oscillator Input. When the REF_CLK is operated in single-ended mode, this is the input. See the Modes of Operation section for the reference clock configuration.

Pin No.	Mnemonic	I/O[1]	Description
24	CLK_MODE_SEL	I	Control Pin for the Oscillator Section. Caution: Do not drive this pin beyond 1.8 V. When high (1.8 V), the oscillator section is enabled to accept a crystal as the REF_CLK source. When low, the oscillator section is bypassed.
27	LOOP_FILTER	I	Connects to the external zero compensation network of the PLL loop filter. Typically, the network consists of a 0 Ω resistor in series with a 680 pF capacitor tied to AVDD.
28, 32, 34, 38	NC	N/A	No Connection.
40, 41, 42, 43	P0, P1, P2, P3	I	Data pins used for modulation (FSK, PSK, ASK), to start/stop for the sweep accumulators, or used to ramp up/ramp down the output amplitude. The data is synchronous to the SYNC_CLK (Pin 54). The data inputs must meet the setup and hold time requirements to the SYNC_CLK. The functionality of these pins is controlled by profile pin configuration (PPC) bits (FR1[14:12]).
46	I/O_UPDATE	I	A rising edge transfers data from the serial I/O port buffer to active registers. I/O_UPDATE is synchronous to the SYNC_CLK (Pin 54). I/O_UPDATE must meet the setup and hold time requirements to the SYNC_CLK to guarantee a fixed pipeline delay of data to the DAC output; otherwise, a ±1 SYNC_CLK period of pipeline uncertainty exists. The minimum pulse width is one SYNC_CLK period.
47	$\overline{\text{CS}}$	I	Active Low Chip Select. Allows multiple devices to share a common I/O bus (SPI).
48	SCLK	I	Serial Data Clock for I/O Operations. Data bits are written on the rising edge of SCLK and read on the falling edge of SCLK.
49	DVDD_I/O	I	3.3 V Digital Power Supply for SPI Port and Digital I/O.
50	SDIO_0	I/O	Data Pin SDIO_0 is dedicated to the serial port I/O only.
51, 52, 53	SDIO_1, SDIO_2, SDIO_3	I/O	Data Pin SDIO_1, Data Pin SDIO_2, and Data Pin SDIO_3 can be used for the serial I/O port or used to initiate a ramp-up/ramp-down (RU/RD) of the DAC output amplitude.
54	SYNC_CLK	O	The SYNC_CLK runs at one fourth the system clock rate. It can be disabled. I/O_UPDATE or data (Pin 40 to Pin 43) is synchronous to the SYNC_CLK. To guarantee a fixed pipeline delay of data to DAC output, I/O_UPDATE or data (Pin 40 to Pin 43) must meet the setup and hold time requirements to the rising edge of SYNC_CLK; otherwise, a ±1 SYNC_CLK period of uncertainty exists.

[1] I = input, O = output.

TYPICAL PERFORMANCE CHARACTERISTICS

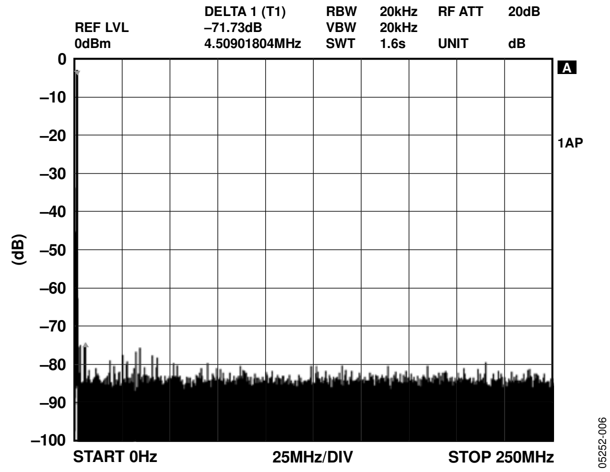


Figure 4. Wideband SFDR, f_{OUT} = 1.1 MHz, f_{CLK} = 500 MSPS

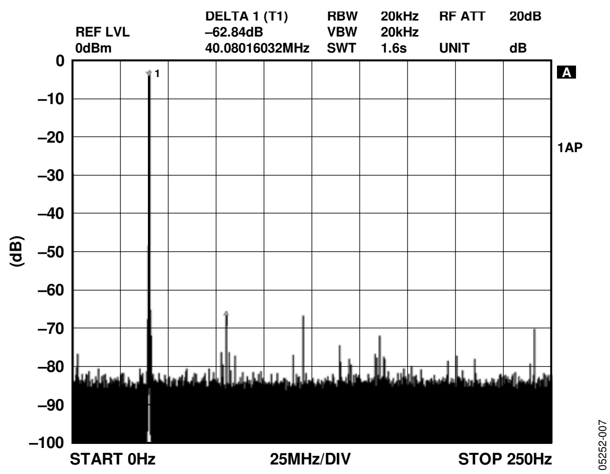


Figure 5. Wideband SFDR, f_{OUT} = 40.1 MHz, f_{CLK} = 500 MSPS

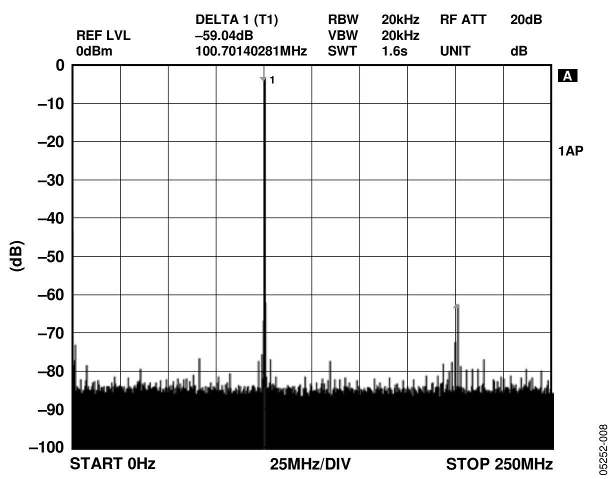


Figure 6. Wideband SFDR, f_{OUT} = 100.3 MHz, f_{CLK} = 500 MSPS

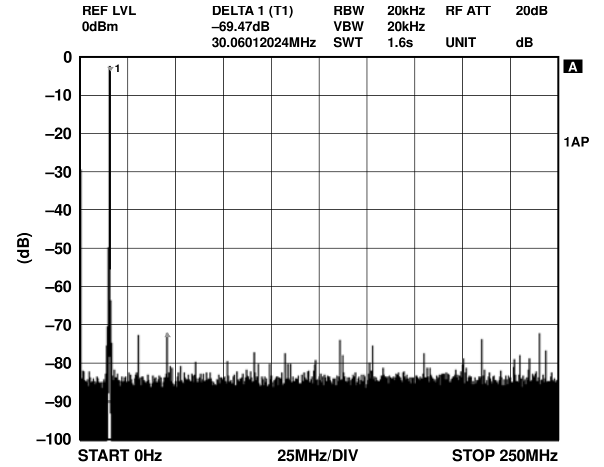


Figure 7. Wideband SFDR, f_{OUT} = 15.1 MHz, f_{CLK} = 500 MSPS

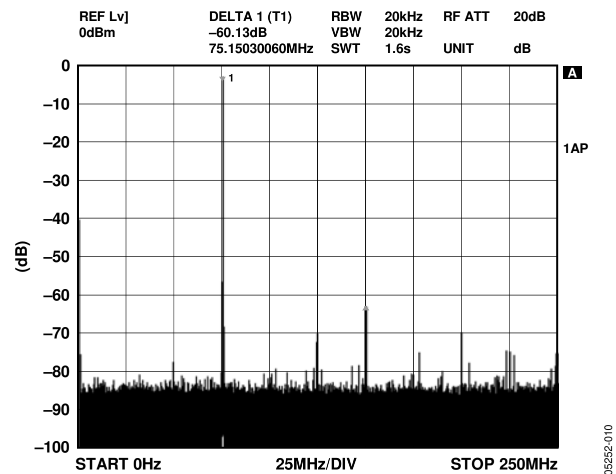


Figure 8. Wideband SFDR, f_{OUT} = 75.1 MHz, f_{CLK} = 500 MSPS

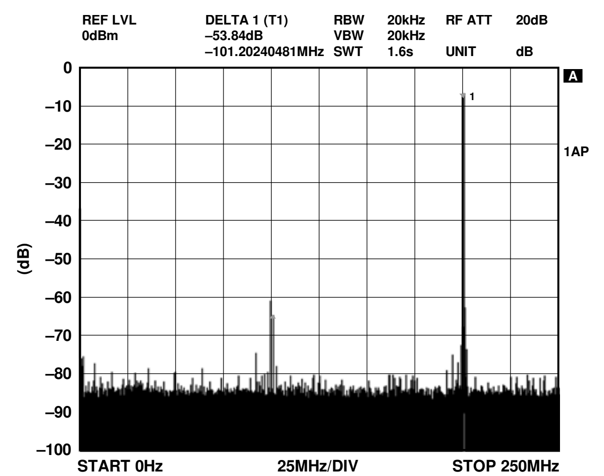


Figure 9. Wideband SFDR, f_{OUT} = 200.3 MHz, f_{CLK} = 500 MSPS

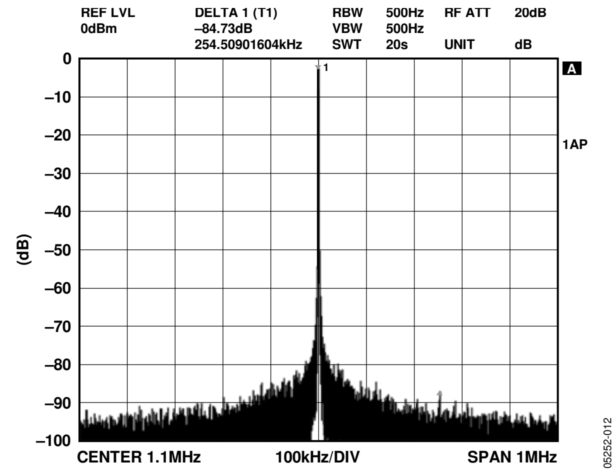


Figure 10. NBSFDR, f_{OUT} = 1.1 MHz, f_{CLK} = 500 MSPS, ±1 MHz

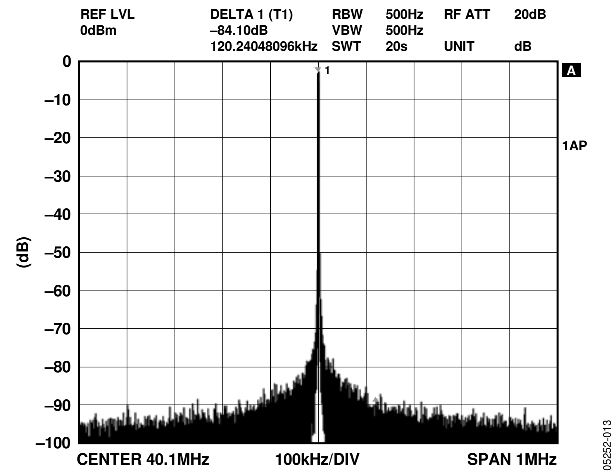


Figure 11. NBSFDR, f_{OUT} = 40.1 MHz, f_{CLK} = 500 MSPS, ±1 MHz

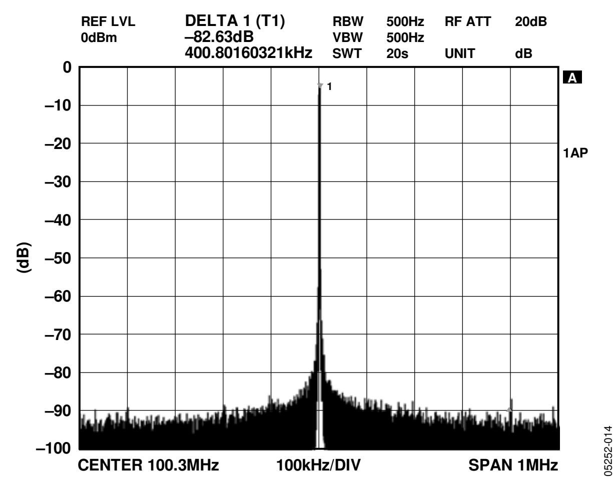


Figure 12. NBSFDR, f_{OUT} = 100.3 MHz, f_{CLK} = 500 MSPS, ±1 MHz

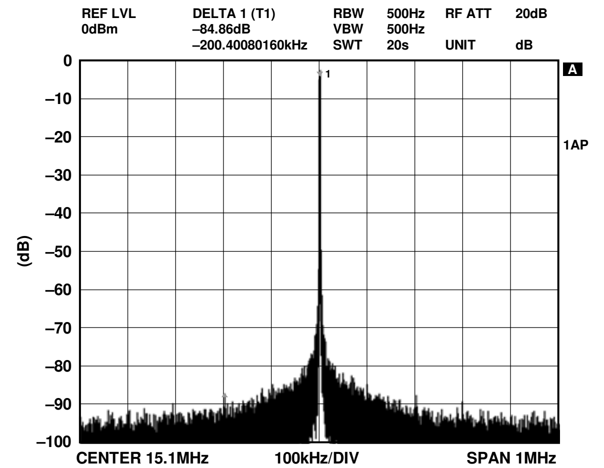


Figure 13. NBSFDR, f_{OUT} = 15.1 MHz, f_{CLK} = 500 MSPS, ±1 MHz

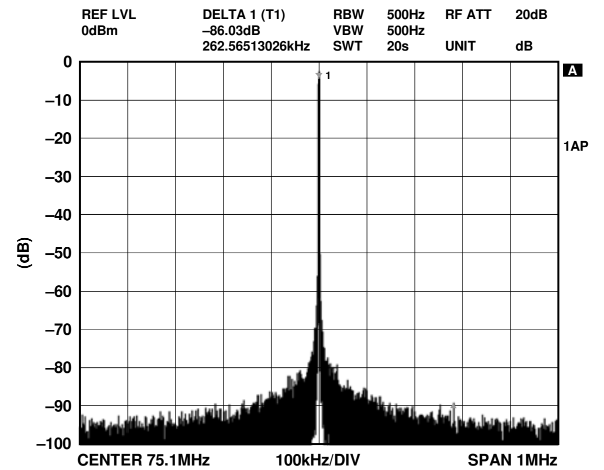


Figure 14. NBSFDR, f_{OUT} = 75.1 MHz, f_{CLK} = 500 MSPS, ±1 MHz

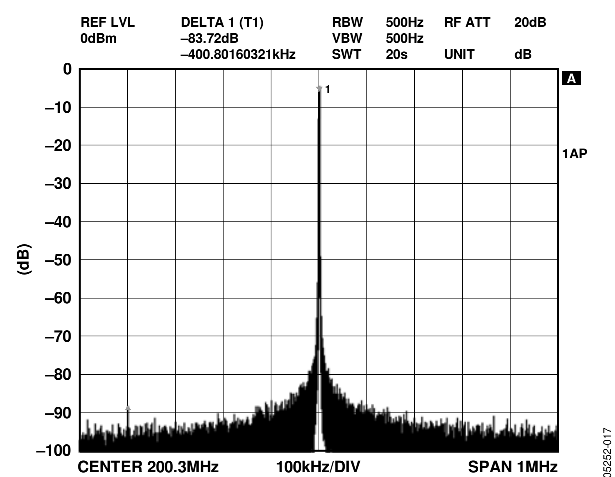


Figure 15. NBSFDR f_{OUT} = 200. 3MHz, f_{CLK} = 500 MSPS, , ±1 MHz

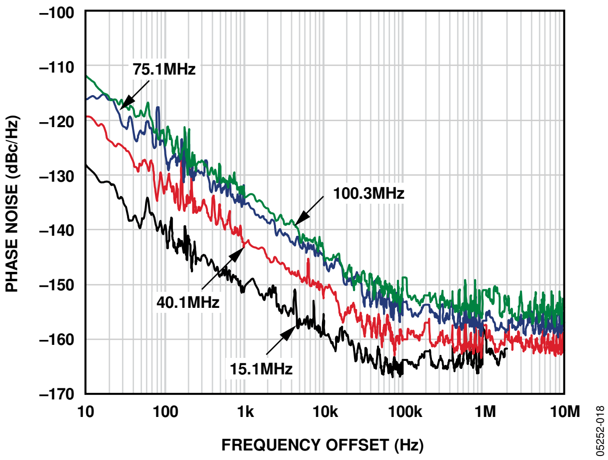


Figure 16. Residual Phase Noise (SSB) with f_{OUT} = 15.1 MHz, 40.1MHz, 75.1 MHz, 100.3 MHz; f_{CLK} = 500 MHz with REFCLK Multiplier Bypassed

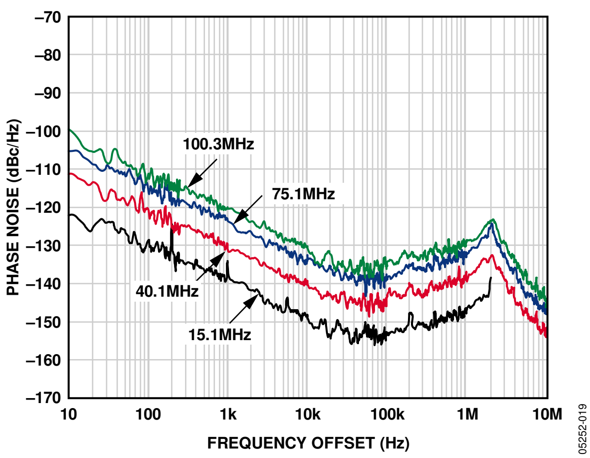


Figure 17. Residual Phase Noise (SSB) with f_{OUT} = 15.1 MHz, 40.1MHz, 75.1 MHz, 100.3 MHz; f_{CLK} = 500 MHz with REFCLK Multiplier = 5×

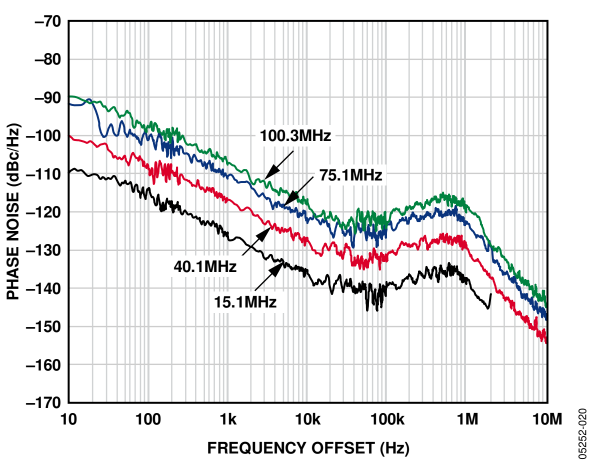


Figure 18. Residual Phase Noise (SSB) with f_{OUT} = 15.1 MHz, 40.1MHz, 75.1 MHz,100.3 MHz; f_{CLK} = 500 MHz with REFCLK Multiplier = 20×

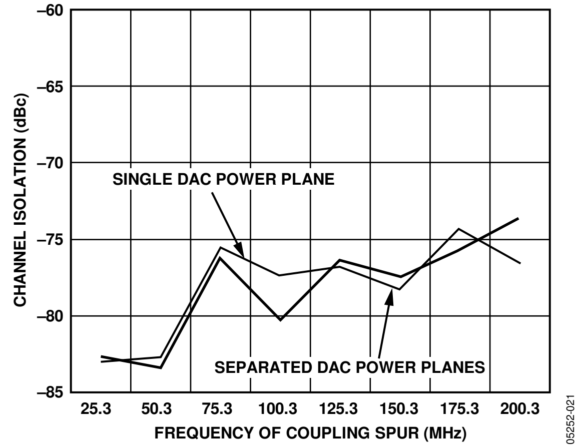


Figure 19. Channel Isolation at 500 MSPS Operation; Conditions are Channel of Interest Fixed at 110.3 MHz, the Other Channels Are Frequency Swept

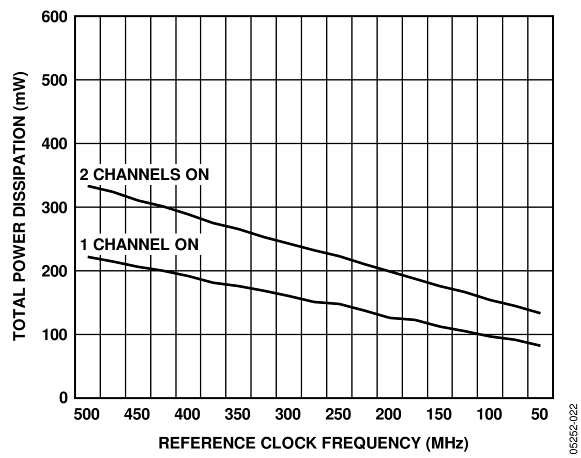


Figure 20. Power Dissipation vs. Reference Clock Frequency vs. Channel(s) Power On/Off

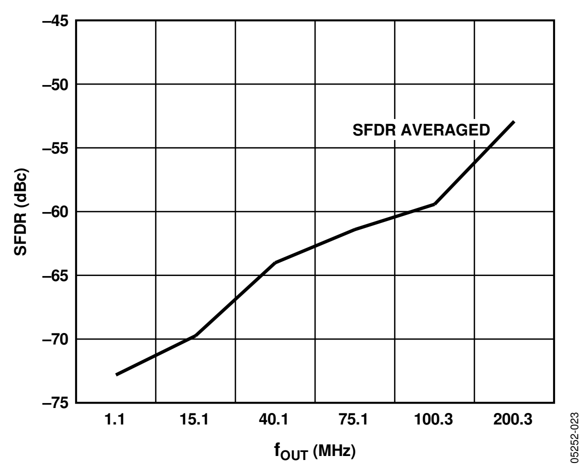


Figure 21. Averaged Channel SFDR vs. f_{OUT}

APPLICATION CIRCUITS

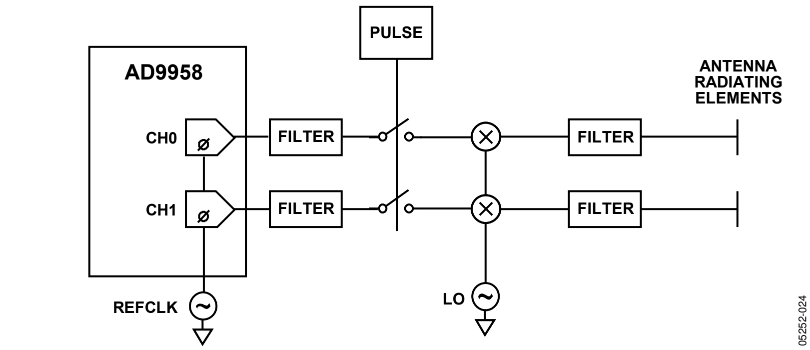


Figure 22. Phase Array Radar Using Precision Frequency/Phase Control from DDS in FMCW or Pulsed Radar Applications; DDS Provides Either Continuous Wave or Frequency Sweep

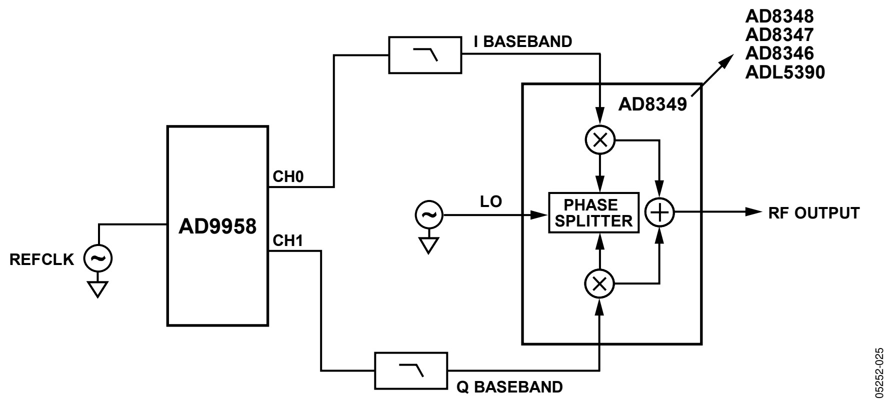


Figure 23. Single-Sideband-Suppressed Carrier Upconversion

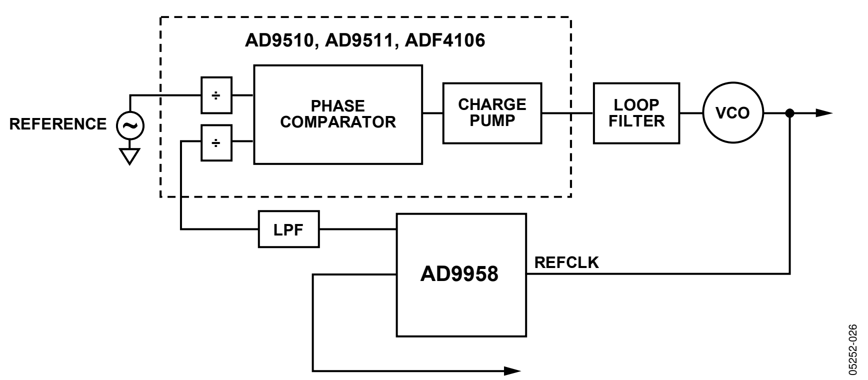


Figure 24. DDS in PLL Locking to Reference Offering Distribution with Fine Frequency and Delay Adjust Tuning

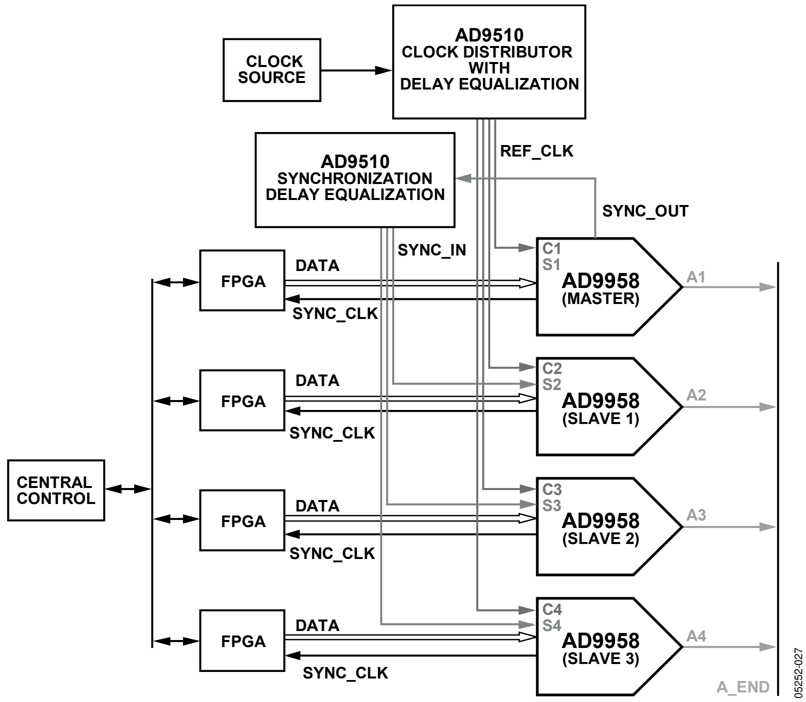


Figure 25. Synchronizing Multiple Devices to Increase Channel Capacity Using the AD9510 as a Clock Distributor for the Reference and SYNC_CLK

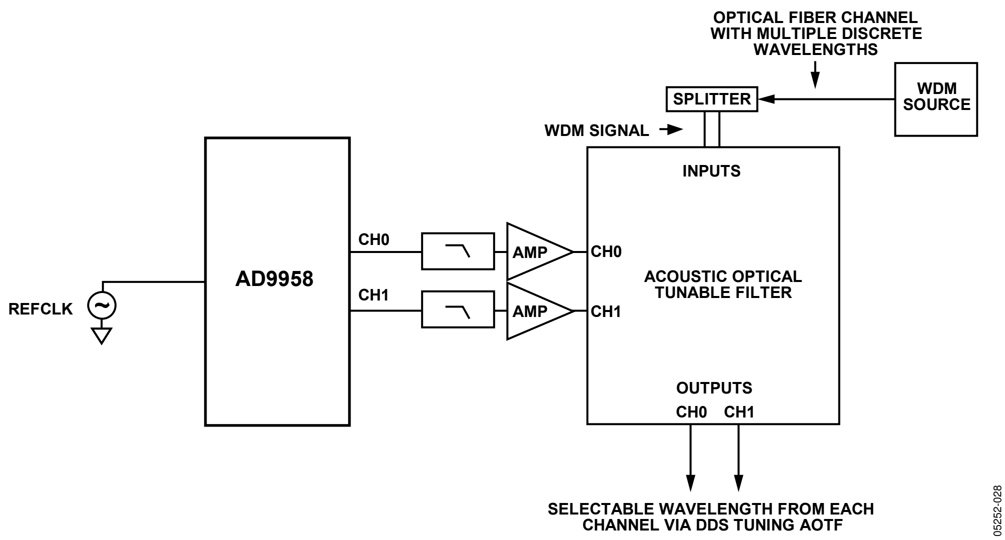


Figure 26. DDS Providing Stimulus for Acoustic Optical Tunable Filter

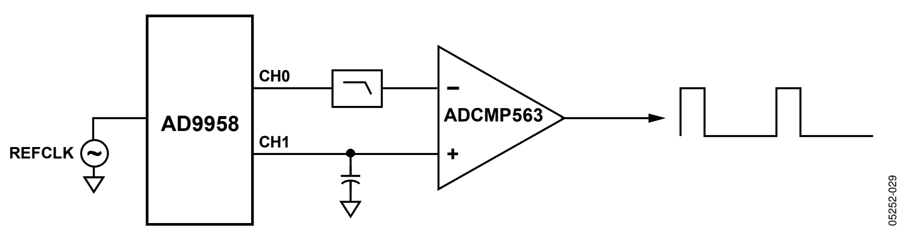


Figure 27. Agile Clock Source with Duty Cycle Control Using the Phase Offset Value in DDS to Change the DC Voltage to the Comparator

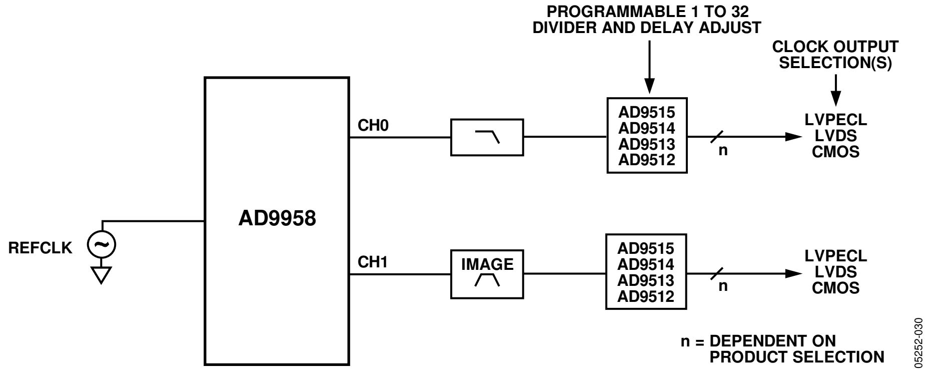


Figure 28. Clock Generation Circuit Using the AD9512/AD9513/AD9514/AD9515 Series of Clock Distribution Chips

EQUIVALENT INPUT AND OUTPUT CIRCUITS

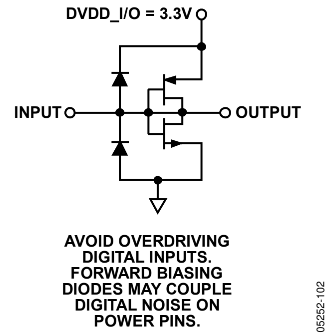


Figure 29. CMOS Digital Inputs

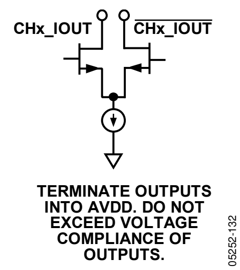


Figure 30. DAC Outputs

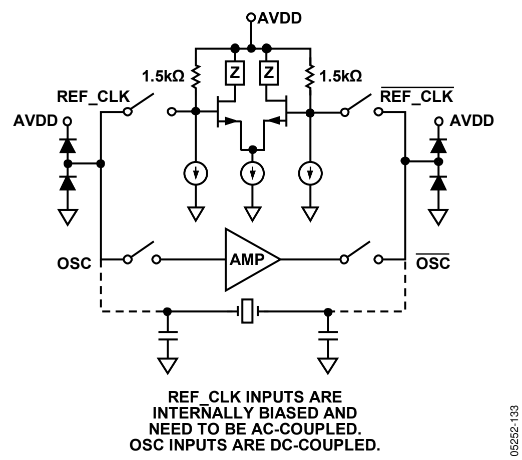


Figure 31. REF_CLK/$\overline{\text{REF\_CLK}}$ Inputs

THEORY OF OPERATION

DDS CORE

The AD9958 has two DDS cores, each consisting of a 32-bit phase accumulator and phase-to-amplitude converter. Together, these digital blocks generate a digital sine wave when the phase accumulator is clocked and the phase increment value (frequency tuning word) is greater than 0. The phase-to-amplitude converter simultaneously translates phase information to amplitude information by a cos(θ) operation.

The output frequency (f_{OUT}) of each DDS channel is a function of the rollover rate of each phase accumulator. The exact relationship is given in the following equation:

$$f_{OUT} = \frac{(FTW)(f_S)}{2^{32}}$$

where:
f_S is the system clock rate.
FTW is the frequency tuning word and is $0 \leq FTW \leq 2^{31}$.
2^{32} represents the phase accumulator capacity.

Because both channels share a common system clock, they are inherently synchronized.

The DDS core architecture also supports the capability to phase offset the output signal, which is performed by the channel phase offset word (CPOW). The CPOW is a 14-bit register that stores a phase offset value. This value is added to the output of the phase accumulator to offset the current phase of the output signal. Each channel has its own phase offset word register. This feature can be used for placing all channels in a known phase relationship relative to one another. The exact value of phase offset is given by the following equation:

$$\Phi = \left(\frac{POW}{2^{14}}\right) \times 360°$$

DIGITAL-TO-ANALOG CONVERTER

The AD9958 incorporates four 10-bit current output DACs. The DAC converts a digital code (amplitude) into a discrete analog quantity. The DAC current outputs can be modeled as a current source with high output impedance (typically 100 kΩ). Unlike many DACs, these current outputs require termination into AVDD via a resistor or a center-tapped transformer for expected current flow.

Each DAC has complementary outputs that provide a combined full-scale output current ($I_{OUT} + I_{\overline{OUT}}$). The outputs always sink current, and their sum equals the full-scale current at any point in time. The full-scale current is controlled by means of an external resistor (R_{SET}) and the scalable DAC current control bits discussed in the Modes of Operation section. The resistor, R_{SET}, is connected between the DAC_RSET pin and analog ground (AGND). The full-scale current is inversely proportional to the resistor value as follows:

$$R_{SET} = \frac{18.91}{I_{OUT}\ (\max)}$$

The maximum full-scale output current of the combined DAC outputs is 15 mA, but limiting the output to 10 mA provides optimal spurious-free dynamic range (SFDR) performance. The DAC output voltage compliance range is AVDD + 0.5 V to AVDD − 0.5 V. Voltages developed beyond this range may cause excessive harmonic distortion. Proper attention should be paid to the load termination to keep the output voltage within its compliance range. Exceeding this range could potentially damage the DAC output circuitry.

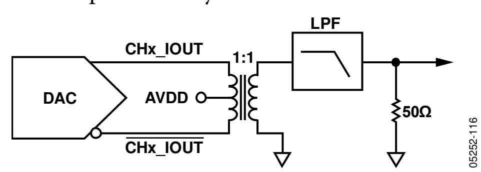


Figure 32. Typical DAC Output Termination Configuration

MODES OF OPERATION

There are many combinations of modes (for example, single-tone, modulation, linear sweep) that the AD9958 can perform simultaneously. However, some modes require multiple data pins, which can impose limitations. The following guidelines can help determine if a specific combination of modes can be performed simultaneously by the AD9958.

CHANNEL CONSTRAINT GUIDELINES

- Single-tone mode, two-level modulation mode, and linear sweep mode can be enabled on either channel and in any combination simultaneously.
- Both channels can perform four-level modulation simultaneously.
- Either channel can perform eight-level or 16-level modulation. The other channel can only be in single-tone mode.
- The RU/RD function can be used on both channels in single-tone mode. See the Output Amplitude Control Mode section for the RU/RD function.
- When Profile Pin P2 and Profile Pin P3 are used for RU/RD, either channel can perform two-level modulation with RU/RD or both channels can perform linear frequency or phase sweep with RU/RD.
- When Profile Pin P3 is used for RU/RD, either channel can be used in eight-level modulation with RU/RD. The other channel can only be in single-tone mode.
- When SDIO_1, SDIO_2, and SDIO_3 pins are used for RU/RD, either or both channels can perform two-level modulation with RU/RD. If one channel is not in two-level modulation, it can only be in single-tone mode.
- When the SDIO_1, SDIO_2, and SDIO_3 pins are used for RU/RD, either or both channels can perform four-level modulation with RU/RD. If one channel is not in four-level modulation, it can only be in single-tone mode.
- When the SDIO_1, SDIO_2, and SDIO_3 pins are used for RU/RD, either channel can perform eight-level modulation with RU/RD. The other channel can only be in single-tone mode.
- When the SDIO_1, SDIO_2, and SDIO_3 pins are used for RU/RD, either channel can perform 16-level modulation with RU/RD. The other channel can only be in single-tone mode.
- Amplitude modulation, linear amplitude sweep modes, and the RU/RD function cannot operate simultaneously, but frequency and phase modulation can operate simultaneously with the RU/RD function.

POWER SUPPLIES

The AVDD and DVDD supply pins provide power to the DDS core and supporting analog circuitry. These pins connect to a 1.8 V nominal power supply.

The DVDD_I/O pin connects to a 3.3 V nominal power supply. All digital inputs are 3.3 V logic except for the CLK_MODE_SEL input. CLK_MODE_SEL (Pin 24) is an analog input and should be operated by 1.8 V logic.

SINGLE-TONE MODE

Single-tone mode is the default mode of operation after a master reset signal. In this mode, both DDS channels share a common address location for the frequency tuning word (Register 0x04) and phase offset word (Register 0x05). Channel enable bits are provided in combination with these shared addresses. As a result, the frequency tuning word and/or phase offset word can be independently programmed between channels (see the following Step 1 through Step 5). The channel enable bits do not require an I/O update to enable or disable a channel.

See the Register Maps and Bit Descriptions section for a description of the channel enable bits in the channel select register (CSR, Register 0x00). The channel enable bits are enabled or disabled immediately after the CSR data byte is written.

Address sharing enables channels to be written simultaneously, if desired. The default state enables all channel enable bits. Therefore, the frequency tuning word and/or phase offset word is common to all channels but written only once through the serial I/O port.

The following steps present a basic protocol to program a different frequency tuning word and/or phase offset word for each channel using the channel enable bits.

1. Power up the DUT and issue a master reset. A master reset places the part in single-tone mode and single-bit mode for serial programming operations (refer to the Serial I/O Modes of Operation section). Frequency tuning words and phase offset words default to 0 at this point.
2. Enable only one channel enable bit (Register 0x00) and disable the other channel enable bit.
3. Using the serial I/O port, program the desired frequency tuning word (Register 0x04) and/or the phase offset word (Register 0x05) for the enabled channel.
4. Repeat Step 2 and Step 3 for each channel.
5. Send an I/O update signal. After an I/O update, all channels should output their programmed frequency and/or phase offset values.

Single-Tone Mode—Matched Pipeline Delay

In single-tone mode, the AD9958 offers matched pipeline delay to the DAC input for all frequency, phase, and amplitude changes. This avoids having to deal with different pipeline delays between the three input ports for such applications. The feature is enabled by asserting the matched pipe delays active bit found in the channel function register (CFR, Register 0x03). This feature is available in single-tone mode only.

REFERENCE CLOCK MODES

The AD9958 supports multiple reference clock configurations to generate the internal system clock. As an alternative to clocking the part directly with a high frequency clock source, the system clock can be generated using the internal, PLL-based reference clock multiplier. An on-chip oscillator circuit is also available for providing a low frequency reference signal by connecting a crystal to the clock input pins. Enabling these features allows the part to operate with a low frequency clock source and still provide a high update rate for the DDS and DAC. However, using the clock multiplier changes the output phase noise characteristics. For best phase noise performance, a clean, stable clock with a high slew is required (see Figure 17 and Figure 18).

Enabling the PLL allows multiplication of the reference clock frequency from 4× to 20×, in integer steps. The PLL multiplication value is represented by a 5-bit multiplier value. These bits are located in Function Register 1 (FR1, Register 0x01), Bits[22:18] (see the Register Maps and Bit Descriptions section).

When FR1[22:18] is programmed with values ranging from 4 to 20 (decimal), the clock multiplier is enabled. The integer value in the register represents the multiplication factor. The system clock rate with the clock multiplier enabled is equal to the reference clock rate multiplied by the multiplication factor. If FR1[22:18] is programmed with a value less than 4 or greater than 20, the clock multiplier is disabled and the multiplication factor is effectively 1.

Whenever the PLL clock multiplier is enabled or the multiplication value is changed, time should be allowed to lock the PLL (typically 1 ms).

Note that the output frequency of the PLL is restricted to a frequency range of 100 MHz to 500 MHz. However, there is a VCO gain control bit that must be used appropriately. The VCO gain control bit defines two ranges (low/high) of frequency output. The VCO gain control bit defaults to low (see Table 1 for details).

The charge pump current in the PLL defaults to 75 µA. This setting typically produces the best phase noise characteristics. Increasing the charge pump current may degrade phase noise, but it decreases the lock time and changes the loop bandwidth.

Enabling the on-chip oscillator for crystal operation is performed by driving CLK_MODE_SEL (Pin 24) to logic high (1.8 V logic). With the on-chip oscillator enabled, connection of an external crystal to the REF_CLK and $\overline{\text{REF\_CLK}}$ inputs is made, producing a low frequency reference clock. The frequency of the crystal must be in the range of 20 MHz to 30 MHz.

Table 4 summarizes the clock modes of operation. See Table 1 for more details.

Reference Clock Input Circuitry

The reference clock input circuitry has two modes of operation controlled by the logic state of Pin 24 (CLK_MODE_SEL). The first mode (logic low) configures as an input buffer. In this mode, the reference clock must be ac-coupled to the input due to internal dc biasing. This mode supports either differential or single-ended configurations. If single-ended mode is chosen, the complementary reference clock input (Pin 22) should be decoupled to AVDD or AGND via a 0.1 µF capacitor. Figure 33 to Figure 35 exemplify typical reference clock configurations for the AD9958.

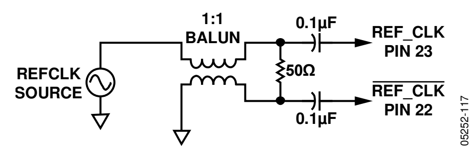


Figure 33. Differential Coupling from Single-Ended Source

The reference clock inputs can also support an LVPECL or PECL driver as the reference clock source.

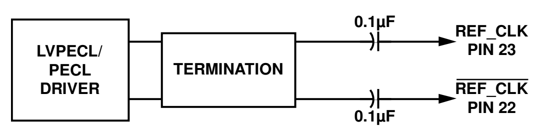


Figure 34. Differential Clock Source Hook-Up

The second mode of operation (Pin 24 = logic high = 1.8 V) provides an internal oscillator for crystal operation. In this mode, both clock inputs are dc-coupled via the crystal leads and are bypassed. The range of crystal frequencies supported is from 20 MHz to 30 MHz. Figure 35 shows the configuration for using a crystal.

Table 4. Clock Configuration

CLK_MODE_SEL, Pin 24	FR1[22:18] PLL Divider Ratio = M	Crystal Oscillator Enabled	System Clock (f_{SYSCLK})	Min/Max Freq. Range (MHz)
High = 1.8 V Logic	4 ≤ M ≤ 20	Yes	$f_{SYSCLK} = f_{OSC} \times M$	100 < f_{SYSCLK} < 500
High = 1.8 V Logic	M < 4 or M > 20	Yes	$f_{SYSCLK} = f_{OSC}$	20 < f_{SYSCLK} < 30
Low	4 ≤ M ≤ 20	No	$f_{SYSCLK} = f_{REFCLK} \times M$	100 < f_{SYSCLK} < 500
Low	M < 4 or M > 20	No	$f_{SYSCLK} = f_{REFCLK}$	0 < f_{SYSCLK} < 500

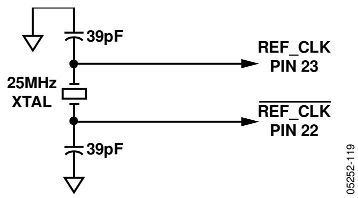


Figure 35. Crystal Input Configuration

SCALABLE DAC REFERENCE CURRENT CONTROL MODE

R_{SET} is common to all four DACs. As a result, the full-scale currents are equal by default. The scalable DAC reference can be used to set the full-scale current of each DAC independent from one another. This is accomplished by using the register bits CFR[9:8]. Table 5 shows how each DAC can be individually scaled for independent channel control. This scaling provides for binary attenuation.

Table 5. DAC Full-Scale Current Control

CFR[9:8]	LSB Current State
11	Full scale
01	Half scale
10	Quarter scale
00	Eighth scale

POWER-DOWN FUNCTIONS

The AD9958 supports an externally controlled power-down feature and the more common software programmable power-down bits found in previous Analog Devices DDS products.

The software control power-down allows the input clock circuitry, the DAC, and the digital logic (for each separate channel) to be individually powered down via unique control bits (CFR[7:6]). These bits are not active when the externally controlled power-down pin (PWR_DWN_CTL) is high. When the input pin, PWR_DWN_CTL, is high, the AD9958 enters a power-down mode based on the FR1[6] bit. When the PWR_DWN_CTL input pin is low, the external power-down control is inactive.

When FR1[6] = 0 and the PWR_DWN_CTL input pin is high, the AD9958 is put into a fast recovery power-down mode. In this mode, the digital logic and the DAC digital logic are powered down. The DAC bias circuitry, PLL, oscillator, and clock input circuitry are not powered down.

When FR1[6] = 1 and the PWR_DWN_CTL input pin is high, the AD9958 is put into full power-down mode. In this mode, all functions are powered down. This includes the DAC and PLL, which take a significant amount of time to power up. When the PLL is bypassed, the PLL is shut down to conserve power.

When the PWR_DWN_CTL input pin is high, the individual power-down bits (CFR[7:6]) and (FR1[7]) are invalid (don't care) and unused. When the PWR_DWN_CTL input pin is low, the individual power-down bits control the power-down modes of operation.

Note that the power-down signals are all designed such that Logic 1 indicates the low power mode and Logic 0 indicates the powered-up mode.

MODULATION MODE

The AD9958 can perform 2-/4-/8-/16-level modulation of frequency, phase, or amplitude. Modulation is achieved by applying data to the profile pins. Each channel can be programmed separately, but the ability to modulate multiple channels simultaneously is constrained by the limited number of profile pins. For instance, 16-level modulation uses all four profile pins, which inhibits modulation for the remaining channel.

In addition, the AD9958 has the ability to ramp up or ramp down the output amplitude before, during, or after a modulation (FSK, PSK only) sequence. This is performed by using the 10-bit output scalar. If the RU/RD feature is desired, unused profile pins or unused SDIO_1/SDIO_2/SDIO_3 pins can be configured to initiate the operation. See the Output Amplitude Control Mode section for more details of the RU/RD feature.

In modulation mode, each channel has its own set of control bits to determine the type (frequency, phase, or amplitude) of modulation. Each channel has 16 profile (channel word) registers for flexibility. Register 0x0A through Register 0x18 are profile registers for modulation of frequency, phase, or amplitude. Register 0x04, Register 0x05, and Register 0x06 are dedicated registers for frequency, phase, and amplitude, respectively. These registers contain the first frequency, phase offset, and amplitude word.

Frequency modulation has 32-bit resolution, phase modulation is 14 bits, and amplitude is 10 bits. When modulating phase or amplitude, the word value must be MSB aligned in the profile (channel word) registers and the unused bits are don't care bits.

In modulation mode, the amplitude frequency phase (AFP) select bits (CFR[23:22]) and modulation level bits (FR1[9:8]) are programmed to configure the modulation type and level (see Table 6 and Table 7). Note that the linear sweep enable bit must be set to Logic 0 in direct modulation mode.

Table 6. Modulation Type Configuration

AFP Select (CFR[23:22])	Linear Sweep Enable (CFR[14])	Description
00	X	Modulation disabled
01	0	Amplitude modulation
10	0	Frequency modulation
11	0	Phase modulation

Table 7. Modulation Level Selection

Modulation Level (FR1[9:8])	Description
00	Two-level modulation
01	Four-level modulation
10	Eight-level modulation
11	16-level modulation

When modulating, the RU/RD function can be limited based on pins available for controlling the feature. The SDIO_x pins are for RU/RD only, not for modulation.

Table 8. RU/RD Profile Pin Assignments

Ramp-Up/Ramp-Down (RU/RD) (FR1[11:10])	Description
00	RU/RD disabled
01	Only Profile Pin P2 and Profile Pin P3 available for RU/RD operation
10	Only Profile Pin P3 available for RU/RD operation
11	Only SDIO_1, SDIO_2, and SDIO_3 pins available for RU/RD operation; this forces the serial I/O to be used only in 1-bit mode

If the profile pins are used for RU/RD, Logic 0 is for ramp-up and Logic 1 is for ramp-down.

Because of the two channels and limited data pins, it is necessary to assign the profile pins and/or SDIO_1, SDIO_2, and SDIO_3 pins to a dedicated channel. This is controlled by the profile pin configuration (PPC) bits (FR1[14:12]). Each of the following modulation descriptions incorporates data pin assignments.

Two-Level Modulation—No RU/RD

The modulation level bits (FR1[9:8]) are set to 00 (two-level). The AFP select bits (CFR[23:22]) are set to the desired modulation type. The RU/RD bits (FR1[11:10]) and the linear sweep enable bit (CFR[14]) are disabled. Table 9 displays how the profile pins and channels are assigned.

As shown in Table 9, only Profile Pin P2 can be used to modulate Channel 0. If frequency modulation is selected and Profile Pin P2 is Logic 0, Channel Frequency Tuning Word 0 (Register 0x04) is chosen; if Profile Pin P2 is Logic 1, Channel Word 1 (Register 0x0A) is chosen.

Four-Level Modulation—No RU/RD

The modulation level bits are set to 01 (four-level). The AFP select bits (CFR[23:22]) are set to the desired modulation type. The RU/RD bits (FR1[11:10]) and the linear sweep enable bit (CFR[14]) are disabled. Table 10 displays how the profile pins and channels are assigned to each other.

For the conditions in Table 10, the profile (channel word) register chosen is based on the 2-bit value presented to Profile Pins [P0:P1] or Profile Pins [P2:P3].

For example, if PPC = 101, [P0:P1] = 11, and [P2:P3] = 01, then the contents of the Channel Word 3 register of Channel 0 are presented to the output of Channel 0 and the contents of the Channel Word 1 register of Channel 1 are presented to the output of Channel 1.

Table 9. Profile Pin Channel Assignments

Profile Pin Configuration (PPC) (FR1[14:12])	P0	P1	P2	P3	Description
XXX	N/A	N/A	CH0	CH1	Two-level modulation, both channels, no RU/RD

Table 10. Profile Pin and Channel Assignments

Profile Pin Configuration (PPC) (FR1[14:12])	P0	P1	P2	P3	Description
101	CH0	CH0	CH1	CH1	Four-level modulation on CH0 and CH1, no RU/RD

Eight-Level Modulation—No RU/RD

The modulation level bits (FR1[9:8]) are set to 10 (eight-level). The AFP select bits (CFR[23:22]) are set to a nonzero value. The RU/RD bits (FR1[11:10]) and the linear sweep enable bit (CFR[14]) are disabled. Note that the AFP select bits of the other channel not being used must be set to 00. Table 11 shows the assignment of profile pins and channels.

For the condition in Table 11, the choice of channel word registers is based on the 3-bit value presented to Profile Pins [P0:P2]. For example, if PPC = X10 and [P0:P2] = 111, the contents of the Channel Word 7 register of Channel 0 are presented to the output Channel 0.

16-Level Modulation—No RU/RD

The modulation level bits (FR1[9:8]) are set to 11 (16-level). The AFP select bits (CFR[23:22]) are set to the desired modulation type. The RU/RD bits (FR1[11:10]) and the linear sweep enable bit (CFR[14]) are disabled. The AFP select bits of the other channel not being used must be set to 00. Table 12 displays how the profile pins and channels are assigned.

For the conditions in Table 12, the profile register chosen is based on the 4-bit value presented to Profile Pins [P0:P3]. For example, if PPC = X11 and [P0:P3] = 1110, the contents of the Channel Word 14 register of Channel 1 is presented to the output of Channel 1.

Two-Level Modulation Using Profile Pins for RU/RD

When the RU/RD bits = 01, Profile Pin P2 and Profile Pin P3 are available for RU/RD. Note that only a modulation level of two is available in this mode. See Table 13 for available pin assignments.

Eight-Level Modulation Using a Profile Pin for RU/RD

When the RU/RD bits = 10, Profile Pin P3 is available for RU/RD. Note that only a modulation level of eight is available in this mode. See Table 14 for available pin assignments.

Table 11. Profile Pin and Channel Assignments for Eight-Level Modulation (No RU/RD)

Profile Pin Config. (PPC) (FR1[14:12])	P0	P1	P2	P3	Description
X10	CH0	CH0	CH0	X	Eight-level modulation on CH0, no RU/RD
X11	CH1	CH1	CH1	X	Eight-level modulation on CH1, no RU/RD

Table 12. Profile Pin and Channel Assignments for 16-Level Modulation (No RU/RD)

Profile Pin Config. (PPC) (FR1[14:12])	P0	P1	P2	P3	Description
X10	CH0	CH0	CH0	CH0	16-level modulation on CH0, no RU/RD
X11	CH1	CH1	CH1	CH1	16-level modulation on CH1, no RU/RD

Table 13. Profile Pin and Channel Assignments for Two-Level Modulation (RU/RD Enabled)

Profile Pin Config. (PPC) (FR1[14:12])	P0	P1	P2	P3	Description
101	CH0	CH1	CH0 RU/RD	CH1 RU/RD	Two-level modulation on CH0 and CH1 with RU/RD

Table 14. Profile Pin and Channel Assignments for Eight-Level Modulation (RU/RD Enabled)

Profile Pin Config. (PPC) (FR1[14:12])	P0	P1	P2	P3	Description
X10	CH0	CH0	CH0	CH0 RU/RD	Eight-level modulation on CH0 with RU/RD
X11	CH1	CH1	CH1	CH1 RU/RD	Eight-level modulation on CH1 with RU/RD