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10-/12-Bit, Low Power, Broadband MxFE

Data Sheet

AD9961/AD9963

FEATURES

Dual 10-bit/12-bit, 100 MSPS ADC
SNR = 67 dB, f_{IN} = 30.1 MHz
Dual 10-bit/12-bit, 170 MSPS DAC
ACLR = 74 dBc
5 channels of analog auxiliary input/output
Low power, <425 mW at maximum sample rates
Supports full and half-duplex data interfaces
Small 72-lead LFCSP lead-free package

APPLICATIONS

Wireless infrastructure
Picocell, femtocell basestations
Medical instrumentation
Ultrasound AFE
Portable instrumentation
Signal generators, signal analyzers

GENERAL DESCRIPTION

The AD9961/AD9963 are pin-compatible, 10-/12-bit, low power MxFE® converters that provide two ADC channels with sample rates of 100 MSPS and two DAC channels with sample rates to 170 MSPS. These converters are optimized for transmit and receive signal paths of communication systems requiring low power and low cost. The digital interfaces provide flexible clocking options. The transmit is configurable for 1×, 2×, 4×, and 8× interpolation. The receive path has a bypassable 2× decimating low-pass filter.

The AD9961 and AD9963 have five auxiliary analog channels. Three are inputs to a 12-bit ADC. Two of these inputs can be configured as outputs by enabling 10-bit DACs. The other two channels are dedicated outputs from two independent 12-bit DACs.

The high level of integrated functionality, small size, and low power dissipation of the AD9961/AD9963 make them well-suited for portable and low power applications.

FUNCTIONAL BLOCK DIAGRAM

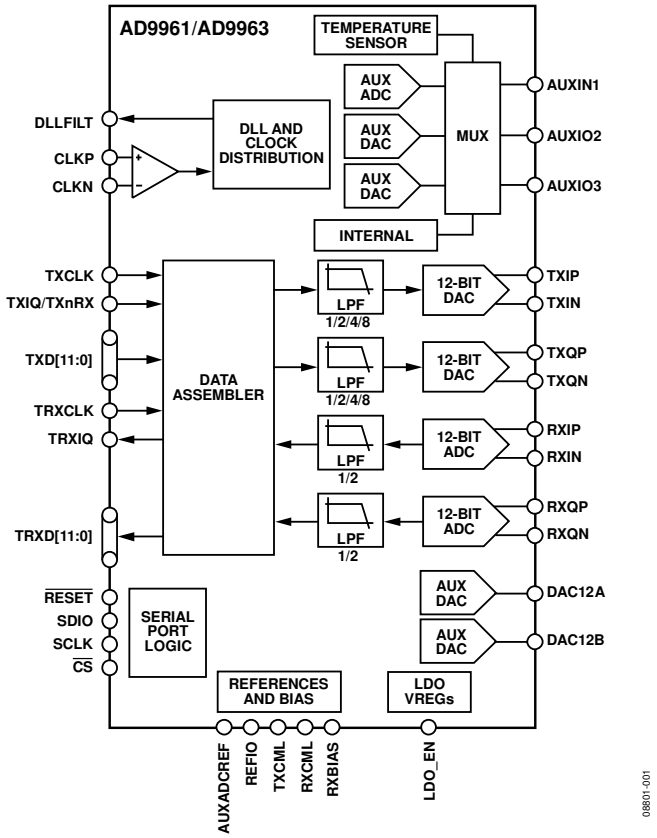

Figure 1.

PRODUCT HIGHLIGHTS

1. High Performance with Low Power Consumption.
   The DACs operate on a single 1.8 V to 3.3 V supply. Transmit path power consumption is <100 mW at 170 MSPS. Receive path power consumption is <350 mW at 100 MSPS from 1.8 V supply. Sleep and power-down modes are provided for low power idle periods.
2. High Integration.
   The dual transmit and dual receive data converters, five channels of auxiliary data conversion and clock generation offer complete solutions for many modem designs.
3. Flexible Digital Interface.
   The interface mates seamlessly to most digital baseband processors.

Rev. A

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7/10—Revision 0: Initial Version

SPECIFICATIONS

T_{MIN} to T_{MAX}, RX33V = TXVDD = CLK33V = DRVDD = AUX33V = 3.3 V. All LDOs enabled, I_{OUTFS} = 2 mA, DAC sample rate = 125 MSPS. No interpolation, unless otherwise noted.

Table 1. Tx Path Specifications

	AD9961			AD9963			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
TxDAC DC CHARACTERISTICS							
Resolution		10			12		Bits
Differential Nonlinearity		0.1			0.3		LSB
Gain Variation (Internal Reference)	−10	0.4	+10	−10	0.4	+10	%FSR
Gain Matching	−2.4	0.4	+2.4	−2.4	0.4	+2.4	%FSR
Offset Error	−0.03		+0.03	−0.03		+0.03	%FSR
Full-Scale Output Current (Default Setting)		2.0			2.0		mA
Output Compliance Range							
TXVDD = 3.3 V, V_{TXCML} = 0 V	−0.5		+1.0	−0.5		+1.0	V
TXVDD = 3.3 V, V_{TXCML} = 0.5 V	+0.7		+1.7	+0.7		+1.7	V
TXVDD = 1.8 V, V_{TXCML} = 0 V	−0.5		+0.8	−0.5		+0.8	V
Offset Temperature Drift		0			0		ppm/°C
Gain Temperature Drift (Internal Reference)		±40			±40		ppm/°C
Tx REFERENCE (DEFAULT REGISTER SETTINGS)							
Internal Reference Voltage (REFIO)		1.02			1.02		V
Output Resistance		10			10		kΩ
Temperature Drift		±25			±25		ppm/°C
Adjustment Range (TXVDD = 3 V)	0.8		1.2	0.8		1.2	V
Adjustment Range (TXVDD = 1.8 V)	0.8		REFIO	0.8		REFIO	V
TxDAC AC CHARACTERISTICS							
Maximum Update Rate	175			175			MSPS
Spurious-Free Dynamic Range							
f_{OUT} = 5 MHz		78			81		dBc
f_{OUT} = 20 MHz		68			70		dBc
Two-Tone Intermodulation Distortion							
f_{OUT1} = 5 MHz, f_{OUT2} = 6 MHz		85			89		dBc
f_{OUT1} = 20 MHz, f_{OUT2} = 21 MHz		78			80		dBc
Noise Spectral Density							
f_{OUT} = 5 MHz		−140			−145		dBm/Hz
f_{OUT} = 20 MHz		−136			−141		dBm/Hz
W-CDMA Adjacent Channel Leakage Ratio, 1 Carrier							
f_{DAC} = 122.88 MHz, f_{OUT} = 11 MHz		70			74		dBc
Tx PATH DIGITAL FILTER INPUT RATES							
SRRC (8× Interpolation Mode)	21.875			21.875			MHz
INT0 (4× Interpolation Mode)	43.75			43.75			MHz
INT1 (2× Interpolation Mode	87.5			87.5			MHz
Transmit DAC (1× Interpolation Mode)	175			175			MHz

T_{MIN} to T_{MAX}, RX33V = TXVDD = CLK33V = DRVDD = AUX33V = 3.3 V. All LDOs enabled, ADC sample rate = 100 MSPS. No decimation, unless otherwise noted.

Table 2. Rx Path Specifications

	AD9961			AD9963			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Rx ADC DC CHARACTERISTICS							
Resolution		10			12		Bits
Differential Nonlinearity		0.1			0.3		LSB
Gain Error		±1			±1		%FSR
Offset Error		±0.5			±0.5		%FSR
Input Voltage Range		1.56			1.56		V p-p diff
Input Capacitance		8			8		pF
Rx ADC AC SPECIFICATIONS							
Maximum Sample Rate	100			100			MSPS
Spurious Free Dynamic Range							
f_{IN} = 10.1 MHz		77			77		dBc
f_{IN} = 70.1 MHz		75			73		dBc
Two-Tone Intermodulation Distortion							
f_{IN1} = 10 MHz, f_{IN2} = 11 MHz		78			82		dBc
f_{IN1} = 29 MHz, f_{IN2} = 32 MHz		76			80		dBc
Signal-to-Noise Ratio							
f_{IN} = 10.1 MHz		61			68		dBFS
f_{IN} = 30.1 MHz		60			67		dBFS
f_{IN} = 70.1 MHz		60			66		dBFS
RXCML OUTPUTS							
Output Voltage		1.4			1.4		V
Output Current			0.1			0.1	mA
Rx DIGITAL FILTER CHARACTERISTICS							
2× Decimation							
Latency (ADC Clock Cycles)	49			49			Cycles
Passband Ripple; f_{OUT}/f_{DAC} ($0.4 \times f_{DATA}$)	0.2			0.2			f_{OUT}/f_{DAC}
Stop-Band Rejection ($f_{DATA} \pm 0.4 \times f_{DATA}$)	70			70			dB

T_{MIN} to T_{MAX}, RX33V = TXVDD = CLK33V = DRVDD = AUX33V = 3.3 V. All LDOs enabled, unless otherwise noted.

Table 3. Auxiliary Converter Specifications

	AD9961			AD9963			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
AUXILIARY DAC12A/AUXDAC12B							
Resolution	12			12			Bits
Differential Nonlinearity		±0.8			±0.8		LSB
Gain Error		±2.0			±2.0		%
Settling Time (±1%)		1			1		µs
AUXILIARY DAC10A/DAC10B (Range = 0.5 V to 1.5 V)							
Resolution	10			10			Bits
Differential Nonlinearity		±1.0			±1.0		LSB
Gain Error		±2.0			±2.0		%
Settling Time (±1%)		10			10		µs
AUXILIARY ADC							
Resolution	12			12			Bits
Differential Nonlinearity	−1.0		+1.0	−1.0		+1.0	LSB
Gain Error (Internal Reference)	−2.0		+2.0	−2.0		+2.0	%
Input Voltage Range	0		3.2	0		3.2	V
Maximum Sample Rate	50			50			kHz

f_{CLK} = 125 MHz, f_{DLL} = 250 MHz, DAC sample rate = 125 MSPS, ADC sample rate = 62.5 MSPS, unless otherwise noted.

Table 4. Power Consumption Specifications

	AD9961			AD9963			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
1.8 V ONLY OPERATION (EXTERNAL 1.8 V)							
CLK33V		1.65			1.65		mA
TXVDD		10.7			10.7		mA
DRVDD		29.4			34.9		mA
DVDD18V		21.0			22.7		mA
CLK18V		3.84			3.84		mA
DLL18V		9.98			9.98		mA
RX18V		79.2			79.2		mA
RX18VF		34.3			34.3		mA
3.3 V ONLY OPERATION (ON-CHIP REGULATORS)							
TXVDD		12.1			12.1		mA
CLK33V		17.0			17.0		mA
RX33V		113			113		mA
DRVDD		93			108		mA
AUX33V		0.55			0.55		mA
SUPPLY VOLTAGE RANGE							
CLK33V, TXVDD (These Supplies Must Be Tied Together)	1.72		3.63	1.72		3.63	V
DRVDD	1.72		3.63	1.72		3.63	V
DVDD18V	1.72		1.89	1.72		1.89	V
CLK18V	1.72		1.89	1.72		1.89	V
DLL18V	1.72		1.89	1.72		1.89	V
RX18V	1.72		1.89	1.72		1.89	V
RX18VF	1.72		1.89	1.72		1.89	V
RX33V	2.50		3.63	2.50		3.63	V
AUX33V (AUXADC Enabled)	3.14		3.63	3.14		3.63	V
AUX33V (AUXADC Disabled)	1.72		3.63	1.72		3.63	V

Table 5. Digital Logic Level Specifications

Parameter	Conditions	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL					
V_{IN} Logic High	DRVDD = 1.8 V	1.2			V
V_{IN} Logic High	DRVDD = 2.5 V	1.7			V
V_{IN} Logic High	DRVDD = 3.3 V	2.0			V
V_{IN} Logic Low	DRVDD = 1.8 V			0.5	V
V_{IN} Logic Low	DRVDD = 2.5 V			0.7	V
V_{IN} Logic Low	DRVDD = 3.3 V			0.8	V
CMOS OUTPUT LOGIC LEVEL					
V_{OUT} Logic High	DRVDD = 1.8 V	1.35			V
V_{OUT} Logic High	DRVDD = 2.5 V	2.05			V
V_{OUT} Logic High	DRVDD = 3.3 V	2.4			V
V_{OUT} Logic Low	DRVDD = 1.8 V			0.4	V
V_{OUT} Logic Low	DRVDD = 2.5 V			0.4	V
V_{OUT} Logic Low	DRVDD = 3.3 V			0.4	V
DAC CLOCK INPUT					
Differential Peak-to-Peak Voltage		200	400	CLK33V	mV p-p diff
Duty Cycle		45		55	%
Slew Rate		0.1			V/ns
DIRECT CLOCKING					
Clock Rate	CLKP/CLKN inputs	0.1		200	MHz
DLL ENABLED					%
Clock Rate	DLL delay line output	100		310	MHz
SERIAL PERIPHERAL INTERFACE					
Maximum Clock Rate		50			MHz
Minimum Pulse Width High (t_{HIGH})		10			ns
Minimum Pulse Width Low (t_{LOW})		10			ns
Setup Time, SDIO (Data In) to SCLK (t_{DS})		5.0			ns
Hold Time, SDI to SCLK (t_{DH})		5.0			ns
Data Valid, SDIO (Data Out) to SCLK (t_{DV})				5.0	ns
Setup Time, $\overline{CS}$ to SCLK (t_S)		5.0			ns

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	With Respect to	Rating
RX33V, AUX33V	RXGND	−0.3 V to +3.9 V
TXVDD	TXGND	−0.3 V to +3.9 V
DRVDD	DGND	−0.3 V to +3.9 V
CLK33V	EPAD	−0.3 V to +3.9 V
RX18V, RX18VF	RXGND	−0.3 to +2.1 V
DVDD18V	EPAD	−0.3 to +2.1 V
CLK18V, DLL18V	EPAD	−0.3 to +2.1 V
RXGND, TXGND, DGND,	EPAD	−0.3 V to +0.3 V
TXIP, TXIN, TXQP, TXQN	TXGND	−1.0 V to TXVDD + 0.3 V
RXIP, RXIN, RXQP, RXQN	RXGND	−0.3 V to RX18V + 0.3 V
$\overline{CS}$, SCLK, SDIO, $\overline{RESET}$, LDO_EN	DGND	−0.3V to DRVDD + 0.3 V
TRXD[11:0], TXD[11:0], TXIQ, TRXIQ, TXCLK, TRXCLK	DGND	−0.3 V to DRVDD + 0.3 V
CLKP, CLKN	EPAD	−0.3 V to CLK33V + 0.3 V
Junction Temperature		+125°C
Storage Temperature Range		−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 7. Thermal Resistance

Airflow	θ_{JA}	θ_{JB}	θ_{JC}	Unit
1 m/sec	17.1	10.6	1.0	°C/W
0 m/sec	20.3			°C/W

Typical θ_{JA}, θ_{JB}, and θ_{JC} are specified for a JEDEC standard 51-7 High-κ thermal test board. Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes, reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

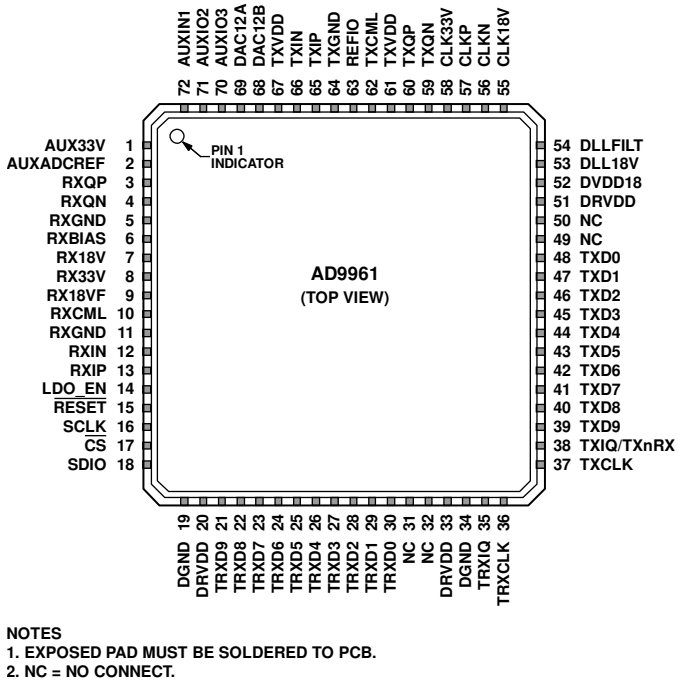

Figure 2. AD9961 Pin Configuration

Table 8. AD9961 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	AUX33V	Analog Supply for the Auxiliary ADC and Auxiliary DACs (3.3 V ± 5%, 1.8 V ± 5% If Auxiliary ADC Is Powered Down).
2	AUXADCREF	Reference Output (Or Input) for Auxiliary ADC.
3, 4	RXQP, RXQN	Differential ADC Q Inputs. The default full-scale input voltage range is 1.56 V p-p differential.
5, 11	RXGND	Receive Path Ground.
6	RXBIAS	External Bias Resistor Connection. An optional 10 kΩ resistor can be connected between this pin and the analog ground to improve the accuracy of the full-scale range of the Rx ADCs.
7	RX18V	Output of RX18V Voltage Regulator.
8	RX33V	Input to RX18V and RX18VF Voltage Regulators (2.5 V to 3.3 V). If LDOs are not being used, short Pin 8 to Pin 7.
9	RX18VF	Output of RX18VF Voltage Regulator.
10	RXCML	ADC Common-Mode Voltage Output.
12, 13	RXIN, RXIP	Differential ADC I Inputs. The default full-scale input voltage range is 1.56 V p-p differential.
14	LDO_EN	Control Pin for LDOs (GND = Disable all LDOs, Float = Enable DVDD18 LDO Only, DRVDD = Enable All LDOs).
15	$\overline{\text{RESET}}$	Reset. Active low to reset the configuration registers to default values and reset device.
16	SCLK	Clock Input for Serial Port.
17	$\overline{\text{CS}}$	Active Low Chip Select.
18	SDIO	Bidirectional Data Line for Serial Port.
19, 34	DGND	Digital Core Ground.
20, 33, 51	DRVDD	Input/Output Pad Ring Supply Voltage (1.8 V to 3.3 V).
21 to 30	TRXD9 to TRXD0	ADC Output Data in Full Duplex Mode. ADC output data and DAC input data in half-duplex mode.
31, 32, 49, 50	NC	Not Connected.
35	TRXIQ	Output Signal Indicating from Which ADC the Output Data Is Sourced.

Pin No.	Mnemonic	Description
36	TRXCLK	Qualifying Clock for the TRXD Bus.
37	TXCLK	Qualifying Clock for the TXD Bus. It can be configured as either an input or output.
38	TXIQ/TXnRX	Dual Function Pin. In half-duplex mode (TXnRX), this pin controls the direction of the TRX port. In full-duplex mode (TXIQ), this input signal indicates to which DAC, I or Q, the TxDAC input data is intended.
39 to 48	TXD9 to TXD0	TxDAC Input Data.
52	DVDD18	Digital Core 1.8 V Supply.
53	DLL18V	Output of DLL18V Voltage Regulator.
54	DLLFILT	DLL Filter Output.
55	CLK18V	Output of CLK18V Voltage Regulator.
56, 57	CLKN, CLKP	Differential Input Clock.
58	CLK33V	Input to CLK18V and DLL18V Voltage Regulators (1.8 V to 3.3 V). If LDOs are not being used, short Pin 58 to Pin 55. CLK33V must track TXVDD.
59, 60	TXQN, TXQP	Complementary DAC Q Current Outputs.
61, 67	TXVDD	Analog Supply Voltage for Tx Path (1.8 V to 3.3 V). TXVDD must track CLK33V.
62	TXCML	Common-Mode Input Voltage for the I and Q Tx DACs.
63	REFIO	Decoupling Point for Internal DAC 1.0 V Bandgap Reference. Use a 0.1 µF capacitor to AGND.
64	TXGND	Transmit Path Ground.
65, 66	TXIP, TXIN	Complementary DAC I Current Outputs.
68	DAC12B	Auxiliary DAC B Output.
69	DAC12A	Auxiliary DAC A Output.
70	AUXIO3	Selectable Analog Pin. Programmable to either Input 3 of the auxiliary ADC or to the auxiliary DAC10B output.
71	AUXIO2	Selectable Analog Pin. Programmable to either Input 2 of the auxiliary ADC or to the auxiliary DAC10A output.
72	AUXIN1	Input 1 of Auxiliary ADC.
	EPAD	Thermal Pad Under Chip. This must be connected to AGND for proper chip operation. It provides both a thermal and electrical connection to the PCB.

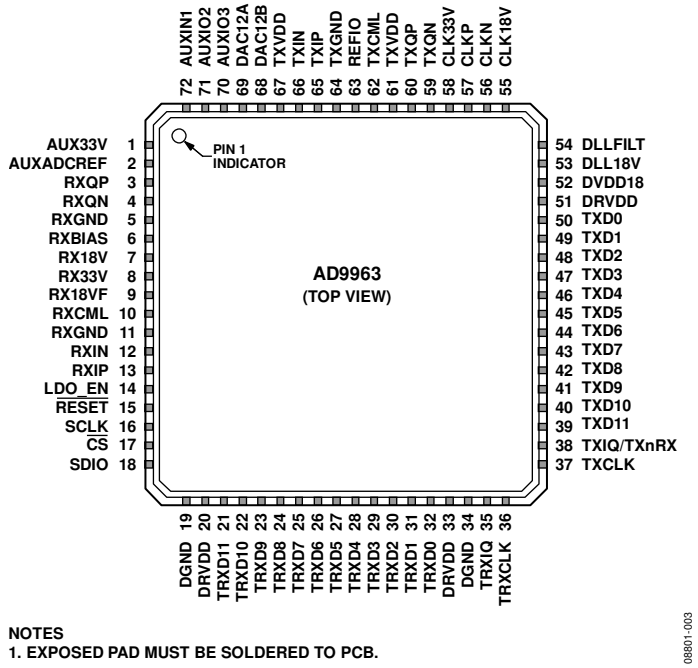

Figure 3. AD9963 Pin Configuration

Table 9. AD9963 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	AUX33V	Analog Supply for the Auxiliary ADC and Auxiliary DACs (3.3 V ± 10%, 1.8 V ± 10% If Auxiliary ADC Is Powered Down).
2	AUXADCREF	Reference Output (or input) for Auxiliary ADC.
3, 4	RXQP, RXQN	Differential ADC Q Inputs. Full-scale input voltage range is 1.56 V p-p differential.
5, 11	RXGND	Receive Path Ground.
6	RXBIAS	External Bias Resistor Connection. This voltage is nominally 0.5 V. A 10 kΩ resistor can be connected between this pin and analog ground to improve the Rx ADC full-scale accuracy.
7	RX18V	Output of RX18V Voltage Regulator.
8	RX33V	Input to RX18V and RX18VF Voltage Regulators (2.5 V to 3.3 V). If LDOs are not being used, short Pin 8 to Pin 7.
9	RX18VF	Output of RX18VF Voltage Regulator.
10	RXCML	ADC Common-Mode Voltage Output.
12, 13	RXIN, RXIP	Differential ADC I Inputs. Full-scale input voltage range is 1.56 V p-p differential.
14	LDO_EN	Control pin for LDOs (GND = Disable all LDOs, Float = Enable DVDD18 LDO Only, DRVDD = Enable All LDOs).
15	$\overline{\text{RESET}}$	Reset. Active low to reset the configuration registers to default values and reset device.
16	SCLK	Clock Input for Serial Port.
17	$\overline{\text{CS}}$	Active Low Chip Select.
18	SDIO	Bidirectional Data Line for Serial Port.
19, 34	DGND	Digital Core Ground.
20, 33, 51	DRVDD	Input/Output Pad Ring Supply Voltage (1.8 V to 3.3 V).
21 to 32	TRXD11 to TRXD0	ADC Output Data in Full Duplex Mode. ADC output data and DAC input data in half-duplex mode.
35	TRXIQ	Output Signal Indicating from Which ADC the Output Data Is Sourced.
36	TRXCLK	Qualifying Clock for the TRXD Bus.
37	TXCLK	Qualifying Clock for the TXD Bus. It can be configured as either an input or output.
38	TXIQ/TXnRX	Dual Function Pin. In half-duplex mode (TXnRX), this pin controls the direction of the TRX port. In full-duplex mode (TXIQ), this input signal indicates to which DAC, I or Q, the TxDAC Input Data is intended.
39 to 50	TXD11 to TXD0	TxDAC Input Data.
52	DVDD18	Digital Core 1.8 V Supply.
53	DLL18V	Output of DLL18V Voltage Regulator.

Pin No.	Mnemonic	Description
54	DLLFILT	DLL Filter Output.
55	CLK18V	Output of CLK18V Voltage Regulator.
56,57	CLKN, CLKP	Differential Input Clock.
58	CLK33V	Input to CLK18V and DLL18V Voltage Regulators (1.8 V to 3.3 V). If LDOs are not being used, short Pin 58 to Pin 55. CLK33V must track TXVDD.
59, 60	TXQN, TXQP	Complementary DAC Q Current Outputs.
61, 67	TXVDD	Analog Supply Voltage for Tx Path (1.8 V to 3.3V). TXVDD must track CLK33V.
62	TXCML	Common-Mode Input Voltage for the I and Q Tx DACs.
63	REFIO	Decoupling Point for Internal DAC 1.0 V Bandgap Reference. Use a 0.1 µF capacitor to AGND.
64	TXGND	Transmit Path Ground.
65, 66	TXIP, TXIN	Complementary DAC I Current Outputs.
68	DAC12B	Auxiliary DAC B Output.
69	DAC12A	Auxiliary DAC A Output.
70	AUXIO3	Selectable Analog Pin. Programmable to either Input 3 of the auxiliary ADC or to the auxiliary DAC10B output.
71	AUXIO2	Selectable Analog Pin. Programmable to either Input 2 of the auxiliary ADC or to the auxiliary DAC10A output.
72	AUXIN1	Input 1 of Auxiliary ADC.
	EPAD	Thermal Pad Under Chip. This must be connected to AGND for proper chip operation. It provides both a thermal and electrical connection to the PCB.

TYPICAL PERFORMANCE CHARACTERISTICS

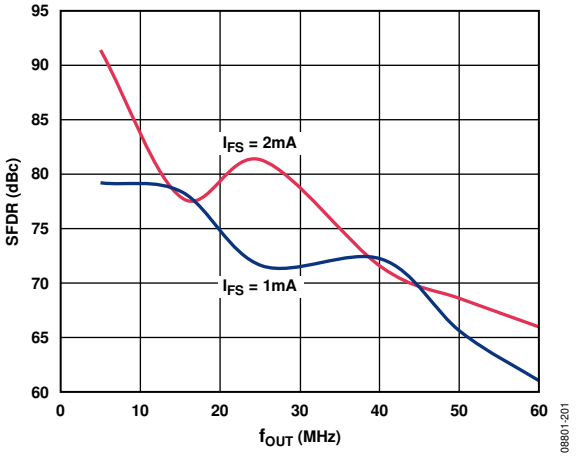

Figure 4. Second Harmonic Distortion vs. f_{OUT} Over Full-Scale Current, f_{DAC} = 125 MHz, 1×, Digital Scale = 0 dBFS, TXVDD = 1.8 V

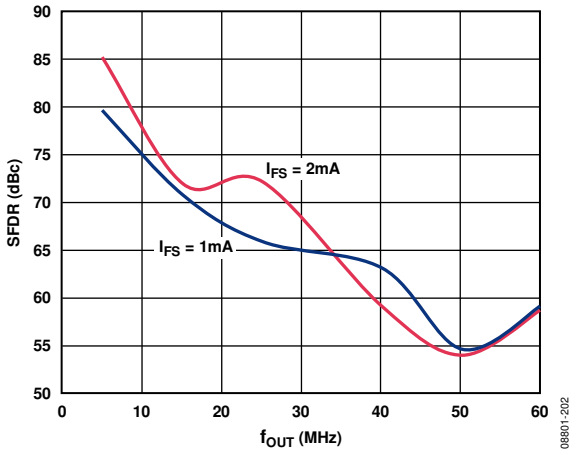

Figure 5. Third Harmonic Distortion vs. f_{OUT} Over Full-Scale Current, f_{DAC} = 125 MHz, 1×, Digital Scale = 0 dBFS, TXVDD = 1.8 V

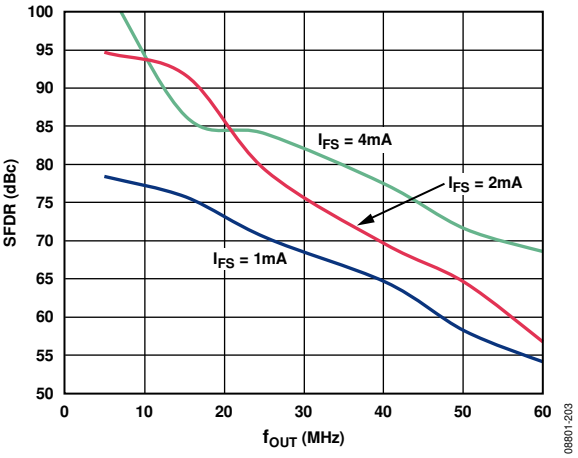

Figure 6. Second Harmonic Distortion vs. f_{OUT} Over Full-Scale Current, f_{DAC} = 125 MHz, 1×, Digital Scale = 0 dBFS, TXVDD = 3.3 V

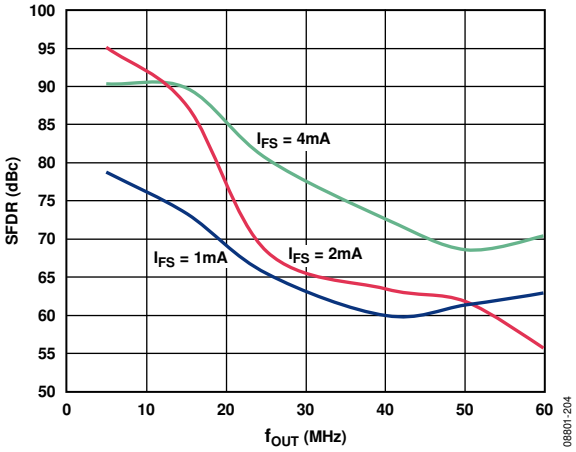

Figure 7. Third Harmonic Distortion vs. f_{OUT} Over Full-Scale Current, f_{DAC} = 125 MHz, 1×, Digital Scale = 0 dBFS, TXVDD = 3.3 V

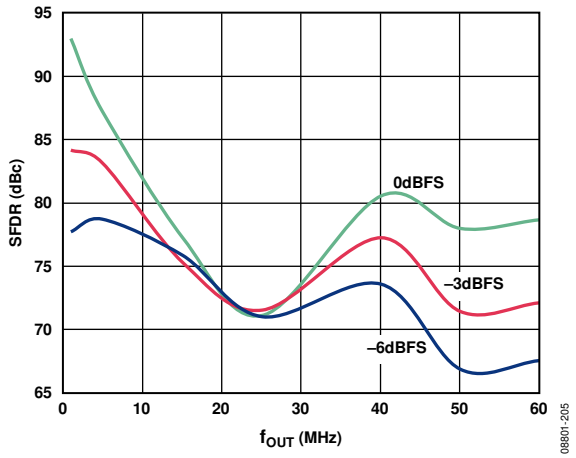

Figure 8. Second Harmonic Distortion vs. f_{OUT} Over Digital Scale, f_{DAC} = 125 MHz, 1×, Full-Scale Current = 2 mA, TXVDD = 1.8 V

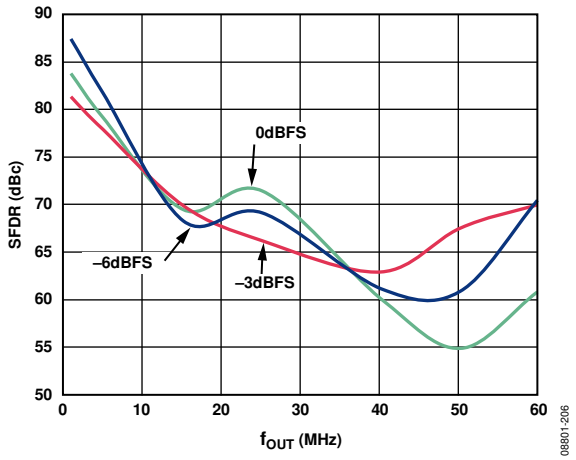

Figure 9. Third Harmonic Distortion vs. f_{OUT} Over Digital Scale, f_{DAC} = 125 MHz, 1×, Full-Scale Current = 2 mA, TXVDD = 1.8 V

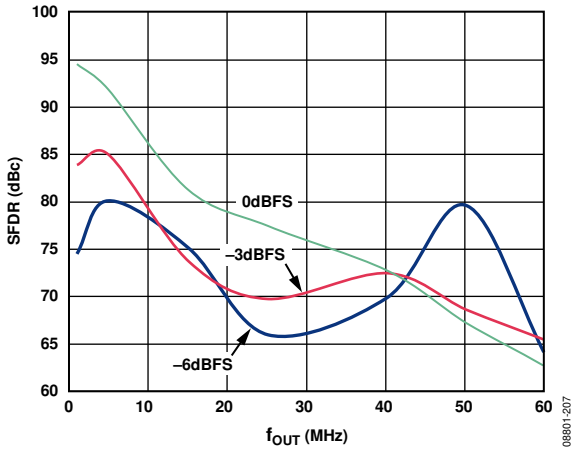

Figure 10. Second Harmonic Distortion vs. f_{OUT} Over Digital Scale, f_{DAC} = 125 MHz, 1×, Full-Scale Current = 2 mA, TXVDD = 3.3 V

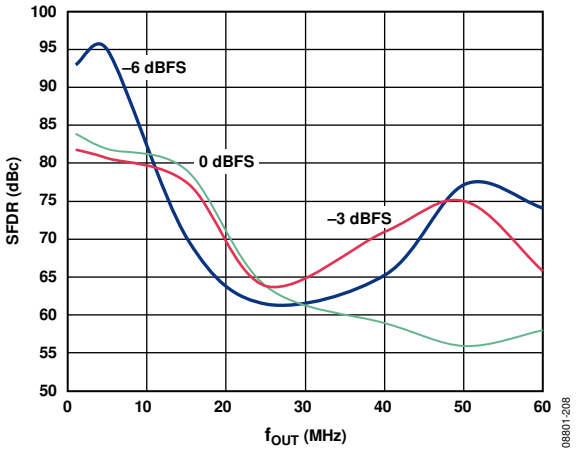

Figure 11. Third Harmonic Distortion vs. f_{OUT} Over Digital Scale, f_{DAC} = 125 MHz, 1×, Full-Scale Current = 2 mA, TXVDD = 3.3 V

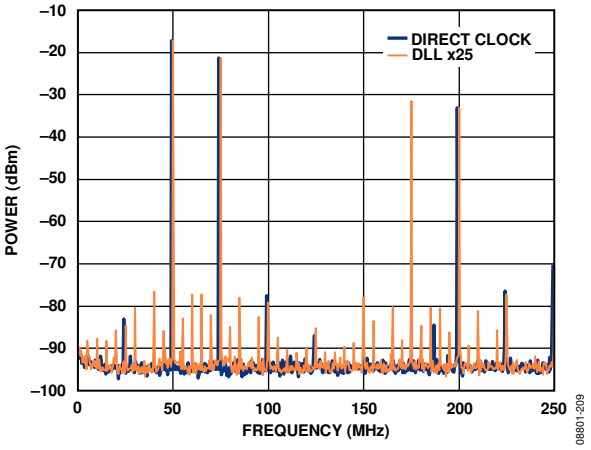

Figure 12. Transmit DAC Output Spectrum, Full-Scale Current = 2 mA, TXVDD = 3.3 V, f_{OUT} = 50 MHz, f_{DAC} = 125 MHz

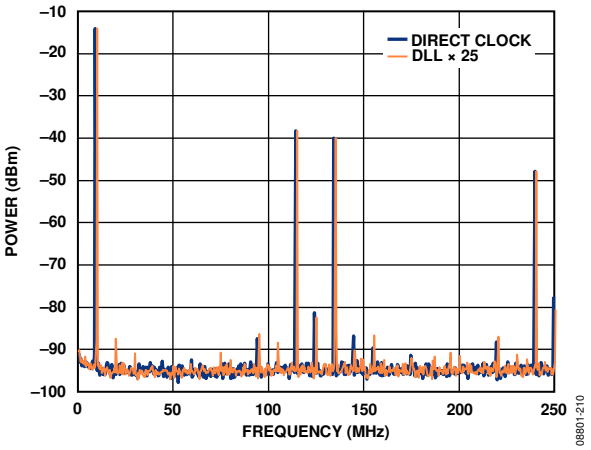

Figure 13. Transmit DAC Output Spectrum, Full-Scale Current = 2 mA, TXVDD = 3.3 V, f_{OUT} = 10 MHz, f_{DAC} = 125 MHz

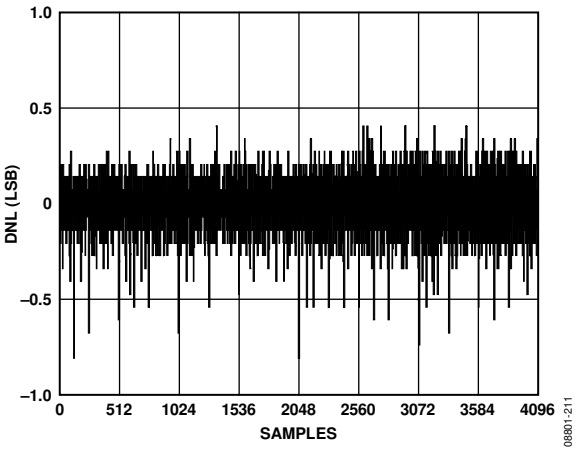

Figure 14. Auxiliary ADC DNL

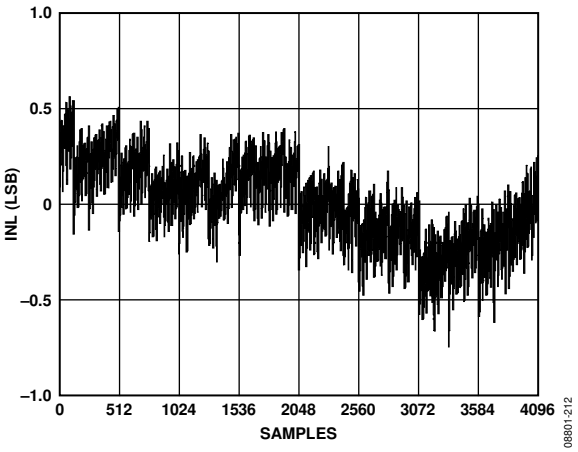

Figure 15. Auxiliary ADC INL

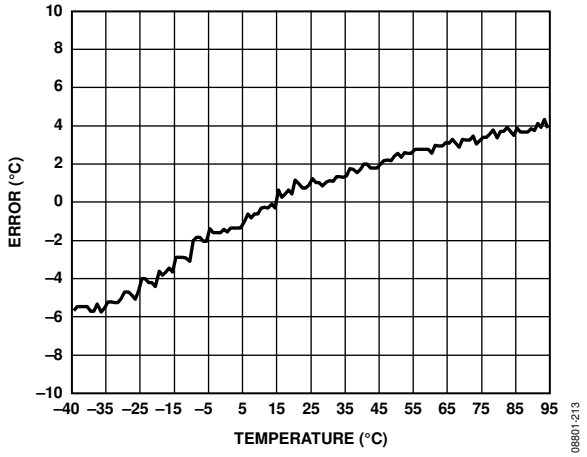

Figure 16. Typical Die Temperature Readback Error vs. Ambient Temperature

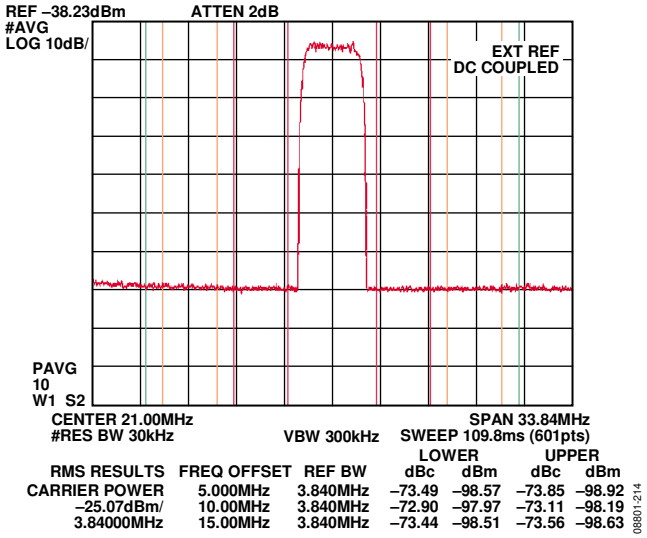

Figure 17. One-Carrier W-CDMA ACLR Performance, IF = ~21 MHz

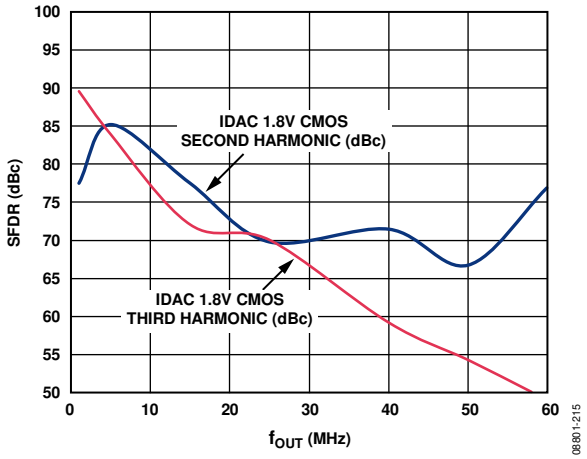

Figure 18. AD9961, Second and Third Harmonic Distortion vs. f_{OUT}, f_{DAC} = 125 MHz, 1×, Digital Scale = 0 dBFS, TXVDD = 1.8 V

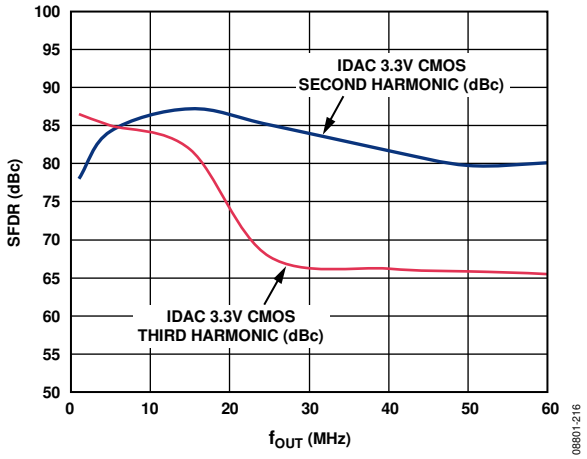

Figure 19. AD9961, Second and Third Harmonic Distortion vs. f_{OUT}, f_{DAC} = 125 MHz, 1×, Digital Scale = 0 dBFS, TXVDD = 3.3 V

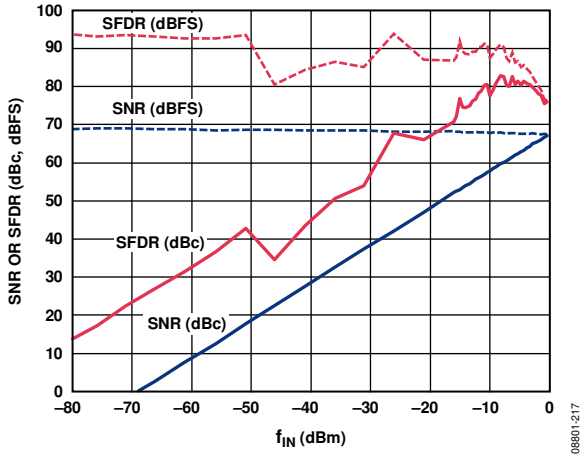

Figure 20. SNR/SFDR vs. Analog Input Level, f_{IN} = 10 MHz, f_{ADC} = 100 MSPS

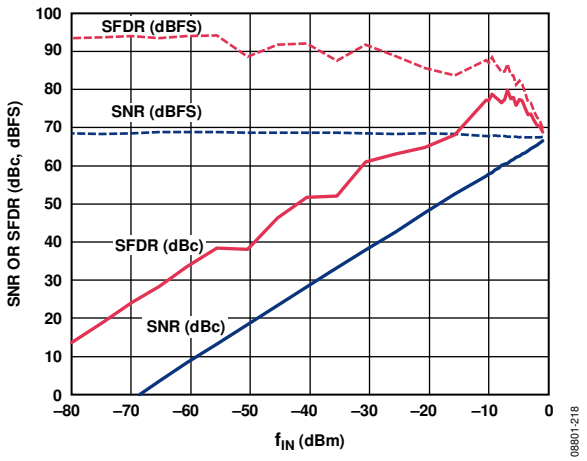

Figure 21. SNR/SFDR vs. Analog Input Level, f_{IN} = 70 MHz, f_{ADC} = 100 MSPS

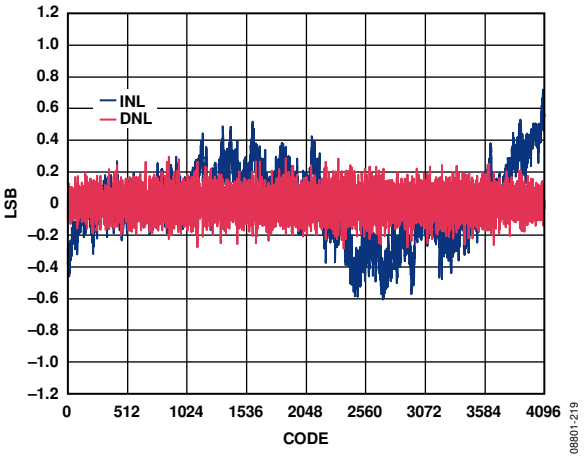

Figure 22. Rx Path ADC, INL and DNL

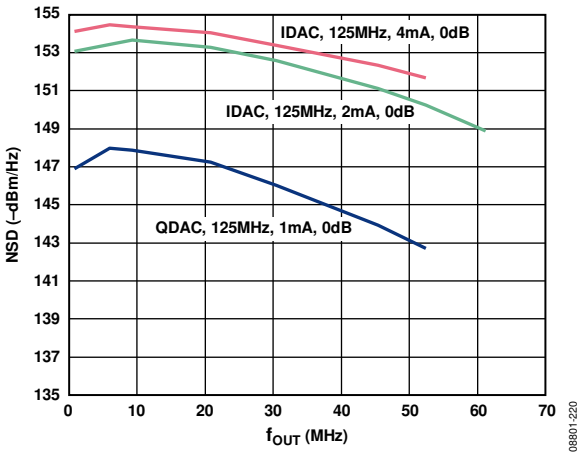

Figure 23. Transmit DAC Noise Spectral Density vs. f_{OUT} Over Full-Scale Current

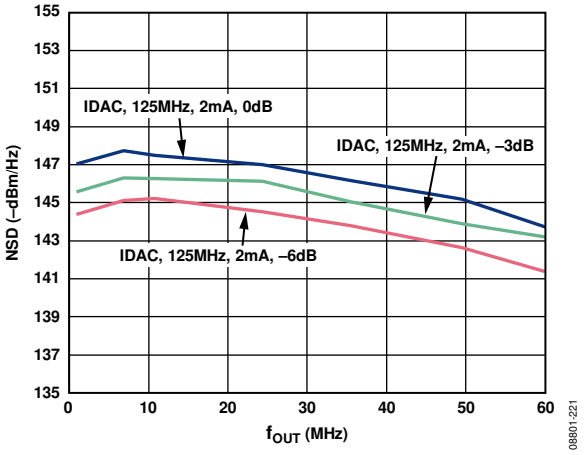

Figure 24. Transmit DAC Noise Spectral Density vs. f_{OUT} Over Digital Scale

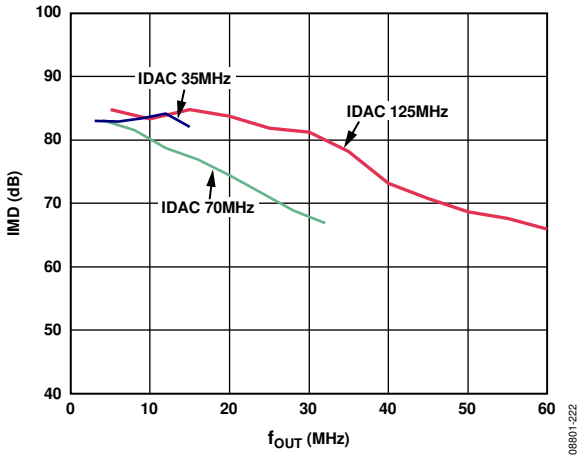

Figure 25. Intermodulation Distortion vs. f_{OUT} Over f_{DAC}, TXVDD = 3.3 V, Full-Scale Current = 2 mA

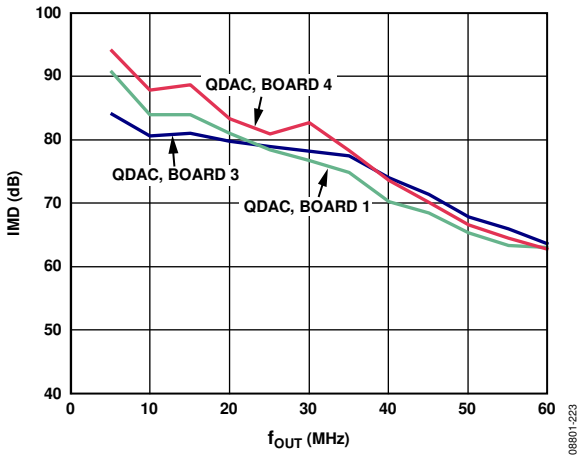

Figure 26. Intermodulation Distortion vs. f_{OUT}, TXVDD = 3.3 V, Full-Scale Current = 2 mA, Board-to-Board Variation

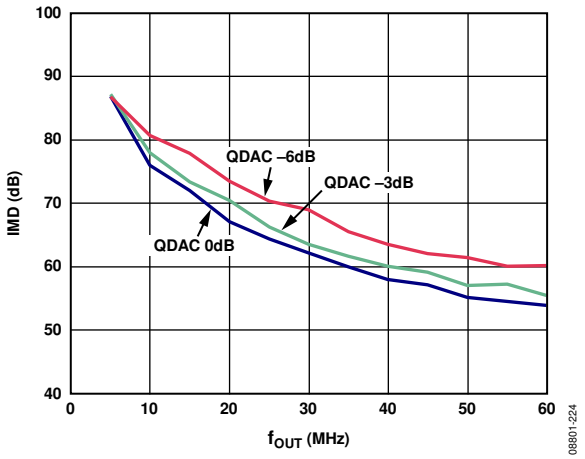

Figure 27. Intermodulation Distortion vs. f_{OUT} Over Digital Scale, TXVDD = 3.3 V, Full-Scale Current = 2 mA

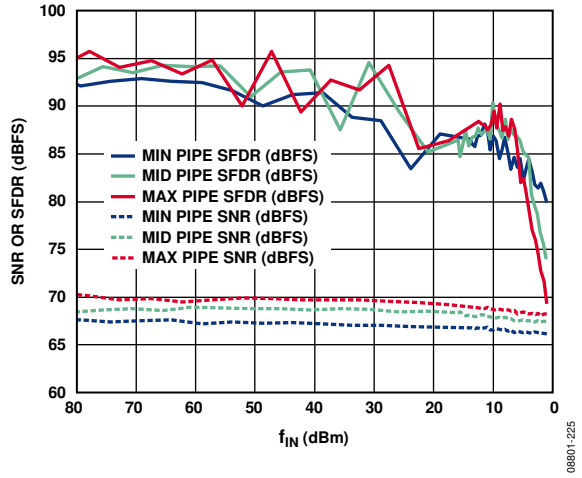

Figure 28. SNR/SFDR vs. Analog Input Level Over Full-Scale Input Range, f_{IN} = 70 MHz, f_{ADC} = 100 MSPS

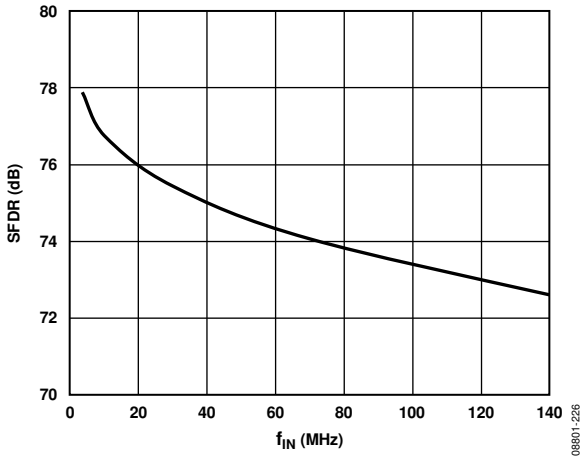

Figure 29. AD9963 100 MSPS Single Tone AC

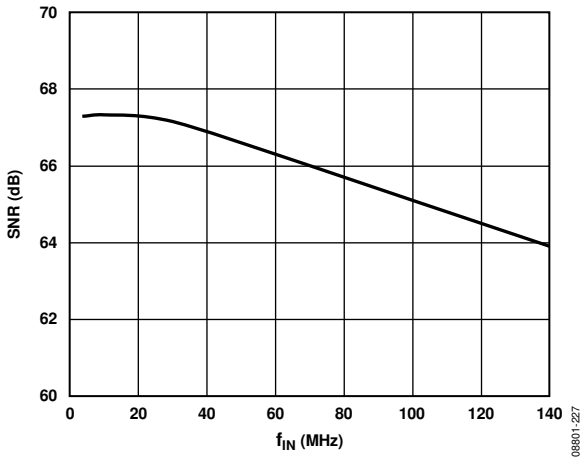

Figure 30. AD9963 1.8 V CMOS IADC, 100 MSPS Single Tone AC

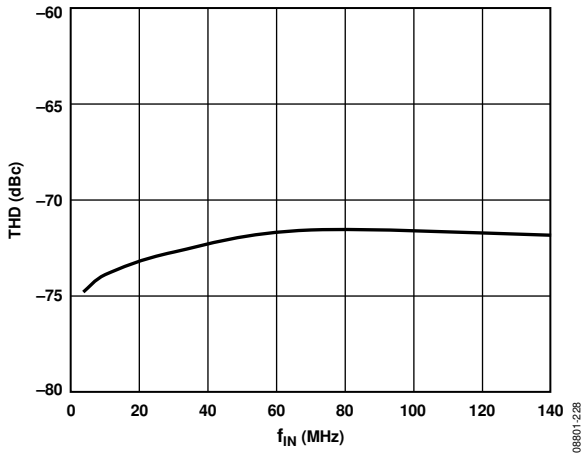

Figure 31. AD9963 1.8 V CMOS IADC, 100 MSPS Single Tone AC

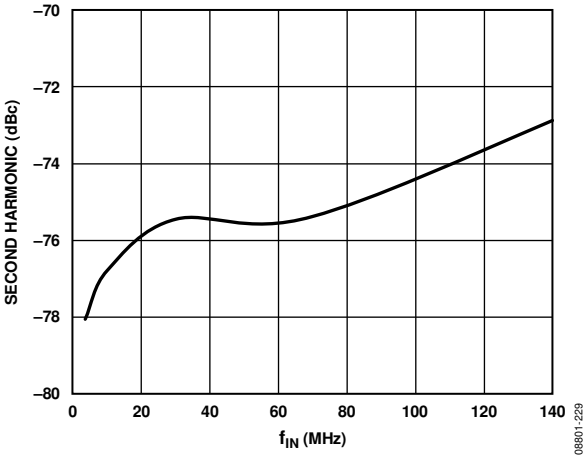

Figure 32. AD9963 1.8 V CMOS IADC, 100 MSPS Single Tone AC

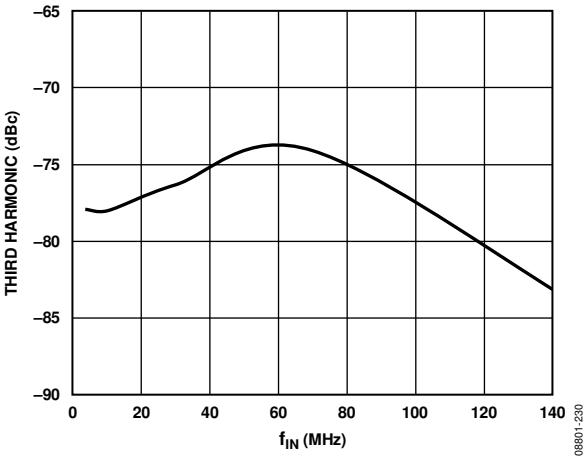

Figure 33. AD9963 1.8 V CMOS IADC, 100 MSPS Single Tone AC

TERMINOLOGY

Linearity Error (Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For TXIN, 0 mA output is expected when the inputs are all 0s. For TXIP, 0 mA output is expected when all inputs are set to 1.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the difference between the output when all inputs are set to 1 and the output when all inputs are set to 0.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in parts per million of full-scale range (FSR) per degree Celsius (°C). For reference drift, the drift is reported in parts per ppm/°C.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

Spurious Free Dynamic Range (SFDR)
The difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal between dc and the frequency equal to half the input data rate.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Adjacent Channel Leakage Ratio (ACLR)
The ratio in dBc between the measured power within a channel relative to its adjacent channel.

Complex Image Rejection
In a traditional two-part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

THEORY OF OPERATION

The AD9961/AD9963 are targeted to cover the mixed-signal front-end needs of multiple wireless communications systems. They feature a receive path that consists of dual 10-/12-bit receive ADCs and a transmit path that consists of dual 10-/12-bit transmit DACs (TxDAC). The AD9961/AD9963 integrate additional functionality typically required in most systems, such as power scalability, Tx gain control, and clock multiplication circuitry.

The AD9961/AD9963 minimize both size and power consumption to address the needs of a range of applications from the low power portable market to the high performance femto base station market. The part is provided in a 72-lead lead frame chip scale package (LFCSP) that has a footprint of only 10 mm × 10 mm. Power consumption can be optimized to suit the particular application by incorporating power-down controls, low power ADC modes, and TxDAC power scaling.

In full duplex mode, the AD9961/AD9963 use two 12-bit buses, along with qualifying clock signals, to transfer Rx path data and Tx path data. These two buses support either single data rate or double data rate data transfers. The data bus, along with many other device options, is configurable through the serial port by writing internal registers. The device can also be used in a single-port, half-duplex configuration.

SERIAL CONTROL PORT

The AD9961/AD9963 serial control ports are a flexible, synchronous, serial communications port that allows an easy interface with many industry-standard microcontrollers and microprocessors. The AD9961/AD9963 serial control ports are compatible with most synchronous transfer formats, including both the Motorola SPI and Intel® SSR® protocols. The serial control port allows read/write access to all registers that configure the AD9961/AD9963. Single or multiple byte transfers are supported, as well as MSB first or LSB first transfer formats.

Serial Control Port Pin Descriptions

The serial control port has three pins, SCLK, SDIO, and $\overline{CS}$:

- SCLK (serial clock) is the input clock used to register serial control port reads and writes. Write data bits are registered on the rising edge of this clock, and read data bits are registered on the falling edge. This pin is internally pulled down by a 30 kΩ resistor to ground.
- SDIO (serial data input/output) functions as both the input and output data pin.
- $\overline{CS}$ (chip select bar) is an active low control that gates the read and write cycles. When $\overline{CS}$ is high, SDIO is in a high impedance state and SCLK is disabled. This pin is internally pulled up by a 30 kΩ resistor to DRVDD.

GENERAL OPERATION OF SERIAL CONTROL PORT

The falling edge of $\overline{CS}$, in conjunction with the rising edge of SCLK, determines the start of a communication cycle. There are two parts to a communication cycle with the AD9961/AD9963. The first part writes a 16-bit instruction word into the AD9961/AD9963, coincident with the first 16 SCLK rising edges. The instruction word provides the AD9961/AD9963 serial control ports with information regarding the data transfer, which is the second part of the communication cycle. The instruction word defines whether the upcoming data transfer is a read or a write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer.

Instruction Header

The MSB of the instruction word is R/$\overline{W}$, which indicates whether the serial port transfer is a read or a write. The next two bits, N1:N0, indicate the length of the transfer in bytes. The final 13 bits are the address (A12 to A0) at which to begin the read or write operation.

For a write, the instruction word is followed by the number of bytes of data indicated by Bit N1 to Bit N0 (see Table 10).

Table 10. Byte Transfer Count

N1	N0	Bytes to Transfer
0	0	1
0	1	2
1	0	3
1	1	Streaming mode

A12 to A0 select the address within the register map that is written to or read from during the data transfer portion of the communications cycle. For multibyte transfers, the address is the starting byte address.

Only Address Bits[A7:A0] are needed to cover the range of the 0xFF registers used by the AD9961/AD9963. Address Bits[A12:A8] must always be 0.

Write Transfer

If the instruction header indicates a write operation, the bytes of data written onto the SDIO line are loaded into the serial control port buffer of the AD9961/AD9963. Data bits are registered on the rising edge of SCLK.

The length of the transfer (1 byte, 2 byte, 3 bytes, or streaming mode) is indicated by two bits (N1:N0) in the instruction byte. During a write, streaming mode does not skip over unused or reserved registers; therefore, the user must know what bit pattern to write to the reserved registers to preserve proper operation of the part. It does not matter what data is written to unused registers.

Read Transfer

If the instruction word is for a read operation, the next N × 8 SCLK cycles clock out the data from the address specified in the instruction word, where N is 1 to 3 as determined by N1:N0. If N = 4, the read operation is in streaming mode, and continues until $\overline{CS}$ is raised. Streaming mode does not skip over reserved or unused registers. The readback data is valid on the falling edge of SCLK.

MSB/LSB First Transfers

The AD9961/AD9963 instruction word and byte data formats can be selected to be MSB first or LSB first. The default for the AD9961/AD9963 is MSB first. When MSB first mode is active, the instruction and data bytes must be written from MSB to LSB. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes must follow in order from the high address to the low address. In MSB first mode, the serial control port internal address generator decrements for each data byte of the multibyte transfer cycle.

When LSB first is active, the instruction and data bytes must be written from LSB to MSB. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The internal byte address generator of the serial control port increments for each byte of the multibyte transfer cycle.

When LSB first is set by Register 0x00, Bit 2 and Register 0x00, Bit 6, it takes effect immediately. In multibyte transfers, subsequent bytes reflect any changes in the serial port configuration. To avoid problems reconfiguring the serial port operation, any data written to 0x00 must be mirrored (the eight bits should read the same, forward or backward). Mirroring the data makes it irrelevant whether LSB first or MSB first is in effect. As an example of this mirroring, the default setting for Register 0x00 is 00011000.

Ending Transfers

When the transfer is 1, 2, or 3 bytes, the data transfer ends after the required number of clock cycles have been received. $\overline{CS}$ can be raised after each sequence of eight bits to stall the bus (except after the last byte, where it ends the cycle). When the bus is stalled, the serial transfer resumes when $\overline{CS}$ is lowered. Raising $\overline{CS}$ on a non byte boundary resets the serial control port.

The AD9961/AD9963 serial control port register addresses decrement from the register address just written toward 0x00 for multibyte I/O operations if the MSB first mode is active (default). If the LSB first mode is active, the register address of the serial control port increments from the address just written toward 0xFF for multibyte I/O operations.

Streaming mode transfers always terminate when $\overline{CS}$ is raised. Streaming mode transfers also terminate whenever the address reaches 0xFF. Note that unused addresses are not skipped during multibyte I/O operations. To avoid unpredictable device behavior, do not write to reserved registers.

Table 11. Streaming Mode (No Addresses Are Skipped)

Write Mode	Address Direction	Stop Sequence
LSB First	Increment	0xFD, 0xFE, 0xFF, stop
MSB First	Decrement	0x01, 0x00, 0xFF, stop

SUB SERIAL INTERFACE COMMUNICATIONS

The AD9963/AD9961 have two registers that require a different communication sequence. These registers are 0x0F and 0x10. The write sequence for these two registers requires a write to Register 0x05, a write to the Register (0x0F or 0x10), and then a write to Register 0xFF. The write takes effect when the write to Register 0xFF is completed.

For example, to enable the RXCML pin output buffer, the register write sequence is:

1. Write 0x03 into Register 0x05. This addresses both of the Rx ADCs.
2. Write 0x02 into Register 0x0F. This sets the RXCML enable bit.
3. Write 0x01 into Register 0xFF. This updates the internal register, which activates the RXCML buffer.
4. Write 0x00 into Register 0x05. This returns the SPI to the normal addressing mode.

An example of updating Register 0x10 is given in the ADC Digital Offset Adjustment section.

Table 12. Serial Control Port, 16-Bit Instruction Word, MSB First

MSB															LSB
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R/$\overline{W}$	N1	N0	0	0	0	0	0	A7	A6	A5	A4	A3	A2	A1	A0

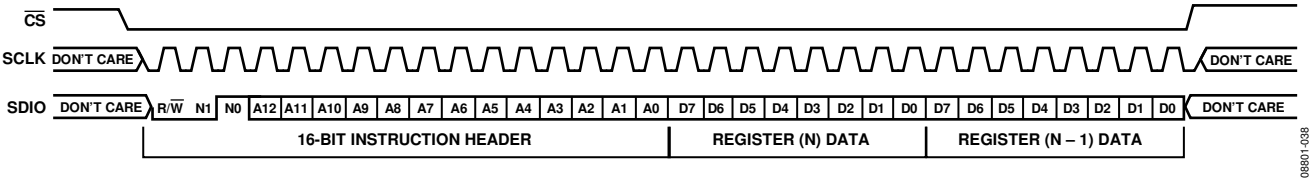

Figure 34. Serial Control Port Access—MSB First, 16-Bit Instruction, 2-Byte Data

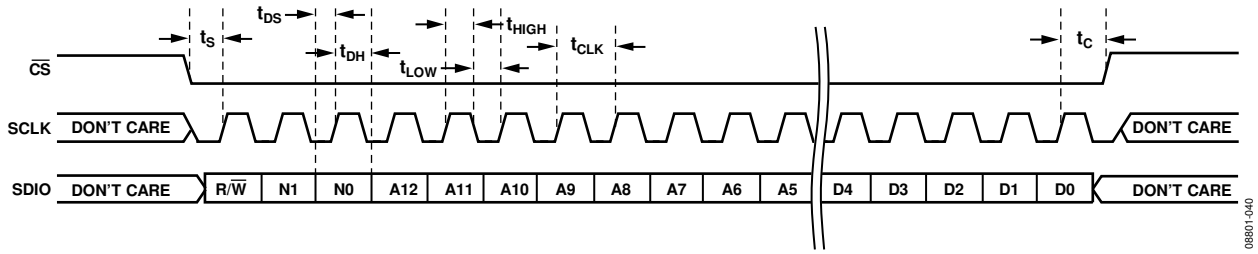

Figure 35. Serial Control Port Write—MSB First, 16-Bit Instruction, Timing Measurements

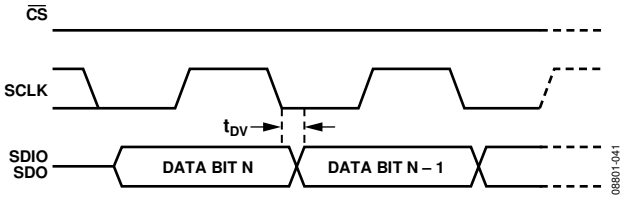

Figure 36. Timing Diagram for Serial Control Port Register Read

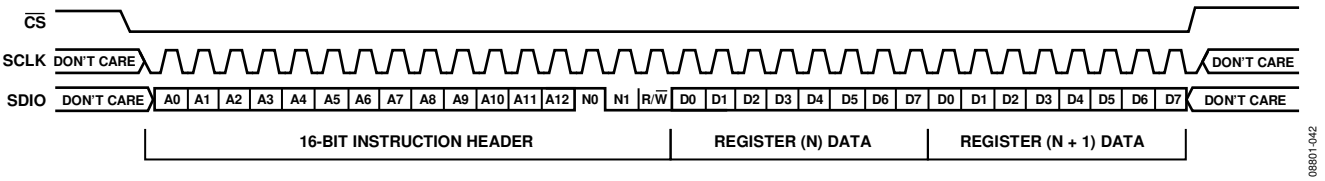

Figure 37. Serial Control Port Access—LSB First, 16-Bit Instruction, Two Bytes Data

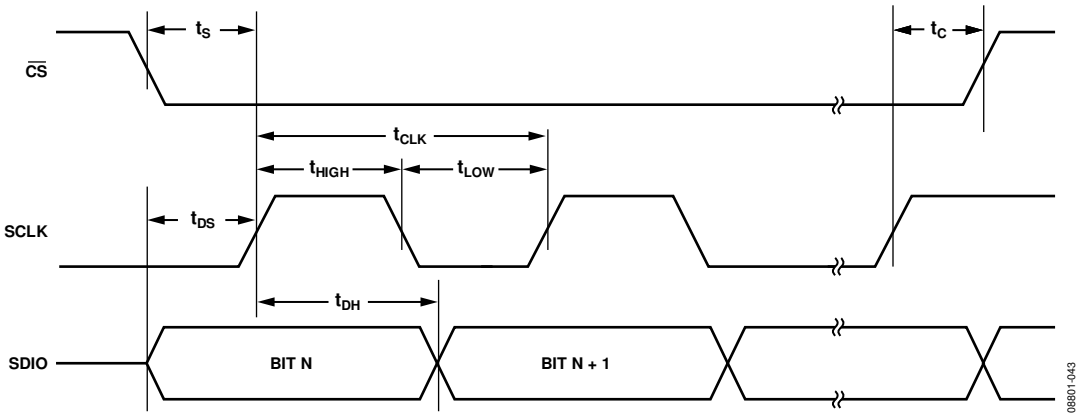

Figure 38. Serial Control Port Timing—Write

Table 13. Serial Control Port Timing

Parameter	Timing (Min, ns)	Description
t_{DS}	5.0	Setup time between data and rising edge of SCLK.
t_{DH}	5.0	Hold time between data and rising edge of SCLK.
t_{CLK}	20.0	Period of the clock.
t_S	5.0	Setup time between $\overline{CS}$ falling edge and SCLK rising edge (start of communication cycle).
t_C	2	Setup time between SCLK rising edge and $\overline{CS}$ rising edge (end of communication cycle).
t_{HIGH}	10	Minimum period that SCLK should be in a logic high state.
t_{LOW}	10	Minimum period that SCLK should be in a logic low state.
t_{DV}	5.0	SCLK to valid SDIO and SDO (see Figure 36).

CONFIGURATION REGISTERS

Table 14. Configuration Register Map

Addr	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	0x18	SDIO	LSB First	Reset	1	1	Reset	LSB First	SDIO
0x05	0x00	Unused						ADDRQ	ADDRI
0x0F	0x00							RXCML	
0x10	0x00	Unused		ADC_OFFSET[5:0]					
0x30	0x3F	Unused		DEC_BP	INT1_BP	INT0_BP	SRRC_BP	TXCLK_EN	RXCLK_EN
0x31	0xA7	TX_SDR	TXCKO_INV	TXCLK_MD[1:0]		TXCKI_INV	TXIQ_HILO	TX_IFIRST	TX_BNRY
0x32	0xA7	RX_SDR	Unused	RXCLK_MD[1:0]		RXCLK_INV	RXIQ_HILO	RX_IFIRST	RX_BNRY
0x33	Varies	Unused	FIFO_INIT	Aligned	ALIGN_ACK	ALIGN_REQ	FIFO_OFFSET[2:0]		
0x34	Varies	FIFO_LVL[7:0]							
0x35	0x10	Unused			SRRC_SCALE[4:0]				
0x36	0x08	Unused			INT0_SCALE[4:0]				
0x37	0x10	Unused			INT1_SCALE[4:0]				
0x38	0x06	Unused			DEC_SCALE[4:0]				
0x39	0x00	RXDLLRST	TXDLLRST	Unused		RXDLL_LKD	TXDLL_LKD	RXDBL_SEL	TXDBL_SEL
0x3A	0x51	TX_UNLOCK[1:0]		TX_LOCK[1:0]		TX_DLYOFS[1:0]		TX_HYST[1:0]	
0x3B	0x51	RX_UNLOCK[1:0]		RX_LOCK[1:0]		RX_DLYOFS[1:0]		RX_HYST[1:0]	
0x3C	0xF0	DBL_TAPDLY[7:0]							
0x3D	0x00	Unused				RX_INVQ	RX_INVI	TX_INVQ	TX_INVI
0x3E	0x09	Unused		TX_DBLPW[2:0]			RX_DBLPW[2:0]		
0x3F	0x07	Unused	RX_CLK	RX_BUS	SINGLERX	TXCLK_MD	HD_BUSCTL	HD_CLKMD	FULL_DUPLEX
0x40	0x01	DAC12B_EN	DAC12A_EN	DAC12B_TOP	DAC12A_TOP	Unused		AUXDAC_REF	DAC_UPDATE
0x41	0x00	DAC12A[11:4]							
0x42	0x00	Unused				DAC12A[3:0]			
0x43	0x00	DAC12B[11:4]							
0x44	0x00	Unused				DAC12B[3:0]			
0x45	0x00	DAC10B_EN	Unused		DAC10B_TOP[2:0]			DAC10B_RNG[1:0]	
0x46	0x00	DAC10B[9:2]							
0x47	0x00	Unused						DAC10B[1:0]	
0x48	0x00	DAC10A_EN	Unused		DAC10A_TOP[2:0]			DAC10A_RNG[1:0]	
0x49	0x00	DAC10A[9:2]							
0x4A	0x00	Unused						DAC10A[1:0]	
0x50	0x00	Unused			TX_PTTRN	TX_INSEL	TX_CONT	TX_START	TX_BISTEN
0x51	0x00	Unused			RX_PTTRN	RX_INSEL	RX_CONT	RX_START	RX_BISTEN
0x52	0x93	TXI_CHK[15:8]							
0x53	0x34	TXI_CHK[7:0]							
0x54	0x5F	TXQ_CHK[15:8]							
0x55	0x36	TXQ_CHK[7:0]							
0x5C	0x08	Chip ID[7:0]							
0x60	0x00	DLL_EN	TXDAC_PD	TXI_SLEEP	TXQ_SLEEP	CLK_PD	RXADC_PD	RXQ_SLEEP	RXI_SLEEP
0x61	0x00	Unused	DLL_LDO_PD	DLLBIAS_PD	CLK_LDO_PD	RX_LDO_PD	RXF_LDO_PD	AUXADC_PD	AUX_REF_PD
0x62	0xF8	DLL_LDO_STAT	CLK_LDO_STAT	RX_LDO_STAT	RXF_LDO_STAT	DIG_LDO_STAT	Unused	Unused	RSET_SEL
0x63	0x00	TRXD_DRV		TRXIQ_DRV		TRXCLK_DRV		TXCLK_DRV	
0x66	0x28	TXI_DCLK	TXQ_DCLK	Unused	RXI_DCLK	RXQ_DCLK	DCS_BP	ADCDIV[1:0]	
0x68	0x00	Unused		IGAIN1[5:0]					
0x69	0x00	Unused		IGAIN2[5:0]					
0x6A	0x00	Unused		IRSET[5:0]					
0x6B	0x00	Unused		QGAIN1[5:0]					
0x6C	0x00	Unused		QGAIN2[5:0]					
0x6D	0x00	Unused		QRSET[5:0]					
0x6E	0x40	Unused		REFIO_ADJ[5:0]					

Addr	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x71	0x00	ADCCLKSEL	DACCLKSEL	Unused	DLL_REF_EN	N[3:0]			
0x72	0x01	DLL_Locked	DLLDIV		M[4:0]				
0x75	0x00	0				DLL_RESB	0		
0x77	0x00	CONV_TIME[1:0]		Unused			AUXADC_CH[2:0]		
0x78	Varies	AUXADC[11:4]							
0x79	Varies	AUXADC[3:0]				CONV_COMPL	CHAN_SEL[2:0]		
0x7A	0x00	AUXADC_EN	AUXADC_RESB	Unused			AUXDIV[2:0]		
0x7B	0x00	TMPSNS_EN	Unused		AUXREF_ADJ[2:0]			Unused	
0x7D	0x00	Unused			RX_FSADJ[4:0]				
0x7E	0x00	Unused	RXTrim_EN	RXTrim_Fine	AUXCML_EN	0			RX_DC
0x7F	0x00	RXI_Trim[9:2]							
0x80	0x00	Unused					RXI_Trim[1:0]		GAINCAL_ENI
0x81	0x00	RXQ_Trim[9:2]							
0x82	0x00	Unused					RXQ_Trim[1:0]		GAINCAL_ENQ
0xFF	0x00	Unused							Update

CONFIGURATION REGISTER BIT DESCRIPTIONS

Table 15.

Register Name	Register Address	Bit(s)	Parameter	Function
Serial Port Config	0x00	7, 0	SDIO	0: use SDIO as both input and output data 1: use SDIO pin as input data only
		6, 1	LSB_First	0: first bit of serial data is MSB of data byte. 1: first bit of serial data is LSB of data byte.
		5, 2	RESET	A transition from 0 to 1 on this bit resets the device. All registers but Register 0x00 revert to their default values.
ADC Address	0x05	1:0	ADDRQ, ADDRI	Bits are set to determine which device on chip receives ADC specific write commands. ADC specific write commends include writes to Registers 0x0F and Register 0x10. These writes also require a rising end on the Update bit (Register 0xFF, Bit 0). 00: no ADCs are addressed. 01: I ADC is addressed. 10: Q ADC is addressed 11: both I and Q ADCs are addressed.
CM Buffer Enable	0x0F	1	RXCML	Enable control for the RXCML output buffer. Note that updating this bit also requires writing to Register 0x05 and Register 0xFF as described in the Sub Serial Interface Communications section. 0: RXCML pin is high impedance. 1: RXCML pin is a low impedance 1.4 V output.
ADC Offset	0x10	5:0	ADC_OFFSET[5:0]	Adds a dc offset to the ADC output of whichever ADC is addressed by Register 0x05. The offset applied is as follows: 011111: offset = +31 LSBs … 000001: offset = +1 LSB 000000: offset = 0 LSB 111111: offset = −1 LSB … 100000: offset = −32 LSBs
Digital Filters	0x30	7:6	Unused	
		5	DEC_BP	1: bypass 2× decimator in Rx path (D0).
		4	INT1_BP	1: bypass 2× Half-Band Interpolation Filter 1 (INT1).
		3	INT0_BP	1: bypass 2× Half-Band Interpolation Filter 0 (INT0).

Register Name	Register Address	Bit(s)	Parameter	Function
		2	SRRC_BP	1: bypass 2× SRRC interpolation filter (SRRC). The filter chain is SRRC→INT0→INT1. If SRRC filter is enabled, the other two filters are enabled too.
		1	TXCLK_EN	1: enables data clocks for transmit path.
		0	RxNTx	0: in HD SPI pin mode, TRx port operates in Tx mode. 1: in HD SPI pin mode, TRx port operates in Rx mode.
Tx Data Interface	0x31	7	TX_SDR	0: chooses DDR clocking mode. Tx data is driven out on both edges of the TXCLK signal. 1: chooses bus rate clocking mode. Tx data is driven out on one edge of the TXCLK signal.
		6	TXCKO_INV	This signal inverts the phase of the transmit path output clock signal. 0: does not invert TxCLK output. 1: inverts TxCLK output.
		5:4	TXCLK_MD[1:0]	Controls the mode of the TXCLK pin. The TXCLK pin can be configured as an input or an output. When configured as an output, it can have two possible sources, the internal TXCLK signal or the DLL output signal. 00: disabled. 01: the TXCLK pin is configured as an input. 10: the TXCLK pin is configured as an output. The source signal is the transmit path clock signal. 11: the TXCLK pin is configured as an output. The source signal is the DLL output signal. Note that the TXCLK signal may appear on either the TXCLK pin or the TRXCLK pin, depending on the mode of the device. In Half-Duplex 1-Clock mode, this signal is present on the TRXCLK pin when TX is active. In Half-Duplex 2-Clock mode and Full-Duplex mode, this signal is present on the TXCLK pin.
		3	TXCKI_INV	Selects which edge of the TXCLK signal samples the transmit path data. 0: TXPCLK negative edge latches transmit path data. 1: TXPCLK positive edge latches transmit path data.
		2	TXIQ_HILO	Data appears on the TXD bus sequentially but is loaded into the transmit path in pairs. TXIQ_HILO selects how the TXIQ signal marks each data pair. 0: each data pair is marked by TXIQ being low then high. 1: each data pair is marked by TXIQ being high then low.
		1	TX_IFIRST	This bit sets the data pairing order of the I and Q samples on transmit path. 0: selects that Q is first, followed by I. 1: selects that I is first, followed by Q.
		0	TX_BNRY	This bit selects the data format of the transmit path data. 0: Tx binary. 1: Tx twos complement.
Rx Data Interface	0x32	7	RX_SDR	0: chooses DDR clocking mode. Rx data is driven out on both edges of the TRXCLK signal. 1: chooses bus rate clocking mode. Rx data is driven out on one edge of the TRXCLK signal.
		6	Unused	
		5:4	RXCLK_MD[1:0]	This sets the way the internal RXCLK signal in the chip is driven. 00: disabled. 01: disabled. 10: RXCLK is driven by internal Rx path clock.