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ANALOG DEVICES

Dual-Channel, 14-Bit, CCD Signal Processor with *Precision Timing* Core

AD9974

FEATURES

1.8 V analog and digital core supply voltage
Correlated double sampler (CDS) with
    −3 dB, 0 dB, +3 dB, and +6 dB gain
6 dB to 42 dB, 10-bit variable gain amplifier (VGA)
14-bit, 65 MHz analog-to-digital converter (ADC)
Black level clamp with variable level control
Complete on-chip timing generator
Precision Timing **core with 240 ps resolution @ 65 MHz**
On-chip 3 V horizontal and RG drivers
100-lead, 9 mm × 9 mm, 0.8 mm pitch, CSP_BGA package
Internal low dropout (LDO) regulator circuitry

APPLICATIONS

Professional HDTV camcorders
Professional/high end digital cameras
Broadcast cameras
Industrial high speed cameras

GENERAL DESCRIPTION

The AD9974 is a highly integrated, dual-channel, charge-coupled device (CCD) signal processor for high speed digital video camera applications. Each channel is specified at pixel rates of up to 65 MHz. The AD9974 consists of a complete analog front end (AFE) with analog-to-digital conversion, combined with a programmable timing driver. The *Precision Timing*™ core allows adjustment of high speed clocks with approximately 240 ps resolution at 65 MHz operation.

Each AFE includes black level clamping, CDS, VGA, and a 65 MSPS, 14-bit ADC. The timing driver provides the high speed CCD clock drivers for the RG_A, RG_B, H1_A to H4_A, and H1_B to H4_B outputs. A 3-wire serial interface is used to program each channel of the AD9974.

Available in a space-saving, 9 mm × 9 mm, CSP_BGA package, the AD9974 is specified over an operating temperature range of −25°C to +85°C.
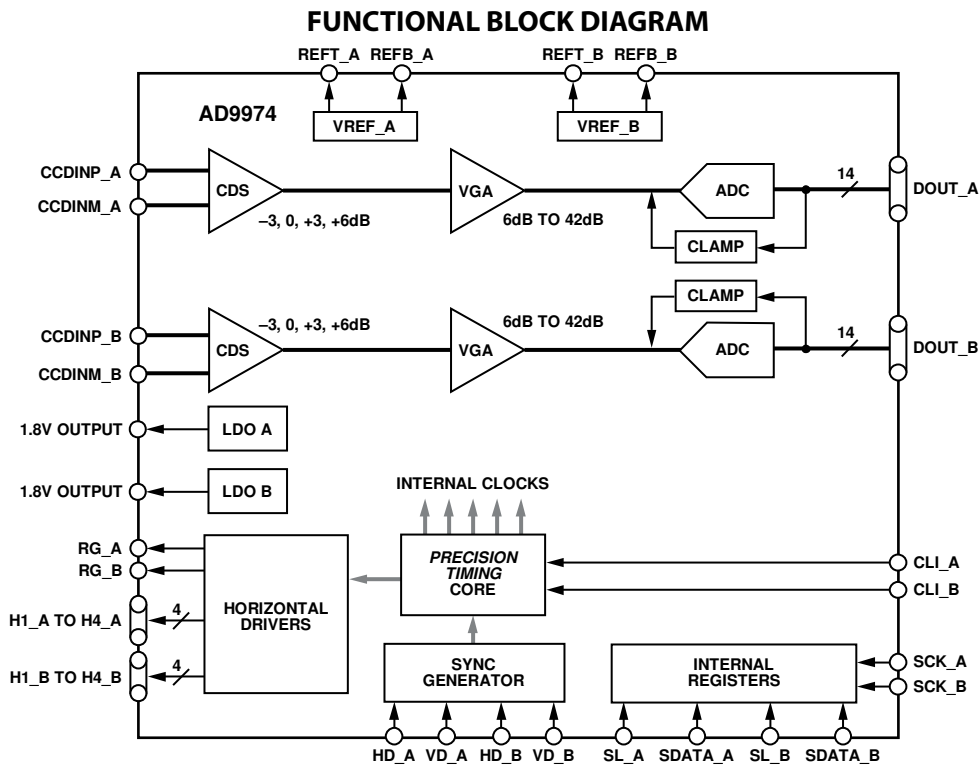
FUNCTIONAL BLOCK DIAGRAM

Figure 1.

AD9974* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS 🗗

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DOCUMENTATION 🗗

Data Sheet

- AD9974: Dual-Channel, 14-Bit, CCD Signal Processor with *Precision Timing*® Core Proprietary Data Sheet

DESIGN RESOURCES 🗗

- AD9974 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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AD9974

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REVISION HISTORY

SPECIFICATIONS

X = A = B, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating	−25		+85	°C
Storage	−65		+150	°C
POWER SUPPLY VOLTAGE				
AVDD_X (AFE, Timing Core)	1.6	1.8	2.0	V
RGVDD_X (RG_X Driver)	2.7	3.3	3.6	V
HVDD_X (H1_X to H4_X Drivers)	2.7	3.3	3.6	V
DVDD_X (All Other Digital)	1.6	1.8	2.0	V
DRVDD_X (Parallel Data Output Drivers)	1.6	3.0	3.6	V
IOVDD_X (I/O Supply Without the Use of LDO)	1.6	1.8	3.6	V
POWER SUPPLY CURRENTS—65 MHz OPERATION				
AVDD_X (1.8 V)		55		mA
RGVDD_X (3.3 V, 20 pF RG Load)		5		mA
HVDD_X[1] (3.3 V, 200 pF Total Load on H1 to H4)		40		mA
DVDD_X (1.8 V)		15		mA
DRVDD_X (3.0 V)		3		mA
IOVDD_X (1.8 V)		2		mA
POWER SUPPLY CURRENTS—STANDBY MODE OPERATION				
Reference Standby		10		mA
Total Shutdown		0.5		mA
LDO[2]				
IOVDD_X (I/O Supply When Using LDO)		3.0		V
Output Voltage		1.85		V
Output Current		60	100	mA
CLOCK RATE (CLI)	8		65	MHz

[1] The total power dissipated by the HVDD (or RGVDD) supply can be approximated as follows: $Total\ HVDD\ Power = [C_{LOAD} \times HVDD \times Pixel\ Frequency] \times HVDD$. Reducing the capacitive load and/or reducing the HVDD supply reduces the power dissipation. C_{LOAD} is the total capacitance seen by all H-outputs.
[2] LDO should be used to supply only AVDD and DVDD.

CHANNEL-TO-CHANNEL SPECIFICATIONS

X = A = B, T_{MIN} to T_{MAX}, AVDD_X = DVDD_X = 1.8 V, f_{CLI} = 65 MHz, typical timing specifications, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LINEARITY MISMATCH[1]		<0.5		%	Absolute value above 1/16 of maximum output code
CROSSTALK ERROR					CDS = 0 dB
Channel A to Channel B		−82		dB	Full-scale step applied to Channel A while measuring response on Channel B
Channel B to Channel A		−82		dB	Full-scale step applied to Channel B while measuring response on Channel A

[1] See the Terminology section for further measurement explanation.

TIMING SPECIFICATIONS

$X = A = B$, $C_L = 20$ pF, $AVDD\_X = DVDD\_X = 1.8$ V, $f_{CLI} = 65$ MHz, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Comments
MASTER CLOCK (CLI)					See Figure 17
CLI Clock Period (t_{CONV})	15.38			ns	
CLI High/Low Pulse Width (t_{ADC})	6.9	7.7	8.9	ns	
Delay from CLI Rising Edge to Internal Pixel Position 0 (t_{CLIDLY})		5		ns	
AFE					
SHP Rising Edge to SHD Rising Edge (t_{S1})	6.9	7.7	8.5	ns	See Figure 21
AFE Pipeline Delay		16		Cycles	See Figure 22
CLPOB Pulse Width (Programmable) (t_{COB})[1]	2	20		Pixels	
HD Pulse Width	t_{CONV}			ns	
VD Pulse Width	1 HD period			ns	
SERIAL INTERFACE					See Figure 52
Maximum SCK Frequency (f_{SCLK})	40			MHz	
SL to SCK Setup Time (t_{LS})	10			ns	
SCK to SL Hold Time (t_{LH})	10			ns	
SDATA Valid to SCK Rising Edge Setup (t_{DS})	10			ns	
SCK Rising Edge to SDATA Valid Hold (t_{DH})	10			ns	
H-COUNTER RESET SPECIFICATIONS					See Figure 49
HD Pulse Width	t_{CONV}			ns	
VD Pulse Width	1 HD period			ns	
VD Falling Edge to HD Falling Edge (t_{VDHD})	0		VD period − t_{CONV}	ns	
HD Falling Edge to CLI Rising Edge (t_{HDCLI})	3		$t_{CONV} − 2$	ns	
CLI Rising Edge to SHPLOC (Internal Sample Edge) (t_{CLISHP})	3		$t_{CONV} − 2$	ns	
TIMING CORE SETTING RESTRICTIONS					
Inhibited Region for SHP Edge Location (t_{SHPINH}) (See Figure 21)[2]	50		64/0		Edge location
Inhibited Region for SHP or SHD with Respect to H-Clocks (See Figure 21)[3, 4, 5, 6]					
RETIME = 0, MASK = 0 (t_{SHDINH})	H × NEGLOC − 15		H × NEGLOC − 0		Edge location
RETIME = 0, MASK = 1 (t_{SHDINH})	H × POSLOC − 15		H × POSLOC − 0		Edge location
RETIME = 1, MASK = 0 (t_{SHPINH})	H × NEGLOC − 15		H × NEGLOC − 0		Edge location
RETIME = 1, MASK = 1 (t_{SHPINH})	H × POSLOC − 15		H × POSLOC − 0		Edge location
Inhibited Region for DOUTPHASE Edge Location ($t_{DOUTINH}$) (See Figure 21)	SHDLOC + 0		SHDLOC + 15		Edge location

[1] Minimum CLPOB pulse width is for functional operation only. Wider typical pulses are recommended to achieve good clamp performance.
[2] Only applies to slave mode operation. The inhibited area for SHP is needed to meet the timing requirements for t_{CLISHP} for proper H-counter reset operation.
[3] When 0x34[2:0] HxBLKRETIME bits are enabled, the inhibit region for SHD location changes to inhibit region for SHP location.
[4] When sequence register 0x09[23:21] HBLK masking registers are set to 0, the H-edge reference becomes H × NEGLOC.
[5] The H-clock signals that have SHP/SHD inhibit regions depend on the HCLK mode: Mode 1 = H1, Mode 2 = H1, H2, and Mode 3 = H1, H3.
[6] These specifications apply when H1POL, H2POL, RGPOL, and HLPOL are all set to 1 (default setting).

DIGITAL SPECIFICATIONS

$X = A = B$, IOVDD_X = 1.6 V to 3.6 V, RGVDD_X = HVDD_X = 2.7 V to 3.6 V, C_L = 20 pF, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS					
High Level Input Voltage (V_{IH})	IOVDD − 0.6			V	
Low Level Input Voltage (V_{IL})			0.6	V	
High Level Input Current (I_{IH})		10		µA	
Low Level Input Current (I_{IL})		10		µA	
Input Capacitance (C_{IN})		10		pF	
LOGIC OUTPUTS					
High Level Output Voltage (V_{OH})	IOVDD − 0.5			V	I_{OH} = 2 mA
Low Level Output Voltage (V_{OL})			0.5	V	I_{OL} = 2 mA
CLI INPUT (CLI_BIAS = 0)					
High Level Input Voltage (V_{IHCLI})	IOVDD/2 + 0.5			V	
Low Level Input Voltage (V_{ILCLI})			IOVDD/2 − 0.5	V	
H-DRIVER OUTPUTS					
High Level Output Voltage at Maximum Current (V_{OH})	HVDD − 0.5			V	
Low Level Output Voltage at Maximum Current			0.5	V	
Maximum Output Current (Programmable) (V_{OL})		30		mA	
Maximum Load Capacitance	100			pF	

AD9974

ANALOG SPECIFICATIONS

X = A = B, AVDD_X = 1.8 V, f_{CLI} = 65 MHz, typical timing specifications, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CDS[1]					
Allowable CCD Reset Transient		0.5	0.8	V	
CDS Gain Accuracy					
−3 dB CDS Gain	−3.3	−2.8	−2.3		
0 dB CDS Gain (Default)	−0.7	−0.2	+0.3		
3 dB CDS Gain	2.3	2.8	3.3		
6 dB CDS Gain	4.9	5.4	5.9		
Maximum Input Voltage					VGA gain = 5.6 dB (Code 15, default value)
−3 dB CDS Gain		1.4		V p-p	
0 dB CDS Gain (Default)		1.0		V p-p	
3 dB CDS Gain		0.7		V p-p	
6 dB CDS Gain		0.5		V p-p	
Allowable OB Pixel Amplitude					
0 dB CDS Gain (Default)	−100		+200	mV	
6 dB CDS Gain	−50		+100	mV	
VARIABLE GAIN AMPLIFIER (VGA_X)					
Gain Control Resolution		1024		Steps	
Gain Monotonicity		Guaranteed			
Low Gain Setting (VGA Code 15, Default)		6		dB	
Maximum Gain Setting (VGA Code 1023)		42		dB	
BLACK LEVEL CLAMP					
Clamp Level Resolution		1024		Steps	
Minimum Clamp Level (Code 0)		0		LSB	Measured at ADC output
Maximum Clamp Level (Code 1023)		1023		LSB	Measured at ADC output
ADC (CHN_A and CHN_B)					
Resolution	14			Bits	
Differential Nonlinearity (DNL)	−1.0	±0.5	+1.2	LSB	
No Missing Codes		Guaranteed			
Integral Nonlinearity (INL)		5	15	LSB	
Full-Scale Input Voltage		2.0		V	
VOLTAGE REFERENCE					
Reference Top Voltage (REFT_X)		1.4		V	
Reference Bottom Voltage (REFB_X)		0.4		V	
SYSTEM PERFORMANCE					Specifications include entire signal chain
VGA Gain Accuracy					0 dB CDS gain (default)
Low Gain (Code 15)	5.1	5.6	6.1	dB	Gain = (0.0359 × code) + 5.1 dB
Maximum Gain (Code 1023)	41.3	41.8	42.3	dB	
Peak Nonlinearity, 500 mV Input Signal		0.1	0.4	%	12 dB total gain applied
Total Output Noise		2		LSB rms	AC-grounded input, 6 dB gain applied
Power Supply Rejection (PSR)		48		dB	Measured with step change on supply

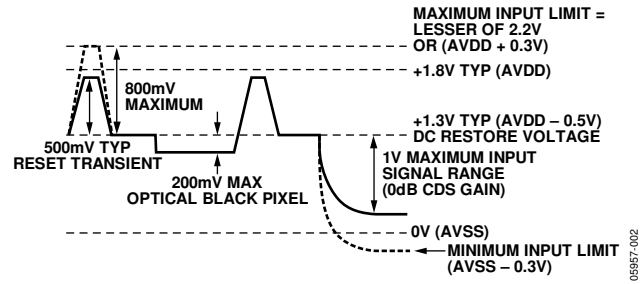[1] Input signal characteristics are defined as shown in Figure 2.

Figure 2. Input Signal Characteristics

ABSOLUTE MAXIMUM RATINGS

Ratings apply to both Channel A and Channel B, unless otherwise noted.

Table 6.

Parameter	Rating
AVDD to AVSS	−0.3 V to +2.2 V
DVDD to DVSS	−0.3 V to +2.2 V
DRVDD to DRVSS	−0.3 V to +3.9 V
IOVDD to DVSS	−0.3 V to +3.9 V
HVDD to HVSS	−0.3 V to +3.9 V
RGVDD to RGVSS	−0.3 V to +3.9 V
Any VSS	−0.3 V to +0.3 V
RG Output to RGVSS	−0.3 V to RGVDD + 0.3 V
H1 to H4, HL Output to HVSS	−0.3 V to HVDD + 0.3 V
SCK, SL, SDI to DVSS	−0.3 V to IOVDD + 0.3 V
REFT, REFB, CCDINM, CCDINP to AVSS	−0.2 V to AVDD + 0.2 V
Junction Temperature	150°C
Lead Temperature (10 sec)	350°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

θ_{JA} is measured using a 4-layer PCB with the exposed paddle soldered to the board.

Table 7. Thermal Resistance

Package Type	θ_{JA}	Unit
100-Lead, 9 mm × 9 mm, CSP_BGA	38.3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

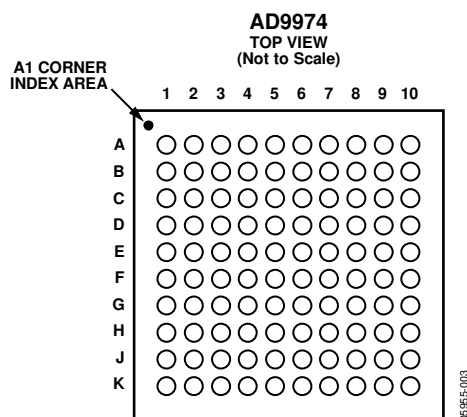# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Ball Location	Mnemonic	Type[1]	Description
B2	SL_A	DI	3-Wire Serial Load for Channel A.
C2	SDATA_A	DI	3-Wire Serial Data for Channel A.
D2	SCK_A	DI	3-Wire Serial Clock for Channel A.
C1	REFT_A	AO	Reference with Top Decoupling for Channel A. Decouple with 0.1 µF to AVSS_A.
D1	REFB_A	AO	Reference with Bottom Decoupling for Channel A. Decouple with 0.1 µF to AVSS_A.
A1	CCDINM_A	AI	Analog Input for Channel A Image Sensor Signal.
F4	H1_A	DO	CCD Horizontal Clock 1 for Channel A.
F3	H2_A	DO	CCD Horizontal Clock 2 for Channel A.
D4	H3_A	DO	CCD Horizontal Clock 3 for Channel A.
D3	H4_A	DO	CCD Horizontal Clock 4 for Channel A.
B4	RG_A	DO	CCD Reset Gate Clock for Channel A.
J2	DRVSS_A	P	Digital Driver Ground for Channel A.
K3	DRVDD_A	P	Digital Driver Supply for Channel A: 1.8 V or 3.0 V.
E3	HVSS_A	P	H1_A to H4_A Driver Ground for Channel A.
E4	HVDD_A	P	H1_A to H4_A Driver Supply for Channel A: 3.0 V.
C3	RGVSS_A	P	RG_A Driver Ground for Channel A.
C4	RGVDD_A	P	RG_A Driver Supply for Channel A: 3.0 V.
B3	IOVDD_A	P	Digital I/O Supply: 1.8 V or 3.0 V (HD, VD, SL, SCK, SDATA) and LDO Input (3.0 V Only) When LDO Is Used.
A4	CLI_A	DI	Master Clock Input for Channel A.
B1	AVSS_A	P	Analog Ground for Channel A.
A2	CCDINP_A	AI	Analog Input for Channel A Image Sensor Signal.
F2	DVSS_A	P	Digital Ground for Channel A.
F1	DVDD_A	P	Digital Supply for Channel A: 1.8 V.
E2	VD_A	DI	Vertical Sync Pulse for Channel A.
E1	HD_A	DI	Horizontal Sync Pulse for Channel A.
B8	SL_B	DI	3-Wire Serial Load for Channel B.
C8	SDATA_B	DI	3-Wire Serial Data for Channel B.
A5	LDO_OUT_A	P	1.8 V LDO Output from Channel A.
A6	CCDINM_B	AI	Analog Input for Channel B Image Sensor Signal.
D8	SCK_B	DI	3-Wire Serial Clock for Channel B.
C7	REFT_B	AO	Reference with Top Decoupling for Channel B. Decouple with 0.1 µF to AVSS_B.
D7	REFB_B	AO	Reference with Bottom Decoupling for Channel B. Decouple with 0.1 µF to AVSS_B.
A7	CCDINP_B	AI	Analog Input for Channel B Image Sensor Signal.
F10	H1_B	DO	CCD Horizontal Clock 1 for Channel B.
F9	H2_B	DO	CCD Horizontal Clock 2 for Channel B.

AD9974

Ball Location	Mnemonic	Type[1]	Description
D10	H3_B	DO	CCD Horizontal Clock 3 for Channel B.
D9	H4_B	DO	CCD Horizontal Clock 4 for Channel B.
B10	RG_B	DO	CCD Reset Gate Clock for Channel B.
J8	DRVSS_B	P	Digital Driver Ground for Channel B.
K9	DRVDD_B	P	Digital Driver Supply for Channel B: 1.8 V or 3.0 V.
E9	HVSS_B	P	H1_B to H4_B Driver Ground for Channel B.
E10	HVDD_B	P	H1_B to H4_B Driver Supply for Channel B: 3.0 V.
C9	RGVSS_B	P	RG_B Driver Ground for Channel B.
C10	RGVDD_B	P	RG_B Driver Supply for Channel B: 3.0 V.
B9	IOVDD_B	P	Digital I/O Supply: 1.8 V or 3.0 V (HD, VD, SL, SCK, SDATA) and LDO Input (3.0 V Only) When LDO Is Used.
A10	LDO_OUT_B	P	1.8 V LDO Output from Channel B.
B7	AVSS_B	P	Analog Ground for Channel B.
A8	AVDD_B	P	Analog Supply for Channel B: 1.8 V.
F8	DVSS_B	P	Digital Ground for Channel B.
F7	DVDD_B	P	Digital Supply for Channel B: 1.8 V.
E8	VD_B	DI	Vertical Sync Pulse for Channel B.
E7	HD_B	DI	Horizontal Sync Pulse for Channel B.
A3	AVDD_A	P	Analog Supply for Channel A: 1.8 V.
G1	D0_A	DO	Data Outputs Channel A.
H1	D1_A	DO	Data Outputs Channel A.
J1	D2_A	DO	Data Outputs Channel A.
K1	D3_A	DO	Data Outputs Channel A.
G2	D4_A	DO	Data Outputs Channel A.
H2	D5_A	DO	Data Outputs Channel A.
K2	D6_A	DO	Data Outputs Channel A.
G3	D7_A	DO	Data Outputs Channel A.
H3	D8_A	DO	Data Outputs Channel A.
J3	D9_A	DO	Data Outputs Channel A.
K4	D10_A	DO	Data Outputs Channel A.
J4	D11_A	DO	Data Outputs Channel A.
H4	D12_A	DO	Data Outputs Channel A.
G4	D13_A	DO	Data Outputs Channel A.
B5, C5, D5, E5, F5, G5, H5, J5, K5, B6, C6, D6, E6, F6, G6, H6, J6, K6	GND	P	Ground Connection.
A9	CLI_B	DI	Master Clock Input for Channel B.
G7	D0_B	DO	Data Outputs Channel B.
H7	D1_B	DO	Data Outputs Channel B.
J7	D2_B	DO	Data Outputs Channel B.
K7	D3_B	DO	Data Outputs Channel B.
G8	D4_B	DO	Data Outputs Channel B.
H8	D5_B	DO	Data Outputs Channel B.
K8	D6_B	DO	Data Outputs Channel B.
G9	D7_B	DO	Data Outputs Channel B.
H9	D8_B	DO	Data Outputs Channel B.
J9	D9_B	DO	Data Outputs Channel B.
K10	D10_B	DO	Data Outputs Channel B.
J10	D11_B	DO	Data Outputs Channel B.
H10	D12_B	DO	Data Outputs Channel B.
G10	D13_B	DO	Data Outputs Channel B.

[1] AI = analog input, AO = analog output, DI = digital input, DO = digital output, P = power.
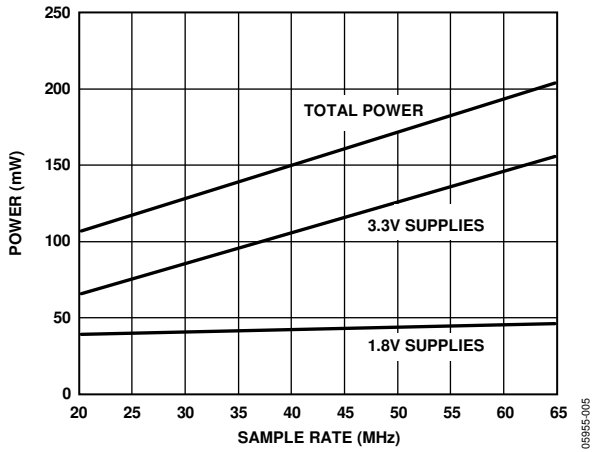
TYPICAL PERFORMANCE CHARACTERISTICS

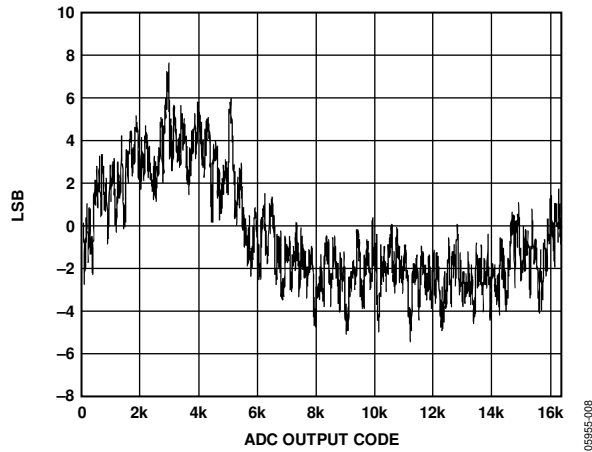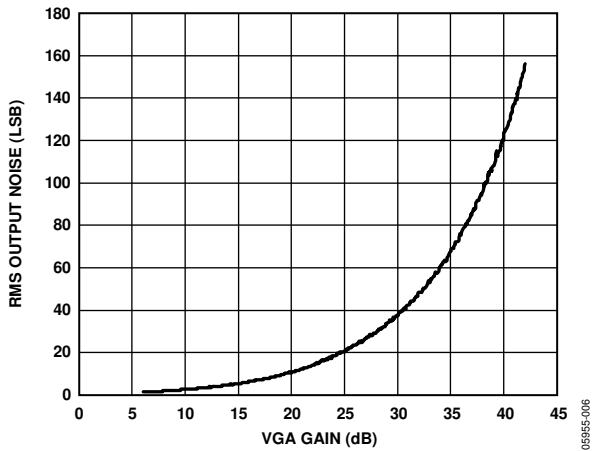Figure 4. Power vs. Sample Rate

Figure 7. Integral Nonlinearity

Figure 5. RMS Output Noise vs. VGA Gain
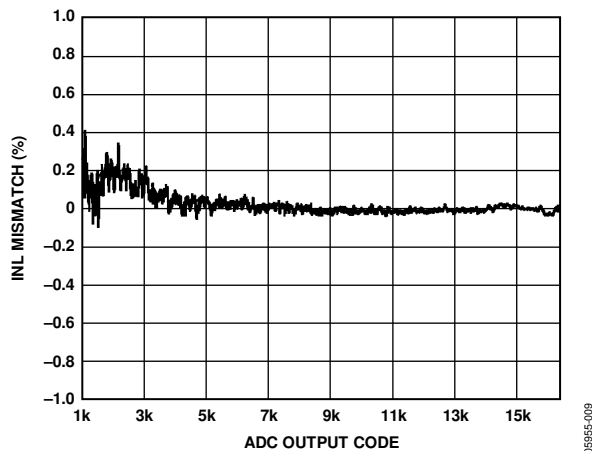
Figure 8. Linearity Mismatch vs. ADC Output Code

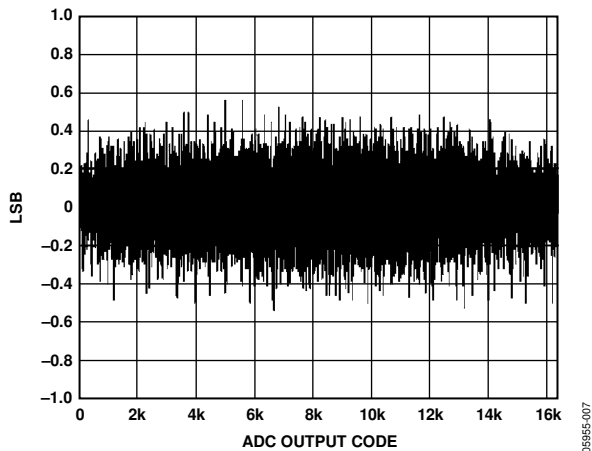Figure 6. Differential Nonlinearity
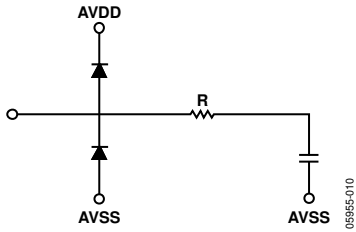
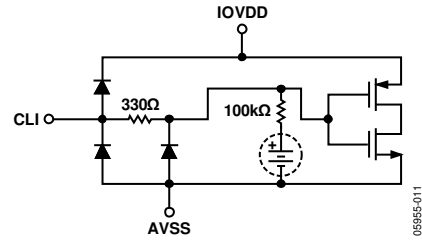# EQUIVALENT INPUT/OUTPUT CIRCUITS

Figure 9. CCDIN Input

Figure 11. CLI Input, Register 0x15[0] = 1 Enables the Bias Circuit
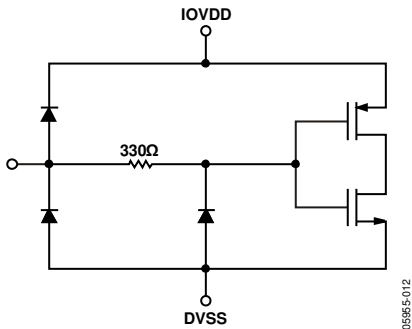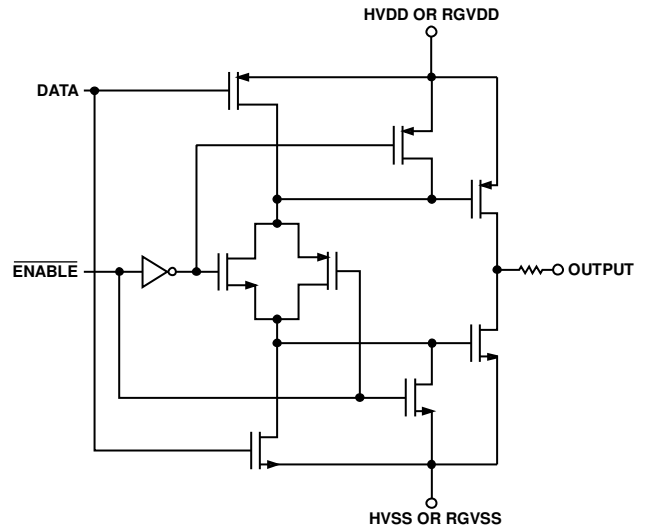

Figure 10. Digital Inputs

Figure 12. H1 to H4 and RG Outputs

TERMINOLOGY

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore, every code must have a finite width. No missing codes guaranteed to 14-bit resolution indicates that all 16,384 codes, each for its respective input, must be present over all operating conditions.

Peak Nonlinearity

Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the output of the AD9974 from a true straight line. The point used as zero scale occurs 0.5 LSB before the first code transition. Positive full scale is defined as a level 1 LSB and 0.5 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always appropriately gained up to fill the ADC full-scale range.

Total Output Noise

The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage using the relationship

$$1 \text{ LSB} = (ADC \ Full \ Scale/2^n \ Codes)$$

where n is the bit resolution of the ADC. For the AD9974, 1 LSB is approximately 122.0 μV.

Linearity Mismatch

The linearity mismatch is calculated by taking the difference in INL of the two channels at Input X, and then expressing the difference as a percentage of the output code at X. The values given in Table 2 are obtained over the range of 1/16 and maximum of the output code. The general trend is for the linearity mismatch to decrease as the output approaches the maximum code, as shown in Figure 8.

$$Linearity \ Mismatch \ (\%) = \frac{|INL\,A(X) - INL\,B(X)|}{Output\,Code(X)}$$
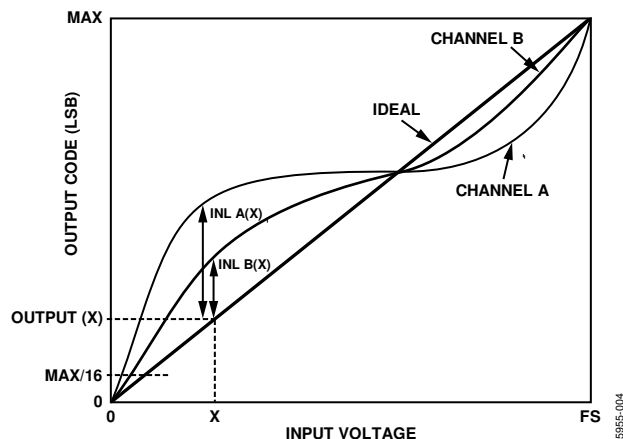

Figure 13. Linearity Mismatch Definition

Power Supply Rejection (PSR)

The PSR is measured with a step change applied to the supply pins. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

Crosstalk

The crosstalk is measured while applying a full-scale step to one channel and measuring the interference on the opposite channel.

$$Crosstalk \ (dB) = 20 \times \log\left(\frac{Interference\ (LSB)}{16,384}\right)$$
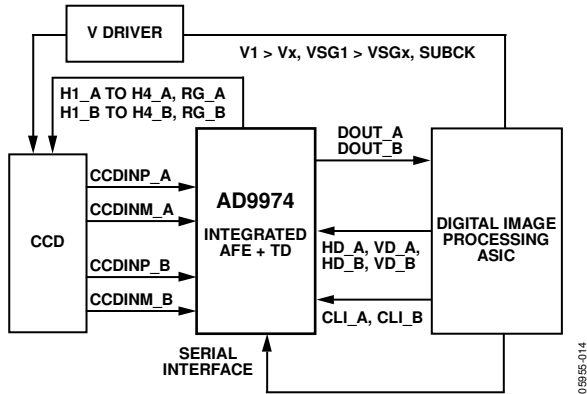
THEORY OF OPERATION

Figure 14. Typical Application

Figure 14 shows the typical system block diagram for the AD9974. The charge-coupled device (CCD) output is processed by the analog front-end (AFE) circuitry of the AD9974, consisting of a CDS, VGA, black level clamp, and ADC. The digitized pixel information is sent to the digital image processor chip, which performs the postprocessing and compression. To operate the CCD, all CCD timing parameters are programmed into the AD9974 from the system ASIC through the 3-wire serial interface. From the system master clock, CLI_X, which is provided by the image processor or external crystal, the AD9974 generates the horizontal clocks of the CCD and all internal AFE clocks.

All AD9974 clocks are synchronized with VD and HD inputs. All of the AD9974 horizontal pulses (CLPOB, PBLK, and HBLK) are programmed and generated internally.

The H-drivers for H1 to H4 and RG are included in the AD9974, allowing these clocks to be directly connected to the CCD. An H-driver voltage of 3 V is supported in the AD9974.

Figure 15 and Figure 16 show the maximum horizontal and vertical counter dimensions for the AD9974. All internal horizontal and vertical clocking is controlled by these counters, which specify line and pixel locations. Maximum HD length is 8191 pixels per line, and maximum VD length is 8191 lines per field.
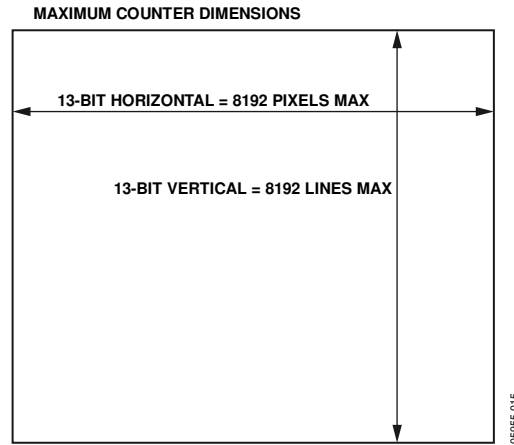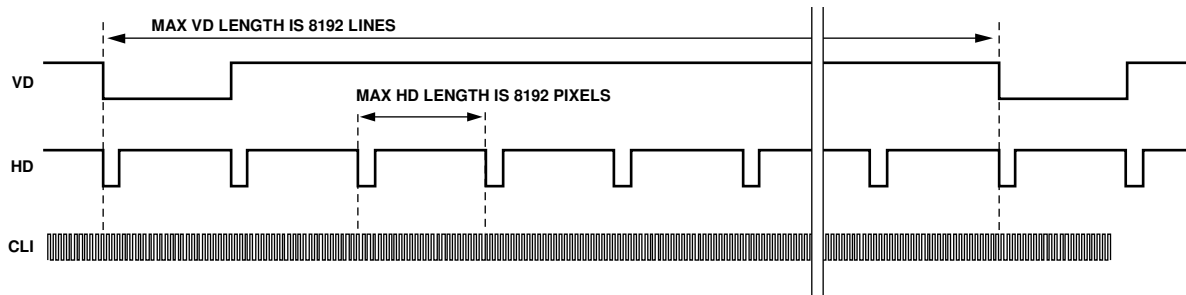

Figure 15. Vertical and Horizontal Counters

Figure 16. Maximum VD/HD Dimensions

PROGRAMMABLE TIMING GENERATION

PRECISION TIMING HIGH SPEED TIMING CORE

The AD9974 generates flexible high speed timing signals using the *Precision Timing* core. This core, composed of the Reset Gate RG, Horizontal Driver H1 to Horizontal Driver H4, and SHP/SHD sample clocks, is the foundation for generating the timing for both the CCD and the AFE. A unique architecture makes it routine for the system designer to optimize image quality by providing precise control over the horizontal CCD readout and the AFE correlated double sampling.

Timing Resolution

The *Precision Timing* core uses a master clock input (CLI_X) as a reference. This clock input should be the same as the CCD pixel clock frequency. Figure 17 illustrates how the internal timing core divides the master clock period into 64 steps or edge positions; therefore, the edge resolution of the *Precision Timing* core is (t_{CLI}/64). For more information on using the CLI input, refer to the Applications Information section.

Using a 65 MHz CLI frequency, the edge resolution of the *Precision Timing* core is approximately 240 ps. If a 1× system clock is not available, it is possible to use a 2× reference clock by programming the CLIDIVIDE register (Address 0x0D). The AD9974 then internally divides the CLI frequency by 2.

High Speed Clock Programmability

Figure 18 shows when the high speed clocks, RG, H1 to H4, SHP, and SHD, are generated. The RG pulse has programmable rising and falling edges and can be inverted using the polarity control. The H1 and H2 horizontal clocks have separate programmable rising and falling edges, as well as separate polarity control. The AD9974 provides additional HCLK-mode programmability, as described in Table 9.

The edge location registers are each six bits wide, allowing the selection of all 64 edge locations. Figure 21 shows the default timing locations for all of the high speed clock signals.
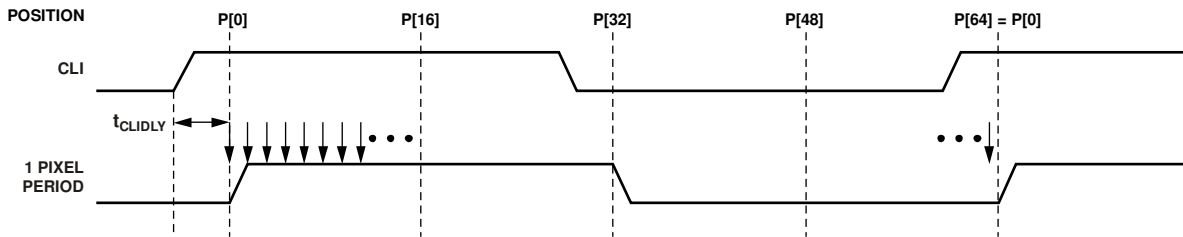
NOTES
1. THE PIXEL CLOCK PERIOD IS DIVIDED INTO 64 POSITIONS, PROVIDING FINE EDGE RESOLUTION FOR HIGH SPEED CLOCKS.
2. THERE IS A FIXED DELAY FROM THE CLI INPUT TO THE INTERNAL PIXEL PERIOD POSITION (t_{CLIDLY}).

Figure 17. High Speed Clock Resolution from CLI Master Clock Input
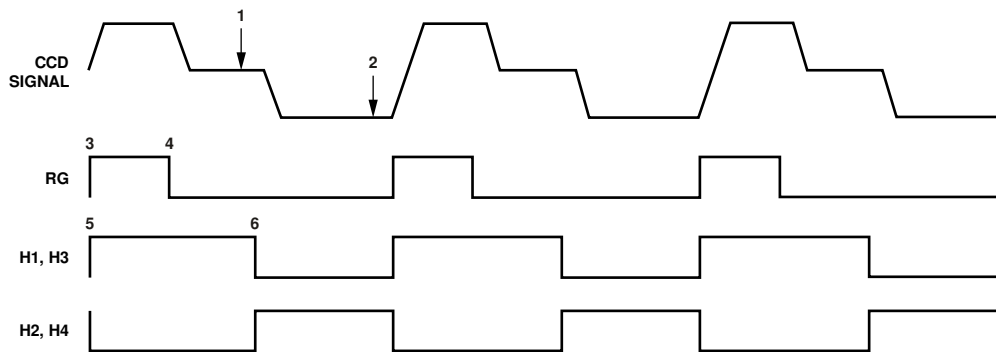
PROGRAMMABLE CLOCK POSITIONS:
[1]SHP SAMPLE LOCATION.
[2]SHD SAMPLE LOCATION.
[3]RG RISING EDGE.
[4]RG FALLING EDGE.
[5]H1 RISING EDGE.
[6]H1 FALLING EDGE.

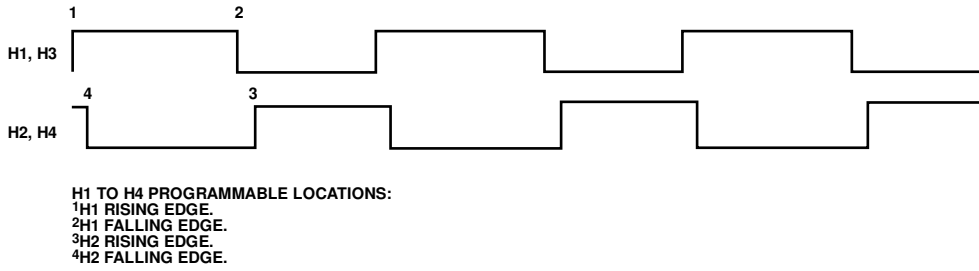*Figure 18. High Speed Clock Programmable Locations (HCLK Mode 1)*

H1 TO H4 PROGRAMMABLE LOCATIONS:
[1]H1 RISING EDGE.
[2]H1 FALLING EDGE.
[3]H2 RISING EDGE.
[4]H2 FALLING EDGE.

Figure 19. HCLK Mode 2 Operation

H1 TO H4 PROGRAMMABLE LOCATIONS:
[1]H1 RISING EDGE.
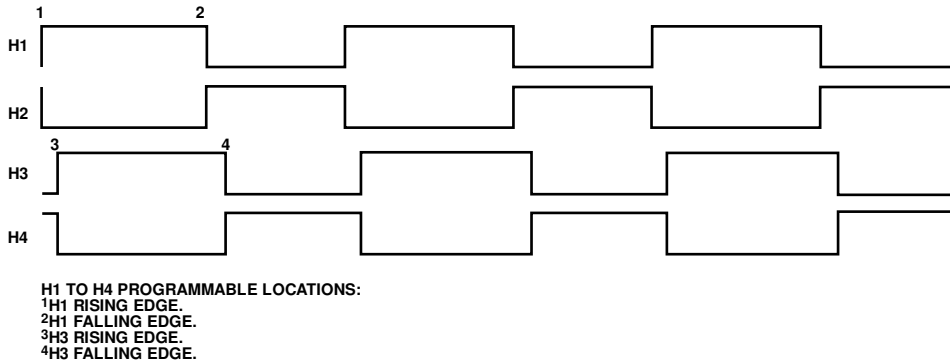[2]H1 FALLING EDGE.
[3]H3 RISING EDGE.
[4]H3 FALLING EDGE.

Figure 20. HCLK Mode 3 Operation
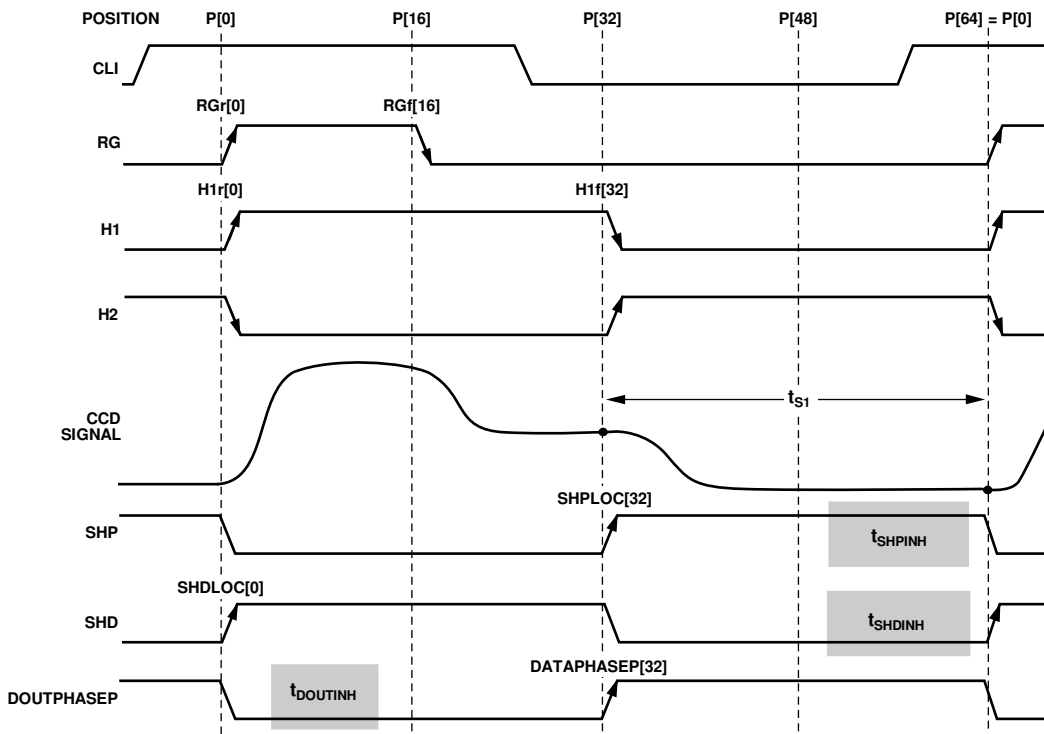
NOTES
1. ALL SIGNAL EDGES ARE FULLY PROGRAMMABLE TO ANY OF THE 64 POSITIONS WITHIN ONE PIXEL PERIOD.
   TYPICAL POSITIONS FOR EACH SIGNAL ARE SHOWN. HCLK MODE 1 IS SHOWN.
2. CERTAIN POSITIONS SHOULD BE AVOIDED FOR EACH SIGNAL, SHOWN ABOVE AS INHIBIT REGIONS.
3. IF A SETTING IN THE INHIBIT REGION IS USED, AN UNSTABLE PIXEL SHIFT CAN OCCUR IN THE HBLK LOCATION OR AFE PIPELINE.

Figure 21. High Speed Timing Default Locations

Table 9. HCLK Modes, Selected by HCLKMODE Register (Address 0x23[7:5])

HCLK Mode	Register Value	Description
Mode 1	001	H1 edges are programmable, with H3 = H1 and H2 = H4 = inverse of H1.
Mode 2	010	H1 edges are programmable, with H3 = H1. H2 edges are programmable, with H4 = H2.
Mode 3	100	H1 edges are programmable, with H2 = inverse of H1. H3 edges are programmable, with H4 = inverse of H3.
Invalid Selection	000, 011, 101, 110, 111	Invalid register settings.

Table 10. H1, H2, RGCONTROL, DRVCONTROL, and SAMPCONTROL Register Parameters

Parameter	Length (Bits)	Range	Description
Polarity	1	High/low	Polarity control for H1/H3 and RG. 0 = no inversion. 1 = inversion.
Positive Edge	6	0 to 63 edge location	Positive edge location for H1/H3 and RG.
Negative Edge	6	0 to 63 edge location	Negative edge location for H1/H3 and RG.
Sample Location	6	0 to 63 sample location	Sampling location for SHP and SHD.
Drive Control	3	0 to 7 current steps	Drive current for H1 to H4 and RG outputs, 0 to 7 steps of 4.3 mA each.

NOTES
1. EXAMPLE SHOWN FOR SHDLOC = 0.
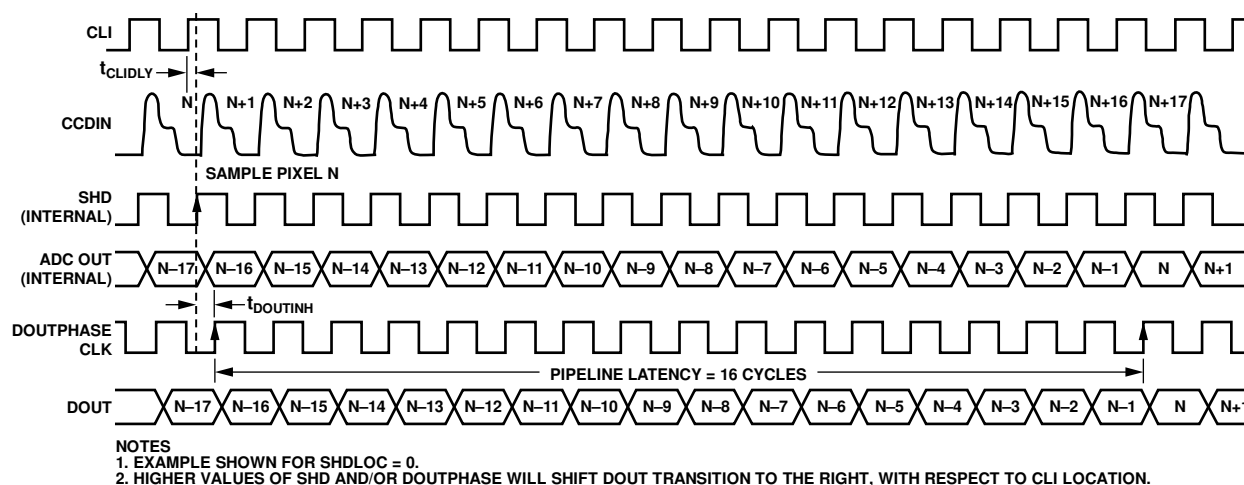2. HIGHER VALUES OF SHD AND/OR DOUTPHASE WILL SHIFT DOUT TRANSITION TO THE RIGHT, WITH RESPECT TO CLI LOCATION.

Figure 22. Pipeline Delay of AFE Data Outputs

H-Driver and RG Outputs

In addition to the programmable timing positions, the AD9974 features on-chip output drivers for the RG and H1 to H4 outputs. These drivers are powerful enough to drive the CCD inputs directly. The H-driver and RG-driver current can be adjusted for optimum rise/fall time into a particular load by using the drive strength control registers (Address 0x35). Use the register to adjust the drive strength in 4.3 mA increments. The minimum setting of 0 is equal to off or three-state, and the maximum setting of 7 is equal to 30.1 mA.

Digital Data Outputs

For maximum system flexibility, the AD9974 uses the DOUTPHASE registers (Address 0x37[11:0]) to select the location for the start of each new pixel data value. Any edge location from 0 to 63 can be programmed. These registers determine the start location of the data output and the DCLK rising edge with respect to the master clock input, CLI_X.

The pipeline delay through the AD9974 is shown in Figure 22. After the CCD input is sampled by SHD, there is a 16-cycle delay until the data is available.

HORIZONTAL CLAMPING AND BLANKING

The horizontal clamping and blanking pulses of the AD9974 are fully programmable to suit a variety of applications. Individual control is provided for CLPOB, PBLK, and HBLK during the different regions of each field. This allows the dark pixel clamping and blanking patterns to be changed at each stage of the readout to accommodate different image transfer timing and high speed line shifts.

Individual CLPOB and PBLK Patterns

The AFE horizontal timing consists of CLPOB and PBLK, as shown in Figure 23. These two signals are programmed independently using the registers in Table 11. The start polarity for the CLPOB or PBLK signal is CLPOB_POL (PBLK_POL), and the first and second toggle positions of the pulse are CLPOB_TOG1 (PBLK_TOG1) and CLPOB_TOG2 (PBLK_TOG2). Both signals are active low and need to be programmed accordingly.

Two separate patterns for CLPOB and PBLK can be programmed for each H-pattern, CLPOB0, CLPOB1, PBLK0, and PBLK1. The CLPOB_PAT and PBLK_PAT field registers select which of the two patterns is used in each field.

Figure 34 shows how the sequence change positions divide the readout field into different regions. By assigning a different H-pattern to each region, the CLPOB and PBLK signals can change with each change in the vertical timing.

CLPOB and PBLK Masking Area

Additionally, the AD9974 allows the CLPOB and PBLK signals to be disabled during certain lines in the field without changing any of the existing pattern settings. There are three sets of start and end registers for both CLPOB and PBLK that allow the creation of up to three masking areas for each signal.

For example, to use the CLPOB masking, program the CLPOBMASKSTART and CLPOBMASKEND registers to specify the starting and ending lines in the field where the CLPOB patterns are to be ignored. Figure 24 illustrates this feature.

The masking registers are not specific to a certain H-pattern; they are always active for any existing field of timing. To disable the CLPOB and PBLK masking feature, set these registers to the maximum value of 0x1FFF.

Note that to disable CLPOB and PBLK masking during power-up, it is recommended that CLPOBMASKSTART (PBLKMASKSTART) be set to 8191 and CLPOBMASKEND (PBLKMASKEND) be set to 0. This prevents any accidental masking caused by different register update events.
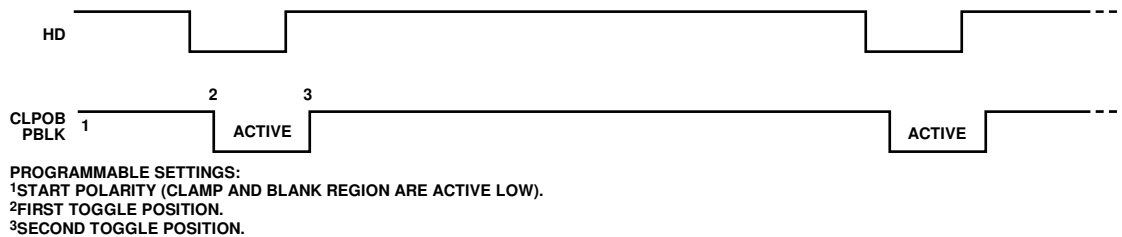

PROGRAMMABLE SETTINGS:
[1]START POLARITY (CLAMP AND BLANK REGION ARE ACTIVE LOW).
[2]FIRST TOGGLE POSITION.
[3]SECOND TOGGLE POSITION.

Figure 23. Clamp and Preblank Pulse Placement
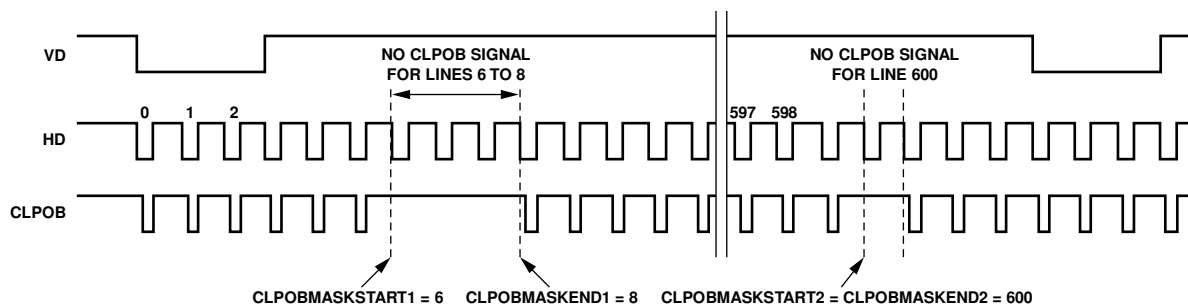
Figure 24. CLPOB Masking Example

Table 11. CLPOB and PBLK Pattern Registers

| Parameter	Length (Bits)	Range	Description
CLPOB0_TOG1	13	0 to 8191 pixel location	First CLPOB0 toggle position within the line for each V-sequence.
CLPOB0_TOG2	13	0 to 8191 pixel location	Second CLPOB0 toggle position within the line for each V-sequence.
CLPOB1_TOG1	13	0 to 8191 pixel location	First CLPOB1 toggle position within the line for each V-sequence.
CLPOB1_TOG2	13	0 to 8191 pixel location	Second CLPOB1 toggle position within the line for each V-sequence.
CLPOB_POL	9	High/low	Starting polarity of CLPOB for each V-sequence [8:0] (in field registers).
CLPOB_PAT	9	0 to 9 settings	CLPOB pattern selection for each V-sequence [8:0] (in field registers).
CLPOBMASKSTART	13	0 to 8191 pixel location	CLPOB mask start position: three values available (in field registers).
CLPOBMASKEND	13	0 to 8191 pixel location	CLPOB mask end position: three values available (in field registers).
PBLK0_TOG1	13	0 to 8191 pixel location	First PBLK0 toggle position within the line for each V-sequence.
PBLK0_TOG2	13	0 to 8191 pixel location	Second PBLK0 toggle position within the line for each V-sequence.
PBLK1_TOG1	13	0 to 8191 pixel location	First PBLK1 toggle position within the line for each V-sequence.
PBLK1_TOG2	13	0 to 8191 pixel location	Second toggle position within the line for each V-sequence.
PBLK_POL	9	High/low	Starting polarity of PBLK for each V-sequence [8:0] (in field registers).
PBLK_PAT	9	0 to 9 settings	PBLK pattern selection for each V-sequence [8:0] (in field registers).
PBLKMASKSTART	13	0 to 8191 pixel location	PBLK mask start position: three values available (in field registers).
PBLKMASKEND	13	0 to 8191 pixel location	PBLK mask end position: three values available (in field registers).
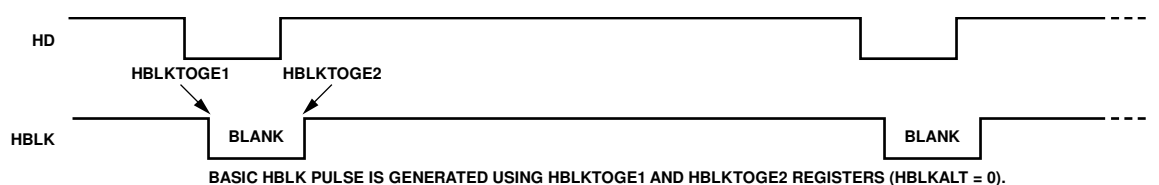
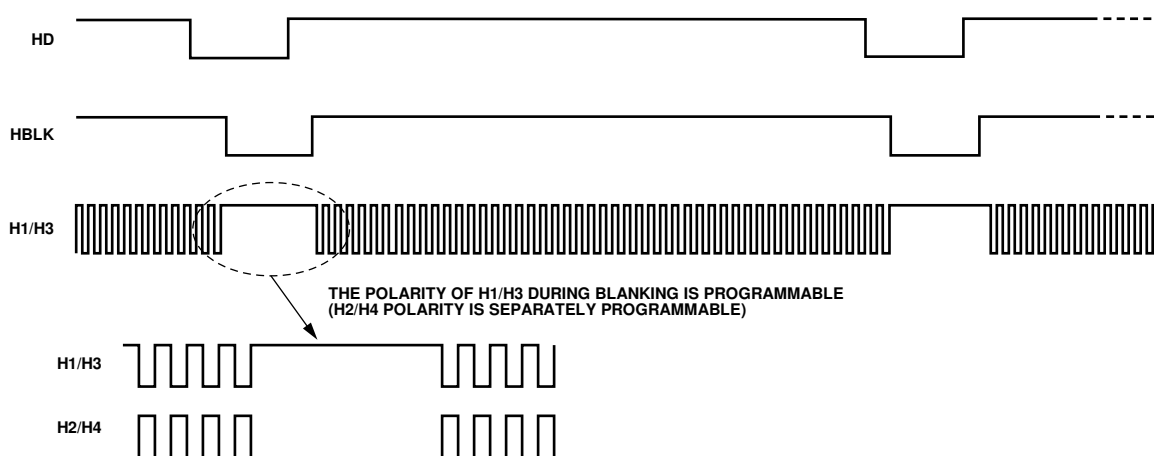Figure 25. Typical Horizontal Blanking Pulse Placement (HBLKMODE = 0)

Figure 26. HBLK Masking Control

AD9974

Individual HBLK Patterns

The HBLK programmable timing shown in Figure 25 is similar to CLPOB and PBLK; however, there is no start polarity control. Only the toggle positions designate the start and the stop positions of the blanking period. Additionally, as shown in Figure 26, there is a polarity control, HBLKMASK, for H1/H3 and H2/H4 that designates the polarity of the horizontal clock signals during the blanking period. Setting HBLKMASK_H1 low sets H1 = H3 = low and HBLKMASK_H2 high sets H2 = H4 = high during the blanking. As with the CLPOB and PBLK signals, HBLK registers are available in each H-pattern group, allowing unique blanking signals to be used with different vertical timing sequences.

The AD9974 supports three modes of HBLK operation. HBLK Mode 0 supports basic operation and provides some support for special HBLK patterns. HBLK Mode 1 supports pixel mixing HBLK operation. HBLK Mode 2 supports advanced HBLK operation. The following sections describe each mode. Register parameters are detailed in Table 12.

HBLK Mode 0 Operation

There are six toggle positions available for HBLK. Normally, only two of the toggle positions are used to generate the standard HBLK interval. However, the additional toggle positions can be used to generate special HBLK patterns, as shown in Figure 27. The pattern in this example uses all six toggle positions to generate two extra groups of pulses during the HBLK interval. By changing the toggle positions, different patterns are created.

Separate toggle positions are available for even and odd lines. If alternation is not needed, load the same values into the registers for even (HBLKTOGE) and odd (HBLKTOGO) lines.
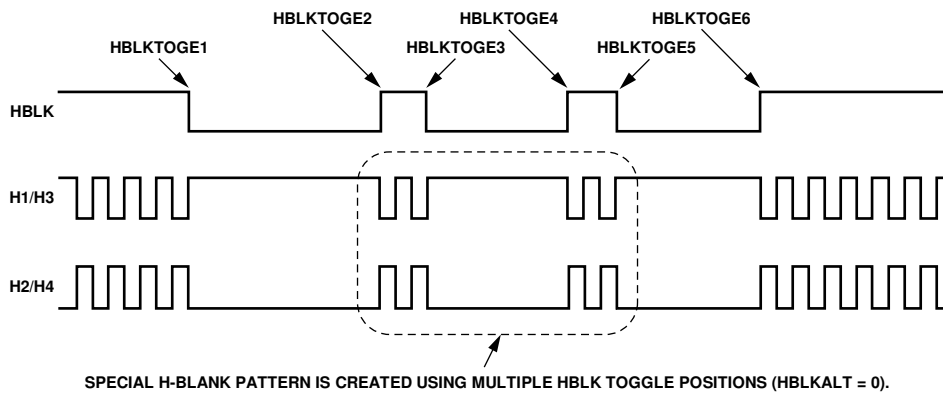

SPECIAL H-BLANK PATTERN IS CREATED USING MULTIPLE HBLK TOGGLE POSITIONS (HBLKALT = 0).

Figure 27. Generating Special HBLK Patterns

Table 12. HBLK Pattern Registers

Register	Length (Bits)	Range	Description
HBLK_MODE	2	0 to 2 HBLK modes	Enables different HBLK toggle position operations.
			0 = normal mode. Six toggle positions available for even and odd lines. If even/odd alternation is not needed, set toggles for even/odd the same.
			1 = pixel mixing mode. In addition to six toggle positions, the HBLKSTART, HBLKEND, HBLKLEN, and HBLKREP registers can be used to generate HBLK patterns. If even/odd alternation is not needed, set toggles for even/odd the same.
			2 = advanced HBLK mode. Divides HBLK interval into six different repeat areas. Uses HBLKSTARTA/B/C and RA*H*REPA/B/C registers.
			3 = test mode only. Do not access.
HBLKSTART	13	0 to 8191 pixel location	Start location for HBLK in HBLK Mode 1 and HBLK Mode 2.
HBLKEND	13	0 to 8191 pixel location	End location for HBLK in HBLK Mode 1 and HBLK Mode 2.
HBLKLEN	13	0 to 8191 pixels	HBLK length in HBLK Mode 1 and HBLK Mode 2.
HBLKREP	13	0 to 8191 repetitions	Number of HBLK repetitions in HBLK Mode 1 and HBLK Mode 2.
HBLKMASK_H1	1	High/low	Masking polarity for H1 and H3 during HBLK.
HBLKMASK_H2	1	High/low	Masking polarity for H2 and H4 during HBLK.

Register	Length (Bits)	Range	Description
HBLKTOGO1	13	0 to 8191 pixel location	First HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO2	13	0 to 8191 pixel location	Second HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO3	13	0 to 8191 pixel location	Third HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO4	13	0 to 8191 pixel location	Fourth HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO5	13	0 to 8191 pixel location	Fifth HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO6	13	0 to 8191 pixel location	Sixth HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE1	13	0 to 8191 pixel location	First HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE2	13	0 to 8191 pixel location	Second HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE3	13	0 to 8191 pixel location	Third HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE4	13	0 to 8191 pixel location	Fourth HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE5	13	0 to 8191 pixel location	Fifth HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE6	13	0 to 8191 pixel location	Sixth HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
RA0H1REPA/B/C	12	0 to 15 HCLK pulses for each A, B, and C	HBLK Repeat Area 0. Number of H1 repetitions for HBLKSTARTA/B/C in HBLK Mode 2 for even lines; odd lines are defined using HBLKALT_PAT. [3:0] RA0H1REPA. Number of H1 pulses following HBLKSTARTA. [7:4] RA0H1REPB. Number of H1 pulses following HBLKSTARTB. [11:8] RA0H1REPC. Number of H1 pulses following HBLKSTARTC.
RA1H1REPA/B/C	12	0 to 15 HCLK pulses	HBLK Repeat Area 1. Number of H1 repetitions for HBLKSTARTA/B/C.
RA2H1REPA/B/C	12	0 to 15 HCLK pulses	HBLK Repeat Area 2. Number of H1 repetitions for HBLKSTARTA/B/C.
RA3H1REPA/B/C	12	0 to 15 HCLK pulses	HBLK Repeat Area 3. Number of H1 repetitions for HBLKSTARTA/B/C.
RA4H1REPA/B/C	12	0 to 15 HCLK pulses	HBLK Repeat Area 4. Number of H1 repetitions for HBLKSTARTA/B/C.
RA5H1REPA/B/C	12	0 to 15 HCLK pulses	HBLK Repeat Area 5. Number of H1 repetitions for HBLKSTARTA/B/C.
RA0H2REPA/B/C	12	0 to 15 HCLK pulses for each A, B, and C	HBLK Repeat Area 0. Number of H2 repetitions for HBLKSTARTA/B/C in HBLK Mode 2 for even lines; odd lines are defined using HBLKALT_PAT. [3:0] RA0H2REPA. Number of H2 pulses following HBLKSTARTA. [7:4] RA0H2REPB. Number of H2 pulses following HBLKSTARTB. [11:8] RA0H2REPC. Number of H2 pulses following HBLKSTARTC.
RA1H2REPA/B/C	12	0 to 15 HCLK pulses	HBLK Repeat Area 1. Number of H2 repetitions for HBLKSTARTA/B/C.
RA2H2REPA/B/C	12	0 to 15 HCLK pulses	HBLK Repeat Area 2. Number of H2 repetitions for HBLKSTARTA/B/C.
RA3H2REPA/B/C	12	0 to 15 HCLK pulses	HBLK Repeat Area 3. Number of H2 repetitions for HBLKSTARTA/B/C.
RA4H2REPA/B/C	12	0 to 15 HCLK pulses	HBLK Repeat Area 4. Number of H2 repetitions for HBLKSTARTA/B/C.
RA5H2REPA/B/C	12	0 to 15 HCLK pulses	HBLK Repeat Area 5. Number of H2 repetitions for HBLKSTARTA/B/C.
HBLKSTARTA	13	0 to 8191 pixel location	HBLK Repeat Area Start Position A for HBLK Mode 2.
HBLKSTARTB	13	0 to 8191 pixel location	HBLK Repeat Area Start Position B for HBLK Mode 2.
HBLKSTARTC	13	0 to 8191 pixel location	HBLK Repeat Area Start Position C for HBLK Mode 2.
HBLKALT_PAT1	3	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 0 pattern, selected from even field. Repeat areas previously defined.
HBLKALT_PAT2	3	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 1 pattern.
HBLKALT_PAT3	3	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 2 pattern.
HBLKALT_PAT4	3	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 3 pattern.
HBLKALT_PAT5	3	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 4 pattern.
HBLKALT_PAT6	3	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 5 pattern.

HBLK Mode 1 Operation

Enable multiple repeats of the HBLK signal by setting HBLK_MODE to 1. In this mode, the HBLK pattern can be generated using a different set of registers: HBLKSTART, HBLKEND, HBLKLEN, and HBLKREP, along with the six toggle positions (see Figure 28).

Separate toggle positions are available for even and odd lines. If alternation is not needed, load the same values into the registers for even (HBLKTOGE) and odd (HBLKTOGO) lines.

Generating HBLK Line Alternation

HBLK Mode 0 and HBLK Mode 1 provide the ability to alternate different HBLK toggle positions on even and odd lines. Separate toggle positions are available for even and odd lines. If even/odd line alternation is not required, load the same values into the registers for even (HBLKTOGE) and odd (HBLKTOGO) lines.

Increasing H-Clock Width During HBLK

HBLK Mode 0 and HBLK Mode 1 allow the H1 to H4 pulse width to be increased during the HBLK interval. As shown in Figure 29, the H-clock frequency can be reduced by a factor of 1/2, 1/4, 1/6, 1/8, 1/10, 1/12, and so on, up to 1/30. To enable this feature, the HCLK_WIDTH register (Address 0x34[7:4]) is set to a value between 1 and 15. When this register is set to 0, the wide HCLK feature is disabled. The reduced frequency occurs only for H1 to H4 pulses that are located within the HBLK area.

The HCLK_WIDTH register is generally used in conjunction with special HBLK patterns to generate vertical and horizontal mixing in the CCD.

Note that the wide HCLK feature is available only in HBLK Mode 0 and HBLK Mode 1, not in HBLK Mode 2.
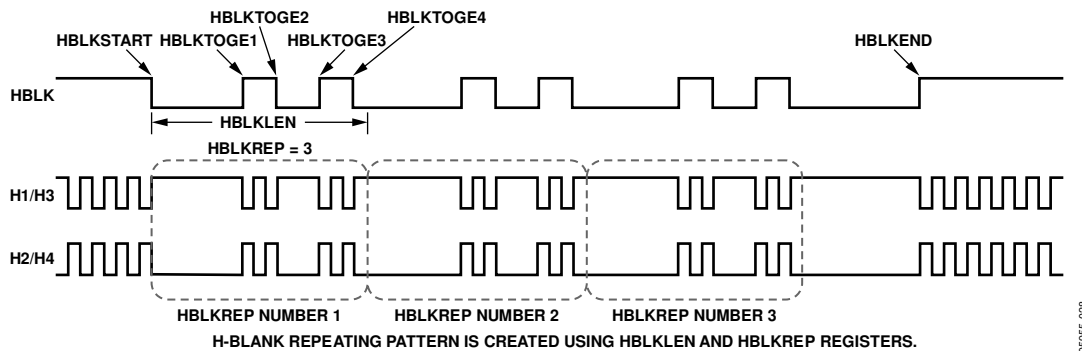
Table 13. HCLK Width Register

Register	Length (Bits)	Description
HCLK_WIDTH	4	Controls H1 to H4 width during HBLK as a fraction of pixel rate.
		0 = same frequency as pixel rate.
		1 = 1/2 pixel frequency, that is, doubles the HCLK pulse width.
		2 = 1/4 pixel frequency.
		3 = 1/6 pixel frequency.
		4 = 1/8 pixel frequency.
		5 = 1/10 pixel frequency.
		…
		15 = 1/30 pixel frequency.

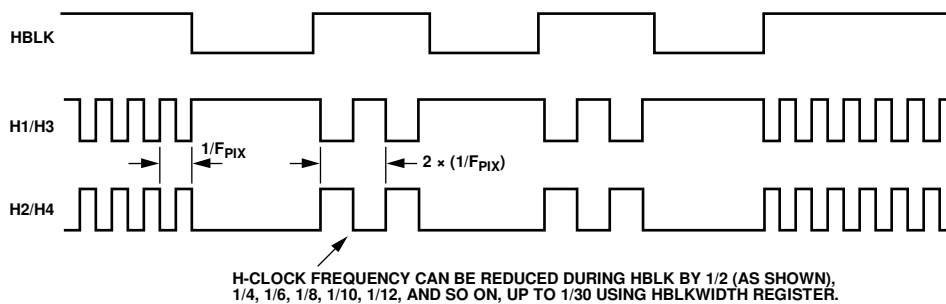Figure 28. HBLK Repeating Pattern Using HBLKMODE = 1

Figure 29. Generating Wide H-Clock Pulses During HBLK Interval

HBLK Mode 2 Operation

HBLK Mode 2 allows more advanced HBLK pattern operation. If unevenly spaced HCLK pulses in multiple areas are needed, HBLK Mode 2 can be used. Using a separate set of registers, HBLK Mode 2 can divide the HBLK region into up to six repeat areas (see Table 12). As shown in Figure 31, each repeat area shares a common group of toggle positions, HBLKSTARTA, HBLKSTARTB, and HBLKSTARTC. However, the number of toggles following each start position can be unique in each repeat area by using the RAH1REP and RAH2REP registers. As shown in Figure 30, setting the RAH1REPA/RAH1REPB/RAH1REPC or RAH2REPA/RAH2REPB/RAH2REPC registers to 0 masks HCLK groups from appearing in a particular repeat area. Figure 31 shows only two repeat areas being used, although six are available. It is possible to program a separate number of repeat area repetitions for H1 and H2, but generally the same value is used for both H1 and H2.

Figure 31 shows the following example:

RA0H1REPA/RA0H1REPB/RA0H1REPC =
RA0H2REPA/RA0H2REPB/RA0H2REPC =
RA1H1REPA/RA1H1REPB/RA1H1REPC =
RA1H2REPA/RA1H2REPB/RA1H2REPC = 2.

Furthermore, HBLK Mode 2 allows a different HBLK pattern on even and odd lines. The HBLKSTARTA, HBLKSTARTB, and HBLKSTARTC registers, as well as the RAH1REPA/RAH1REPB/RAH1REPC and RAH2REPA/RAH2REPB/RAH2REPC registers, define operation for the even lines. For separate control of the odd lines, the HBLKALT_PAT registers specify up to six repeat areas on the odd lines by reordering the repeat areas used for the even lines. New patterns are not available, but the order of the previously defined repeat areas on the even lines can be changed for the odd lines to accommodate advanced CCD operation.
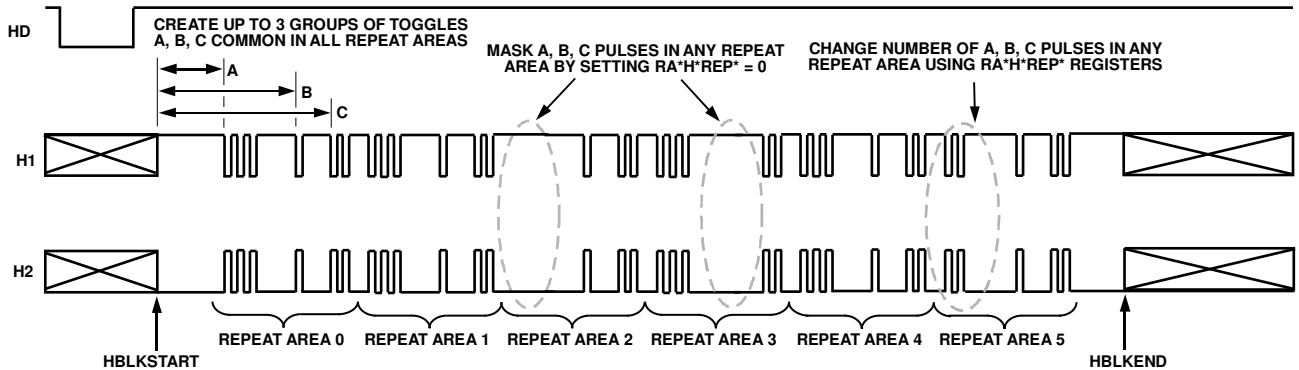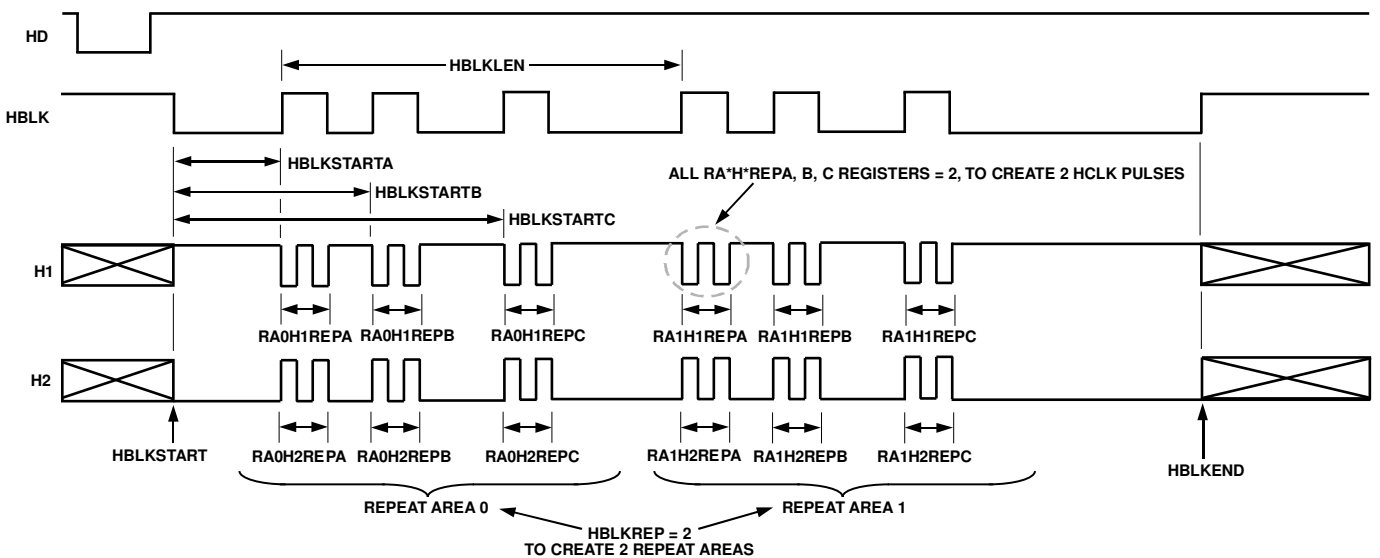

Figure 30. HBLK Mode 2 Operation

Figure 31. HBLK Mode 2 Registers

HBLK, PBLK, and CLPOB Toggle Positions

The AD9974 uses an internal horizontal pixel counter to position the HBLK, PBLK, and CLPOB toggle positions. The horizontal counter does not reset to 0 until 12 CLI periods after the falling edge of HD. This 12-cycle pipeline delay must be considered when determining the register toggle positions. For example, if CLPOB_TOG1 is 100 and the pipeline delay is not considered, the final toggle position is applied at 112. To obtain the correct toggle positions, the toggle position registers must be set to the desired toggle position minus 12.

For example, if the desired toggle position is 100, CLPOB_TOG should be set to 88 (that is, 100 − 12). Figure 49 shows the 12-cycle pipeline delay referenced to the falling edge of HD.

Caution

Toggle positions cannot be programmed during the 12-cycle delay from the HD falling edge until the H-counter has reset. See Figure 33 for an example of this restriction.
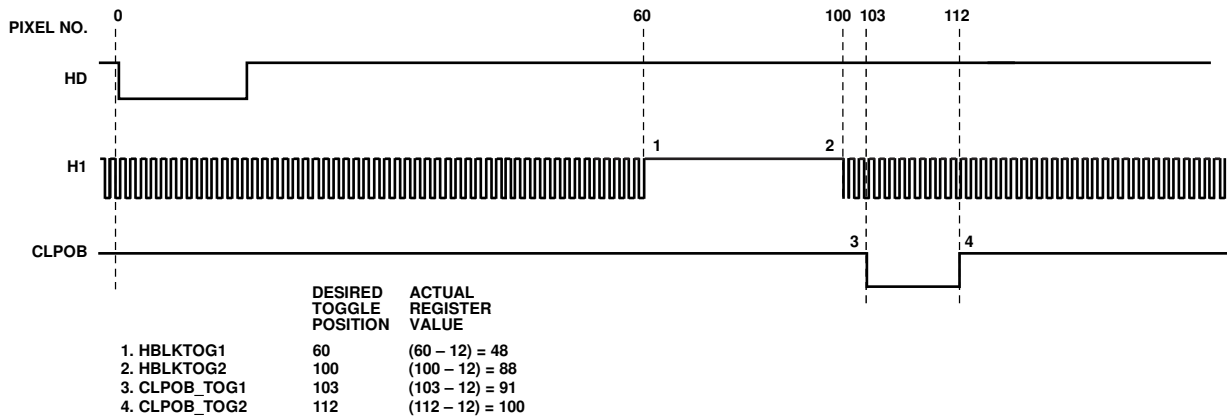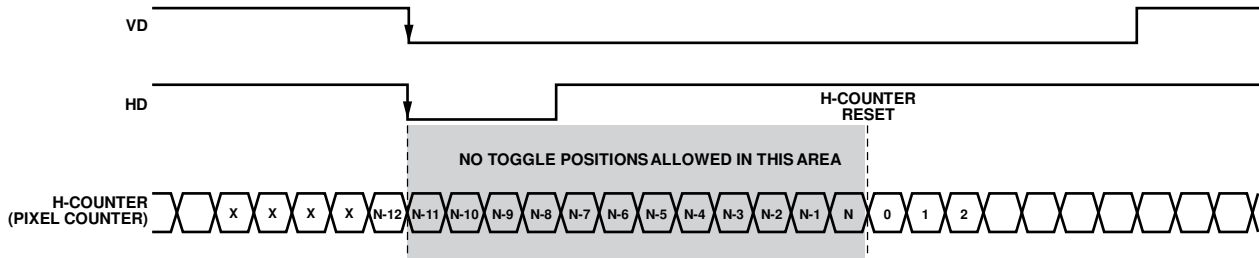

	DESIRED TOGGLE POSITION	ACTUAL REGISTER VALUE
1. HBLKTOG1	60	(60 − 12) = 48
2. HBLKTOG2	100	(100 − 12) = 88
3. CLPOB_TOG1	103	(103 − 12) = 91
4. CLPOB_TOG2	112	(112 − 12) = 100

Figure 32. Example of Register Setting to Obtain Desired Toggle Positions

NOTES
1. TOGGLE POSITIONS CANNOT BE PROGRAMMED WITHIN 12 PIXELS OF PIXEL 0 LOCATION.

Figure 33. Restriction for Toggle Position Placement