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14-Bit, CCD Signal Processor with *Precision Timing* Core

AD9979

FEATURES

1.8 V analog and digital core supply voltage
Correlated double sampler (CDS) with –3 dB, 0 dB, +3 dB, and +6 dB gain
6 dB to 42 dB 10-bit variable gain amplifier (VGA)
14-bit 65 MHz analog-to-digital converter
Black-level clamp with variable level control
Complete on-chip timing generator
***Precision Timing*™ core with 240 ps resolution @ 65 MHz**
On-chip 3 V horizontal and RG drivers
General-purpose outputs (GPOs) for shutter and system support
7 mm × 7 mm, 48-lead LFCSP
Internal LDO regulator circuitry

APPLICATIONS

Professional HDTV camcorders
Professional/high end digital cameras
Broadcast cameras
Industrial high speed cameras

GENERAL DESCRIPTION

The AD9979 is a highly integrated CCD signal processor for high speed digital video camera applications. Specified at pixel rates of up to 65 MHz, the AD9979 consists of a complete analog front end with analog-to-digital conversion, combined with a programmable timing driver. The *Precision Timing* core allows adjustment of high speed clocks with approximately 240 ps resolution at 65 MHz operation.

The analog front end includes black-level clamping, CDS, VGA, and a 65 MSPS, 14-bit analog-to-digital converter (ADC). The timing driver provides the high speed CCD clock drivers for RG, HL, and H1 to H4. Operation is programmed using a 3-wire serial interface.

Available in a space-saving, 7 mm × 7 mm, 48-lead LFCSP, the AD9979 is specified over an operating temperature range of −25°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

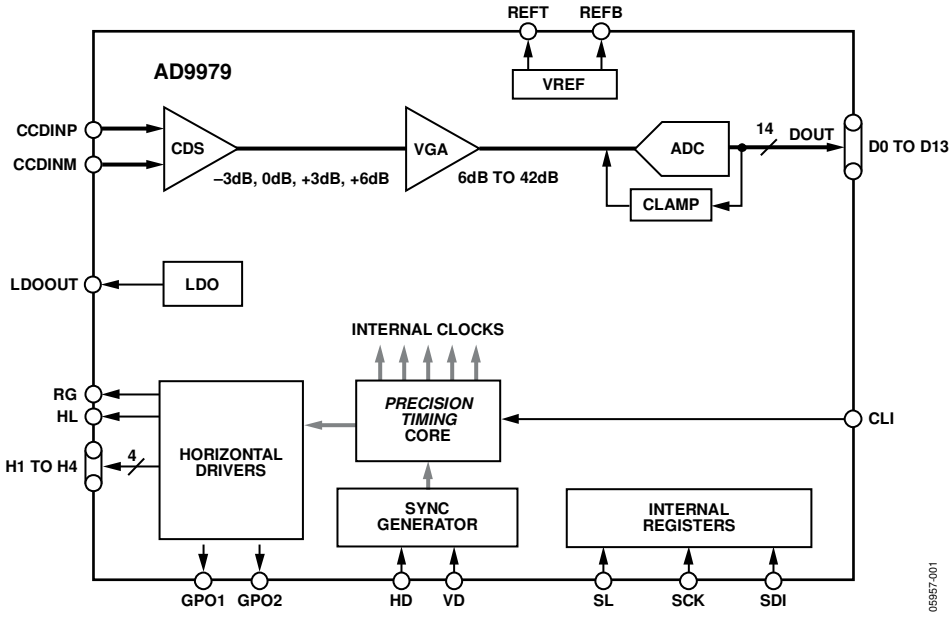

Figure 1.

Rev. C

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DOCUMENTATION

Data Sheet

- AD9979: 14-Bit, CCD Signal Processor with *Precision Timing* Core Data Sheet

DESIGN RESOURCES

- AD9979 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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2/07—Revision Sp0: Initial Version

SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating	−25		+85	°C
Storage	−65		+150	°C
POWER SUPPLY VOLTAGE				
AVDD (AFE, Timing Core)	1.6	1.8	2.0	V
RGVDD (RG, HL Drivers)	2.7	3.3	3.6	V
HVDD (H1 to H4 Drivers)	2.7	3.3	3.6	V
DVDD (Internal Digital Supply)	1.6	1.8	2.0	V
DRVDD (Parallel Data Output Drivers)	1.6	3.0	3.6	V
IOVDD (I/O Supply Without the Use of LDO)	1.6	1.8	3.6	V
POWER SUPPLY CURRENTS—65 MHz OPERATION				
AVDD (1.8 V)		48		mA
RGVDD (3.3 V, 20 pF RG Load, 20 pF HL Load)		8		mA
HVDD[1] (3.3 V, 200 pF Total Load on H1 to H4)		40		mA
DVDD (1.8 V)		13		mA
DRVDD (3.0 V)		4		mA
IOVDD (1.8 V)		2		mA
POWER SUPPLY CURRENTS—STANDBY MODE OPERATION				
Reference Standby		10		mA
Total Shutdown		0.5		mA
LDO[2]				
IOVDD (I/O Supply When Using LDO)	2.5	3.0	3.6	V
Output Voltage	1.8	1.85	1.9	V
Output Current	60			mA
CLOCK RATE (CLI)	8		65	MHz

[1] The total power dissipated by the HVDD (or RGVDD) supply can be approximated using the equation

$$Total\ HVDD\ Power = [C_{LOAD} \times HVDD \times Pixel\ Frequency] \times HVDD$$

where C_{LOAD} is the total capacitance seen by all H outputs.
Reducing the capacitive load and/or reducing the HVDD supply reduces the power dissipation.

[2] LDO can be used to supply AVDD and DVDD only.

TIMING SPECIFICATIONS

C_L = 20 pF, AVDD = DVDD = 1.8 V, f_{CLI} = 65 MHz, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Comments
MASTER CLOCK (CLI)						See Figure 15
CLI Clock Period	t_{CONV}	15.38			ns	
CLI High/Low Pulse Width	t_{ADC}	6.9	7.7	8.9	ns	
Delay from CLI Rising Edge to Internal Pixel Position 0	t_{CLIDLY}		5		ns	
AFE						
SHP Rising Edge to SHD Rising Edge	t_{S1}	6.9	7.7	8.5	ns	See Figure 19
AFE Pipeline Delay			16		Cycles	See Figure 20
CLPOB Pulse Width (Programmable)[1]	t_{COB}	2	20		Pixels	
HD Pulse Width		t_{CONV}			ns	
VD Pulse Width		1 HD period			ns	
SERIAL INTERFACE						See Figure 56
Maximum SCK Frequency	f_{SCLK}	40			MHz	
SL to SCK Setup Time	t_{LS}	10			ns	
SCK to SL Hold Time	t_{LH}	10			ns	
SDATA Valid to SCK Rising Edge Setup	t_{DS}	10			ns	
SCK Rising Edge to SDATA Hold	t_{DH}	10			ns	
H-COUNTER RESET SPECIFICATIONS						See Figure 53
HD Pulse Width		t_{CONV}			ns	
VD Pulse Width		1 HD period			ns	
VD Falling Edge to HD Falling Edge	t_{VDHD}	0		VD period − t_{CONV}	ns	
HD Falling Edge to CLI Rising Edge	t_{HDCLI}	3		t_{CONV} − 2	ns	
CLI Rising Edge to SHPLOC (Internal Sample Edge)	t_{CLISHP}	3		t_{CONV} − 2	ns	
TIMING CORE SETTING RESTRICTIONS						
Inhibited Region for SHP Edge Location[2] (See Figure 19)	t_{SHPINH}	50		64/0		Edge location
Inhibited Region for SHP or SHD with Respect to H-Clocks(See Figure 19)[3, 4, 5, 6]						
RETIME = 0, MASK = 0	t_{SHDINH}	H × NEGLOC − 15		H × NEGLOC − 0		Edge location
RETIME = 0, MASK = 1	t_{SHDINH}	H × POSLOC − 15		H × POSLOC − 0		Edge location
RETIME = 1, MASK = 0	t_{SHPINH}	H × NEGLOC − 15		H × NEGLOC − 0		Edge location
RETIME = 1, MASK = 1	t_{SHPINH}	H × POSLOC − 15		H × POSLOC − 0		Edge location
Inhibited Region for DOUTPHASE Edge Location (See Figure 19)	$t_{DOUTINH}$	SHDLOC + 0		SHDLOC + 15		Edge location

[1] Minimum CLPOB pulse width is for functional operation only. Wider typical pulses are recommended to achieve good clamp performance.
[2] Only applies to slave mode operation. The inhibited area for SHP is needed to meet the timing requirements for t_{CLISHP} for proper H-counter reset operation.
[3] When 0x34[2:0] HxBLKRETIME bits are enabled, the inhibit region for SHD location changes to inhibit region for SHP location.
[4] When sequence register 0x09[23:21] HBLK masking registers are set to 0, the H-edge reference becomes H × NEGLOC.
[5] The H-clock signals that have SHP/SHD inhibit regions depends on the HCLK mode: Mode 1 = H1, Mode 2 = H1, H2, and Mode 3 = H1, H3.
[6] These specifications apply when H1POL, H2POL, RGPOL, and HLPOL are all set to 1 (default setting).

DIGITAL SPECIFICATIONS

IOVDD = 1.6 V to 3.6 V, RGVDD = HVDD = 2.7 V to 3.6 V, C_L = 20 pF, t_{MIN} to t_{MAX}, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
LOGIC INPUTS						
High Level Input Voltage	V_{IH}	IOVDD – 0.6			V	
Low Level Input Voltage	V_{IL}			0.6	V	
High Level Input Current	I_{IH}		10		µA	
Low Level Input Current	I_{IL}		10		µA	
Input Capacitance	C_{IN}		10		pF	
LOGIC OUTPUTS						
High Level Output Voltage	V_{OH}	IOVDD – 0.5			V	I_{OH} = 2 mA
Low Level Output Voltage	V_{OL}			0.5	V	I_{OL} = 2 mA
CLI INPUT (CLI_BIAS = 0)						
High Level Input Voltage	V_{IHCLI}	IOVDD/2 + 0.5			V	
Low Level Input Voltage	V_{ILCLI}			IOVDD/2 – 0.5	V	
H-DRIVER OUTPUTS						
High Level Output Voltage at Maximum Current	V_{OH}	HVDD – 0.5			V	
Low Level Output Voltage at Maximum Current	V_{OL}			0.5	V	
Maximum Output Current (Programmable)			30		mA	
Maximum Load Capacitance		100			pF	

ANALOG SPECIFICATIONS

AVDD = 1.8 V, f_{CLI} = 65 MHz, typical timing specifications, t_{MIN} to t_{MAX}, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CDS[1]					
Allowable CCD Reset Transient		0.5	0.8	V	
CDS Gain Accuracy					
−3.0 dB CDS Gain	−3.7	−3.2	−2.7	dB	
0 dB CDS Gain (Default)	−0.9	−0.4	+0.1	dB	
+3 dB CDS Gain	+1.9	+2.4	+2.9	dB	
+6 dB CDS Gain	+4.3	+4.8	+5.3	dB	
Maximum Input Voltage					VGA gain = 6.3 dB, Code 15 (default value)
−3 dB CDS Gain		1.4		V p-p	
0 dB CDS Gain (Default)		1.0		V p-p	
+3 dB CDS Gain		0.7		V p-p	
+6 dB CDS Gain		0.5		V p-p	
Allowable Optical Black Pixel Amplitude					
0 dB CDS Gain (Default)	−100		+200	mV	
+6 dB CDS Gain	−50		+100	mV	
VARIABLE GAIN AMPLIFIER (VGA)					
Gain Control Resolution		1024		Steps	
Gain Monotonicity		Guaranteed			
Low Gain Setting		6		dB	VGA Code 15 (default)
Maximum Gain Setting		42		dB	VGA Code 1023
BLACK LEVEL CLAMP					
Clamp Level Resolution		1024		Steps	
Minimum Clamp Level (Code 0)		0		LSB	Measured at ADC output
Maximum Clamp Level (Code 1023)		1023		LSB	Measured at ADC output
ANALOG-TO-DIGITAL CONVERTER (ADC)					
Resolution	14			Bits	
Differential Nonlinearity (DNL)	−1.0	± 0.5	+1.2	LSB	
No Missing Codes		Guaranteed			
Integral Nonlinearity (INL)		5	16	LSB	
Full-Scale Input Voltage		2.0		V	
VOLTAGE REFERENCE					
Reference Top Voltage (REFT)		1.4		V	
Reference Bottom Voltage (REFB)		0.4		V	
SYSTEM PERFORMANCE					Specifications include entire signal chain
VGA Gain Accuracy					0 dB CDS gain (default)
Low Gain (Code 15)	5.1	5.6	6.1	dB	Gain = (0.0359 × code) + 5.1 dB
Maximum Gain (Code 1023)	41.3	41.8	42.3	dB	
Peak Nonlinearity, 500 mV Input Signal		0.1	0.4	%	12 dB total gain applied
Total Output Noise		2		LSB rms	AC grounded input, 6 dB gain applied
Power Supply Rejection (PSR)		45		dB	Measured with step change on supply

[1] Input signal characteristics are defined as shown in Figure 2.

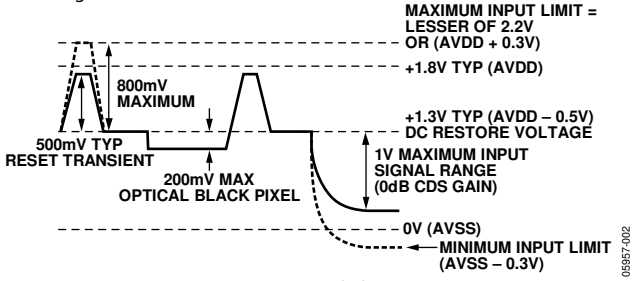


Figure 2. Input Signal Characteristics

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect To	Rating
AVDD	AVSS	−0.3 V to +2.2 V
DVDD	DVSS	−0.3 V to +2.2 V
DRVDD	DRVSS	−0.3 V to +3.9 V
IOVDD	DVSS	−0.3 V to +3.9 V
HVDD	HVSS	−0.3 V to +3.9 V
RGVDD	RGVSS	−0.3 V to +3.9 V
Any VSS	Any VSS	−0.3 V to +0.3 V
RG Output	RGVSS	−0.3 V to RGVDD + 0.3 V
H1 to H4, HL Output	HVSS	−0.3 V to HVDD + 0.3 V
SCK, SL, SDI	DVSS	−0.3 V to IOVDD + 0.3 V
REFT, REFB, CCDINM, CCDINP	AVSS	−0.2 V to AVDD + 0.2 V
Junction Temperature		150°C
Lead Temperature (10 sec)		350°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is measured using a 4-layer printed circuit board (PCB) with the exposed paddle soldered to the board.

Table 6.

Package Type	θ_{JA}	Unit
48-Lead, 7 mm × 7 mm LFCSP	25.8	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

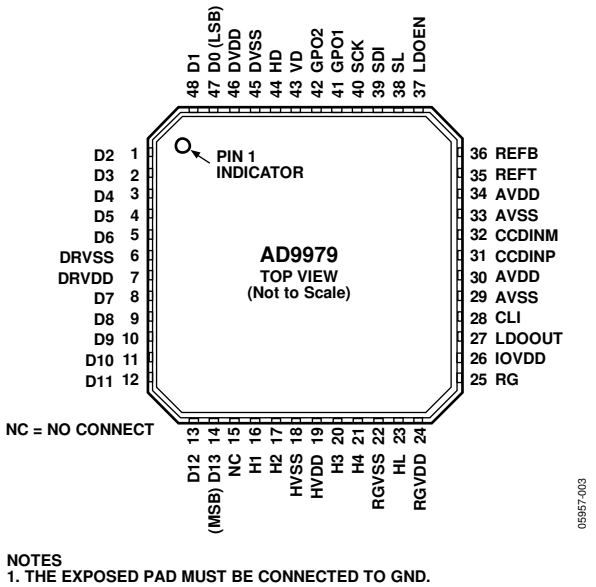


Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	D2	DO	Data Output
2	D3	DO	Data Output
3	D4	DO	Data Output
4	D5	DO	Data Output
5	D6	DO	Data Output
6	DRVSS	P	Digital Driver Ground
7	DRVDD	P	Digital Driver Supply (1.8 V or 3 V)
8	D7	DO	Data Output
9	D8	DO	Data Output
10	D9	DO	Data Output
11	D10	DO	Data Output
12	D11	DO	Data Output
13	D12	DO	Data Output
14	D13 (MSB)	DO	Data Output
15	NC		Not Connected
16	H1	DO	CCD Horizontal Clock 1
17	H2	DO	CCD Horizontal Clock 2
18	HVSS	P	H1 to H4 Driver Ground
19	HVDD	P	H1 to H4 Driver Supply (3 V)
20	H3	DO	CCD Horizontal Clock 3
21	H4	DO	CCD Horizontal Clock 4
22	RGVSS	P	RG Driver Ground
23	HL	DO	CCD Last Horizontal Clock
24	RGVDD	P	RG Driver Supply (3 V)
25	RG	DO	CCD Reset Gate Clock
26	IOVDD	P	Digital I/O Supply (1.8 V or 3 V)/LDO Input Voltage (3 V)
27	LDOOUT	P	LDO Output Voltage (1.8 V)

Pin No.	Mnemonic	Type[1]	Description
28	CLI	DI	Master Clock Input
29	AVSS	P	Analog Ground for AFE
30	AVDD	P	Analog Supply for AFE (1.8 V)
31	CCDINP	AI	CCD Signal Positive Input
32	CCDINM	AI	CCD Signal Negative Input; Normally Tied to AVSS
33	AVSS	P	Analog Ground for AFE
34	AVDD	P	Analog Supply for AFE (1.8 V)
35	REFT	AO	Reference Top Decoupling (Decouple with 1.0 µF to AVSS)
36	REFB	AO	Reference Bottom Decoupling (Decouple with 1.0 µF to AVSS)
37	LDOEN	DI	LDO Output Enable; 3 V = LDO Enabled, GND = LDO Disabled
38	SL	DI	3-Wire Serial Load
39	SDI	DI	3-Wire Serial Data Input
40	SCK	DI	3-Wire Serial Clock
41	GPO1	DIO	General-Purpose Input/Output 1
42	GPO2	DIO	General-Purpose Input/Output 2
43	VD	DI	Vertical Sync Pulse
44	HD	DI	Horizontal Sync Pulse
45	DVSS	P	Digital Ground
46	DVDD	P	Digital Supply (1.8 V)
47	D0 (LSB)	DO	Data Output
48	D1	DO	Data Output
	EPAD		The exposed pad must be connected to GND.

[1] AI = analog input, AO = analog output, DI = digital input, DO = digital output, DIO = digital input/output, P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

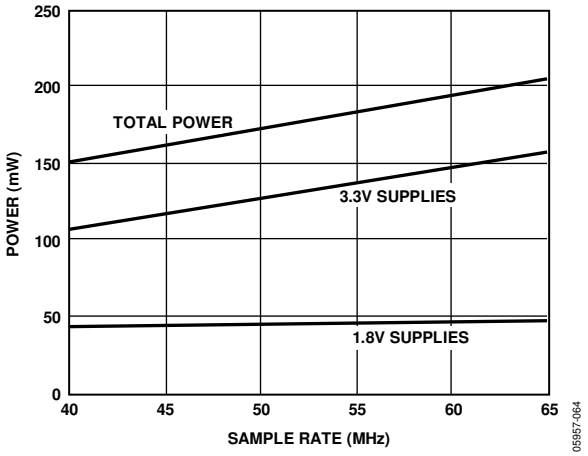


Figure 4. Power vs. Sample Rate

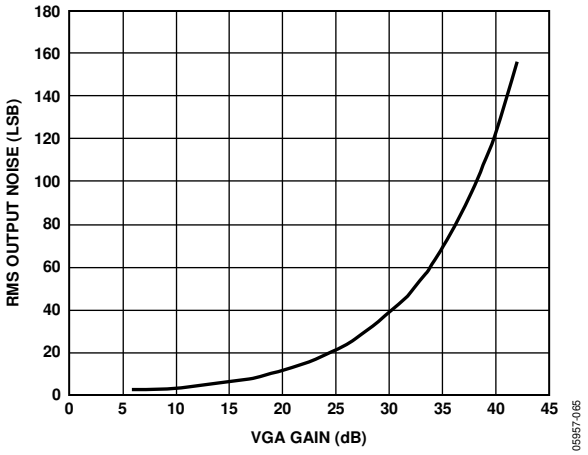


Figure 5. RMS Output Noise vs. VGA Gain

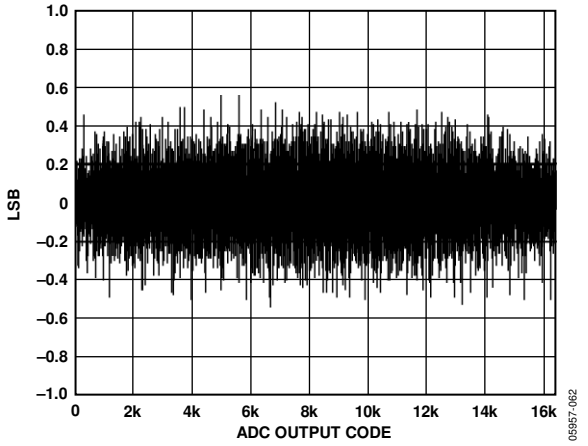


Figure 6. Differential Nonlinearity (DNL)

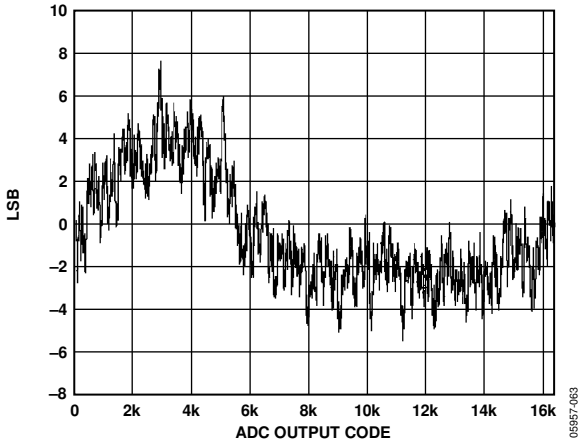


Figure 7. System Integral Nonlinearity (INL)

EQUIVALENT INPUT/OUTPUT CIRCUITS

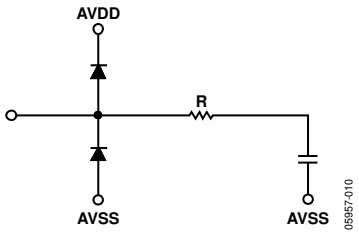


Figure 8. CCD Input

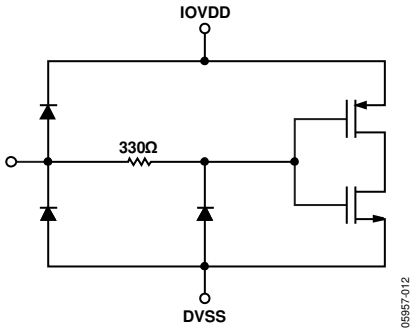


Figure 10. Digital Inputs

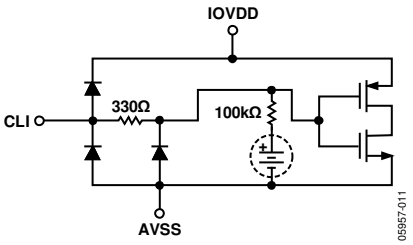


Figure 9. CLI Input, Register 0x15[0] =1 Enables the Bias Circuit

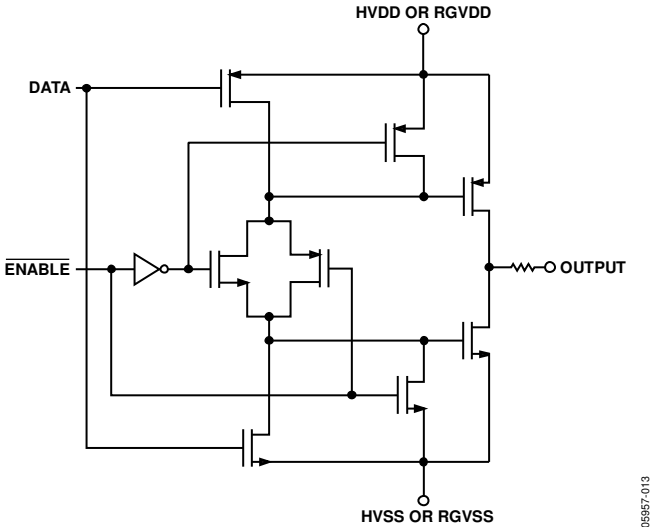


Figure 11. H1 to H4, HL, and RG Outputs

THEORY OF OPERATION

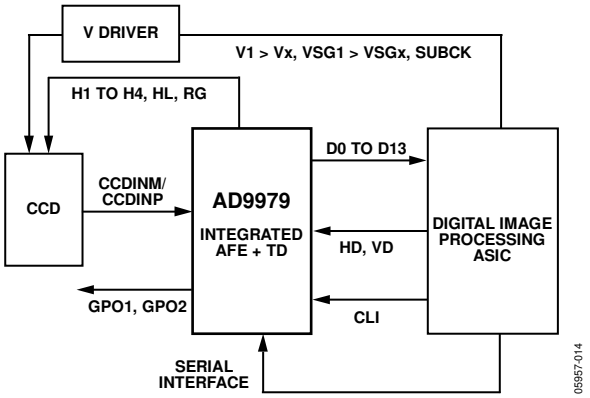


Figure 12. Typical Application

Figure 12 shows the typical application for the AD9979. The CCD output is processed by the AFE circuitry of the AD9979, which consists of a CDS, a VGA, a black-level clamp, and an ADC. The digitized pixel information is sent to the digital image processor chip, which performs the post-processing and compression. To operate the CCD, all CCD timing parameters are programmed into the AD9979 from the system ASIC, through the 3-wire serial interface. From the system master clock, CLI, provided by the image processor or an external crystal, the AD9979 generates the horizontal clocks of the CCD and all internal AFE clocks.

All AD9979 clocks are synchronized with VD and HD inputs. All of the horizontal pulses (CLPOB, PBLK, and HBLK) of the AD9979 are programmed and generated internally.

The H drivers for H1 to H4 and RG are included in the AD9979, allowing these clocks to be directly connected to the CCD. The H-drive voltage of 3 V is supported in the AD9979.

Figure 13 and Figure 14 show the maximum horizontal and vertical counter dimensions for the AD9979.These counters control all internal horizontal and vertical clocking, to specify line and pixel locations. The maximum HD length is 8191 pixels per line, and the maximum VD length is 8192 lines per field.

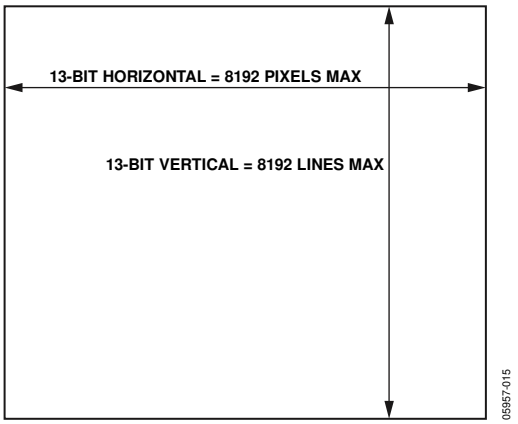


Figure 13. Maximum Dimensions for Vertical and Horizontal Counters

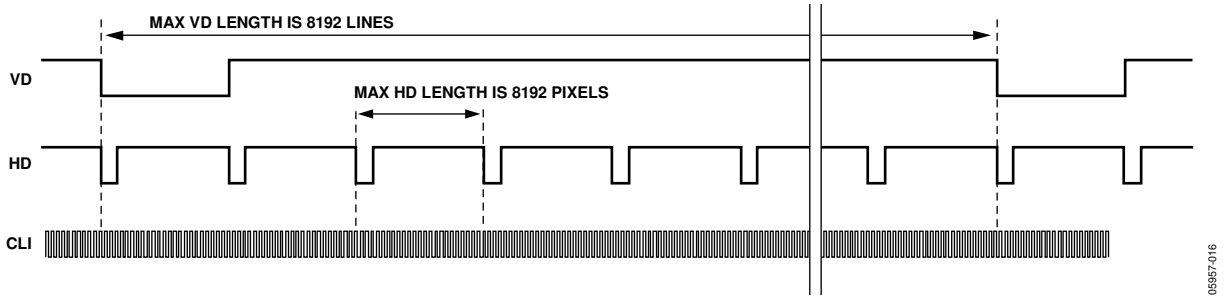


Figure 14. Maximum VD and HD Dimensions

PROGRAMMABLE TIMING GENERATION

PRECISION TIMING HIGH SPEED TIMING CORE

The AD9979 generates flexible high speed timing signals using the *Precision Timing* core. This core is the foundation for generating the timing for both the CCD and the AFE; the reset gate (RG), the HL, Horizontal Driver H1 to Horizontal Driver H4, and the SHP and SHD sample clocks. A unique architecture makes it routine for the system designers to optimize image quality by providing precise control over the horizontal CCD readout and the AFE-correlated double sampling.

Timing Resolution

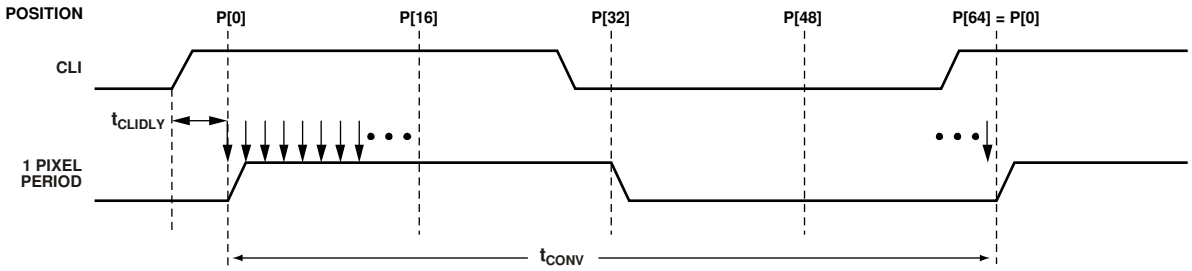
The *Precision Timing* core uses a master clock input (CLI) as a reference. This clock is recommended to be the same as the CCD pixel clock frequency. Figure 15 illustrates how the internal timing core divides the master clock period into 64 steps, or edge positions. Therefore, the edge resolution of the *Precision Timing* core is $t_{CLI}/64$. (For more information on using the CLI input, refer to the Applications Information section.)

Using a 65 MHz CLI frequency, the edge resolution of the *Precision Timing* core is approximately 240 ps. If a 1× system clock is not available, it is also possible to use a 2× reference clock, by programming the CLIDIVIDE register (Address 0x0D). The AD9979 then internally divides the CLI frequency by 2.

High Speed Clock Programmability

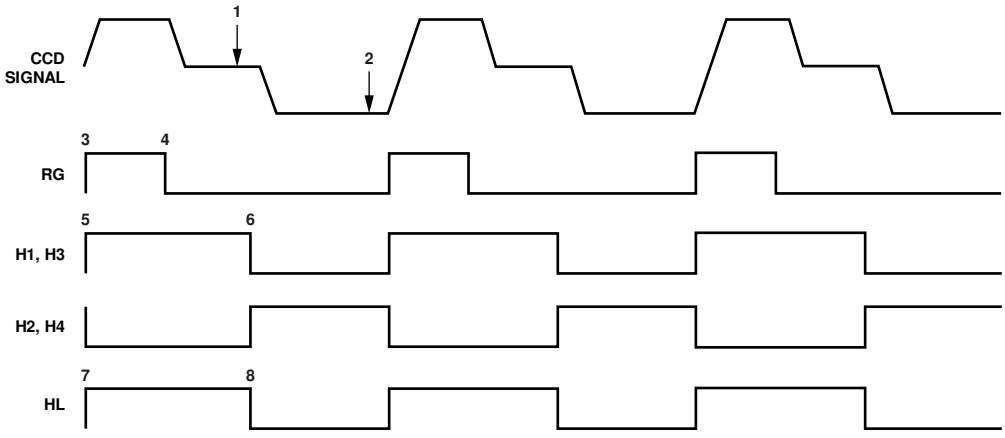
Figure 16 shows how the high speed clocks, RG, HL, H1 to H4, SHP, and SHD, are generated. The RG pulse has programmable rising and falling edges and can be inverted using the polarity control. The HL, H1, and H2 horizontal clocks have separate programmable rising and falling edges and polarity control. The AD9979 provides additional HCLK mode programmability, see Table 8.

The edge location registers are each six bits wide, allowing the selection of all 64 edge locations. Figure 19 shows the default timing locations for all of the high speed clock signals.



NOTES
1. THE PIXEL CLOCK PERIOD IS DIVIDED INTO 64 POSITIONS, PROVIDING FINE EDGE RESOLUTION FOR HIGH SPEED CLOCKS.
2. THERE IS A FIXED DELAY FROM THE CLI INPUT TO THE INTERNAL PIXEL PERIOD POSITION (t_{CLIDLY}).

Figure 15. High Speed Clock Resolution From CLI Master Clock Input



PROGRAMMABLE CLOCK POSITIONS:
[1]SHP SAMPLE LOCATION.
[2]SHD SAMPLE LOCATION.
[3]RG RISING EDGE.
[4]RG FALLING EDGE.
[5]H1 RISING EDGE.
[6]H1 FALLING EDGE.
[7]HL RISING EDGE.
[8]HL FALLING EDGE.

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Figure 16. High Speed Clock Programmable Locations (HCLKMODE = 1)

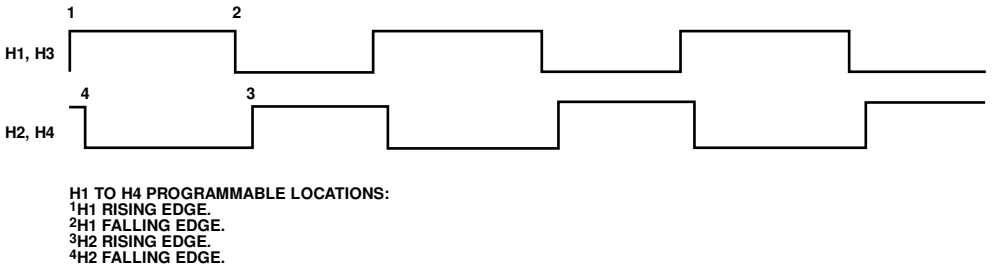

Figure 17. HCLK Mode 2 Operation

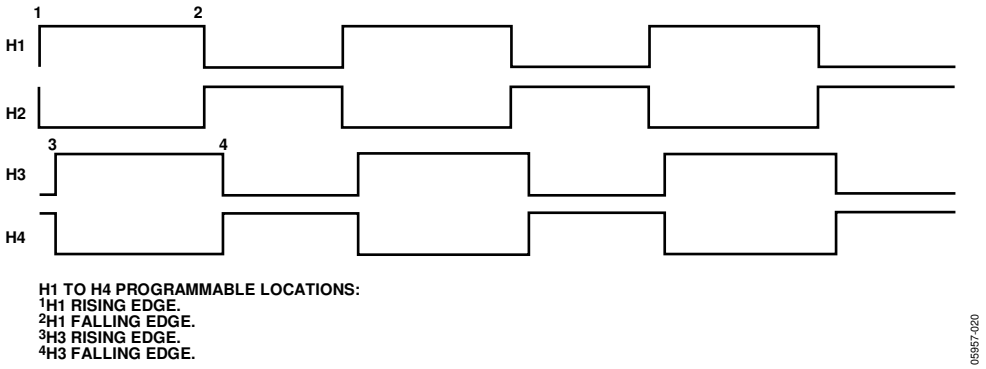

Figure 18. HCLK Mode 3 Operation

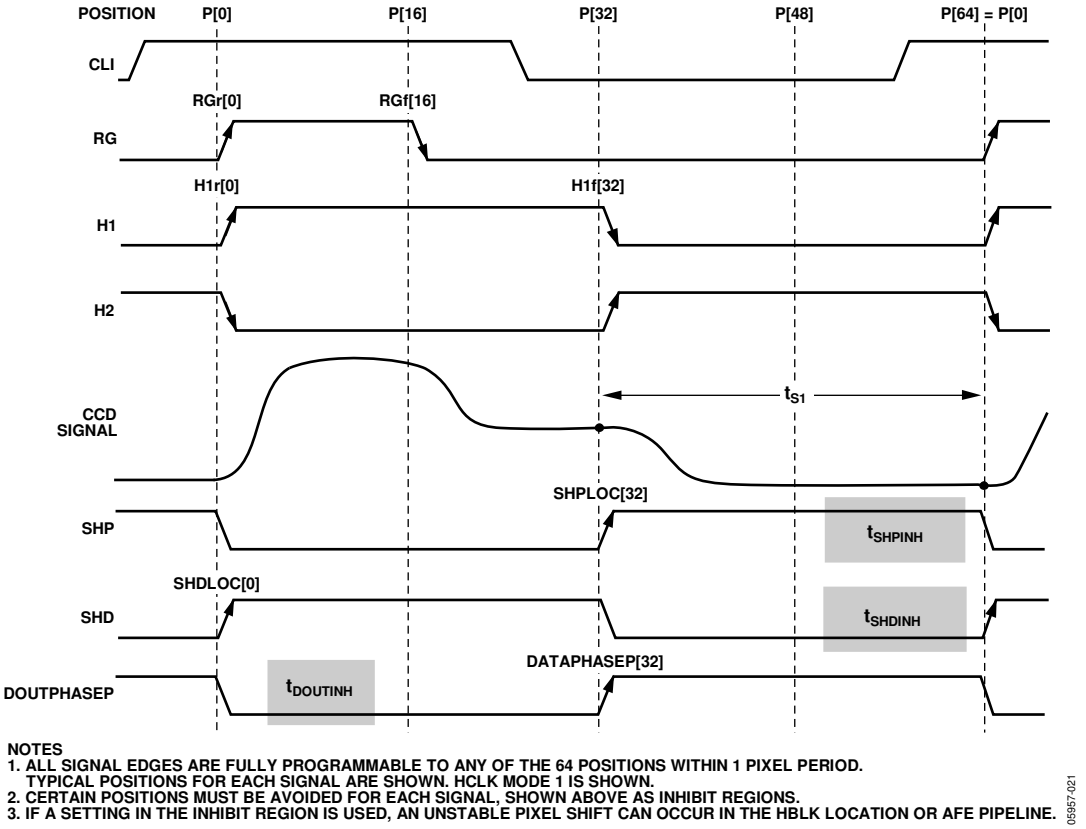

Figure 19. High Speed Timing Default Locations

Table 8. HCLK Modes (Selected by Register Address 0x23, Bits[7:5])

HCLK Mode	Register Value	Description
Mode 1	001	H1 edges are programmable; H3 = H1, H2 = H4 = inverse of H1.
Mode 2	010	H1 edges are programmable; H3 = H1. H2 edges are programmable; H4 = H2.
Mode 3	100	H1 edges are programmable; H2 = inverse of H1. H3 edges are programmable; H4 = inverse of H3.
Invalid Selection	000, 011, 101, 110, 111	Invalid register settings.

Table 9. Horizontal Clock, RG, Drive, and Sample Control Registers Parameters

Name	Length	Range	Description
Polarity	1 bit	High/low	Polarity control for H1/H3 and RG; 0 = no inversion, 1 = inversion
Positive Edge	6 bits	0 to 63 edge location	Positive edge location for H1/H3 and RG
Negative Edge	6 bits	0 to 63 edge location	Negative edge location for H1/H3 and RG
Sample Location	6 bits	0 to 63 sample location	Sampling location for SHP and SHD
Drive Control	3 bits	0 to 7 current steps	Drive current for H1 to H4 and RG outputs (4.3 mA steps)

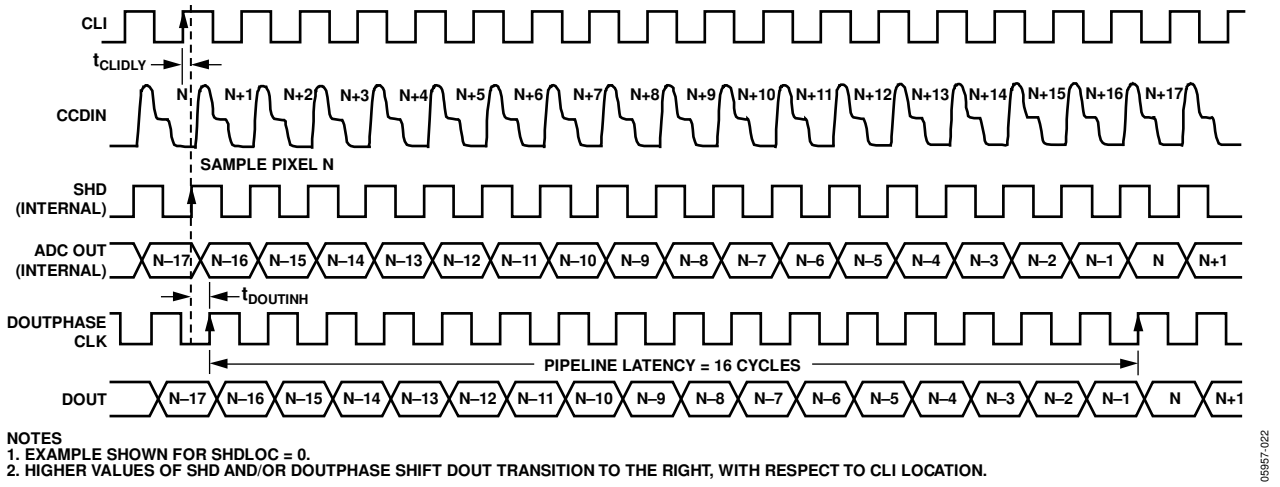

Figure 20. Pipeline Delay of AFE Data Outputs

H-Driver and RG Outputs

In addition to the programmable timing positions, the AD9979 features on-chip output drivers for the HL, RG, and H1 to H4 outputs. These drivers are powerful enough to directly drive the CCD inputs. The H-driver and RG-driver currents can be adjusted for optimum rise/fall times into a particular load by using the drive strength control register (Address 0x35). Use the register to adjust the drive strength in 4.3 mA increments. The minimum setting of 0 is equal to off or three-state, and the maximum setting of 7 is equal to 30.1 mA.

Digital Data Outputs

For maximum system flexibility, the AD9979 uses DOUTPHASEN and DOUTPHASEP (Address 0x37, Bits[11:0]) to select the location for the start of each new pixel data value. Any edge location from 0 to 63 can be programmed. Register 0x37 determines the start location of the data output and the DOUTPHASEx clock rising edge with respect to the master clock input CLI.

The pipeline delay through the AD9979 is shown in Figure 20. After the CCD input is sampled by SHD, there is a 16-cycle delay before the data is available.

HORIZONTAL CLAMPING AND BLANKING

The horizontal clamping and blanking pulses of the AD9979 are fully programmable to suit a variety of applications. Individual control is provided for CLPOB, PBLK, and HBLK during the different regions of each field. This allows the dark-pixel clamping and blanking patterns to be changed at each stage of the readout to accommodate the different image transfer timing and high speed line shifts.

Individual CLPOB and PBLK Patterns

The AFE horizontal timing consists of CLPOB and PBLK, as shown in Figure 21. These two signals are independently programmed using the registers in Table 10. The start polarity for the CLPOB (PBLK) signal is CLPOB_POL (PBLK_POL), and the first and second toggle positions of the pulse are CLPOBx_TOG1 (PBLKx_TOG1) and CLPOBx_TOG2 (PBLKx_TOG2), respectively. Both signals are active low and need to be programmed accordingly.

Two separate patterns for CLPOB and PBLK can be programmed for each H-pattern, CLPOB0, CLPOB1, PBLK0, and PBLK1. The CLPOB_PAT and PBLK_PAT field registers select which of the two patterns are used in each field.

Figure 32 shows how the sequence change positions divide the readout field into different regions. By assigning a different H-pattern to each region, the CLPOB and PBLK signals can change with each change in the vertical timing.

CLPOB and PBLK Masking Area

Additionally, the AD9979 allows the CLPOB and PBLK signals to be disabled during certain lines in the field, without changing any of the existing pattern settings. There are three sets of start and end registers for both CLPOB and PBLK that allows the creation of up to three masking areas for each signal.

For example, to use the CLPOB masking, program the CLPOBMASKSTARTx and CLPOBMASKENDx registers to specify the starting and ending lines in the field where the CLPOB patterns are to be ignored. Figure 22 illustrates this feature.

The masking registers are not specific to a certain H-pattern; they are always active for any existing field of timing. To disable the CLPOB and PBLK masking feature, set these registers to the maximum value of 0x1FFF.

Note that to disable CLPOB and PBLK masking during power-up, it is recommended to set CLPOBMASKSTARTx (PBLKMASKSTARTx) to 8191 and CLPOBMASKENDx (PBLKMASKENDx) to 0. This prevents any accidental masking caused by different register update events.

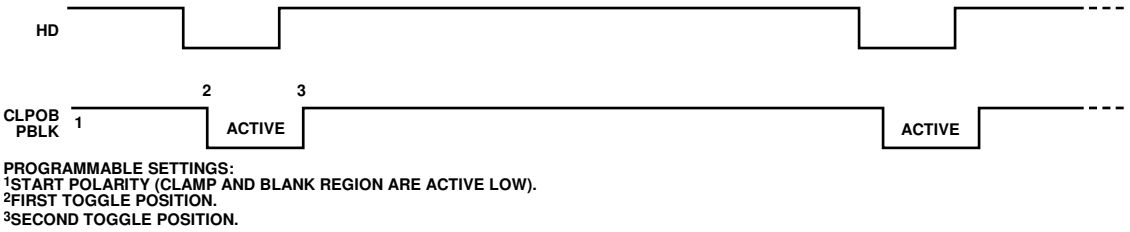

Figure 21. Clamp and Preblank Pulse Placement

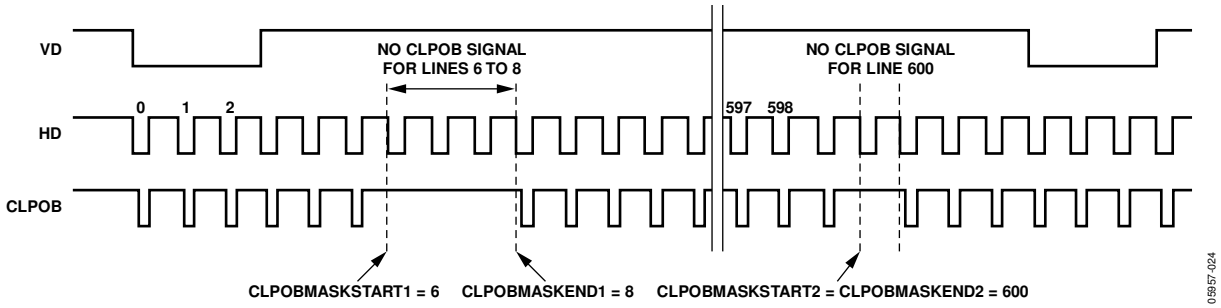

Figure 22. CLPOB Masking Example

Table 10. CLPOB and PBLK Registers

Name	Length	Range	Description
CLPOB0_TOG1	13 bits	0 to 8191 pixel location	First CLPOB0 toggle position within the line for each V-sequence.
CLPOB0_TOG2	13 bits	0 to 8191 pixel location	Second CLPOB0 toggle position within the line for each V-sequence.
CLPOB1_TOG1	13 bits	0 to 8191 pixel location	First CLPOB1 toggle position within the line for each V-sequence.
CLPOB1_TOG2	13 bits	0 to 8191 pixel location	Second CLPOB1 toggle position within the line for each V-sequence.
CLPOB_POL	9 bits	High/low	Starting polarity of CLPOB for each V-sequence[8:0] (in field registers).
CLPOB_PAT	9 bits	0 to 9 settings	CLPOB pattern selection for each V-sequence[8:0] (in field registers).
CLPOBMASKSTARTx	13 bits	0 to 8191 pixel location	CLPOB mask start position. Three values available (in field registers).
CLPOBMASKENDx	13 bits	0 to 8191 pixel location	CLPOB mask end position. Three values available (in field registers).
PBLK0_TOG1	13 bits	0 to 8191 pixel location	First PBLK0 toggle position within the line for each V-sequence.
PBLK0_TOG2	13 bits	0 to 8191 pixel location	Second PBLK0 toggle position within the line for each V-sequence.
PBLK1_TOG1	13 bits	0 to 8191 pixel location	First PBLK1 toggle position within the line for each V-sequence.
PBLK1_TOG2	13 bits	0 to 8191 pixel location	Second PBLK1 toggle position within the line for each V-sequence.
PBLK_POL	9 bits	High/low	Starting polarity of PBLK for each V-sequence[8:0] (in field registers).
PBLK_PAT	9 bits	0 to 9 settings	PBLK pattern selection for each V-sequence[8:0] (in field registers).
PBLKMASKSTARTx	13 bits	0 to 8191 pixel location	PBLK mask start position. Three values available (in field registers).
PBLKMASKENDx	13 bits	0 to 8191 pixel location	PBLK mask end position. Three values available (in field registers).

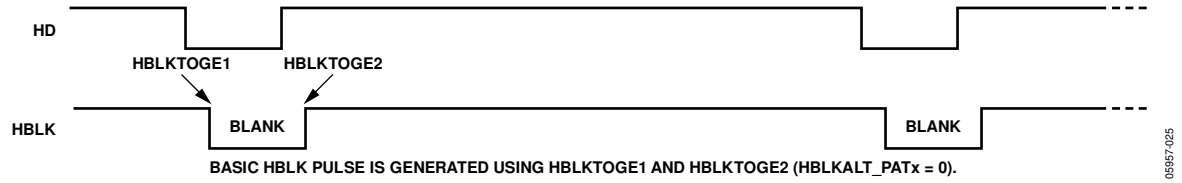

Figure 23. Typical Horizontal Blanking Pulse Placement (HBLKMODE = 0)

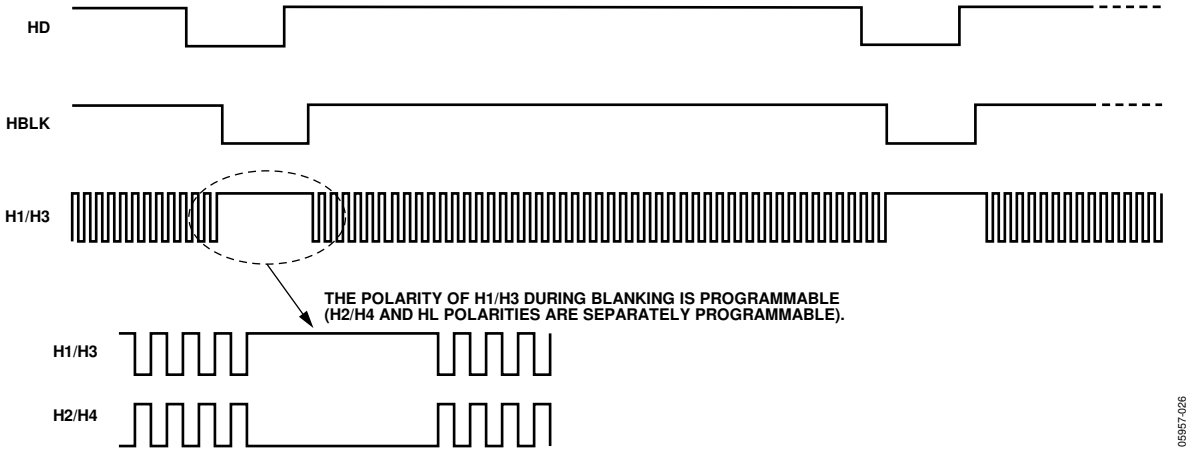

Figure 24. HBLK Masking Control

Individual HBLK Patterns

The HBLK programmable timing shown in Figure 23 is similar to CLPOB and PBLK; however, there is no start polarity control. Only the toggle positions designate the start and the stop positions of the blanking period. Additionally, as shown in Figure 24, there is a polarity control, HBLKMASK, for H1/H3 and H2/H4 that designates the polarity of the horizontal clock signals during the blanking period. Setting HBLKMASK_H1 low sets H1 = H3 = low and HBLKMASK_H2 high sets H2 = H4 = high during the blanking. As with the CLPOB and PBLK signals, HBLK registers are available in each H-pattern group, allowing unique blanking signals to be used with different vertical timing sequences.

The AD9979 supports three different modes for HBLK operation. HBLK Mode 0 supports basic operation and offers some support for special HBLK patterns. HBLK Mode 1 supports pixel mixing HBLK operation. HBLK Mode 2 supports advanced HBLK operation. The following sections describe each mode. Register names are detailed in Table 11.

HBLK Mode 0 Operation

There are six toggle positions available for HBLK. Normally, only two of the toggle positions are used to generate the standard HBLK interval. However, the additional toggle positions can be used to generate special HBLK patterns, as shown in Figure 25. The pattern in this example uses all six toggle positions to generate two extra groups of pulses during the HBLK interval. By changing the toggle positions, different patterns are created.

Separate toggle positions are available for even and odd lines. If alternation is not needed, load the same values into both the HBLKTOGEx and HBLKTOGOx registers.

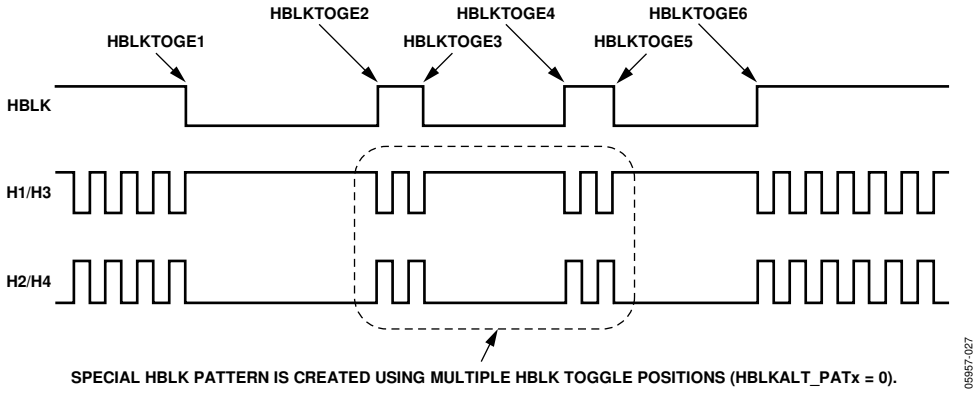

Figure 25. Generating Special HBLK Patterns

Table 11. HBLK Pattern Registers

Name	Length	Range	Description
HBLKMODE	2 bits	0 to 2	Enables different HBLK toggle position operation. 0 = normal mode. Six toggle positions are available for even and odd lines. If even/odd alternation is not need, set the toggle positions for the even/odd the same. 1 = pixel mixing mode. Instead of only six toggle positions, use the HBLKSTART, HBLKEND, HBLKLEN, and HBLKREP registers, along with HBLKTOGOx and HBLKTOGEx. If even/odd alternation is not need, set the even/odd toggles the same. 2 = advanced HBLK mode. It divides HBLK interval into six different repeat areas. It uses HBLKSTARTA, HBLKSTARTB, HBLKSTARTC, and RAxHyREPA/RAxHyREPB/RAxHyREPC registers. 3 = test mode. Do not access.
HBLKSTART	13 bits	0 to 8191 pixel location	Start location for HBLK in HBLK Mode 1 and HBLK Mode 2.
HBLKEND	13 bits	0 to 8191 pixel location	End location for HBLK in HBLK Mode 1 and HBLK Mode 2.
HBLKLEN	13 bits	0 to 8191 pixels	HBLK length in HBLK Mode 1 and HBLK Mode 2.
HBLKREP	13 bits	0 to 8191 repetitions	Number of HBLK repetitions in HBLK Mode 1 and HBLK Mode 2.
HBLKMASK_H1	1 bit	High/low	Masking polarity for H1/H3 during HBLK.
HBLKMASK_H2	1 bit	High/low	Masking polarity for H2/H4 during HBLK.
HBLKMASK_HL	1 bit	High/low	Masking polarity for HL during HBLK.

Name	Length	Range	Description
HBLKTOGO1	13 bits	0 to 8191 pixel location	First HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO2	13 bits	0 to 8191 pixel location	Second HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO3	13 bits	0 to 8191 pixel location	Third HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO4	13 bits	0 to 8191 pixel location	Fourth HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO5	13 bits	0 to 8191 pixel location	Fifth HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO6	13 bits	0 to 8191 pixel location	Sixth HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE1	13 bits	0 to 8191 pixel location	First HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE2	13 bits	0 to 8191 pixel location	Second HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE3	13 bits	0 to 8191 pixel location	Third HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE4	13 bits	0 to 8191 pixel location	Fourth HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE5	13 bits	0 to 8191 pixel location	Fifth HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1
HBLKTOGE6	13 bits	0 to 8191 pixel location	Sixth HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
RAxHyREPz[1]	12 bits	0 to 15 HCLK pulses	HBLK Mode 2 even field Repeat Area x. Number of Hy repetitions for HBLKSTARTz even lines.[2] Bits[3:0]: number of Hy pulses following HBLKSTARTA. Bits[7:4]: number of Hy pulses following HBLKSTARTB. Bits[11:8]: number of Hy pulses following HBLKSTARTC.
HBLKSTARTA	13 bits	0 to 8191 pixel location	HBLK Repeat Area Start Position A for HBLK Mode 2.
HBLKSTARTB	13 bits	0 to 8191 pixel location	HBLK Repeat Area Start Position B for HBLK Mode 2.
HBLKSTARTC	13 bits	0 to 8191 pixel location	HBLK Repeat Area Start Position C for HBLK Mode 2.
HBLKALT_PATx[3]	3 bits	0 to 5 even repeat area	HBLK Mode 2 odd field Repeat Area x pattern. Selected from even field repeat areas.[4]

[1] The variable x represents the repeat area, from 0 to 5. The variable y represents the horizontal driver, 1 or 2. The variable z represents the HBLK repeat area start position for HBLK Mode 2, A, B, or C.
[2] Odd lines defined using HBLKALT_PATx.
[3] The variable x represents the repeat area, from 0 to 5.
[4] Even lines defined using RAxHyREPz; also see Note 1.

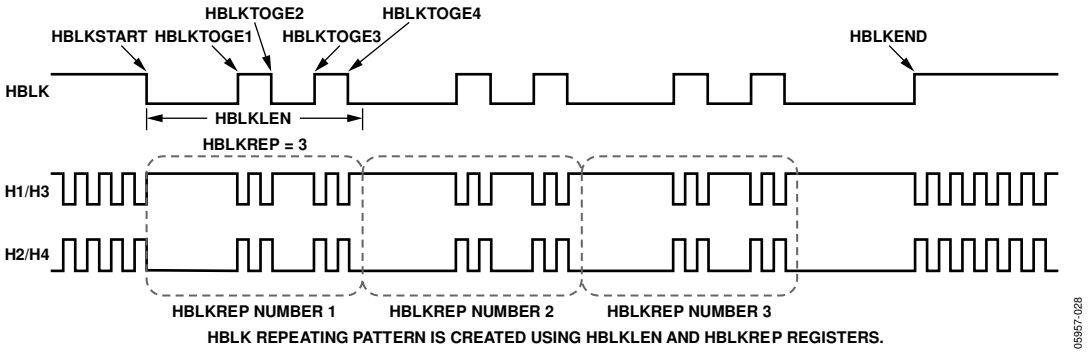

Figure 26. HBLK Repeating Pattern Using HBLK Mode 1 (Register Value = 1)

HBLK Mode 1 Operation

Multiple repeats of the HBLK signal can be enabled by setting HBLKMODE to 1. In this mode, the HBLK pattern is generated using a different set of registers: HBLKSTART, HBLKEND, HBLKLEN, and HBLKREP, along with the six toggle positions (see Figure 26).

Generating HBLK Line Alternation

HBLK Mode 0 and HBLK Mode 1 provide the ability to alternate HBLK toggle positions on even and odd lines for which separate toggle positions are available. If even/odd line alternation is not required, load the same values into the registers for the even lines (HBLKTOGEx) as the odd (HBLKTOGOx) lines.

Increasing Horizontal Clock Width During HBLK

HBLK Mode 0 and HBLK Mode 1 allow the H1 to H4 pulse width to increase during the HBLK interval. As shown in Figure 27, the horizontal clock frequency can reduce by a factor of 1/2, 1/4, 1/6, 1/8, 1/10, 1/12, and so on, up to 1/30 (see Table 12). To enable this feature, the HCLK_WIDTH register (Address 0x34, Bits[7:4]) is set to a value between 1 and 15. When this register is set to 0, the wide HCLK feature is disabled.

The reduced frequency occurs only for H1 to H4 pulses that are located within the HBLK area.

The HCLK_WIDTH feature is generally used in conjunction with special HBLK patterns to generate vertical and horizontal mixing in the CCD.

Note that the wide HCLK feature is available only in HBLK Mode 0 and HBLK Mode 1, and not in HBLK Mode 2.

Table 12. HCLK Width Register

Name	Length	Description
HCLK_WIDTH	4 bits	Controls H1 to H4 width during HBLK as a fraction of pixel rate. 0 = same frequency as pixel rate 1 = 1/2 pixel frequency, that is, doubles the HCLK pulse width 2 = 1/4 pixel frequency 3 = 1/6 pixel frequency 4 = 1/8 pixel frequency 5 = 1/10 pixel frequency 6 = 1/12 pixel frequency 7 = 1/14 pixel frequency 8 = 1/16 pixel frequency 9 = 1/18 pixel frequency 10 = 1/20 pixel frequency 11 = 1/22 pixel frequency 12 = 1/24 pixel frequency 13 = 1/26 pixel frequency 14 = 1/28 pixel frequency 15 = 1/30 pixel frequency

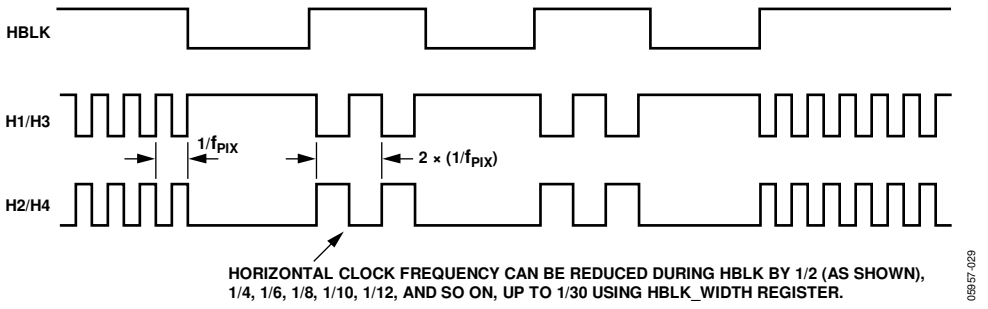

Figure 27. Generating Wide Horizontal Clock Pulses During HBLK Interval

HBLK Mode 2 Operation

HBLK Mode 2 allows more advanced HBLK pattern operation. If unevenly spaced, multiple areas of HCLK pulses are needed; therefore, use HBLK Mode 2. Using a separate set of registers, HBLK Mode 2 can divide the HBLK region into up to six different repeat areas (see Table 11). As shown in Figure 28, each repeat area shares a common group of toggle positions, HBLKSTARTA, HBLKSTARTB, and HBLKSTARTC. However, the number of toggles following each HBLKSTARTA, HBLKSTARTB, and HBLKSTARTC position can be unique in each repeat area by using RAxHyREPz, where x represents the repeat area, from 0 to 5, y represents the horizontal driver, 1 or 2, and z represents the HBLK repeat area start position for HBLK Mode 2, A, B, or C. As shown in Figure 29, setting the RAxH1REPA/RAxH1REPB/RAxH1REPC or RAxH2REPA/RAxH2REPB/RAxH2REPC registers to 0 masks the HCLK groups from appearing in a particular repeat area. Figure 28 shows only two repeat areas being used, although up to six are available. It is possible to program a separate number of repeat area repetitions for H1 and H2, but generally, the same value is used for both H1 and H2.

Figure 28 shows the example

RA0H1REPA/RA0H1REPB/RA0H1REPC =
RA0H2REPA/RA0H2REPB/RA0H2REPC =
RA1H1REPA/RA1H1REPB/RA1H1REPC =
RA1H2REPA/RA1H2REPB/RA1H2REPC = 2.

Furthermore, HBLK Mode 2 allows a different HBLK pattern on even and odd lines. HBLKSTARTA, HBLKSTARTB, and HBLKSTARTC, as well as RAxH1REPA/RAxH1REPB/RAxH1REPC and RAxH2REPA/RAxH2REPB/RAxH2REPC, define operation for the even lines. For separate control of the odd lines, the HBLKALT_PATx registers specify up to six repeat areas on the odd lines by reordering the repeat areas used for the even lines. New patterns are not available, but the order of the previously defined repeat areas on the even lines can be changed for the odd lines to accommodate advanced CCD operation.

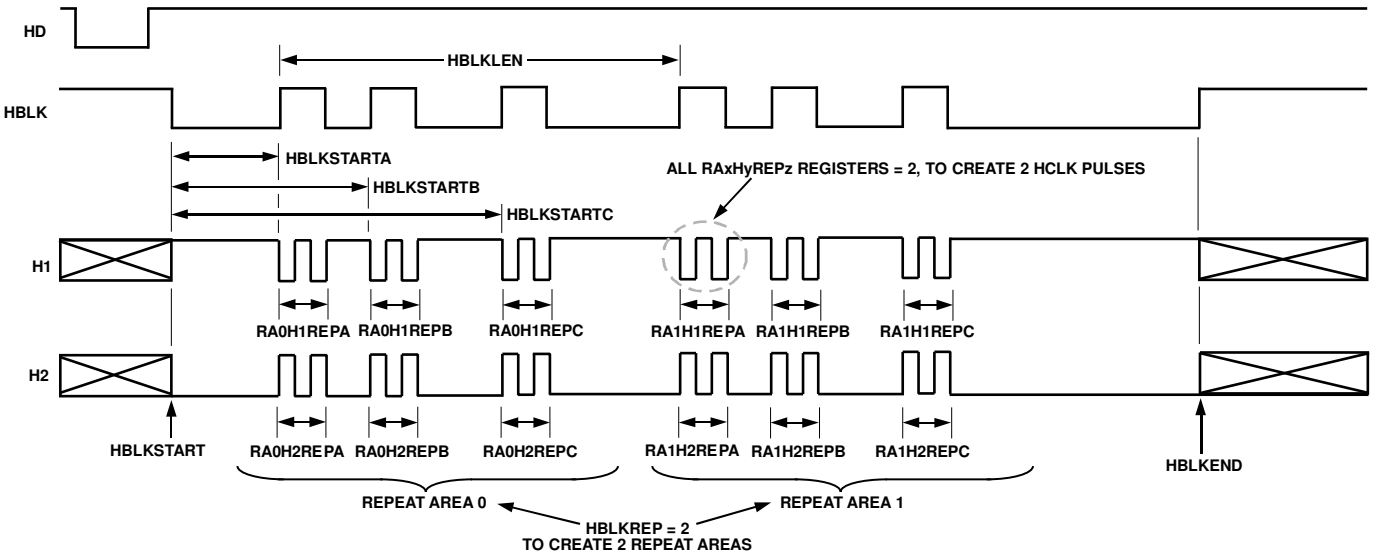

Figure 28. HBLK Mode 2 Registers

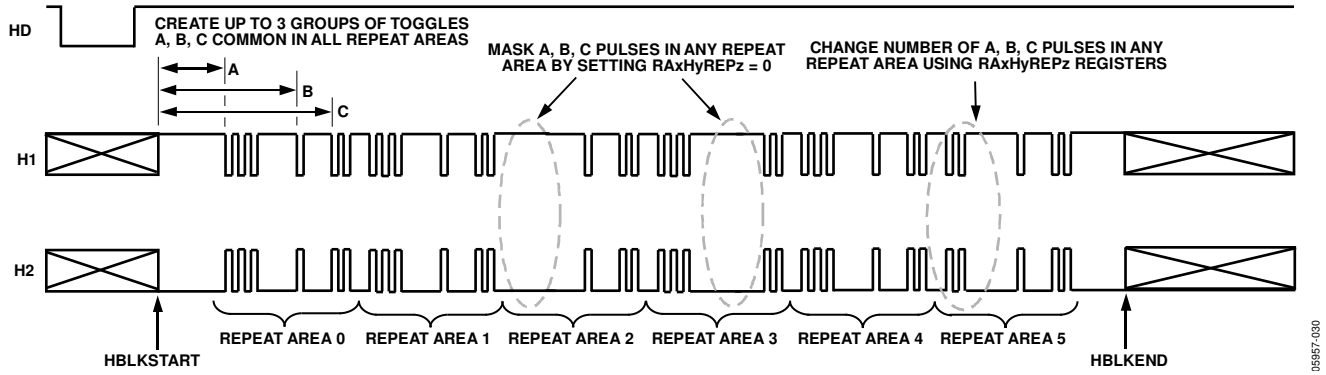

Figure 29. HBLK Mode 2 Operation

HBLK, PBLK, and CLPOB Toggle Positions

The AD9979 uses an internal horizontal pixel counter to position the HBLK, PBLK, and CLPOB toggle positions. The horizontal counter does not reset to 0 until 12 CLI periods after the falling edge of HD. This 12-cycle pipeline delay must be considered when determining the register toggle positions. For example, if CLPOBx_TOGy is 100 and the pipeline delay is not considered, the final toggle position is applied at 112. To obtain the correct toggle positions, the toggle position registers must be set to the desired toggle position minus 12. For example, if the desired toggle position is 100, CLPOBx_TOGy needs to be set to 88, that is, 100 minus 12. Figure 53 shows the 12-cycle pipeline delay referenced to the falling edge of HD.

Note that toggle positions cannot be programmed during the 12-cycle delay from the HD falling edge until the horizontal counter has reset. See Figure 31 for an example of this restriction.

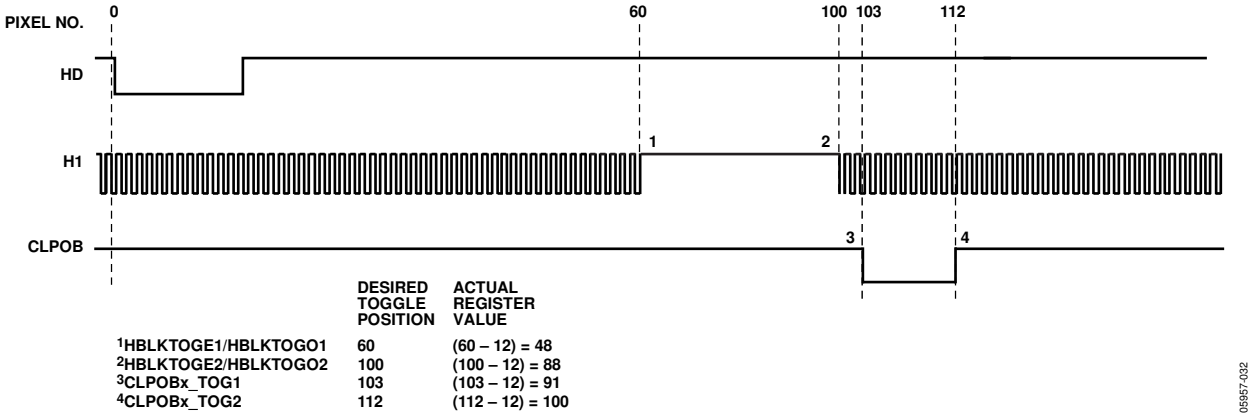

Figure 30. Example of Register Setting to Obtain Desired Toggle Positions

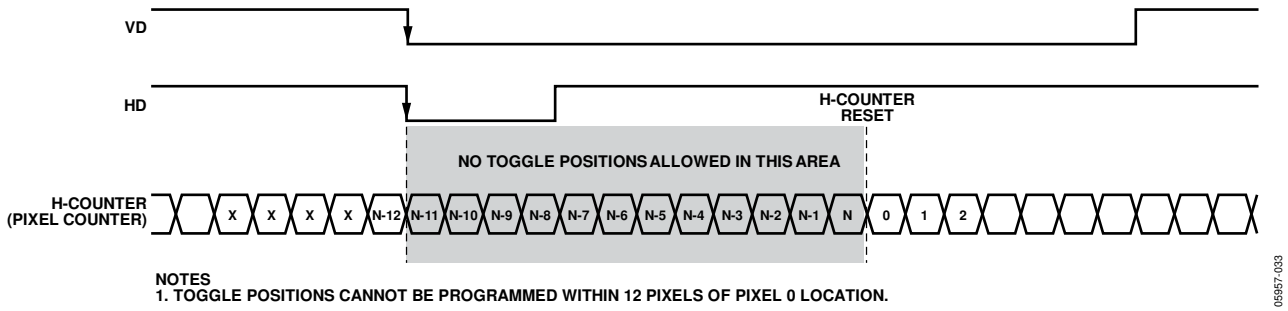

Figure 31. Restriction for Toggle Position Placement

COMPLETE FIELD—COMBINING H-PATTERNS

After creating the H-patterns, they combine to create different readout fields. A field consists of up to nine different regions determined by the SCP registers, and within each region, a different H-pattern group can be selected, up to a maximum of 32 groups. Registers to control the H-patterns are located in the field registers. Table 13 describes the field registers.

H-Pattern Selection

The H-patterns are stored in the HPAT memory, as described in Table 33. The user decides how many H-pattern groups are required, up to a maximum of 32, and then uses the HPAT_SELx registers to select which H-pattern group is output in each region of the field. Figure 32 shows how to use the HPAT_SELx and SCPx registers. The SCPx registers create the line boundaries for each region.

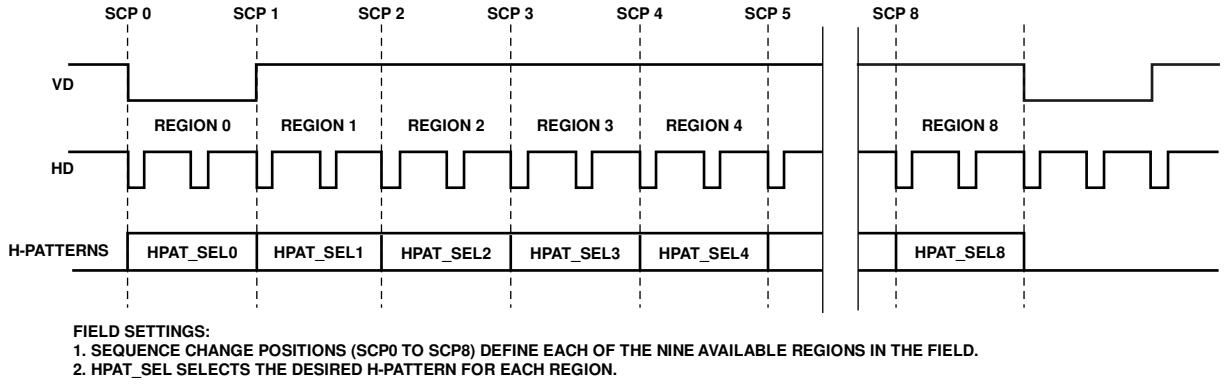

Figure 32. Complete Field Divided into Regions

Table 13. Field Registers

Name	Length	Range	Description
SCPx	13 bits	0 to 8191 line number	Sequence change position for each region; selects an individual line
HPAT_SELx	5 bits	0 to 31 H-patterns	Selected H-pattern for each region of the field
CLPOB_POL	9 bits	High/low	CLPOB start polarity settings for each region of the field
CLPOB_PAT	9 bits	0 to 9 patterns	CLPOB pattern selector for each region of the field
CLPOBMASKSTARTx, CLPOBMASKENDx	13 bits	Number of lines	CLPOB mask positions for up to three masking configurations
PBLK_POL	9 bits	High/low	PBLK start polarity settings for each region of the field
PBLK_PAT	9 bits	0 to 9 patterns	PBLK pattern selector for each region of the field
PBLKMASKSTARTx, PBLKMASKENDx,	13 bits	Number of lines	PBLK mask positions for up to three masking configurations

MODE REGISTERS

To select the final field timing of the AD9979, use the mode registers. Typically, all of the field and H-pattern group information is programmed into the AD9979 at startup. During operation, the mode registers allows the user to select any combination of field timing to meet the current requirements of the system. The advantage of using the mode registers in conjunction with preprogrammed timing is that it greatly reduces the system programming requirements during camera operation. Only a few register writes are required when the camera operating mode is changed, rather than having to write in all of the vertical timing information with each camera mode change.

A basic still camera application can require five different fields of horizontal timing: one for draft mode operation, one for auto focusing, and three for still-image readout. With the AD9979, all register timing information for the five fields is loaded at startup. Then, during camera operation, the mode registers selects which field timing to activate depending on how the camera is being used.

The AD9979 supports up to seven field sequences, selected from up to 31 preprogrammed field groups, using the FIELD_SELx registers. When FIELDNUM is greater than 1, the AD9979 starts with Field 1 and increments to each Field N at the start of each VD.

Figure 33 provides examples of the mode configuration settings. This example assumes having four field groups, Field Group 0 to Field Group 3, stored in memory.

Table 14. Mode Registers

Name	Length	Range	Description
HPATNUM	5 bits	0 to 31 H-pattern groups	Total number of H-pattern groups starting at Address 0x800
FIELDNUM	3 bits	0 to 7 fields	Total number of applied fields (1 = single-field operation)
FIELD_SEL1	5 bits	0 to 31 field groups	Selected first field
FIELD_SEL2	5 bits	0 to 31 field groups	Selected second field
FIELD_SEL3	5 bits	0 to 31 field groups	Selected third field
FIELD_SEL4	5 bits	0 to 31 field groups	Selected fourth field
FIELD_SEL5	5 bits	0 to 31 field groups	Selected fifth field
FIELD_SEL6	5 bits	0 to 31 field groups	Selected sixth field
FIELD_SEL7	5 bits	0 to 31 field groups	Selected seventh field