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FEATURES

- 8-bit analog-to-digital converters
- 140 MSPS maximum conversion rate
- Low PLL clock jitter at 140 MSPS
- Automatic gain matching
- Automated offset adjustment
- 2:1 input mux
- Power-down via dedicated pin or serial register
- 4:4:4, 4:2:2, and DDR output format modes
- Variable output drive strength
- Odd/even field detection
- External clock input
- Regenerated Hsync output
- Programmable output high impedance control
- Hsyncs per Vsync counter
- Pb-free package

APPLICATIONS

- Advanced TVs
- Plasma display panels
- LCDTV
- HDTV
- RGB graphics processing
- LCD monitors and projectors
- Scan converters

GENERAL DESCRIPTION

The AD9983A is a complete 8-bit, 140 MSPS, monolithic analog interface optimized for capturing YPbPr video and RGB graphics signals. Its 140 MSPS encode rate capability and full power analog bandwidth of 300 MHz support all HDTV video modes up to 1080i and 720p as well as graphics resolutions up to SXGA (1280 x 1024 at 75 Hz).

The AD9983A includes a 140 MHz triple ADC with an internal reference, a PLL, and programmable gain, offset, and clamp control. The user provides only a 1.8 V power supply and an analog input. Three-state CMOS outputs can be powered from 1.8 V to 3.3 V.

The AD9983A on-chip PLL generates a sample clock from the tri-level sync (for YPbPr video) or the horizontal sync (for RGB graphics). Sample clock output frequencies range from 10 MHz to 140 MHz. With internal coast generation, the PLL maintains its output frequency in the absence of sync input. A 32-step

FUNCTIONAL BLOCK DIAGRAM

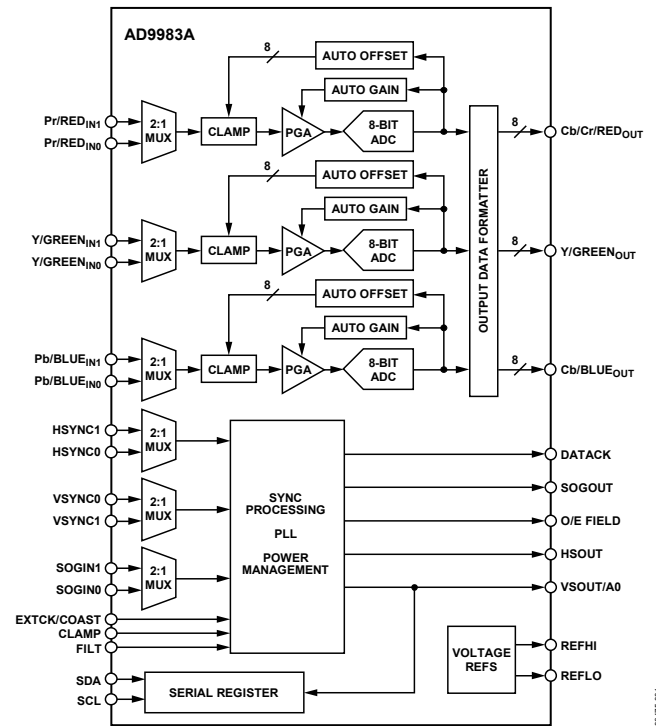


Figure 1.

sampling clock phase adjustment is provided. Output data, sync, and clock phase relationships are maintained.

The auto-offset feature can be enabled to automatically restore the signal reference levels and to automatically calibrate out any offset differences between the three channels. The auto channel-to-channel gain matching feature can be enabled to minimize any gain mismatches between the three channels.

The AD9983A also offers full sync processing for composite sync and sync-on-green applications. A clamp signal is generated internally or may be provided by the user through the CLAMP input pin.

Fabricated in an advanced CMOS process, the AD9983A is provided in a space-saving 80-lead, Pb-free, LQFP surface-mount plastic package, and is specified over the 0°C to 70°C temperature range.

Rev. 0

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- AD9983A Evaluation Board

DOCUMENTATION

Data Sheet

- AD9983A: High Performance 8-Bit Display Interface Data Sheet

REFERENCE MATERIALS

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- Advantiv™ Advanced TV Solutions

Technical Articles

- Analysis of Common Failures of HDMI CT

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- AD9983A Material Declaration
- PCN-PDN Information
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REVISION HISTORY

5/07—Revision 0: Initial Version

SPECIFICATIONS

ANALOG INTERFACE CHARACTERISTICS

$V_D = 1.8\text{ V}$, $V_{DD} = 3.3\text{ V}$, $PV_D = 1.8\text{ V}$, $DAV_{DD} = 1.8\text{ V}$, ADC clock = maximum conversion rate, full temperature range = 0°C to 70°C .

Table 1.

Parameter	Temperature	Test Level ¹	Min	Typ	Max	Unit
RESOLUTION						
Number of bits				8		Bits
LSB Size				0.391		% of Full Scale
DC ACCURACY						
Differential Nonlinearity	25°C	I		±0.25	±0.85	LSB
	Full	VI		±0.3		LSB
Integral Nonlinearity	25°C	I		±0.75	1.45/–2.60	LSB
	Full	VI		±1.0		LSB
No Missing Codes	Full	VI		GNT		
ANALOG INPUT						
Input Voltage Range						
Minimum	Full	VI			0.5	V p-p
Maximum	Full	VI	1.0			V p-p
Gain Tempco	25°C	V		125		ppm/°C
Input Bias Current	25°C	IV			1	µA
	Full	IV			1	µA
Input Full-Scale Matching	Full	VI		1	5	% FS
Offset Adjustment Range	Full	VI		50		% FS
SWITCHING PERFORMANCE						
Maximum Conversion Rate	Full	VI	140			MSPS
Minimum Conversion Rate	Full	IV			10	MSPS
Clock to Data Skew t_{SKEW}	Full	IV	–0.5		2.0	ns
t_{BUFF}	Full	VI	4.7			µs
t_{STAH}	Full	VI	4.0			µs
t_{DHO}	Full	VI	0			µs
t_{DAL}	Full	VI	4.7			µs
t_{DAH}	Full	VI	4.0			µs
t_{DSU}	Full	VI	250			ns
t_{STASU}	Full	VI	4.7			µs
t_{STOSU}	Full	VI	4.0			µs
Maximum PLL Clock Rate	Full	VI	140			MHz
Minimum PLL Clock Rate	Full	IV			10	MHz
Jitter ²	25°C	IV				pS p-p
	Full	IV				pS p-p
Sampling Phase Tempco	Full	IV		15		pS/°C
DIGITAL INPUTS						
Input Voltage, High (V_{IH})	Full	VI	1.0			V
Input Voltage, Low (V_{IL})	Full	VI			0.8	V
Input Current, High (I_{IH})	Full	V			–1.0	µA
Input Current, Low (I_{IL})	Full	V			1.0	µA
Input Capacitance	25°C	V		2		pF
DIGITAL OUTPUTS						
Output Voltage, High (V_{OH})	Full	VI	$V_{DD} - 0.1$			V
Output Voltage, Low (V_{OL})	Full	VI			0.1	V
Duty Cycle, DATAACK	Full	IV	45	50	55	%
Output Coding				Binary		

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Parameter	Temperature	Test Level ¹	Min	Typ	Max	Unit
POWER SUPPLY						
V _D Supply Voltage	Full	IV	1.7	1.8	1.9	V
V _{DD} Supply Voltage	Full	IV	1.7	3.3	3.47	V
PV _D Supply Voltage	Full	IV	1.7	1.8	1.9	V
DAV _{DD} Supply Voltage	Full	IV	1.7	1.8	1.9	V
V _D Supply Current (I _D)	25°C	V		250		mA
V _{DD} Supply Current (I _{DD})	25°C	V		31		mA
PV _D Supply Current (IPV _D)	25°C	V		9		mA
DAV _{DD} Supply Current (IDAV _{DD})	25°C	V		16		mA
Total Power Dissipation	Full	VI			800	mW
Power-Down Supply Current	Full	VI		10		mA
Power-Down Dissipation	Full	VI		18		mW
DYNAMIC PERFORMANCE						
Analog Bandwidth, Full Power	25°C	V		300		MHz
Crosstalk	Full	V		60		dBc

¹ See the Explanation of Test Levels section.

² Jitter measurements taken at SXGA with recommended PLL settings.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_D	1.98 V
V_{DD}	3.6 V
PV_D	1.98 V
DAV_{DD}	1.98 V
Analog Inputs	V_D to 0.0 V
REFHI	V_D to 0.0 V
REFLO	V_D to 0.0 V
Digital Inputs	5 V to 0.0 V
Digital Output Current	20 mA
Operating Temperature	-25°C to +85°C
Storage Temperature	-65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

- I. 100% production tested.
- II. 100% production tested at 25°C and sample tested at specified temperatures.
- III. Sample tested only.
- IV. Parameter is guaranteed by design and characterization testing.
- V. Parameter is a typical value only.
- VI. 100% production tested at 25°C; guaranteed by design and characterization testing.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
80-lead LQFP	35	16	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

AD9983A

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

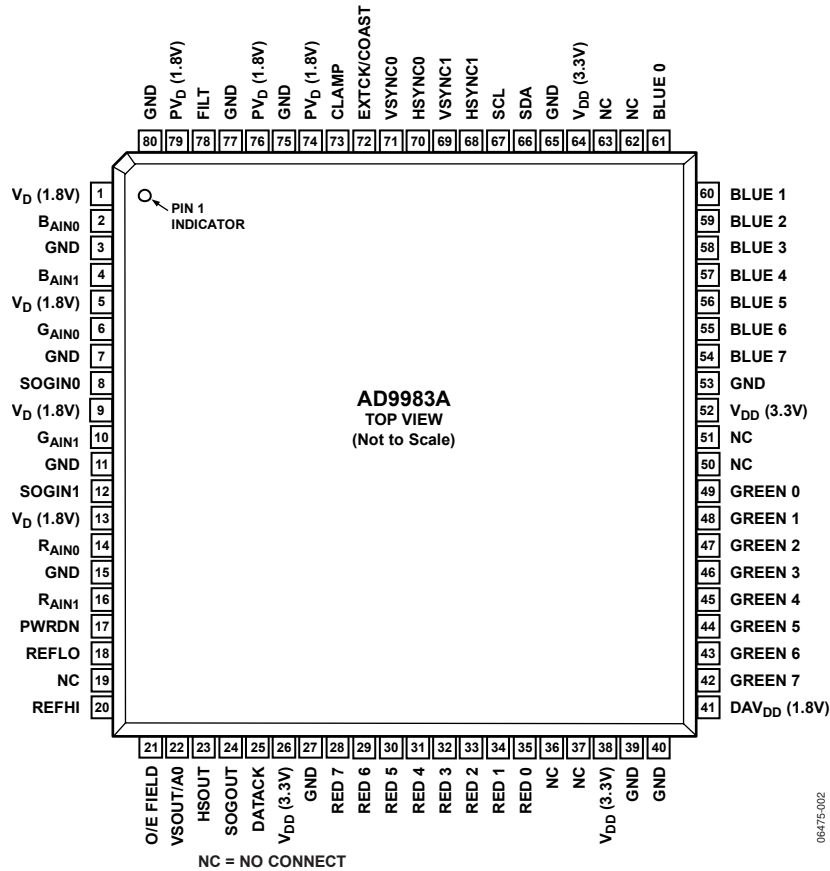


Figure 2. 80-Lead LQFP Pin Configuration

Table 4. Complete Pinout List

Pin Type	Pin Number	Mnemonic	Function	Value
Inputs	14	R _{AIN0}	Channel 0 Analog Input for Converter R	0.0V to 1.0V
	16	R _{AIN1}	Channel 1 Analog Input for Converter R	0.0V to 1.0V
	6	G _{AIN0}	Channel 0 Analog Input for Converter G	0.0V to 1.0V
	10	G _{AIN1}	Channel 1 Analog Input for Converter G	0.0V to 1.0V
	2	B _{AIN0}	Channel 0 Analog Input for Converter B	0.0V to 1.0V
	4	B _{AIN1}	Channel 1 Analog Input for Converter B	0.0V to 1.0V
	70	HSYNC0	Horizontal Sync Input for Channel 0	3.3V CMOS
	68	HSYNC1	Horizontal Sync Input for Channel 1	3.3V CMOS
	71	VSYNC0	Vertical Sync Input for Channel 0	3.3V CMOS
	69	VSYNC1	Vertical Sync Input for Channel 1	3.3V CMOS
	8	SOGIN0	Input for Sync-on-Green Channel 0	0.0V to 1.0V
	12	SOGIN1	Input for Sync-on-Green Channel 1	0.0V to 1.0V
	72 ¹	EXTCK	External Clock Input	3.3V CMOS
	73	CLAMP	External Clamp Input Signal	3.3V CMOS
	72 ¹	COAST	External PLL Coast Signal Input	3.3V CMOS
17	PWRDN	Power-Down Control	3.3V CMOS	

Pin Type	Pin Number	Mnemonic	Function	Value
Outputs	28 to 35	RED [7:0]	Outputs of Converter R, Bit 9 is the MSB	3.3 V CMOS
	42 to 49	GREEN [7:0]	Outputs of Converter G, Bit 9 is the MSB	3.3 V CMOS
	54 to 61	BLUE [7:0]	Outputs of Converter B, Bit 9 is the MSB	3.3 V CMOS
	25	DATAACK	Data Output Clock	3.3 V CMOS
	23	HSOUT	Hsync Output Clock (Phase-Aligned with DATAACK)	3.3 V CMOS
	22 ²	VSOUT	Vsync Output Clock	3.3 V CMOS
	24	SOGOUT	Sync-on-Green Slicer Output	3.3 V CMOS
	21	O/E FIELD	Odd/Even Field Output	3.3 V CMOS
References	78	FILT	Connection for External Filter Components for Internal PLL	
	18	REFLO	Connection for External Capacitor for Input Amplifier	
	20	REFHI	Connection for External Capacitor for Input Amplifier	
Power Supply	1, 5, 9, 13	V _D	Analog Power Supply	1.8 V
	26, 38, 52, 64	V _{DD}	Output Power Supply	1.8 V or 3.3 V
	74, 76, 79	PV _D	PLL Power Supply	1.8 V
	41	DAV _{DD}	Digital Logic Power Supply	1.8 V
	3, 7, 11, 15, 39, 40, 53, 65, 75, 77, 80	GND	Ground	0 V
Control	66	SDA	Serial Port Data I/O	3.3 V CMOS
	67	SCL	Serial Port Data Clock (100 kHz maximum)	3.3 V CMOS
	22 ²	A0	Serial Port Address Input	3.3 V CMOS

¹ EXTCK and COAST share the same pin.

² VSOUT and A0 share the same pin.

Table 5. Pin Function Descriptions

Mnemonic	Function	Description
R _{AIN0} G _{AIN0} B _{AIN0} R _{AIN1} G _{AIN1} B _{AIN1}	Analog Input for the Red Channel 0 Analog Input for the Green Channel 0 Analog Input for the Blue Channel 0 Analog Input for the Red Channel 1 Analog Input for the Green Channel 1 Analog Input for the Blue Channel 1	These are high impedance inputs that accept the red, green, and blue channel graphics signals, respectively. The three channels are identical and can be used for any colors, but colors are assigned for convenient reference. They accommodate input signals ranging from 0.5 V to 1.0 V full scale. Signals should be ac-coupled to these pins to support clamp operation. See Figure 4 and Figure 5.
HSYNC0 HSYNC1	Horizontal Sync Input Channel 0 Horizontal Sync Input Channel 1	These inputs receive a logic signal that establishes the horizontal timing reference and provides the frequency reference for pixel clock generation. The logic sense of this pin can be automatically determined by the chip or manually controlled by Serial Register 0x12, Bits[5:4] (Hsync polarity). Only the leading edge of Hsync is used by the PLL; the trailing edge is used in clamp timing. When Hsync polarity = 0, the falling edge of Hsync is used. When Hsync polarity = 1, the rising edge is active. The input includes a Schmitt trigger for noise immunity.
VSYNC0 VSYNC1	Vertical Sync Input Channel 0 Vertical Sync Input Channel 1	These are the inputs for vertical sync and provide timing information for generation of the field (odd/even) and internal Coast generation. The logic sense of this pin can be automatically determined by the chip or manually controlled by Serial Register 0x14, Bits[5:4] (Vsync polarity).
SOGIN0 SOGIN1	Sync-on-Green Input Channel 0 Sync-on-Green Input Channel 1	These inputs process signals with embedded sync, typically on the green channel. The pin is connected to a high speed comparator with an internally generated threshold. The threshold level can be programmed in 8 mV steps to any voltage between 8 mV and 256 mV above the negative peak of the input signal. The default voltage threshold is 128 mV. When connected to an ac-coupled graphics signal with embedded sync, it produces a noninverting digital output on SOGOUT. This is usually a composite sync signal, containing both vertical and horizontal sync information that must be separated before passing the horizontal sync signal for Hsync processing. When not used, this input should be left unconnected. For more details on this function and how it should be configured, refer to the Sync-on-Green section.
CLAMP	External Clamp Input (Optional)	This logic input can be used to define the time during which the input signal is clamped to ground or midscale. It should be exercised when the reference dc level is known to be present on the analog input channels, typically during the back porch of the graphics signal. The CLAMP pin is enabled by setting the control bit clamp function to 1, (Register 0x18, Bit 4; default is 0). When disabled, this pin is ignored and the clamp timing is determined internally by counting a delay and duration from the trailing edge of the Hsync input. The logic sense of this pin can be automatically determined by the chip or controlled by clamp polarity Register 0x1B, Bits[7:6]. When not used, this pin may be left unconnected (there is an internal pull-down resistor) and the clamp function programmed to 0.
EXTCK/COAST	External Clock Coast Input to Clock Generator (Optional)	EXTCK allows the insertion of an external clock source rather than the internally generated, PLL locked clock. EXTCK is enabled by programming Register 0x03, Bit 2 to 1. This pin is shared with the Coast function, which does not affect EXTCK functionality. COAST can be used to cause the pixel clock generator to stop synchronizing with Hsync and continue producing a clock at its current frequency and phase. This is useful when processing signals from sources that fail to produce Hsync pulses during the vertical interval. The coast signal is generally <i>not</i> required for PC-generated signals. The logic sense of this pin can be determined automatically or controlled by Coast polarity (Register 0x18, Bits[7:6]). When not used and EXTCK not used, this pin may be grounded and Coast polarity programmed to 1. Input Coast polarity defaults to 1 at power-up. This pin is shared with the EXTCK function, which does not affect coast functionality. For more details on EXTCK, see the description in this section.
PWRDN	Power-Down Control	This pin can be used along with Register 0x1E, Bit 3 for manual power-down control. If manual power-down control is selected (Register 0x1E, Bit 4) and this pin is not used, it is recommended to set the pin polarity (Register 0x1E, Bit 2) to active high and hardwire this pin to ground with a 10 kΩ resistor.

Mnemonic	Function	Description
REFLO, REFHI	Input Amplifier Reference	REFLO and REFHI are connected together through a 10 μ F capacitor. These are used for stability in the input ADC circuitry. See Figure 6.
FILT	External Filter Connection	For proper operation, the pixel clock generator PLL requires an external filter. Connect the filter shown in Figure 6 to this pin. For optimal performance, minimize noise and parasitics on this node. For more information, see the PCB Layout Recommendations section.
HSOUT	Horizontal Sync Output	A reconstructed and phase-aligned version of the Hsync input. Both the polarity and duration of this output can be programmed via serial bus registers. By maintaining alignment with DATAACK and Data, data timing with respect to Hsync can always be determined.
VSOUT/A0	Vertical Sync Output Serial Port Address Input 0	Pin shared with A0, serial port address. This can be either a separated Vsync from a composite signal or a direct pass through of the Vsync signal. The polarity of this output can be controlled via a serial bus bit. The placement and duration in all modes can be set by the graphics transmitter or the duration can be set by Register 0x14 and Register 0x15. This pin is shared with the A0 function, which does not affect Vsync Output functionality. For more details on A0, see the description in the Serial Control Port section. Pin shared with VSOUT. This pin selects the LSB of the serial port device address, allowing two Analog Devices parts to be on the same serial bus. A high impedance external pull-up resistor enables this pin to be read at power-up as 1, or a high impedance, external pull-down resistor enables this pin to be read at power-up as a 0 and not interfere with the VSOUT functionality.
SOGOUT	Sync-On-Green Slicer Output	This pin outputs one of four possible signals (controlled by Register 0x1D, Bits[1:0]): raw SOG, raw Hsync, regenerated Hsync from the filter, or the filtered Hsync. See Figure 8 to view how this pin is connected. Other than slicing off SOG, the output from this pin gets no additional processing on the AD9983A. Vsync separation is performed via the sync separator.
O/E FIELD	Odd/Even Field Bit for Interlaced Video	This output will identify whether the current field (in an interlaced signal) is odd or even.
SDA	Serial Port Data I/O	Data I/O for the I ² C [®] serial port.
SCL	Serial Port Data Clock	Clock for the I ² C serial port.
RED [7:0] GREEN [7:0] BLUE [7:0]	Data Output, Red Channel Data Output, Green Channel Data Output, Blue Channel	The main data outputs. Bit 9 is the MSB. The delay from pixel sampling time to output is fixed. When the sampling time is changed by adjusting the phase register, the output timing is shifted as well. The DATAACK and HSOUT outputs are also moved, so the timing relationship among the signals is maintained.
DATAACK	Data Clock Output	This is the main clock output signal used to strobe the output data and HSOUT into external logic. Four possible output clocks can be selected with Register 0x20, Bits[7:6]. Three of these are related to the pixel clock (pixel clock, 90° phase-shifted pixel clock and 2x frequency pixel clock). They are produced either by the internal PLL clock generator or EXTCK and are synchronous with the pixel sampling clock. The fourth option for the data clock output is an internally generated 1/2x pixel clock. The sampling time of the internal pixel clock can be changed by adjusting the phase register (Register 0x04). When this is changed, the pixel related DATAACK timing is also shifted. The data, DATAACK, and HSOUT outputs are all moved so that the timing relationship among the signals is maintained.
V _D (1.8 V) V _{DD} (1.8 V to 3.3 V)	Main Power Supply Digital Output Power Supply	These pins supply power to the main elements of the circuit. They should be as quiet and filtered as possible. A large number of output pins (up to 29) switching at high speed (up to 140 MHz) generates a lot of power supply transients (noise). These supply pins are identified separately from the V _D pins, so special care can be taken to minimize output noise transferred into the sensitive analog circuitry. If the AD9983A is interfacing with lower voltage logic, V _{DD} can be connected to a lower supply voltage (as low as 1.8 V) for compatibility.
PV _D (1.8 V)	Clock Generator Power Supply	The most sensitive portion of the AD9983A is the clock generation circuitry. These pins provide power to the clock PLL and help the user design for optimal performance. The designer should provide quiet, noise-free power to these pins.
DAV _{DD} (1.8 V)	Digital Input Power Supply	This supplies power to the digital logic.
GND	Ground	The ground return for all circuitry on-chip. It is recommended that the AD9983A be assembled on a single solid ground plane, with careful attention to ground current paths.

THEORY OF OPERATION

The AD9983A is a fully integrated solution for capturing analog RGB or YPbPr signals and digitizing them for display on advanced TVs, flat panel monitors, projectors, and other types of digital displays. Implemented in a high performance CMOS process, the interface can capture signals with pixel rates of up to 140 MHz.

The AD9983A includes all necessary input buffering, signal dc restoration (clamping), offset and gain (brightness and contrast) adjustment, pixel clock generation, sampling phase control, and output data formatting. All controls are programmable via a 2-wire serial interface (I²C). Full integration of these sensitive analog functions makes system design straightforward and less sensitive to the physical and electrical environment.

With a typical power dissipation of less than 800 mW and an operating temperature range of 0°C to 70°C, the device requires no special environmental considerations.

DIGITAL INPUTS

All digital inputs on the AD9983A operate to 3.3 V CMOS levels. The following digital inputs are 5 V tolerant (that is, applying 5 V to them does not cause any damage.): HSYNC0, HSYNC1, VSYNC0, VSYNC1, SOGIN0, SOGIN1, SDA, SCL and CLAMP.

ANALOG INPUT SIGNAL HANDLING

The AD9983A has six high impedance analog input pins for the red, green, and blue channels. They accommodate signals ranging from 0.5 V to 1.0 V p-p.

Signals are typically brought onto the interface board with a DVI-I connector, a 15-pin D connector, or RCA connectors. The AD9983A should be located as close as possible to the input connector. Signals should be routed using matched-impedance traces (normally 75 Ω) to the IC input pins.

At the input pins the signal should be resistively terminated (75 Ω to the signal ground return) and capacitively coupled to the AD9983A inputs through 47 nF capacitors. These capacitors form part of the dc restoration circuit.

In an ideal world of perfectly matched impedances, the best performance can be obtained with the widest possible signal bandwidth. The wide bandwidth inputs of the AD9983A (300 MHz) can track the input signal continuously as it moves from one pixel level to the next and can digitize the pixel during a long, flat pixel time. In many systems, however, there are mismatches, reflections, and noise, which can result in excessive ringing and distortion of the input waveform. This makes it more difficult to establish a sampling phase that provides good image quality. A small inductor in series with the input is effective in rolling off the input bandwidth slightly and providing a high quality signal over a wider range of conditions. Using a Fair-Rite #2508051217Z0-High Speed, Signal Chip Bead Inductor in the circuit shown in Figure 3 provides good results in most applications.

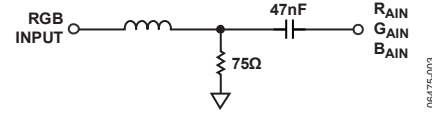


Figure 3. Analog Input Interface Circuit

HSYNC AND VSYNC INPUTS

The interface also accepts Hsync and Vsync signals, which are used to generate the pixel clock, clamp timing, coast and field information. These can be either a sync signal directly from the graphics source, or a preprocessed TTL- or CMOS-level signal.

The Hsync input includes a Schmitt trigger buffer for immunity to noise and signals with long rise times. In typical PC-based graphic systems, the sync signals are simply TTL-level drivers feeding unshielded wires in the monitor cable. As such, no termination is required.

SERIAL CONTROL PORT

The serial control port is designed for 3.3 V logic; however, it is tolerant of 5 V logic signals. Refer to the 2-Wire Serial Control Port section.

OUTPUT SIGNAL HANDLING

The digital outputs operate from 1.8 V to 3.3 V (V_{DD}).

CLAMPING

RGB Clamping

To properly digitize the incoming signal, the dc offset of the input must be adjusted to fit the range of the on-board ADCs.

Most graphics systems produce RGB signals with black at ground and white at approximately 0.75 V. However, if sync signals are embedded in the graphics, the sync tip is often at ground, black is at 300 mV, and white is at approximately 1.0 V. Some common RGB line amplifier boxes use emitter-follower buffers to split signals and increase drive capability. This introduces a 700 mV dc offset to the signal, which must be removed for proper capture by the AD9983A.

The key to clamping is to identify a portion (time) of the signal when the graphic system is known to be producing black. An offset is then introduced that results in the ADC producing a black output (Code 0x00) when the known black input is present. The offset then remains in place when other signal levels are processed, and the entire signal is shifted to eliminate offset errors.

In most PC graphics systems, black is transmitted between active video lines. With CRT displays, when the electron beam has completed writing a horizontal line on the screen (at the right side), the beam is deflected quickly to the left side of the screen (called horizontal retrace) and a black signal is provided to prevent the beam from disturbing the image.

In systems with embedded sync, a blacker-than-black signal (Hsync) is produced briefly to signal the CRT that it is time to begin a retrace. Because the input is not at black level at this time, it is important to avoid clamping during Hsync. Fortunately, there is usually a period following Hsync, called the back porch, where a good black reference is provided. This is the time when clamping should be done.

The clamp timing can be established by simply exercising the CLAMP pin at the appropriate time with clamp source (Register 0x18, Bit 4) = 1. The polarity of this signal is set by the clamp polarity bit, (Register 0x1B, Bits[7:6]).

A simpler method of clamp timing employs the AD9983A internal clamp timing generator. The clamp placement register (Register 0x19) is programmed with the number of pixel periods that should pass after the trailing edge of Hsync before clamping starts. A second register, clamp duration, (Register 0x1A) sets the duration of the clamp. These are both 8-bit values, providing considerable flexibility in clamp generation. The clamp timing is referenced to the trailing edge of Hsync because, though Hsync duration can vary widely, the back porch (black reference) always follows Hsync. A good starting point for establishing clamping is to set the clamp placement to 0x04 (providing 4 pixel periods for the graphics signal to stabilize after sync) and set the clamp duration to 0x28 (giving the clamp 40 pixel periods to reestablish the black reference).

Clamping is accomplished by placing an appropriate charge on the external input coupling capacitor. The value of this capacitor affects the performance of the clamp. If it is too small, there will be a significant amplitude change during a horizontal line time (between clamping intervals). If the capacitor is too large, it will take too long for the clamp to recover from a large change in incoming signal offset. The recommended value (47 nF) results in recovering from a step error of 100 mV to within 1 LSB in 30 lines with a clamp duration of 20 pixel periods on a 85 Hz XGA signal.

YPbPr Clamping

YPbPr graphic signals are slightly different from RGB signals in that the dc reference level (black level in RGB signals) of color difference signals is at the midpoint of the video signal rather than at the bottom. The three inputs are composed of luminance (Y) and color difference (Pb and Pr) signals. For color difference signals, it is necessary to clamp to the midscale range of the ADC range (512) rather than to the bottom of the ADC range (0), while the Y channel is clamped to ground.

Clamping to midscale rather than ground can be accomplished by setting the clamp select bits in the serial bus register. Each of the three converters has its own selection bit so that they can be clamped to either midscale or ground independently. These bits are located in Register 0x18, Bits[3:1]. The midscale reference voltage is internally generated for each converter.

GAIN AND OFFSET CONTROL

The AD9983A contains three PGAs, one for each of the three analog inputs. The range of the PGA is sufficient to accommodate input signals with inputs ranging from 0.5 V to 1.0 V full scale. The gain is set in three 7-bit registers (red gain [0x05], green gain [0x07], blue gain [0x09]). For each register, a gain setting of 0 corresponds to the highest gain, while a gain setting of 127 corresponds to the lowest gain. Note that increasing the gain setting results in an image with less contrast.

The offset control shifts the analog input, resulting in a change in brightness. Three 9-bit registers red offset [Register 0x0B and Register 0x0C], green offset [Register 0x0D and Register 0x0E], and blue offset [Register 0x0F and Register 0x10] provide independent settings for each channel. Note that the function of the offset register depends on whether auto-offset is enabled (Register 0x1B, Bit 5).

If manual offset is used, seven bits of the offset registers (for the red channel Register 0x0B, Bits[6:0]) control the absolute offset added to the channel. The offset control provides ± 63 LSBs of adjustment range, with 1 LSB of offset corresponding to 1 LSB of output code.

Automatic Offset

In addition to the manual offset adjustment mode, the AD9983A also includes circuitry to automatically calibrate the offset for each channel. By monitoring the output of each ADC during the back porch of the input signals, the AD9983A can self-adjust to eliminate any offset errors in its own ADC channels and any offset errors present on the incoming graphics or video signals.

To activate the auto-offset mode, set Register 0x1B, Bit 5 to 1. Next, the target code registers (Register 0x0B through Register 0x10) must be programmed. The values programmed into the target code registers should be the output code desired from the AD9983A ADCs, which are generated during the back porch reference time. For example, for RGB signals, all three registers are normally programmed to Code 2, while for YPbPr signals the green (Y) channel is normally programmed to Code 2 and the blue and red channels (Pb and Pr) are normally set to 128. The target code registers have nine bits per channel and are in twos complement format. This allows any value between -256 and $+255$ to be programmed. Although any value in this range can be programmed, the AD9983A offset range may not be able to reach every value. Intended target code values range from (but are not limited to) -40 to -1 and 1 to 40 when ground clamping and 88 to 168 when midscale clamping. Note that a target code of 0 is not valid.

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Negative target codes are included in order to duplicate a feature that is present with manual offset adjustment. The benefit that is being mimicked is the ability to easily adjust brightness on a display. By setting the target code to a value that does not correspond to the ideal ADC range, the end result is an image that is either brighter or darker. A target code higher than ideal results in a brighter image. A target code lower than ideal results in a darker image.

The ability to program a target code gives a large degree of freedom and flexibility. In most cases all channels are set to either 1 or 128, but the flexibility to select other values allows for the possibility of inserting intentional skews between channels. It also allows the ADC range to be skewed so that voltages outside of the normal range can be digitized. For example, setting the target code to 40 allows the sync tip, which is normally below black level, to be digitized and evaluated.

The internal logic for the auto-offset circuit requires 16 data clock cycles to perform its function. This operation is executed immediately after the clamping pulse. Therefore, it is important to end the clamping pulse signal at least 16 data clock cycles before active video. This is true whether using the AD9983A internal clamp circuit or an external clamp signal. The auto-offset function can be programmed to run continuously or on a one-time basis (see auto-offset hold, Register 0x2C, Bit 4). In continuous mode, the update frequency can be programmed (Register 0x1B, Bits[4:3]). Continuous operation with updates every 64 Hsyncs is recommended.

A guideline for basic auto-offset operation is shown in Table 6 and Table 7.

Table 6. RGB Auto-Offset Register Settings

Register	Value	Comments
0x0B	0x02	Sets red target to 4
0x0C	0x00	Must be written
0x0D	0x02	Sets green target to 4
0x0E	0x00	Must be written
0x0F	0x02	Sets blue target to 4
0x10	0x00	Must be written
0x18, Bits[3:1]	000	Sets red, green, and blue channels to ground clamp
0x1B, Bits[5:3]	110	Selects update rate and enables auto-offset.

Table 7. PbPr Auto-Offset Register Settings

Register	Value	Comments
0x0B	0x40	Sets Pr (red) target to 128
0x0C	0x00	Must be written
0x0D	0x02	Sets Y (green) target to 4
0x0E	0x00	Must be written
0x0F	0x40	Sets Pb (blue) target to 128
0x10	0x00	Must be written
0x18 Bits[3:1]	101	Sets Pb, Pr to midscale clamp and Y to ground clamp
0x1B, Bits[5:3]	110	Selects update rate and enables auto-offset

Automatic Gain Matching

The AD9983A includes circuitry to match the gains between the three channels to within 1% of each other. Matching the gains of each channel is necessary in order to achieve good color balance on a display. On products without this feature, gain matching is achieved by writing software that evaluates the output of each channel, calculates gain mismatches, then writes values to the gain registers of each channel to compensate. With the auto gain matching function, this software routine is no longer needed. To activate auto gain matching, set Register 0x3C, Bit 2 to Bit 1.

Auto gain matching has similar timing requirements to auto offset. It requires 16 data clock cycles to perform its function, starting immediately after the end of the clamp pulse. Unlike auto offset it does not require that these 16 clock cycles occur during the back porch reference time, although that is what is recommended. During auto gain matching operation, the data outputs of the AD9983A are frozen (held at the value they had just prior to operation). The auto gain matching function can be programmed to run continuously or on a one-time basis (see the 0x3C—Bit[3] Auto Gain Matching Hold section).

SYNC-ON-GREEN

The sync-on-green inputs (SOGIN0, SOGIN1) operate in two steps. First, they set a baseline clamp level off of the incoming video signal with a negative peak detector. Second, they set the sync trigger level to a programmable (Register 0x1D, Bits[7:3]) level (typically 128 mV) above the negative peak. The sync-on-green inputs must be ac-coupled to the green analog input through their own capacitors. The value of the capacitors must be 1 nF \pm 20%. If sync-on-green is not used, this connection is not required. The sync-on-green signal always has negative polarity.

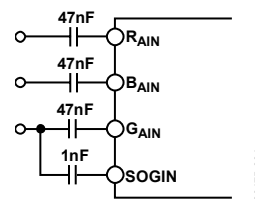


Figure 4. Typical Input Configuration

REFERENCE BYPASSING

REFLO and REFHI are connected to each other by a 10 μ F capacitor. These references are used by the input ADC circuitry.

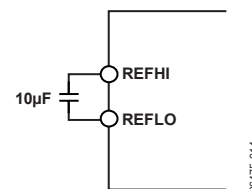


Figure 5. Input Amplifier Reference Capacitors

CLOCK GENERATION

A PLL is used to generate the pixel clock. The Hsync input provides a reference frequency to the PLL. A voltage controlled oscillator (VCO) generates a much higher pixel clock frequency. The pixel clock is divided by the PLL divide value (Register 0x01 and Register 0x02) and phase-compared with the Hsync input. Any error is used to shift the VCO frequency and maintain lock between the two signals.

The stability of this clock is a very important element in providing the clearest and most stable image. During each pixel time, there is a period during which the signal slews from the old pixel amplitude and settles at its new value. Then there is a time when the input voltage is stable, before the signal must slew to a new value (see Figure 6). The ratio of the slewing time to the stable time is a function of the bandwidth of the graphics DAC and the bandwidth of the transmission system (cable and termination). It is also a function of the overall pixel rate. Clearly, if the dynamic characteristics of the system remain fixed, then the slewing and settling time is likewise fixed. This time must be subtracted from the total pixel period, leaving the stable period. At higher pixel frequencies, the total cycle time is shorter and the stable pixel time also becomes shorter.

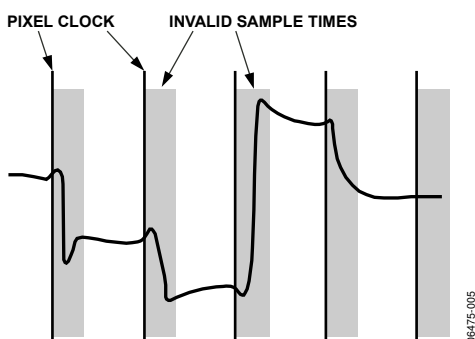


Figure 6. Pixel Sampling Times

Any jitter in the clock reduces the precision with which the sampling time can be determined and must also be subtracted from the stable pixel time. Considerable care has been taken in the design of the AD9983A clock generation circuit to minimize jitter. The clock jitter of the AD9983A is low in all operating modes, making the reduction in the valid sampling time due to jitter negligible.

The PLL characteristics are determined by the loop filter design, the PLL charge pump current, and the VCO range setting. The loop filter design is shown in Figure 7. Recommended settings of the VCO range and charge pump current for VESA standard display modes are listed in Table 10.

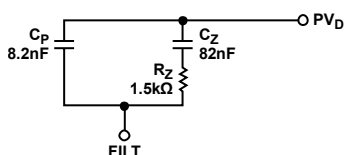


Figure 7. PLL Loop Filter Detail

Four programmable registers are provided to optimize the performance of the PLL. These registers are the 12-Bit Divisor Register, the 2-Bit VCO Range Register, the 3-Bit Charge Pump Current Register, and the 5-Bit Phase Adjust Register.

The 12-Bit Divisor Register

The input Hsync frequencies can accommodate any Hsync as long as the product of the Hsync and the PLL divisor falls within the operating range of the VCO. The PLL multiplies the frequency of the Hsync signal, producing pixel clock frequencies in the range of 10 MHz to 140 MHz. The divisor register controls the exact multiplication factor. This register may be set to any value between 2 and 4095 as long as the output frequency is within range.

The 2-Bit VCO Range Register

To improve the noise performance of the AD9983A, the VCO operating frequency range is divided into four overlapping regions. The VCO range register sets this operating range. The frequency ranges for the four regions are shown in Table 8.

Table 8. VCO Frequency Ranges

PV1	PV0	Pixel Clock Range (MHz)	KVCO Gain (MHz/V)
0	0	10 to 21	150
0	1	21 to 42	150
1	0	42 to 84	150
1	1	84 to 140	150

The 3-Bit Charge Pump Current Register

This register varies the current that drives the low pass loop filter. The possible current values are listed in Table 9.

Table 9. Charge Pump Current/Control Bits

Ip2	Ip1	Ip0	Current (μ A)
0	0	0	50
0	0	1	100
0	1	0	150
0	1	1	250
1	0	0	350
1	0	1	500
1	1	0	750
1	1	1	1500

The 5-Bit Phase Adjust Register

The phase of the generated sampling clock can be shifted to locate an optimum sampling point within a clock cycle. The phase adjust register provides 32 phase-shift steps of 11.25° each. The Hsync signal with an identical phase shift is available through the HSOUT pin. Phase adjust is still available if an external pixel clock is used. The COAST pin or the internal coast is used to allow the PLL to continue to run at the same frequency in the absence of the incoming Hsync signal or during disturbances in Hsync (such as from equalization pulses). This can be used during the vertical sync period or at any other time that the Hsync signal is unavailable.

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The polarity of the coast signal may be set through the coast polarity register (Register 0x18, Bits[6:5]). Also, the polarity of the Hsync signal can be set through the Hsync polarity register (Register 0x12, Bits[5:4]). For both Hsync and coast, a value of 1

is active high. The internal coast function is driven off the Vsync signal, which is typically a time when Hsync signals may be disrupted with extra equalization pulses.

Table 10. Recommended VCO Range and Charge Pump and Current Settings for Standard Display Formats

Standard	Resolution	Refresh Rate (Hz)	Horizontal Frequency (kHz)	Pixel Rate (MHz)	PLL Divider	VCO Range	Current	VCO Gear (R0x36[0])
VGA	640 × 480	60	31.500	25.175	800	00	101	0
		72	37.700	31.500	832	01	100	0
		75	37.500	31.500	840	01	100	0
		85	43.300	36.000	832	01	100	0
SVGA	800 × 600	56	35.100	36.000	1024	01	100	0
		60	37.900	40.000	1056	01	101	0
		72	48.100	50.000	1040	01	101	0
		75	46.900	49.500	1056	01	101	0
		85	53.700	56.250	1048	01	110	0
XGA	1024 × 768	60	48.400	65.000	1344	10	100	0
		70	56.500	75.000	1328	10	101	0
		75	60.000	78.750	1312	10	101	0
		80	64.000	85.500	1336	10	101	0
		85	68.300	94.500	1376	10	110	0
SXGA	1280 × 1024	60	64.000	108.000	1688	10	110	0
		75	80.000	135.000	1688	11	110	0
TV	480i	30	15.750	13.510	858	00	101	1
	480p	60	31.470	27.000	858	00	101	0
	576i	30	15.625	13.500	864	00	101	1
	576p	60	31.250	27.000	864	00	101	0
	720p	60	45.000	74.250	1650	10	101	0
	1035i	30	33.750	74.250	2200	10	101	0
	1080i	60	33.750	74.250	2200	10	101	0

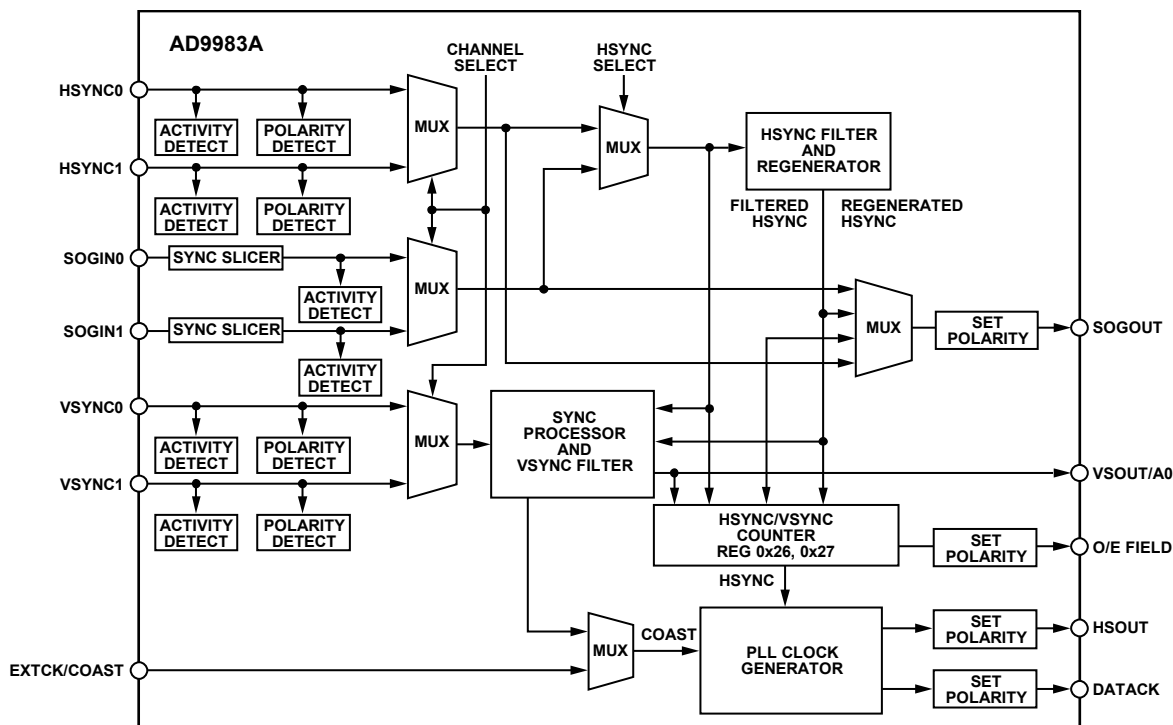


Figure 8. Sync Processing Block Diagram

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SYNC PROCESSING

The inputs of the sync processing section of the AD9983A are combinations of digital Hsyncs and Vsyncs, analog sync-on-green, or sync-on-Y signals, and an optional external coast signal. From these signals it generates a precise, jitter-free clock from its PLL; an odd/even field signal; HSOUT and VSOUT signals; a count of Hsyncs per Vsync; and a programmable SOGOUT. The main sync processing blocks are the sync slicer, sync separator, Hsync filter, Hsync regenerator, Vsync filter, and coast generator.

- The sync slicer extracts the sync signal from the green graphics or luminance video signal that is connected to the SOGINx input and outputs a digital composite sync.
- The sync separator's task is to extract Vsync from the composite sync signal, which can come from either the sync slicer or the HSYNCx inputs.
- The Hsync filter is used to eliminate any extraneous pulses from the HSYNCx or SOGINx inputs, outputting a clean, low jitter signal that is appropriate for mode detection and clock generation.

- The Hsync regenerator is used to recreate a clean, although not low jitter, Hsync signal that can be used for mode detection and counting Hsyncs per Vsync.
- The Vsync filter is used to eliminate spurious Vsyncs, maintain a stable timing relationship between the Vsync and Hsync output signals, and generate the odd/even field output.
- The coast generator creates a robust coast signal that allows the PLL to maintain its frequency in the absence of Hsync pulses.

Sync Slicer

The purpose of the sync slicer is to extract the sync signal from the green graphics or luminance video signal that is connected to the SOG input. The sync signal is extracted in a two step process. First, the SOG input is clamped to its negative peak, (typically 0.3 V below the black level). Next, the signal goes to a comparator with a variable trigger level (set by Register 0x1D, Bits[7:3]), but nominally 0.128 V above the clamped level. The sync slicer output is a digital composite sync signal containing both Hsync and Vsync information (see Figure 9).

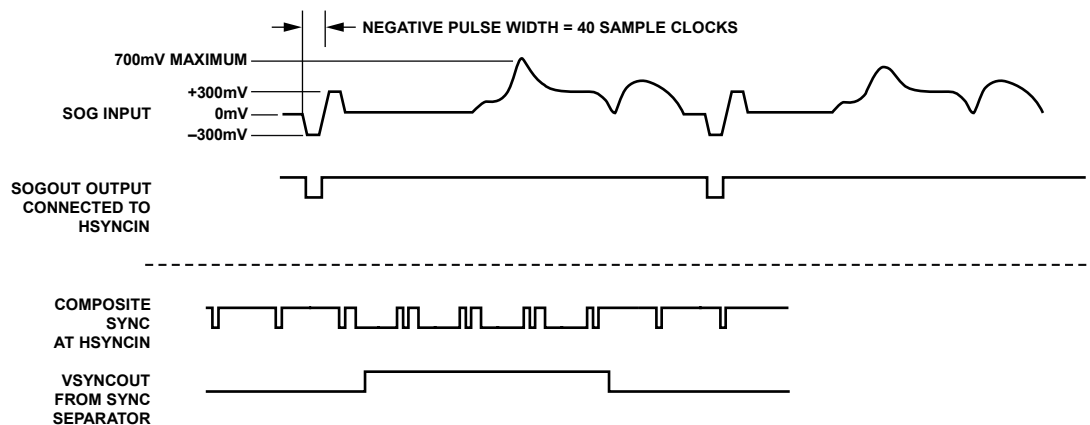


Figure 9. Sync Slicer and Sync Separator Output

Sync Separator

As part of sync processing, the sync separator's task is to extract Vsync from the composite sync signal. It works on the idea that the Vsync signal stays active for a much longer time than the Hsync signal. By using a digital low-pass filter and a digital comparator, it rejects pulses with small durations (such as Hsyncs and equalization pulses) and only passes pulses with large durations, such as Vsync (see Figure 9).

The threshold of the digital comparator is programmable for maximum flexibility. To program the threshold duration, write a value (N) to Register 0x11. The resulting pulse width is $N \times 200$ ns. So, if $N = 5$, the digital comparator threshold is 1 μ s. Any pulse less than 1 μ s is rejected, while any pulse greater than 1 μ s passes through.

There are two factors to consider when using the sync separator. First, the resulting clean Vsync output is delayed from the original Vsync by a duration equal to the digital comparator threshold ($N \times 200$ ns). Second, there is some variability to the 200 ns multiplier value. The maximum variability over all operating conditions is $\pm 20\%$ (160 ns to 240 ns). Since normal Vsync and Hsync pulse widths differ by a factor of approximately 500 or more, the 20% variability is not an issue.

Hsync Filter and Regenerator

The Hsync filter is used to eliminate any extraneous pulses from the Hsync or SOGIN inputs, outputting a clean, low jitter signal that is appropriate for mode detection and clock generation.

The Hsync regenerator is used to recreate a clean, although not low jitter, Hsync signal that can be used for mode detection and counting Hsyncs per Vsync. The Hsync regenerator has a high

degree of tolerance to extraneous and missing pulses on the Hsync input, but is not appropriate for use by the PLL in creating the pixel clock due to jitter.

The Hsync regenerator runs automatically and requires no setup to operate. The Hsync filter requires the setting up of a filter window. The filter window sets a periodic window of time around the regenerated Hsync leading edge where valid Hsyncs are allowed to occur. The general idea is that extraneous pulses on the sync input occur outside of this filter window and thus are filtered out. To set the filter window timing, program a value (x) into Register 0x23. The resulting filter window time is $\pm x$ times 25 ns around the regenerated Hsync leading edge. Just as for the sync separator threshold multiplier, allow a $\pm 20\%$ variance in the 25 ns multiplier to account for all operating conditions (20 ns to 30 ns range).

A second output from the Hsync filter is a status bit (Register 0x25, Bit 1) that tells whether extraneous pulses were present on the incoming sync signal or not. Often, extraneous pulses are included for copy protection purposes, so this status bit can be used to detect that.

The filtered Hsync (rather than the raw HSYNCx/SOGINx signal) for pixel clock generation by the PLL is controlled by Register 0x20, Bit 2. The regenerated Hsync (rather than the raw Hsync/SOGIN signal) for the sync processing is controlled by Register 0x20, Bit 1. Use of the filtered Hsync and regenerated Hsync is recommended. See Figure 10 for an illustration of a filtered Hsync.

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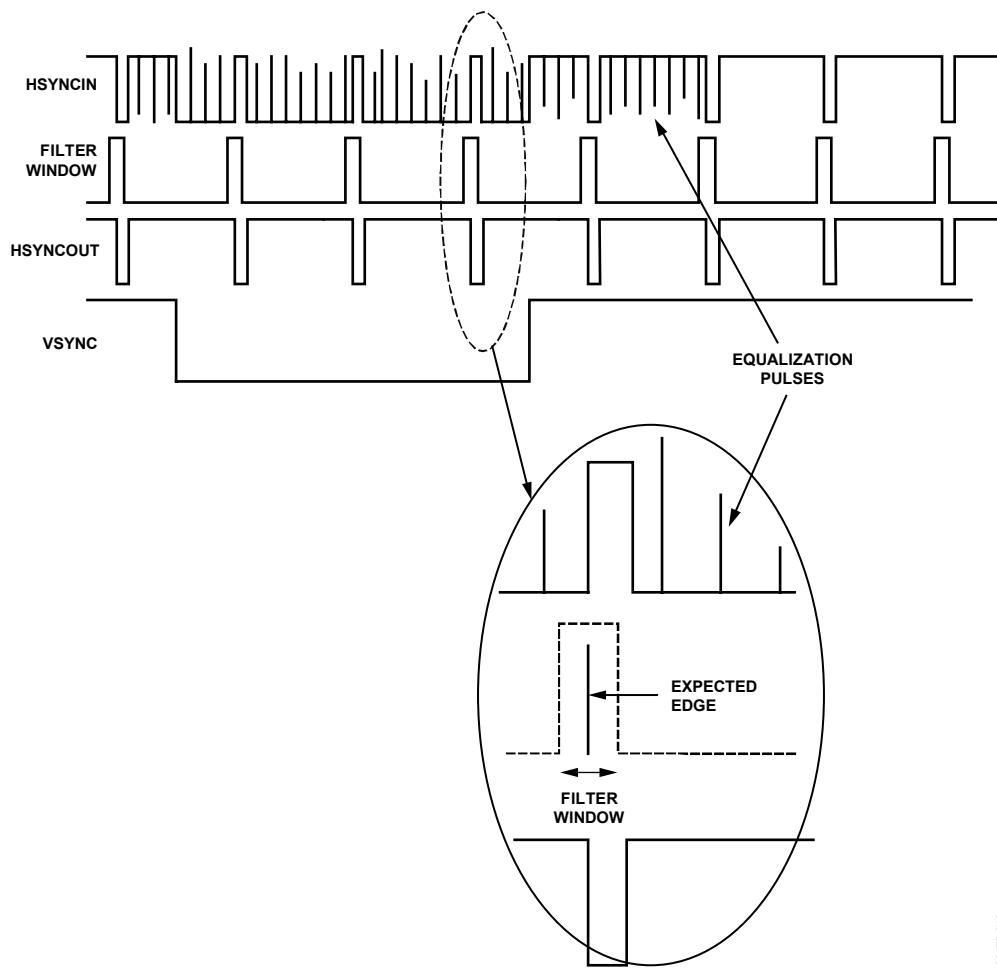


Figure 10. Sync Processing Filter

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Vsync Filter and Odd/Even Fields

The Vsync filter is used to eliminate spurious Vsyns, maintain a stable timing relationship between the Vsync and Hsync output signals, and generate the odd/even field output.

The filter works by examining the placement of Vsync with respect to Hsync and if necessary shifting it in time slightly. The goal is to keep the Vsync and Hsync leading edges from switching at the same time, thus eliminating confusion as to when the first line of a frame occurs. Register 0x14, Bit 2 enables the Vsync filter. Use of the Vsync filter is recommended for all cases, including interlaced video, and is required when using the Hsyncs per Vsync counter. Figure 11 and Figure 12 illustrate even/odd field determination in two situations.

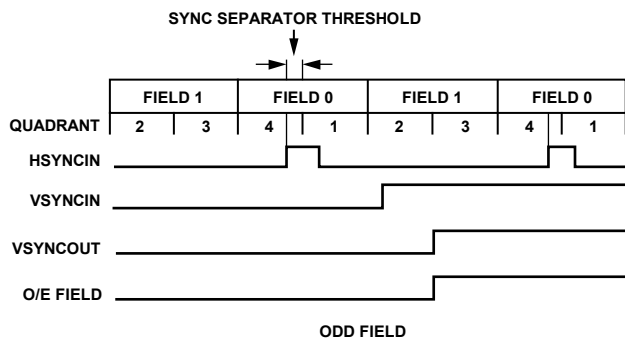


Figure 11. Vsync Filter—Odd Field

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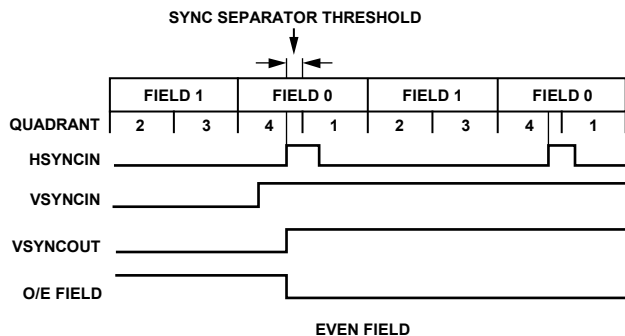


Figure 12. Vsync Filter—Even Field

06475-018

AD9983A

POWER MANAGEMENT

To meet display requirements for low standby power, the AD9983A includes a power-down mode. The power-down state can be controlled manually (via Pin 17 or Register 0x1E, Bit 3), or automatically by the chip. If automatic control is selected (Register 0x1E, Bit 4), the AD9983A decision is based on the status of the sync detect bits (Register 0x24, Bit 2, Bit 3, Bit 6, and Bit 7). If either an Hsync or a sync-on-green input is detected on any input, the chip powers up, otherwise it powers down. For manual control, the AD9983A allows flexibility of control through both a dedicated pin and a register bit. The dedicated pin allows a hardware watchdog circuit to control power-down, while the register bit allows power-down to be controlled by software. With manual power-down control, the polarity of the power-down pin must be set (Register 0x1E, Bit 2) whether the pin is used or not. If unused, it is recommended to set the polarity to active high and hardwire the pin to ground with a 10 kΩ resistor.

In power-down mode, there are several circuits that continue to operate as normal. The serial register and sync detect circuits maintain power so that the AD9983A can be woken up from its power-down state. The bandgap circuit maintains power because it is needed for sync detection. The sync-on-green and SOGOUT functions continue to operate because the SOGOUT output is needed when sync detection is performed by a secondary chip. All of these circuits require minimal power to operate. Typical standby power on the AD9983A is about 50 mW.

There are two options that can be selected when in power-down. These are controlled by Bit 0 and Bit 1 in Register 0x1E. Bit 0 controls whether the SOGOUT pin is in high impedance or not. In most cases, the user will not place SOGOUT in high impedance during normal operation. The option to put SOGOUT in high impedance is included mainly to allow for factory testing modes. Bit 1 keeps the AD9983A powered up while placing only the outputs in high impedance. This option is useful when the data outputs from two chips are connected on a PCB and the user wants to switch instantaneously between the two.

Table 11. Power-Down Control and Mode Descriptions

Mode	Inputs			Powered On/Comments
	Auto Power-Down Control ¹	Power-Down ²	Sync Detect ³	
Power-Up	1	X	1	Everything
Power-Down	1	X	0	Only the serial bus, sync activity detect, SOG, bandgap reference
Power-Up	0	0	X	Everything
Power-Down	0	1	X	Only the serial bus, sync activity detect, SOG, bandgap reference

¹ Auto power-down control is set by Register 0x1E, Bit 4.

² Power-down is controlled by OR'ing Pin 17 with Register 0x1E, Bit 3. The polarity of Pin 17 is set by Register 0x1E, Bit 2.

³ Sync detect is determined by OR'ing Register 0x24, Bit 2, Bit 3, Bit 6, and Bit 7.

TIMING DIAGRAMS

The timing diagrams in Figure 13 to Figure 16 show the operation of the AD9983A. The output data clock signal is created so that its rising edge always occurs between data transitions and can be used to latch the output data externally. There is a pipeline in the AD9983A, which must be flushed before valid data becomes available. This means six data sets are presented before valid data is available.

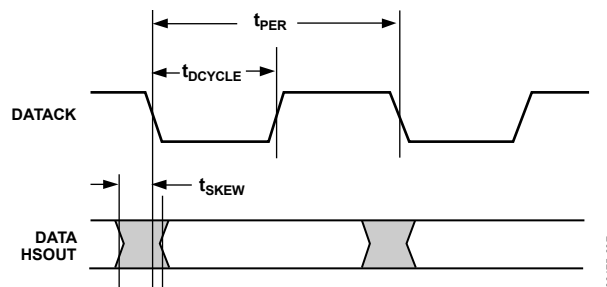


Figure 13. Output Timing

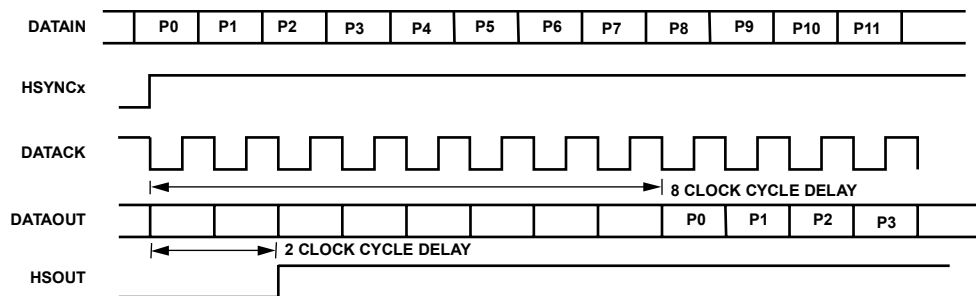
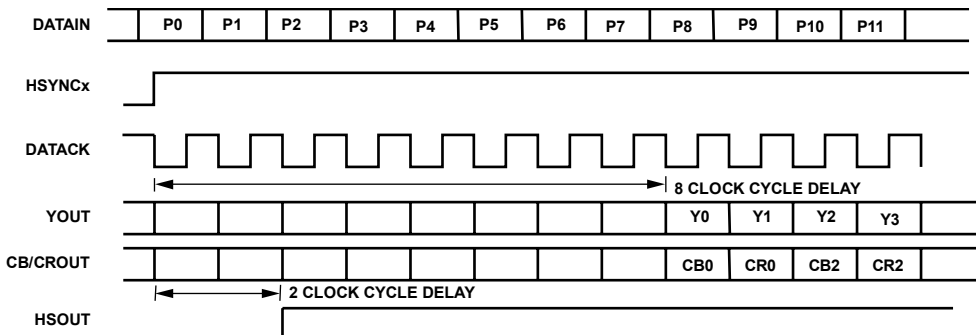


Figure 14. 4:4:4 Timing Mode

06475-008

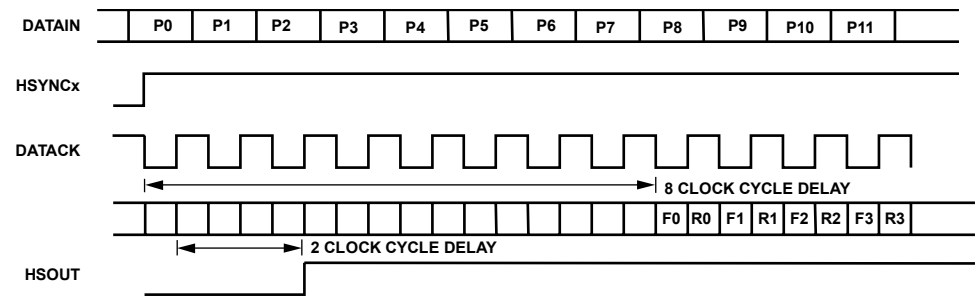


NOTES

1. PIXEL AFTER HSOUT CORRESPONDS TO BLUE INPUT.
2. EVEN NUMBER OF PIXEL DELAY BETWEEN HSOUT AND DATAOUT.

Figure 15. 4:2:2 Timing Mode

06475-009



DDR NOTES

1. OUTPUT DATAACK MAY BE DELAYED 1/4 CLOCK PERIOD IN THE REGISTERS.
2. SEE PROJECT DOCUMENT FOR VALUES OF F (FALLING EDGE) AND R (RISING EDGE).
3. FOR DDR 4:2:2 MODE: TIMING IS IDENTICAL, VALUES OF F AND R CHANGE.

GENERAL NOTES

1. DATA DELAY MAY VARY ± ONE CLOCK CYCLE, DEPENDING ON PHASE SETTING.
2. ADCs SAMPLE INPUT ON FALLING EDGE OF DATAACK.
3. HSYNC SHOWN IS ACTIVE HIGH (EDGE SHOWN IS LEADING EDGE).

Figure 16. Double Data Rate (DDR) Timing Mode

06475-010

HSYNC TIMING

The Hsync is processed in the AD9983A to eliminate ambiguity in the timing of the leading edge with respect to the phase-delayed pixel clock and data.

The Hsync input is used as a reference to generate the pixel sampling clock. The sampling phase can be adjusted with respect to Hsync through a full 360° in 32 steps via the phase adjust register (to optimize the pixel sampling time). Display systems use Hsync to align memory and display write cycles, so it is important to have a stable timing relationship between Hsync output (HSOUT) and the data clock (DATAACK).

Three things happen to Hsync in the AD9983A. First, the polarity of Hsync input is determined and thus has a known output polarity. The known output polarity can be programmed either active high or active low (Register 0x12, Bit 3). Second, HSOUT is aligned with DATAACK and data outputs. Third, the duration of HSOUT (in pixel clocks) is set via Register 0x13. HSOUT is the sync signal that should be used to drive the rest of the display system.

COAST TIMING

In most computer systems, the Hsync signal is provided continuously on a dedicated wire. In these systems, the coast input and function are unnecessary and should not be used.

In some systems, however, Hsync is disturbed during the vertical sync period (Vsync). In some cases, Hsync pulses disappear. In other systems, such as those that employ composite sync (Csync) signals or embedded sync-on-green, Hsync may include equalization pulses or other distortions during Vsync. To avoid upsetting the clock generator during Vsync, it is important to ignore these distortions. If the pixel clock PLL sees extraneous pulses, it attempts to lock to this new frequency, and will have changed frequency by the end of the Vsync period. It then takes a few lines of correct Hsync timing to recover at the beginning of a new frame, resulting in a tearing of the image at the top of the display.

The COAST input is provided to eliminate this problem. It is an asynchronous input that disables the PLL input and holds the clock at its current frequency. The PLL can free run for several lines without significant frequency drift. Coast can be generated internally by the AD9983A (see Register 0x18) or can be provided externally by the graphics controller.

When internal coast is selected (Register 0x18, Bit 7 = 0, and Register 0x14, Bits[7:6] to select source), Vsync is used as a basis for determining the position of COAST. The internal coast signal is enabled a programmed number of Hsync periods before the periodic Vsync signal (Precoast Register 0x16) and dropped a programmed number of Hsync periods after Vsync (Postcoast Register 0x17). It is recommended that the Vsync filter be enabled when using the internal coast function to allow the AD9983A to determine precisely the number of Hsyncs/Vsync and their location. In many applications where disruptions occur and coast is used, values of 2 for Precoast and 10d for Postcoast are sufficient to avoid most extraneous pulses.

OUTPUT FORMATTER

The output formatter is capable of generating several output formats to be presented to the 24 data output pins. The output formats and the pin assignments for each format are listed in Table 12. Also, there are several clock options for the output clock. The user may select the pixel clock, a 90° phase-shifted pixel clock, a 2× pixel clock, or a fixed frequency 40 MHz clock for test purposes. The output clock may also be inverted.

Data output is available as 24-pin RGB or YCbCr, or if either 4:2:2 or 4:4:4 DDR is selected, a secondary channel is available. This secondary channel is always 4:2:2 DDR and allows the flexibility of having a second channel with the same video data that can be utilized by either another display or even a storage device. Depending on the choice of output modes, the primary output can be 24 pins, 16 pins, or as little as 12 pins.

Mode Descriptions

4:4:4

All channels come out with their 8 data bits at the same time. Data is aligned to the negative edge of the clock for easy capture. This is the normal 24-bit output mode for RGB or 4:4:4 YCbCr.

4:2:2

Red and green channels contain 4:2:2 formatted data (16 pins) with Y data on the green channel and Cb, Cr data on the red channel. Data is aligned to the negative edge of the clock. The blue channel contains the secondary channel with Cb, Y, Cr, Y formatted 4:2:2 DDR data. The data edges are aligned to both edges of the pixel clock, so use of the 90° clock may be necessary to capture the DDR data.

4:4:4 DDR

This mode puts out full 4:4:4 data on 12 bits of the red and green channels, thus saving 12 pins. The first half (RGB[11:0]) of the 24-bit data is sent on the rising edge and the second half (RGB[23:12]) is sent on the falling edge. DDR 4:2:2 data is sent on the blue channel, as in 4:2:2 mode.

$$\text{RGB [23:0]} = \text{R [7:0]} + \text{G [7:0]} + \text{B [7:0]}, \text{ so}$$

$$\text{RGB [23:12]} = \text{R [7:0]} + \text{G [7:4]} \text{ and}$$

$$\text{RGB [11:0]} = \text{G [3:0]} + \text{B [7:0]}$$

Table 12. Output Formats

Port	Red								Green								Blue							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
4:4:4	Red/Cr								Green/Y								Blue/Cb							
4:2:2 ¹	Cb, Cr								Y								DDR 4:2:2 ↑ Cb, Cr ↓ Y, Y							
4:4:4 DDR	DDR ↑ ² G [3:0]				DDR ↑ B [7:4]				DDR ↑ B [3:0]				N/A				DDR 4:2:2 ↑ Cb, Cr							
	DDR ↓ ² R [7:0]								DDR ↓ G [7:4]				N/A				DDR 4:2:2 ↓ Y, Y							

¹ For 4:2:2 Cb sent before Cr.

² Arrows in table indicate clock edge. Rising edge of clock = ↑, falling edge = ↓.

2-WIRE SERIAL CONTROL PORT

A 2-wire serial interface control interface is provided. Up to two AD9983A devices may be connected to the 2-wire serial interface, with each device having a unique address.

The 2-wire serial interface comprises a clock (SCL) and a bi-directional data (SDA) pin. The analog flat panel interface acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled high by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is low. If SDA changes state while SCL is high, the serial interface interprets that action as a start or stop sequence.

The following are the five components to serial bus operation:

- Start signal
- Slave address byte
- Base register address byte
- Data byte to read or write
- Stop signal

When the serial interface is inactive (SCL and SDA are high), communications are initiated by sending a start signal. The start signal is a high-to-low transition on SDA while SCL is high. This signal alerts all slaved devices that a data transfer sequence is coming.

The first 8 bits of data transferred after a start signal comprise a 7-bit slave address (the first 7 bits) and a single R/W bit (the eighth bit). The R/W bit indicates the direction of data transfer, read from 1 or write to 0 on the slave device. If the transmitted slave address matches the address of the device, the AD9983A acknowledges the match by bringing SDA low on the ninth SCL pulse. If the addresses do not match, the AD9983A does not acknowledge it.

Table 13. Serial Port Addresses

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
A6 (MSB)	A5	A4	A3	A2	A1	A0
1	0	0	1	1	0	0
1	0	0	1	1	0	1

DATA TRANSFER VIA SERIAL INTERFACE

For each byte of data read or written, the MSB is the first bit in the sequence.

If the AD9983A does not acknowledge the master device during a write sequence, the SDA remains high so the master can generate a stop signal. If the master device does not acknowledge the AD9983A during a read sequence, the AD9983A interprets this as end of data. The SDA remains high so the master can generate a stop signal.

Writing data to specific control registers of the AD9983A requires writing to the 8-bit address of the control register of interest after the slave address has been established. This control register address is the base address for subsequent write operations. The base address auto-increments by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address does not increment and remains at its maximum value of 0x2E. Any base address higher than 0x2E will not produce an acknowledge signal. Data are read from the control registers of the AD9983A in a similar manner. Reading requires two data transfer operations:

The base address must be written with the R/W bit of the slave address byte low to set up a sequential read operation. Reading (the R/W bit of the slave address byte high) begins at the previously established base address. The address of the read register auto-increments after each byte is transferred.

To terminate a read/write sequence to the AD9983A, a stop signal must be sent. A stop signal comprises a low-to-high transition of SDA while SCL is high.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

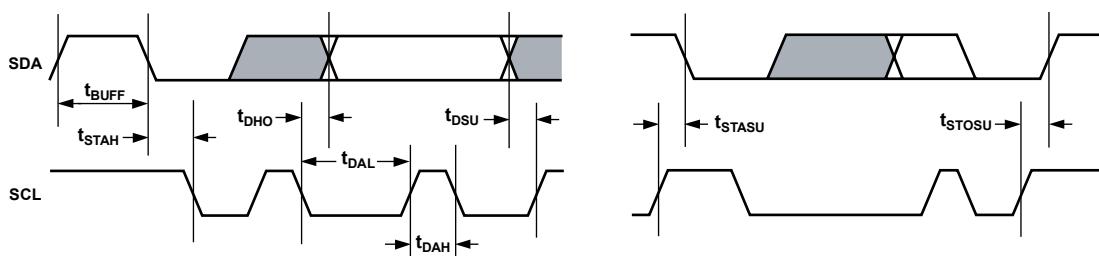


Figure 17. Serial Port Read/Write Timing

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Serial Interface Read/Write Examples

Write to One Control Register

1. Start signal
2. Slave address byte (R/\overline{W} bit = low)
3. Base address byte
4. Data byte to base address
5. Stop signal

Write to Four Consecutive Control Registers

1. Start signal
2. Slave address byte (R/\overline{W} bit = low)
3. Base address byte
4. Data byte to base address
5. Data byte to (base address + 1)
6. Data byte to (base address + 2)
7. Data byte to (base address + 3)
8. Stop signal

Read from One Control Register

1. Start signal
2. Slave address byte (R/\overline{W} bit = low)
3. Base address byte
4. Start signal
5. Slave address byte (R/\overline{W} bit = high)
6. Data byte from base address
7. Stop signal

Read from Four Consecutive Control Registers

1. Start signal
2. Slave address byte (R/\overline{W} bit = low)
3. Base address byte
4. Start signal
5. Slave address byte (R/\overline{W} bit = high)
6. Data byte from base address
7. Data byte from (base address + 1)
8. Data byte from (base address + 2)
9. Data byte from (base address + 3)
10. Stop signal

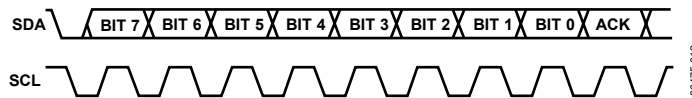


Figure 18. Serial Interface—Typical Byte Transfer

2-WIRE SERIAL REGISTER MAP

The AD9983A is initialized and controlled by a set of registers that determine the operating modes. An external controller is employed to write and read the control registers through the 2-wire serial interface port.

Table 14. Control Register Map

Hex Address	Read/Write, Read Only	Bits	Default Value	Register Name	Description
0x00	RO	7:0		Chip Revision	An 8-bit register that represents the silicon revision level.
0x01	R/W	7:0	0110 1001	PLL Div MSB	This register is for Bits [11:4] of the PLL divider. Larger values mean the PLL operates at a faster rate. This register should be loaded first whenever a change is needed. (This will give the PLL more time to lock). ¹
0x02	R/W	7:4	1101 ****	PLL Div LSB	LSBs of the PLL Divider Word. Links to the PLL Div MSB to make a 12-bit register. ¹
0x03	R/W	7:6 5:3 2	01** **** **00 1*** **** *0**	VCO/CPMP	VCO Range. Selects VCO frequency range. (See PLL section). Charge Pump Current. Varies the current that drives the low-pass filter. (See PLL section). External Clock Enable.
0x04	R/W	7:3	1000 0***	Phase Adjust	ADC Clock Phase Adjustment. Larger values mean more delay. (1 LSB = T/32).
0x05	R/W	6:0	*100 0000	Red Gain MSB	7-Bit Red Channel Gain Control. Controls the ADC input range (contrast) of each respective channel. Bigger values give less contrast. ²
0x06	R/W	7:0	0000 0000		Must be written to 0x00 following a write of Reg. 0x05 for proper operation.
0x07	R/W	6:0	*100 0000	Green Gain MSB	7-Bit Green Channel Gain Control. Controls the ADC input range (contrast) of each respective channel. Bigger values give less contrast. ²
0x08	R/W	7:0	0000 0000		Must be written to 0x00 following a write of Reg. 0x07 for proper operation.
0x09	R/W	6:0	*100 0000	Blue Gain MSB	7-Bit Blue Channel Gain Control. Controls the ADC input range (contrast) of each respective channel. Bigger values give less contrast. ²
0x0A	R/W	7:0	0000 0000		Must be written to 0x00 following a write of Reg. 0x09 for proper operation.
0x0B	R/W	7:0	0100 0000	Red Offset MSB	8-Bit MSB of the Red Channel Offset Control. Controls the dc offset (brightness) of each respective channel. Bigger values decrease brightness. ¹
0x0C	R/W	7	0*** ****	Red Offset LSB	Linked with Reg. 0x0B to form the 9-bit red offset that controls the dc offset (brightness) of the red channel in auto-offset mode.
0x0D	R/W	7:0	0100 0000	Green Offset MSB	8-Bit MSB of the Green Channel Offset Control. Controls the dc offset (brightness) of each respective channel. Bigger values decrease brightness. ¹
0x0E	R/W	7	0*** ****	Green Offset LSB	Linked with Reg. 0x0D to form the 9-bit green offset that controls the dc offset (brightness) of the green channel in auto-offset mode.
0x0F	R/W	7:0	0100 0000	Blue Offset MSB	8-Bit MSB of the Red Channel Offset Control. Controls the dc offset (brightness) of each respective channel. Bigger values decrease brightness. ¹
0x10	R/W	7	0*** ****	Blue Offset LSB	Linked with Reg. 0x0F to form the 9-bit blue offset that controls the dc offset (brightness) of the blue channel in auto-offset mode.
0x11	R/W	7:0	0010 0000	Sync Separator Threshold	This register sets the threshold of the sync separator's digital comparator.

AD9983A

Hex Address	Read/Write, Read Only	Bits	Default Value	Register Name	Description
0x12	R/W	7 6 5 4 3	0*** **** *0** **** **0* **** ***1 **** **** 1***	Hsync Control	<p>Active Hsync Override. 0 = The chip determines the active Hsync source 1 = The active Hsync source is set by Reg. 0x12, Bit 6</p> <p>Selects the source of the Hsync for PLL and sync processing. This bit is used only if Reg. 0x12, Bit 7 is set to 1 or if both syncs are active. 0 = Hsync is from HSYNCx input pin 1 = Hsync is from SOGINx</p> <p>Hsync Input Polarity Override. 0 = The chip selects the Hsync input polarity 1 = The polarity of the input Hsync is controlled by Reg. 0x12, Bit 4 This applies to both HSYNC0 and HSYNC1.</p> <p>Hsync Input Polarity. This bit is used only if Reg. 0x12, Bit 5 is set to 1. 0 = Active low input Hsync 1 = Active high input Hsync</p> <p>Sets the polarity of the Hsync output signal. 0 = Active low Hsync output 1 = Active high Hsync output</p>
0x13	R/W	7:0	0010 0000	Hsync Duration	Sets the number of pixel clocks that HSOUT is active.
0x14	R/W	7 6 5 4 3 2 1	0*** **** *0** **** **0* **** ***1 **** **** 1*** **** *0** **** **0*	Vsync Control	<p>Active Vsync Override. 0 = The chip determines the active Vsync source 1 = The active Vsync source is set by Reg. 0x14, Bit 6</p> <p>Selects the source of Vsync for the sync processing. This bit is used only if Reg. 0x14, Bit 7 is set to 1. 0 = Vsync is from the Vsync input pin 1 = Vsync is from the sync separator</p> <p>Vsync Input Polarity Override. This applies to both VSYNC0 and VSYNC1. 0 = The chip selects the input Vsync polarity 1 = The polarity of the input Vsync is set by Reg. 0x14, Bit 4</p> <p>Vsync Input Polarity. This bit is used only if Reg. 0x14, Bit 5 is set to 1. 0 = Active low input Vsync 1 = Active high input Vsync</p> <p>Sets the polarity of the output Vsync signal. 0 = Active low output Vsync 1 = Active high output Vsync</p> <p>Vsync Filter Enable. This needs to be enabled when using the Hsync to Vsync counter. 0 = The Vsync filter is disabled 1 = The Vsync filter is enabled</p> <p>Enables the Vsync duration block. This is designed to be used with the Vsync filter. 0 = Vsync output duration is unchanged 1 = Vsync output duration is set by Reg. 0x15</p>
0x15	R/W	7:0	0000 1010	Vsync Duration	Sets the number of Hsyncs that Vsync out is active. This is only used if Reg. 0x14, Bit 1 is set to 1.
0x16	R/W	7:0	0000 0000	Precoast	The number of Hsync periods to coast prior to Vsync.
0x17	R/W	7:0	0000 0000	Postcoast	The number of Hsync periods to coast after Vsync.
0x18	R/W	7 6 5	0*** **** *0** **** **1* ****	Coast and Clamp Control	<p>Coast Source. Selects the source of the coast signal. 0 = Using internal coast generated from Vsync 1 = Using external coast signal from external COAST pin</p> <p>Coast Polarity Override. 0 = The chip selects the external coast polarity 1 = The polarity of the external coast signal is set by Reg. 0x18, Bit 5</p> <p>Coast Input Polarity. This bit is used only if Reg. 0x18, Bit 6 is set to 1. 0 = Active low external coast 1 = Active high external coast</p>