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# 10-Bit CCD Signal Processor with *Precision Timing*™ Generator

## AD9991

**ANALOG DEVICES**

## FEATURES
**6-Phase Vertical Transfer Clock Support**
**Correlated Double Sampler (CDS)**
**6 dB to 42 dB 10-Bit Variable Gain Amplifier (VGA)**
**10-Bit 27 MHz A/D Converter**
**Black Level Clamp with Variable Level Control**
**Complete On-Chip Timing Generator**
**Precision Timing Core with 800 ps Resolution**
**On-Chip 3 V Horizontal and RG Drivers**
**2-Phase and 4-Phase H-Clock Modes**
**Electronic and Mechanical Shutter Modes**
**On-Chip Driver for External Crystal**
**On-Chip Sync Generator with External Sync Input**
**56-Lead LFCSP Package**

## APPLICATIONS
**Digital Still Cameras**
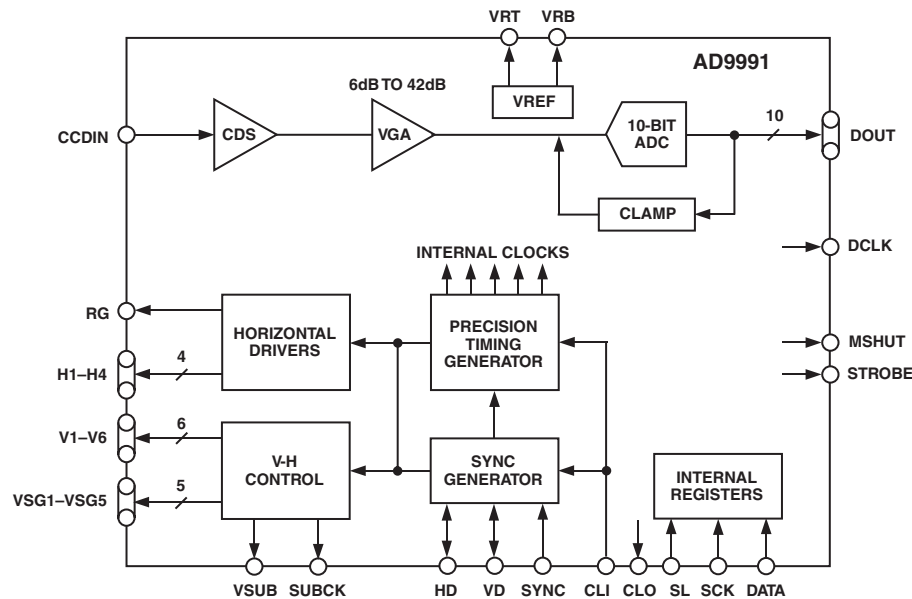**Digital Video Camcorders**
**Industrial Imaging**

## GENERAL DESCRIPTION
The AD9991 is a highly integrated CCD signal processor for digital still camera and camcorder applications. It includes a complete analog front end with A/D conversion, combined with a full-function programmable timing generator. The timing generator is capable of supporting both 4- and 6-phase vertical clocking. A Precision Timing core allows adjustment of high speed clocks with 800 ps resolution at 27 MHz operation.

The AD9991 is specified at pixel rates of up to 27 MHz. The analog front end includes black level clamping, CDS, VGA, and a 10-bit A/D converter. The timing generator provides all the necessary CCD clocks: RG, H-clocks, V-clocks, sensor gate pulses, substrate clock, and substrate bias control. Operation is programmed using a 3-wire serial interface.

Packaged in a space-saving 56-lead LFCSP, the AD9991 is specified over an operating temperature range of –20°C to +85°C.

## FUNCTIONAL BLOCK DIAGRAM



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# AD9991

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# AD9991–SPECIFICATIONS

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| TEMPERATURE RANGE | | | | |
|    Operating | –20 | | +85 | °C |
|    Storage | –65 | | +150 | °C |
| POWER SUPPLY VOLTAGE | | | | |
|    AVDD (AFE Analog Supply) | 2.7 | 3.0 | 3.6 | V |
|    TCVDD (Timing Core Analog Supply) | 2.7 | 3.0 | 3.6 | V |
|    RGVDD (RG Driver) | 2.7 | 3.0 | 3.6 | V |
|    HVDD (H1–H4 Drivers) | 2.7 | 3.0 | 3.6 | V |
|    DRVDD (Data Output Drivers) | 2.7 | 3.0 | 3.6 | V |
|    DVDD (Digital) | 2.7 | 3.0 | 3.6 | V |
| POWER DISSIPATION  (See TPC 1 for Power Curves) | | | | |
|    27 MHz, Typ Supply Levels, 100 pF H1–H4 Loading | | 270 | | mW |
|    Power from HVDD Only* | | 100 | | mW |
|    Standby 1 Mode | | 105 | | mW |
|    Standby 2 Mode | | 10 | | mW |
|    Standby 3 Mode | | 0.5 | | mW |
| MAXIMUM CLOCK RATE (CLI) | 27 | | | MHz |

*The total power dissipated by the HVDD supply may be approximated using the equation

$$Total\ HVDD\ Power = [C_{LOAD} \times HVDD \times Pixel\ Frequency] \times HVDD \times Number\ of\ H\text{-}outputs\ used$$

Reducing the H-loading, using only two of the outputs, and/or using a lower HVDD supply will reduce the power dissipation.

Specifications subject to change without notice.

## DIGITAL SPECIFICATIONS (RGVDD = HVDD = DVDD = DRVDD = 2.7 V to 3.6 V, $C_L$ = 20 pF, $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.)

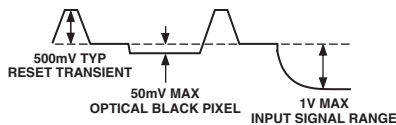| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LOGIC INPUTS | | | | | |
|    High Level Input Voltage | $V_{IH}$ | 2.1 | | | V |
|    Low Level Input Voltage | $V_{IL}$ | | | 0.6 | V |
|    High Level Input Current | $I_{IH}$ | | 10 | | µA |
|    Low Level Input Current | $I_{IL}$ | | 10 | | µA |
|    Input Capacitance | $C_{IN}$ | | 10 | | pF |
| LOGIC OUTPUTS (Except H and RG) | | | | | |
|    High Level Output Voltage @ $I_{OH}$ = 2 mA | $V_{OH}$ | 2.2 | | | V |
|    Low Level Output Voltage @ $I_{OL}$ = 2 mA | $V_{OL}$ | | | 0.5 | V |
| RG and H-DRIVER OUTPUTS (H1–H4) | | | | | |
|    High Level Output Voltage @ Max Current | $V_{OH}$ | VDD – 0.5 | | | V |
|    Low Level Output Voltage @ Max Current | $V_{OL}$ | | | 0.5 | V |
|    Maximum Output Current (Programmable) | | 30 | | | mA |
|    Maximum Load Capacitance (For Each Output) | | 100 | | | pF |

Specifications subject to change without notice.

# AD9991

## ANALOG SPECIFICATIONS (AVDD = 3.0 V, f_CLI = 27 MHz, Typical Timing Specifications, T_MIN to T_MAX, unless otherwise noted.)

| Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|
| CDS* | | | | | |
| Allowable CCD Reset Transient | | 500 | | mV | |
| Max Input Range before Saturation | 1.0 | | | V p-p | |
| Max CCD Black Pixel Amplitude | | ±50 | | mV | |
| VARIABLE GAIN AMPLIFIER (VGA) | | | | | |
| Gain Control Resolution | | 1024 | | Steps | |
| Gain Monotonicity | | Guaranteed | | | |
| Gain Range | | | | | |
| Min Gain (VGA Code 0) | | 6 | | dB | |
| Max Gain (VGA Code 1023) | | 42 | | dB | |
| BLACK LEVEL CLAMP | | | | | |
| Clamp Level Resolution | | 256 | | Steps | |
| Clamp Level | | | | | Measured at ADC output. |
| Min Clamp Level (Code 0) | | 0 | | LSB | |
| Max Clamp Level (Code 255) | | 63.75 | | LSB | |
| A/D CONVERTER | | | | | |
| Resolution | 10 | | | Bits | |
| Differential Nonlinearity (DNL) | −1.0 | ±0.5 | +1.0 | LSB | |
| No Missing Codes | | Guaranteed | | | |
| Full-Scale Input Voltage | | 2.0 | | V | |
| VOLTAGE REFERENCE | | | | | |
| Reference Top Voltage (REFT) | | 2.0 | | V | |
| Reference Bottom Voltage (REFB) | | 1.0 | | V | |
| SYSTEM PERFORMANCE | | | | | Includes entire signal chain. |
| Gain Accuracy | | | | | |
| Low Gain (VGA Code 0) | 5.0 | 5.5 | 6.0 | dB | Gain = (0.0351 × Code) + 6 dB |
| Max Gain (VGA Code 1023) | 40.5 | 41.5 | 42.5 | dB | |
| Peak Nonlinearity, 500 mV Input Signal | | 0.2 | | % | 12 dB gain applied. |
| Total Output Noise | | 0.25 | | LSB rms | AC grounded input, 6 dB gain applied. |
| Power Supply Rejection (PSR) | | 50 | | dB | Measured with step change on supply. |

*Input signal characteristics defined as follows:



**500mV TYP RESET TRANSIENT**

**50mV MAX OPTICAL BLACK PIXEL**

**1V MAX INPUT SIGNAL RANGE**

Specifications subject to change without notice.

# TIMING SPECIFICATIONS ($C_L$ = 20 pF, AVDD = DVDD = DRVDD = 3.0 V, $f_{CLI}$ = 27 MHz, unless otherwise noted.)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| MASTER CLOCK, CLI (Figure 4) | | | | | |
|     CLI Clock Period | $t_{CONV}$ | 37 | | | ns |
|     CLI High/Low Pulsewidth | | 14.8 | 18.5 | 21.8 | ns |
|     Delay from CLI Rising Edge to Internal Pixel Position 0 | $t_{CLIDLY}$ | | 6 | | ns |
| AFE CLPOB Pulsewidth[1,2] (Figures 9 and 14) | | 2 | 20 | | Pixels |
| AFE SAMPLE LOCATION[1] (Figure 7) | | | | | |
|     SHP Sample Edge to SHD Sample Edge | $t_{S1}$ | 17 | 18.5 | | ns |
| DATA OUTPUTS (Figures 8a and 8b) | | | | | |
|     Output Delay from DCLK Rising Edge[1] | $t_{OD}$ | | 8 | | ns |
|     Pipeline Delay from SHP/SHD Sampling to DOUT | | | 11 | | Cycles |
| SERIAL INTERFACE (Figures 40a and 40b) | | | | | |
|     Maximum SCK Frequency | $f_{SCLK}$ | 10 | | | MHz |
|     SL to SCK Setup Time | $t_{LS}$ | 10 | | | ns |
|     SCK to SL Hold Time | $t_{LH}$ | 10 | | | ns |
|     SDATA Valid to SCK Rising Edge Setup | $t_{DS}$ | 10 | | | ns |
|     SCK Falling Edge to SDATA Valid Hold | $t_{DH}$ | 10 | | | ns |
|     SCK Falling Edge to SDATA Valid Read | $t_{DV}$ | 10 | | | ns |

NOTES

[1]Parameter is programmable.

[2]Minimum CLPOB pulsewidth is for functional operation only. Wider typical pulses are recommended to achieve good clamp performance.

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS*

| Parameter | With Respect To | Min | Max | Unit |
|---|---|---|---|---|
| AVDD | AVSS | −0.3 | +3.9 | V |
| TCVDD | TCVSS | −0.3 | +3.9 | V |
| HVDD | HVSS | −0.3 | +3.9 | V |
| RGVDD | RGVSS | −0.3 | +3.9 | V |
| DVDD | DVSS | −0.3 | +3.9 | V |
| DRVDD | DRVSS | −0.3 | +3.9 | V |
| RG Output | RGVSS | −0.3 | RGVDD + 0.3 | V |
| H1–H4 Output | HVSS | −0.3 | HVDD + 0.3 | V |
| Digital Outputs | DVSS | −0.3 | DVDD + 0.3 | V |
| Digital Inputs | DVSS | −0.3 | DVDD + 0.3 | V |
| SCK, SL, SDATA | DVSS | −0.3 | DVDD + 0.3 | V |
| REFT, REFB, CCDIN | AVSS | −0.3 | AVDD + 0.3 | V |
| Junction Temperature | | | 150 | °C |
| Lead Temperature, 10 sec | | | 350 | °C |

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to GND.

## PACKAGE THERMAL CHARACTERISTICS

**Thermal Resistance**

$\theta_{JA}$ = 25°C/W*

*$\theta_{JA}$ is measured using a 4-layer PCB with the exposed paddle soldered to the board.

### ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD9991KCP | −20°C to +85°C | LFCSP | CP-56 |
| AD9991KCPRL | −20°C to +85°C | LFCSP | CP-56 |

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9991 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



WARNING!

ESD SENSITIVE DEVICE

# AD9991

## PIN CONFIGURATION
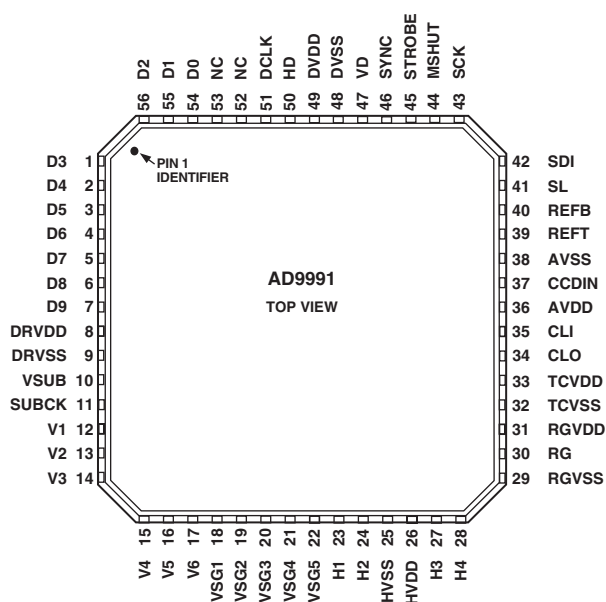


## PIN FUNCTION DESCRIPTIONS[1]

| Pin | Mnemonic | Type[2] | Description |
|-----|----------|---------|-------------|
| 1 | D3 | DO | Data Output |
| 2 | D4 | DO | Data Output |
| 3 | D5 | DO | Data Output |
| 4 | D6 | DO | Data Output |
| 5 | D7 | DO | Data Output |
| 6 | D8 | DO | Data Output |
| 7 | D9 | DO | Data Output (MSB) |
| 8 | DRVDD | P | Data Output Driver Supply |
| 9 | DRVSS | P | Data Output Driver Ground |
| 10 | VSUB | DO | CCD Substrate Bias |
| 11 | SUBCK | DO | CCD Substrate Clock (E-Shutter) |
| 12 | V1 | DO | CCD Vertical Transfer Clock 1 |
| 13 | V2 | DO | CCD Vertical Transfer Clock 2 |
| 14 | V3 | DO | CCD Vertical Transfer Clock 3 |
| 15 | V4 | DO | CCD Vertical Transfer Clock 4 |
| 16 | V5 | DO | CCD Vertical Transfer Clock 5 |
| 17 | V6 | DO | CCD Vertical Transfer Clock 6 |
| 18 | VSG1 | DO | CCD Sensor Gate Pulse 1 |
| 19 | VSG2 | DO | CCD Sensor Gate Pulse 2 |
| 20 | VSG3 | DO | CCD Sensor Gate Pulse 3 |
| 21 | VSG4 | DO | CCD Sensor Gate Pulse 4 |
| 22 | VSG5 | DO | CCD Sensor Gate Pulse 5 |
| 23 | H1 | DO | CCD Horizontal Clock 1 |
| 24 | H2 | DO | CCD Horizontal Clock 2 |
| 25 | HVSS | P | H1–H4 Driver Ground |
| 26 | HVDD | P | H1–H4 Driver Supply |
| 27 | H3 | DO | CCD Horizontal Clock 3 |
| 28 | H4 | DO | CCD Horizontal Clock 4 |
| 29 | RGVSS | P | RG Driver Ground |
| 30 | RG | DO | CCD Reset Gate Clock |
| 31 | RGVDD | P | RG Driver Supply |
| 32 | TCVSS | P | Analog Ground for Timing Core |
| 33 | TCVDD | P | Analog Supply for Timing Core |
| 34 | CLO | DO | Clock Output for Crystal |
| 35 | CLI | DI | Reference Clock Input |
| 36 | AVDD | P | Analog Supply for AFE |
| 37 | CCDIN | AI | CCD Signal Input |
| 38 | AVSS | P | Analog Ground for AFE |
| 39 | REFT | AO | Voltage Reference Top Bypass |
| 40 | REFB | AO | Voltage Reference Bottom Bypass |
| 41 | SL | DI | 3-Wire Serial Load Pulse |
| 42 | SDI | DI | 3-Wire Serial Data Input |
| 43 | SCK | DI | 3-Wire Serial Clock |
| 44 | MSHUT | DO | Mechanical Shutter Pulse |
| 45 | STROBE | DO | Strobe Pulse |
| 46 | SYNC | DI | External System Sync Input |
| 47 | VD | DIO | Vertical Sync Pulse (Input for Slave Mode, Output for Master Mode) |
| 48 | DVSS | P | Digital Ground |
| 49 | DVDD | P | Power Supply for VSG, V1–V6, HD/VD, MSHUT, STROBE, SYNC, and Serial Interface |
| 50 | HD | DIO | Horizontal Sync Pulse (Input for Slave Mode, Output for Master Mode) |
| 51 | DCLK | DO | Data Clock Output |
| 52 | NC | | Not Internally Connected |
| 53 | NC | | Not Internally Connected |
| 54 | D0 | DO | Data Output (LSB) |
| 55 | D1 | DO | Data Output |
| 56 | D2 | DO | Data Output |

NOTES
[1]See Figure 38 for circuit configuration.
[2]AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, DIO = Digital Input/Output, P = Power.

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## TERMINOLOGY

**Differential Nonlinearity (DNL)**
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Thus every code must have a finite width. No missing codes guaranteed to 10-bit resolution indicates that all 1024 codes must be present over all operating conditions.

**Peak Nonlinearity**
Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the output of the AD9991 from a true straight line. The point used as zero scale occurs 0.5 LSB before the first code transition. Positive full scale is defined as a level 1.5 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line. The error is then expressed as a percent-age of the 2 V ADC full-scale signal. The input signal is always appropriately gained up to fill the ADC's full-scale range.
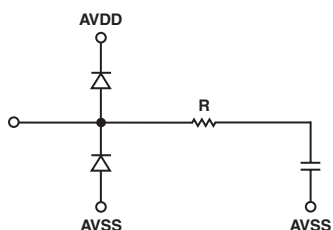
**Total Output Noise**
The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage using the relationship 1 LSB = (ADC Full Scale/$2^n$ codes), where n is the bit resolution of the ADC. For the AD9991, 1 LSB is 1.95 mV.

**Power Supply Rejection (PSR)**
The PSR is measured with a step change applied to the supply pins. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

## EQUIVALENT CIRCUITS



Circuit 1. CCDIN
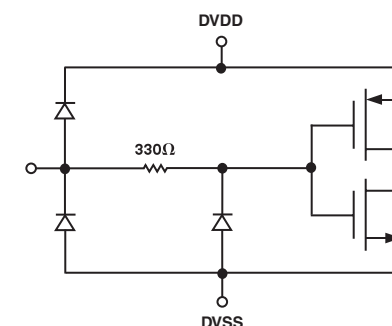


Circuit 3. Digital Inputs



Circuit 2. Digital Data Outputs



Circuit 4. H1–H4, RG Drivers

# AD9991–Typical Performance Characteristics



TPC 1. Power Dissipation vs. Sample Rate



TPC 3. Output Noise vs. VGA Gain



TPC 2. Typical DNL Performance

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## SYSTEM OVERVIEW

Figure 1 shows the typical system block diagram for the AD9991 used in Master mode. The CCD output is processed by the AD9991's AFE circuitry, which c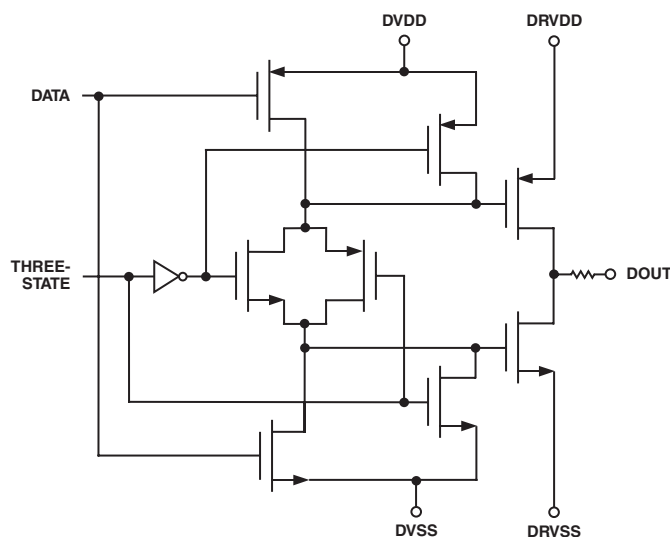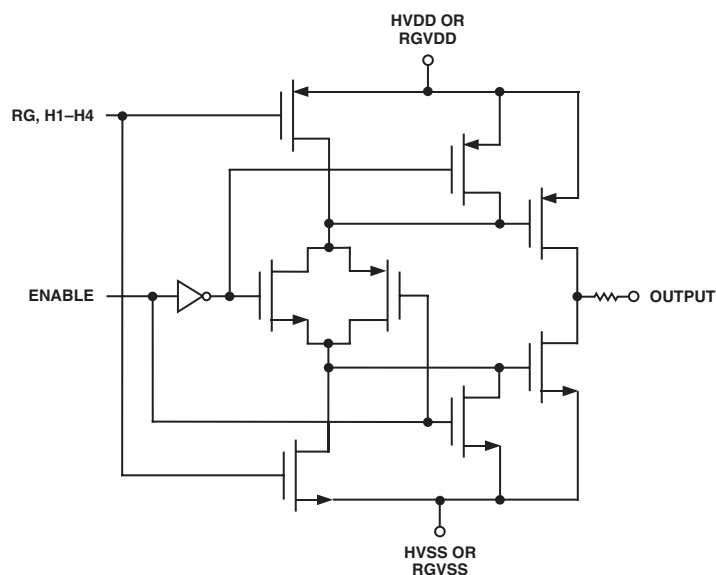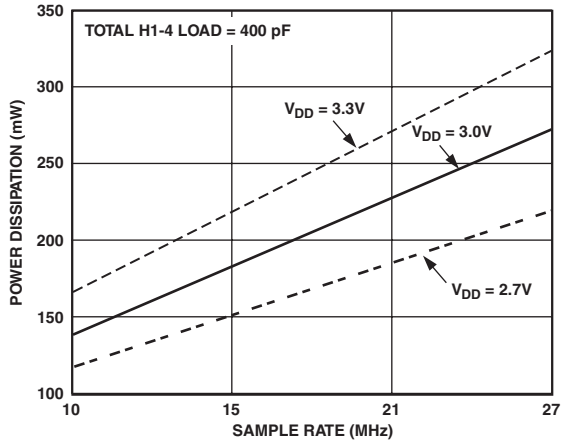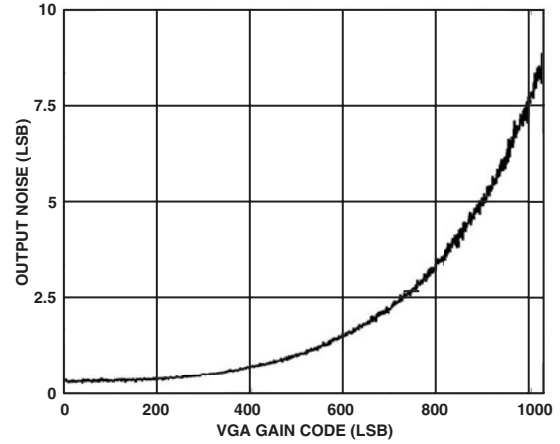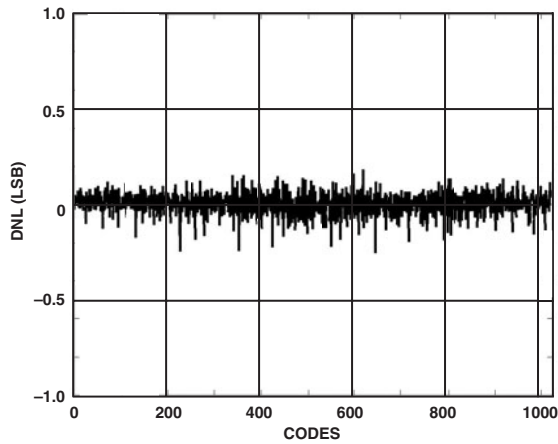onsists of a CDS, VGA, black level clamp, and A/D converter. The digitized pixel information is sent to the digital image processor chip, which performs the postprocessing and compression. To operate the CCD, all CCD timing parameters are programmed into the AD9991 from the system microprocessor through the 3-wire serial interface. From the system master clock, CLI, provided by the image processor or external crystal, the AD9991 generates all of the CCD's horizontal and vertical clocks and all internal AFE clocks. External synchronization is provided by a SYNC pulse from the microprocessor, which will reset internal counters and resync the VD and HD outputs.

Alternatively, the AD9991 may be operated in Slave mode, in which VD and HD are provided externally from the image processor. In this mode, all AD9991 timing will be synchronized with VD and HD.

The H-drivers for H1–H4 and RG are included in the AD9991, allowing these clocks to be directly connected to the CCD. H-drive voltage of up to 3.3 V is supported. An external V-driver is required for the vertical transfer clocks, the sensor gate pulses, and the substrate clock.

The AD9991 also includes programmable MSHUT and STROBE outputs, which may be used to trigger mechanical shutter and strobe (flash) circuitry.

Figures 2 and 3 show the maximum horizontal and vertical counter dimensions for the AD9991. All internal horizontal and vertical clocking is controlled by these counters to specify line and pixel locations. Maximum HD length is 4095 pixels per line, and maximum VD length is 4095 lines per field.
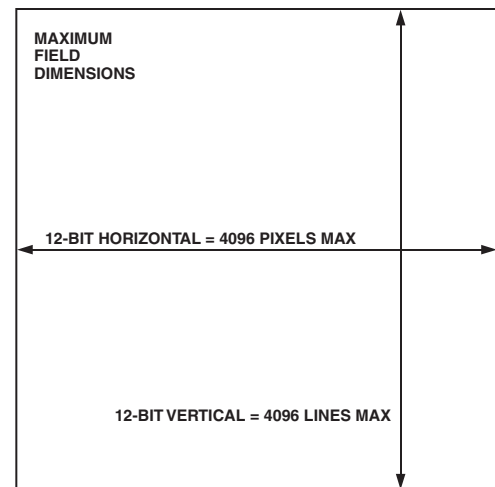


Figure 2. Vertical and Horizontal Counters



Figure 1. Typical System Block Diagram, Master Mode
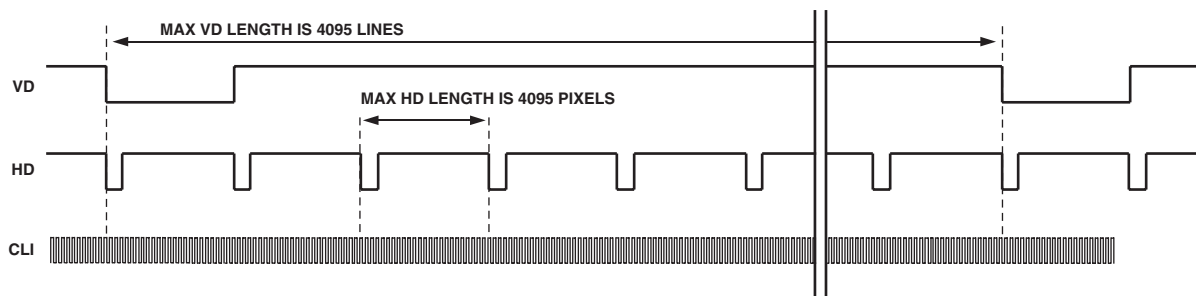


Figure 3. Maximum VD/HD Dimensions

# AD9991

**PRECISION TIMING HIGH SPEED TIMING GENERATION**
The AD9991 generates high speed timing signals using the flexible Precision Timing core. This core is the foundation for generating the timing used for both the CCD and the AFE: the reset gate RG, horizontal drivers H1–H4, and the SHP/SHD sample clocks. A unique architecture makes it routine for the system designer to optimize image quality by providing precise control over the horizontal CCD readout and the AFE correlated double sampling.

The high speed timing of the AD9991 operates the same in either Master or Slave mode configuration. For more information on synchronization and pipeline delays, see the Power-Up and Synchronization section.

**Timing Resolution**
The Precision Timing core uses a 1× master clock input (CLI) as a reference. This clock should be the same as the CCD pixel clock frequency. Figure 4 illustrates how the internal timing core divides the master clock period into 48 steps or edge positions. Using a 20 MHz CLI frequency, the edge resolution of the Precision Timing core is 1 ns. If a 1× system clock is not available, it is also possible to use a 2× reference clock by programming the

CLIDIVIDE register (Addr 0x30). The AD9991 will then internally divide the CLI frequency by 2.

The AD9991 also includes a master clock output, CLO, which is the inverse of CLI. This output is intended to be used as a crystal driver. A crystal can be placed between the CLI and CLO pins to generate the master clock for the AD9991. For more information on using a crystal, see Figure 39.

**High Speed Clock Programmability**
Figure 5 shows how the high speed clocks RG, H1–H4, SHP, and SHD are generated. The RG pulse has programmable rising and falling edges, and may be inverted using the polarity control. The horizontal clocks H1 and H3 have programmable rising and falling edges and polarity control. The H2 and H4 clocks are always inverses of H1 and H3, respectively. Table I summarizes the high speed timing registers and their parameters. Figure 6 shows the typical 2-phase H-clock arrangement in which H3 and H4 are programmed for the same edge location as H1 and H2.

The edge location registers are six bits wide, but there are only 48 valid edge locations available. Therefore, the register values are mapped into four quadrants, with each quadrant containing
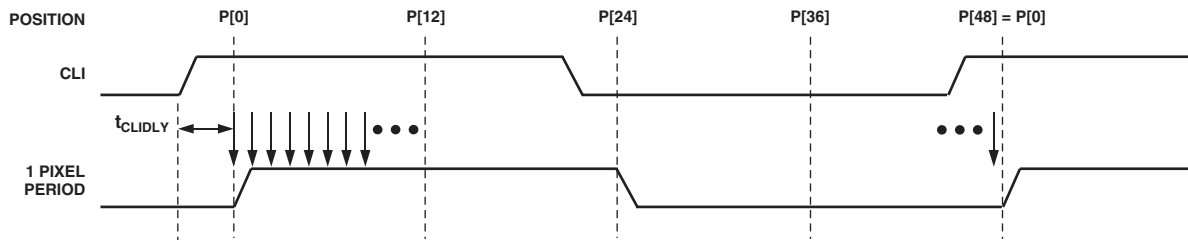


NOTES
PIXEL CLOCK PERIOD IS DIVIDED INTO 48 POSITIONS, PROVIDING FINE EDGE RESOLUTION FOR HIGH SPEED CLOCKS.
THERE IS A FIXED DELAY FROM THE CLI INPUT TO THE INTERNAL PIXEL PERIOD POSITIONS ($t_{CLIDLY}$ = 6ns TYP).

*Figure 4. High Speed Clock Resolution from CLI Master Clock Input*
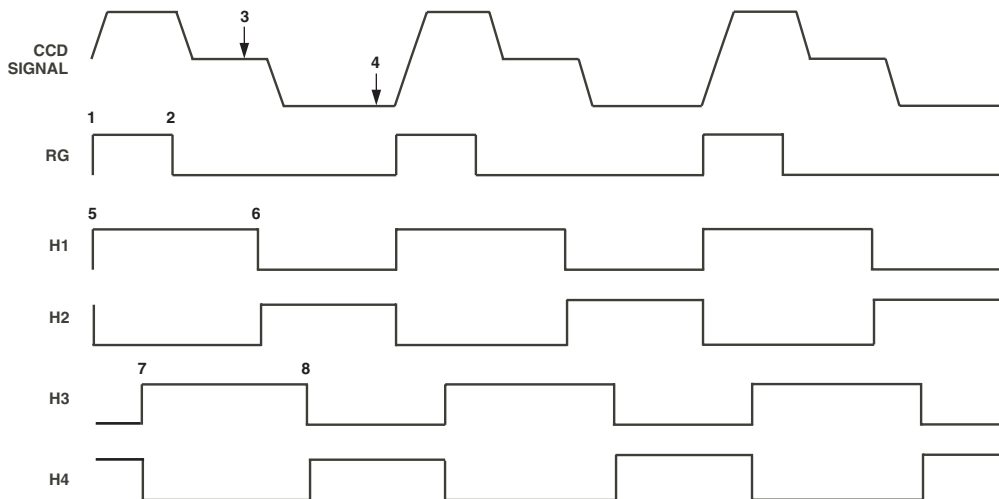


PROGRAMMABLE CLOCK POSITIONS:
1. RG RISING EDGE
2. RG FALLING EDGE
3. SHP SAMPLE LOCATION
4. SHD SAMPLE LOCATION
5. H1 RISING EDGE POSITION
6. H1 FALLING EDGE POSITION (H2 IS INVERSE OF H1)
7. H3 RISING EDGE POSITION
8. H3 FALLING EDGE POSITION (H4 IS INVERSE OF H3)

*Figure 5. High Speed Clock Programmable Locations*

12 edge locations. Table II shows the correct register values for the corresponding edge locations.

Figure 7 shows the default timing locations for all of the high speed clock signals.

**H-Driver and RG Outputs**
In addition to the programmable timing positions, the AD9991 features on-chip output drivers for the RG and H1–H4 outputs. These drivers are powerful enough to directly drive the CCD inputs. The H-driver and RG current can be adjusted for optimum rise/fall time into a particular load by using the DRVCONTROL register (Addr 0x35). The 3-bit drive setting for each output is adjustable in 4.1 mA increments, with the minimum setting of 0 equal to OFF or three-state, and the maximum setting of 7 equal to 30.1 mA.

As shown in Figures 5, 6, and 7, the H2 and H4 outputs are inverses of H1 and H3, respectively. The H1/H2 crossover voltage is approximately 50% of the output swing. The crossover voltage is not programmable.

**Digital Data Outputs**
The AD9991 data output and DCLK phases are programmable using the DOUTPHASE register (Addr 0x37, Bits [5:0]). Any edge from 0 to 47 may be programmed, as shown in Figure 8a. Normally, the DOUT and DCLK signals will track in phase based on the DOUTPHASE register contents. The DCLK output phase can also be held fixed with respect to the data outputs by changing the DCLKMODE register HIGH (Addr 0x37, Bit 6). In this mode, the DCLK output will remain at a fixed phase equal to CLO (the inverse of CLI) while the data output phase is still programmable.

There is a fixed output delay from the DCLK rising edge to the DOUT transition, called $t_{OD}$. This delay can be programmed to four values between 0 ns and 12 ns, by using the DOUTDELAY register (Addr 0x037, Bits [8:7]). The default value is 8 ns.

The pipeline delay through the AD9991 is shown in Figure 8b. After the CCD input is sampled by SHD, there is an 11-cycle delay until the data is available.

**Table I. Timing Core Register Parameters for H1, H3, RG, SHP/SHD**

| Parameter | Length | Range | Description |
|---|---|---|---|
| Polarity | 1b | High/Low | Polarity Control for H1, H3, and RG (0 = No Inversion, 1 = Inversion) |
| Positive Edge | 6b | 0–47 Edge Location | Positive Edge Location for H1, H3, and RG |
| Negative Edge | 6b | 0–47 Edge Location | Negative Edge Location for H1, H3, and RG |
| Sampling Location | 6b | 0-47 Edge Location | Sampling Location for Internal SHP and SHD Signals |
| Drive Strength | 3b | 0–47 Current Steps | Drive Current for H1–H4 and RG Outputs (4.1 mA per Step) |
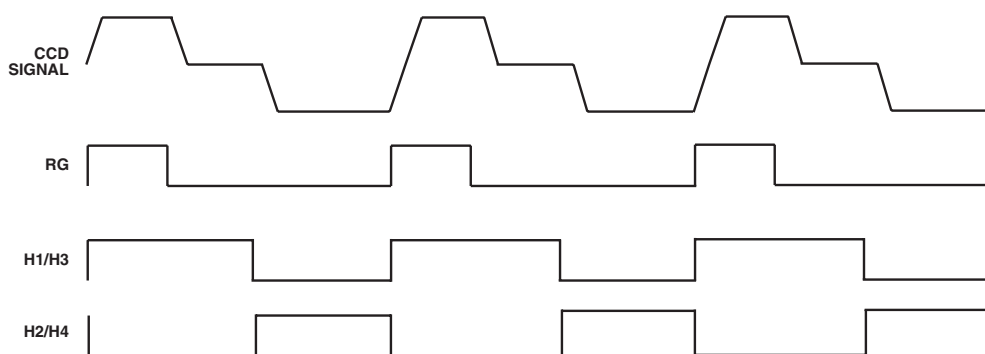


USING THE SAME TOGGLE POSITIONS FOR H1 AND H3 GENERATES STANDARD 2-PHASE H-CLOCKING.

Figure 6. 2-Phase H-Clock Operation

**Table II. Precision Timing Edge Locations**

| Quadrant | Edge Location (Dec) | Register Value (Dec) | Register Value (Bin) |
|---|---|---|---|
| I | 0 to 11 | 0 to 11 | 000000 to 001011 |
| II | 12 to 23 | 16 to 27 | 010000 to 011011 |
| III | 24 to 35 | 32 to 43 | 100000 to 101011 |
| IV | 36 to 47 | 48 to 59 | 110000 to 111011 |

# AD9991
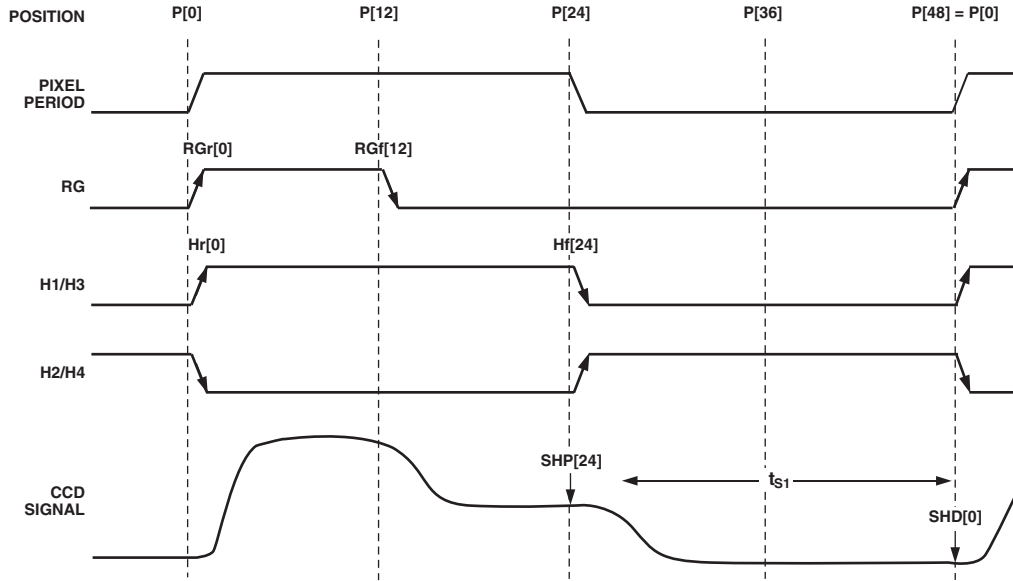


NOTES
ALL SIGNAL EDGES ARE FULLY PROGRAMMABLE TO ANY OF THE 48 POSITIONS WITHIN ONE PIXEL PERIOD.
DEFAULT POSITIONS FOR EACH SIGNAL ARE SHOWN.

*Figure 7. High Speed Timing Default Locations*
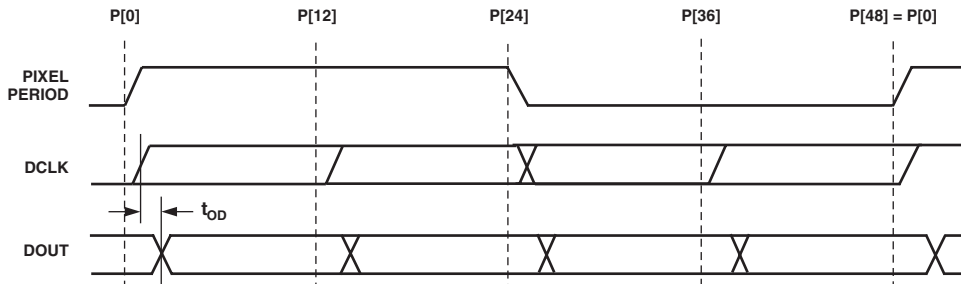


NOTES
DATA OUTPUT (DOUT) AND DCLK PHASE ARE ADJUSTABLE WITH RESPECT TO THE PIXEL PERIOD.
WITHIN ONE CLOCK PERIOD, THE DATA TRANSITION CAN BE PROGRAMMED TO 48 DIFFERENT LOCATIONS.
OUTPUT DELAY ($t_{OD}$) FROM DCLK RISING EDGE TO DOUT RISING EDGE IS PROGRAMMABLE.

*Figure 8a. Digital Output Phase Adjustment*
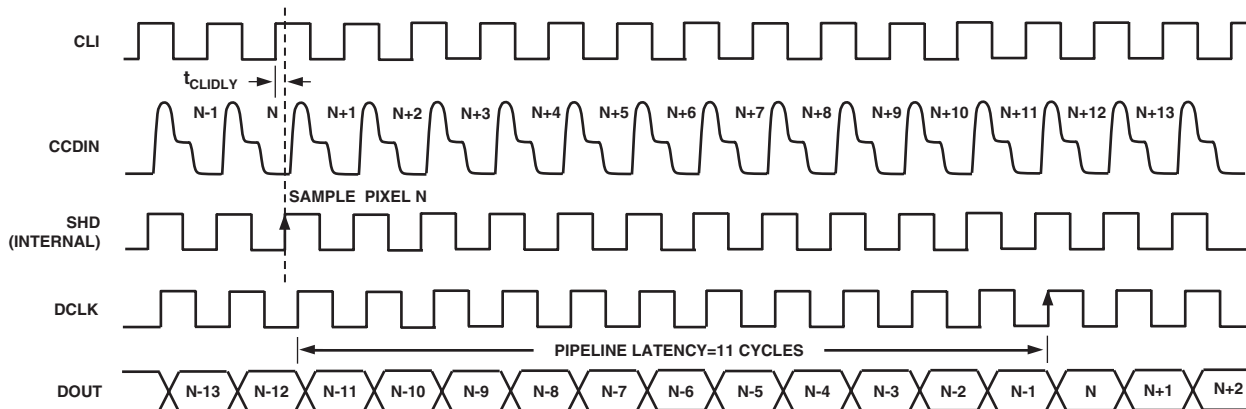


NOTES
DEFAULT TIMING VALUES ARE SHOWN: SHDLOC = 0, DOUT PHASE = 0, DCLKMODE = 0.
HIGHER VALUES OF SHD AND/OR DOUTPHASE WILL SHIFT DOUT TRANSITION TO THE RIGHT, WITH RESPECT TO CLI LOCATION.

*Figure 8b. Pipeline Delay*

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## HORIZONTAL CLAMPING AND BLANKING

The AD9991's horizontal clamping and blanking pulses are fully programmable to suit a variety of applications. Individual control is provided for CLPOB, PBLK, and HBLK during the different regions of each field. This allows the dark pixel clamping and blanking patterns to be changed at each stage of the readout in order to accommodate different image transfer timing and high speed line shifts.

### Individual CLPOB and PBLK Patterns

The AFE horizontal timing consists of CLPOB and PBLK, as shown in Figure 9. These two signals are independently programmed using the registers in Table III. SPOL is the start polarity for the signal, and TOG1 and TOG2 are the first and second toggle positions of the pulse. Both signals are active low and should be programmed accordingly.

A separate pattern for CLPOB and PBLK may be programmed for each 10 V-sequence. As described in the Vertical Timing Generation section, up to 10 separate V-sequences can be created,

each containing a unique pulse pattern for CLPOB and PBLK. Figure 9 shows how the sequence change positions divide the readout field into different regions. A different V-Sequence can be assigned to each region, allowing the CLPOB and PBLK signals to be changed accordingly with each change in the vertical timing.

### Individual HBLK Patterns

The HBLK programmable timing shown in Figure 10 is similar to CLPOB and PBLK. However, there is no start polarity control. Only the toggle positions are used to designate the start and stop positions of the blanking period. Additionally, there is a polarity control HBLKMASK that designates the polarity of the horizontal clock signals H1–H4 during the blanking period. Setting HBLKMASK high will set H1 = H3 = Low and H2 = H4 = High during the blanking, as shown in Figure 11. As with the CLPOB and PBLK signals, HBLK registers are available in each V-sequence, allowing different blanking signals to be used with different vertical timing sequences.



NOTES
PROGRAMMABLE SETTINGS:
(1) START POLARITY (CLAMP AND BLANK REGION ARE ACTIVE LOW)
(2) FIRST TOGGLE POSITION
(3) SECOND TOGGLE POSITION
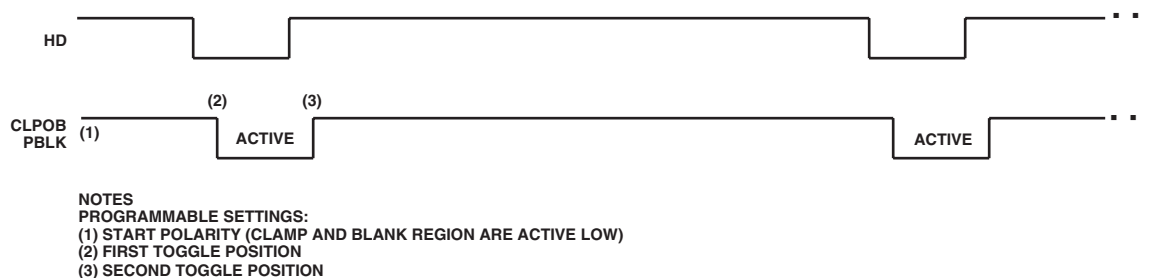
*Figure 9. Clamp and Pre-Blank Pulse Placement*

**Table III. CLPOB and PBLK Pattern Registers**

| Register | Length | Range | Description |
|---|---|---|---|
| SPOL | 1b | High/Low | Starting Polarity of CLPOB/PBLK for V-Sequence 0–9 |
| TOG1 | 12b | 0–4095 Pixel Location | First Toggle Position within Line for V-Sequence 0–9 |
| TOG2 | 12b | 0–4095 Pixel Location | Second Toggle Position within Line for V-Sequence 0–9 |

**Table IV. HBLK Pattern Registers**

| Register | Length | Range | Description |
|---|---|---|---|
| HBLKMASK | 1b | High/Low | Masking Polarity for H1/H3 (0 = H1/H3 Low, 1 = H1/H3 High) |
| HBLKALT | 2b | 0–3 Alternation Mode | Enables Odd/Even Alternation of HBLK Toggle Positions 0 = Disable Alternation. 1 = TOG1–TOG2 Odd, TOG3–TOG6 Even. 2 = 3 = TOG1–TOG2 Even, TOG3–TOG6 Odd |
| HBLKTOG1 | 12b | 0–4095 Pixel Location | First Toggle Position within Line for Each V-Sequence 0–9 |
| HBLKTOG2 | 12b | 0–4095 Pixel Location | Second Toggle Position within Line for Each V-Sequence 0–9 |
| HBLKTOG3 | 12b | 0–4095 Pixel Location | Third Toggle Position within Line for Each V-Sequence 0–9 |
| HBLKTOG4 | 12b | 0–4095 Pixel Location | Fourth Toggle Position within Line for Each V-Sequence 0–9 |
| HBLKTOG5 | 12b | 0–4095 Pixel Location | Fifth Toggle Position within Line for Each V-Sequence 0–9 |
| HBLKTOG6 | 12b | 0–4095 Pixel Location | Sixth Toggle Position within Line for Each V-Sequence 0–9 |

# AD9991

**Generating Special HBLK Patterns**

There are six toggle positions available for HBLK. Normally, only two of the toggle positions are used to generate the standard HBLK interval. However, the additional toggle positions may be used to generate special HBLK patterns, as shown in Figure 12. The pattern in this example uses all six toggle positions to generate two extra groups of pulses during the HBLK interval. By changing the toggle positions, different patterns can be created.

**Generating HBLK Line Alternation**

One further feature of the AD9991 is the ability to alternate different HBLK toggle positions on odd and even lines. This may be used in conjunction with V-pattern odd/even alternation or on its own. When a 1 is written to the HBLKALT register, TOG1 and TOG2 are used on odd lines only, while TOG3–TOG6 are used on even lines. Writing a 2 to the HBLKALT register gives the opposite result: TOG1 and TOG2 are used on even lines, while TOG3–TOG6 are used on odd lines. See the Vertical Timing Generation, Line Alternation section for more information.



PROGRAMMABLE SETTINGS:
1. FIRST TOGGLE POSITION = START OF BLANKING
2. SECOND TOGGLE POSITION = END OF BLANKING
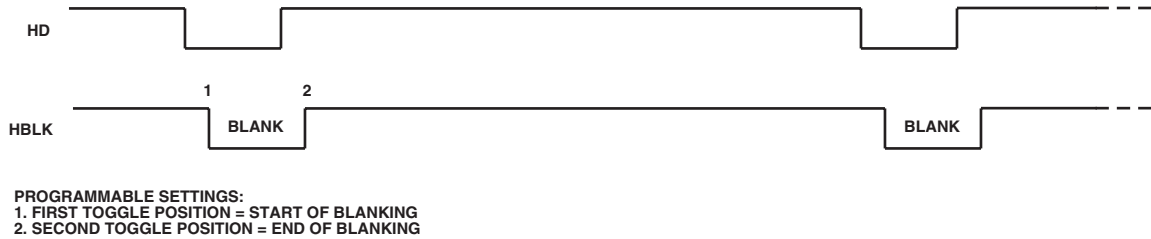
*Figure 10. Horizontal Blanking (HBLK) Pulse Placement*



THE POLARITY OF H1 DURING BLANKING IS PROGRAMMABLE (H2 IS OPPOSITE POLARITY OF H1).
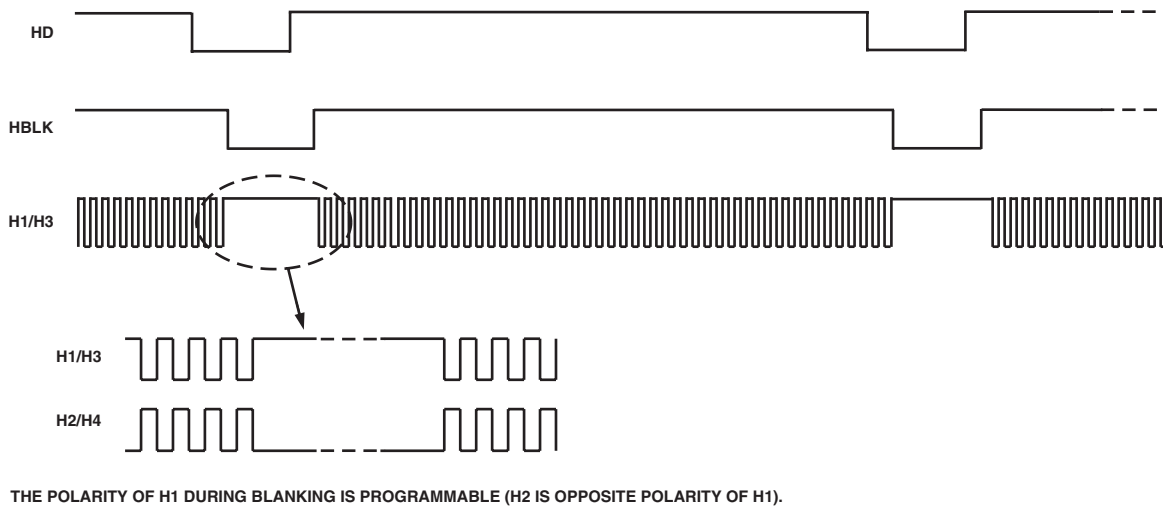
*Figure 11. HBLK Masking Control*



SPECIAL H-BLANK PATTERN IS CREATED USING MULTIPLE HBLK TOGGLE POSITIONS
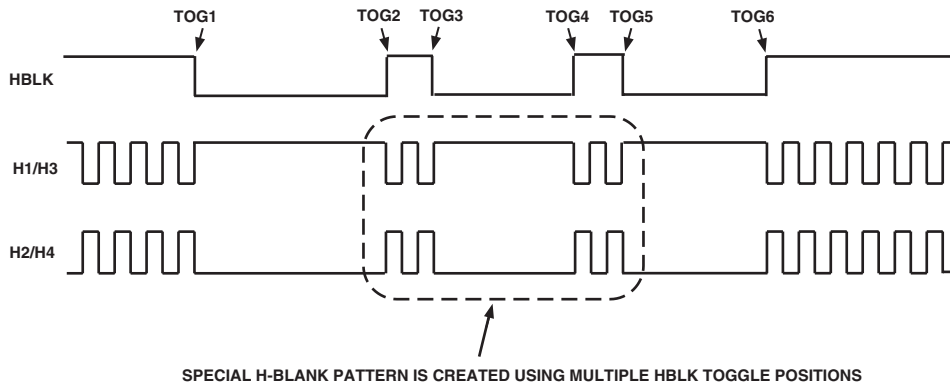
*Figure 12. Generating Special HBLK Patterns*

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## HORIZONTAL TIMING SEQUENCE EXAMPLE

Figure 13 shows an example CCD layout. The horizontal register contains 28 dummy pixels, which will occur on each line clocked from the CCD. In the vertical direction, there are 10 optical black (OB) lines at the front of the readout and two at the back of the readout. The horizontal direction has four OB pixels in the front and 48 in the back.

Figure 14 shows the basic sequence layout, to be used during the effective pixel readout. The 48 OB pixels at the end of each line are used for the CLPOB signals. PBLK is optional and is often used to blank the digital outputs during the noneffective CCD pixels. HBLK is used during the vertical shift interval.

The HBLK, CLPOB, and PBLK parameters are programmed in the V-sequence registers.

More elaborate clamping schemes may be used, such as adding in a separate sequence to clamp during the entire shield OB lines. This requires configuring a separate V-sequence for reading out the OB lines.
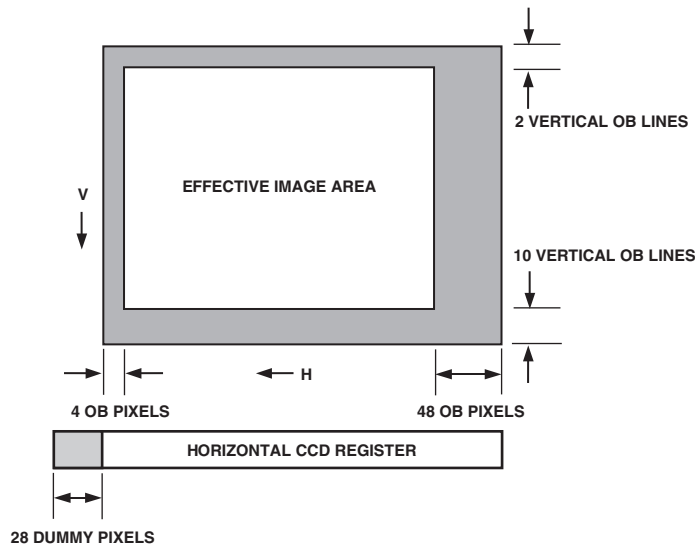
Figure 13. Example CCD Configuration
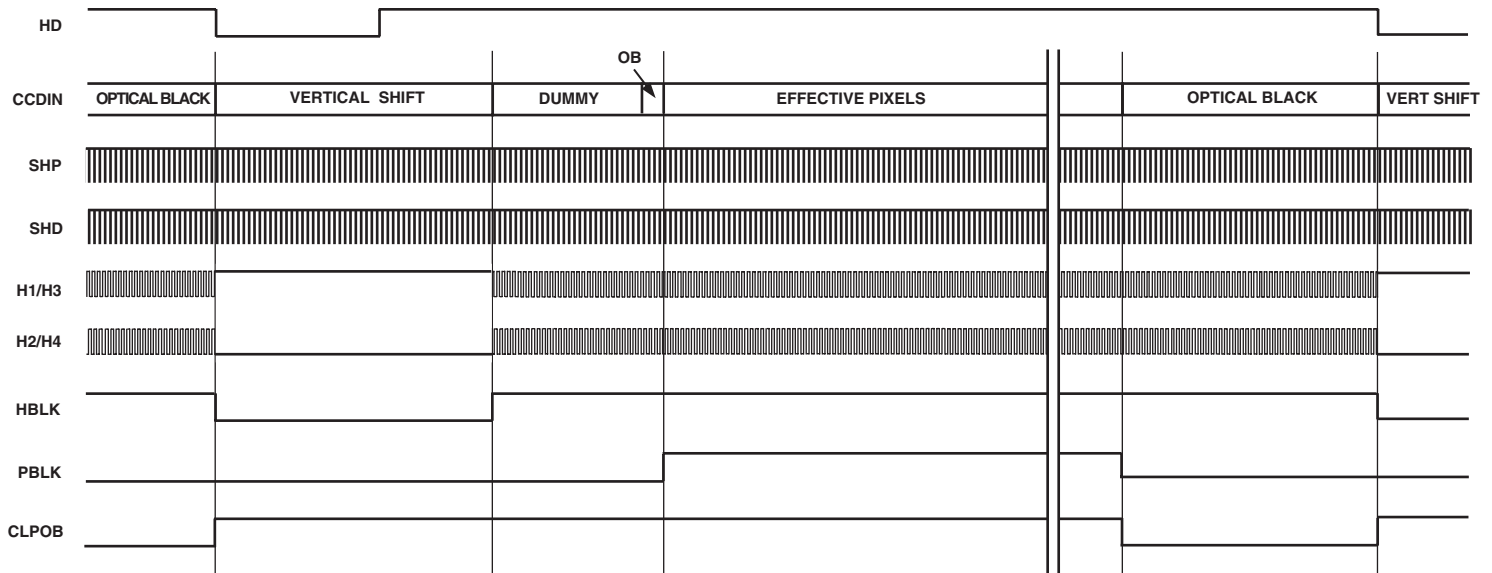
Figure 14. Horizontal Sequence Example

# AD9991

## VERTICAL TIMING GENERATION

The AD9991 provides a very flexible solution for generating vertical CCD timing, and can support multiple CCDs and different system architectures. The 6-phase vertical transfer clocks V1–V6 are used to shift each line of pixels into the horizontal output register of the CCD. The AD9991 allows these outputs to be individually programmed into various readout configurations using a four step process.

Figure 15 shows an overview of how the vertical timing is generated in four steps. First, the individual pulse patterns for V1–V6

are created by using the vertical pattern group registers. Second, the V-pattern groups are used to build the sequences, where additional information is added. Third, the readout for an entire field is constructed by dividing the field into different regions and then assigning a sequence to each region. Each field can contain up to seven different regions to accommodate different steps of the readout such as high speed line shifts and unique vertical line transfers. Up to six different fields may be created. Finally, the Mode register allows the different fields to be combined into any order for various readout configurations.
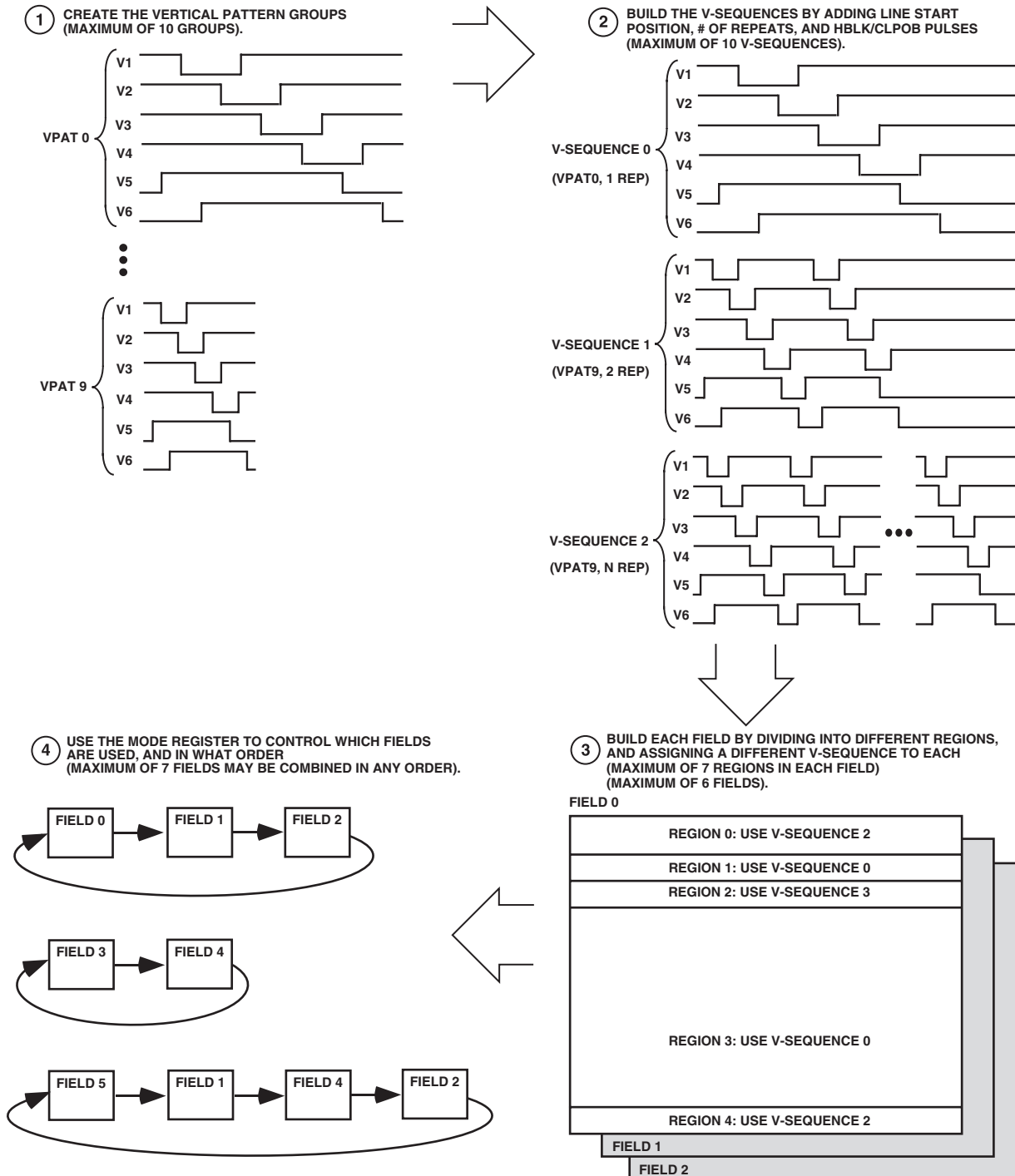


Figure 15. Summary of Vertical Timing Generation

## Vertical Pattern Groups (VPAT)

The vertical pattern groups define the individual pulse patterns for each V1–V6 output signal. Table V summarizes the registers available for generating each of the 10 V-pattern groups. The start polarity (VPOL) determines the starting polarity of the vertical sequence, and can be programmed high or low for each V1–V6 output. The first, second, and third toggle position (VTOG1, VTOG2, VTOG3) are the pixel locations within the line where the pulse transitions. A fourth toggle position (VTOG4) is also available for V-Pattern Groups 8 and 9. All toggle positions are 12-bit values, allowing their placement anywhere in the horizontal line. A separate register, VPATSTART, specifies the start position of the V-pattern group within the line (see the Vertical Sequences section). The VPATLEN register designates the total length of the V-pattern group, which will determine the number of pixels between each of the pattern repetitions, when repetitions are used (see the Vertical Sequences section).

The FREEZE and RESUME registers are used to temporarily stop the operation of the V1–V6 outputs. At the pixel location specified in the FREEZE register, the V1–V6 outputs will be held static at their current dc state, high or low. The V1–V6 outputs are held until the pixel location specified by RESUME register. Two sets of FREEZE/RESUME registers are provided, allowing the vertical outputs to be interrupted twice in the same line. The FREEZE and RESUME positions are programmed in the V-pattern group registers, but are separately enabled using the VMASK registers, which are described in the Vertical Sequence section.

**Table V. Vertical Pattern Group Registers**

| Register | Length | Range | Description |
|---|---|---|---|
| VPOL | 1b | High/Low | Starting Polarity of Each V1–V6 Output |
| VTOG1 | 12b | 0–4096 Pixel Location | First Toggle Position within Line for Each V1–V6 Output |
| VTOG2 | 12b | 0–4096 Pixel Location | Second Toggle Position within Line for Each V1–V6 Output |
| VTOG3 | 12b | 0–4096 Pixel Location | Third Toggle Position within Line for Each V1–V6 Output |
| VTOG4 | 12b | 0–4096 Pixel Location | Fourth Toggle Position, only Available in V-Pattern Groups 8 and 9 |
| VPATLEN | 12b | 0–4096 Pixels | Total Length of Each V-Pattern Group |
| FREEZE1 | 12b | 0–4096 Pixel Location | Holds the V1–V6 Outputs at Their Current Levels (Static DC) |
| RESUME1 | 12b | 0–4096 Pixel Location | Resumes Operation of the V1–V6 Outputs to Finish Their Pattern |
| FREEZE2 | 12b | 0–4096 Pixel Location | Holds the V1–V6 Outputs at Their Current Levels (Static DC) |
| RESUME2 | 12b | 0–4096 Pixel Location | Resumes Operation of the V1–V6 Outputs to Finish Their Pattern |



PROGRAMMABLE SETTINGS FOR EACH V-PATTERN:
1. START POLARITY
2. FIRST TOGGLE POSITION
3. SECOND TOGGLE POSITION (THIRD TOGGLE POSITION ALSO AVAILABLE, FOURTH TOGGLE POSITION AVAILABLE FOR V-PATTERN GROUPS 8 AND 9)
4. TOTAL PATTERN LENGTH FOR ALL V1–V6 OUTPUTS
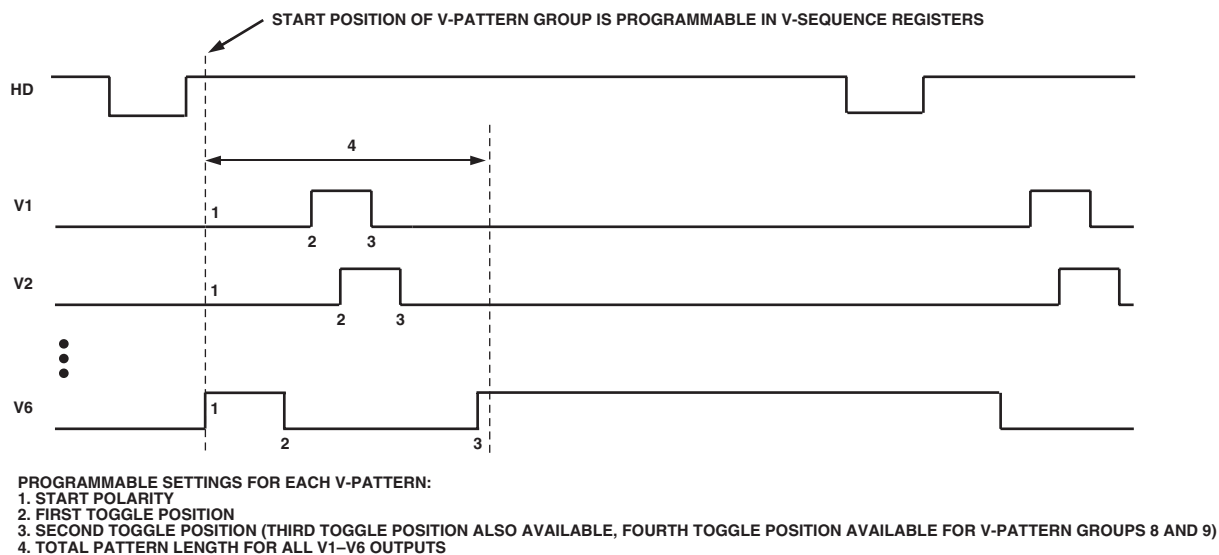
*Figure 16. Vertical Pattern Group Programmability*

# AD9991

## Vertical Sequences (VSEQ)

The vertical sequences are created by selecting one of the 10 V-pattern groups and adding repeats, start position, and horizontal clamping, and blanking information. Up to 10 V-sequences can be programmed, each using the registers shown in Table VI. Figure 17 shows how the different registers are used to generate each V-sequence.

The VPATSEL register selects which V-pattern group will be used in a given V-sequence. The basic V-pattern group can have repetitions added, for high speed line shifts or line binning, by using the VPATREPO and VPATREPE registers. Generally, the same number of repetitions are programmed into both registers, but if a different number of repetitions is required on odd and even lines, separate values may be used for each register (see the V-Sequence Line Alternation section). The VPATSTART register specifies where in the line the V-pattern group will start. The VMASK register is used in conjunction with the FREEZE/RESUME registers to enable optional masking of the V-outputs. Either or both of the FREEZE1/RESUME1 and FREEZE2/RESUME2 registers can be enabled.

The line length (in pixels) is programmable using the HDLEN registers. Each V-sequence can have a different line length to accommodate various image readout techniques. The maximum number of pixels per line is 4096. Note that the last line of the field is separately programmable using the HDLAST register located in the Field register section.

Table VI. V-Sequence Registers (see Tables III and IV for HBLK, CLPOB, PBLK Registers)

| Register | Length | Range | Description |
|---|---|---|---|
| VPATSEL | 4b | 0–9 V-Pattern Group # | Selected V-Pattern Group for Each V-Sequence. |
| VMASK | 2b | 0–3 Mask Mode | Enables the Masking of V1–V6 Outputs at the Locations Specified by the FREEZE/RESUME Registers. 0 = No Mask, 1 = Enable FREEZE1/RESUME1, 2 = Enable FREEZE2/RESUME2, 3 = Enable both 1 and 2. |
| VPATREPO | 12b | 0–4095 # of Repeats | Number of Repetitions for the V-Pattern Group for Odd Lines. If no odd/even alternation is required, set equal to VPATREPE. |
| VPATREPE | 12b | 0–4095 # of Repeats | Number of Repetitions for the V-Pattern Group for Even Lines. If no odd/even alternation is required, set equal to VPATREPO. |
| VPATSTART | 12b | 0–4095 Pixel Location | Start Position for the Selected V-Pattern Group. |
| HDLEN | 12b | 0–4095 # of Pixels | HD Line Length for Lines in Each V-Sequence. |
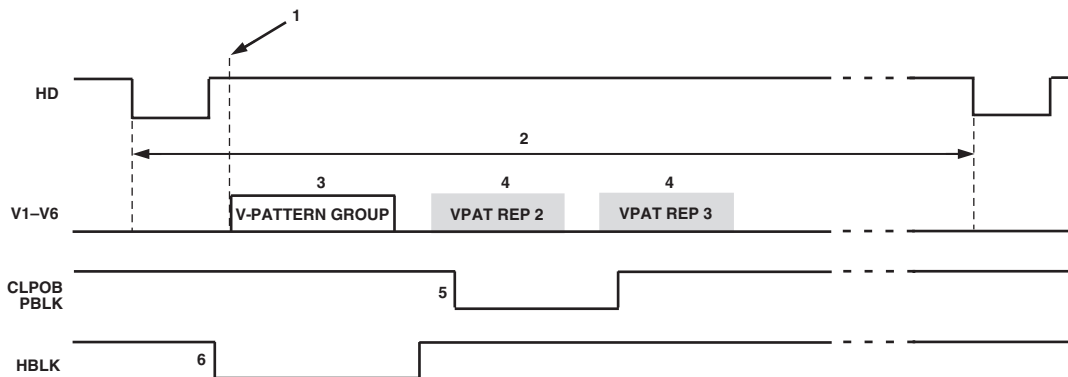


PROGRAMMABLE SETTINGS FOR EACH V-SEQUENCE:
1. START POSITION IN THE LINE OF SELECTED V-PATTERN GROUP
2. HD LINE LENGTH
3. V-PATTERN SELECT (VPATSEL) TO SELECT ANY V-PATTERN GROUP
4. NUMBER OF REPETITIONS OF THE V-PATTERN GROUP (IF NEEDED)
5. START POLARITY AND TOGGLE POSITIONS FOR CLPOB AND PBLK SIGNALS
6. MASKING POLARITY AND TOGGLE POSITIONS FOR HBLK SIGNAL

Figure 17. V-Sequence Programmability

**Complete Field: Combining V-Sequences**

After the V-sequences have been created, they are combined to create different readout fields. A field consists of up to seven different regions, and within each region a different V-sequence can be selected. Figure 18 shows how the sequence change positions (SCP) designate the line boundry for each region, and the VSEQSEL registers then select which V-sequence is used during each region. Registers to control the VSG outputs are also included in the Field registers.

Table VII summarizes the registers used to create the different fields. Up to six different fields can be preprogrammed using all of the Field registers.

The VEQSEL registers, one for each region, select which of the 10 V-sequences will be active during each region. The SWEEP registers are used to enable SWEEP mode during any region. The MULTI registers are used to enable Multiplier mode dur-

ing any region. The SCP registers create the line boundries for each region. The VDLEN register specifies the total number of lines in the field. The total number of pixels per line (HDLEN) is specified in the V-sequence registers, but the HDLAST register specifies the number of pixels in the last line of the field. The VPATSECOND register is used to add a second V-pattern group to the V1–6 outputs during the sensor gate (VSG) line.

The SGMASK register is used to enable or disable each individual VSG output. There is a single bit for each VSG output: setting the bit high will mask the output, setting it low will enable the output. The SGPAT register assigns one of the four different SG patterns to each VSG output. The individual SG patterns are created separately using the SG pattern registers. The SGLINE1 register specifies which line in the field will contain the VSG outputs. The optional SGLINE2 register allows the same VSG pulses to be repeated on a different line.

**Table VII. Field Registers**

| Register | Length | Range | Description |
|---|---|---|---|
| VSEQSEL | 4b | 0–9 V-Sequence # | Selected V-Sequence for Each Region in the Field. |
| SWEEP | 1b | High/Low | Enables Sweep Mode for Each Region, When Set High. |
| MULTI | 1b | High/Low | Enables Multiplier Mode for Each Region, When Set High. |
| SCP | 12b | 0–4095 Line # | Sequence Change Position for Each Region. |
| VDLEN | 12b | 0–4095 # of Lines | Total Number of Lines in Each Field. |
| HDLAST | 12b | 0–4095 # of Pixels | Length in Pixels of the Last HD Line in Each Field. |
| VPATSECOND | 4b | 0–9 V-Pattern Group # | Selected V-Pattern Group for Second Pattern Applied During VSG Line. |
| SGMASK | 6b | High/Low, Each VSG | Set High to Mask Each Individual VSG Output. VSG1 [0], VSG2 [1], VSG3 [2], VSG4 [3], VSG5 [4]. |
| SGPATSEL | 12b | 0–3 Pattern #, Each VSG | Selects the VSG Pattern Number for Each VSG Output. VSG1 [1:0], VSG2 [3:2], VSG3 [5:4], VSG4 [7:6], VSG5 [9:8]. |
| SGLINE1 | 12b | 0–4095 Line # | Selects the Line in the Field where the VSG Are Active. |
| SGLINE2 | 12b | 0–4095 Line # | Selects a Second Line in the Field to Repeat the VSG Signals. |
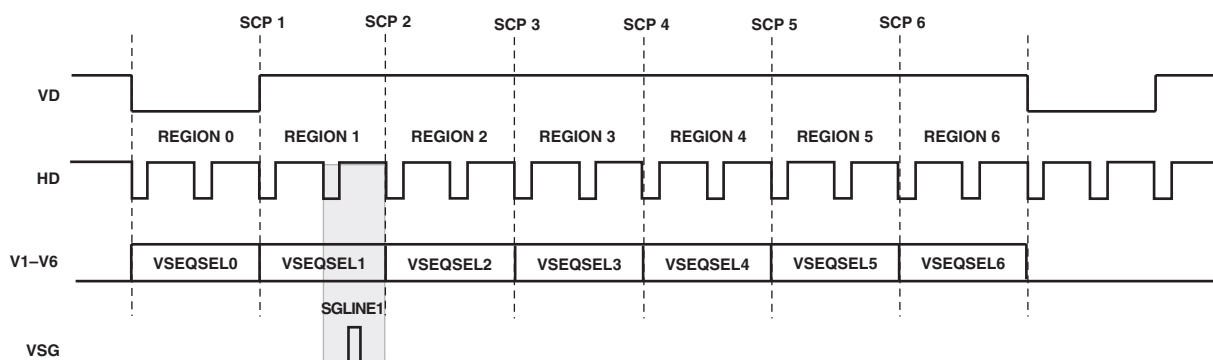


FIELD SETTINGS:
1. SEQUENCE CHANGE POSITIONS (SCP1–6) DEFINE EACH OF THE 7 REGIONS IN THE FIELD.
2. VSEQSEL0–6 SELECTS THE DESIRED V-SEQUENCE (0–9) FOR EACH REGION.
3. SGLINE1 REGISTER SELECTS WHICH HD LINE IN THE FIELD WILL CONTAIN THE SENSOR GATE PULSE(S).

*Figure 18. Complete Field is Divided into Regions*

# AD9991

**Generating Line Alternation for V-Sequence and HBLK**
During low resolution readout, some CCDs require a different number of vertical clocks on alternate lines. The AD9991 can support this by using the VPATREPO and VPATREPE registers. This allows a different number of VPAT repetitions to be programmed on odd and even lines. Note that only the number of repeats can be different in odd and even lines, but the VPAT group remains the same.

Additionally, the HBLK signal can also be alternated for odd and even lines. When the HBLKALT register is set high, the HBLK TOG1 and TOG2 positions will be used on odd lines, while the TOG3–TOG6 positions will be used on even lines. This allows the HBLK interval to be adjusted on odd and even lines if needed.

Figure 19 shows an example of VPAT repetition alternation and HBLK alternation used together. It is also possible to use VPAT and HBLK alternation separately.

**Second V-Pattern Group during VSG Active Line**
Most CCDs require additional vertical timing during the sensor gate line. The AD9991 supports the option to output a second V-pattern group for V1–V6 during the line when the sensor gates VSG1–VSG5 are active. Figure 20 shows a typical VSG line, which includes two separate sets of V-pattern groups for V1–V6. The V-pattern group at the start of the VSG line is selected in the same manner as the other regions, using the appropriate VSEQSEL register. The second V-pattern group, unique to the VSG line, is selected using the VPATSECOND register, located with the Field registers. The start position of the second VPAT group uses the VPATLEN register from the selected VPAT registers. Because the VPATLEN register is used as the start position and not as the VPAT length, it is not possible to program multiple repetitions for the second VPAT group.
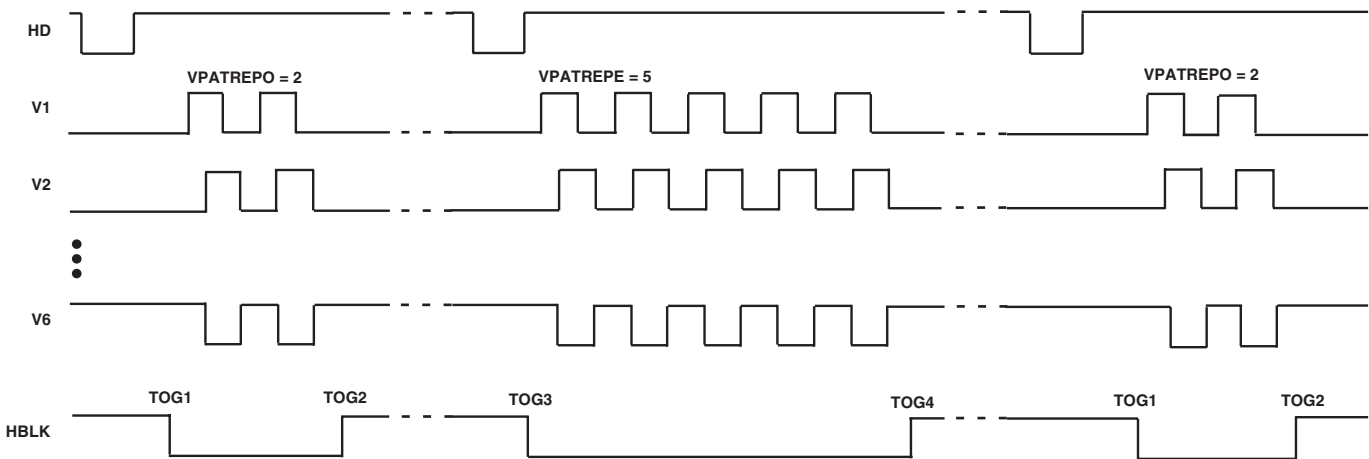


NOTES
1. THE NUMBER OF REPEATS FOR THE V-PATTERN GROUP MAY BE ALTERNATED ON ODD AND EVEN LINES.
2. THE HBLK TOGGLE POSITIONS MAY BE ALTERNATED BETWEEN ODD AND EVEN LINES IN ORDER TO GENERATE DIFFERENT HBLK PATTERNS FOR ODD/EVEN LINES.

*Figure 19. Odd/Even Line Alternation of VPAT Repetitions and HBLK Toggle Positions*
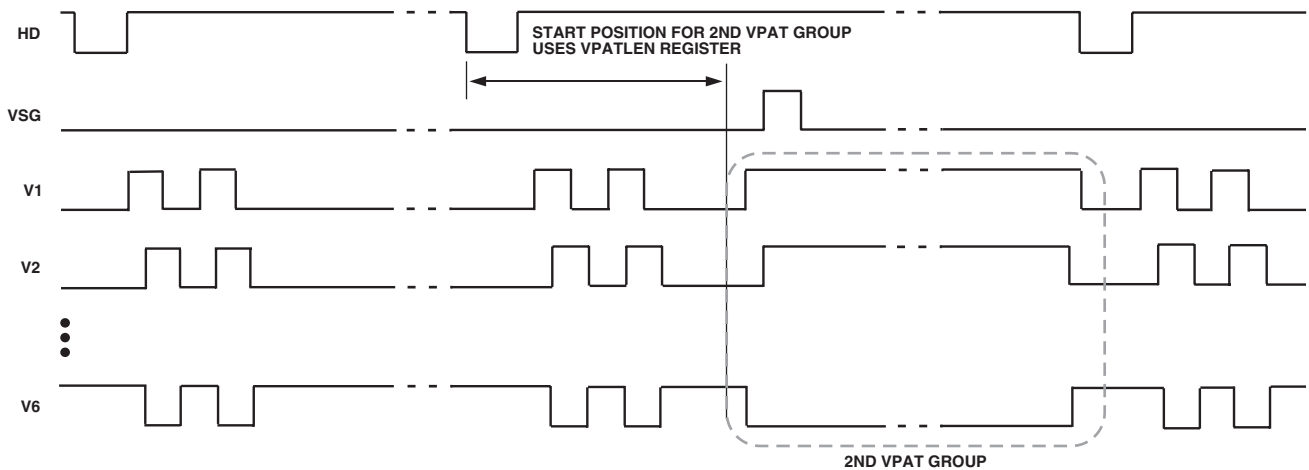


*Figure 20. Example of Second VPAT Group during Sensor Gate Line*

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**Sweep Mode Operation**

The AD9991 contains an additional mode of vertical timing operation called Sweep mode. This mode is used to generate a large number of repetitive pulses that span multiple HD lines. One example of where this mode is needed is at the start of the CCD readout operation. At the end of the image exposure but before the image is transferred by the sensor gate pulses, the vertical interline CCD registers should be free of all charge. This can be accomplished by quickly shifting out any charge using a long series of pulses from the V1–V6 outputs. Depending on the vertical resolution of the CCD, up to 2,000 or 3,000 clock cycles will be needed to shift the charge out of each vertical CCD line. This operation will span across multiple HD line lengths. Normally, the AD9991 vertical timing must be contained within one HD line length, but when Sweep mode is enabled, the HD boundaries will be ignored until the region is finished. To enable Sweep mode within any region, program the appropriate SWEEP register to High.

Figure 21 shows an example of the Sweep mode operation. The number of vertical pulses needed will depend on the vertical resolution of the CCD. The V1–V6 output signals are generated using the V-pattern registers (shown in Table VII). A single pulse is created using the polarity and toggle position registers. The number of repetitions is then programmed to match the number of vertical shifts required by the CCD. Repetitions are programmed in the V-sequence registers using the VPATREP registers. This produces a pulse train of the appropriate length. Normally, the pulse train would be truncated at the end of the HD line length, but with Sweep mode enabled for this region, the HD boundaries will be ignored. In Figure 21, the Sweep

region occupies 23 HD lines. After the Sweep mode region is completed, in the next region, normal sequence operation will resume. When using Sweep mode, be sure to set the region boundries (using the sequence change positions) to the appropriate lines to prevent the Sweep operation from overlapping the next V-sequence.

**Multiplier Mode**

To generate very wide vertical timing pulses, a vertical region may be configured into a multiplier region. This mode uses the V-pattern registers in a slightly different manner. Multiplier mode can be used to support unusual CCD timing requirements, such as vertical pulses that are wider than a single HD line length.

The start polarity and toggle positions are still used in the same manner as the standard VPAT group programming, but the VPATLEN is used differently. Instead of using the pixel counter (HD counter) to specify the toggle position locations (VTOG1, 2, 3) of the VPAT group, the VPATLEN is multiplied with the VTOG position to allow very long pulses to be generated. To calculate the exact toggle position, counted in pixels after the start position, use the equation

$$Multiplier\ Mode\ Toggle\ Position = VTOG \times VPATLEN$$

Because the VTOG register is multiplied by VPATLEN, the resolution of the toggle position placement is reduced. If VPATLEN = 4, the toggle position accuracy is now reduced to 4-pixel steps instead of single pixel steps. Table VIII summarizes how the VPAT group registers are used in Multiplier mode operation. In Multiplier mode, the VPATREPO and VPATREPE registers should always be programmed to the same value as the highest toggle position.
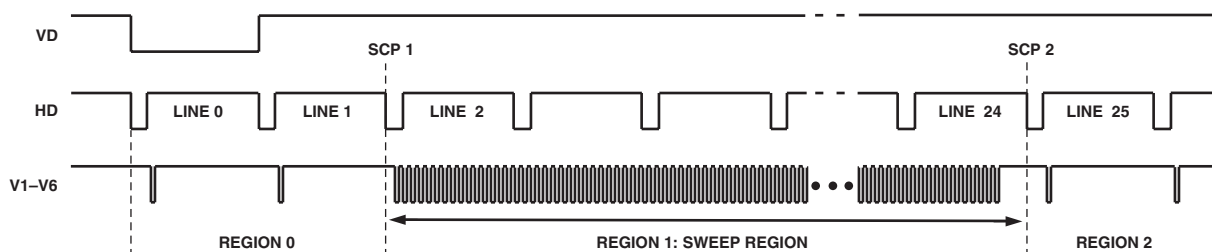


*Figure 21. Example of Sweep Region for High Speed Vertical Shift*

**Table VIII. Multiplier Mode Register Parameters**

| Register | Length | Range | Description |
|---|---|---|---|
| MULTI | 1b | High/Low | High enables Multiplier mode. |
| VPOL | 1b | High/Low | Starting Polarity of V1–V6 Signal in Each VPAT Group. |
| VTOG1 | 12b | 0–4095 Pixel Location | First Toggle Position for V1–V6 Signal in Each VPAT Group. |
| VTOG2 | 12b | 0–4095 Pixel Location | Second Toggle Position for V1–V6 Signal in Each VPAT Group. |
| VTOG3 | 12b | 0–4095 Pixel Location | Third Toggle Position for V1–V6 Signal in Each VPAT Group. |
| VPATLEN | 10b | 0–1023 Pixels | Used as Multiplier Factor for Toggle Position Counter. |
| VPATREP | 12b | 0–4096 | VPATREPE/VPATREPO should be set to the same value as TOG2 or 3. |

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The example shown in Figure 22 illustrates this operation. The first toggle position is 2, and the second toggle position is 9. In non-Multiplier mode, this would cause the V-sequence to toggle at pixel 2 and then pixel 9 within a single HD line. However, toggle positions are now multiplied by the VTPLEN = 4, so the first toggle occurs at pixel count 8, and the second toggle occurs at pixel count 36. Sweep mode has also been enabled to allow the toggle positions to cross the HD line boundaries.

## Vertical Sensor Gate (Shift Gate) Patterns

In an Interline CCD, the vertical sensor gates (VSG) are used to transfer the pixel charges from the light-sensitive image area into light-shielded vertical registers. From the light-shield vertical registers, the image is then read out line-by-line by using the vertical transfer pulses V1–V6 in conjunction with the high speed horizontal clocks.

Table IX contains the summary of the VSG pattern registers. The AD9991 has five VSG outputs, VSG1–VSG5. Each of the outputs can be assigned to one of four programmed patterns by using the SGPATSEL registers. Each pattern is generated in a similar manner as the V-pattern groups, with a programmable start polarity (SGPOL), first toggle position (SGTOG1), and second toggle position (SGTOG2). The active line where the VSG1–VSG5 pulses occur is programmable using the SGLINE1 and SGLINE2 registers. Additionally, any of the VSG1–VSG5 pulses may be individually disabled by using the SGMASK register. The individual masking allows all of the SG patterns to be preprogrammed, and the appropriate pulses for the different fields can be separately enabled. For maximum flexibility, the SGPATSEL, SGMASK, and SGLINE registers are separately programmable for each field. More detail is given in the Complete Field section.



MULTIPLIER MODE V-PATTERN GROUP PROPERTIES:
1. START POLARITY (ABOVE: STARTPOL = 0)
2. FIRST, SECOND, AND THIRD TOGGLE POSITIONS (ABOVE: VTOG1 = 2, VTOG2 = 9)
3. LENGTH OF VPAT COUNTER (ABOVE: VPATLEN = 4). THIS IS THE MINIMUM RESOLUTION FOR TOGGLE POSITION CHANGES.
4. TOGGLE POSITIONS OCCUR AT LOCATION EQUAL TO (VTOG × VPATLEN)
5. IF SWEEP REGION IS ENABLED, THE V-PULSES MAY ALSO CROSS THE HD BOUNDRIES, AS SHOWN ABOVE

*Figure 22. Example of Multiplier Region for Wide Vertical Pulse Timing*

### Table IX. VSG Pattern Registers (also see Field Registers in Table VII)

| Register | Length | Range | Description |
|---|---|---|---|
| SGPOL | 1b | High/Low | Sensor Gate Starting Polarity for SG Pattern 0–3 |
| SGTOG1 | 12b | 0–4095 Pixel Location | First Toggle Position for SG Pattern 0–3 |
| SGTOG2 | 12b | 0–4095 Pixel Location | Second Toggle Position for SG Pattern 0–3 |



PROGRAMMABLE SETTINGS FOR EACH PATTERN:
1. START POLARITY OF PULSE
2. FIRST TOGGLE POSITION
3. SECOND TOGGLE POSITION
4. ACTIVE LINE FOR VSG PULSES WITHIN THE FIELD (PROGRAMMABLE IN THE FIELD REGISTER, NOT FOR EACH PATTERN)

*Figure 23. Vertical Sensor Gate Pulse Placement*

**MODE Register**

The MODE register is a single register that selects the field timing of the AD9991. Typically, all of the field, V-sequence, and V-pattern group information is programmed into the AD9991 at startup. During operation, the MODE register allows the user to select any combination of field timing to meet the current requirements of the system. The advantage of using the MODE register in conjunction with preprogrammed timing is that it greatly reduces the system programming requirements during camera operation. Only a few register writes are required when the camera operating mode is changed, rather than having to write in all of the vertical timing information with each camera mode change.

A basic still camera application might require five different fields of vertical timing: one for draft mode operation, one for autofocusing, and three for still image readout. All of the register timing information for the five fields would be loaded at

startup. Then, during camera operation, the MODE register would select which field timing would be active, depending on how the camera was being used.

Table X shows how the MODE register bits are used. The three MSBs, D23–D21, are used to specify how many total fields will be used. Any value from 1 to 7 can be selected using these three bits. The remaining register bits are divided into 3-bit sections to select which of the six fields are used and in which order. Up to seven fields may be used in a single MODE write. The AD9991 will start with the Field timing specified by the first Field bits, and on the next VD will switch to the timing specified by the second Field bits, and so on.

After completing the total number of fields specified in Bits D23 to D21, the AD9991 will repeat by starting at the first Field again. This will continue until a new write to the MODE register occurs. Figure 24 shows example MODE register settings for different field configurations.

**Table X. MODE Register Data Bit Breakdown (D23 = MSB)**

| D23 22 21 | 20 19 18 | 17 16 15 | 14 13 12 | 11 10 9 | 8 7 6 | 5 4 3 | 2 1 D0 |
|---|---|---|---|---|---|---|---|
| Total Number of Fields to Use. 1 = 1st Field Only 7 = All 7 Fields 0 = Invalid | 7th Field 0 = Field 0 5 = Field 5 6, 7 = Invalid | 6th Field 0 = Field 0 5 = Field 5 6, 7 = Invalid | 5th Field 0 = Field 0 5 = Field 5 6, 7 = Invalid | 4th Field 0 = Field 0 5 = Field 5 6, 7 = Invalid | 3rd Field 0 = Field 0 5 = Field 5 6, 7 = Invalid | 2nd Field 0 = Field 0 5 = Field 5 6, 7 = Invalid | 1st Field 0 = Field 0 5 = Field 5 6, 7 = Invalid |

EXAMPLE 1:
TOTAL FIELDS = 3, 1ST FIELD = FIELD 0, 2ND FIELD = FIELD 1, 3RD FIELD = FIELD 2
MODE REGISTER CONTENTS = 0x600088

FIELD 0 → FIELD 1 → FIELD 2

EXAMPLE 2:
TOTAL FIELDS = 2, 1ST FIELD = FIELD 3, 2ND FIELD = FIELD 4
MODE REGISTER CONTENTS = 0x400023

FIELD 3 → FIELD 4

EXAMPLE 3:
TOTAL FIELDS = 4, 1ST FIELD = FIELD 5, 2ND FIELD = FIELD 1, 3RD FIELD = FIELD 4, 4TH FIELD = FIELD 2
MODE REGISTER CONTENTS = 0x80050D
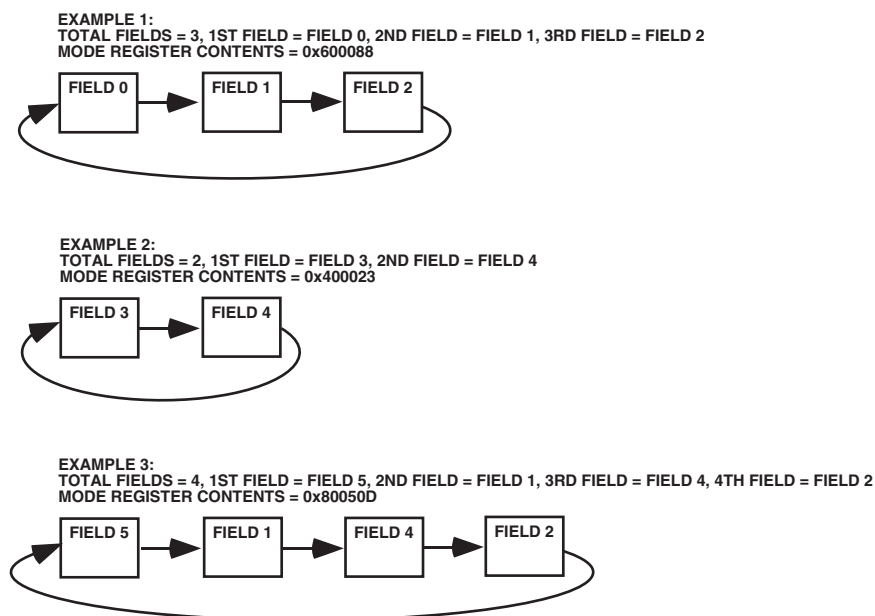
FIELD 5 → FIELD 1 → FIELD 4 → FIELD 2

*Figure 24. Using the MODE Register to Select Field Timing*

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**VERTICAL TIMING EXAMPLE**
To better understand how the AD9991 vertical timing generation is used, consider the example CCD timing chart in Figure 25. This particular example illustrates a CCD using a general 3-field readout technique. As described in the previous Field section, each readout field should be divided into separate regions to perform each step of the readout. The sequence change positions (SCP) determine the line boundaries for each region, and the VSEQSEL registers will then assign a particular V-sequence to each region. The V-sequences will contain the specific timing information required in each region: V1–V6 pulses (using VPAT groups), HBLK/CLPOB timing, and VSG patterns for the SG active lines.

This particular timing example requires four regions for each of the three fields, labeled Region 0, Region 1, Region 2, and Region 3. Because the AD9991 allows up to six individual fields to be programmed, the Field 0, Field 1, and Field 2 registers can be used to meet the requirements of this timing example. The four regions for each field are very similar in this example, but the individual registers for each field allow flexibility to accommodate other timing charts.

Region 0 is a high speed vertical shift region. Sweep mode can be used to generate this timing operation, with the desired number of high speed vertical pulses needed to clear any charge from the CCD's vertical registers.

Region 1 consists of only two lines, and uses standard single line vertical shift timing. The timing of this region area will be the same as the timing in Region 3.

Region 2 is the sensor gate line, where the VSG pulses transfer the image into the vertical CCD registers. This region may require the use of the second V-pattern group for SG active line.

Region 3 also uses the standard single line vertical shift timing, the same timing as Region 1.

In summary, four regions are required in each of the three fields. The timing for Regions 1 and 3 is essentially the same, reducing the complexity of the register programming.

Other registers will need to be used during the actual readout operation, such as the MODE register, shutter control registers (TRIGGER, SUBCK, VSUB, MSHUT, STROBE), and the AFE gain register. These registers will be explained in other examples.

**Important Note About Signal Polarities**
When programming the AD9991 to generate the V1–V6, VSG1–VSG5, and SUBCK signals, it is important to note that the V-driver circuit usually inverts these signals. Carefully check the required timing signals needed at the input and output of the V-driver circuit being used, and adjust the polarities of the AD9991 outputs accordingly.
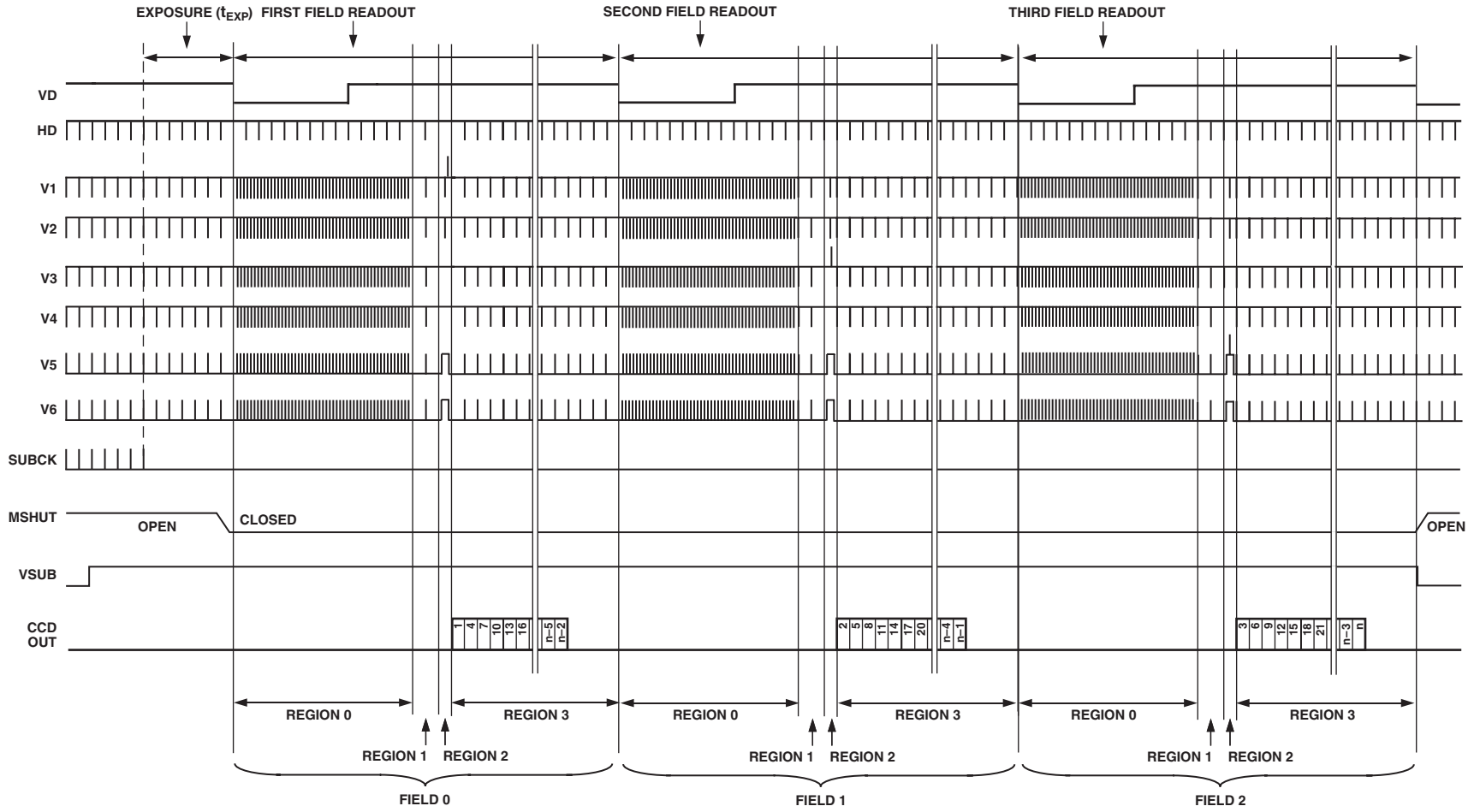
Figure 25. CCD Timing Example: Dividing Each Field into Regions

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