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12-Bit CCD Signal Processor with *Precision Timing* Generator

AD9992

FEATURES

1.8 V AFETG core
Internal LDO regulator and charge pump circuitry
Compatibility with 3 V or 1.8 V systems
24 programmable vertical clock outputs
Correlated double sampler (CDS) with −3 dB, 0 dB, +3 dB, and +6 dB gain
6 dB to 42 dB, 10-bit variable gain amplifier (VGA)
12-bit, 40 MHz ADC
Black level clamp with variable level control
Complete on-chip timing generator
***Precision Timing* core with 400 ps resolution**
On-chip 3 V horizontal and RG drivers
General-purpose outputs (GPOs) for shutter and system support
On-chip driver for external crystal
On-chip sync generator with external sync input
105-lead CSP_BGA package, 8 mm × 8 mm, 0.65 mm pitch

APPLICATIONS

Digital still cameras

GENERAL DESCRIPTION

The AD9992 is a highly integrated CCD signal processor for digital still camera applications. It includes a complete analog front end with analog to digital conversion combined with a full-function programmable timing generator. The timing generator is capable of supporting up to 24 vertical clock signals to control advanced CCDs. A *Precision Timing*™ core allows adjustment of high speed clocks with approximately 400 ps resolution at 40 MHz operation. The AD9992 also contains eight general-purpose inputs/outputs that can be used for shutter and system functions.

The AD9992 is specified at pixel rates of up to 40 MHz. The analog front end includes black level clamping, CDS, VGA, and a 12-bit analog-to-digital converter (ADC). The timing generator provides all the necessary CCD clocks: RG, H-clocks, V-clocks, sensor gate pulses, substrate clock, and substrate bias control. Operation is programmed using a 3-wire serial interface.

The AD9992 is specified over an operating temperature range of −25°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

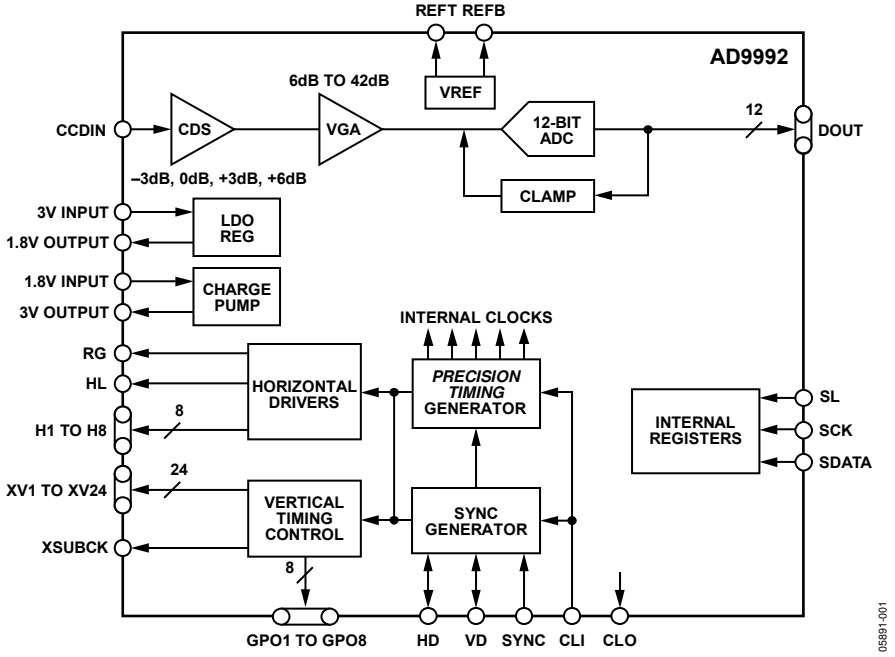

Figure 1.

Rev. C

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SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating	−25		+85	°C
Storage	−65		+150	°C
POWER SUPPLY VOLTAGE INPUTS				
AVDD (AFE Analog Supply)	1.6	1.8	2.0	V
TCVDD (Timing Core Supply)	1.6	1.8	2.0	V
CLIVDD (CLI Input Supply)	1.6	3.0	3.6	V
RGVDD (RG, HL Driver)	2.7	3.0	3.6	V
HVDD1/HVDD2 (H1 to H8 Drivers)[1]	2.7	3.0	3.6	V
DVDD (Digital Logic)	1.6	1.8	2.0	V
DRVDD (Parallel Data Output Drivers)	1.6	3.0	3.6	V
IOVDD (Digital I/O)	1.6	3.0	3.6	V
XVVDD (Vertical Output Drivers)	1.6	3.0	3.6	V
CP1P8 (CP Supply Input)	1.6	1.8	2.0	V
LDOIN (LDO Supply Input)	2.25	3.0	3.6	V
POWER SUPPLY CURRENTS—40 MHz OPERATION				
AVDD (1.8 V)		27		mA
TCVDD (1.8 V)		5		mA
CLIVDD (3 V)		1.5		mA
RGVDD (3.3 V, 20 pF RG Load, 20 pF HL Load)		10		mA
HVDD1/HVDD2 (3.3 V, 480 pF Total Load on H1 to H8)[1]		59		mA
DVDD (1.8 V)		9.5		mA
DRVDD (3 V, 10 pF Load on Each DOUT Pin)		6		mA
IOVDD (3 V, Depends on Load and Output Frequency of Digital I/O)		2		mA
XVVDD (3 V, Depends on Load and Output Frequency of XV Signals)		2		mA
POWER SUPPLY CURRENTS—STANDBY MODE OPERATION				
Standby1 Mode		12		mA
Standby2 Mode		5		mA
Standby3 Mode		1.5		mA
MAXIMUM CLOCK RATE (CLI)	40			MHz

[1] The total power dissipated by the HVDD (or RGVDD) supply can be approximated using the equation
Total HVDD Power = [$C_L \times HVDD \times Pixel\ Frequency$] × *HVDD*
Reducing the capacitive load and/or reducing the HVDD supply reduces the power dissipation. C_L is the total capacitance seen by all H-outputs.

DIGITAL SPECIFICATIONS

IOVDD = 1.6 V to 3.6 V, RGVDD = HVDD = 2.7 V to 3.6 V, C_L = 20 pF, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS (IOVDD)					
High Level Input Voltage	V_{IH}	V_{DD} – 0.6			V
Low Level Input Voltage	V_{IL}			0.6	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS (IOVDD, XVDD)					
High Level Output Voltage @ I_{OH} = 2 mA	V_{OH}	V_{DD} – 0.5			V
Low Level Output Voltage @ I_{OL} = 2 mA	V_{OL}			0.5	V
RG and H-DRIVER OUTPUTS (HVDD, RGVDD)					
High Level Output Voltage @ Maximum Current	V_{OH}	V_{DD} – 0.5			V
Low Level Output Voltage @ Maximum Current	V_{OL}			0.5	V
Maximum Output Current (Programmable)		18			mA
Maximum Load Capacitance (for Each Output)		60			pF

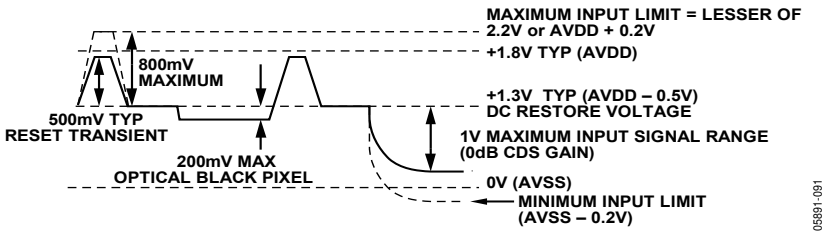


Figure 2. Input Signal Characteristics
(See Allowable OB Pixel Amplitude in Table 3)

ANALOG SPECIFICATIONS

AVDD = 1.8 V, f_{CLI} = 40 MHz, typical timing specifications, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CDS					
Allowable CCD Reset Transient		0.5	0.8	V	The limit is the lower of AVDD + 0.2 V or 2.2 V.
CDS Gain Accuracy					VGA gain = 6.3 dB (Code 15, default value).
−3.0 dB CDS Gain	−3.3	−2.8	−2.3	dB	
0 dB CDS Gain	−0.5	0	+0.5	dB	
+3 dB CDS Gain	2.4	2.9	3.4	dB	
+6 dB CDS Gain	5.0	5.5	6.0	dB	
Maximum Input Range Before Saturation					VGA gain = 6.3 dB (Code 15, default value).
−3 dB CDS Gain		1.4		V p-p	
0 dB CDS Gain		1.0		V p-p	
+3 dB CDS Gain		0.7		V p-p	
+6 dB CDS Gain		0.5		V p-p	
Allowable OB Pixel Amplitude (See Figure 2)					
0 dB CDS Gain (Default)	−100		+200	mV	
+6 dB CDS Gain	−50		+100	mV	
VARIABLE GAIN AMPLIFIER (VGA)					
Gain Control Resolution		1024		Steps	
Gain Monotonicity		Guaranteed			
Gain Range					
Low Gain (VGA Code 15, Default)		6.3		dB	
Maximum Gain (VGA Code 1023)		42.4		dB	
BLACK LEVEL CLAMP					
Clamp Level Resolution		1024		Steps	
Clamp Level					Measured at ADC output.
Minimum Clamp Level (Code 0)		0		LSB	
Maximum Clamp Level (Code 1023)		255		LSB	
ADC					
Resolution	12			Bits	
Differential Nonlinearity (DNL)	−1.0	±0.5	+1.0	LSB	
No Missing Codes		Guaranteed			
Integral Nonlinearity (INL)		1	4	LSB	
Full-Scale Input Voltage		2.0		V	
VOLTAGE REFERENCE					
Reference Top Voltage (REFT)		1.4		V	
Reference Bottom Voltage (REFB)		0.4		V	
SYSTEM PERFORMANCE					Includes entire signal chain.
Gain Accuracy					0 dB CDS gain.
Low Gain (VGA Code 15)	5.8	6.3	6.8	dB	Gain = (0.0358 × Code) + 5.76 dB.
Maximum Gain (VGA Code 1023)	41.9	42.4	42.9	dB	
Peak Nonlinearity, 1.0 V Input Signal		0.1	0.2	%	6 dB VGA gain, 0 dB CDS gain applied.
Total Output Noise		0.5		LSB rms	AC-grounded input, 6 dB VGA gain applied.
Power Supply Rejection (PSR)		50		dB	Measured with step change on supply.

TIMING SPECIFICATIONS

C_L = 20 pF, AVDD = DVDD = TCVDD = 1.8 V, DRVDD = 3.0 V, f_{CLI} = 40 MHz, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
MASTER CLOCK (See Figure 15)					
CLI Clock Period	t_{CONV}	25			ns
CLI High/Low Pulse Width		10	12.5	15	ns
Delay from CLI Rising Edge to Internal Pixel Position 0	t_{CLIDLY}		6		ns
SLAVE MODE SPECIFICATIONS (See Figure 76)					
VD Falling Edge to HD Falling Edge in Slave Mode	t_{VDHD}	0		VD period − 5 × t_{CONV}	ns
HD Edge to CLI Rising Edge (Only Valid if OSC_RSTB = LO)	t_{HDCLI}	3		t_{CONV} − 2	ns
HD Edge to CLO Rising Edge (Only Valid if OSC_RSTB = HI)	t_{HDCLO}	3		t_{CONV} − 2	ns
Inhibit Region for SHP Edge Location	t_{SHPINH}	48		63	Edge location
AFE CLPOB PULSE WIDTH (See Figure 22 and Figure 32)[1, 2]		2	20		Pixels
AFE SAMPLE LOCATION (See Figure 16 and Figure 19)[1]					
SHP Sample Edge to SHD Sample Edge	t_{S1}	11	12.5		ns
DATA OUTPUTS (See Figure 20 and Figure 21)					
Output Delay from DCLK Rising Edge	t_{OD}		1		ns
Inhibited Area for DOUTPHASE Edge Location	$t_{DOUTINH}$	SHDLOC + 1		SHDLOC + 15	Edge location
Pipeline Delay from SHP/SHD Sampling to DOUT			16		Cycles
SERIAL INTERFACE (See Figure 83)					
Maximum SCK Frequency (Must Not Exceed CLI Frequency)	f_{SCLK}	40			MHz
SL to SCK Setup Time	t_{LS}	10			ns
SCK to SL Hold Time	t_{LH}	10			ns
SDATA Valid to SCK Rising Edge Setup	t_{DS}	10			ns
SCK Falling Edge to SDATA Valid Hold	t_{DH}	10			ns
INHIBIT REGION FOR SHP AND SHD WITH RESPECT TO H-CLOCK EDGE PLACEMENT (see Figure 19) for H*POL = 1					
RETIME = 0, MASK = 0	t_{SHDINH}	H*NEGLOC − 15		H*NEGLOC − 0	Edge location
RETIME = 0, MASK = 1	t_{SHDINH}	H*POSLOC − 15		H*POSLOC − 0	Edge location
RETIME = 1, MASK = 0	t_{SHPINH}	H*NEGLOC − 15		H*NEGLOC − 0	Edge location
RETIME = 1, MASK = 1	t_{SHPINH}	H*POSLOC − 15		H*POSLOC − 0	Edge location

[1] Parameter is programmable.
[2] Minimum CLPOB pulse width is for functional operation only. Wider typical pulses are recommended to achieve good clamp performance.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect To	Rating
AVDD	AVSS	−0.2 V to +2.2 V
TCVDD	TCVSS	−0.2 V to +2.2 V
HVDD1/HVDD2	HVSS1/HVSS2	−0.3 V to +3.9 V
RGVDD	RGVSS	−0.3 V to +3.9 V
DVDD	DVSS	−0.2 V to +2.2 V
DRVDD	DRVSS	−0.3 V to +3.9 V
IOVDD	DVSS	−0.3 V to +3.9 V
XVVDD	DVSS	−0.3 V to +3.9 V
CLIVDD	TCVSS	−0.3 V to +3.9 V
CP1P8	CPVSS	−0.2 V to +2.2 V
RG Output	RGVSS	−0.3 V to RGVDD + 0.3 V
H1 to H8, HL Output	HVSS1/HVSS2	−0.3 V to HVDD + 0.3 V
Digital Outputs	DVSS	−0.3 V to IOVDD + 0.3 V
Digital Inputs	DVSS	−0.3 V to IOVDD + 0.3 V
SCK, SL, SDATA	DVSS	−0.3 V to IOVDD + 0.3 V
REFT, REFB, CCDIN	AVSS	−0.2 V to AVDD + 0.2 V
Junction Temperature		150°C
Lead Temperature, 10 sec		350°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
106-Lead CSP_BGA	40.3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

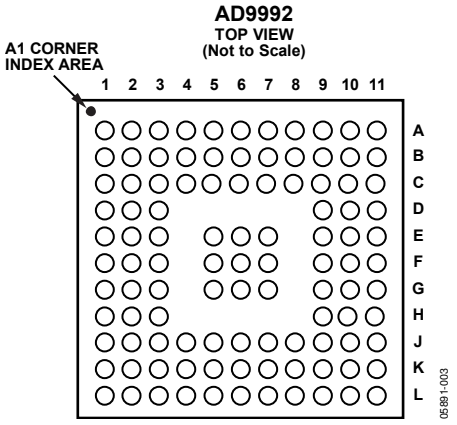


Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1	GPO8	DIO	General-Purpose Output 8
B2	GPO7	DIO	General-Purpose Output 7
C2	GPO6	DIO	General-Purpose Output 6
B1	GPO5	DIO	General-Purpose Output 5
B4	GPO4	DIO	General-Purpose Output 4
C1	GPO3	DIO	General-Purpose Output 3
D2	GPO2	DIO	General-Purpose Output 2
C3	GPO1	DIO	General-Purpose Output 1
D3	SYNC	DI	External System Sync Input
E2	VD	DIO	Vertical Sync Pulse (input for slave mode, output for master mode)
D1	HD	DIO	Horizontal Sync Pulse (input for slave mode, output for master mode)
E7	RSTB	DI	External Reset Input (active low pulse to reset, internal pull-up resistor)
E6	IOVDD	P	Digital I/O Supply: 1.8 V, 3.0 V (GPO, SUBCK, HD/VD, SL, SCK, SDATA, SYNC, RSTB)
E5	IOVSS	P	Digital I/O Ground
E3	XVVDD	P	XV Output Supply: 1.8 V, 3.0 V
E1	XSUBCK	DO	CCD Substrate Clock
F2	XV1	DO	CCD Vertical Clock 1
F3	XV2	DO	CCD Vertical Clock 2
F7	XV3	DO	CCD Vertical Clock 3
G3	XV4	DO	CCD Vertical Clock 4
F5	XV5	DO	CCD Vertical Clock 5
F6	XV6	DO	CCD Vertical Clock 6
G2	XV7	DO	CCD Vertical Clock 7
F1	XV8	DO	CCD Vertical Clock 8
G1	XV9	DO	CCD Vertical Clock 9
G5	XV10	DO	CCD Vertical Clock 10
H2	XV11	DO	CCD Vertical Clock 11
H1	XV12	DO	CCD Vertical Clock 12
G6	XV13	DO	CCD Vertical Clock 13
G7	XV14	DO	CCD Vertical Clock 14
J2	XV15	DO	CCD Vertical Clock 15
J1	XV16	DO	CCD Vertical Clock 16
L1	XV17	DO	CCD Vertical Clock 17
L2	XV18	DO	CCD Vertical Clock 18

Pin No.	Mnemonic	Type[1]	Description
L3	XV19	DO	CCD Vertical Clock 19
K1	XV20	DO	CCD Vertical Clock 20
K2	XV21	DO	CCD Vertical Clock 21
K3	XV22	DO	CCD Vertical Clock 22
J3	XV23	DO	CCD Vertical Clock 23
H3	XV24	DO	CCD Vertical Clock 24
L4	DVDD	P	Digital Logic Supply: 1.8 V
K4	DVSS	P	Digital Logic Ground
L6	D0	DO	Data Output 0 (LSB)
K6	D1	DO	Data Output 1
J6	D2	DO	Data Output 2
L7	D3	DO	Data Output 3
K7	D4	DO	Data Output 4
J7	D5	DO	Data Output 5
L8	D6	DO	Data Output 6
K8	D7	DO	Data Output 7
J8	D8	DO	Data Output 8
L9	D9	DO	Data Output 9
K9	D10	DO	Data Output 10
J9	D11	DO	Data Output 11 (MSB)
L10	DCLK	DO	Data Clock Output
K10	DRVSS	P	Data Driver Ground
L11	DRVDD	P	Data Driver Supply: 1.8 V, 3.0 V
K11	CP3P3	P	Charge Pump 3.3 V Output
J10	CPFCT	AO	Charge Pump Flying Capacitor Top
J11	CPFCB	AO	Charge Pump Flying Capacitor Bottom
H10	CPVSS	P	Charge Pump Ground
H11	CP1P8	P	Charge Pump 1.8 V Input
H9	CPCLI	DI	Charge Pump Clock Input
G11	LDO3P2EN	DI	LDO 3.2 V Output Enable
G9	LDOVSS	P	LDO Ground
F10	LDO1P8EN	DI	LDO 1.8 V Output Enable
F11	SENSE	AI	LDO Output Sense
E11	LDOOUT	AO	LDO Output Voltage
E10	LDOIN	P	LDO 3.3 V Input
F9	H1	DO	CCD Horizontal Clock 1
E9	H2	DO	CCD Horizontal Clock 2
D11	HVSS1	P	H-Driver Ground 1
C11	HVDD1	P	H-Driver Supply 1: 3.3 V
D10	H3	DO	CCD Horizontal Clock 3
C10	H4	DO	CCD Horizontal Clock 4
D9	H5	DO	CCD Horizontal Clock 5
C9	H6	DO	CCD Horizontal Clock 6
B11	HVSS2	P	H-Driver Ground 2
A11	HVDD2	P	H-Driver Supply 2: 3.3 V
B10	H7	DO	CCD Horizontal Clock 7
A10	H8	DO	CCD Horizontal Clock 8
B9	HL	DO	CCD Last Horizontal Clock
B8	RGVSS	P	RG Driver Ground
A8	RGVDD	P	RG Driver Supply: 3.3 V
C8	RG	DO	CCD Reset Gate Clock
B7	TCVSS	P	Analog Ground for Timing Core
A7	TCVDD	P	Timing Core Supply: 1.8 V

Pin No.	Mnemonic	Type[1]	Description
C7	CLIVDD	P	CLI Input Supply: 3.0 V
C6	CLO	DO	Clock Output for Crystal
C5	CLI	DI	Reference Clock Input
B6	AVDD	P	AFE Supply: 1.8 V
A6	CCDIN	AI	CCD Signal Input
B5, A5	AVSS	P	Analog Supply Ground
A4	REFT	AO	Voltage Reference Top Bypass
A3	REFB	AO	Voltage Reference Bottom Bypass
C4	SL	DI	3-Wire Serial Load Pulse (internal pull-up resistor)
A2	SDATA	DI	3-Wire Serial Data Input
B3	SCK	DI	3-Wire Serial Clock
A9, G10, K5, J4, J5, L5	NC		Not Internally Connected

[1] DIO = digital input/output, DI = digital input, P = power, DO = digital output, AI = analog input, AO = analog output.

TYPICAL PERFORMANCE CHARACTERISTICS

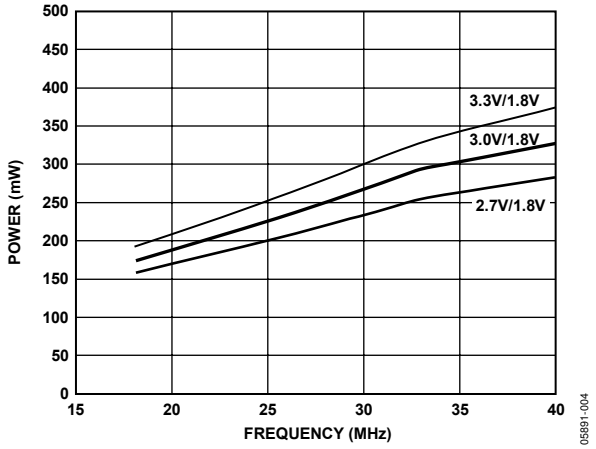


Figure 4. Power vs. Frequency
(AVDD = TCVDD = DVDD = 1.8 V, All Other Supplies at 2.7 V, 3.0 V, or 3.3 V)

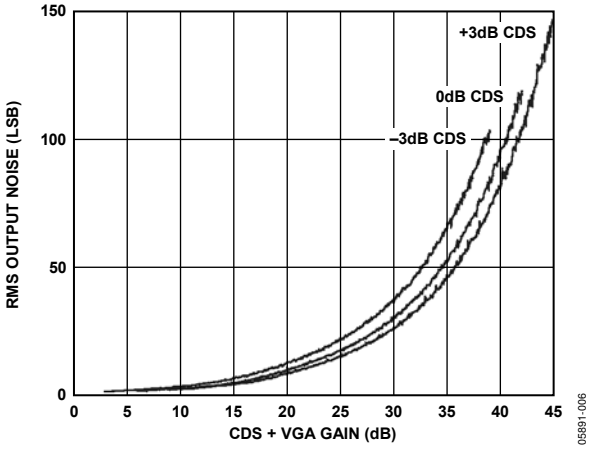


Figure 6. Output Noise vs. Total Gain (CDS + VGA)

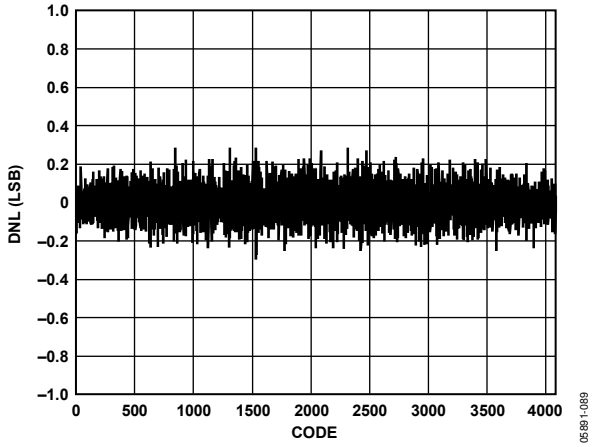


Figure 5. Typical Differential Nonlinearity (DNL) Performance

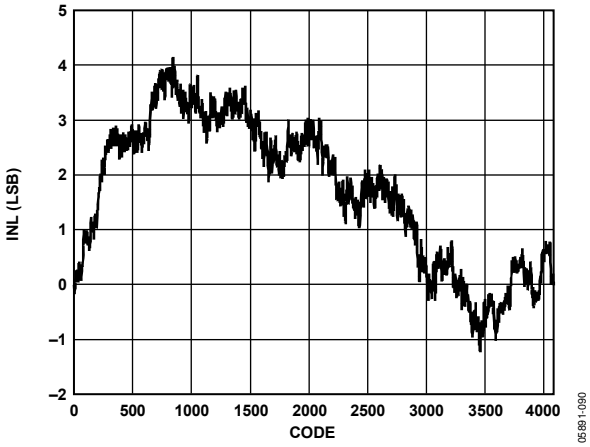


Figure 7. Typical Integral Nonlinearity (INL) Performance

EQUIVALENT CIRCUITS

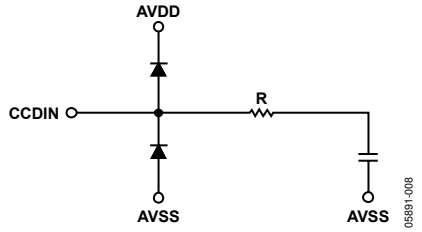


Figure 8. CCDIN

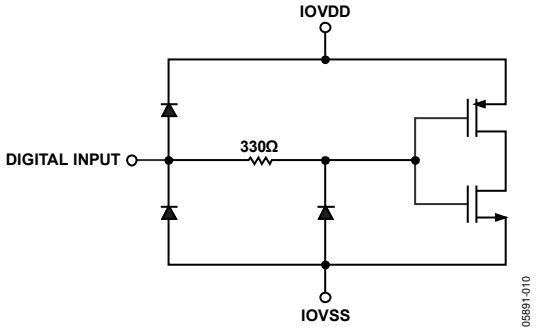


Figure 10. Digital Inputs

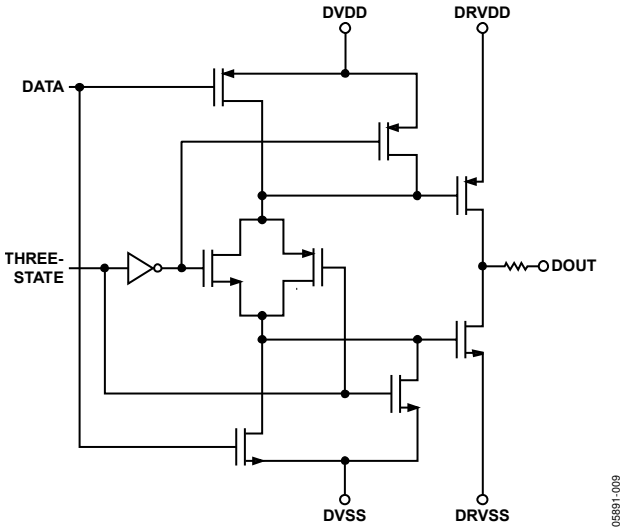


Figure 9. Digital Data Outputs

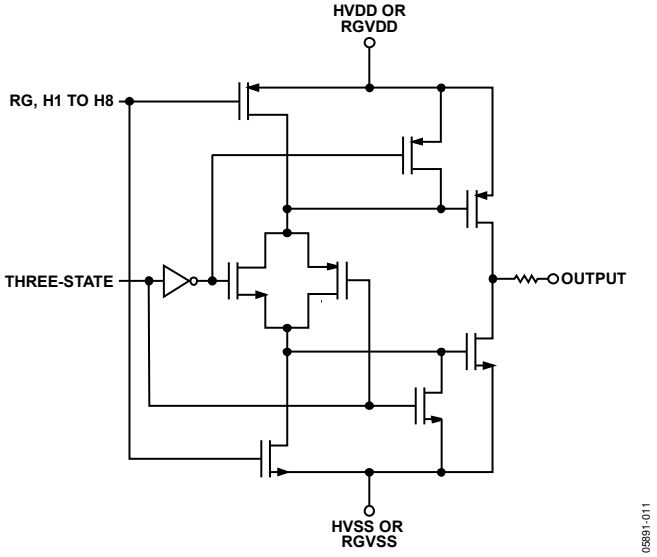


Figure 11. H1 to H8, HL, RG Drivers

TERMINOLOGY

Differential Nonlinearity (DNL)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore, every code must have a finite width. No missing codes guaranteed to 12-bit resolution indicates that all 4096 codes must be present over all operating conditions.

Peak Nonlinearity
Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the output of the AD9992 from a true straight line. The point used as zero scale occurs 0.5 LSB before the first code transition. Positive full scale is defined as a level 1 LSB and 0.5 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always appropriately amplified to fill the full-scale range of the ADC.

Total Output Noise
The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage using the relationship

$$1\ \text{LSB} = (\textit{ADC Full Scale}/2^{n}\ \textit{Codes})$$

where n is the bit resolution of the ADC. For the AD9992, 1 LSB is 0.488 mV.

Power Supply Rejection (PSR)
The PSR is measured with a step change applied to the supply pins. The PSR specification is calculated from the change in data outputs for a given step change in the supply voltage.

SYSTEM OVERVIEW

Figure 12 shows the typical system block diagram for the AD9992 in master mode. The CCD output is processed by AD9992 AFE circuitry, which consists of a CDS, VGA, black level clamp, and ADC. The digitized pixel information is sent to the digital image processor chip, which performs the postprocessing and compression. To operate the CCD, all CCD timing parameters are programmed into the AD9992 from the system microprocessor through the 3-wire serial interface. The AD9992 generates the CCD's horizontal and vertical clocks and internal AFE clocks from the master clock, CLI, which is provided by the image processor or external crystal,. External synchronization is provided by a sync pulse from the microprocessor, which resets the internal counters and resyncs the VD and HD outputs.

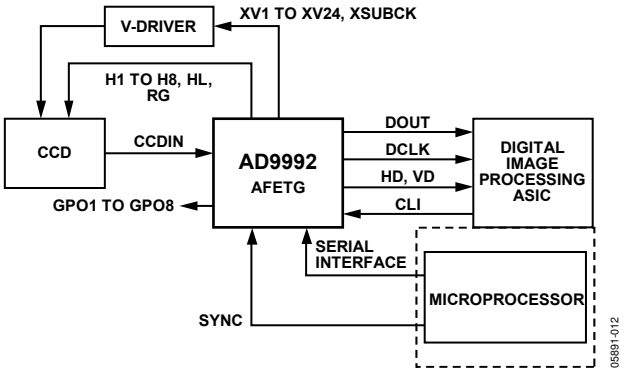


Figure 12. Typical System Block Diagram, Master Mode

Alternatively, the AD9992 can operate in slave mode. In slave mode, the VD and HD are provided externally from the image processor, and all AD9992 timing synchronizes with VD and HD.

H-drivers for H1 to H8, HL, and RG are included in the AD9992, allowing these clocks to be directly connected to the CCD. An H-driver voltage of up to 3.3 V is supported. An external V-driver is required for the vertical transfer clocks, the sensor gate pulses, and the substrate clock.

The AD9992 includes programmable general-purpose outputs (GPO), which can trigger mechanical shutter and strobe (flash) circuitry.

Figure 13 and Figure 14 show the maximum horizontal and vertical counter dimensions for the AD9992. All internal horizontal and vertical clocking is controlled by these counters, which specify line and pixel locations. Maximum HD length is 8192 pixels per line; maximum VD length is 8192 lines per field.

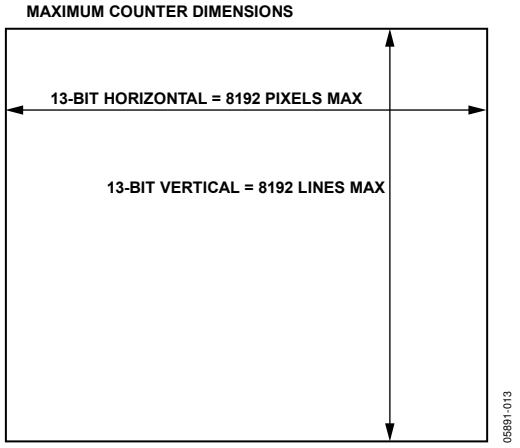


Figure 13. Vertical and Horizontal Counters

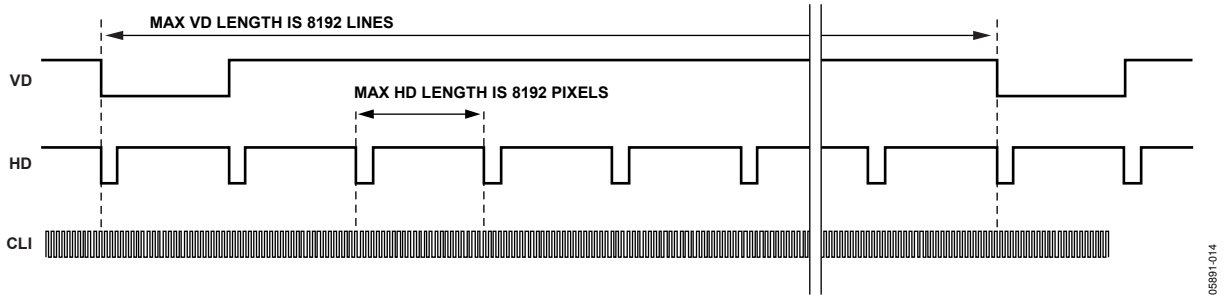


Figure 14. Maximum VD/HD Dimensions

HIGH SPEED *PRECISION TIMING* CORE

The AD9992 generates high speed timing signals using the flexible *Precision Timing* core. This core is the foundation for generating timing used for both the CCD and the AFE; it includes the reset gate RG, horizontal drivers H1 to H8, HL, and SHP/SHD sample clocks. A unique architecture makes it routine for the system designer to optimize image quality by providing precise control over the horizontal CCD readout and the AFE correlated double sampling.

The high speed timing of the AD9992 operates the same way in either master or slave mode configuration. For more information on synchronization and pipeline delays, see the Power-Up Sequence for Master Mode section.

Timing Resolution

The *Precision Timing* core uses a 1× master clock input (CLI) as a reference. This clock should be the same as the CCD pixel clock frequency. Figure 15 illustrates how the internal timing core divides the master clock period into 64 steps or edge positions. Using a 40 MHz CLI frequency, the edge resolution of the *Precision Timing* core is approximately 0.4 ns. If a 1× system clock is not available, it is possible to use a 2× reference clock by programming the CLIDIVIDE register (AFE Register Address 0x0D). The AD9992 then internally divides the CLI frequency by 2.

The AD9992 includes a master clock output (CLO) which is the inverse of CLI. This output should be used as a crystal driver. A crystal can be placed between the CLI and CLO pins to generate the master clock for the AD9992.

High Speed Clock Programmability

Figure 16 shows when the high speed clocks RG, H1 to H8, SHP, and SHD are generated. The RG pulse has programmable rising and falling edges and can be inverted using the polarity control. Horizontal Clock H1 has programmable rising and falling edges and polarity control. In HCLK Mode 1, H3, H5, and H7 are equal to H1. H2, H4, H6, and H8 are always inverses of H1.

The edge location registers are each six bits wide, allowing selection of all 64 edge locations. Figure 19 shows the default timing locations for all high speed clock signals.

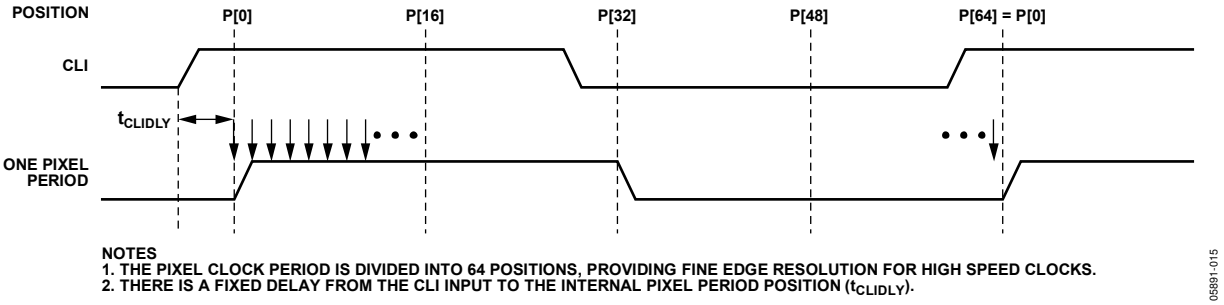


Figure 15. High Speed Clock Resolution from CLI, Master Clock Input

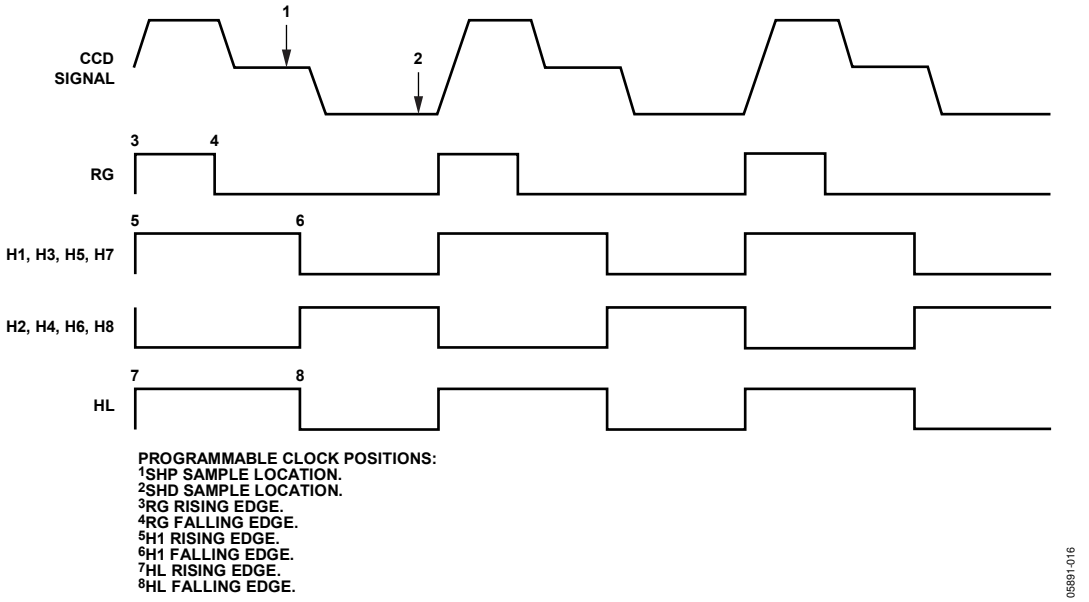


Figure 16. High Speed Clock Programmable Locations (HCLKMODE = 001)

H-Driver and RG Outputs

In addition to the programmable timing positions, the AD9992 features on-chip output drivers for the RG, HL, and H1 to H8 outputs. These drivers are powerful enough to drive the CCD inputs directly. The H-driver and RG current can be adjusted for optimum rise/fall time for a particular load by using the drive strength control registers (Address 0x35 and Address 0x36). The 3-bit drive setting for each output is adjustable in 4.3 mA increments: 0 = three-state; 1 = 4.3 mA; 2 = 8.6 mA; 3 = 12.9 mA; and 4, 5, 6, 7 = 17.2 mA.

As shown in Figure 16, when HCLK Mode 1 is used, the H2, H4, H6, and H8 outputs are inverses of the H1, H3, H5, and H7 outputs, respectively. Using the HCLKMODE register (Address 0x23, Bits [9:7]), it is possible to select a different configuration. Table 9 shows a comparison of the different programmable settings for each HCLK mode. Figure 17 and Figure 18 show the settings for HCLK Mode 2 and HCLK Mode 3, respectively.

It is recommended that all H1 to H8 outputs on the AD9992 be used together for maximum flexibility in drive strength settings. A typical CCD with H1 and H2 inputs should only have the AD9992 H1, H3, H5, and H7 outputs connected together to drive the CCD's H1, and the H2, H4, H6, and H8 outputs connected together to drive the CCD's H2. Similarly, a CCD with H1, H2, H3, and H4 inputs should have

- H1 and H3 connected to the CCD's H1.
- H2 and H4 connected to the CCD's H2.
- H5 and H7 connected to the CCD's H3.
- H6 and H8 connected to the CCD's H4.

Table 8. Timing Core Register Parameters for H1, H2, HL, RG, SHP, SHD

Parameter	Length	Range	Description
Polarity	1b	High/low	Polarity control for H1, H2, HL, and RG (0 = inversion, 1 = no inversion)
Positive Edge	6b	0 to 63 edge location	Positive edge location for H1, H2, HL, and RG
Negative Edge	6b	0 to 63 edge location	Negative edge location for H1, H2, HL, and RG
Sampling Location	6b	0 to 63 edge location	Sampling location for internal SHP and SHD signals
Drive Strength	3b	0 to 4 current steps	Drive current for H1 to H8 , HL, and RG outputs (4.3 mA per step)

Table 9. HCLK Modes, Selected by Address 0x23, Bits[9:7]

HCLKMODE	Register Value	Description
Mode 1	001	H1 edges are programmable, with H3 = H5 = H7 = H1, H2 = H4 = H6 = H8 = inverse of H1
Mode 2	010	H1 edges are programmable, with H3 = H5 = H7 = H1 H2 edges are programmable, with H4 = H6 = H8 = H2
Mode 3	100	H1 edges are programmable, with H3 = H1 and H2 = H4 = inverse of H1 H5 edges are programmable, with H7 = H5 and H6 = H8 = inverse of H5
Invalid Selection	000, 011, 101, 110, 111	Invalid register settings

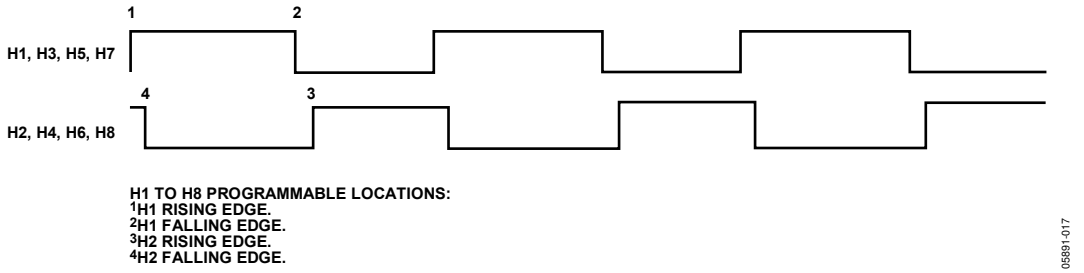


Figure 17. HCLK Mode 2 Operation

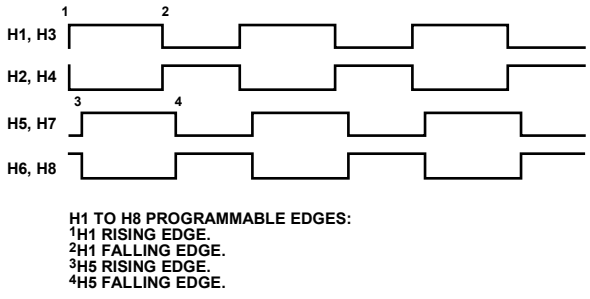


Figure 18. HCLK Mode 3 Operation

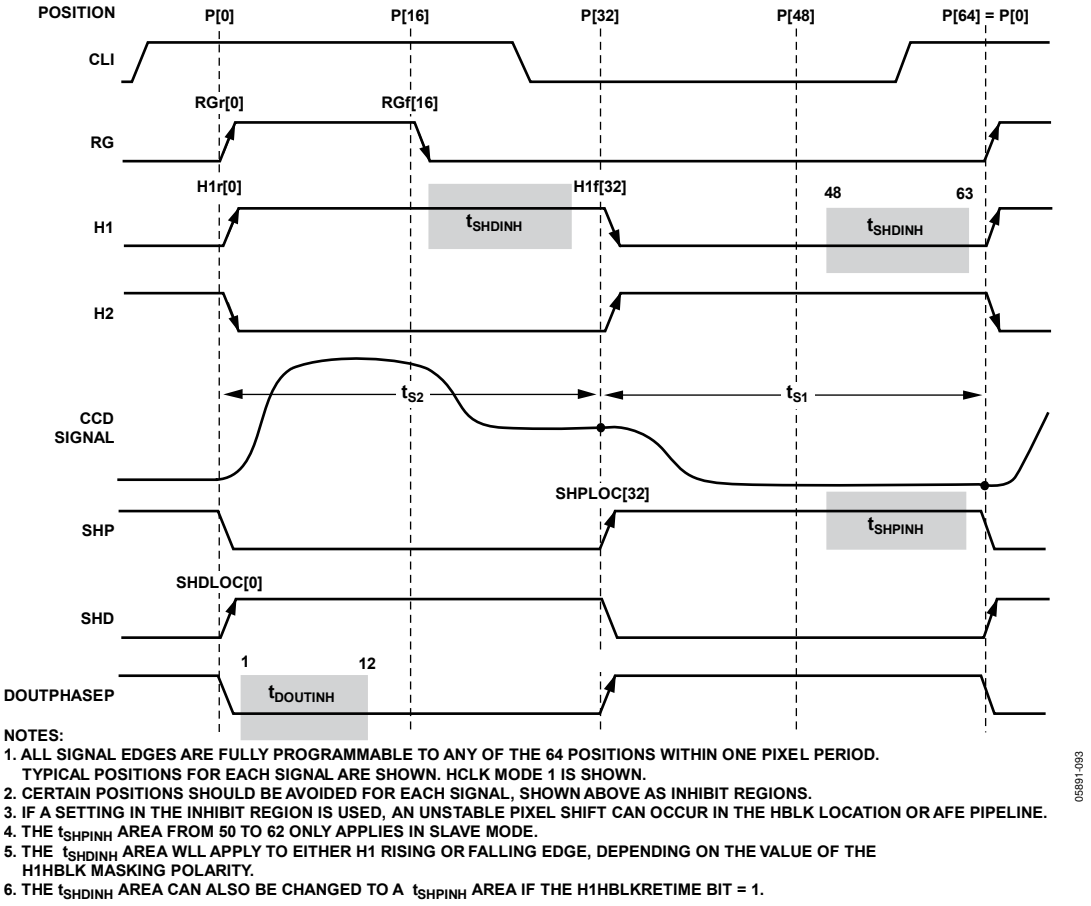


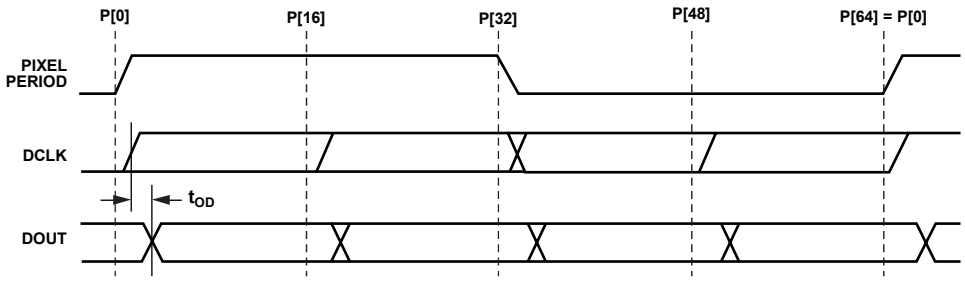
Figure 19. High Speed Timing Default Locations

Digital Data Outputs

The AD9992 data output and DCLK phase are programmable using the DOUTPHASE registers (Address 0x38, Bits [11:0]). DOUTPHASEP (Bits [5:0]) selects any edge location from 0 to 63, as shown in Figure 20. DOUTPHASEN (Bits [11:6]) does not actually program the phase of the data outputs but is used internally and should always be programmed to a value of DOUTPHASEP plus 32 edges. For example, if DOUTPHASEP is set to 0, DOUTPHASEN should be set to 32 (0x20).

Normally, the DOUT and DCLK signals track in phase, based on the contents of the DOUTPHASE registers. The DCLK output phase can also be held fixed with respect to the data outputs by changing the DCLKMODE register high (Address 0x38, Bit 12). In this mode, the DCLK output remains at a fixed phase equal to a delayed version of CLI while the data output phase is still programmable.

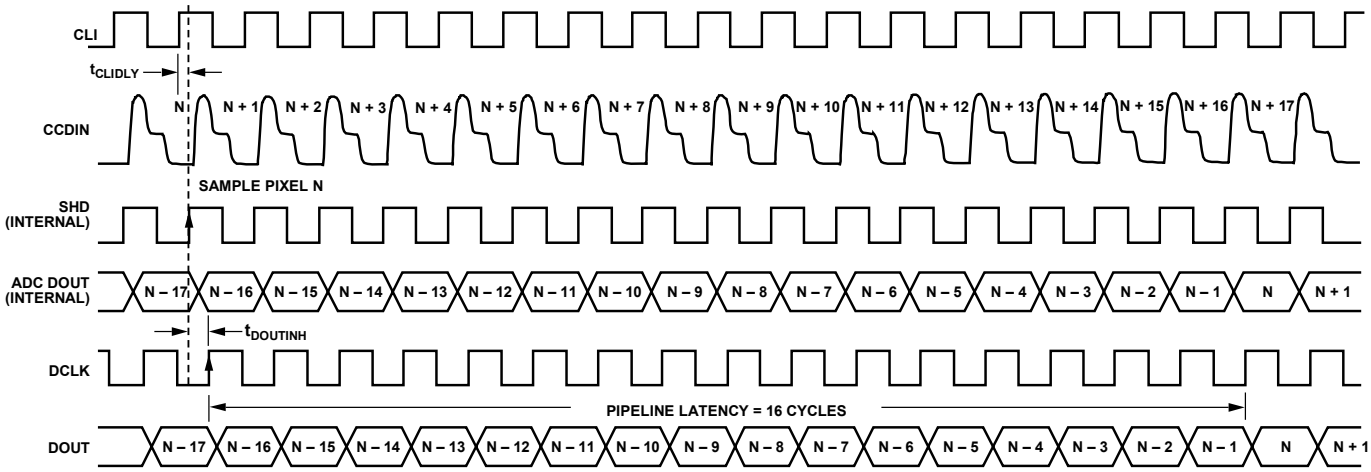
The pipeline delay through the AD9992 is shown in Figure 21. After the CCD input is sampled by SHD, there is a 16-cycle delay until the data is available.



NOTES
1. DATA OUTPUT (DOUT) AND DCLK PHASE ARE ADJUSTABLE WITH RESPECT TO THE PIXEL PERIOD.
2. WITHIN ONE CLOCK PERIOD, THE DATA TRANSITION CAN BE PROGRAMMED TO 64 DIFFERENT LOCATIONS.
3. DCLK CAN BE INVERTED WITH RESPECT TO DOUT BY USING THE DCLKINV REGISTER.

05891-020

Figure 20. Digital Output Phase Adjustment Using DOUTPHASEP Register



NOTES
1. TIMING VALUES SHOWN ARE SHDLOC = 0, WITH DCLKMODE = 0.
2. HIGHER VALUES OF SHD AND/OR DOUT PHASE SHIFTS DOUT TRANSITION TO THE RIGHT, WITH RESPECT TO CLI LOCATION.
3. RECOMMENDED VALUE FOR DOUT PHASE IS TO USE SHPLOC OR UP TO 15 EDGES FOLLOWING SHPLOC.

05891-021

Figure 21. Digital Data Output Pipeline Delay

HORIZONTAL CLAMPING AND BLANKING

The horizontal clamping and blanking pulses of the AD9992 are fully programmable to suit a variety of applications. Individual control is provided for CLPOB, PBLK, and HBLK in the different regions of each field. This allows the dark pixel clamping and blanking patterns to be changed at each stage of the readout to accommodate different image transfer timing and high speed line shifts.

Individual CLPOB and PBLK Patterns

The AFE horizontal timing consists of CLPOB and PBLK, as shown in Figure 22. These two signals are programmed independently using the registers listed in Table 10. The start polarity for the CLPOB (and PBLK) signal is CLPOBPOL (PBLKPOL), and the first and second toggle positions of the pulse are CLPOBTOG1 (PBLKTOG1) and CLPOBTOG2 (PBLKTOG2). Both signals are active low and should be programmed accordingly.

A separate pattern for CLPOB and PBLK can be programmed for each vertical sequence. As described in the Vertical Timing Generation section, several V-sequences can be created, each containing a unique pulse pattern for CLPOB and PBLK. Figure 48 shows how the sequence change positions divide the readout field into different regions. By assigning a different V-sequence to each region, the CLPOB and PBLK signals can change with each change in the vertical timing.

CLPOB and PBLK Masking Areas

Additionally, the AD9992 allows the CLPOB and PBLK signals to be disabled in certain lines in the field without changing any of the existing CLPOB pattern settings.

To use CLPOB (or PBLK) masking, the CLPMASKSTART (PBLKMASKSTART) and CLPMASKEND (PBLKMASKEND) registers are programmed to specify the start and end lines in the field where the CLPOB (PBLK) patterns are ignored. The three sets of start and end registers allow up to three CLPOB (PBLK) masking areas to be created.

The CLPOB and PBLK masking registers are not specific to a certain V-sequence; they are always active for any existing field of timing. During operation, to disable the CLPOB masking feature, these registers must be set to the maximum value of 0x1FFF or a value greater than the programmed VD length.

Note that to disable CLPOB (and PBLK) masking during power-up, it is recommended to set CLPMASKSTART (PBLKMASKSTART) to 8191 and CLPMASKEND (PBLKMASKEND) to 0. This prevents any accidental masking caused by register update events.

Table 10. CLPOB and PBLK Pattern Registers

Register	Length	Range	Description
CLPOBPOL	1b	High/low	Starting polarity of CLPOB for each V-sequence.
PBLKPOL	1b	High/low	Starting polarity of PBLK for each V-sequence.
CLPOBTOG1	13b	0 to 8191 pixel locations	First CLPOB toggle position within line for each V-sequence.
CLPOBTOG2	13b	0 to 8191 pixel locations	Second CLPOB toggle position within line for each V-sequence.
PBLKTOG1	13b	0 to 8191 pixel locations	First PBLK toggle position within line for each V-sequence.
PBLKTOG2	13b	0 to 8191 pixel locations	Second PBLK toggle position within line for each V-sequence.
CLPMASKSTART	13b	0 to 8191 line locations	CLPOB masking area—starting line within field (maximum of three areas).
CLPMASKEND	13b	0 to 8191 line locations	CLPOB masking area—ending line within field (maximum of three areas).
PBLKMASKSTART	13b	0 to 8191 line locations	PBLK masking area—starting line within field (maximum of three areas).
PBLKMASKEND	13b	0 to 8191 line locations	PBLK masking area—ending line within field (maximum of three areas).

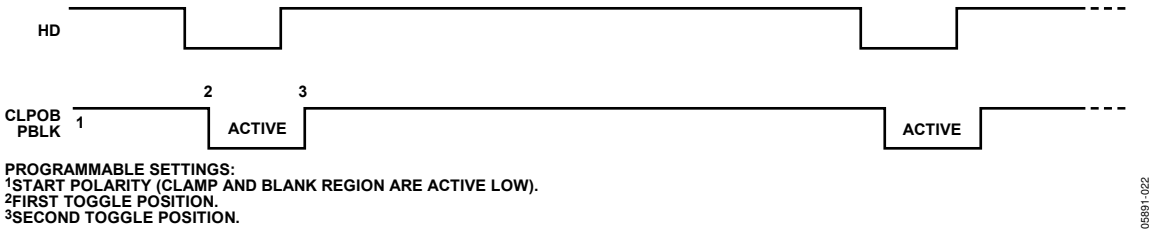


Figure 22. Clamp and Preblank Pulse Placement

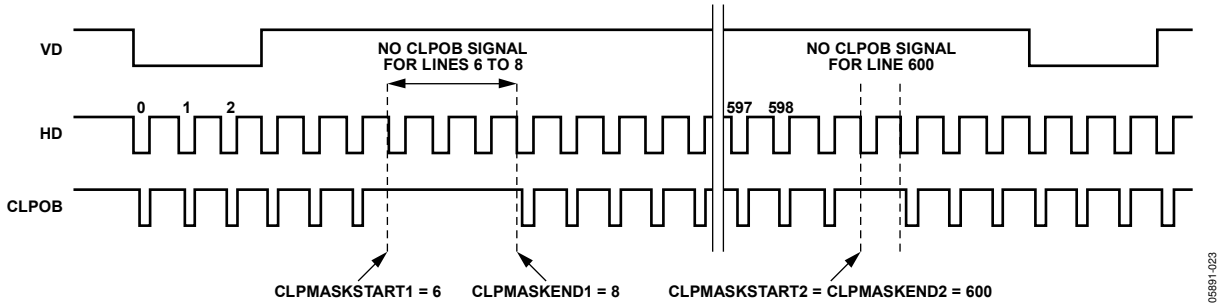


Figure 23. CLPOB Masking Example

Individual HBLK Patterns

The HBLK programmable timing shown in Figure 24 is similar to CLPOB and PBLK; however, there is no start polarity control. Only the toggle positions are used to designate the start and stop positions of the blanking period. Additionally, there are separate masking polarity controls for H1, H2, and HL that designate the polarity of the horizontal clock signals during the blanking period. Setting HBLKMASK_H1 high sets H1, and therefore H3, H5, and H7, low during the blanking, as shown in Figure 25. As with the CLPOB and PBLK signals, HBLK registers are available in each V-sequence, allowing different blanking signals to be used with different vertical timing sequences.

The AD9992 supports three modes of HBLK operation. HBLK Mode 0 supports basic operation and some support for special HBLK patterns. HBLK Mode 1 supports pixel mixing HBLK operation. HBLK Mode 2 supports advanced HBLK operation. The following sections describe each mode in detail. Register parameters are described in detail in Table 11.

HBLK Mode 0 Operation

There are six toggle positions available for HBLK. Normally, only two of the toggle positions are used to generate the standard HBLK interval. However, the additional toggle positions can be used to generate special HBLK patterns, as shown in Figure 26. The pattern in this example uses all six toggle positions to generate two extra groups of pulses during the HBLK interval. By changing the toggle positions, different patterns can be created.

Separate toggle positions are available for even and odd lines. If alternation is not needed, the same values should be loaded into the registers for even (HBLKTOGE) and odd (HBLKTOGO) lines.

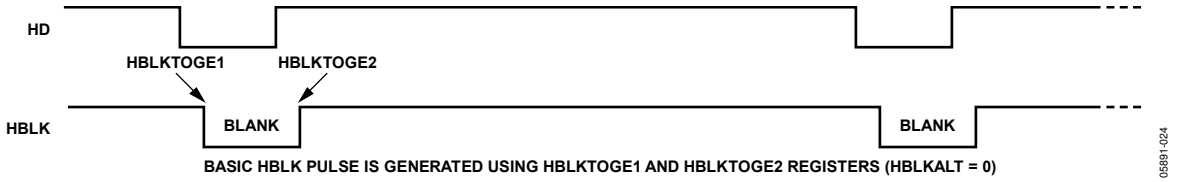


Figure 24. Typical Horizontal Blanking Pulse Placement (HBLKMODE = 0)

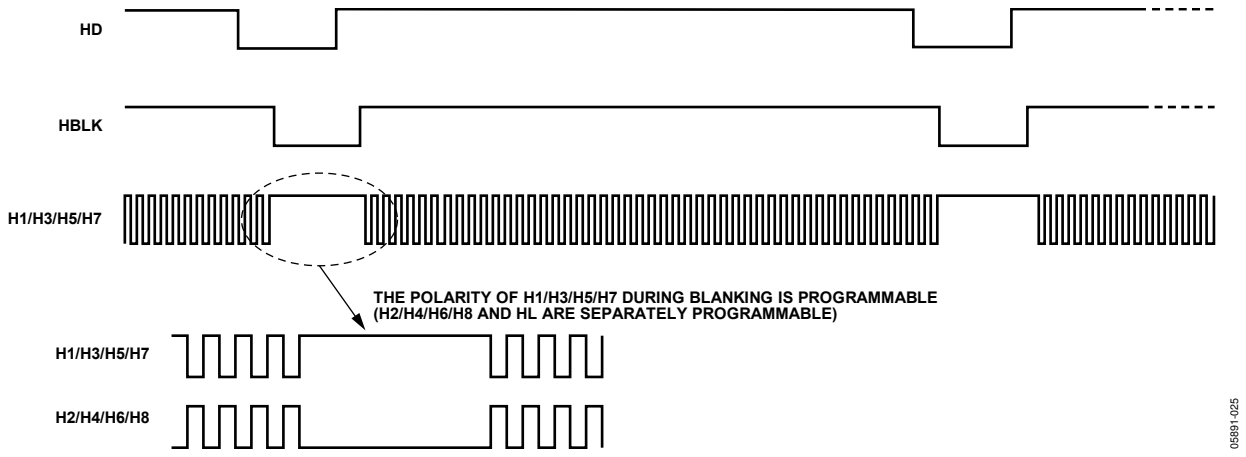


Figure 25. HBLK Masking Polarity Control

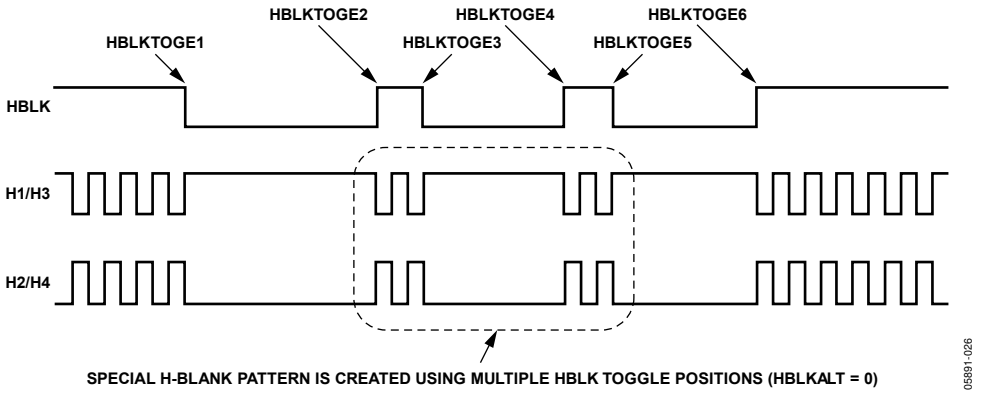


Figure 26. Using Multiple Toggle Positions for HBLK (HBLKMODE = 0)

Table 11. HBLK Pattern Registers

Register	Length	Range	Description
HBLKMODE	2b	0 to 2 HBLK modes	Enables different HBLK toggle position operation. 0: Normal mode. Six toggle positions available for even and odd lines. If even/odd alternation is not needed, set toggles for even/odd the same. 1: Pixel mixing mode. In addition to the six toggle positions, the HBLKSTART, HBLKEND, HBLKLEN, and HBLKREP registers can be used to generate HBLK patterns. If even/odd alternation is not need, set toggles for even/odd the same. 2: Advanced HBLK mode. Divides HBLK interval into six repeat areas. Uses HBLKSTARTA/B/C and RA*H*REPA/B/C registers. 3: Test mode only. Do not access.
HBLKSTART	13b	0 to 8191 pixel location	Start location for HBLK in HBLK Mode 1 and HBLK Mode 2.
HBLKEND	13b	0 to 8191 pixel location	End location for HBLK in HBLK Mode 1 and HBLK Mode 2.
HBLKLEN	13b	0 to 8191 pixels	HBLK length in HBLK Mode 1 and HBLK Mode 2.
HBLKREP	13b	0 to 8191 repetitions	Number of HBLK repetitions in HBLK Mode 1 and HBLK Mode 2.
HBLKMASK_H1	1b	High/low	Masking polarity for H1, H3, H5, H7 during HBLK.
HBLKMASK_H2	1b	High/low	Masking polarity for H2, H4, H6, H8 during HBLK.
HBLKMASK_HL	1b	High/low	Masking polarity for HL during HBLK.
HBLKTOGO1	13b	0 to 8191 pixel location	First HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO2	13b	0 to 8191 pixel location	Second HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO3	13b	0 to 8191 pixel location	Third HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO4	13b	0 to 8191 pixel location	Fourth HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO5	13b	0 to 8191 pixel location	Fifth HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO6	13b	0 to 8191 pixel location	Sixth HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE1	13b	0 to 8191 pixel location	First HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE2	13b	0 to 8191 pixel location	Second HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE3	13b	0 to 8191 pixel location	Third HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE4	13b	0 to 8191 pixel location	Fourth HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE5	13b	0 to 8191 pixel location	Fifth HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE6	13b	0 to 8191 pixel location	Sixth HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
RA0H1REPA/B/C	12b	0 to 15 HCLK pulses for each A, B, and C	HBLK Repeat Area 0. Number of H1 repetitions for HBLKSTARTA/B/C in HBLK Mode 2 for even lines; odd lines defined using HBLKALT_PAT. [3:0] RA0H1REPA. Number of H1 pulses following HBLKSTARTA. [7:4] RA0H1REPB. Number of H1 pulses following HBLKSTARTB. [11:8] RA0H1REPC. Number of H1 pulses following HBLKSTARTC.
RA1H1REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 1. Number of H1 repetitions for HBLKSTARTA/B/C.
RA2H1REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 2. Number of H1 repetitions for HBLKSTARTA/B/C.
RA3H1REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 3. Number of H1 repetitions for HBLKSTARTA/B/C.
RA4H1REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 4. Number of H1 repetitions for HBLKSTARTA/B/C.
RA5H1REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 5. Number of H1 repetitions for HBLKSTARTA/B/C.
RA0H2REPA/B/C	12b	0 to 15 HCLK pulses for each A, B, and C	HBLK Repeat Area 0. Number of H2 repetitions for HBLKSTARTA/B/C in HBLK Mode 2 for even lines; odd lines defined using HBLKALT_PAT. [3:0] RA0H2REPA. Number of H2 pulses following HBLKSTARTA. [7:4] RA0H2REPB. Number of H2 pulses following HBLKSTARTB. [11:8] RA0H2REPC. Number of H2 pulses following HBLKSTARTC.
RA1H2REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 1. Number of H2 repetitions for HBLKSTARTA/B/C.
RA2H2REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 2. Number of H2 repetitions for HBLKSTARTA/B/C.
RA3H2REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 3. Number of H2 repetitions for HBLKSTARTA/B/C.
RA4H2REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 4. Number of H2 repetitions for HBLKSTARTA/B/C.
RA5H2REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 5. Number of H2 repetitions for HBLKSTARTA/B/C.
HBLKSTARTA	13b	0 to 8191 pixel location	HBLK Repeat Area Start Position A for HBLK Mode 2. Set to 8191 if not used.
HBLKSTARTB	13b	0 to 8191 pixel location	HBLK Repeat Area Start Position B for HBLK Mode 2. Set to 8191 if not used.
HBLKSTARTC	13b	0 to 8191 pixel location	HBLK Repeat Area Start Position C for HBLK Mode 2. Set to 8191 if not used.
HBLKALT_PAT1	3b	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 0 pattern, selected from even field repeat areas previously defined.

Register	Length	Range	Description
HBLKALT_PAT2	3b	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 1 pattern.
HBLKALT_PAT3	3b	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 2 pattern.
HBLKALT_PAT4	3b	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 3 pattern.
HBLKALT_PAT5	3b	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 4 pattern.
HBLKALT_PAT6	3b	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 5 pattern.

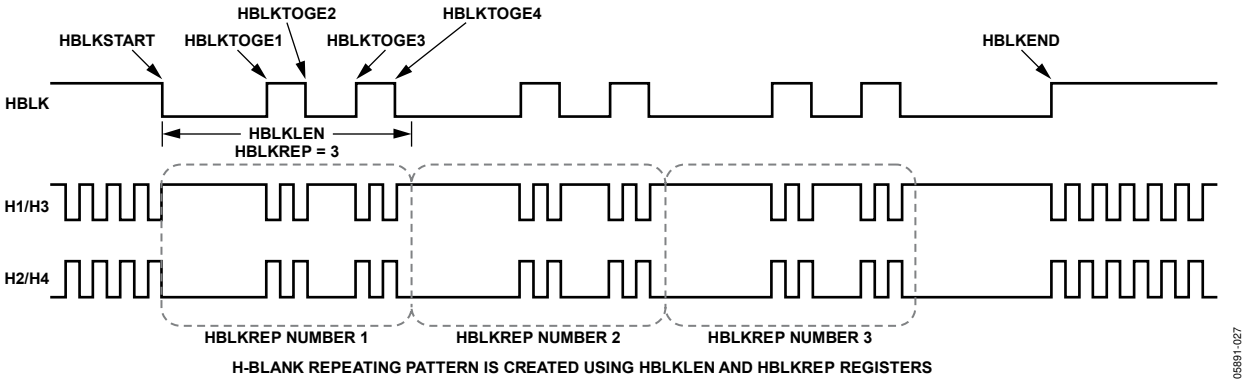


Figure 27. HBLK Repeating Pattern Using HBLKMODE = 1

HBLK Mode 1 Operation

Multiple repeats of the HBLK signal are enabled by setting HBLKMODE to 1. In this mode, the HBLK pattern can be generated using a different set of registers: HBLKSTART, HBLKEND, HBLKLEN, and HBLKREP, along with the six toggle positions (see Figure 27).

Separate toggle positions are available for even and odd lines. If alternation is not needed, the same values should be loaded into the registers for even (HBLKTOGE) and odd (HBLKTOGO) lines.

Generating HBLK Line Alternation

HBLK Mode 0 and HBLK Mode 1 provide the ability to alternate different HBLK toggle positions on even and odd lines. HBLK line alternation can be used in conjunction with V-pattern odd/even alternation or on its own. Separate toggle positions are available for even and odd lines. If even/odd line alternation is not required, the same values should be loaded into the registers for even (HBLKTOGE) and odd (HBLKTOGO) lines.

Increasing H-Clock Width During HBLK

HBLK Mode 0 and HBLK Mode 1 allow the H1 to H8 pulse widths to be increased during the HBLK interval. As shown in Figure 28, the H-clock frequency can be reduced by a factor of 1/2, 1/4, 1/6, 1/8, 1/10, 1/12, and so on, up to 1/30. To enable this feature, the HCLK_WIDTH register (Address 0x34, Bits [7:4]) is set to a value between 1 and 15. When this register is set to 0, the wide HCLK feature is disabled. The reduced frequency occurs only for H1 to H8 pulses that are located within the HBLK area.

The HCLK_WIDTH register is generally used in conjunction with special HBLK patterns to generate vertical and horizontal mixing in the CCD.

Note that the wide HCLK feature is available only in HBLK Mode 0 and HBLK Mode 1. HBLK Mode 2 does not support wide HCLKs.

Table 12. HCLK Width Register

Register	Length	Description
HCLK_WIDTH	4b	Controls H1 to H8 pulse widths during HBLK as a fraction of pixel rate 0: Same frequency as pixel rate 1: 1/2 pixel frequency, that is, doubles the HCLK pulse width 2: 1/4 pixel frequency 3: 1/6 pixel frequency 4: 1/8 pixel frequency 5: 1/10 pixel frequency … 15: 1/30 pixel frequency

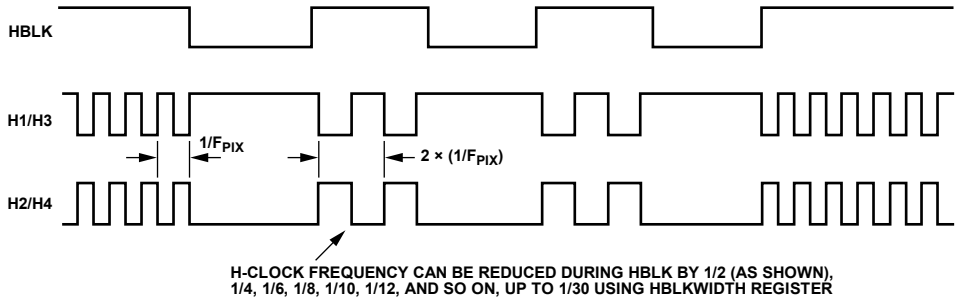


Figure 28. Generating Wide H-Clock Pulses During HBLK Interval

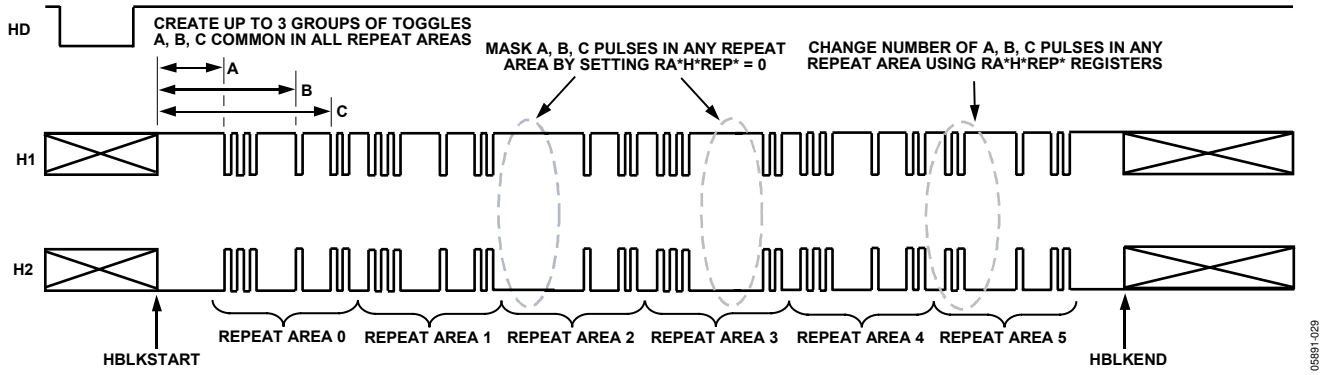


Figure 29. HBLK Mode 2 Operation

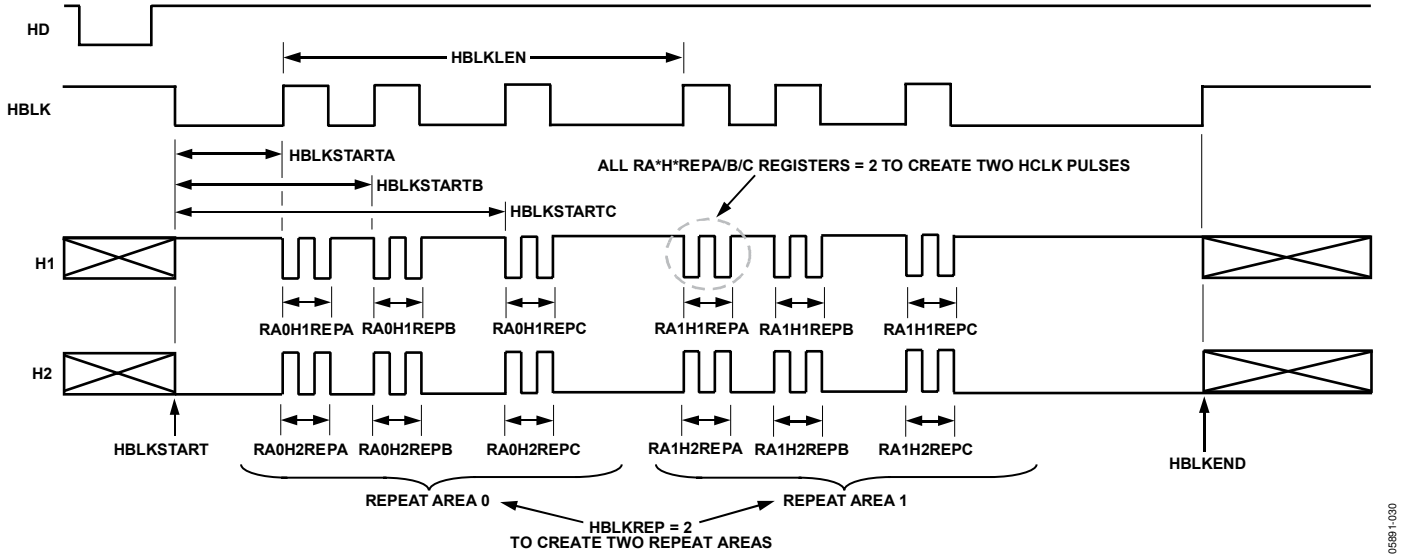


Figure 30. HBLK Mode 2 Registers

HBLK Mode 2 Operation

HBLK Mode 2 allows more advanced HBLK pattern operation. If multiple areas of HCLK pulses that are unevenly spaced apart from one another are needed, HBLK Mode 2 can be used. Using a separate set of registers, HBLK Mode 2 can divide the HBLK region into up to six repeat areas (see Table 11). As shown in Figure 30, each repeat area shares a common group of toggle positions, HBLKSTARTA, HBLKSTARTB, and HBLKSTARTC. However, the number of toggles following each start position can be unique in each repeat area by using the RA*H1REP* and RA*H2REP* registers. As shown in Figure 29, setting the RA*H1REPA/RA*H1REPB/RA*H1REPC or RA*H2REPA/ RA*H2REPB/RA*H2REPC registers to 0 masks HCLK groups from appearing in a particular repeat area. Figure 30 shows only two repeat areas being used, although six are available. It is possible to program a separate number of repeat area repetitions for H1 and H2, but generally the same value is used for both H1 and H2. Figure 30 shows an example of RA0H1REPA/RA0H1REPB/ RA0H1REPC = RA0H2REPA/RA0H2REPB/RA0H2REPC = RA1H1REPA/RA1H1REPB/RA1H1REPC = RA1H2REPA/ RA1H2REPB/RA1H2REPC = 2.

Furthermore, HBLK Mode 2 allows a different HBLK pattern on even and odd lines. The HBLKSTARTA, HBLKSTARTB, and HBLKSTARTC registers, as well as the RA*H1REPA/RA*H1REPB /RA*H1REPC and RA*H2REPA/ RA*H2REPB/RA*H2REPC registers, define operation for the even lines. For separate control of the odd lines, the HBLKALT_PAT registers specify up to six repeat areas on the odd lines by reordering the repeat areas used for the even lines. New patterns are not available, but the order of the previously defined repeat areas on the even lines can be changed for the odd lines to accommodate advanced CCD operation.

HORIZONTAL TIMING SEQUENCE EXAMPLE

Figure 31 shows an example CCD layout. The horizontal register contains 28 dummy pixels, which occur on each line clocked from the CCD. In the vertical direction, there are 10 optical black (OB) lines at the front of the readout and two at the back of the readout. The horizontal direction has four OB pixels in the front and 48 in the back.

Figure 32 shows the basic sequence layout to be used during the effective pixel readout. The 48 OB pixels at the end of each line are used for the CLPOB signals. PBLK is optional and is often used to blank the digital outputs during the HBLK time. HBLK is used during the vertical shift interval.

Because PBLK is used to isolate the CDS input (see the Analog Preblanking section), the PBLK signal should not be used during CLPOB operation. The change in the offset behavior that occurs during PBLK impacts the accuracy of the CLPOB circuitry.

The HBLK, CLPOB, and PBLK parameters are programmed in the V-sequence registers. More elaborate clamping schemes, such as adding in a separate sequence to clamp in the entire shield OB lines, can be used. This requires configuring a separate V-sequence for clocking out the OB lines.

The CLPMASK registers are also useful for disabling the CLPOB on a few lines without affecting the setup of the clamping sequences. It is important that CLPOB be used only during valid OB pixels. During other portions on the frame timing, such as vertical blanking or SG line timing, the CCD does not output valid OB pixels. Any CLPOB pulse that occurs during this time causes errors in clamping operation and changes in the black level of the image.

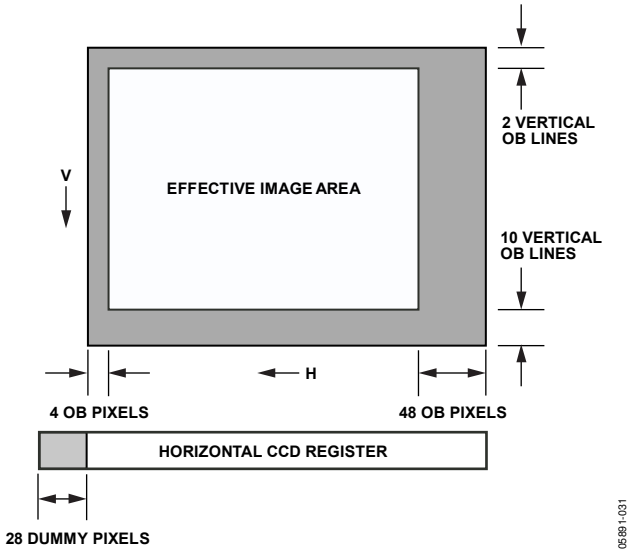


Figure 31. Example CCD Configuration