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Integrated Mixed-Signal Front End (MxFE)

Data Sheet **AD9993**

FEATURES

Quad 14-bit 250 MSPS ADC
SFDR = 83 dBc at 87 MHz input
Dual 14-bit 500 MSPS DAC
SFDR = 75 dBc at 20 MHz output
On-chip PLL clock synthesizer
Low power
1536 mW, 1 GHz master clock, on-chip synthesizer
500 MHz double data rate (DDR)
LVDS interfaces for DACs and ADCs
Small 12 mm × 12 mm lead-free BGA package

APPLICATIONS

Point to point microwave backhaul radios
Wireless repeaters

GENERAL DESCRIPTION

The AD9993 is a mixed-signal front-end (MxFE®) device that integrates four 14-bit ADCs and two 14-bit DACs. Figure 1 shows the block diagram of the MxFE. The MxFE is programmable using registers accessed via a serial peripheral interface (SPI). ADC and DAC datapaths include FIFO buffers to absorb phase differences between LVDS lane clocks and the data converter sampling clocks.

The MxFE DACs are part of the Analog Devices, Inc., high speed CMOS DAC core family. These DACs are designed to be used in wide bandwidth communication system transmitter (Tx) signal chains.

The MxFE ADCs are multistage pipelined CMOS ADC cores designed for use in communications receivers.

FUNCTIONAL BLOCK DIAGRAM

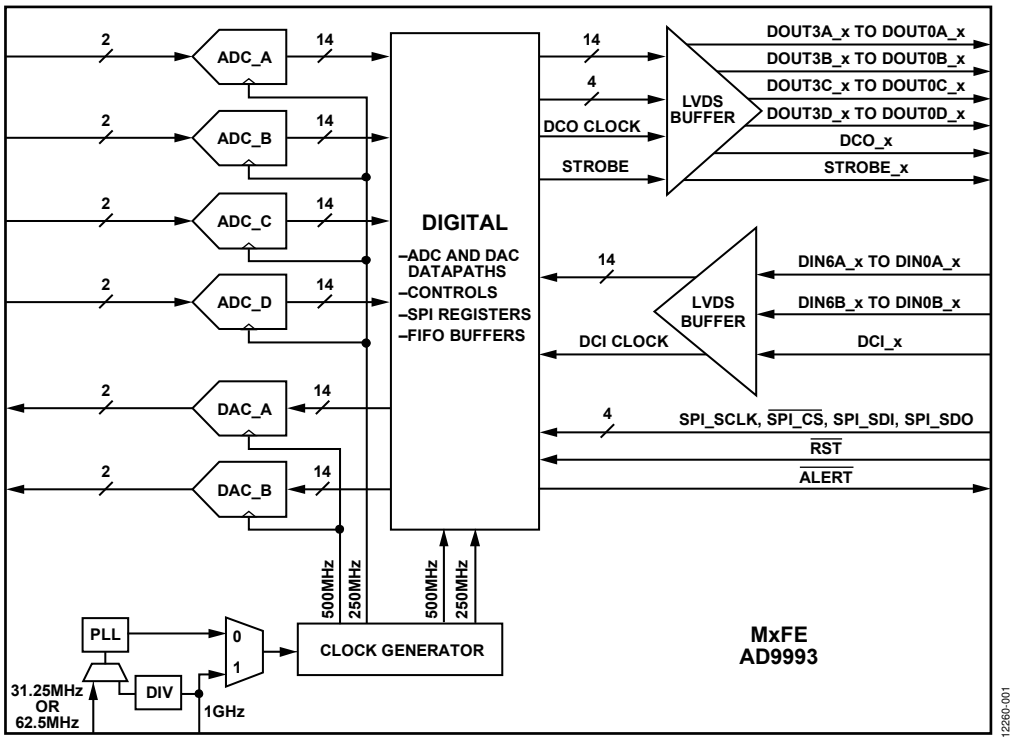

Figure 1.

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5/14—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD = AVDD = 1.8 V, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Tx DAC RESOLUTION			14		Bits
Tx DAC OUTPUT CHARACTERISTICS					
Offset Error			±0.5		% FSR
Gain Error			±2.0		% FSR
Full-Scale Output Current (I_{OUTFS})			20.0		mA
Output Compliance Voltage Range	CML_A, CML_B connected to AVSS, setting of DAC_VCM_VREF_BIT[2:0] following reset	−0.5		+0.5	V
Output Compliance Voltage Range	CML_A, CML_B connected to a bypass capacitor, DAC_VCM_VREF_BIT[2:0] set to 010	0.0		1.0	V
Output Resistance			10		MΩ
Tx DAC TEMPERATURE DRIFT					
Gain	Gain using on-chip VREF_DAC		±85		ppm/°C
Reference Voltage (VREF_DAC)	On-chip VREF_DAC		±215		ppm/°C
REFERENCE (VREF_DAC)					
Internal Reference Voltage		0.95	1.0	1.05	V
Rx ADC RESOLUTION			14		Bits
Rx ADC CHARACTERISTICS					
Gain Error			±1.0		% FSR
Peak-to-Peak Differential Input Voltage Range	Setting of VREF_FS_ADJ[4:0] at reset		1.75		V p-p
Input Capacitance			2.5		pF
Rx ADC FULL-SCALE V_{REF} ADJUSTMENT		1.383	1.75	2.087	V
COMMON-MODE VOLTAGE REFERENCE (A_CML, B_CML, C_CML, D_CML)					
ADC Common-Mode Voltage Output	ADC inputs are not self biased	0.84	0.9	0.96	V
ANALOG SUPPLY VOLTAGES					
AVDD33		3.14	3.3	3.47	V
AVDD		1.71	1.8	1.89	V
DIGITAL SUPPLY VOLTAGES					
DVDD		1.62	1.8	1.98	V
POWER CONSUMPTION					
Single Tone Input, Single Tone Output			1536		mW
AVDD33			55		mA
AVDD			65		mA
DVDD			210		mA
Power-Down Mode			10.0		mA
OPERATING RANGE		−40	+25	+85	°C

AC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD = AVDD = 1.8 V, DAC sampling rate = 500 MSPS and ADC sampling rate = 250 MSPS, unless otherwise specified.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DAC OUTPUT					
Spurious-Free Dynamic Range (SFDR)	f_{OUT} = 20 MHz		75		dBc
Two Tone Intermodulation Distortion (IMD3)	f_{OUT} = 80 MHz		65		dBc
Noise Spectral Density (NSD), Single Tone	f_{OUT} = 80 MHz		−160		dBm/Hz
256-QAM Adjacent Channel Power (ACP)	f_{CENTER} = 50 MHz, single carrier, 3.375 MHz offset frequency		76		dBc
ADC INPUT					
Signal to Noise Ratio (SNR)	Measured with −1.0 dBFS sine wave input				
f_{IN} = 87 MHz			70		dBc
Spurious-Free Dynamic Range (SFDR)	Measured with −1.0 dBFS sine wave input				
f_{IN} = 10 MHz			86		dBc
f_{IN} = 87 MHz			83		dBc
Two-Tone IMD3	f_{IN1} = 89 MHz, f_{IN2} = 92 MHz, A_{IN} = −12 dBFS		90		dBc
Full Power Bandwidth	Bandwidth of operation in which proper ADC performance can be achieved		1000		MHz

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD33 = 3.3 V, DVDD = AVDD = 1.8 V, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL					
Input V_{IN} Logic High			1.8		V
Input V_{IN} Logic Low			0.0		V
CMOS OUTPUT LOGIC LEVEL					
Output V_{OUT} Logic High		1.2			V
Output V_{OUT} Logic Low				0.8	V
ADC AND DAC LVDS DATA INTERFACES					
ADC LVDS Transmitter Outputs					
DCO_P/DCO_N to Data Skew (t_{SKEW})	Data to DDR DCO_P/DCO_N transition delay	350			ps
Output Voltage High, V_{OH}, Single Ended	Applies to output voltage, positive and negative, V_{OUTP} and V_{OUTN}		1375		mV
Output Voltage Low, V_{OL}, Single Ended	Applies to V_{OUTP} and V_{OUTN}		1025		mV
Output Differential Voltage			200		mV
Output Offset Voltage			1200		mV
DAC LVDS Receiver Inputs	Specifications apply to DAC data inputs and DCI_P/DCI_N				
Input Voltage Range, Single Ended	Applies to input voltage, positive and negative, V_{INP} and V_{INN}	825		1575	mV
Input Differential Threshold		−100		+100	mV
Input Differential Hysteresis			25		mV
Receiver Differential Input Impedance		85		115	Ω

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK INPUT (CLKP, CLKN)					
Differential Peak to Peak Voltage			350		mV
Common Mode Voltage			1.2		V
Master Clock Frequency		200		1000	MHz
REFCLK Input (REFCLK)					
Input V_{IN} Logic High			1.8		V
Input V_{IN} Logic Low			0.0		V
REFCLK Frequency			31.25 or 62.5		MHz
SERIAL PERIPHERAL INTERFACE (SPI)					
SPI_SCLK Frequency				25	MHz
SPI_SCLK Pulse Width High		10			ns
SPI_SCLK Pulse Width Low		10			ns
Setup Time, SPI_SDI to SPI_SCLK Rising Edge		2			ns
Hold Time, SPI_SCLK Rising Edge to SPI_SDI		2			ns
Setup Time, $\overline{\text{SPI\_CS}}$ to SPI_SCLK Rising Edge		2			ns
Hold Time, SPI_SCLK Rising Edge to $\overline{\text{SPI\_CS}}$		2			ns
Data Valid, SPI_SCLK Falling Edge to SPI_SDO		2			ns

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
AVSS to DVSS	−0.3 V to +0.3 V
AVDD33 to AVSS, DVSS	−0.3 V to +3.9 V
AVDD to AVSS, DVSS	−0.3 V to +2.2 V
DVDD to DVSS, AVSS	−0.3 V to +2.2 V
CP, A_VINP, A_VINN, B_VINP, B_VINN, C_VINP, C_VINN, D_VINP, D_VINN, IBIAS_TEST to AVSS	−0.3 V to AVDD + 0.3 V
VREF_DAC, FSAJ_A, FSAJ_B, CML_A, CML_B, A_CML, B_CML, B_CML, D_CML to AVSS	−0.3 V to AVDD + 0.3 V
IOUTA_P, IOUTA_N, IOUTB_P, IOUTB_N to AVSS	−0.3 V to AVDD + 0.3 V
CLKP, CLKN, REFCLK to AVSS	−0.3 V to AVDD + 0.3 V
PDWN, $\overline{\text{ALERT}}$, $\overline{\text{RST}}$, MODE, SPI_SCLK, $\overline{\text{SPI\_CS}}$, SPI_SDI, SPI_SDO to DVSS	−0.3 V to DVDD + 0.3 V
LVDS Data Inputs to DVSS	−0.3 V to DVDD + 0.3 V
LVDS Data Outputs to DVSS	−0.3 V to DVDD + 0.3 V
STROBE_P, STROBE_N to DVSS	−0.3 V to DVDD + 0.3 V
DCI_N, DCI_P, DCO_N, DCO_P	−0.3 V to DVDD + 0.3 V
Junction Temperature	125°C
Storage Temperature Range	−65°C to +160°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 5. Thermal Resistances and Characterization Parameters

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	ψ_{JT}	ψ_{JB}	Unit
196-Ball CSP_BGA	27.0	15.4	5.38	0.11	15.0	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	AVSS	CLKP	AVSS	D_VINP	C_CML	C_VINP	AVSS	AVSS	B_VINP	B_CML	A_VINP	AVSS	IBIAS_TEST	AVSS
B	CLKN	REFCLK	AVSS	D_VINN	D_CML	C_VINN	AVSS	AVSS	B_VINN	A_CML	A_VINN	AVSS	IOUTA_N	IOUTA_P
C	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVDD33	AVDD33
D	LDO15	CP	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	IOUTB_N	IOUTB_P
E	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD
F	PDWN	$\overline{\text{ALERT}}$	$\overline{\text{RST}}$	MODE	AVDD33	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	VREF_DAC	FSAJ_B	FSAJ_A
G	SPI_SCLK	$\overline{\text{SPI\_CS}}$	SPI_SDI	SPI_SDO	DVDD	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVDD	CML_B	CML_A
H	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS
J	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD
K	DIN6B_N	DIN4B_N	DIN1B_N	DOUT3D_P	DOUT3D_N	DOUT3C_P	DCO_N	DCO_P	DOUT3B_P	DOUT3A_N	DOUT3A_P	DIN1A_N	DIN4A_N	DIN6A_N
L	DIN6B_P	DIN4B_P	DIN1B_P	DOUT1D_N	DOUT2D_N	DOUT1C_N	DOUT3C_N	DOUT3B_N	DOUT1B_N	DOUT2A_N	DOUT1A_N	DIN1A_P	DIN4A_P	DIN6A_P
M	DIN5B_N	DIN3B_N	DIN3B_P	DOUT1D_P	DOUT2D_P	DOUT1C_P	STROBE_N	STROBE_P	DOUT1B_P	DOUT2A_P	DOUT1A_P	DIN3A_N	DIN3A_P	DIN5A_N
N	DIN5B_P	DIN2B_N	DIN0B_N	DOUT0D_N	DOUT0C_N	DOUT2C_N	DVSS	DVSS	DOUT2B_N	DOUT0B_N	DOUT0A_N	DIN0A_N	DIN2A_N	DIN5A_P
P	DVSS	DIN2B_P	DIN0B_P	DOUT0D_P	DOUT0C_P	DOUT2C_P	DCI_N	DCI_P	DOUT2B_P	DOUT0B_P	DOUT0A_P	DIN0A_P	DIN2A_P	DVSS

12260-002

Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1, A3, A7, A8, A12, A14, B3, B7, B8, B12, C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, F6, F7, F8, F9, F10, F11, G6, G7, G8, G9, G10, G11	AVSS	Analog Ground.
A2	CLKP	External Master Clock Input Positive.
A4	D_VINP	ADC D Input Voltage Positive.
A5	C_CML	Common-Mode Level Bias Voltage Output ADC C.
A6	C_VINP	ADC C Input Voltage Positive.
A9	B_VINP	ADC B Voltage Input Positive.
A10	B_CML	Common-Mode Level Bias Voltage Output for ADC B.

Pin No.	Mnemonic	Description
A11	A_VINP	ADC A Voltage Input Positive.
A13	IBIAS_TEST	Test. Connect to ground.
B1	CLKN	External Master Clock Input Negative
B2	REFCLK	On-Chip PLL Synthesizer Reference Clock Input.
B4	D_VINN	ADC D Input Voltage Negative.
B5	D_CML	Common-Mode Level Bias Voltage Output ADC D.
B6	C_VINN	ADC C Input Voltage Negative.
B9	B_VINN	ADC B Voltage Input Negative.
B10	A_CML	Common-Mode Level Bias Voltage Output for ADC A.
B11	A_VINN	ADC A Voltage Input Negative.
B13	IOUTA_N	DAC A Output Current Negative.
B14	IOUTA_P	DAC A Output Current Positive.
C13, C14, F5	AVDD33	3.3 V Analog Power Supply.
D1	LDO15	On-Chip Regulator Output. Bypass with 4.7 µF capacitor to ground.
D2	CP	Connection for On-Chip PLL Optional External Portion of Loop Filter.
D13	IOUTB_N	DAC B Output Current Negative.
D14	IOUTB_P	DAC B Output Current Positive.
E1, E2, E3, E4, E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, G12	AVDD	1.8 V Analog Power Supply.
F1	PDWN	Power-Down. Set to 1 to place the device in low power mode.
F2	$\overline{\text{ALERT}}$	Active Low Alarm Indicator Output, Open Drain.
F3	$\overline{\text{RST}}$	Reset Input, Active Low.
F4	MODE	Connect to ground.
F12	VREF_DAC	DAC A and DAC B Reference Voltage Input/Output.
F13	FSAJ_B	DAC B Full-Scale Current Output Adjust.
F14	FSAJ_A	DAC A Full-Scale Current Output Adjust.
G1	SPI_SCLK	SPI Clock.
G2	$\overline{\text{SPI\_CS}}$	SPI Chip Select, Active Low.
G3	SPI_SDI	SPI Serial Data Input.
G4	SPI_SDO	SPI Serial Data Output.
G5, J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14	DVDD	1.8 V Digital Supply.
G13	CML_B	DAC B Common-Mode Control. Connect to ground for DAC bias < 0.5 V. Connect a 0.1 µF capacitor between CML_B and ground for other DAC bias values ≥ 0.5 V.
G14	CML_A	DAC A Common-Mode Control. Connect to ground for DAC bias < 0.5 V. Connect a 0.1 µF capacitor between CML_A and ground for other DAC bias values ≥ 0.5 V.
H1, H2, H3, H4, H5, H6, H7, H8, H9, H10, H11, H12, H13, H14, N7, N8, P1, P14	DVSS	Digital Ground.
K1	DIN6B_N	DAC B Data Input Lane 6 Negative.
K2	DIN4B_N	DAC B Data Input Lane 4 Negative.
K3	DIN1B_N	DAC B Data Input Lane 1 Negative.
K4	DOUT3D_P	ADC D Data Output Lane 3 Positive.
K5	DOUT3D_N	ADC D Data Output Lane 3 Negative.
K6	DOUT3C_P	ADC C Data Output Lane 3 Positive.
K7	DCO_N	LVDS Data Clock Output Negative.
K8	DCO_P	LVDS Data Clock Output Positive.
K9	DOUT3B_P	ADC B Data Output Lane 3 Positive.
K10	DOUT3A_N	ADC A Data Output Lane 3 Negative.
K11	DOUT3A_P	ADC A Data Output Lane 3 Positive.
K12	DIN1A_N	DAC A Data Input Lane 1 Negative.
K13	DIN4A_N	DAC A Data Input Lane 4 Negative.
K14	DIN6A_N	DAC A Data Input Lane 6 Negative.

Pin No.	Mnemonic	Description
L1	DIN6B_P	DAC B Data Input Lane 6 Positive.
L2	DIN4B_P	DAC B Data Input Lane 4 Positive.
L3	DIN1B_P	DAC B Data Input Lane 1 Positive.
L4	DOUT1D_N	ADC D Data Output Lane 1 Negative.
L5	DOUT2D_N	ADC D Data Output Lane 2 Negative.
L6	DOUT1C_N	ADC C Data Output Lane 1 Negative.
L7	DOUT3C_N	ADC C Data Output Lane 3 Negative.
L8	DOUT3B_N	ADC B Data Output Lane 3 Negative.
L9	DOUT1B_N	ADC B Data Output Lane 1 Negative.
L10	DOUT2A_N	ADC A Data Output Lane 2 Negative.
L11	DOUT1A_N	ADC A Data Output Lane 1 Negative.
L12	DIN1A_P	DAC A Data Input Lane 1 Positive.
L13	DIN4A_P	DAC A Data Input Lane 4 Positive.
L14	DIN6A_P	DAC A Data Input Lane 6 Positive.
M1	DIN5B_N	DAC B Data Input Lane 5 Negative.
M2	DIN3B_N	DAC B Data Input Lane 3 Negative.
M3	DIN3B_P	DAC B Data Input Lane 3 Positive.
M4	DOUT1D_P	ADC D Data Output Lane 1 Positive.
M5	DOUT2D_P	ADC D Data Output Lane 2 Positive.
M6	DOUT1C_P	ADC C Data Output Lane 1 Positive.
M7	STROBE_N	LVDS Data Output Strobe Negative.
M8	STROBE_P	LVDS Data Output Strobe Positive.
M9	DOUT1B_P	ADC B Data Output Lane 1 Positive.
M10	DOUT2A_P	ADC A Data Output Lane 2 Positive.
M11	DOUT1A_P	ADC A Data Output Lane 1 Positive.
M12	DIN3A_N	DAC A Data Input Lane 3 Negative.
M13	DIN3A_P	DAC A Data Input Lane 3 Positive.
M14	DIN5A_N	DAC A Data Input Lane 5 Negative.
N1	DIN5B_P	DAC B Data Input Lane 5 Positive.
N2	DIN2B_N	DAC B Data Input Lane 2 Negative.
N3	DIN0B_N	DAC B Data Input Lane 0 Negative.
N4	DOUT0D_N	ADC D Data Output Lane 0 Negative.
N5	DOUT0C_N	ADC C Data Output Lane 0 Negative.
N6	DOUT2C_N	ADC C Data Output Lane 2 Negative.
N9	DOUT2B_N	ADC B Data Output Lane 2 Negative.
N10	DOUT0B_N	ADC B Data Output Lane 0 Negative.
N11	DOUT0A_N	ADC A Data Output Lane 0 Negative.
N12	DIN0A_N	DAC A Data Input Lane 0 Negative.
N13	DIN2A_N	DAC A Data Input Lane 2 Negative.
N14	DIN5A_P	DAC A Data Input Lane 5 Positive.
P2	DIN2B_P	DAC B Data Input Lane 2 Positive.
P3	DIN0B_P	DAC B Data Input Lane 0 Positive.
P4	DOUT0D_P	ADC D Data Output Lane 0 Positive.
P5	DOUT0C_P	ADC C Data Output Lane 0 Positive.
P6	DOUT2C_P	ADC C Data Output Lane 2 Positive.
P7	DCI_N	LVDS Data Clock Input Negative.
P8	DCI_P	LVDS Data Clock Input Positive.
P9	DOUT2B_P	ADC B Data Output Lane 2 Positive.
P10	DOUT0B_P	ADC B Data Output Lane 0 Positive.
P11	DOUT0A_P	ADC A Data Output Lane 0 Positive.
P12	DIN0A_P	DAC A Data Input Lane 0 Positive.
P13	DIN2A_P	DAC A Data Input Lane 2 Positive.

TYPICAL PERFORMANCE CHARACTERISTICS

RECEIVER ADC PERFORMANCE

f_{ADC} = 250 MHz, unless otherwise specified.

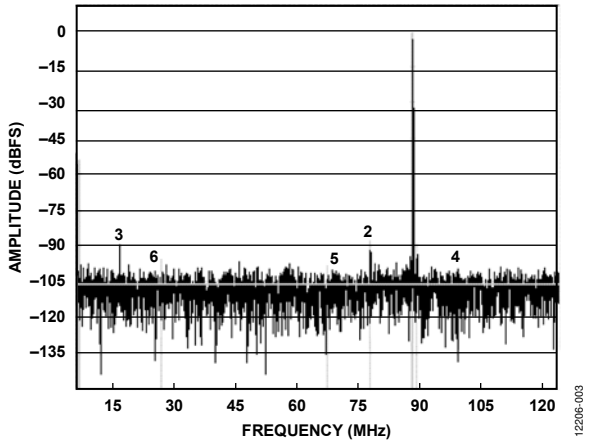

Figure 3. Single Tone FFT, f_{IN} = 87 MHz

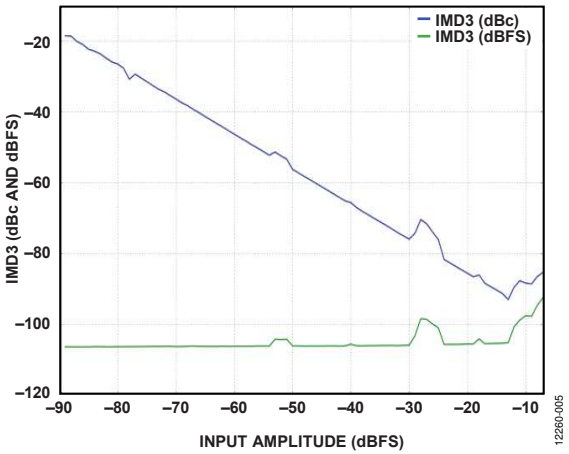

Figure 6. Two Tone IMD3 vs. Input Amplitude (A_{IN}), f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz

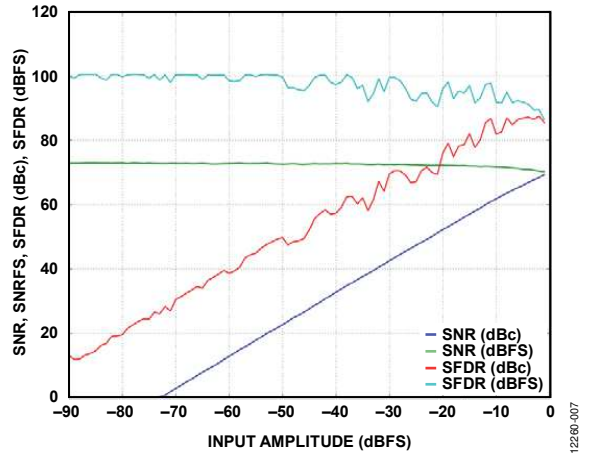

Figure 4. Single Tone SNR and SFDR vs. Input Amplitude (A_{IN}), f_{IN} = 87 MHz

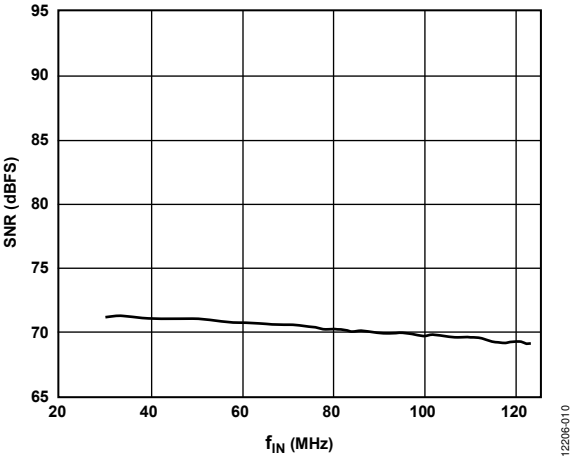

Figure 7. Single Tone SNR vs. Input Frequency (f_{IN})

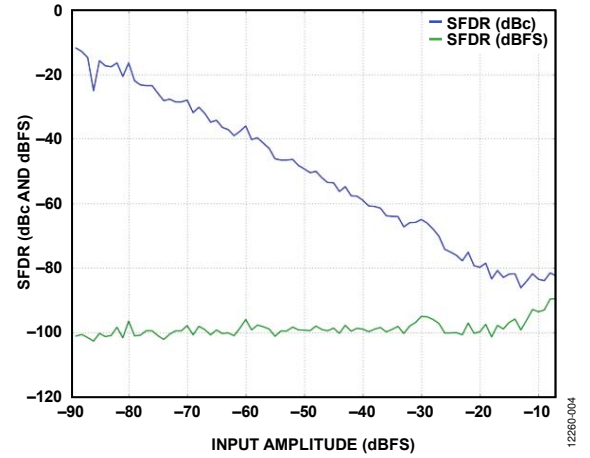

Figure 5. Two Tone SFDR vs. Input Amplitude (A_{IN}), f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz

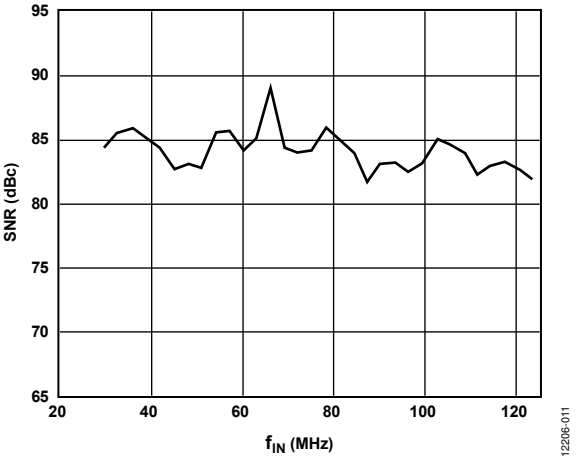

Figure 8. Single Tone SNR vs. Input Frequency (f_{IN})

f_{ADC} = 250 MHz, unless otherwise specified.

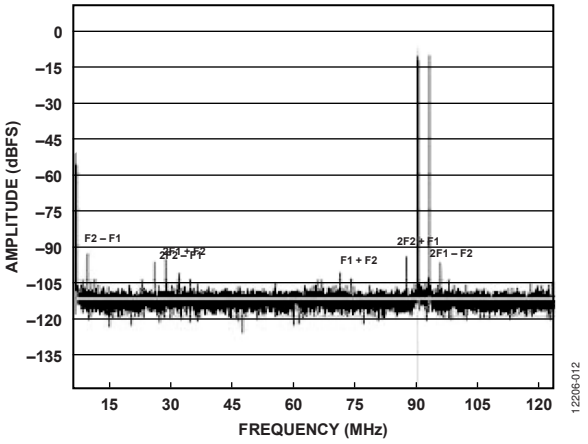

Figure 9. Two Tone FFT, f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz

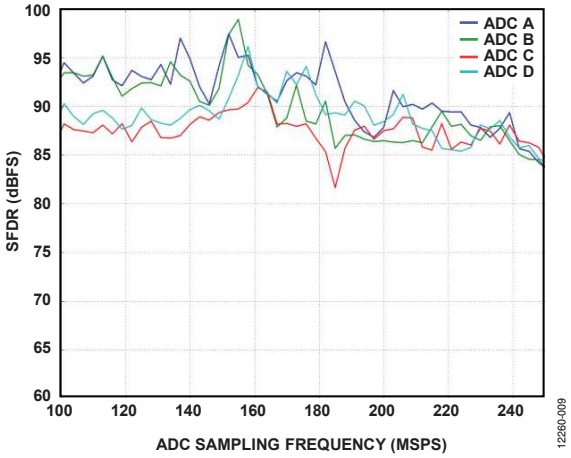

Figure 11. Single Tone SFDR vs. ADC Sampling Freqency (f_{ADC}), f_{IN} = 90.0 MHz, All Four ADCs

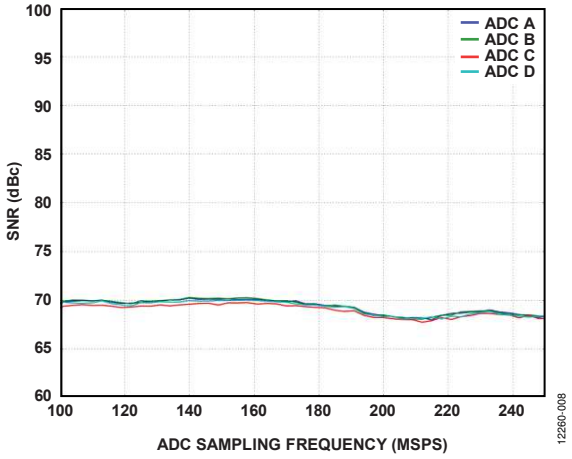

Figure 10. Single Tone SNR vs. ADC Sampling Freqency (f_{ADC}), f_{IN} = 90.0 MHz, All Four ADCs

TRANSMITTER DAC PERFORMANCE

f_{DAC} = 500 MHz, unless otherwise specified.

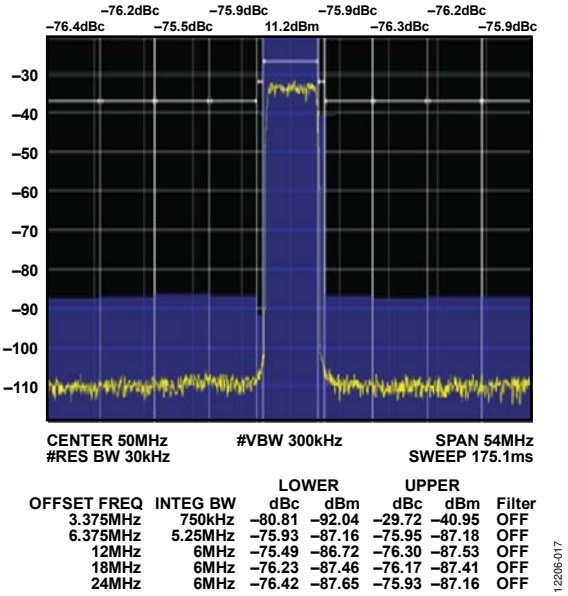

Figure 12. 5 MHz Bandwidth 256-QAM Adjacent Channel Power

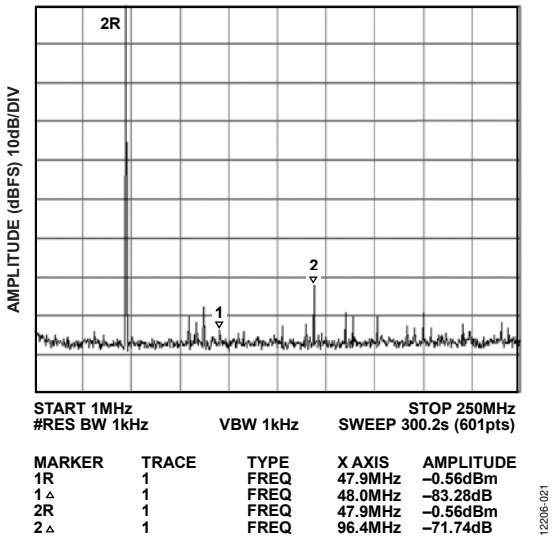

Figure 15. 1st Nyquist Zone Output Spectrum, f_{OUT} = 48 MHz

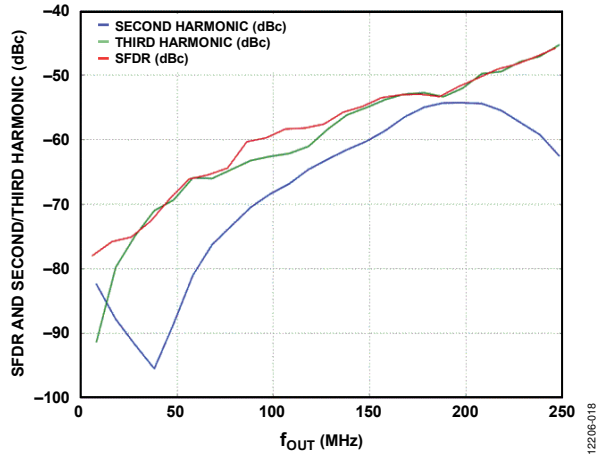

Figure 13. SFDR, 2nd and 3rd Harmonics vs. f_{OUT}, Maximum I_{OUTFS} (DAC Gain)

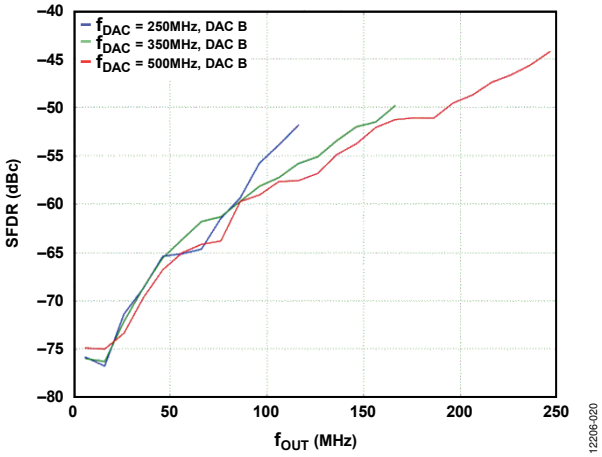

Figure 16. SFDR at Three DAC Sampling Frequencies (f_{DAC}) vs. f_{OUT}

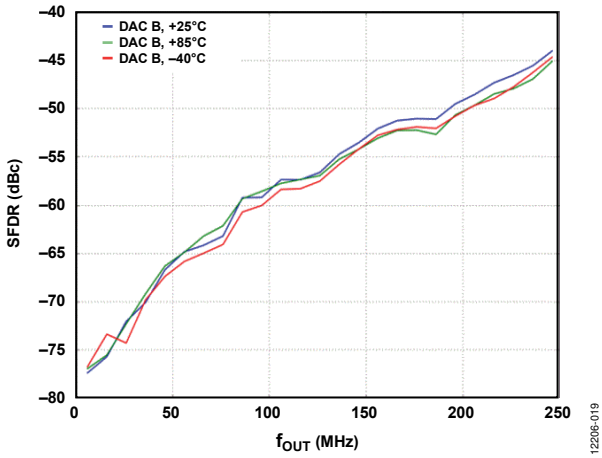

Figure 14. SFDR at Three Temperatures vs. f_{OUT}

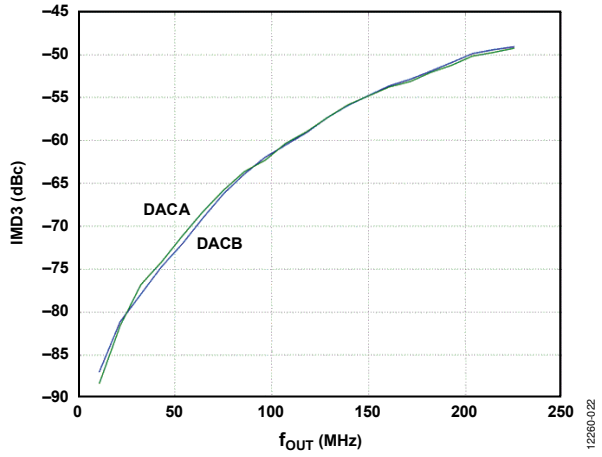

Figure 17. IMD3 vs. f_{OUT}, Both DACs

f_{DAC} = 500 MHz, unless otherwise specified.

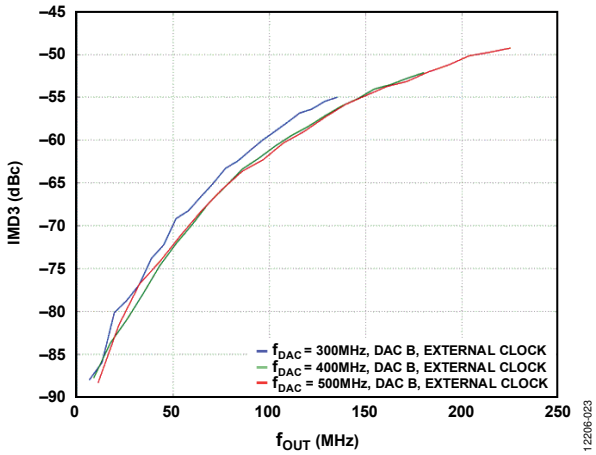

Figure 18. IMD3 at Three DAC Sampling Frequencies (f_{DAC}) vs. f_{OUT}

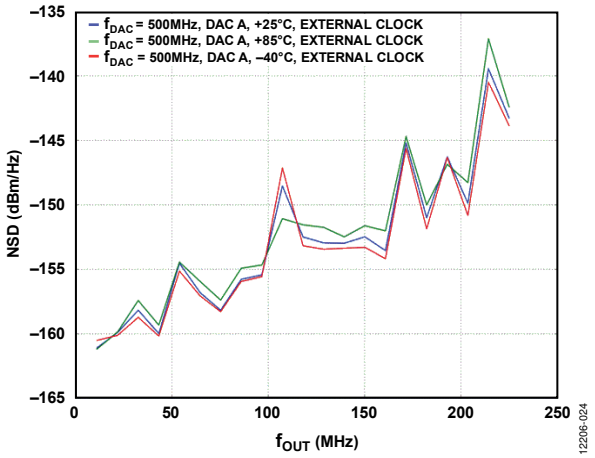

Figure 19. NSD at Three Temperatures vs. f_{OUT}

TERMINOLOGY

Linearity Error (Integral Nonlinearity or INL)
INL is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A digital-to-analog converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
Offset error is the deviation of the output current from the ideal of zero. For IOUTx_P, 0 mA output is expected when the inputs are all 0s. For IOUTx_N, 0 mA output is expected when all inputs are set to 1.

Gain Error
Gain error is the difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1, minus the output when all inputs are set to 0. The ideal gain is calculated using the measured VREF. Therefore, the gain error does not include effects of the reference.

Output Compliance Voltage
Output compliance voltage is the range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels (dB), between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Noise Spectral Density (NSD)
Noise spectral density is the average noise power normalized to a 1 Hz bandwidth, with the DAC converting and producing an output tone.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Signal to Noise and Distortion (SINAD)
The ratio of the total signal power level (wanted signal + noise + distortion or SND) to unwanted signal power (noise + distortion or ND).

THEORY OF OPERATION

PRODUCT DESCRIPTION

Figure 1 shows a block diagram of the MxFE. This product integrates four 14-bit ADCs and two 14-bit DACs. The DAC data interface consists of six DDR LVDS data lanes for each DAC and a shared DCI_P/DCI_N clock (hereafter referred to as DCI). The ADC data interface consists of four DDR LVDS data lanes for each ADC with a shared DCO_P/DCO_N clock (hereafter referred to as DCO) and a shared STROBE output. The MxFE control and status registers are written/read via an SPI interface. ADC and DAC datapaths include FIFO buffers to absorb phase differences between LVDS lane timing and the data converter sampling clocks. Internal AD9993 clock signals can be developed from an external clock signal or from the output of an on-chip PLL frequency multiplier driven by an external reference oscillator.

SPI PORT

The AD9993 provides a 4-wire synchronous serial communications SPI port that allows easy interfacing to ASICs, FPGAs, and industry-standard microcontrollers. The interface facilitates read/write access to all registers that configure the AD9993. Its data rate can be up to 25 MHz.

SPI Port Signals

SPI_SCLK (serial clock) is the serial shift clock. The serial clock pin synchronizes data to and from the device and runs the internal state machines. All address and input data bits are sampled on the rising edge of SPI_SCLK. All output data is driven out on the falling edge of SPI_SCLK.

$\overline{\text{SPI\_CS}}$ (chip select) is an active low control signal used by the SPI master to select the AD9993 SPI port. When $\overline{\text{SPI\_CS}}$ is high, SPI_SDO is in a high impedance state. During the communication cycle, chip select must remain low.

SPI_SDI (serial data input) is the address and data input, sampled on the rising edge of SPI_SCLK.

SPI_SDO (serial data output) is the data output pin. Data is shifted out on the falling edge of SCLK

Figure 20 shows a timing diagram for a single byte MSB first AD9993 SPI write operation. Each AD9993 register address is an 8-bit value. During the first SPI_SCLK cycle, SPI_SDI = 0, indicating that the operation is a data write. SPI_SDI is always held low for the next two clock cycles. The next 13 clock cycles are the first register address. The next eight clock cycles contain data to be written. The write operation ends when $\overline{\text{SPI\_CS}}$ goes high. In this example, data for one 8-bit register is written. Multiple registers can be written in a single write operation by keeping $\overline{\text{SPI\_CS}}$ low for multiple byte periods. The register address is automatically updated using an address counter as bytes are written while $\overline{\text{SPI\_CS}}$ remains low.

Figure 21 depicts an MSB first register read operation. Register data from the AD9993 appears on SPI_SDO starting on the SPI_SCLK cycle following the last bit of the 16-bit instruction header on SPI_SDI. Multiple registers can be read in a single read operation by keeping $\overline{\text{SPI\_CS}}$ low for multiple byte periods.

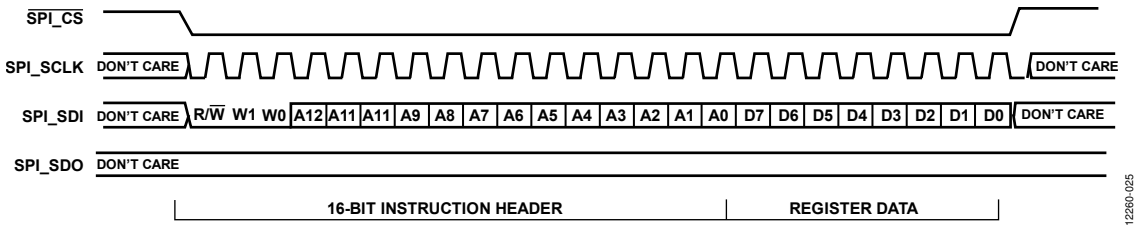

Figure 20. 4-Wire SPI Interface Timing, MSB First Write

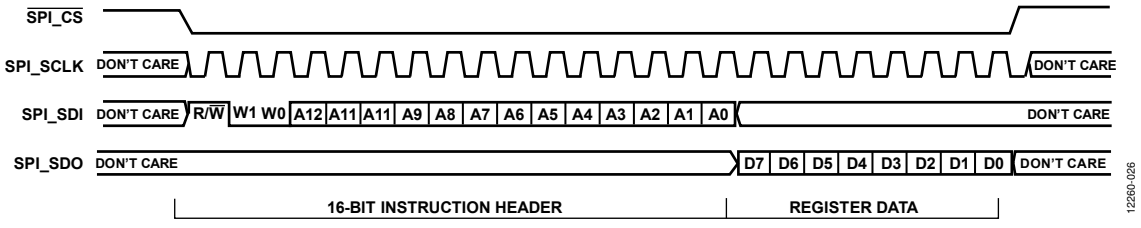

Figure 21. 4-Wire SPI Interface Timing, MSB First Read

SPI CONFIGURATION PROGRAMMING

The SPI_CONFIG register controls AD9993 SPI interface operation. By default, the SPI bus operates MSB first. In MSB fist mode, the register address counter decrements automatically during multiple byte reads or writes. The SPI bus can be configured to run LSB first by setting the SPI_LSB_FIRSTx bits to 1. During LSB first multiple register read or write operations, the register address counter is incremented automatically. SPI registers can be reset to their Reset values by setting the self clearing SPI_SOFT_RESETx bits to 1.

REGISTER UPDATE TRANSFER METHOD

Changes to the writeable SPI registers labeled transfer in Table 10 do not take effect immediately when written to the device via the SPI. Values are held in a shadow register set until the self clearing CHIP_REGMAP_TRANSFER bit in the DEVICE_UPDATE register is set. All changes to transfer register values then take effect simultaneously.

ADC REGISTER UPDATE INDEXING

In addition to the register transfer mechanism, the POWER_MODES and FLEX_OUTPUT_MODE registers have an indexing mechanism. Each of the four ADC cores has its own page containing these registers. These pages can be programmed independently or simultaneously in any combination. ADC core register sets are addressed for a particular register map master/slave transfer by setting the SPI_ADC_x_INDEX bits in the DEVICE_INDEX register. Register data is transferred to the ADC core pages that have these bits set when the next transfer occurs.

ADCs

The MxFE ADCs are multistage pipelined CMOS ADC cores designed for use in communications receivers.

ADC ARCHITECTURE

The AD9993 architecture consists of a dual front-end sample-and-hold circuit, followed by a pipelined switched capacitor ADC. The quantized outputs from each stage are combined into a final 14-bit result.

The input stage of each ADC core contains a differential sampling circuit that can be ac- or dc-coupled in differential or single-ended modes.

Input Common-Mode Voltage (V_{CM}) References

The analog inputs of the AD9993 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that V_{CM} = 0.5 × AVDD (or 0.9 V) is recommended for optimum performance. Four on-board common-mode voltage references are included in the design, one for each AD9993 ADC, and are available from the A_CML, B_CML, C_CML, and D_CML pins. Using these common-mode voltage outputs to set the input common mode of each ADC is recommended. Optimum performance is achieved when the common-mode voltage of the analog input is set by the on-chip common mode references. The A_CML, B_CML, C_CML, and D_CML pins must be decoupled to ground by a 0.1 µF capacitor.

ADC SECTION PROGRAMMING

Each of the four ADCs has its power mode programmed by the indexed ADC_PDWN_MODE bit field of the POWER_MODES register (see the ADC Register Update Indexing section). At reset, all four ADC cores are in power-down mode.

ADC digital data output modes are programmed by the indexed FLEX_OUTPUT_MODE register (see the ADC Register Update Indexing section). Setting the DP_OUT_DATA_EN_N bit to 0 enables the data output of each ADC selected in the DEVICE_INDEX register. At reset, ADC output data is disabled. Setting the DP_OUT_DATA_INV bit to 1 inverts the data output from selected ADCs. The DP_OUT_DFS bit field selects the output code for each selected ADC, offset binary (twos complement with the sine bit inverted), twos complement (reset value), or gray code.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9993 is a differential switched capacitor circuit that has been designed for optimum performance while processing a differential input signal.

For baseband applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 22. To bias the analog input, the V_{CM} voltage can be connected to the center tap of the secondary winding of the transformer.

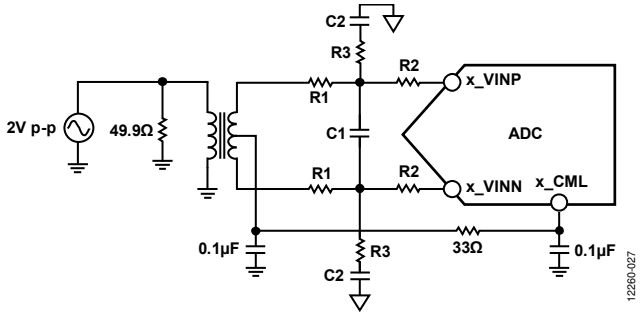

Figure 22. Differential Transformer-Coupled Configuration

Differential double balun coupling is used as the input configuration for AD9993 ADC performance characterization (see Figure 23). In this configuration, the input is ac-coupled and the V_{CM} voltage is provided to each input through a 33 Ω resistor. These resistors compensate for losses in the input baluns to provide a 50 Ω impedance to the driver.

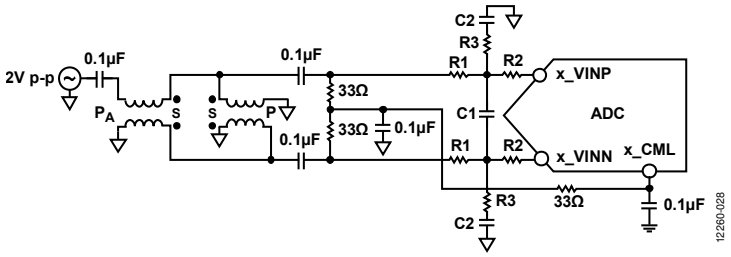

Figure 23. Differential Double Balun Input Configuration

In the double balun and transformer configurations, the value of the input capacitors and resistors is dependent on the input frequency and source impedance. Based on these parameters, the value of the input resistors and capacitors may need to be adjusted or some components may need to be removed. Table 7 displays recommended values to set the RC network for the 0 MHz to 100 MHz frequency range:

Table 7. Example RC Network

Component	Value
R1 Series	33 Ω
C1 Differential	8.2 pF
R2 Series	0 Ω
C2 Shunt	15 pF
R3 Shunt	49.9 Ω

The values given in Table 7 are for each R1, R2, C1, C2, and R3 component shown in Figure 22 and Figure 23.

ADRF6518 as ADC Driver

The ADRF6518 is a variable gain amplifier and low-pass filter that is designed to drive the analog inputs of analog-to-digital converters like the ones included in the AD9993. A principle application of the ADRF6518 is as part of the signal chain in a wideband radio receiver. Figure 32 shows a block diagram for a wideband microwave radio that includes the ADRF6518 and the AD9993.

The low impedance (<10 Ω) output buffers of the ADRF6518 are designed to drive ADC inputs. They are capable of delivering up to 4 V p-p composite two-tone signals into 400 Ω differential loads with >60 dBc IMD3. The output common-mode voltage can be adjusted to 900 mV (the AD9993 input common-mode voltage) without loss of drive capability by presenting the ADRF6518 VOCM pin with the desired common-mode voltage. The high input impedance of VOCM allows the AD9993 reference output (A_CML, B_CML, C_CML or D_CML) to be connected directly.

DACs

The MxFE DACs are part of the Analog Devices high speed CMOS DAC core family. These DACs are designed to be used as part of wide bandwidth communication system transmitter signal chains.

DAC TRANSFER FUNCTION

The AD9993 DACs provide two differential current outputs: IOUTA_P/IOUTA_N, and IOUTB_P/IOUTB_N.

The DAC output current equations are as follows:

$$IOUTx\_P = I_{OUTFS} \times DACx\ input\ code/2^{14}$$

$$IOUTx\_N = I_{OUTFS} \times ((2^{14} - 1) - DACx\ input\ code)/2^{14}$$

where:
DACx input code = 0 to $2^{14} - 1$.
I_{OUTFS} is the full-scale output current or DAC gain specified in Table 1.

$$I_{OUTFS} = 32 \times I_{IREFx}$$

where $I_{REFx} = V_{REFDAC}/R_{FSADJ\_x}$.

Each DAC has its own I_{REFx} set resistor, R_{FSADJ_x}. R_{FSADJ_x} resistors can be on or off chip at the discretion of the users. The nominal value of R_{FSADJ_x} is 1.6 kΩ. The nominal value of V_{REFDAC} is 1.0 V. V_{REFDAC} can be selected as the on-chip band gap reference or as an external user supplied reference.

DAC outputs have a $\sin(\pi f_{OUT}/f_{DAC})/(\pi f_{OUT}/f_{DAC})$ envelope response as a function frequency. This response is also referred to as a sinc envelope.

DAC OUTPUT COMPLIANCE VOLTAGE RANGE AND AC PERFORMANCE

Each DAC has a pair of differential current outputs. The compliance voltage range for each of these two outputs is specified in Table 1. Optimal DAC ac performance is achieved when the output common-mode voltage is between 0.0 V and 0.5 V. and the signal swing falls within the compliance range.

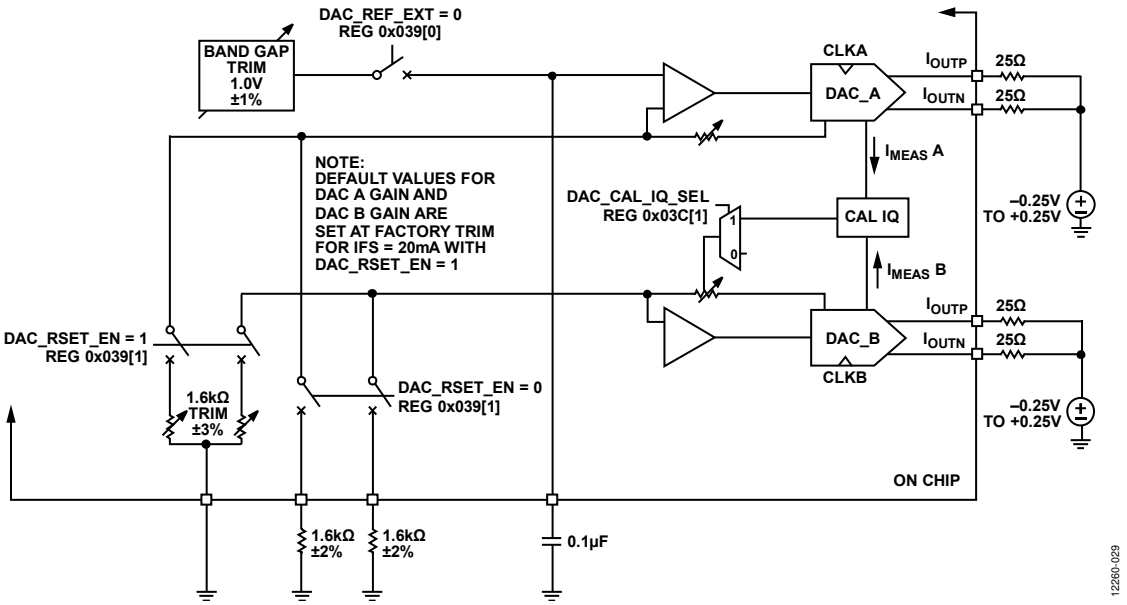

Figure 24. DACs, Band Gap Reference, On-Chip and Off-Chip R_{FSADJ_x}, DAC Gain Setting, and IQ Calibration

Selecting DAC Output Common-Mode Voltage

Two steps are required to select the common-mode output voltages for the two DACs. For a common-mode voltage less than 0.5 V, the CML_A and CML_B pins are grounded. For common-mode voltages that are greater than or equal to 0.5 V, connect a 0.1 µF capacitor between CML_A or CML_B and ground. The second step is to program the DAC_VCM_VREF_BIT bit field. There are three common-mode level settings to choose from. This common-mode setting applies to both DACs.

DAC VOLTAGE REFERENCE

The DACs use a single common voltage reference. An on-chip band gap reference is provided. Optionally, an off-chip voltage reference can be used. If an off-chip DAC reference is used, set the DAC_REF_EXT bit in the DAC_CTRL register to 1. After reset, the on-chip reference is selected.

DAC GAIN SETTING

Figure 24 is a diagram of the AD9993 DACs gain setting section. It shows the two transmit DACs, the bypassable built-in 1.0 V band gap reference, and the selectable internal and board level R_{FSADJ_x} resistors. By default, the on-chip band gap reference is selected. If using a board level. DAC reference voltage, write 1 to the DAC_REF_EXT bit of the DAC_CTRL register.

Each DAC has its own R_{FSADJ_x} set resistor. These resistors can be on or off chip at the discretion of the user. When the on-chip resistors are in use, their gain accuracy is factory calibrated. When the off-chip R_{FSADJ_x} resistors are used, an on-chip IQ calibration scheme can be employed to maintain accuracy between DAC pairs. By default, the on-chip R_{FSADJ_x} is selected. If using a board level R_{FSADJ_x}, write 0 to the DAC_RSET_EN bit of the DAC_CTRL register.

DAC IQ Gain Calibration

When board level R_{FSADJ_x} resistors are used, the gains of the two DACs can be better matched by running the automatic DAC IQ gain calibration procedure. This is done by programming the DAC_CAL_IQ_CTRL register and observing the DAC_CAL_IQ_STAT register as follows:

1. Write 0x23 to DAC_CAL_IQ_CTRL (power up the DAC clock, enable IQ calibration, and start IQ calibration).
2. Read the DAC_CAL_IQ_DONE bit of the DAC_CAL_IQ_STAT register until it goes high.
3. Write 0x4 to DAC_CAL_IQ_CTRL.

DAC DATAPATH FORMAT SELECTION

At reset, the DAC_BINARY bit in the DAC_DP_FMT register is set to 0, selecting twos complement as the data input format for both DACs. To select binary offset, set the DAC_BINARY bit to 1.

DAC TEST TONE GENERATOR DDS

The AD9993 includes a tunable direct digital synthesizer for DAC output tone generation. When the DDS_EN bit of the DDS_CTRL register is set to 1, the DDS becomes the digital signal source for the two DACs. The DDS_CTRL register also has a clock inversion control and amplitude attenuation controls. At reset, the 32-bit DDS tuning word in the DDS_TW1_3, DDS_TW1_2, DDS_TW1_1, and DDS_TW1_0 registers is set to 0x19A00000. This value programs the DDS to produce a 50 MHz tone at both DAC outputs if the master clock frequency is 1 GHz (DAC sampling rate = 500 MSPS). The equation for DDS output frequency is

$$f_{DDS} = (DDS\_TW1/2^{32}) \times f_{DAC}$$

CLOCKING

The clock signals for the LVDS lanes, the DACs, and the ADCs are developed from a single master clock signal. This signal is either input directly on the CLKP/CLKN pins or synthesized by an on-chip PLL multiplier using the REFCLK input signal as a reference. The ADC output and DAC input LVDS lanes run at the master clock frequency divided by 2 and are DDR. Data is clocked on both edges. The sampling rate of the ADCs is ¼ the master clock rate. The sampling rate of the DACs is ½ the master clock frequency. A 1 GHz master clock is shown in Figure 1.

At a 1 GHz master clock frequency, the other on-chip clock frequencies are as follows:

- DCO (ADC DDR LVDS output lane clock): 500 MHz
- DCI (DAC DDR LVDS input lane clock): 500 MHz
- DAC sampling rate: 500 MSPS
- ADC sampling rate: 250 MSPS

ON-CHIP PLL CLOCK MULTIPLIER

Figure 25 shows a block diagram of the MxFE on-chip PLL clock multiplier. If the PLL clock multiplier is used to generate the master clock, the buffered VCO output signal is divided by 4 to produce the synthesized master clock signal.

The reference clock of the on-chip PLL can be either 31.25 MHz or 62.5 MHz. When using a 62.5 MHz clock, a divide by 2 option is provided, as shown in Figure 25, such that the internal PLL reference clock can be set to 31.25 MHz.

A programmable loop filter is integrated on chip. At reset, the on-chip loop filter bandwidth is set to 500 kHz. Lower loop bandwidth can be achieved using an external loop filter connected to the CP pin, as shown in Figure 25.

An on-chip LDO provides the supply voltage for the VCO.

PLL Synthesizer Control and Status Registers

At reset, the SYNTH_INT register contains the reset default value for the VCO output divider of 64 (shown in Figure 25). The PLL multiplier lock status can be read back on Bit 1 of the SYNTH_STAT register. Calibration status is also read from this register. Bits in the SYNTH_CTRL register are used to enable charge pump calibration and to start synthesizer calibration. Synthesizer calibration is required as part of the process of acquiring lock. Charge pump calibration and synthesizer calibration are steps described in the Power-Up Routine When Using the On-Chip Clock Synthesizer section.

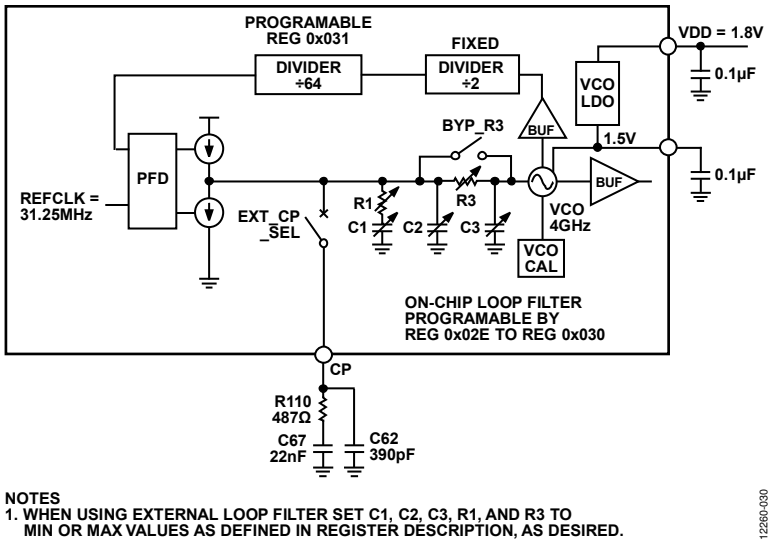

Figure 25. On-Chip PLL Clock Multiplier Block Diagram

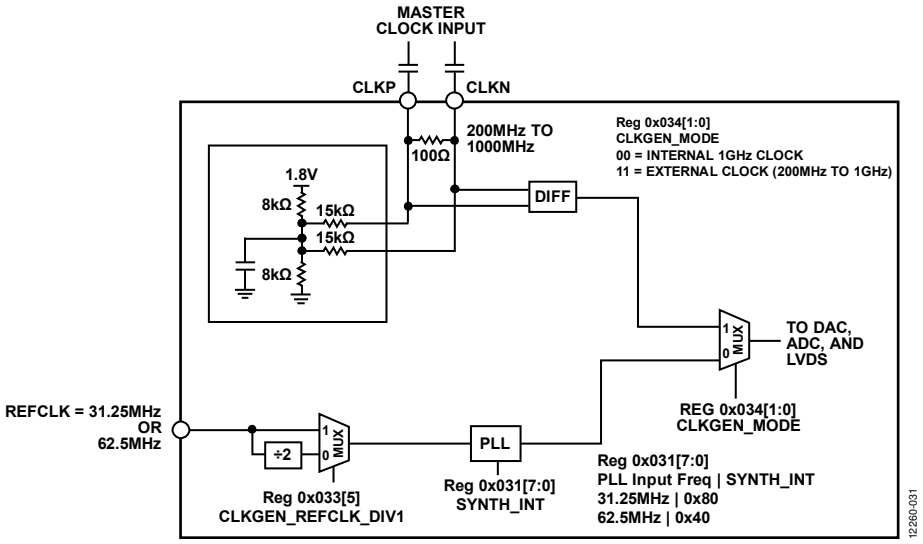

Figure 26. MxFE Clock Control

SELECTING CLOCKING OPTIONS

Figure 26 is a block diagram of the MxFE clocking system and its controls. Options of using either an external master clock or a master clock generated from the on-chip PLL are provided. CLKGEN_MODE[1:0] in the CLKGEN_CTRL2 register selects the PLL multiplier or CLKP/CLKN as the master clock source.

ADC DATAPATH AND DAC DATAPATH FIFOS

In the AD9993, data FIFOs are placed between the ADC core outputs and the LVDS buffers and drivers. Similarly, on the DAC side, data FIFOs are placed between the LVDS input buffers and the DAC cores. These FIFOs absorb the phase difference between DCI and the DAC sampling clock and between the ADC sampling clock and DCO. DAC sampling clock and DCI are locked in frequency but have an unknown phase relationship. The ADC sampling clock and DCO have the same characteristics.

FIFOs are eight samples deep. During a start-up register sequence, both the DAC input datapath FIFOs and the ADC output data path FIFOs have their read and write pointers initialized (see the Start-Up Register Sequences section). This occurs after all clocks in the AD9993 are running and settled. The pointers are set four data samples apart. The ADC datapath FIFO depth can be read in the RXFIFO_WR_OFFSET bit field in the align register. The DAC datapath FIFO depth can be read as the RXFIFO_THERM[7:0] value in the DAC_FIFO_STS1 register. This value is a thermometer code. FIFO depths remain constant after initialization when all clocks are running properly.

LVDS INTERFACES

Each DAC has seven DDR LVDS input data lanes. Each DAC sample input requires the user to input two 7-bit words to the interface with appropriate zero stuffing. Each ADC has four DDR LVDS output data lanes. For each ADC output sample, four 4-bit words are output.

LVDS ADC Data Link

There are two LVDS ADC buses for the two ADCs. Each LVDS ADC Data bus has four lanes for 14-bit data output in two full DDR cycles. A strobe lane is shared by the four ADC LVDS links to identify the MSB of the 14-bit data. Figure 27 shows one LVDS ADC output data link with four lanes. Lane 0 to Lane 2 output the 12 MSBs of the 14-bit ADC data. Lane 3 carries the two LSBs of the 14-bit ADC data and an overrange bit.

LVDS DAC Data Link

There are two LVDS DAC data links for the dual DAC. Each LVDS DAC data link has seven lanes capable of transmitting 14-bit data in one DDR full cycle. Figure 28 shows one LVDS DAC input data link with seven lanes.

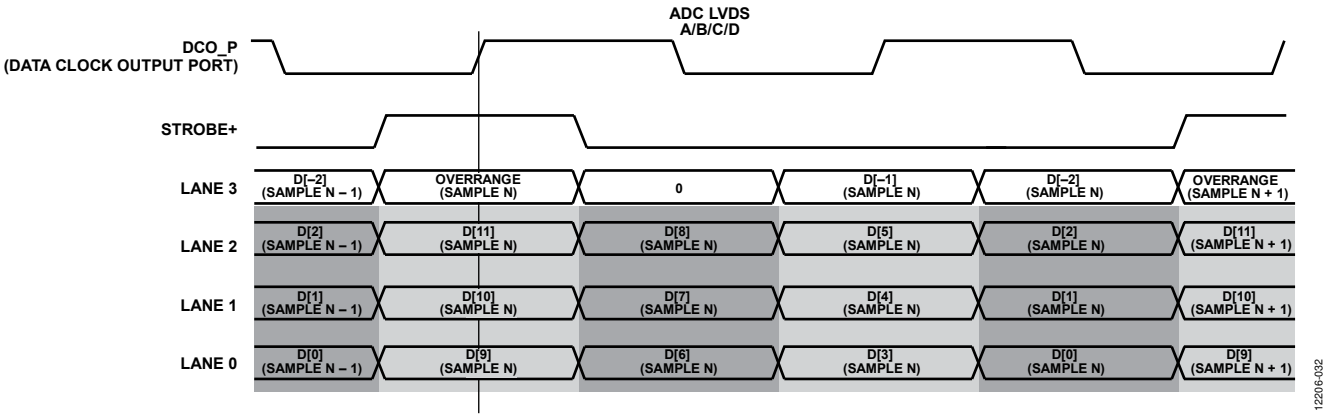

Figure 27. Output Sample Data Format

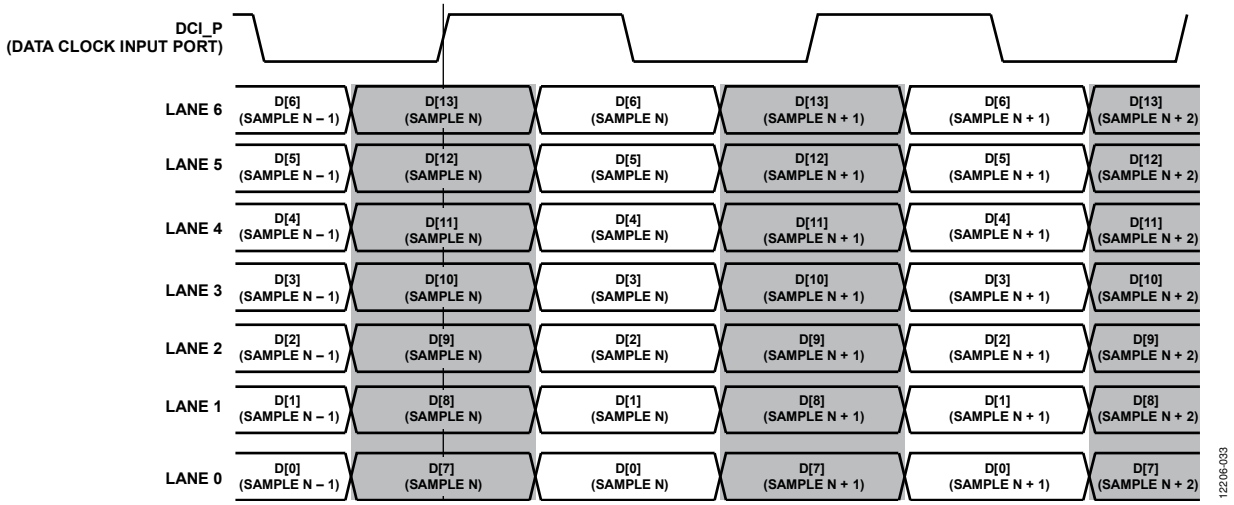

Figure 28. DAC Input Sample Data Format

LVDS INTERFACE TIMING

DAC Input Interface

Table 8 specifies the setup and hold time requirements for DAC LVDS data lane inputs relative to DCI. Figure 29 shows a timing diagram for this interface. DDR DCI edges occur at the position within the data eye (the white region in Figure 29) listed in Table 8.

Table 8. DAC DDR LVDS Input Setup and Hold Times Relative to DCI (Guaranteed)

Parameter	Minimum	Unit
$\|t_{SU}\|$	150	ps
$\|t_{HOLD}\|$	200	ps
Data Period	1000	Ps

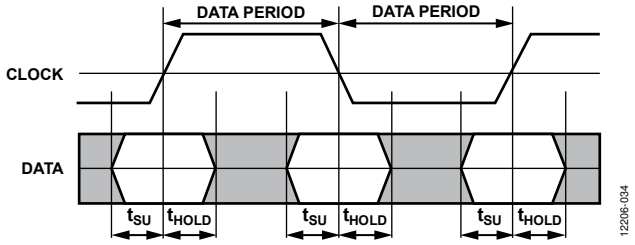

Figure 29. DAC Input LVDS Lane Timing

ADC Output Interface

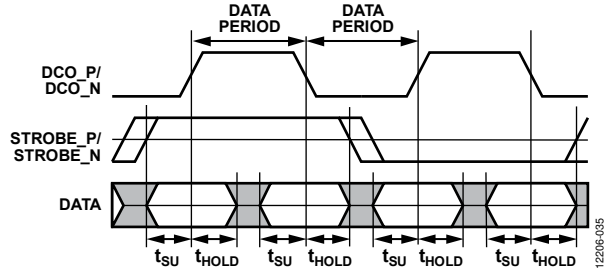

Figure 30. ADC Output LVDS Lane Timing

Table 9 specifies the time between the ADC LVDS data lane output transitions and the DDR DCO clock edge 50% transition point.

Table 9. ADC DDR LVDS Data and Strobe Output Setup and Hold Times Relative to DCO (Guaranteed)

Parameter	Minimum	Unit
$\|t_{SU}\|$	400	ps
$\|t_{HOLD}\|$	430	ps
Data Period	1000	ps

LVDS LANE TESTING USING PRBS

One pseudorandom binary sequence (PRBS) generator is included for each ADC LVDS lane and one PRBS detector on each DAC LVDS lane. The designs for the generator and detector are implemented as a 23rd-order pseudorandom noise (PN23) sequence defined by the generator polynomial $x^{23} + x^{18} + 1$. The initial seed of the generator is programmable so that each lane can output different values if started simultaneously. The four seed registers are indexed as described in the ADC Register Update Indexing section.

DAC PRBS test results are read back on the DAC_A_PRBS_ERRx and DAC_B_PRBS_ERRx error counter registers. The DAC input PRBS error counters are enabled and the error counters cleared by the bits in the DAC_PRBS_CTRL register. ADC output lane PRBS generation is controlled by the bits in the PRBS_GEN_CTRL register.

POWER MODE PROGRAMMING

The AD9993 has a POWER_MODES register that allows the user to place sections of the chip into different power modes. The PDWN_PIN_FUNC bit programs the function of the PDWN pin. By default, assertion of PDWN causes the AD9993 to go into full power-down. The clock generator, indexed ADCs, DACs, and PLL synthesizer are all powered down at reset. The indexed ADCs have four power modes. See the ADC Register Update Indexing section for a definition of indexing.

INTERRUPT REQUEST OPERATION

The AD9993 provides an interrupt request signal, $\overline{\text{ALERT}}$. It is used to notify the user system of significant on-chip events. The $\overline{\text{ALERT}}$ pin is an open-drain, active low output.

Eight different event flags provide visibility into the device. These raw events are located in the INT_RAW register. These raw events are always latched in the INT register. If the event is left unmasked, the latched event triggers an external interrupt on $\overline{\text{ALERT}}$. INTEN is the interrupt enable register. When an event is masked, the INT register captures the event in latched form. A masked event does not cause $\overline{\text{ALERT}}$ to go true.

The eight events that trigger an interrupt (if enabled) are

- PLL lock lost
- PLL locked
- FIFO Warning 1
- FIFO Warning 2
- ADC A overrange
- ADC B overrange
- ADC C overrange
- ADC D overrange

Interrupt Service Routine

For the interrupt service routine, interrupt request management starts by selecting the set of events that require host intervention or monitoring using the bits in the INTEN register. For events requiring host intervention, upon $\overline{\text{ALERT}}$ activation, run the following routine to clear an interrupt request:

1. Read the status of the latched bits in the INT register that are being monitored.
2. Monitor the unlatched status bits in the INT_RAW register directly if needed.
3. Perform any actions that may be required to clear the interrupt(s).
4. Read the INT_RAW bits to verify that the actions taken have cleared the event.
5. Clear the interrupt by writing 1 to the event flag bit in the INT register.

TEMPERATURE SENSOR

The AD9993 has a diode-based temperature sensor for measuring the temperature of the die. The temperature reading is accessed using the TS_RD_LSB and TS_RD_MSB registers. The temperature of the die can be calculated as

$$T_{DIE} = \frac{Die\ Temp[15:0] - 41{,}237}{106}$$

where:
T_{DIE} is the die temperature in degrees Celsius.
Die Temp is the concatenated 16-bit contents of the TD_RD_LSB and TD_RD_MSB registers. The temperature accuracy is ±7°C typical over the −40°C to +85°C range with one point temperature calibration against a known temperature. A typical plot of the die temperature code readback vs. die temperature is shown in Figure 31.

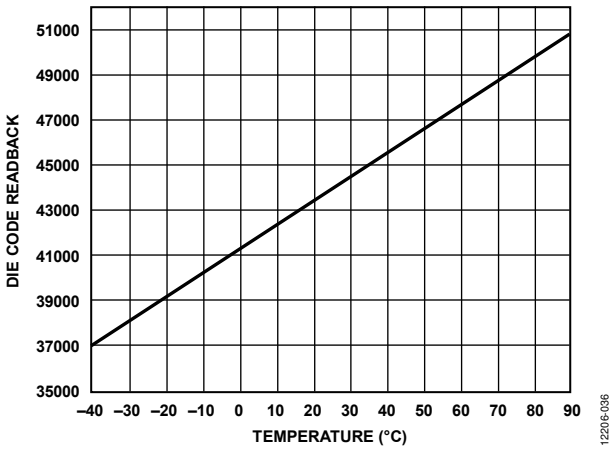

Figure 31. Die Temperature Code Readback vs. Die Temperature

Estimates of the ambient temperature can be made if the power dissipation of the device is known.