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30 V, Low Noise, Rail-to-Rail Input/Output, Low Power Operational Amplifiers

Data Sheet

ADA4084-1/ADA4084-2/ADA4084-4

FEATURES

Rail-to-rail input/output
Low power: 0.625 mA typical per amplifier at ±15 V
Gain bandwidth product: 15.9 MHz at A_V = 100 typical
Unity-gain crossover: 9.9 MHz typical
−3 dB closed-loop bandwidth: 13.9 MHz typical at ±15 V
Low offset voltage: 100 µV maximum (SOIC)
Unity-gain stable
High slew rate: 4.6 V/µs typical
Low noise: 3.9 nV/√Hz typical at 1 kHz

APPLICATIONS

Battery-powered instrumentation
High-side and low-side sensing
Power supply control and protection
Telecommunications
Digital-to-analog converter (DAC) output amplifiers
Analog-to-digital converter (ADC) input buffers

GENERAL DESCRIPTION

The ADA4084-1 (single), ADA4084-2 (dual), and ADA4084-4 (quad) are single-supply, 10 MHz bandwidth amplifiers featuring rail-to-rail inputs and outputs. They are guaranteed to operate from +3 V to +30 V (or ±1.5 V to ±15 V).

These amplifiers are well suited for single-supply applications requiring both ac and precision dc performance. The combination of wide bandwidth, low noise, and precision makes the ADA4084-1, ADA4084-2, and ADA4084-4 useful in a wide variety of applications, including filters and instrumentation.

Other applications for these amplifiers include portable telecommunications equipment, power supply control and protection, and use as amplifiers or buffers for transducers with wide output ranges. Sensors requiring a rail-to-rail input amplifier include Hall effect, piezoelectric, and resistive transducers.

The ability to swing rail to rail at both the input and output enables designers to build multistage filters in single-supply systems and to maintain high signal-to-noise ratios.

The ADA4084-1, ADA4084-2, and ADA4084-4 are specified over the industrial temperature range of −40°C to +125°C.

PIN CONNECTION DIAGRAM

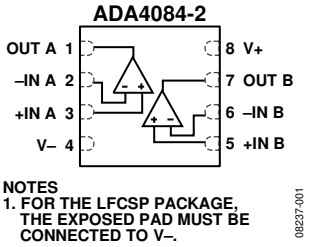

Figure 1. ADA4084-2, 8-Lead LFCSP (CP)

See the Pin Configurations and Function Descriptions section for additional pin configurations and information about the pin functions.

The single ADA4084-1 is available in the 5-lead SOT-23 and 8-lead SOIC; the dual ADA4084-2 is available in the 8-lead SOIC, 8-lead MSOP, and 8-lead LFCSP surface-mount packages; and the ADA4084-4 is offered in the 14-lead TSSOP and 16-lead LFCSP.

The ADA4084-1, ADA4084-2, and ADA4084-4 are members of a growing series of high voltage, low noise op amps offered by Analog Devices, Inc. (see Table 1).

Table 1. Low Noise Op Amps

Single	Dual	Quad	Voltage Noise
AD8597	AD8599		1.1 nV/Hz
ADA4004-1	ADA4004-2	ADA4004-4	1.8 nV/Hz
AD8675	AD8676		2.8 nV/Hz rail-to-rail output
AD8671	AD8672	AD8674	2.8 nV/Hz
OP27, OP37			3.2 nV/Hz
ADA4084-1	ADA4084-2	ADA4084-4	3.9 nV/Hz rail-to-rail input/output

Rev. H
Document Feedback

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{SY} = 3 V, V_{CM} = 1.5 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	SOIC package		20	100	µV
		−40°C ≤ T_A ≤ +125°C			200	µV
		SOT-23, MSOP, TSSOP packages		50	130	µV
		−40°C ≤ T_A ≤ +125°C			250	µV
		ADA4084-2 LFCSP package		80	200	µV
		−40°C ≤ T_A ≤ +125°C			300	µV
Offset Voltage Drift	Δt/ΔT	−40°C ≤ T_A ≤ +125°C		0.5	1.75	µV/°C
Offset Voltage Matching		T_A = 25°C			150	µV
		ADA4084-4 LFCSP package			200	µV
Input Bias Current	I_B			140	250	nA
		−40°C ≤ T_A ≤ +125°C			400	nA
Input Offset Current	I_{OS}			5	25	nA
		−40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3 V	64	88		dB
		−40°C ≤ T_A ≤ +125°C	60			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.5 V ≤ V_{OUT} ≤ 2.5 V	100	104		dB
		−40°C ≤ T_A ≤ +125°C	97			dB
Input Impedance						
Differential				100||1.1		kΩ||pF
Common Mode				80||2.9		MΩ||pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	2.90	2.95		V
		−40°C ≤ T_A ≤ +125°C	2.80			V
		R_L = 2 kΩ to V_{CM}	2.85	2.9		V
		−40°C ≤ T_A ≤ +125°C	2.70			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		10	20	mV
		−40°C ≤ T_A ≤ +125°C			40	mV
		R_L = 2 kΩ to V_{CM}		20	30	mV
		−40°C ≤ T_A ≤ +125°C			50	mV
Short-Circuit Current	I_{SC}			−17/+10		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = 1		0.1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±1.25 V to ±1.75 V	100	110		dB
		−40°C ≤ T_A ≤ +125°C	90			dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA		0.565	0.650	mA
		−40°C ≤ T_A ≤ +125°C			0.950	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	2.0	2.6		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		15.4		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		8.08		MHz
Phase Margin	Φ_M			86		Degrees
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = 1, V_{IN} = 5 mV p-p		12.3		MHz
Settling Time	t_S	A_V = 10, V_{IN} = 2 V p-p, 0.1%		4		µs
Total Harmonic Distortion Plus Noise	THD + N	V_{IN} = 300 mV rms, R_L = 2 kΩ, f = 1 kHz		0.009		%
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.14		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		3.9		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.55		pA/√Hz

V_{SY} = ±5.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	SOIC package		30	100	µV
		−40°C ≤ T_A ≤ +125°C			200	µV
		SOT-23, MSOP, TSSOP packages		60	130	µV
		−40°C ≤ T_A ≤ +125°C			250	µV
		ADA4084-2 LFCSP package		90	200	µV
		−40°C ≤ T_A ≤ +125°C			300	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.5	1.75	µV/°C
Offset Voltage Matching		T_A = 25°C			150	µV
		ADA4084-4 LFCSP package			200	µV
Input Bias Current	I_B			140	250	nA
		−40°C ≤ T_A ≤ +125°C			400	nA
Input Offset Current	I_{OS}			5	25	nA
		−40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			−5		+5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±4 V, −40°C ≤ T_A ≤ +125°C	106	124		dB
		V_{CM} = ±5 V	76			dB
		V_{CM} = ±5 V, −40°C ≤ T_A ≤ +125°C	70			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, −4 V ≤ V_{OUT} ≤ 4 V	108	112		dB
		−40°C ≤ T_A ≤ +125°C	103			dB
Input Impedance						
Differential				100||1.1		kΩ||pF
Common Mode				200||2.5		MΩ||pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	4.9	4.95		V
		−40°C ≤ T_A ≤ +125°C	4.8			V
		R_L = 2 kΩ to V_{CM}	4.8	4.85		V
		−40°C ≤ T_A ≤ +125°C	4.7			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		−4.95	−4.9	V
		−40°C ≤ T_A ≤ +125°C			−4.8	V
		R_L = 2 kΩ to V_{CM}		−4.95	−4.8	V
		−40°C ≤ T_A ≤ +125°C			−4.7	V
Short-Circuit Current	I_{SC}			−24/+17		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = 1		0.1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±2 V to ±18 V	110	120		dB
		−40°C ≤ T_A ≤ +125°C	105			dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA		0.595	0.700	mA
		−40°C ≤ T_A ≤ +125°C			1.00	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ to V_{CM}	2.4	3.7		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		15.9		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		9.6		MHz
Phase Margin	Φ_M			85		Degrees
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = 1, V_{IN} = 5 mV p-p		13.9		MHz
Settling Time	t_S	A_V = 10, V_{IN} = 8 V p-p, 0.1%		4		µs
Total Harmonic Distortion Plus Noise	THD + N	V_{IN} = 2 V rms, R_L = 2 kΩ, f = 1 kHz		0.003		%
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.14		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		3.9		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.55		pA/√Hz

V_{SY} = ±15.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	SOIC package		40	100	µV
		−40°C ≤ T_A ≤ +125°C			200	µV
		SOT-23, MSOP, TSSOP packages		70	130	µV
		−40°C ≤ T_A ≤ +125°C			250	µV
		ADA4084-2 LFCSP package		100	200	µV
		−40°C ≤ T_A ≤ +125°C			300	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.5	1.75	µV/°C
Offset Voltage Matching		T_A = 25°C			150	µV
		ADA4084-4 LFCSP package			200	µV
Input Bias Current	I_B			140	250	nA
		−40°C ≤ T_A ≤ +125°C			400	nA
Input Offset Current	I_{OS}			5	25	nA
		−40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			−15		+15	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±14 V, −40°C ≤ T_A ≤ +125°C	106	124		dB
		V_{CM} = ±15 V	85			dB
		V_{CM} = ±15 V, −40°C ≤ T_A ≤ +125°C	80			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, −13.5 V ≤ V_{OUT} ≤ +13.5 V	110	117		dB
		−40°C ≤ T_A ≤ +125°C	105			dB
Input Impedance						
Differential				100‖1.1		kΩ‖pF
Common Mode				200‖2.5		MΩ‖pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	14.85	14.9		V
		−40°C ≤ T_A ≤ +125°C	14.8			V
		R_L = 2 kΩ to V_{CM}	14.5	14.6		V
		−40°C ≤ T_A ≤ +125°C	14.0			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		−14.95	−14.9	V
		−40°C ≤ T_A ≤ +125°C			−14.8	V
		R_L = 2 kΩ to V_{CM}		−14.9	−14.8	V
		−40°C ≤ T_A ≤ +125°C			−14.7	V
Short-Circuit Current	I_{SC}			±30		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +1		0.1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±2 V to ±18 V	110	120		dB
		−40°C ≤ T_A ≤ +125°C	105			dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA		0.625	0.750	mA
		−40°C ≤ T_A ≤ +125°C			1.050	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	2.4	4.6		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		15.9		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		9.9		MHz
Phase Margin	Φ_M			86		Degrees
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = 1, V_{IN} = 5 mV p-p		13.9		MHz
Settling Time	t_S	A_V = 10, V_{IN} = 10 V p-p, 0.1%		4		µs
Total Harmonic Distortion Plus Noise	THD + N	V_{IN} = 5 V rms, R_L = 2 kΩ, f = 1 kHz		0.003		%
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.1		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		3.9		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.55		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	$V- \le V_{IN} \le V+$
Differential Input Voltage[1]	±0.6 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C
ESD	
Human Body Model[2]	4.5 kV
Machine Model[3]	200 V
Field-Induced Charged-Device Model (FICDM)[4]	1.25 kV

[1] For input differential voltages greater than 0.6 V, limit the input current to less than 5 mA to prevent degradation or destruction of the input devices.
[2] Applicable standard: MIL-STD-883, Method 3015.7.
[3] Applicable standard: JESD22-A115-A (ESD machine model standard of JEDEC).
[4] Applicable standard: JESD22-C101-C (ESD FICDM standard of JEDEC).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device soldered on a 4-layer JEDEC standard printed circuit board (PCB) with zero airflow.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead SOT-23 (RJ-5)	219.4	155.6	°C/W
8-Lead SOIC_N (R-8)	121	43	°C/W
8-Lead MSOP (RM-8)	142	45	°C/W
8-Lead LFCSP (CP-8-12)[1, 3]	84	40	°C/W
14-Lead TSSOP (RU-14)	112	43	°C/W
16-Lead LFCSP (CP-16-26)[2, 3]	55	30	°C/W

[1] Values are based on 4-layer (2S2P) JEDEC standard PCB, with four thermal vias. Exposed pad soldered to PCB.
[2] Values are based on 4-layer (2S2P) JEDEC standard PCB, with nine thermal vias. Exposed pad soldered to PCB.
[3] θ_{JC} measured on top of package.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

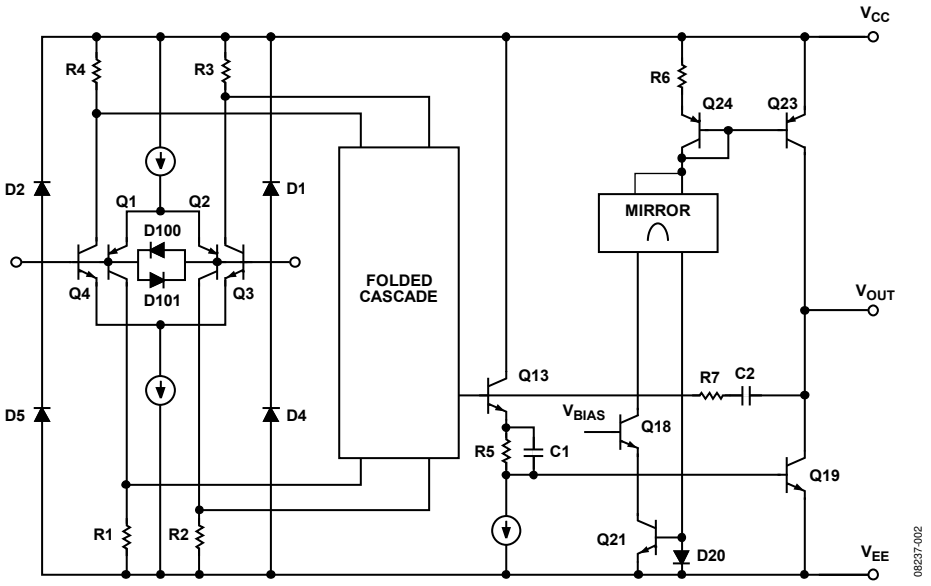

Figure 2. Simplified Schematic

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

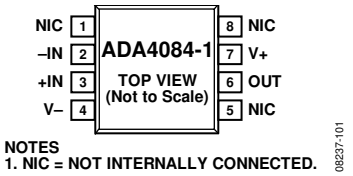

Figure 3. ADA4084-1, 8-Lead SOIC (R)

Table 7. 8-Lead SOIC, ADA4084-1 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NIC	Not Internally Connected
2	–IN	Negative Input
3	+IN	Positive Input
4	V–	Negative Supply
5	NIC	Not Internally Connected
6	OUT	Output
7	V+	Positive Supply
8	NIC	Not Internally Connected

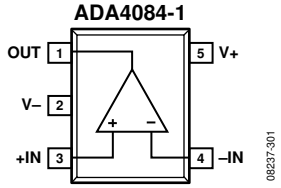

Figure 4. ADA4084-1, 5-Lead SOT-23 (RJ)

Table 8. 5-Lead SOT-23, ADA4084-1 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT	Output
2	V–	Negative Supply
3	+IN	Positive Input
4	–IN	Negative Input
5	V+	Positive Supply

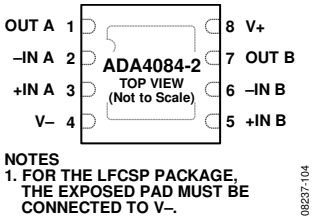

Figure 5. ADA4084-2, 8-Lead LFCSP (CP)

Table 9. 8-Lead LFCSP, ADA4084-2 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A
2	–IN A	Negative Input, Channel A
3	+IN A	Positive Input, Channel A
4	V–	Negative Supply
5	+IN B	Positive Input, Channel B
6	–IN B	Negative Input, Channel B
7	OUT B	Output, Channel B
8	V+	Positive Supply
	EPAD	Exposed Pad. For the LFCSP package, the exposed pad must be connected to V–.

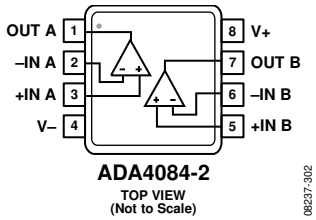

Figure 6. ADA4084-2, 8-Lead MSOP (RM)

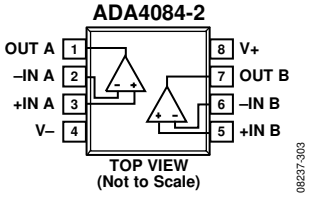

Figure 7. ADA4084-2, 8-Lead SOIC (R)

Table 10. 8-Lead MSOP, 8-Lead SOIC, ADA4084-2 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A
2	–IN A	Negative Input, Channel A
3	+IN A	Positive Input, Channel A
4	V–	Negative Supply
5	+IN B	Positive Input, Channel B
6	–IN B	Negative Input, Channel B
7	OUT B	Output, Channel B
8	V+	Positive Supply B

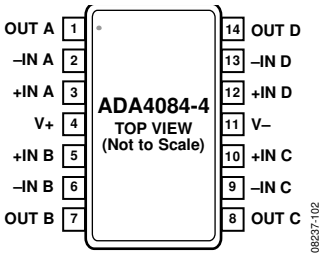

Figure 8. ADA4084-4, 14-Lead TSSOP (RU)

Table 11. 14-Lead TSSOP, ADA4804-4 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A
2	–IN A	Negative Input, Channel A
3	+IN A	Positive Input, Channel A
4	V+	Positive Supply
5	+IN B	Positive Input, Channel B
6	–IN B	Negative Input, Channel B
7	OUT B	Output, Channel B
8	OUT C	Output, Channel C
9	–IN C	Negative Input, Channel C
10	+IN C	Positive Input, Channel C
11	V–	Negative Supply
12	+IN D	Positive Input, Channel D
13	–IN D	Negative Input, Channel D
14	OUT D	Output, Channel D

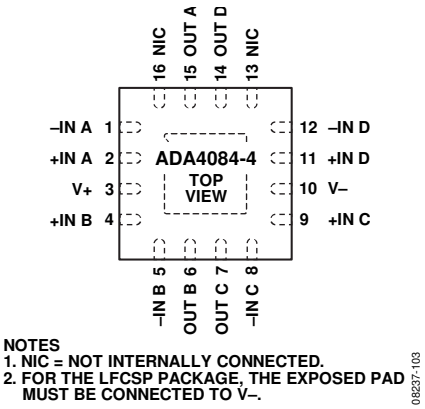

Figure 9. ADA4084-4, 16-Lead LFCSP (CP)

Table 12. 16-Lead LFCSP, ADA4084-4 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	–IN A	Negative Input Channel A
2	+IN A	Positive Input, Channel A
3	V+	Positive Supply
4	+IN B	Positive Input, Channel B
5	–IN B	Negative Input, Channel B
6	OUT B	Output, Channel B
7	OUT C	Output, Channel C
8	–IN C	Negative Input, Channel C
9	+IN C	Positive Input, Channel C
10	V–	Negative Supply
11	+IN D	Positive Input, Channel D
12	–IN D	Negative Input, Channel D
13	NIC	Not Internally Connected
14	OUT D	Output, Channel D
15	OUT A	Output, Channel A
16	NIC	Not Internally Connected

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

±1.5 V CHARACTERISTICS

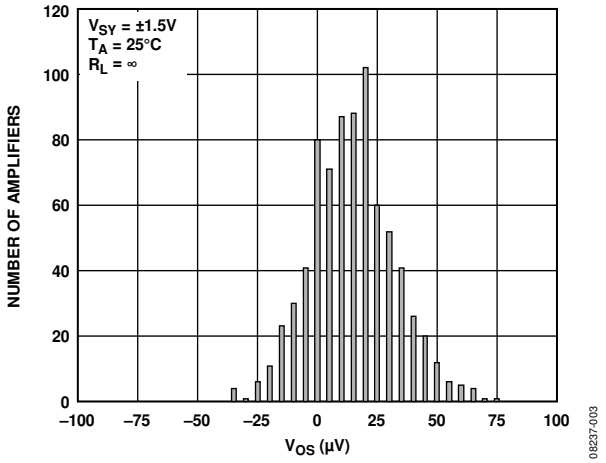

Figure 10. Input Offset Voltage (V_{OS}) Distribution, SOIC

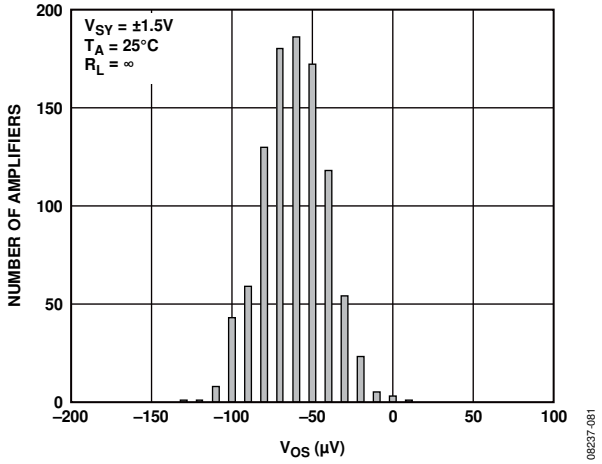

Figure 13. Input Offset Voltage (V_{OS}) Distribution, LFCSP

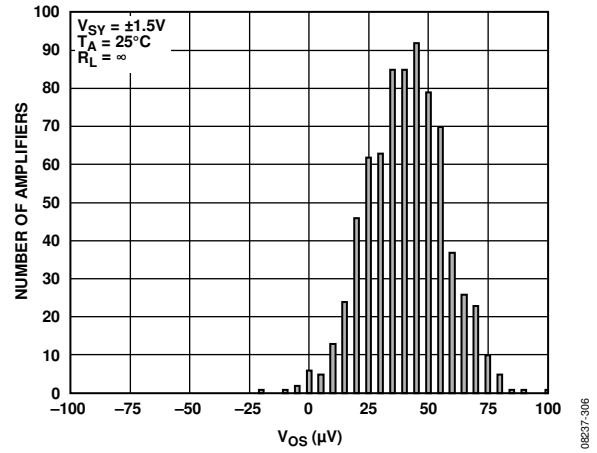

Figure 11. Input Offset Voltage (V_{OS}) Distribution, SOT-23

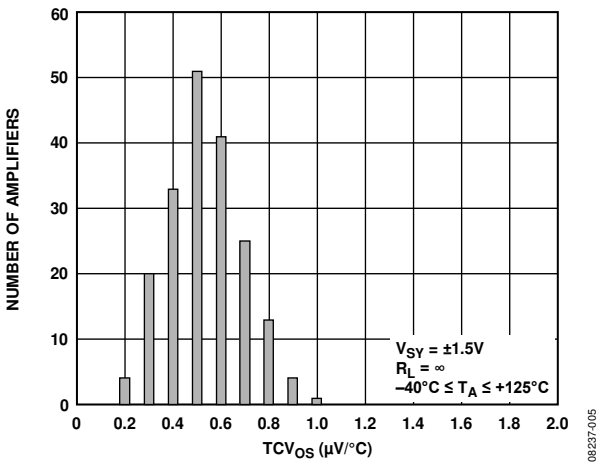

Figure 14. TCV_{OS} Distribution, SOIC, MSOP, and TSSOP

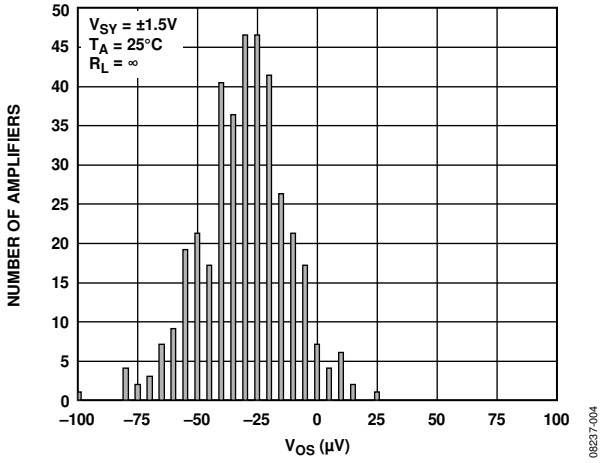

Figure 12. Input Offset Voltage (V_{OS}) Distribution, MSOP and TSSOP

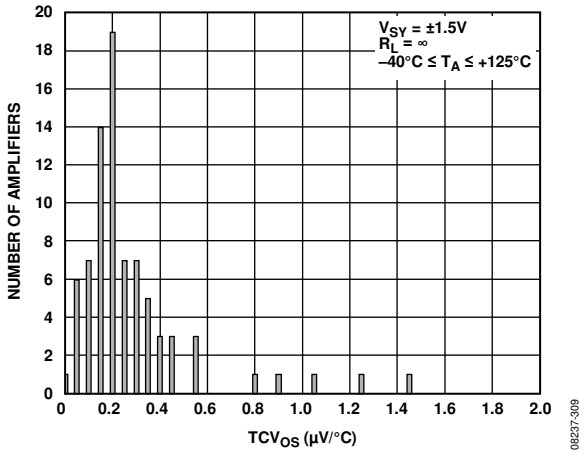

Figure 15. TCV_{OS} Distribution, SOT-23

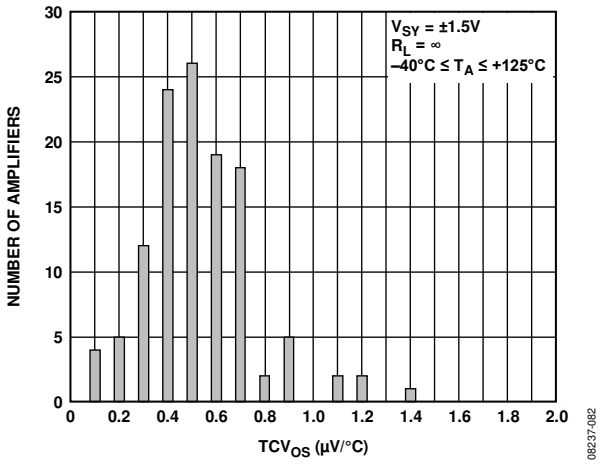

Figure 16. TCV_{OS} Distribution, LFCSP

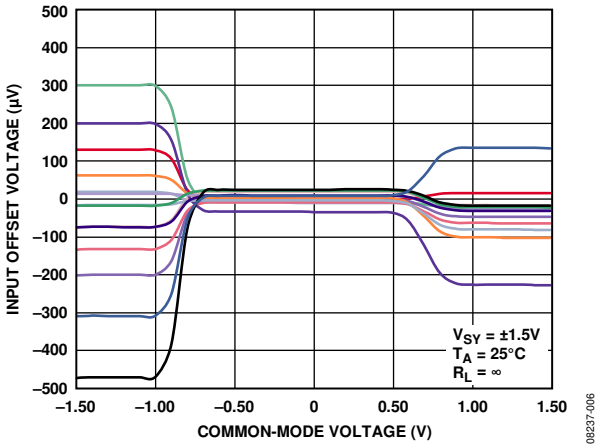

Figure 17. Input Offset Voltage vs. Common-Mode Voltage

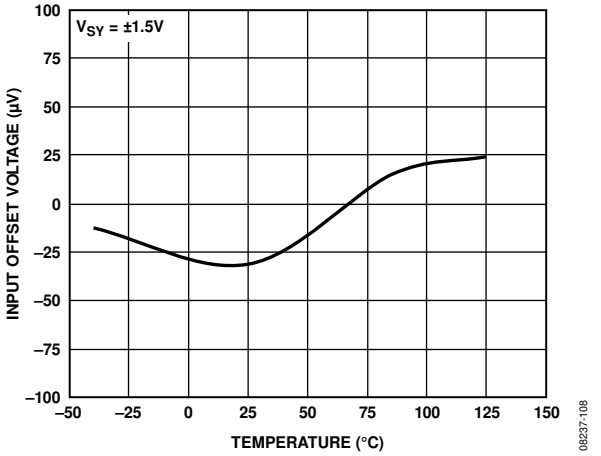

Figure 18. Input Offset Voltage vs. Temperature

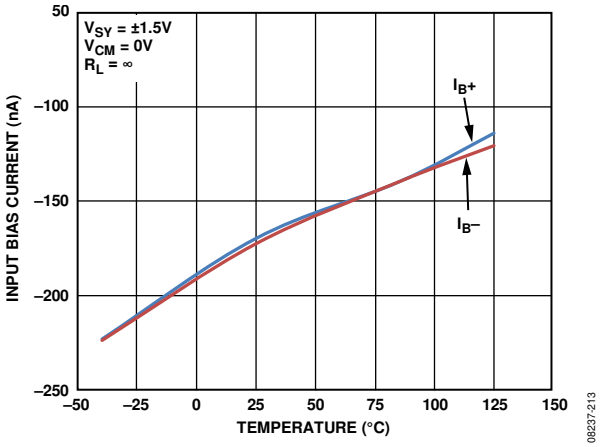

Figure 19. Input Bias Current vs. Temperature

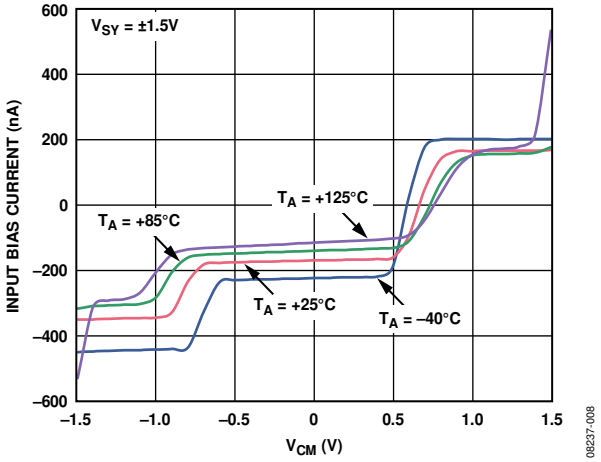

Figure 20. Input Bias Current vs. V_{CM} for Various Temperatures

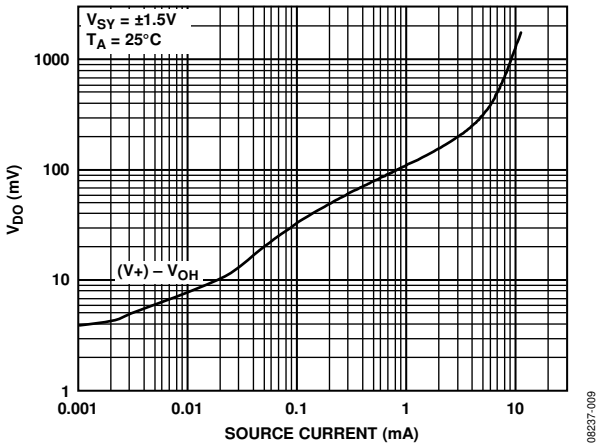

Figure 21. Dropout Voltage (V_{DO}) vs. Source Current

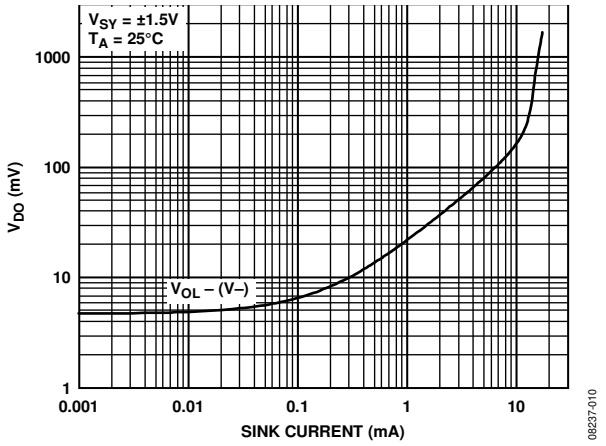

Figure 22. Dropout Voltage (V_{DO}) vs. Sink Current

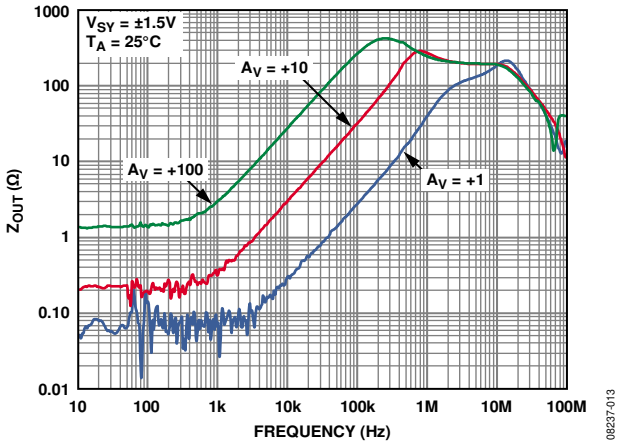

Figure 25. Output Impedance (Z_{OUT}) vs. Frequency

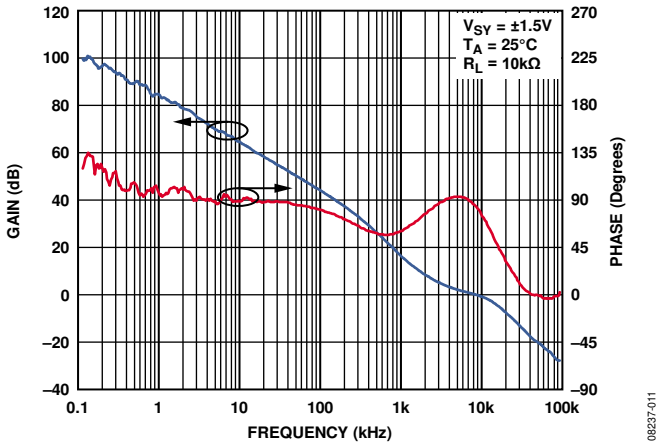

Figure 23. Open-Loop Gain and Phase vs. Frequency

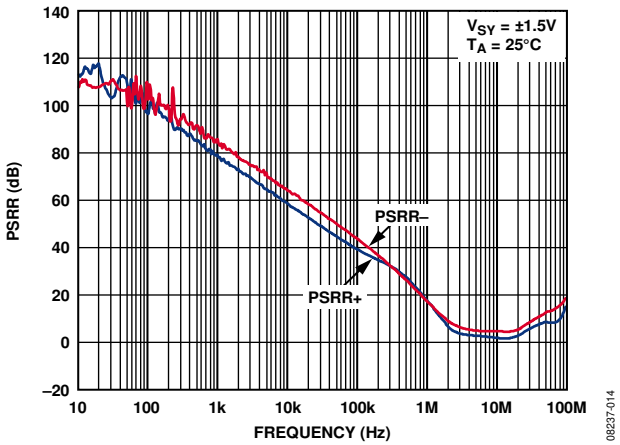

Figure 26. PSRR vs. Frequency

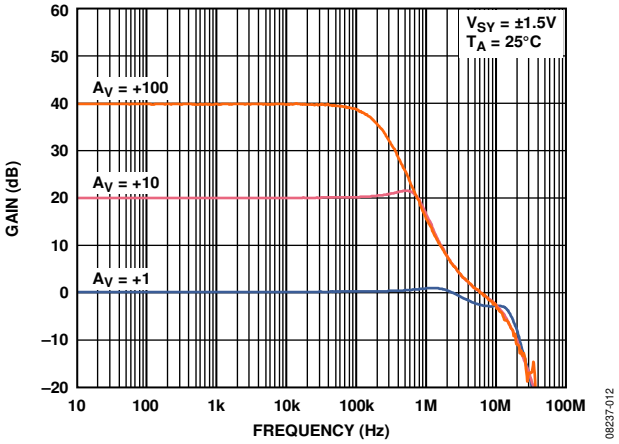

Figure 24. Closed-Loop Gain vs. Frequency

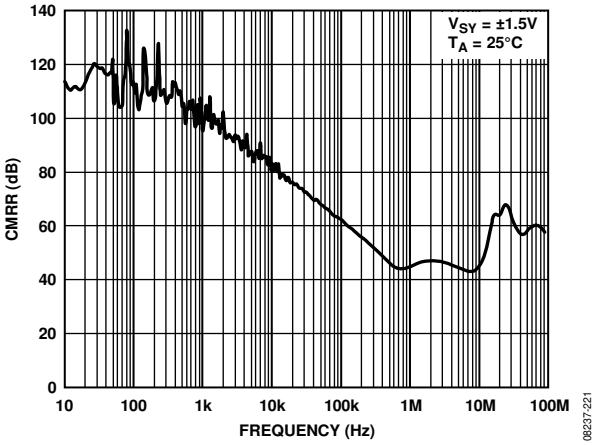

Figure 27. CMRR vs. Frequency

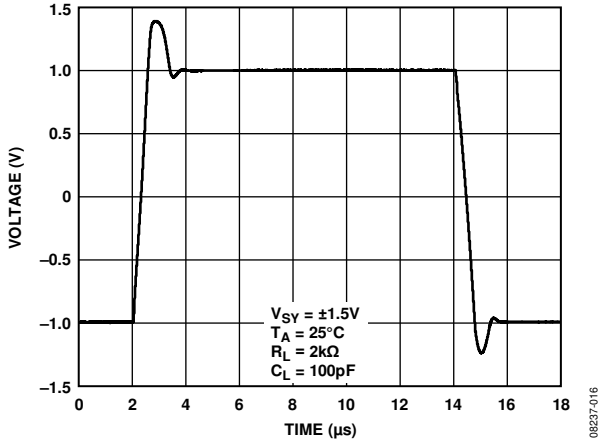

Figure 28. Large Signal Transient Response

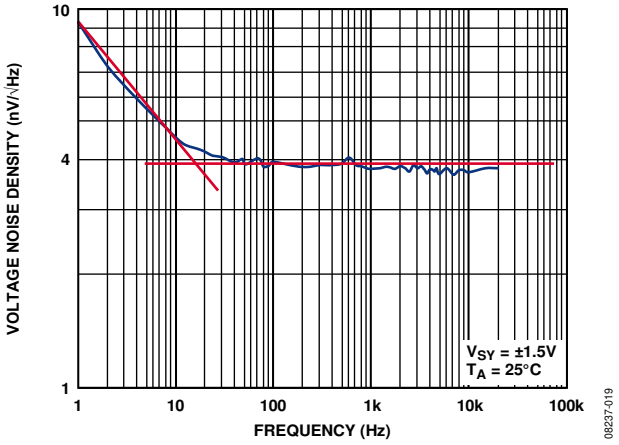

Figure 31. Voltage Noise Density vs. Frequency

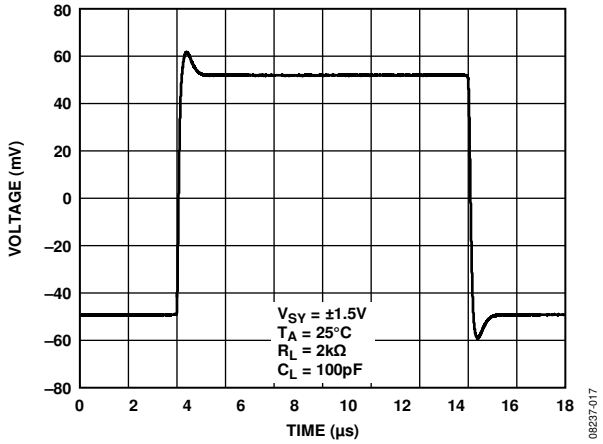

Figure 29. Small Signal Transient Response

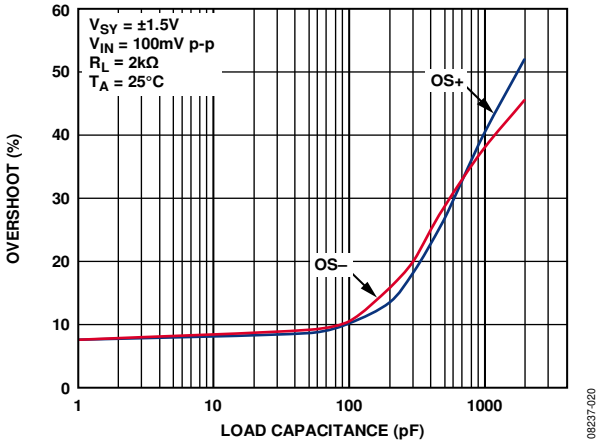

Figure 32. Overshoot vs. Load Capacitance

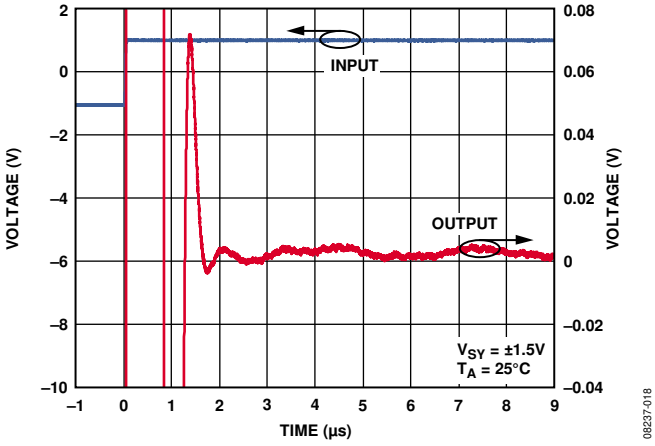

Figure 30. Settling Time

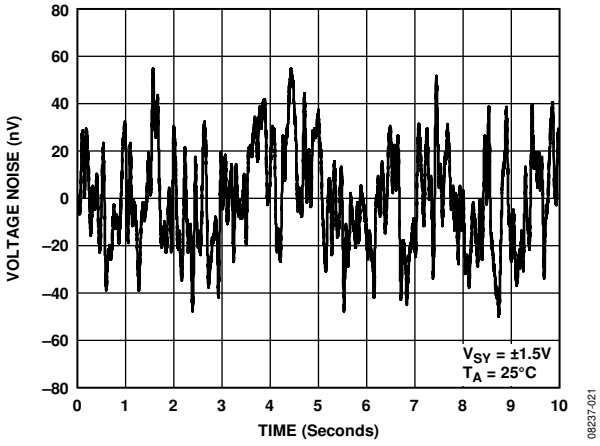

Figure 33. Voltage Noise, 0.1 Hz to 10 Hz

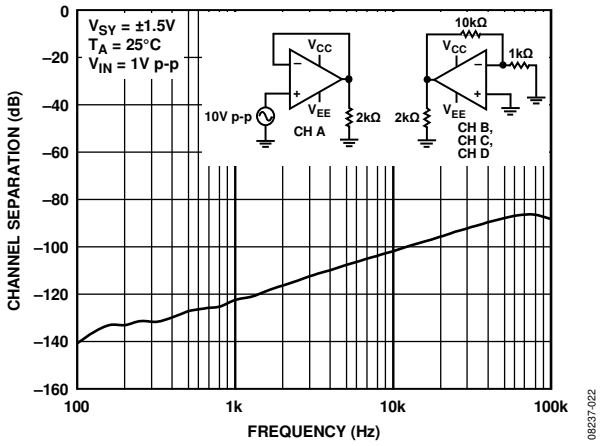

Figure 34. Channel Separation vs. Frequency

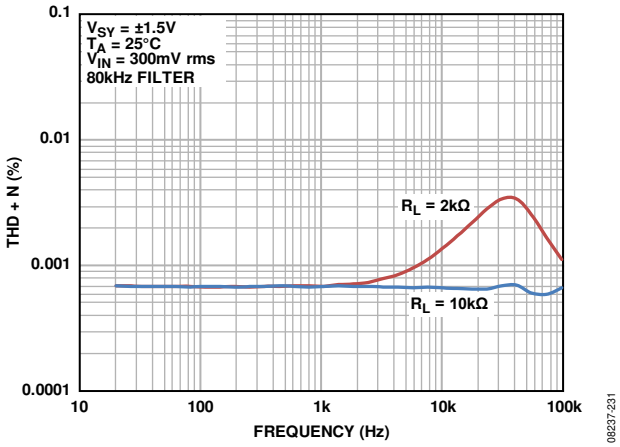

Figure 37. THD + N vs. Frequency, 80 kHz Filter

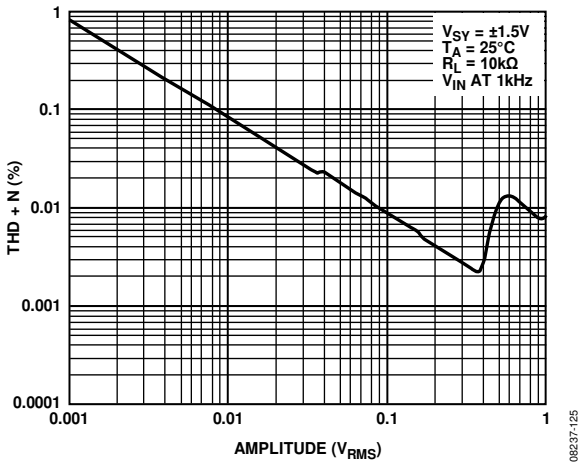

Figure 35. THD + N vs. Amplitude

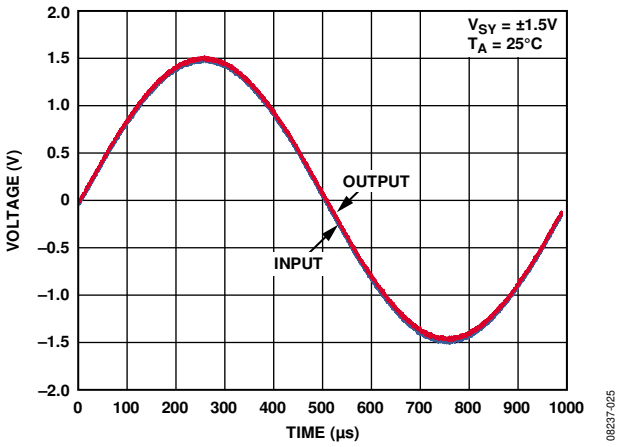

Figure 38. No Phase Reversal

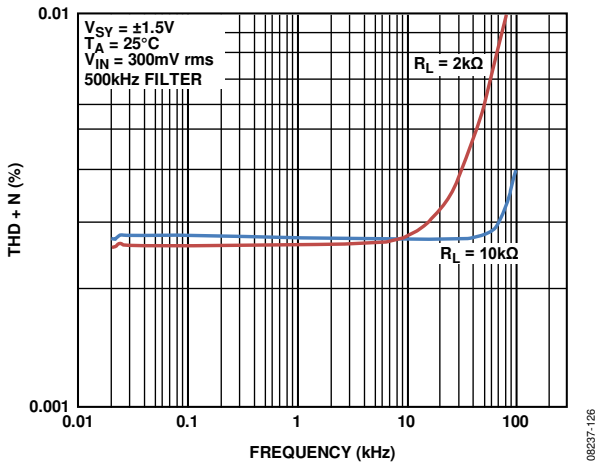

Figure 36. THD + N vs. Frequency, 500 kHz Filter

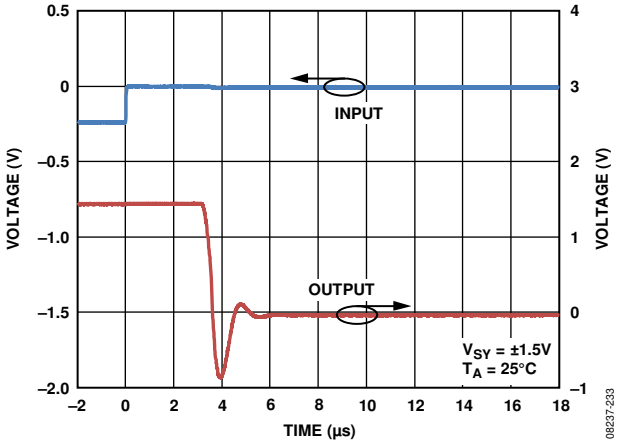

Figure 39. Positive 50% Overload Recovery

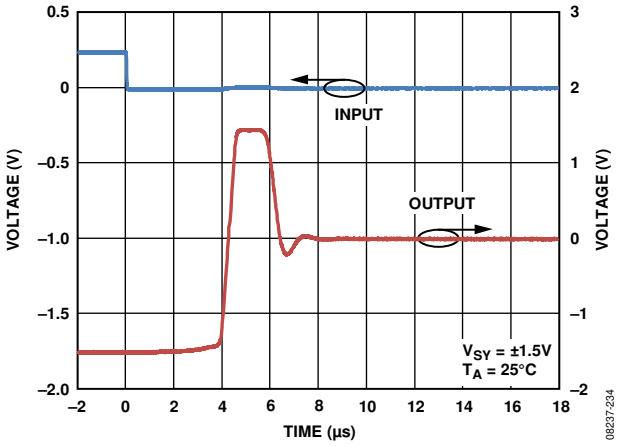

Figure 40. Negative 50% Overload Recovery

±5 V CHARACTERISTICS

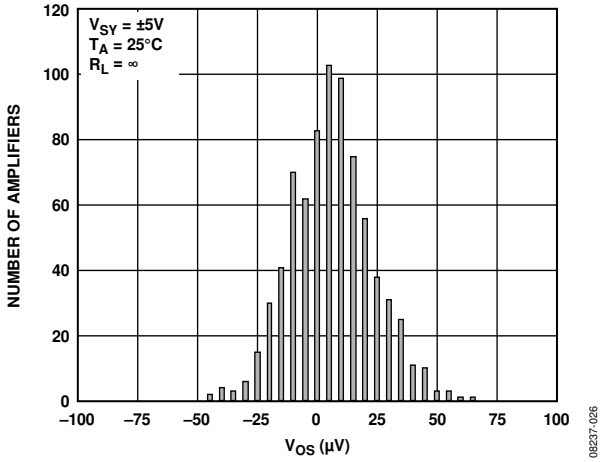

Figure 41. Input Offset Voltage (V_{OS}) Distribution, SOIC

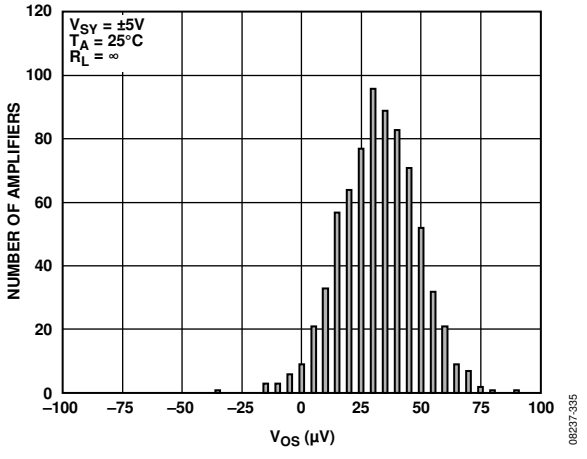

Figure 42. Input Offset Voltage (V_{OS}) Distribution, SOT-23

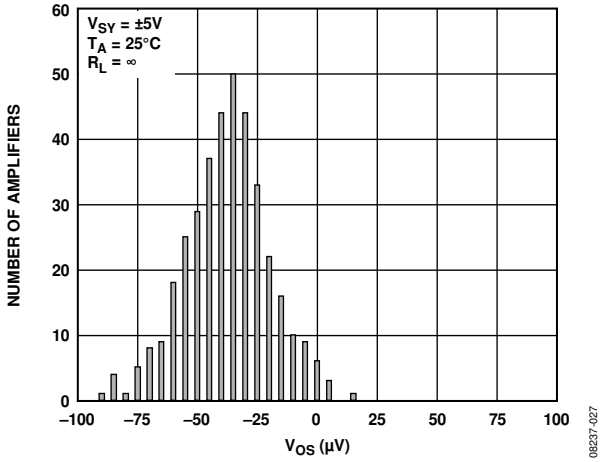

Figure 43. Input Offset Voltage (V_{OS}) Distribution, MSOP and TSSOP

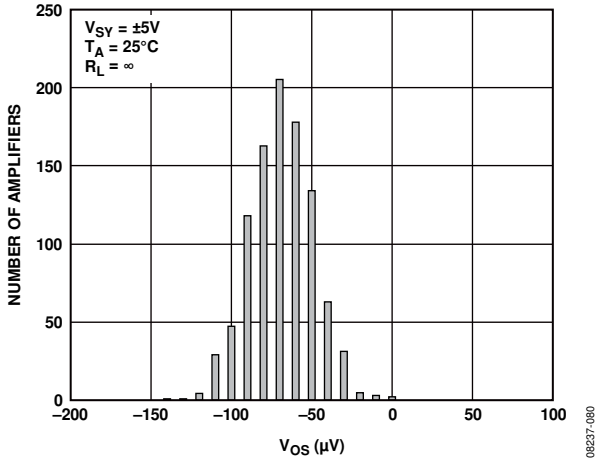

Figure 44. Input Offset Voltage (V_{OS}) Distribution, LFCSP

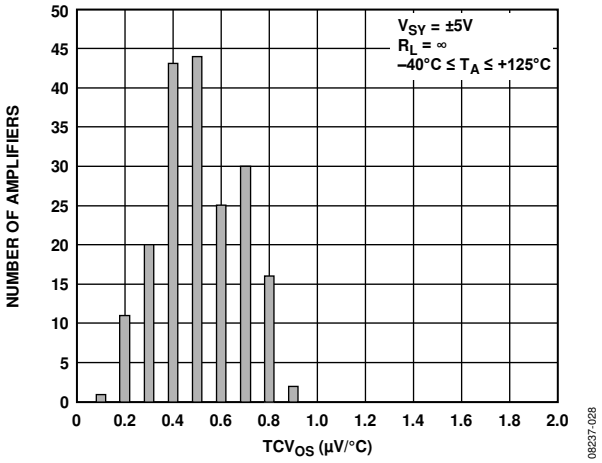

Figure 45. TCV_{OS} Distribution, SOIC, MSOP, and TSSOP

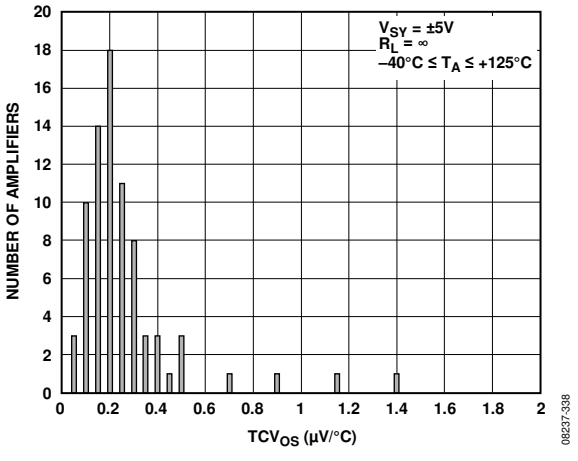

Figure 46. TCV_{OS} Distribution for SOT-23

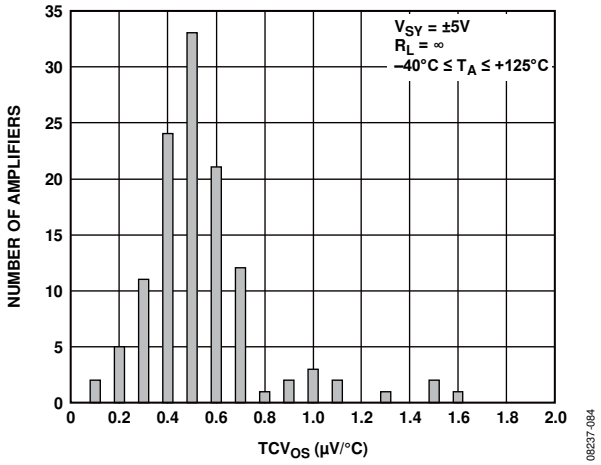

Figure 47. TCV_{OS} Distribution, LFCSP

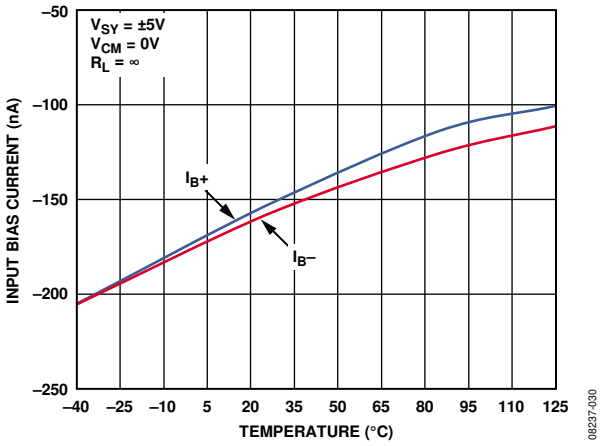

Figure 50. Input Bias Current vs. Temperature

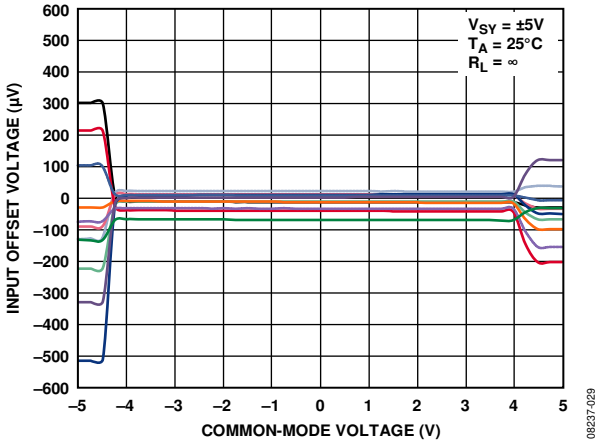

Figure 48. Input Offset Voltage vs. Common-Mode Voltage

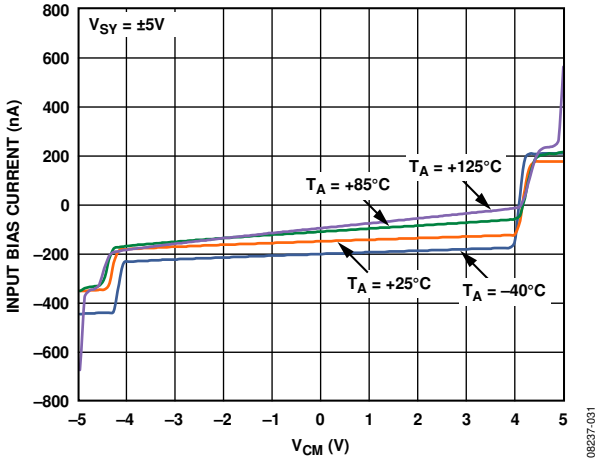

Figure 51. Input Bias Current vs. V_{CM} for Various Temperatures

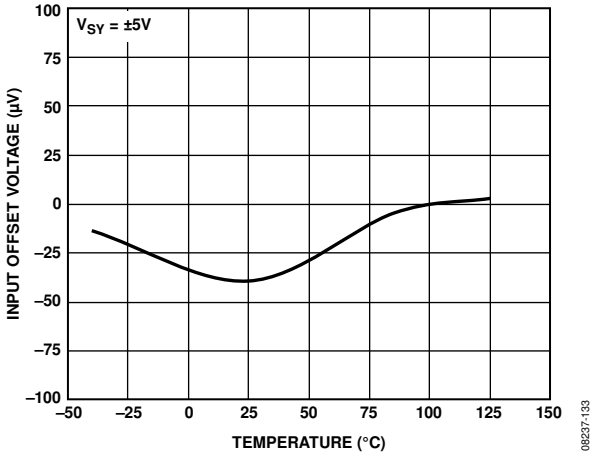

Figure 49. Input Offset Voltage vs. Temperature

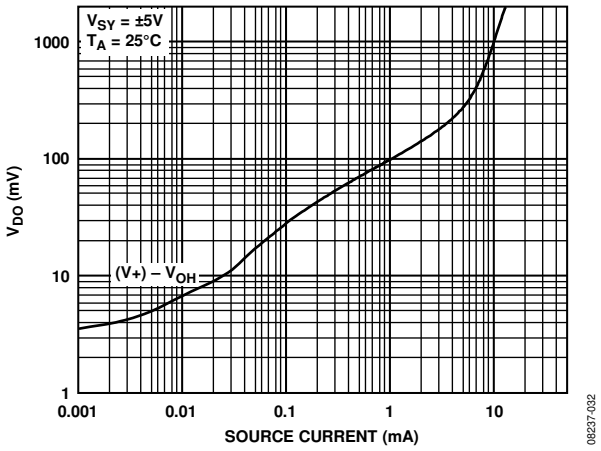

Figure 52. Dropout Voltage (V_{DO}) vs. Source Current

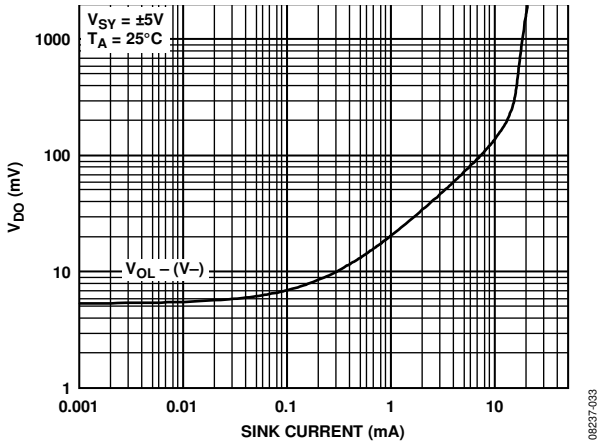

Figure 53. Dropout Voltage (V_{DO}) vs. Sink Current

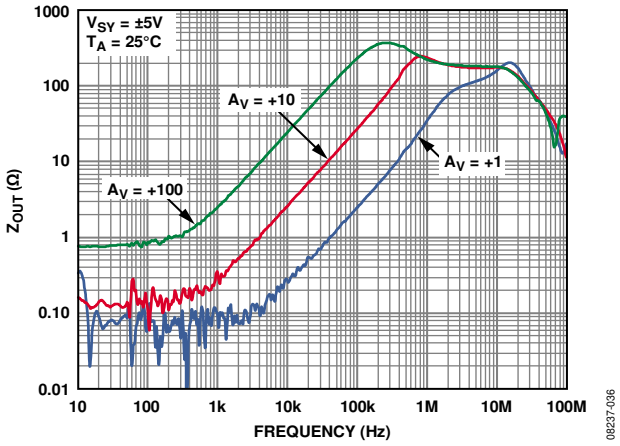

Figure 56. Output Impedance (Z_{OUT}) vs. Frequency

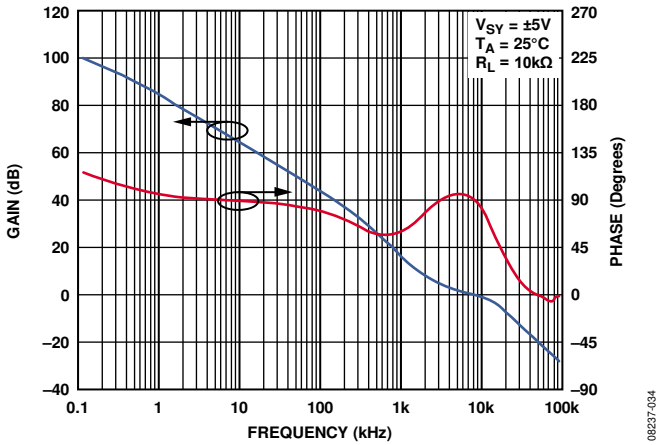

Figure 54. Open-Loop Gain and Phase vs. Frequency

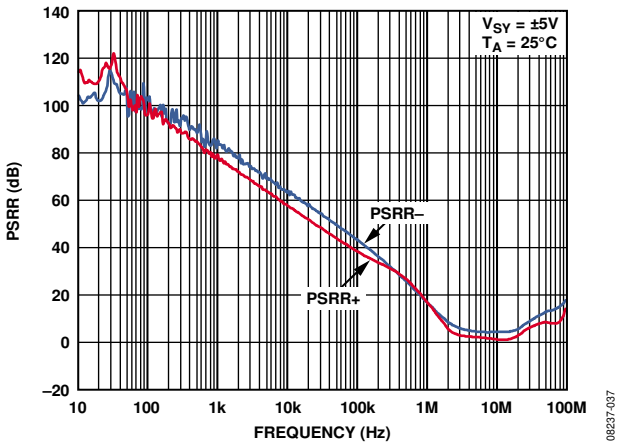

Figure 57. PSRR vs. Frequency

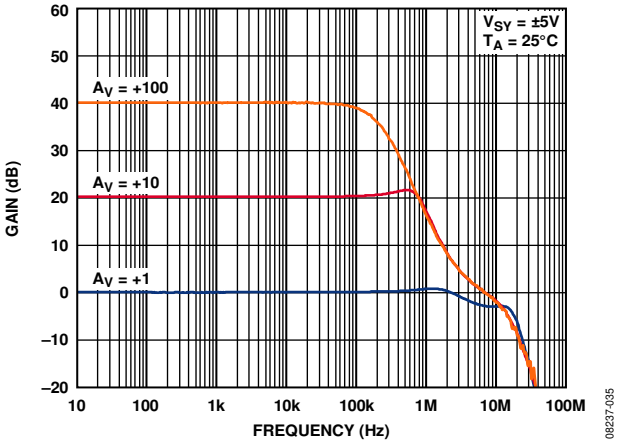

Figure 55. Closed-Loop Gain vs. Frequency

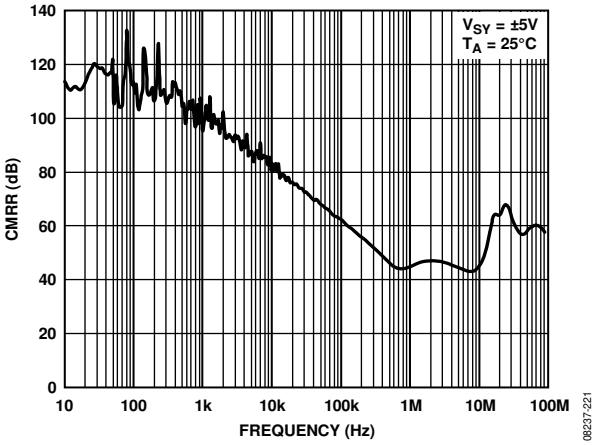

Figure 58. CMRR vs. Frequency

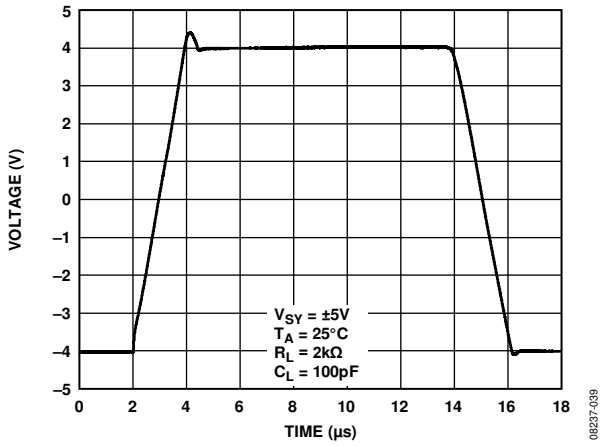

Figure 59. Large Signal Transient Response

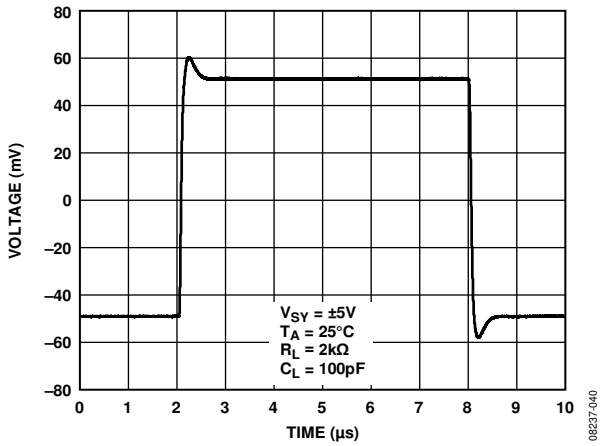

Figure 60. Small Signal Transient Response

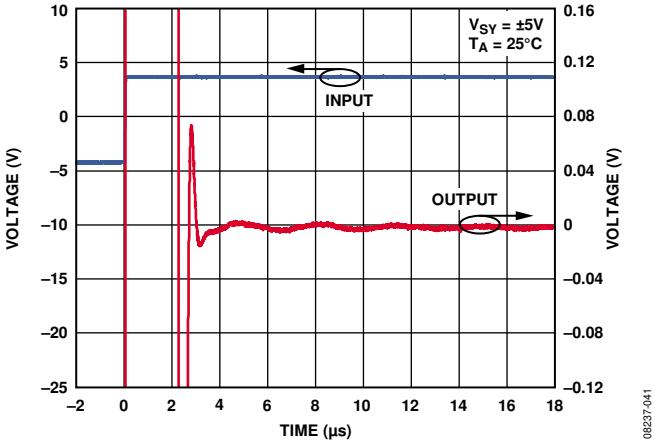

Figure 61. Settling Time

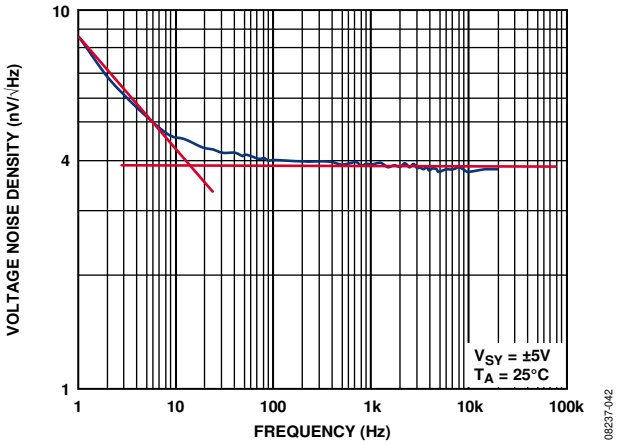

Figure 62. Voltage Noise Density vs. Frequency

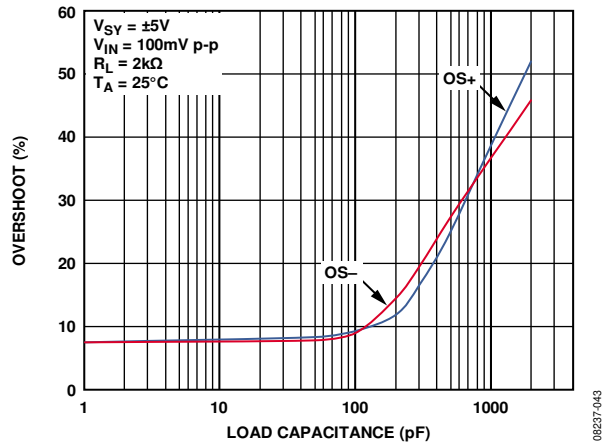

Figure 63. Overshoot vs. Load Capacitance

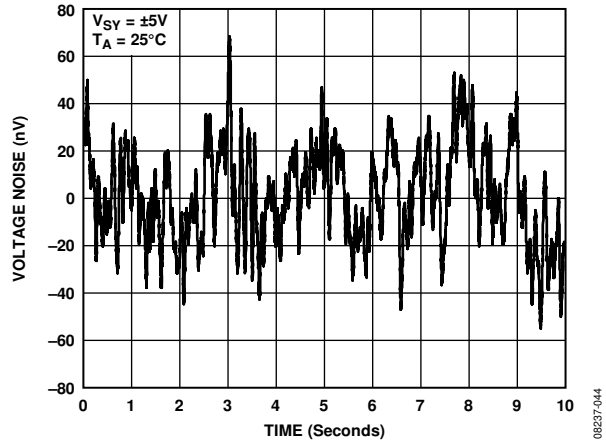

Figure 64. Voltage Noise, 0.1 Hz to 10 Hz

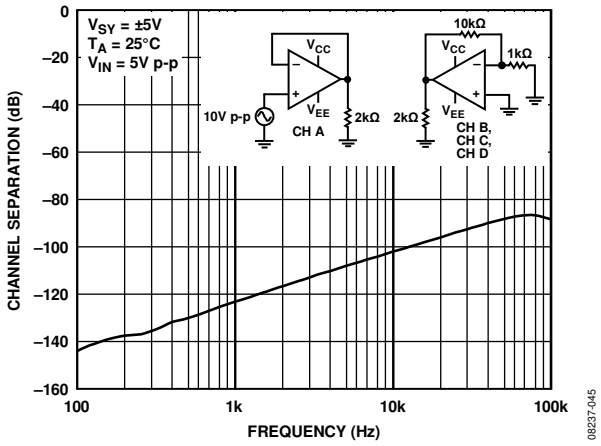

Figure 65. Channel Separation vs. Frequency

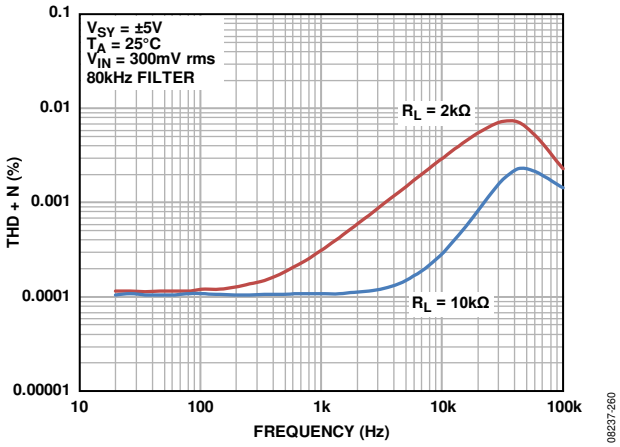

Figure 68. THD + N vs. Frequency, 80 kHz Filter

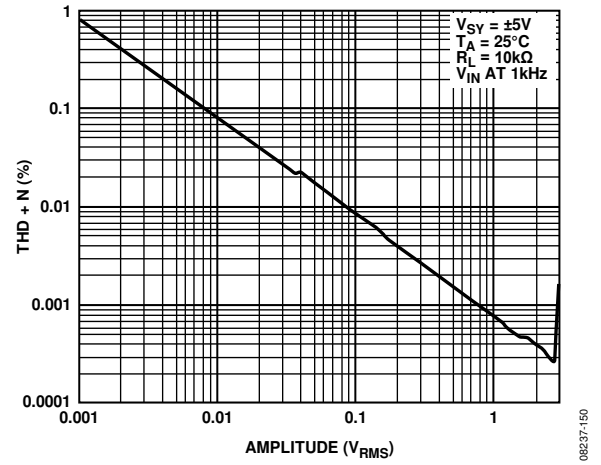

Figure 66. THD + N vs. Amplitude

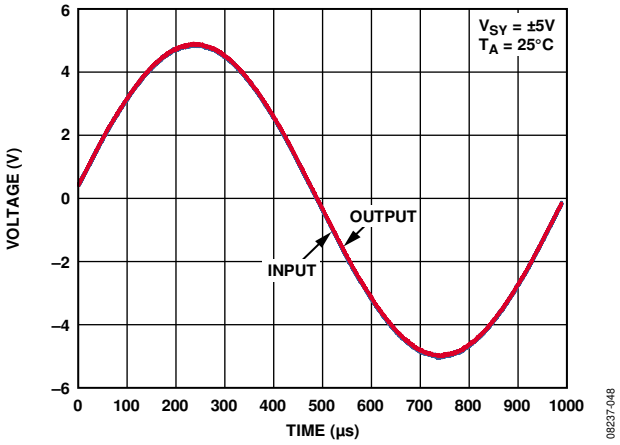

Figure 69. No Phase Reversal

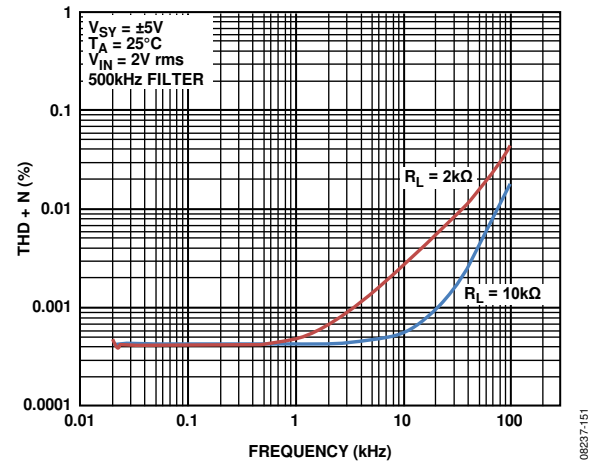

Figure 67. THD + N vs. Frequency, 500 kHz Filter

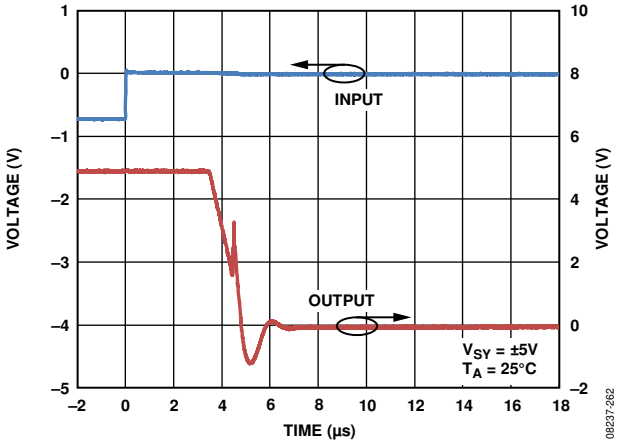

Figure 70. Positive 50% Overload Recovery

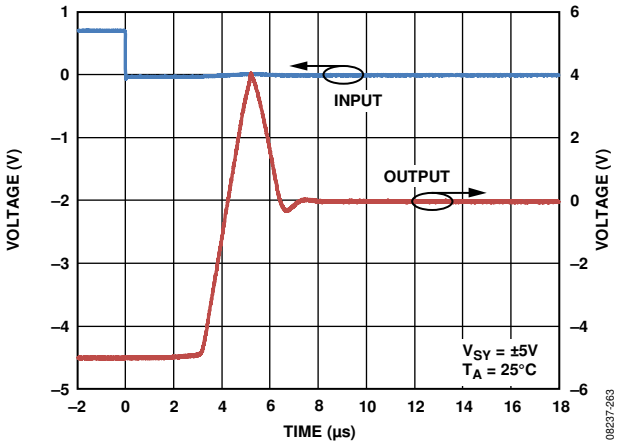

Figure 71. Negative 50% Overload Recovery

±15 V CHARACTERISTICS

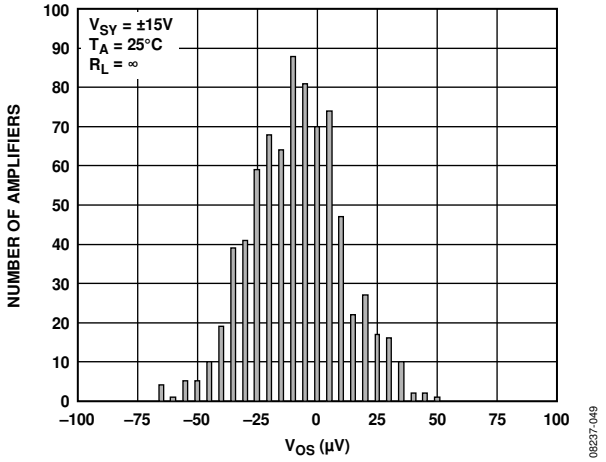

Figure 72. Input Offset Voltage (V_{OS}) Distribution, SOIC

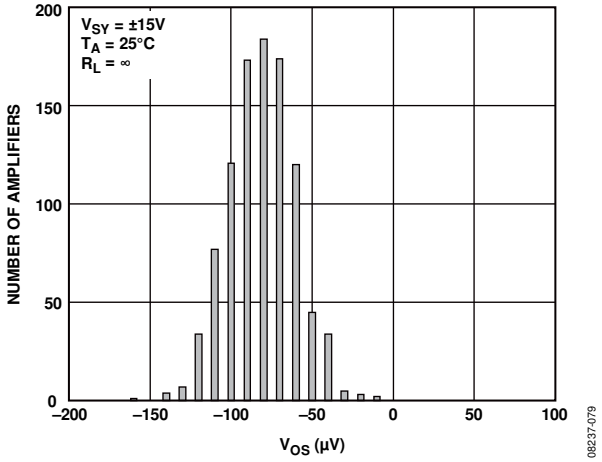

Figure 75. Input Offset Voltage (V_{OS}) Distribution, LFCSP

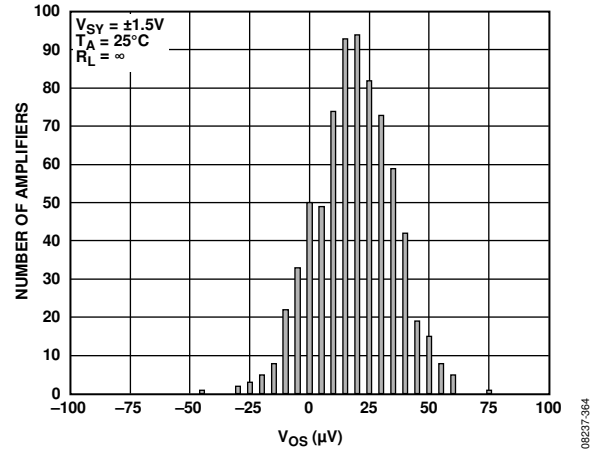

Figure 73. Input Offset Voltage (V_{OS}) Distribution, SOT-23

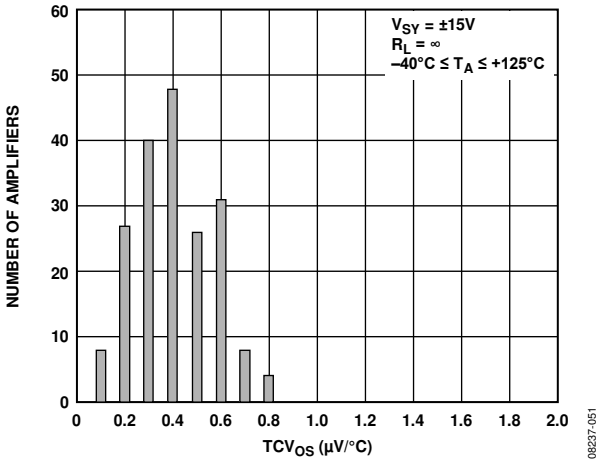

Figure 76. TCV_{OS} Distribution, SOIC, MSOP, and TSSOP

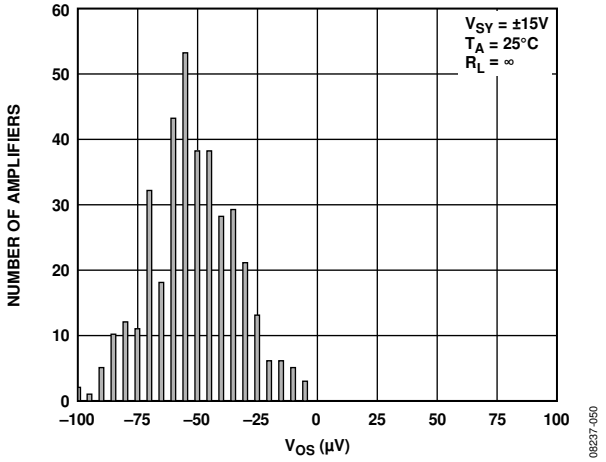

Figure 74. Input Offset Voltage (V_{OS}) Distribution, MSOP and TSSOP

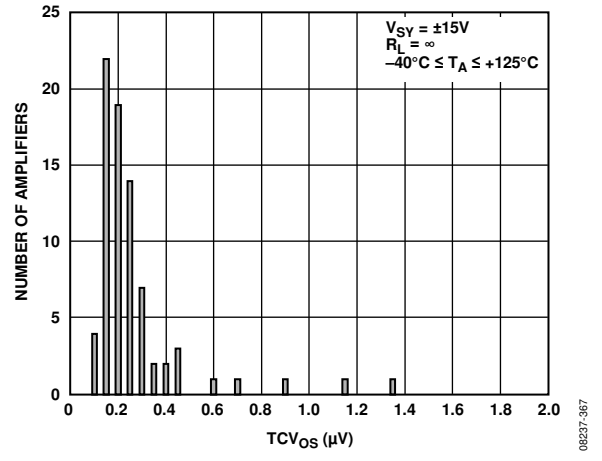

Figure 77. TCV_{OS} Distribution, SOT-23

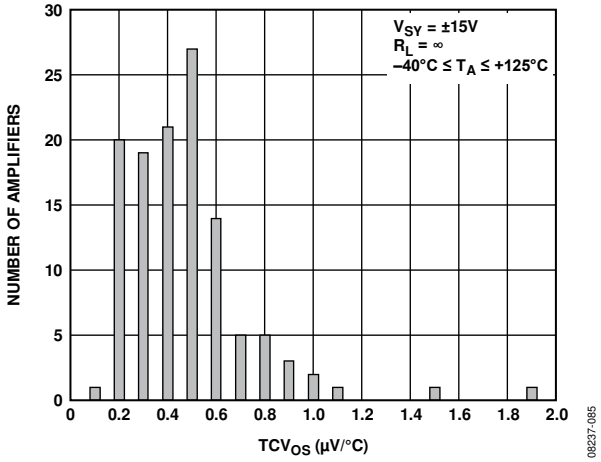

Figure 78. TCV_{OS} Distribution, LFCSP

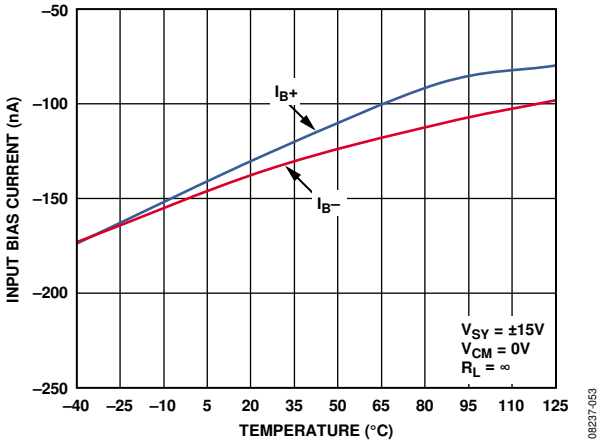

Figure 81. Input Bias Current vs. Temperature

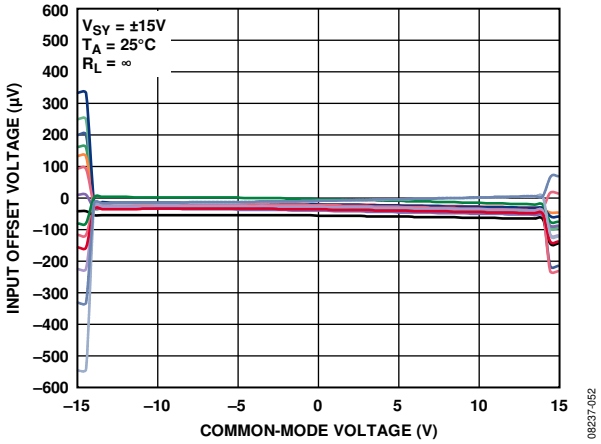

Figure 79. Input Offset Voltage vs. Common-Mode Voltage

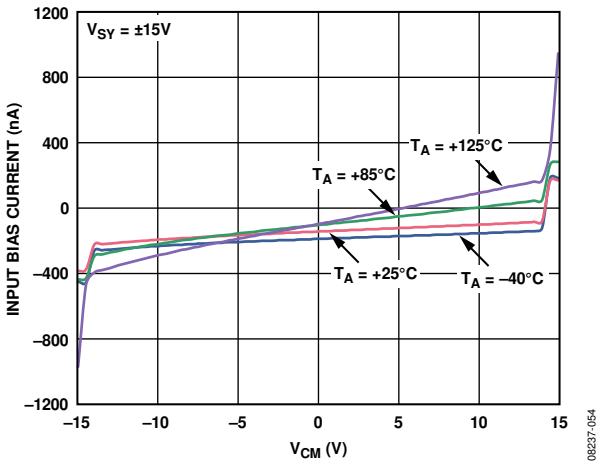

Figure 82. Input Bias Current vs. V_{CM} for Various Temperatures

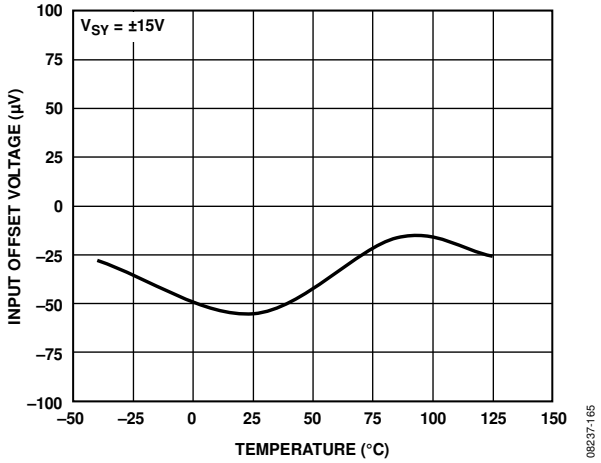

Figure 80. Input Offset Voltage vs. Temperature

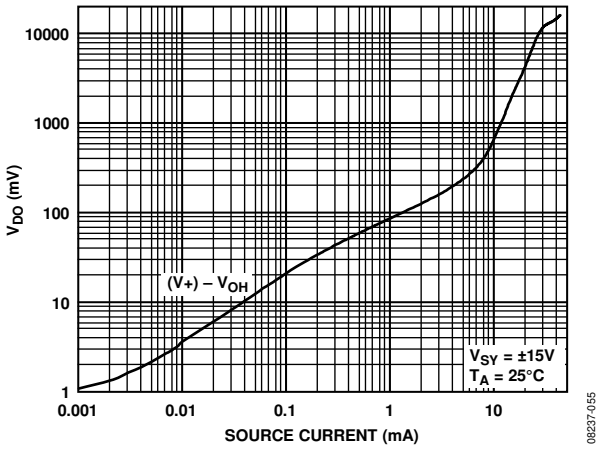

Figure 83. Dropout Voltage (V_{DO}) vs. Source Current

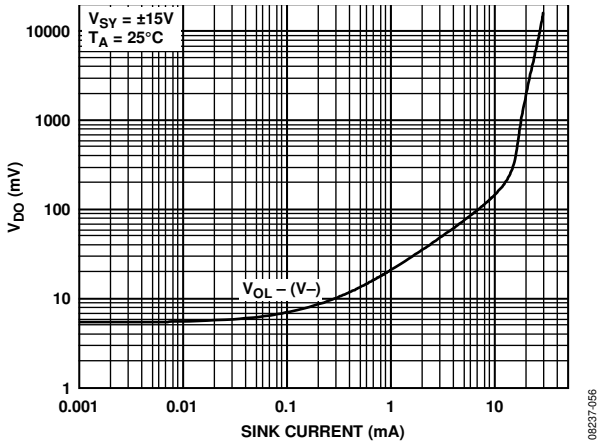

Figure 84. Dropout Voltage (V_{DO}) vs. Sink Current

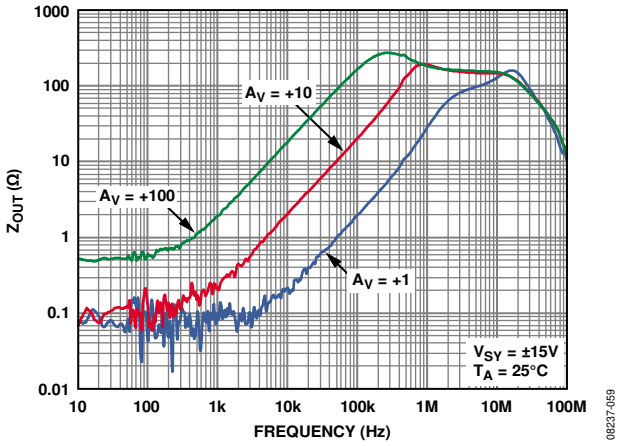

Figure 87. Output Impedance (Z_{OUT}) vs. Frequency

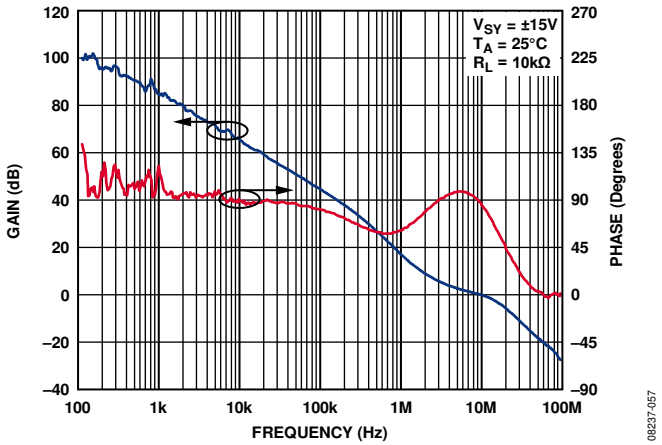

Figure 85. Open-Loop Gain and Phase vs. Frequency

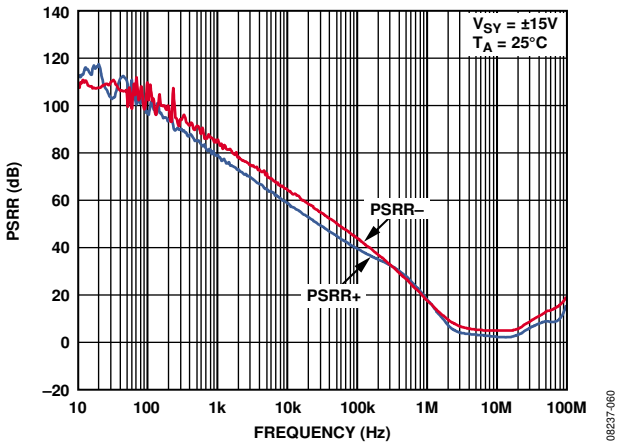

Figure 88. PSRR vs. Frequency

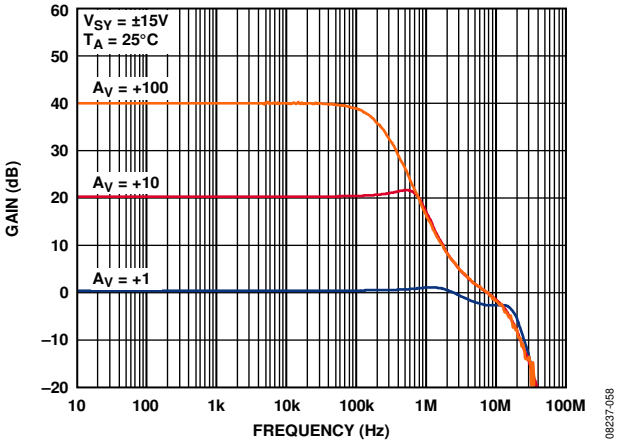

Figure 86. Closed-Loop Gain vs. Frequency

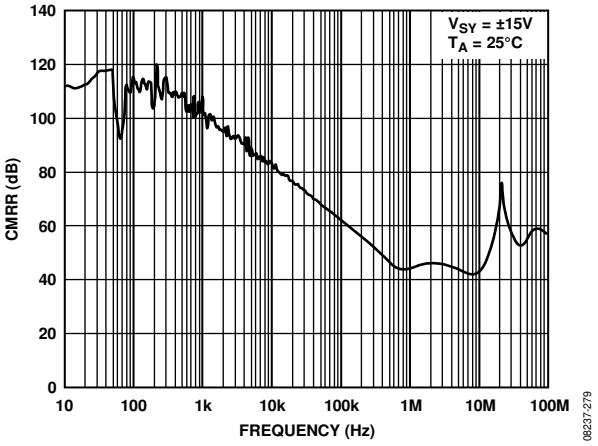

Figure 89. CMRR vs. Frequency