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ANALOG DEVICES

OVP and EMI Protected, Precision, Low Noise and Bias Current Op Amps

Data Sheet

ADA4177-1/ADA4177-2/ADA4177-4

FEATURES

- Low offset voltage: 60 μV maximum at 25°C (8-lead and 14-lead SOIC)
- Low offset voltage drift: 1 μV/°C maximum (8-lead and 14-lead SOIC)
- Low input bias current: 1 nA maximum at 25°C
- Low voltage noise density: 8 nV/√Hz typical at 1 kHz
- Large signal voltage gain (A_{VO}): 100 dB minimum over full supply voltage and operating temperature
- Input overvoltage protection to 32 V above and below the supply voltage rail
- Integrated EMI filter
  - 70 dB typical rejection at 1000 MHz
  - 90 dB typical rejection at 2400 MHz
- Rail-to-rail output swing
- Low supply current: 500 μA typical per amplifier
- Wide bandwidth
  - Gain bandwidth product (A_V = +100): 3.5 MHz typical
  - Unity-gain crossover (A_V = +1): 3.5 MHz typical
  - −3 dB bandwidth (A_V = +1): 6 MHz typical
- Dual-supply operation
  - Specified at ±5 V to ±15 V, operates over ±2.5 V to ±18 V
- Unity-gain stable
- No phase reversal

APPLICATIONS

- Wireless base station control circuits
- Optical network control circuits
- Instrumentation
- Sensors and controls
  - Thermocouples, resistor thermal detectors (RTDs), strain gages, shunt current measurements
- Precision filters

GENERAL DESCRIPTION

The ADA4177-1 single channel, ADA4177-2 dual channel, and ADA4177-4 quad channel amplifiers feature low offset voltage (2 μV typical) and drift (1 μV/°C maximum), low input bias current, low noise, and low current consumption (500 μA typical). Outputs are stable with capacitive loads of more than 1000 pF with no external compensation.

The inputs of the ADA4177-1, ADA4177-2, and ADA4177-4 set a new standard in precision amplifier robustness, providing input protection against signal excursions 32 V beyond either supply, as well as 70 dB of rejection for electromagnetic interference (EMI) at 1000 MHz.

PIN CONNECTION DIAGRAM

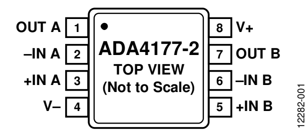

Figure 1. ADA4177-2

Applications for this amplifier include sensor signal conditioning (such as thermocouples, RTDs, and strain gages), process control front-end amplifiers, and precision diode power measurement in optical and wireless transmission systems.

The ADA4177-2 and ADA4177-4 operate over the −40°C to +125°C industrial temperature range. The ADA4177-1 and the ADA4177-2 are available in an 8-lead SOIC package and an 8-lead MSOP package. The ADA4177-4 is available in a 14-lead TSSOP and a 14-lead SOIC package.

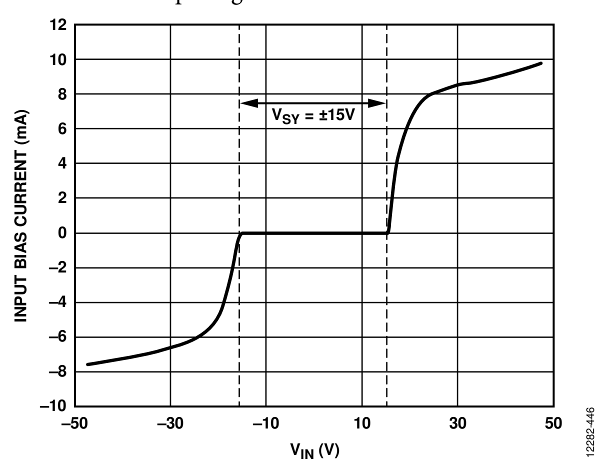

Figure 2. Overvoltage Current Limiting, Voltage Follower Configuration

Table 1. Evolution of Protected Input Op Amps by Generation[1]

Gen. 1, OVP (10 V)	Gen. 2, OVP (25 V)	Gen. 3, OVP (32 V)	Gen. 4 EMI Filters	Gen. 5, OVP (32 V) + EMI
OP191	ADA4091-2	ADA4096-2	AD8657	ADA4177-1
OP291	ADA4091-4	ADA4096-4	AD8659	ADA4177-2
OP491	ADA4092-4		AD8546	ADA4177-4
			AD8548	
			ADA4661-2	
			ADA4666-2	

[1] Gen. stands for Generation.

Rev. C   Document Feedback

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS, ±5 V

V_{SY} = ±5.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
8-Lead SOIC and 14-Lead SOIC				2	60	µV
		−40°C < T_A < +125°C			120	µV
8-Lead MSOP				3	120	µV
		−40°C < T_A < +125°C			200	µV
14-Lead TSSOP				3	150	µV
		−40°C < T_A < +125°C			300	µV
Offset Voltage Matching						
8-Lead SOIC					40	µV
8-Lead MSOP					110	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C				
8-Lead SOIC and 14-Lead SOIC					1	µV/°C
8-Lead MSOP and 14-Lead TSSOP					1.6	µV/°C
Input Bias Current	I_B		−1	−0.4	+1	nA
		−40°C < T_A < +125°C	−2		+2	nA
Input Offset Current	I_{OS}		−0.75	0.1	+0.75	nA
		−40°C < T_A < +125°C	−1.5		+1.5	nA
Input Voltage Range	IVR		−3.5		+3.5	V
Overvoltage Current Limit[1]	I_{OVP}	5 V < V_{CM} < 37 V		12		mA
		−37 V < V_{CM} < −5 V		10		mA
Common-Mode Rejection Ratio	CMRR	V_{CM} = −3.5 V to +3.5 V	122	130		dB
		−40°C < T_A < +125°C	120			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_{OUT} = −4.5 V to +4.5 V	108	110		dB
		−40°C < T_A < +125°C	100			dB
		R_L = 10 kΩ, V_{OUT} = −4.5 V to +4.5 V	115	120		dB
		−40°C < T_A < +125°C	110			dB
Input Capacitance	C_{INDM}	Differential mode		1		pF
	C_{INCM}	Common mode		1		pF
Input Resistance	R_{DIFF}	Differential mode		4		MΩ
	R_{CM}	Common mode		100		GΩ
OUTPUT CHARACTERISTICS						
Output Voltage						
High	V_{OH}	I_{LOAD} = 1 mA	4.95			V
		−40°C < T_A < +125°C	4.90			V
		I_{LOAD} = 7 mA	4.80			V
		−40°C < T_A < +125°C	4.75			V
Low	V_{OL}	I_{LOAD} = 1 mA			−4.95	V
		−40°C < T_A < +125°C			−4.90	V
		I_{LOAD} = 7 mA			−4.80	V
		−40°C < T_A < +125°C			−4.75	V
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1 V		25		mA
Short-Circuit Current	I_{SC}	T_A = 25°C				
Sourcing				36		mA
Sinking				48		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +1		0.11		Ω

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±18 V	125	145		dB
		−40°C < T_A < +125°C	120			dB
Supply Current per Amplifier	I_{SY}	V_{OUT} = 0 V		500	560	µA
		−40°C < T_A < +125°C			600	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		1.5		V/µs
Settling Time	t_S					
To 0.1%		V_{IN} = 1 V step, R_L = 2 kΩ, A_V = −1		1.8		µs
To 0.01%		V_{IN} = 1 V step, R_L = 2 kΩ, A_V = −1		3.5		µs
Gain Bandwidth Product	GBP	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +100		3.5		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		3.5		MHz
−3 dB Closed-Loop Bandwidth	$f_{-3\,dB}$	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		6		MHz
Total Harmonic Distortion Plus Noise	THD + N	V_{IN} = 1 V rms, R_L = 2 kΩ, A_V = +1, f = 1 kHz		0.003		%
EMI Rejection of +IN x	EMIRR	V_{IN} = 200 mV p-p				
f = 1000 MHz				70		dB
f = 2400 MHz				90		dB
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		175		nV p-p
Voltage Noise Density	e_n	f = 10 Hz		10		nV/√Hz
		f = 1 kHz		8		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.2		pA/√Hz

[1] All inputs are stressed to 32 V beyond supplies for 500 ms. See Figure 71 for the typical input bias current vs. the input voltage over the overvoltage protected input range.

ELECTRICAL CHARACTERISTICS, ±15 V

V_{SY} = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
8-Lead SOIC and 14-Lead SOIC				2	60	µV
		−40°C < T_A < +125°C			120	µV
8-Lead MSOP				3	120	µV
		−40°C < T_A < +125°C			200	µV
14-Lead TSSOP				3	150	µV
		−40°C < T_A < +125°C			300	µV
Offset Voltage Matching						
8-Lead SOIC					40	µV
8-Lead MSOP					110	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C				
8-Lead SOIC and 14-Lead SOIC					1	µV/°C
8-Lead MSOP and 14-Lead TSSOP					1.6	µV/°C
Input Bias Current	I_B		−1	−0.3	+1	nA
		−40°C < T_A < +125°C	−2		+2	nA
Input Offset Current	I_{OS}		−0.75	0.1	+0.75	nA
		−40°C < T_A < +125°C	−1.5		+1.5	nA
Input Voltage Range	IVR		−13.5		+13.5	V
Overvoltage Current Limit[1]	I_{OVP}	15 V < V_{CM} < 47 V		12		mA
		−47 V < V_{CM} < −15 V		10		mA
Common-Mode Rejection Ratio	CMRR	V_{CM} = −13.5 V to +13.5 V	128	130		dB
		−40°C < T_A < +125°C	125			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_{OUT} = −14.2 V to +14.2 V	110	114		dB
		−40°C < T_A < +125°C	103			dB
		R_L = 10 kΩ, V_{OUT} = −14.5 V to +14.5 V	118	120		dB
		−40°C < T_A < +125°C	110			dB
Input Capacitance	C_{INDM}	Differential mode		1		pF
	C_{INCM}	Common mode		1		pF
Input Resistance	R_{DIFF}	Differential mode		4		MΩ
	R_{CM}	Common mode		130		GΩ
OUTPUT CHARACTERISTICS						
Output Voltage						
High	V_{OH}	I_{LOAD} = 1 mA	14.95			V
		−40°C < T_A < +125°C	14.90			V
		I_{LOAD} = 7 mA	14.80			V
		−40°C < T_A < +125°C	14.75			V
Low	V_{OL}	I_{LOAD} = 1 mA			−14.95	V
		−40°C < T_A < +125°C			−14.90	V
		I_{LOAD} = 7 mA			−14.80	V
		−40°C < T_A < +125°C			−14.75	V
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1 V		25		mA
Short-Circuit Current	I_{SC}	T_A = 25°C				
Sourcing				53		mA
Sinking				65		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +1		0.08		Ω

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±18 V	125	145		dB
		−40°C < T_A < +125°C	120			dB
Supply Current per Amplifier	I_{SY}	V_{OUT} = 0 V		500	580	µA
		−40°C < T_A < +125°C			620	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		1.5		V/µs
Settling Time	t_S					
To 0.1%		V_{IN} = 10 V p-p, R_L = 2 kΩ, A_V = −1		5.5		µs
To 0.01%		V_{IN} = 10 V p-p, R_L = 2 kΩ, A_V = −1		7.5		µs
Gain Bandwidth Product	GBP	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +100		3.5		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		3.5		MHz
−3 dB Closed-Loop Bandwidth	$f_{-3 dB}$	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		6		MHz
Total Harmonic Distortion Plus Noise	THD + N	V_{IN} = 1 V rms, A_V = +1, R_L = 2 kΩ, f = 1 kHz		0.002		%
EMI Rejection of +IN x	EMIRR	V_{IN} = 200 mV p-p				
f = 1000 MHz				70		dB
f = 2400 MHz				90		dB
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		175		nV p-p
Voltage Noise Density	e_n	f = 10 Hz		10		nV/√Hz
		f = 1 kHz		8		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.2		pA/√Hz
MULTIPLE AMPLIFIERS CHANNEL SEPARATION	C_S	f = 1 kHz		127		dB

[1] All inputs are stressed to 32 V beyond supplies for 500 ms. See Figure 74 for the typical input bias current vs. the input voltage over the overvoltage protected input range.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	V_{SY} ± 32 V
Differential Input Voltage	$\pm V_{SY}$
Output Short-Circuit Duration to GND	See the Maximum Power Dissipation section
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature, Soldering (10 sec)[1]	300°C
ESD	
Human Body Model (HBM)[2]	4 kV
Field Induced Charged Device Model (FICDM)[3]	1250 V
Machine Model (MM)	200 V

[1] IPC/JEDEC J-STS-020D applicable standard.
[2] ESDA/JEDEC JS-001-2011 applicable standard.
[3] JESD22-C101 (ESD FICDM standard of JEDEC) applicable standard.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

MAXIMUM POWER DISSIPATION

The ADA4177-1, ADA4177-2, and ADA4177-4 can drive a short-circuit output current of up to 65 mA. However, the usable output load current drive is limited by the maximum power dissipation allowed by the device package. The absolute maximum junction temperature is 150°C (see Table 4). The junction temperature can be estimated as follows:

$$T_J = P_D \times \theta_{JA} + T_A$$

where:
T_J is the die junction temperature.
P_D is the power dissipated in the package.
θ_{JA} is the thermal resistance of the package.
T_A is the ambient temperature.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated by the output stage transistor. It is calculated as follows:

$$P_D = (V_{SY} \times I_{SY}) + (V_{SY} - V_{OUT}) \times I_{LOAD}$$

where:
V_{SY} is the power supply rail.
I_{SY} is the quiescent current.
V_{OUT} is the output of the amplifier.
I_{LOAD} is the output load.

Do not exceed the 150°C maximum junction temperature for the device. Exceeding the junction temperature limit can cause degradation in the parametric performance or even destroy the device. Refer to Technical Article MS-2251, *Data Sheet Intricacies—Absolute Maximum Ratings and Thermal Resistances*, for more information.

THERMAL RESISTANCE

Thermal resistance between junction and ambient (θ_{JA}) is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP	190	44	°C/W
8-Lead SOIC	158	43	°C/W
14-Lead TSSOP	240	43	°C/W
14-Lead SOIC	115	36	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

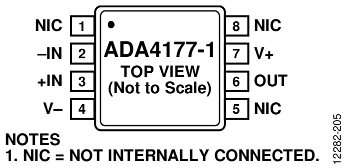

Figure 3. 8-Lead MSOP Pin Configuration, ADA4177-1

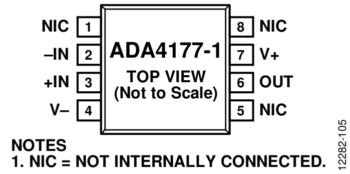

Figure 4. 8-Lead SOIC Pin Configuration, ADA4177-1

Table 6. ADA4177-1 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5, 8	NIC	Not Internally Connected.
2	−IN	Inverting Input Channel.
3	+IN	Noninverting Input Channel.
4	V−	Negative Supply Voltage.
6	OUT	Output Channel.
7	V+	Positive Supply Voltage.

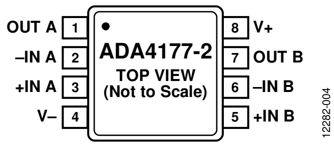

Figure 5. 8-Lead MSOP Pin Configuration, ADA4177-2

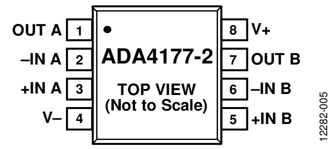

Figure 6. 8-Lead SOIC Pin Configuration, ADA4177-2

Table 7. ADA4177-2 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output Channel A.
2	−IN A	Inverting Input Channel A.
3	+IN A	Noninverting Input Channel A.
4	V−	Negative Supply Voltage.
5	+IN B	Noninverting Input Channel B.
6	−IN B	Inverting Input Channel B.
7	OUT B	Output Channel B.
8	V+	Positive Supply Voltage.

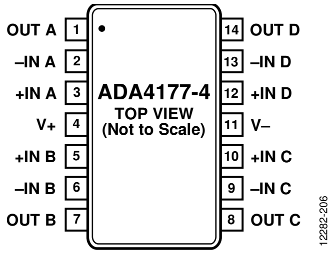

Figure 7. 14-Lead TSSOP Pin Configuration, ADA4177-4

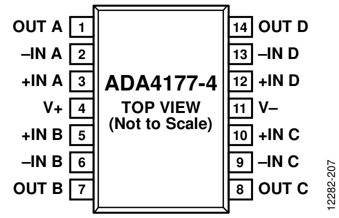

Figure 8. 14-Lead SOIC Pin Configuration, ADA4177-4

Table 8. ADA4177-4 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output Channel A.
2	−IN A	Inverting Input Channel A.
3	+IN A	Noninverting Input Channel A.
4	V+	Positive Supply Voltage.
5	+IN B	Noninverting Input Channel B.
6	−IN B	Inverting Input Channel B.
7	OUT B	Output Channel B.
8	OUT C	Output Channel C.
9	−IN C	Inverting Input Channel C.
10	+IN C	Noninverting Input Channel C.
11	V−	Negative Supply Voltage.
12	+IN D	Noninverting Input Channel D.
13	−IN D	Inverting Input Channel D.
14	OUT D	Output Channel D.

TYPICAL PERFORMANCE CHARACTERISTICS

Ambient temperature (T_A) = 25°C unless otherwise noted.

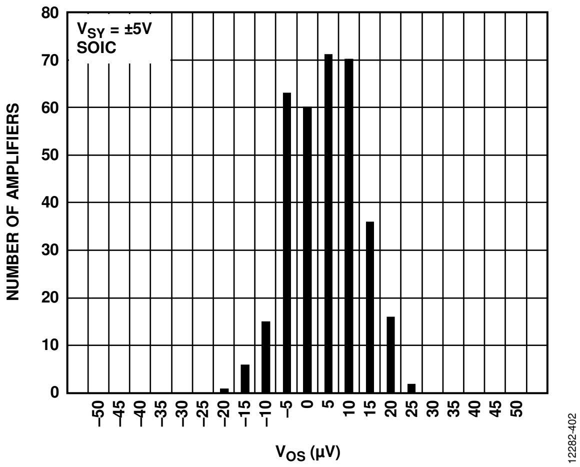

Figure 9. Input Offset Voltage (V_{OS}) Distribution, V_{SY} = ±5 V, 8-Lead SOIC

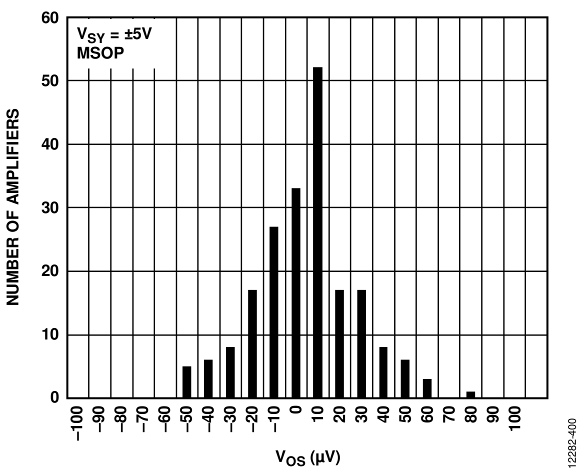

Figure 10. Input Offset Voltage (V_{OS}) Distribution, V_{SY} = ±5 V, 8-Lead MSOP

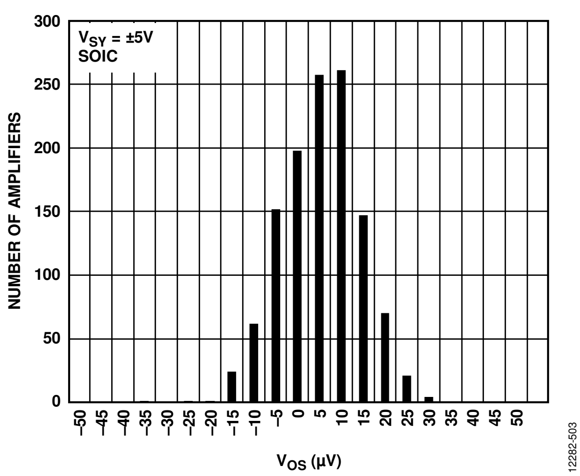

Figure 11. Input Offset Voltage (V_{OS}) Distribution, V_{SY} = ±5 V, 14-Lead SOIC

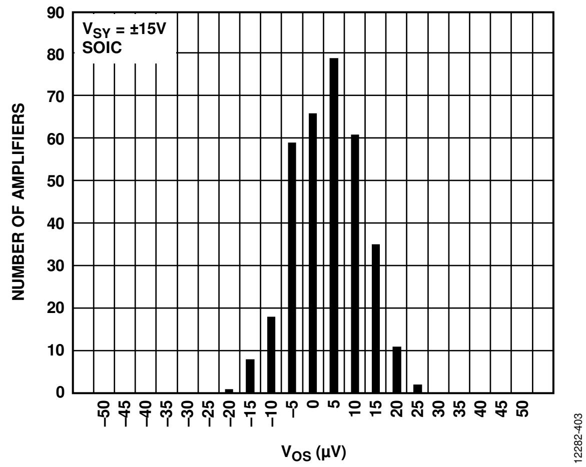

Figure 12. Input Offset Voltage (V_{OS}) Distribution, V_{SY} = ±15 V, 8-Lead SOIC

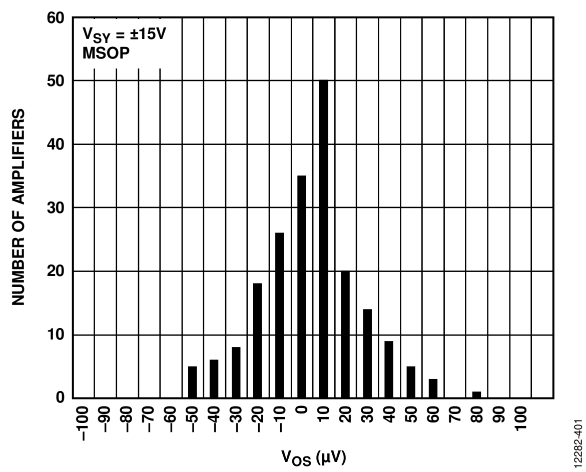

Figure 13. Input Offset Voltage (V_{OS}) Distribution, V_{SY} = ±15 V, 8-Lead MSOP

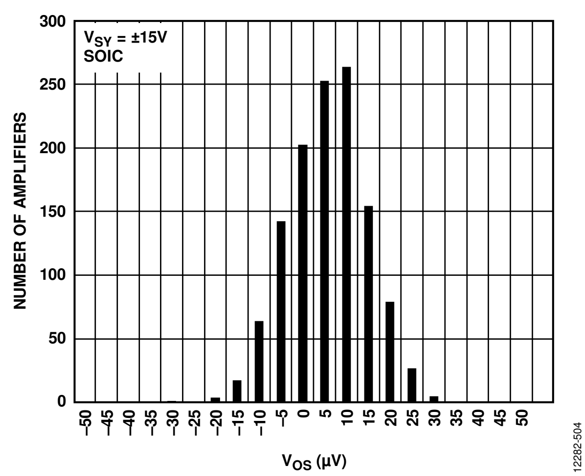

Figure 14. Input Offset Voltage (V_{OS}) Distribution, V_{SY} = ±15 V, 14-Lead SOIC

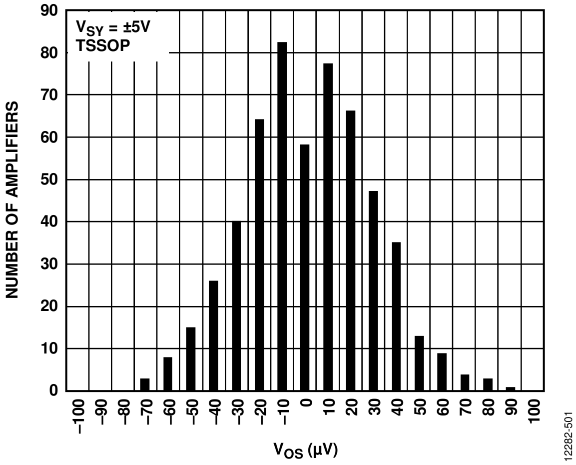

Figure 15. Input Offset Voltage (V_{OS}) Distribution, V_{SY} = ±5 V, 14-Lead TSSOP

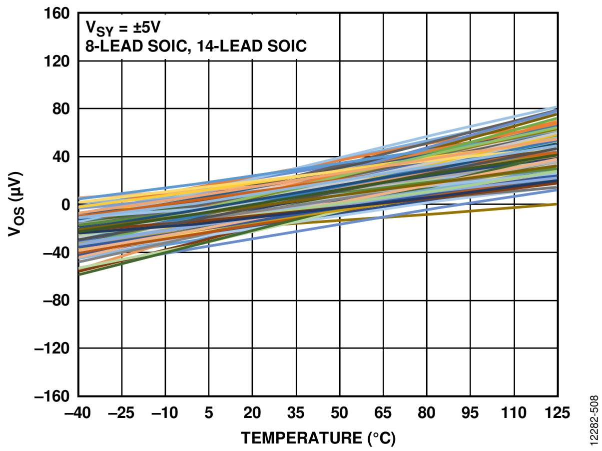

Figure 16. Input Offset Voltage (V_{OS}) vs. Temperature, V_{SY} = ±5 V, 8-Lead SOIC and 14-Lead SOIC

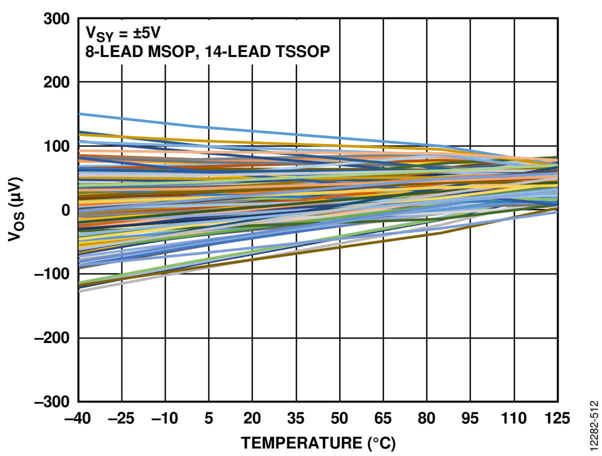

Figure 17. Input Offset Voltage (V_{OS}) vs. Temperature, V_{SY} = ±5 V, 8-Lead MSOP and 14-Lead TSSOP

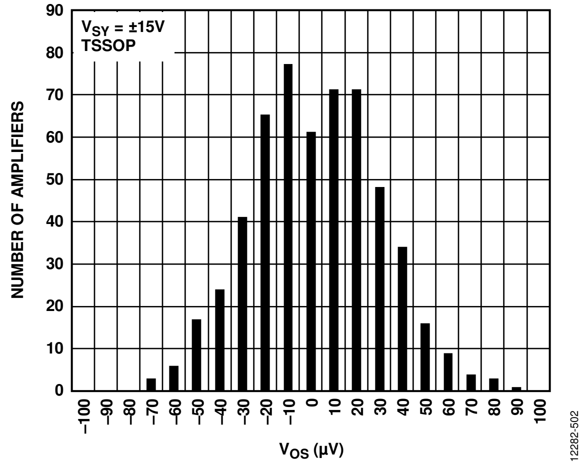

Figure 18. Input Offset Voltage (V_{OS}) Distribution, V_{SY} = ±15 V, 14-Lead TSSOP

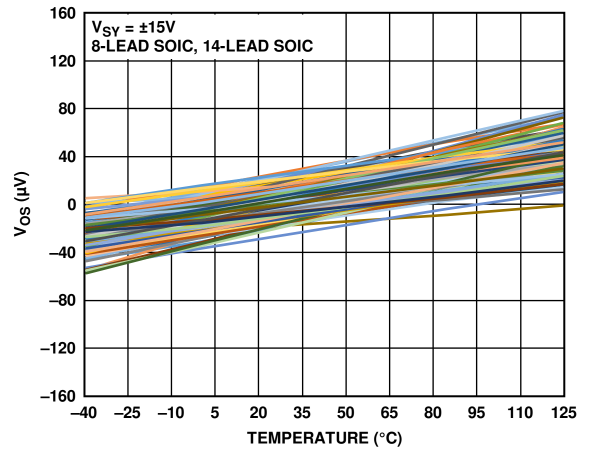

Figure 19. Input Offset Voltage (V_{OS}) vs. Temperature, V_{SY} = ±15 V, 8-Lead SOIC and 14-Lead SOIC

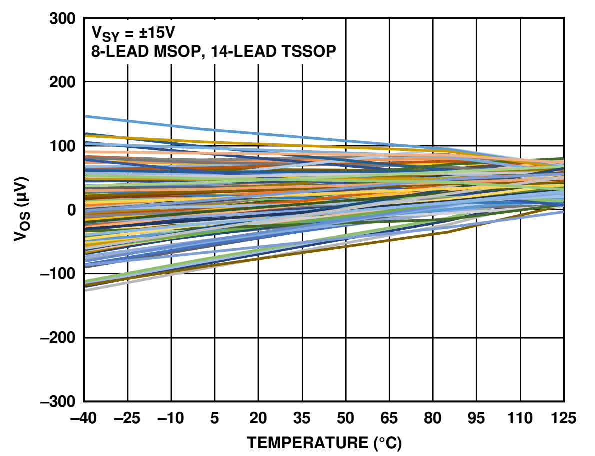

Figure 20. Input Offset Voltage (V_{OS}) vs. Temperature, V_{SY} = ±15 V, 8-Lead MSOP and 14-Lead TSSOP

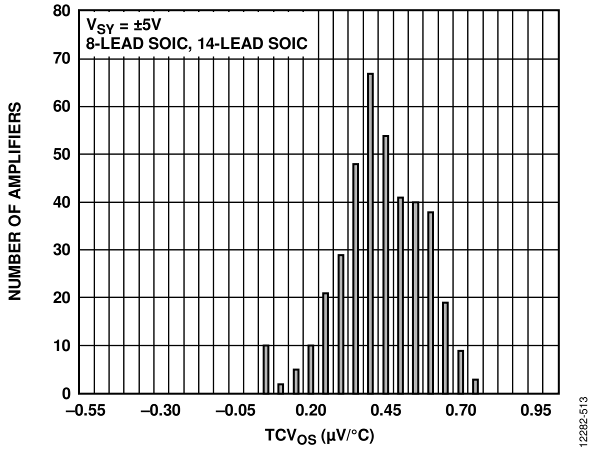

Figure 21. Temperature Coefficient of Offset Voltage (TCV_{OS}), V_{SY} = ±5 V, 8-Lead SOIC and 14-Lead SOIC

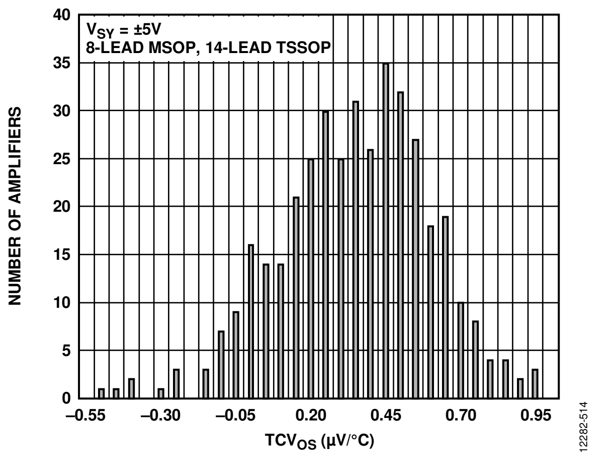

Figure 22. Temperature Coefficient of Offset Voltage (TCV_{OS}), V_{SY} = ±5 V, 8-Lead MSOP and 14-Lead TSSOP

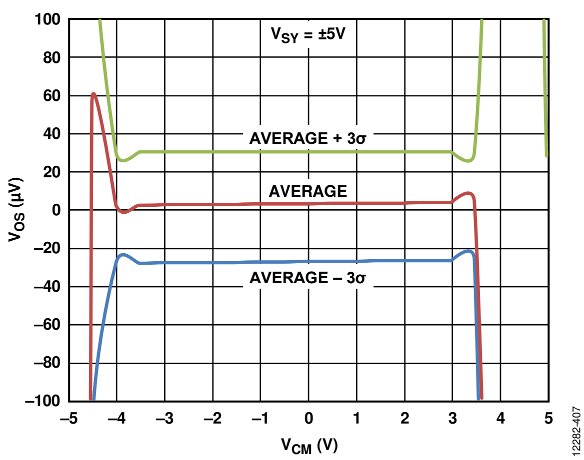

Figure 23. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = ±5 V

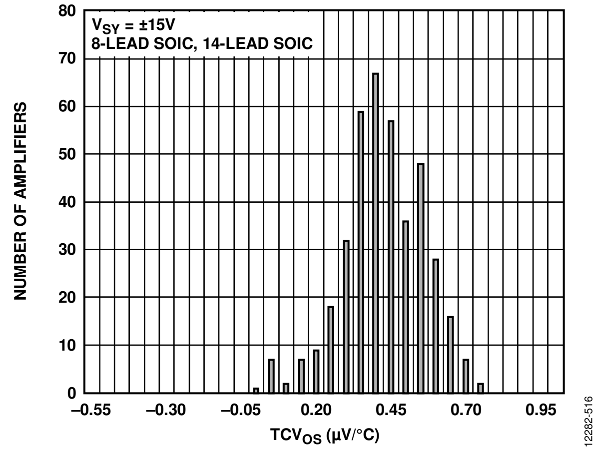

Figure 24. Temperature Coefficient of Offset Voltage (TCV_{OS}), V_{SY} = ±15 V, 8-Lead SOIC and 14-Lead SOIC

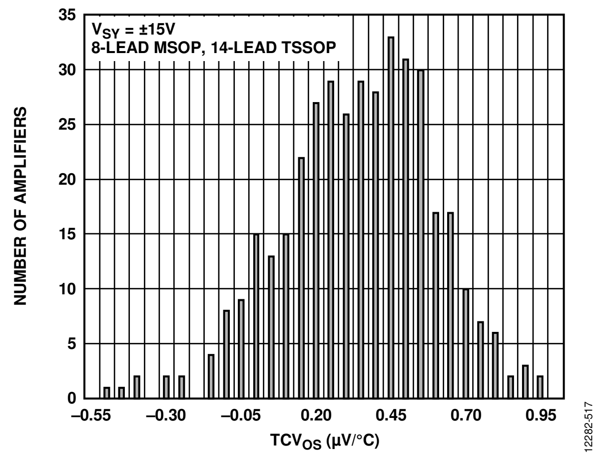

Figure 25. Temperature Coefficient of Offset Voltage (TCV_{OS}), V_{SY} = ±15 V, 8-Lead MSOP and 14-Lead TSSOP

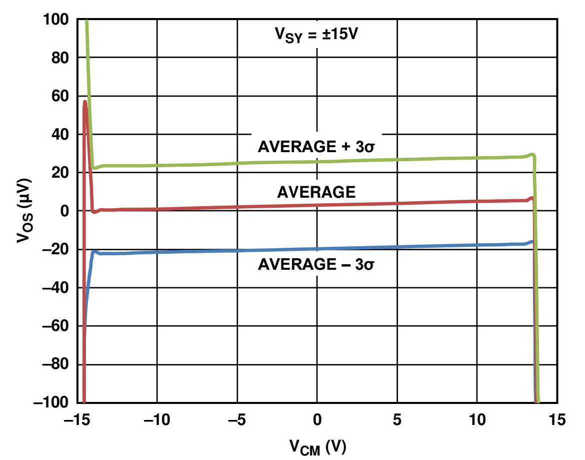

Figure 26. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), V_S = ±15 V

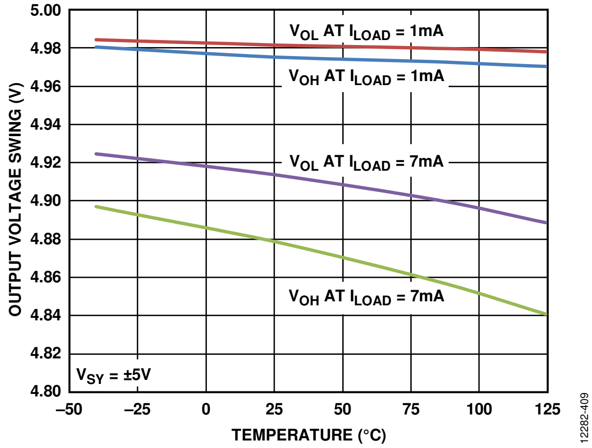

Figure 27. Output Voltage Swing vs. Temperature, V_{SY} = ±5 V

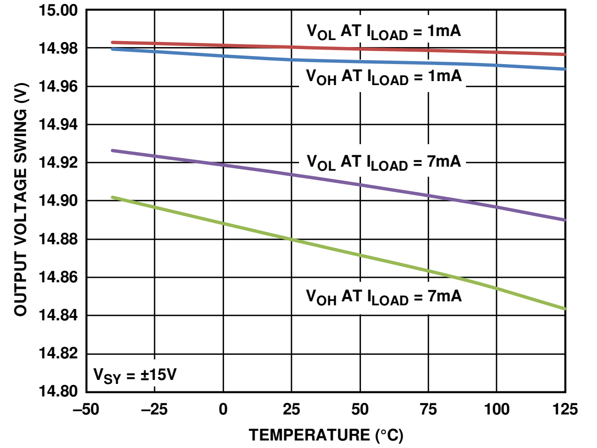

Figure 30. Output Voltage Swing vs. Temperature, V_{SY} = ±15 V

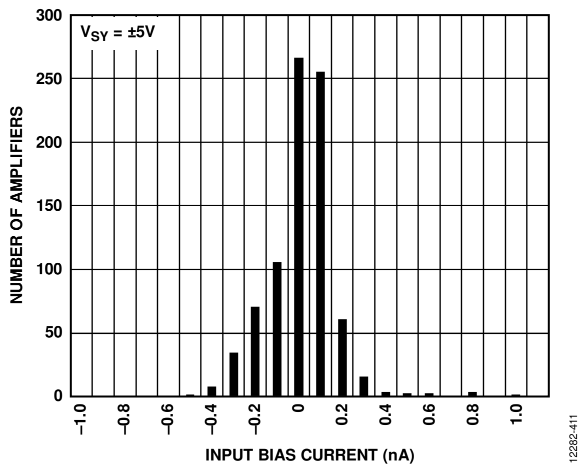

Figure 28. Input Bias Current Distribution, V_{SY} = ±5 V

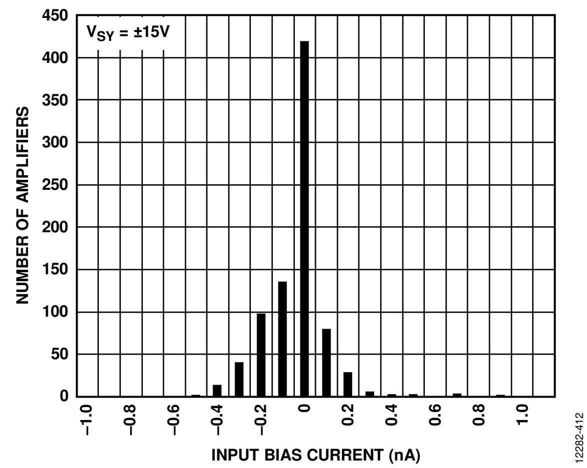

Figure 31. Input Bias Current Distribution, V_{SY} = ±15 V

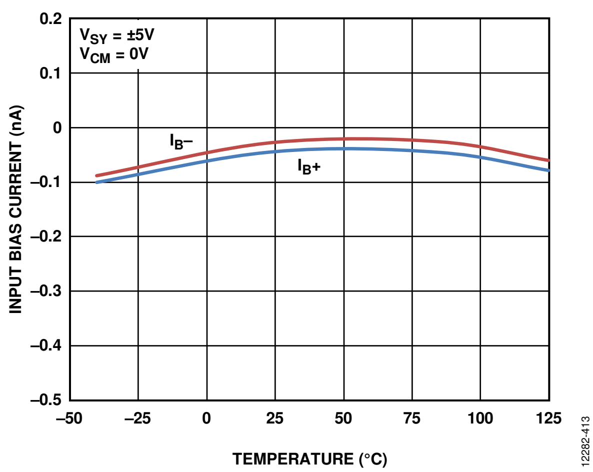

Figure 29. Input Bias Current (I_B) vs. Temperature, V_{SY} = ±5 V

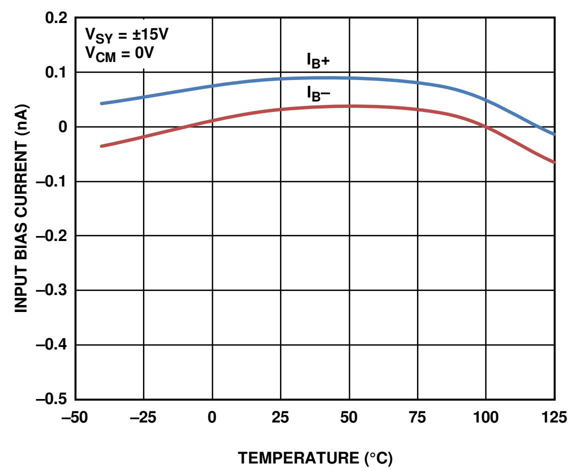

Figure 32. Input Bias Current (I_B) vs. Temperature, V_{SY} = ±15 V

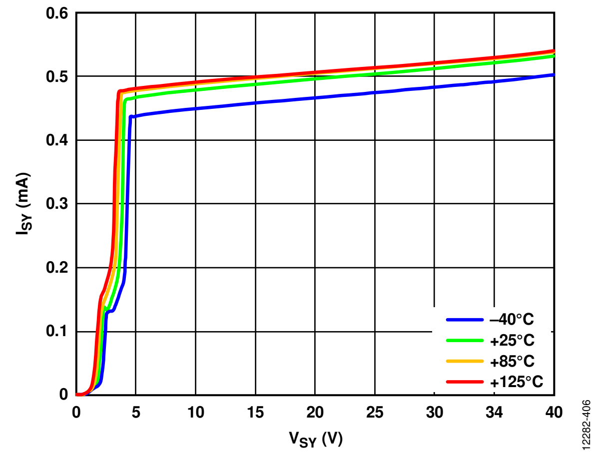

Figure 33. Supply Current per Amplifier (I_{SY}) vs. Power Supply Voltage (V_{SY})

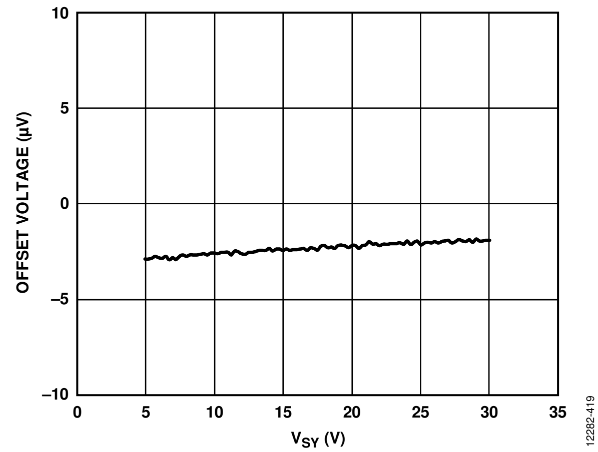

Figure 36. Offset Voltage (V_{OS}) vs. Power Supply Voltage (V_{SY})

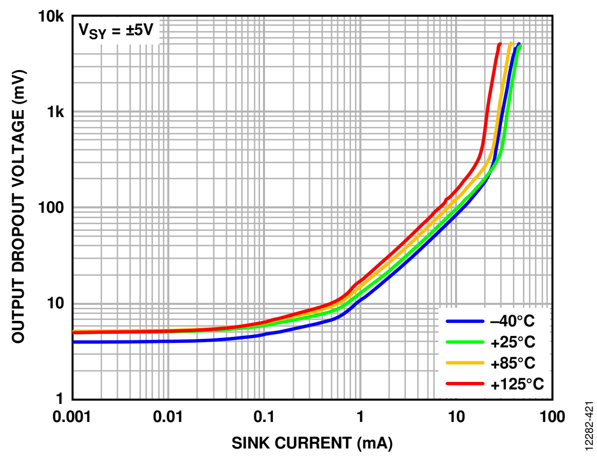

Figure 34. Output Dropout Voltage vs. Sink Current, V_{SY} = ±5 V

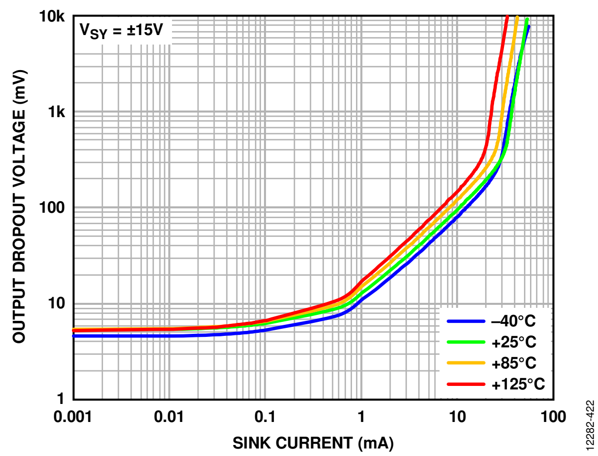

Figure 37. Output Dropout Voltage vs. Sink Current, V_{SY} = ±15 V

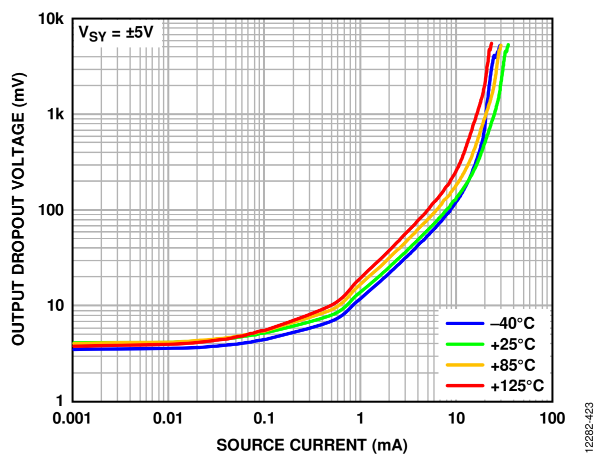

Figure 35. Output Dropout Voltage vs. Source Current, V_{SY} = ±5 V

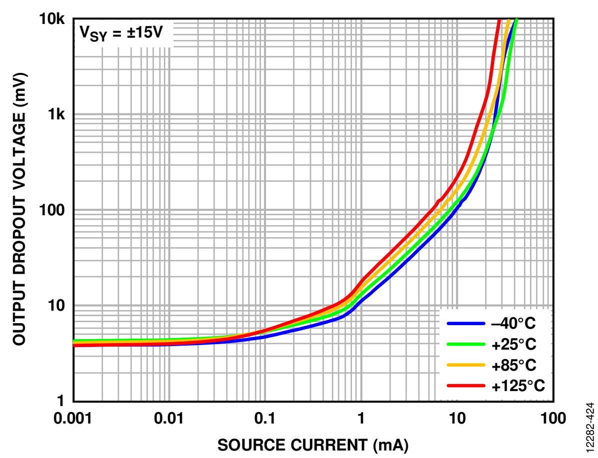

Figure 38. Output Dropout Voltage vs. Source Current, V_{SY} = ±15 V

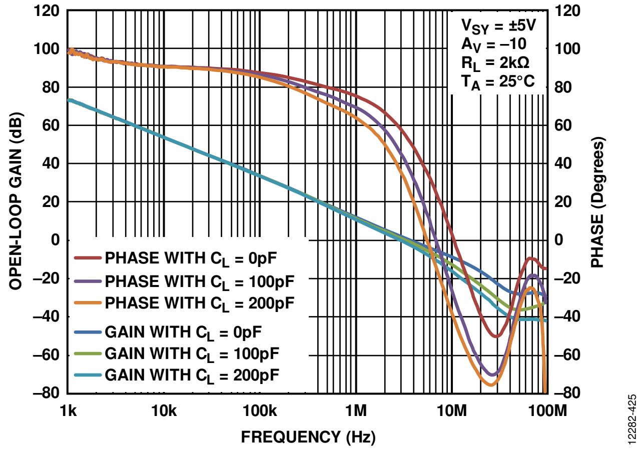

Figure 39. Open-Loop Gain and Phase vs. Frequency, V_{SY} = ±5 V

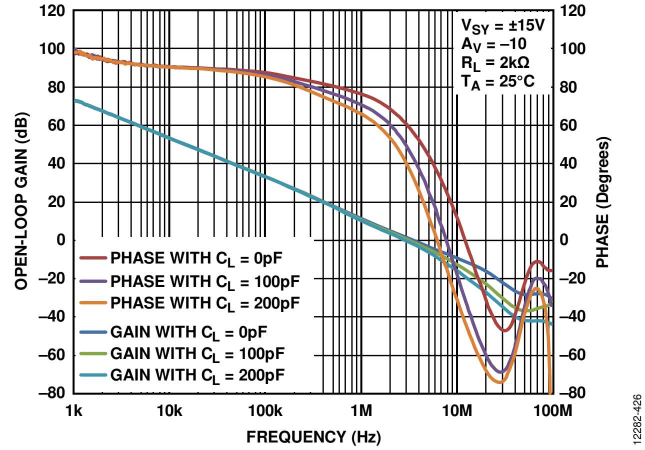

Figure 42. Open-Loop Gain and Phase vs. Frequency, V_{SY} = ±15 V

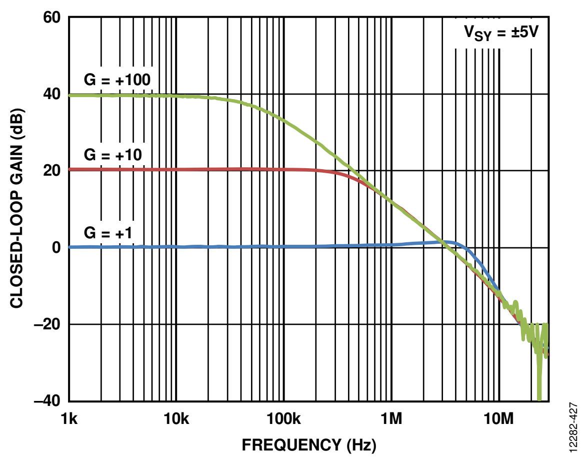

Figure 40. Closed-Loop Gain vs. Frequency, V_{SY} = ±5 V

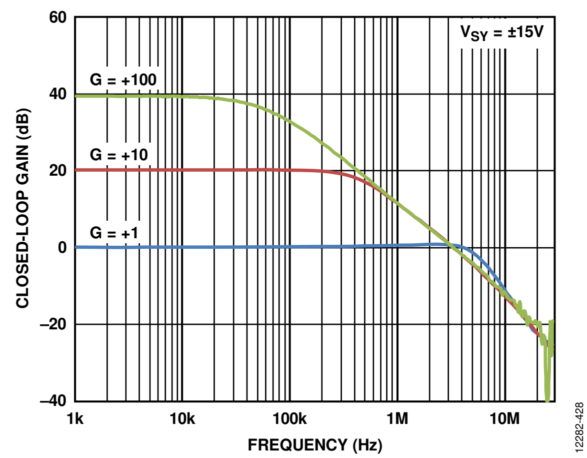

Figure 43. Closed-Loop Gain vs. Frequency, V_{SY} = ±15 V

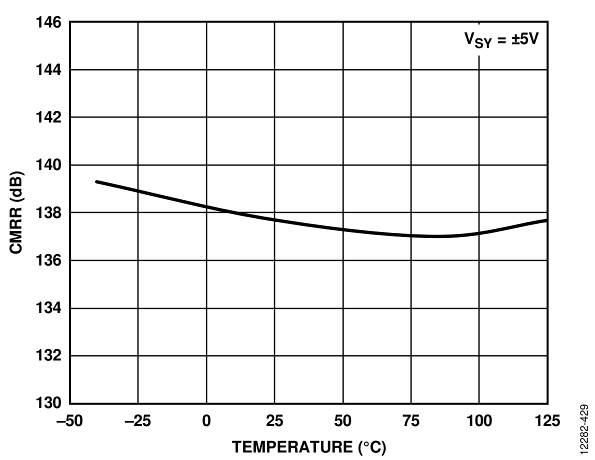

Figure 41. Common-Mode Rejection Ratio (CMRR) vs. Temperature, V_{SY} = ±5 V

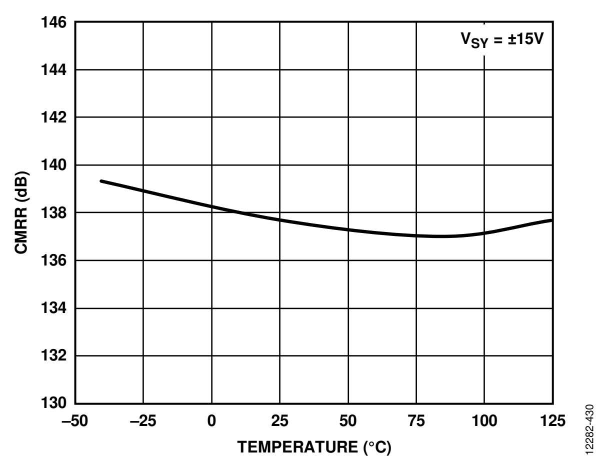

Figure 44. Common-Mode Rejection Ratio (CMRR) vs. Temperature, V_{SY} = ±15 V

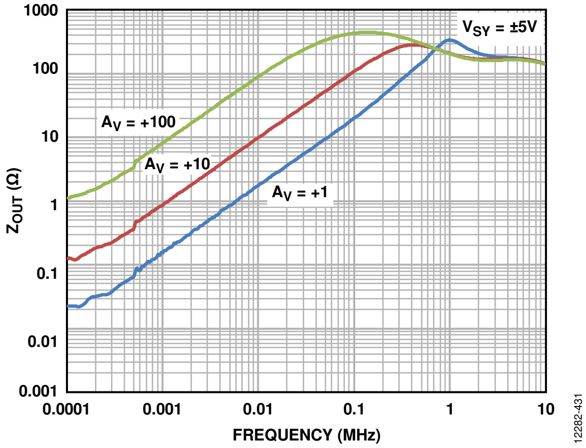

Figure 45. Output Impedance (Z_{OUT}) vs. Frequency, V_{SY} = ±5 V

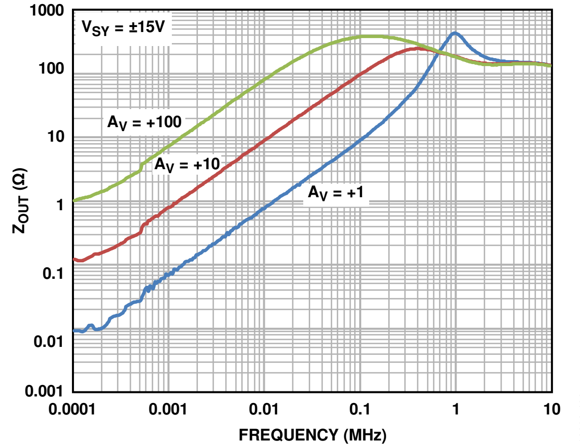

Figure 48. Output Impedance (Z_{OUT}) vs. Frequency, V_{SY} = ±15 V

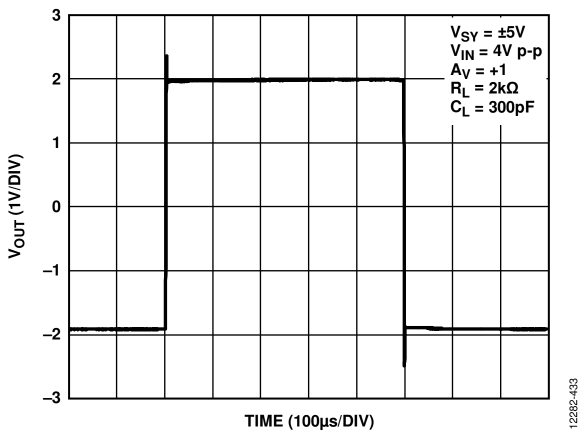

Figure 46. Large Signal Transient Response, V_{SY} = ±5 V

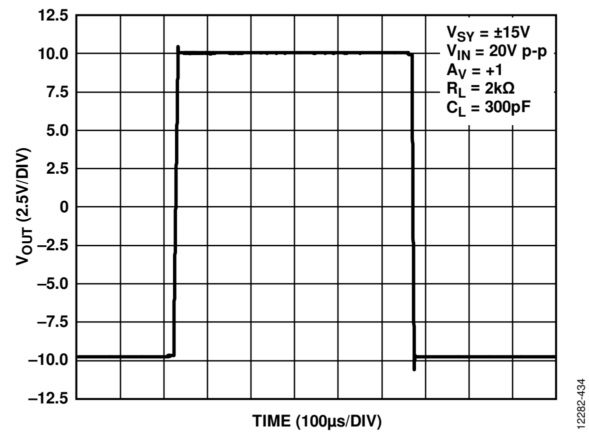

Figure 49. Large Signal Transient Response, V_{SY} = ±15 V

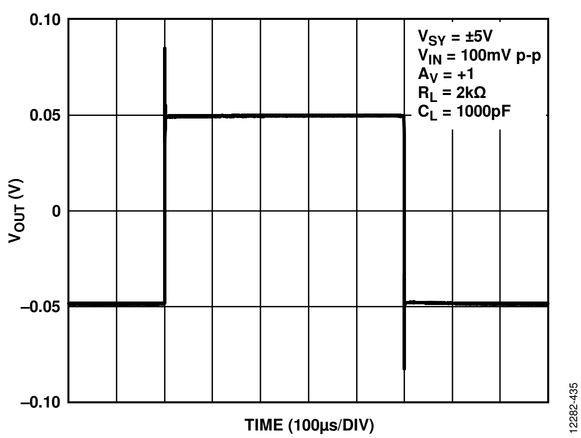

Figure 47. Small Signal Transient Response, V_{SY} = ±5 V

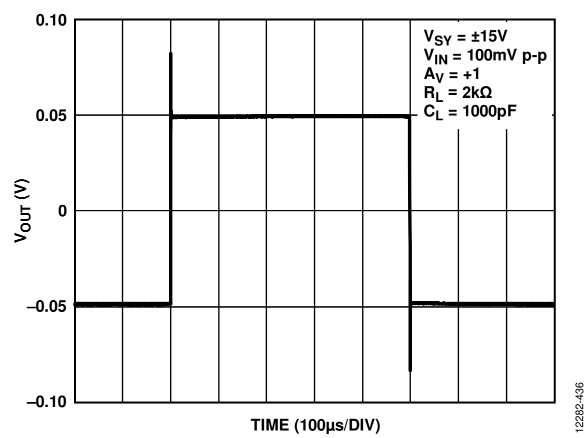

Figure 50. Small Signal Transient Response, V_{SY} = ±15 V

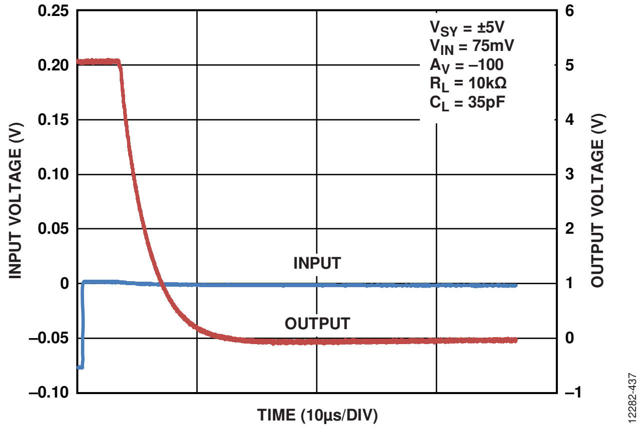

Figure 51. Positive Overload Recovery, V_{SY} = ±5 V

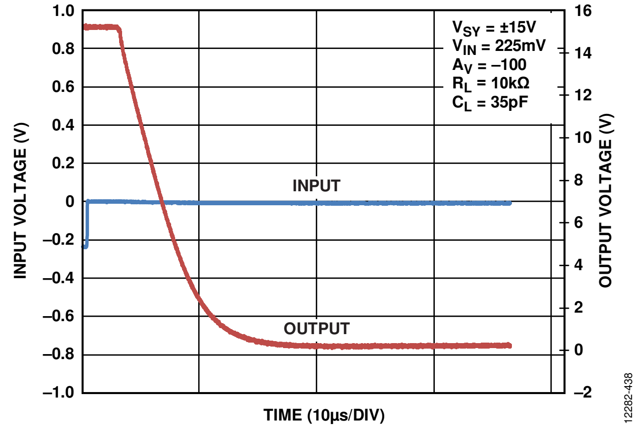

Figure 54. Positive Overload Recovery, V_{SY} = ±15 V

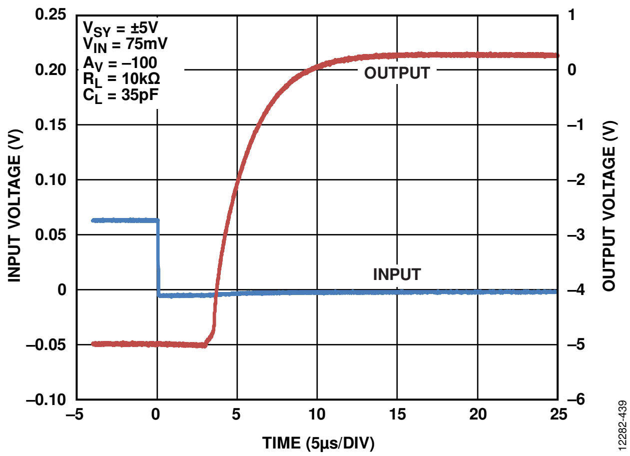

Figure 52. Negative Overload Recovery, V_{SY} = ±5 V

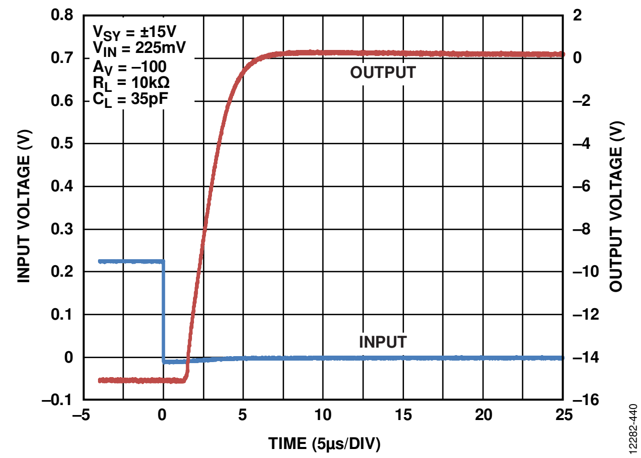

Figure 55. Negative Overload Recovery, V_{SY} = ±15 V

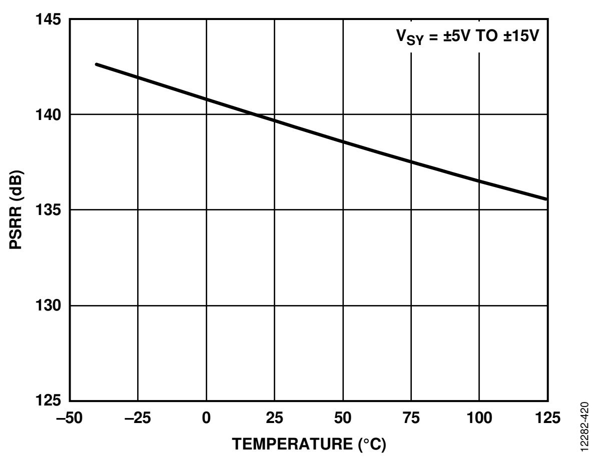

Figure 53. Power Supply Rejection Ratio (PSRR) vs. Temperature, V_{SY} = ±5 V to ±15 V

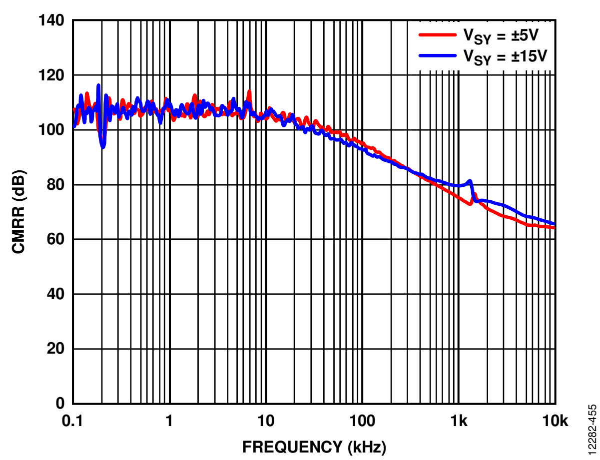

Figure 56. Common-Mode Rejection Ratio (CMRR) vs. Frequency, V_{SY} = ±5 V and V_{SY} = ±15 V

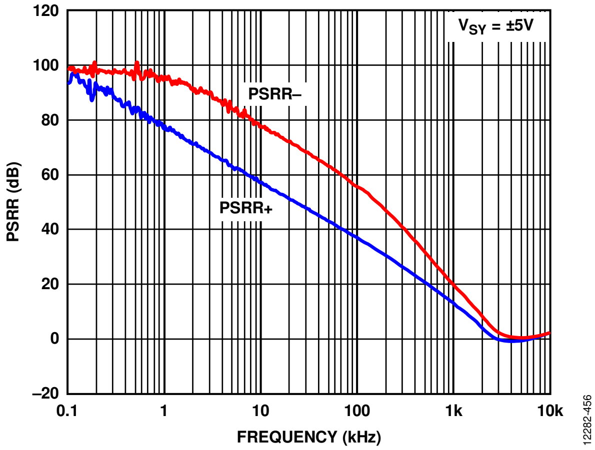

Figure 57. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{SY} = ±5 V

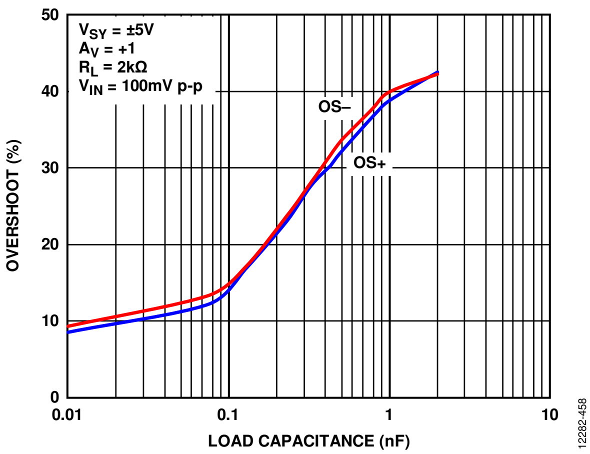

Figure 58. Small Signal Overshoot vs. Load Capacitance, V_{SY} = ±5 V

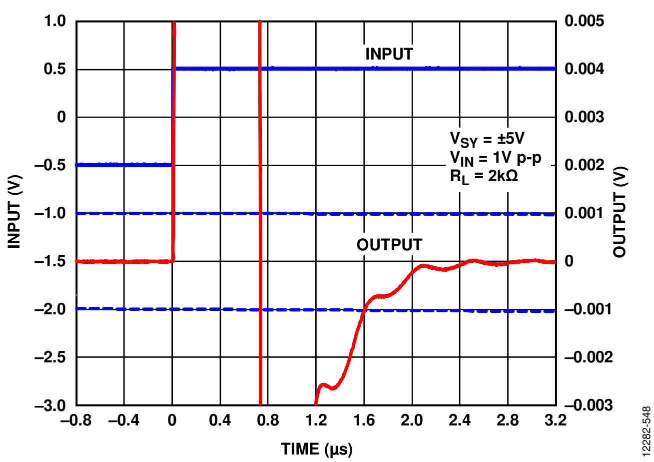

Figure 59. Positive Settling Time to 0.1%, V_{SY} = ±5 V

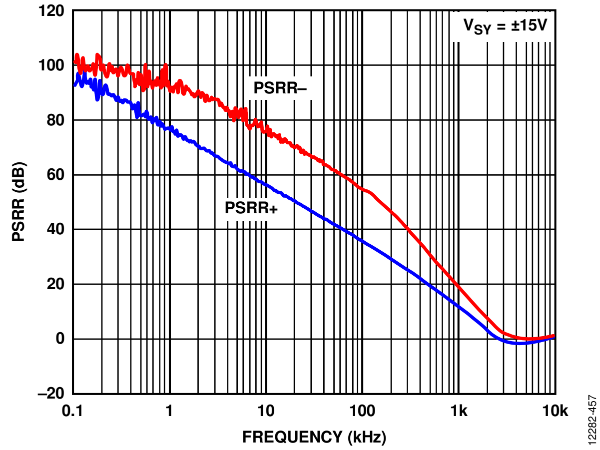

Figure 60. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{SY} = ±15 V

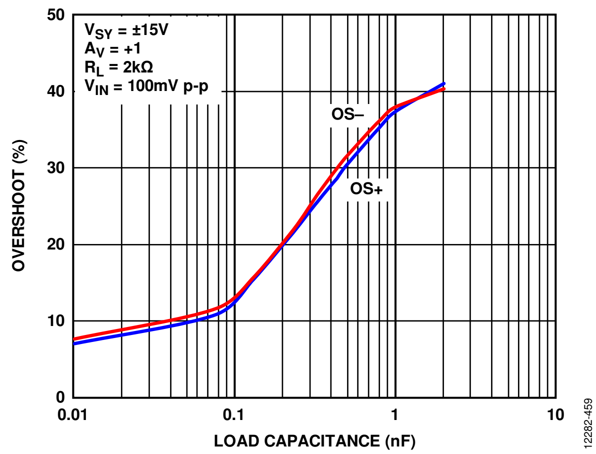

Figure 61. Small Signal Overshoot vs. Load Capacitance, V_{SY} = ±15 V

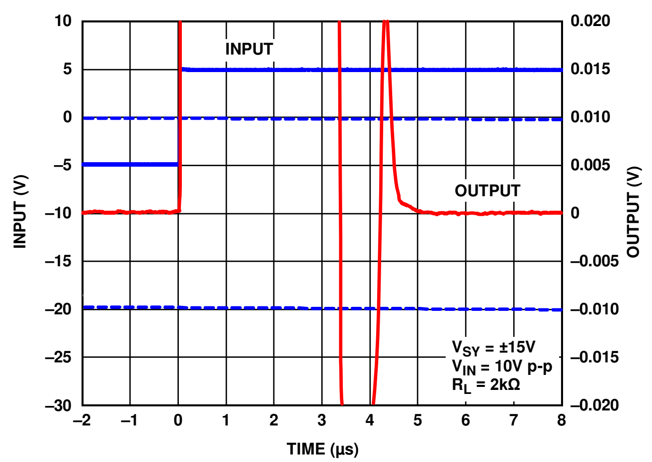

Figure 62. Positive Settling Time to 0.1%, V_{SY} = ±15 V

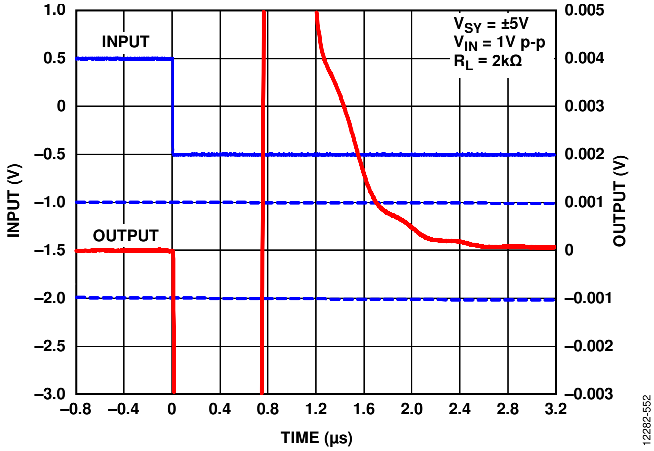

Figure 63. Negative Settling Time to 0.1%, V_{SY} = ±5 V

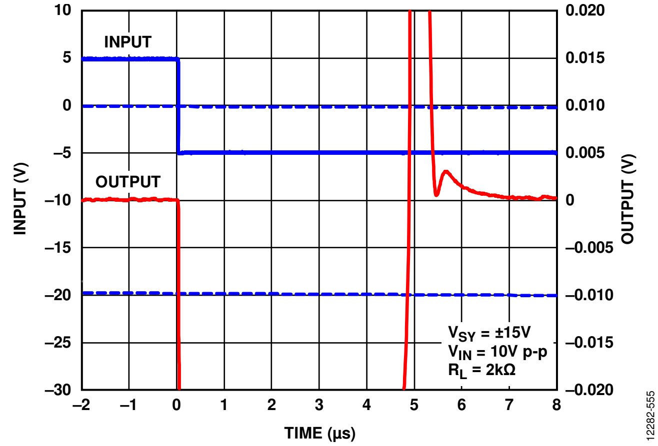

Figure 66. Negative Settling Time 0.1%, V_{SY} = ±15 V

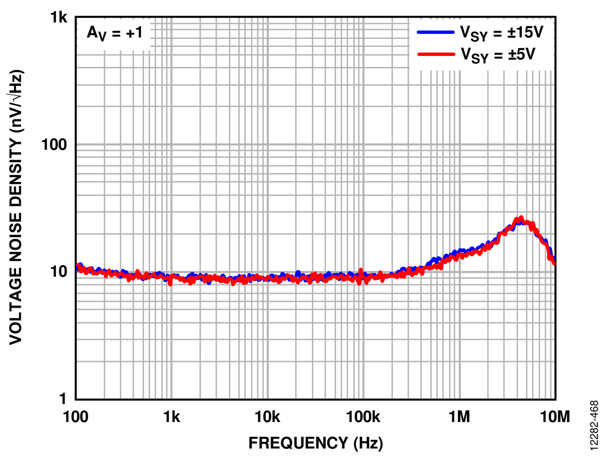

Figure 64. Voltage Noise Density vs. Frequency, V_{SY} = ±5 V and V_{SY} = ±15 V

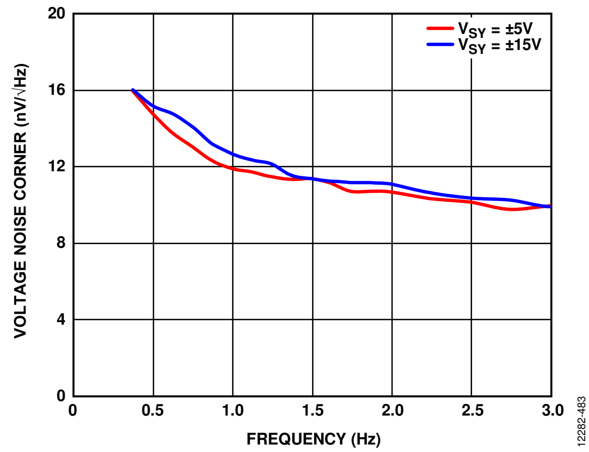

Figure 67. Voltage Noise Corner vs. Frequency, V_{SY} = ±5 V and V_{SY} = ±15 V

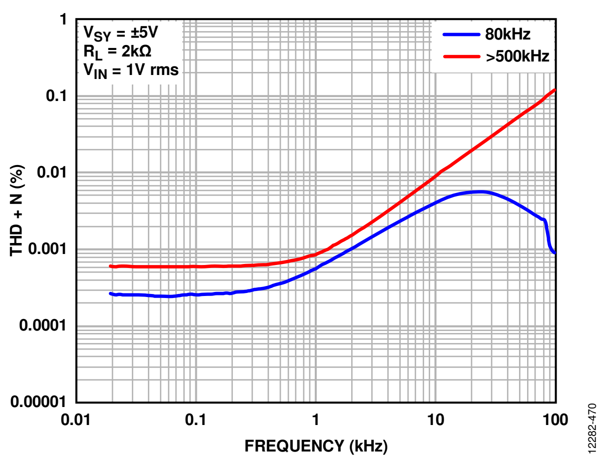

Figure 65. THD + N vs. Frequency, V_{SY} = ±5 V

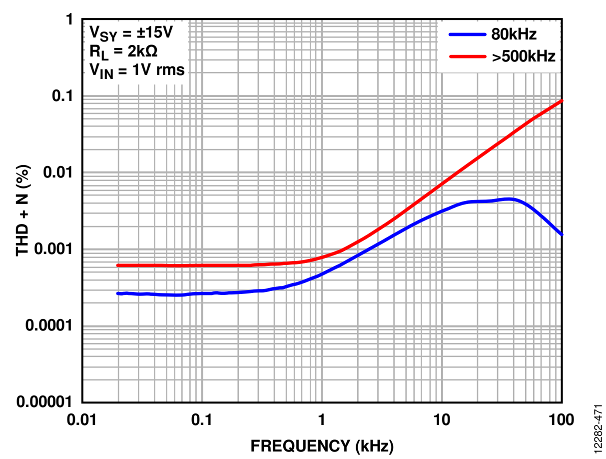

Figure 68. THD + N vs. Frequency, V_{SY} = ±15 V

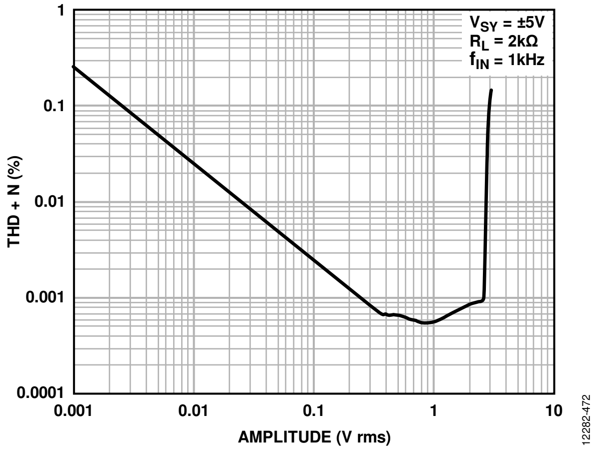

Figure 69. THD + N vs. Amplitude, V_{SY} = ±5 V

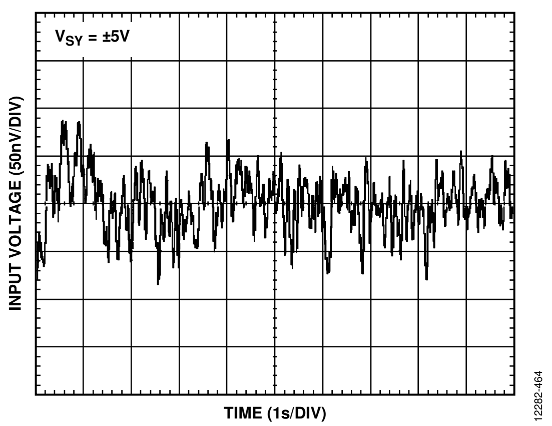

Figure 70. 0.1 Hz to 10 Hz Noise, V_{SY} = ±5 V

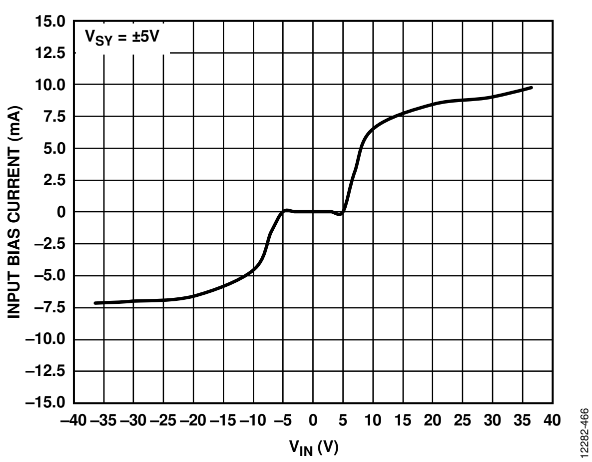

Figure 71. Input Bias Current vs. Input Voltage (V_{IN}) Including Input Overvoltage Range (Beyond V_{SY} = ±5 V)

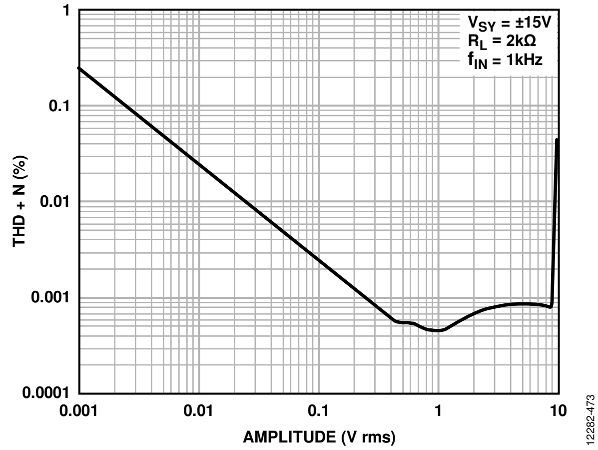

Figure 72. THD + N vs. Amplitude, V_{SY} = ±15 V

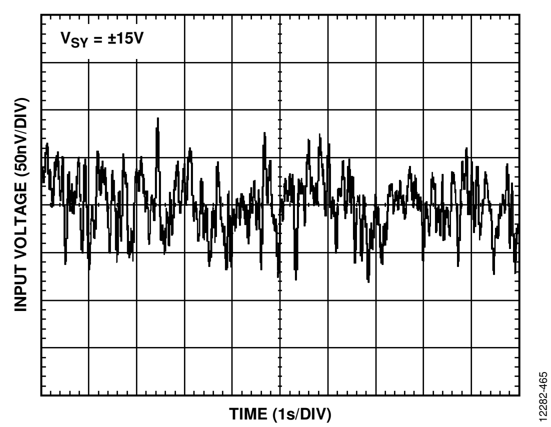

Figure 73. 0.1 Hz to 10 Hz Noise, V_{SY} = ±15 V

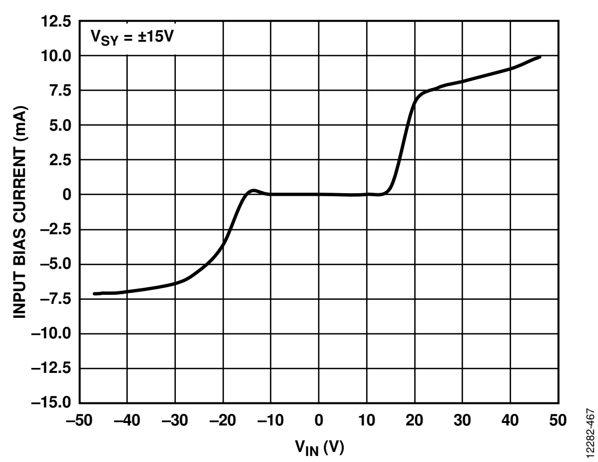

Figure 74. Input Bias Current vs. Input Voltage (V_{IN}) Including Input Overvoltage Range (Beyond V_{SY} = ±15 V)

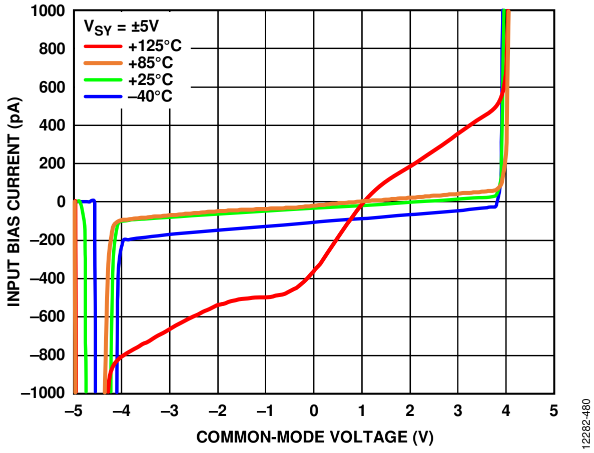

Figure 75. Input Bias Current vs. Common-Mode Voltage (V_{CM}) and Temperature, V_{SY} = ±5 V

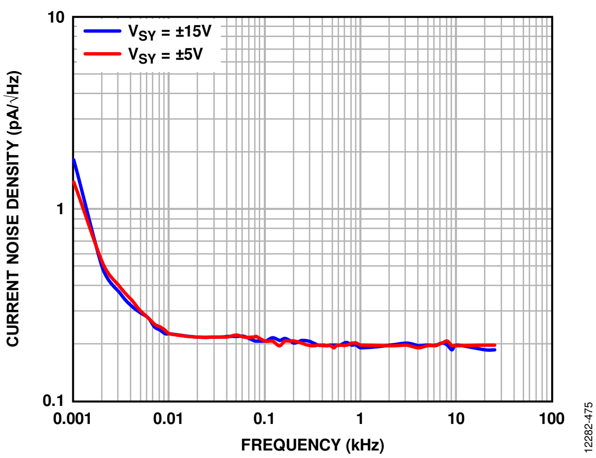

Figure 76. Current Noise Density vs. Frequency, V_{SY} = ±5 V and V_{SY} = ±15 V

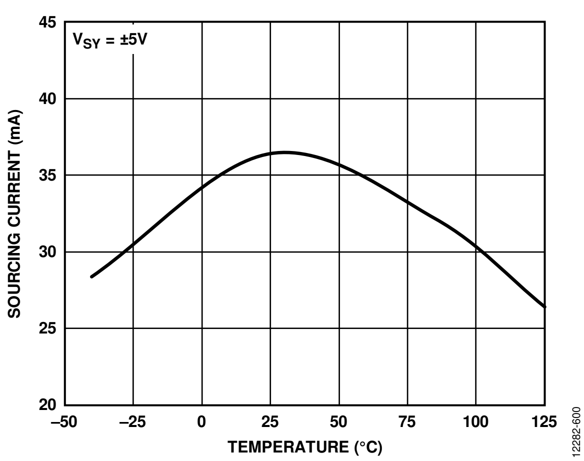

Figure 77. Output Short-Circuit Sourcing Current vs. Temperature, V_{SY} = ±5 V

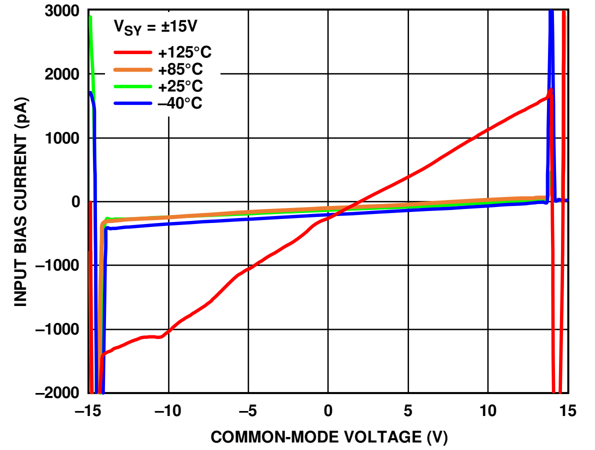

Figure 78. Input Bias Current vs. Common-Mode Voltage (V_{CM}) and Temperature, V_{SY} = ±15 V

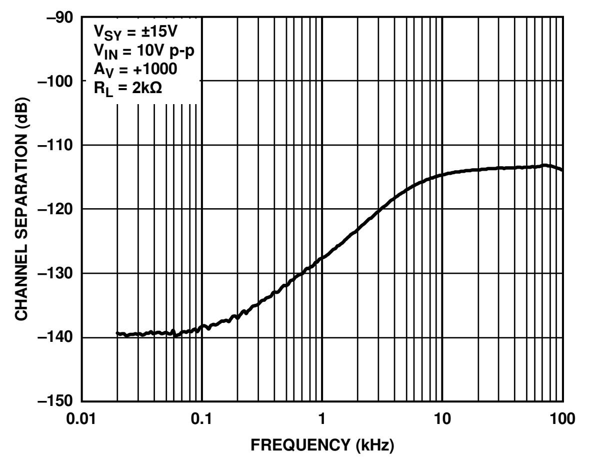

Figure 79. Channel Separation vs. Frequency, V_{SY} = ±15 V

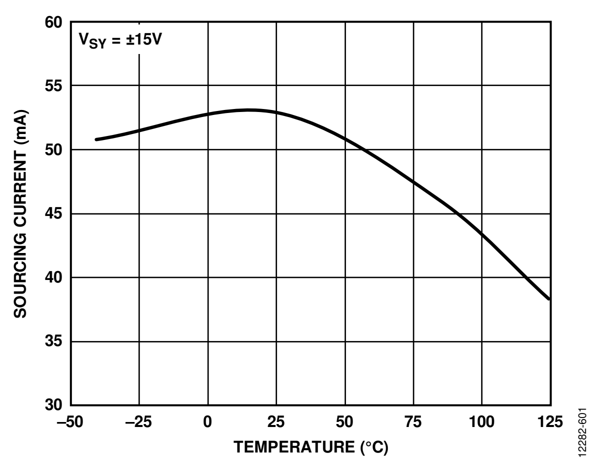

Figure 80. Output Short-Circuit Sourcing Current vs. Temperature, V_{SY} = ±15 V

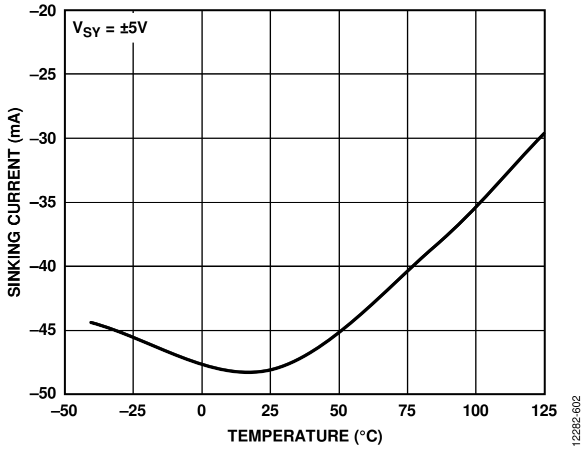

Figure 81. Output Short-Circuit Sinking Current vs. Temperature, V_{SY} = ±5 V

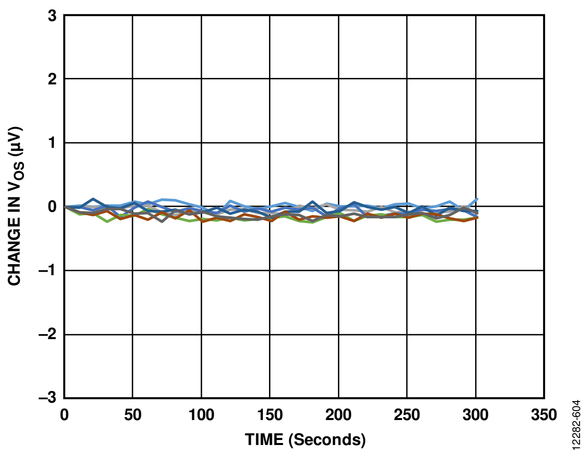

Figure 82. Offset Voltage Short-Term Drift

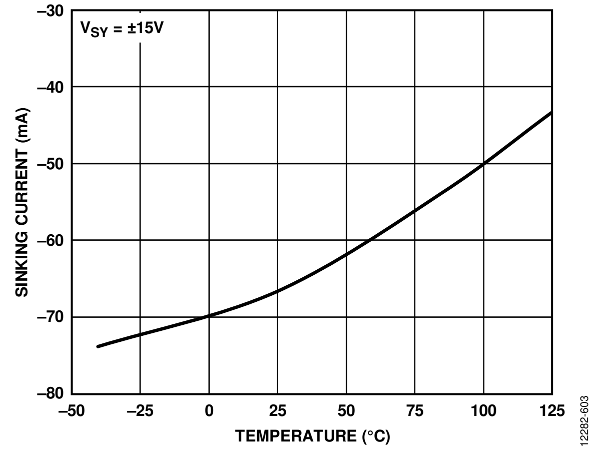

Figure 83. Output Short-Circuit Sinking Current vs. Temperature, V_{SY} = ±15 V

THEORY OF OPERATION

The ADA4177-1, ADA4177-2, and ADA4177-4 are precision, bipolar op amps that integrate both input overvoltage protection (OVP) and input EMI filtering while maintaining a low 2 nA maximum bias current and a rail-to-rail output operation. Figure 84 shows a conceptual schematic of the main amplifier that uses super beta, bipolar input transistors and bias current cancellation to minimize the input bias current. The inputs are cascoded to protect the super beta input devices from damage during overvoltage conditions. The cascoded inputs feed into an active load that makes up the primary gain stage. A buffered transconductance (g_m) stage converts a differential voltage to a differential current to drive the output stage. The rail-to-rail output can swing to 50 mV maximum (for example, the guaranteed room temperature limit for V_{OH} is 14.95 V when the positive supply is 15 V) with a 1 mA load at 25°C.

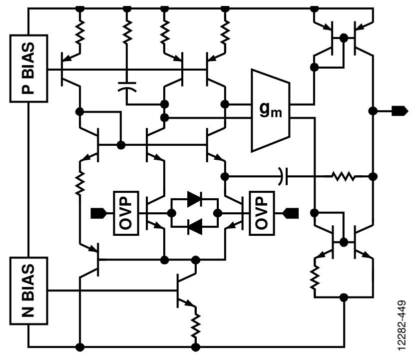

Figure 84. Conceptual Schematic

APPLICATIONS INFORMATION

ACTIVE OVERVOLTAGE PROTECTION

The ADA4177-1/ADA4177-2/ADA4177-4 use active overvoltage protection to protect the device from damage when the inputs are driven to a voltage up to 32 V above the positive supply voltage or 32 V below the negative supply voltage. The ADA4177-1/ADA4177-2/ADA4177-4 not only protect the input from damage, but they also reduce the input noise.

Common Protection Methods

Add an External Series Input Resistor

When an op amp does not have input overvoltage protection, moving the input voltage above or below the supply voltage can cause excessive input current, which can damage the op amp. To avoid this, add a series resistor at the input. To protect the op amp from a 30 V transient beyond either rail, limit the input current to 5 mA, and add a 6 kΩ series resistor to the input. However, a trade-off of adding the series resister is that it adds thermal noise. The 6 kΩ series resistor exhibits 10 nV/√Hz of thermal noise, which adds quadrature thermal noise from the resistor with the op amp noise.

$$N_{TOTAL} = \sqrt{N_{OP\ AMP}{}^2 + N_{RESISTOR}{}^2}$$

where:
$N_{OP\ AMP}$ is the op amp noise.
$N_{RESISTOR}$ is the thermal noise generated by the resistor.

When the additional thermal noise from the series resistor is added to the thermal noise (8 nV/√Hz) of the ADA4177-1/ADA4177-2/ADA4177-4, the 6 kΩ series resistor brings the total thermal noise to 12 nV/√Hz, which is a 70% increase in thermal noise. Figure 85 shows how noise from the additional source resistance adds to the total noise at the amplifier input; the higher the source resistance, the higher the total noise. Because the ADA4177-1/ADA4177-2/ADA4177-4 have integrated input protection for overvoltage conditions, the noise trade-off is avoided.

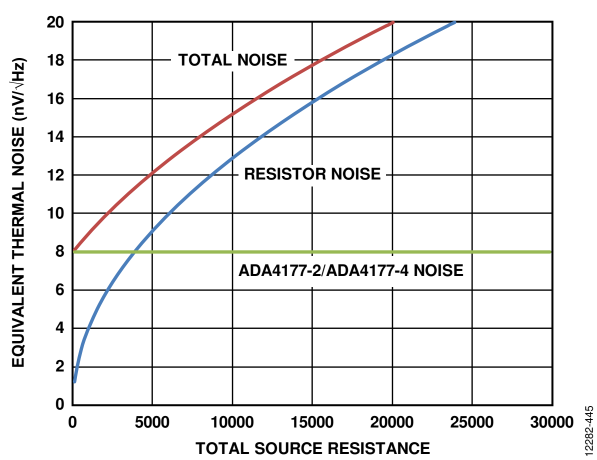

Figure 85. Equivalent Thermal Noise vs. Total Source Resistance

Add External Clamping Diodes

Precision op amps have a low offset voltage (V_{OS}) and a high common-mode rejection ratio (CMRR). Both of these characteristics simplify system calibration and minimize dynamic error. To maintain these specifications in the presence of electrostatic discharge (ESD) events, bipolar op amps often have internal clamp diodes and small limiting resistors in series with their inputs; however, these do not address fault conditions where the inputs exceed the rails. In these cases, the system designer commonly adds clamping diodes (D1 and D2) along with a series resistor (R_{OVP}), as shown in Figure 86.

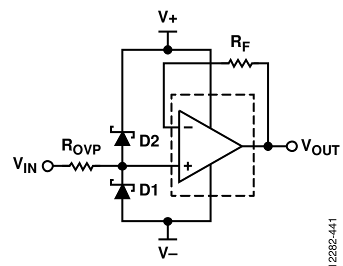

Figure 86. Common Scheme for Protecting Precision Amplifier Inputs from Overvoltage Conditions

If the signal source at V_{IN} is driven to one diode voltage beyond the op amp supplies, the fault current is limited by R_{OVP}. Schottky diodes have a low forward knee voltage of 200 mV less than a typical small signal diode. Therefore, all overvoltage currents are shunted through the external diodes (D1 and D2). The reverse leakage current for a typical Schottky diode is extremely variable with the reverse voltage level. Therefore, as the noninverting input of the op amp swings, the D1 and D2 leakage currents do not match, and the differences pass through R_{OVP}, creating a voltage drop. The voltage drop on R_{OVP} appears as a variation in V_{OS}, which can drastically reduce the CMRR performance. Because the ADA4177-1/ADA4177-2/ADA4177-4 have integrated input protection during overvoltage conditions, the degradation in performance is avoided.

Input Protection Circuit

The ADA4177-1/ADA4177-2/ADA4177-4 inputs provide overvoltage protection without the trade-offs encountered in the common design methods. The conceptual schematic of the input is shown in Figure 87.

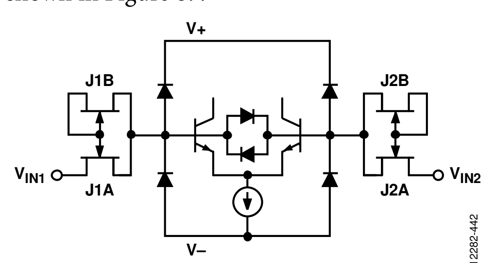

Figure 87. Conceptual Schematic of the Inputs of the ADA4177-1/ADA4177-2/ADA4177-4