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FET Input Analog Front End with ADC Driver

Data Sheet

ADA4350

FEATURES

- Low noise, low input bias current FET input amplifier
  - Very low input bias current: ±0.25 pA typical at 25°C
  - Low input voltage noise
    - 92 nV/√Hz typical at 10 Hz at 5 V
    - 5 nV/√Hz typical at 100 kHz at ±5 V
  - Gain bandwidth product: 175 MHz
  - Input capacitance
    - 3 pF typical, differential mode
    - 2 pF typical, common mode
- Integrated gain switching
  - Sampling and feedback switch off leakage: ±0.5 pA typical
  - Worst case t_{ON}/t_{OFF} times: 105 ns typical/65 ns typical
- Integrated analog-to-digital converter (ADC) driver
  - Differential mode and single-ended mode
  - Adjustable output common-mode voltage
    - −5 V to +3.8 V typical for ±5 V supply
  - Wide output voltage swing: ±4.8 V minimum for ±5 V supply
  - Linear output current: 18 mA rms typical for ±5 V supply
- SPI or parallel switch control of all functions
- Wide operating range: 3.3 V to 12 V
- Quiescent current: 8.5 mA typical (±5 V full system)

APPLICATIONS

- Current to voltage (I to V) conversions
- Photodiode preamplifiers
- Chemical analyzers
- Mass spectrometry
- Molecular spectroscopy
- Laser/LED receivers
- Data acquisition systems

GENERAL DESCRIPTION

The ADA4350 is an analog front end for photodetectors or other sensors whose output produces a current proportional to the sensed parameter or voltage input applications where the system requires the user to select between very precise gain levels to maximize the dynamic range.

The ADA4350 integrates a FET input amplifier, a switching network, and an ADC driver with all functions controllable via a serial peripheral interface (SPI) or parallel control logic into a single IC. The FET input amplifier has very low voltage noise and current noise making it an excellent choice to work with a wide range of photodetectors, sensors, or precision data acquisition systems.

Its switching network allows the user individual selection of up to six different, externally configurable feedback networks; by using external components for the feedback network, the user can more easily match the system to their desired photodetector or sensor capacitance. This feature also allows the use of low thermal drift resistors, if required.

The design of the switches minimizes error sources so that they add virtually no error in the signal path. The output driver can be used in either single-ended or a differential mode and is ideal for driving the input of an ADC.

The ADA4350 can operate from a single +3.3 V supply or a dual ±5 V supply, offering user flexibility when choosing the polarity of the detector. It is available in a Pb-free, 28-lead TSSOP package and is specified to operate over the −40°C to +85°C temperature range.

Multifunction pin names may be referenced by their relevant function only.

FUNCTIONAL BLOCK DIAGRAM

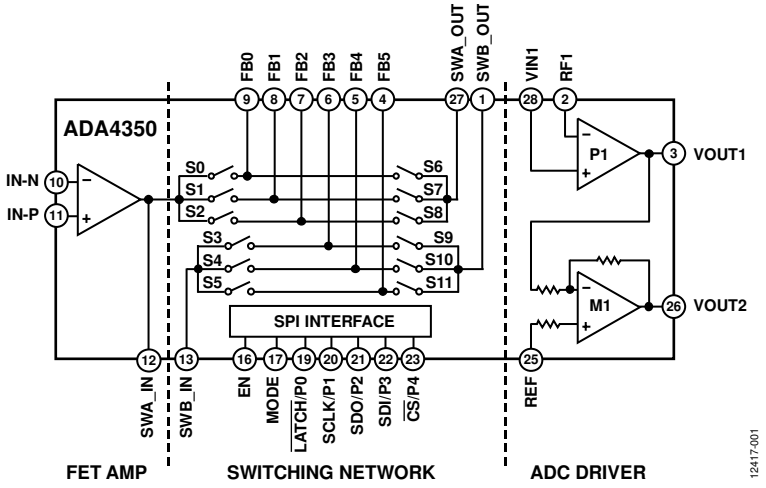

Figure 1.

Rev. B

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
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COMPARABLE PARTS

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EVALUATION KITS

- ADA4350 Evaluation Board

DOCUMENTATION

Data Sheet

- ADA4350: FET Input Analog Front End With ADC Driver Data Sheet

User Guides

- UG-655: Evaluating the ADA4350, a FET Input Analog Front End With ADC Driver Offered in a 28-Lead 9.8 mm × 6.4 mm TSSOP

TOOLS AND SIMULATIONS

- ADA4350 SPICE Macro-Model

REFERENCE MATERIALS

Press

- Integrated Analog Front-end Simplifies Sensor Interfaces

DESIGN RESOURCES

- ADA4350 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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4/15—Revision 0: Initial Version

SPECIFICATIONS

±5 V FULL SYSTEM

T_A = 25°C, $+V_S$ = +5 V, $-V_S$ = −5 V, R_L = 1 kΩ differential, unless otherwise specified.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	Gain (G) = −5, V_{OUT} = 200 mV p-p		20		MHz
	G = −5, V_{OUT} = 2 V p-p		12		MHz
Slew Rate	V_{OUT} = 2 V step, 10% to 90%		60		V/µs
HARMONIC PERFORMANCE					
Harmonic Distortion (HD2/HD3)	G = −5, f_C = 100 kHz		−95/−104		dBc
	G = −5, f_C = 1 MHz		−77/−78		dBc
DC PERFORMANCE					
Input Bias Current	At 25°C		±0.25	±1	pA
	At 85°C		±8	±25	pA
INPUT CHARACTERISTICS					
Input Resistance	Common mode		100		GΩ
Input Capacitance	Common mode		2		pF
	Differential mode		3		pF
Input Common-Mode Voltage Range	Common-mode rejection ratio (CMRR) > 80 dB	−4.5		+3.8	V
	CMRR > 68 dB	−5		+3.9	V
Common-Mode Rejection	V_{CM} = ±3.0 V	92	104		dB
OUTPUT CHARACTERISTICS					
Linear Output Current	V_{OUT} = 4 V p-p, 60 dB spurious-free dynamic range (SFDR)		18		mA rms
Short-Circuit Current	Sinking/sourcing		43/76		mA
Settling Time to 0.1%	G = −5, V_{OUT} = 2 V step		100		ns
ANALOG POWER SUPPLY ($+V_S$, $-V_S$)					
Operating Range		3.3		12	V
Quiescent Current	Enabled		8.5	10	mA
	M1 disabled (see Figure 1)		7		mA
	All disabled		2		µA
Positive Power Supply Rejection Ratio			90		dB
Negative Power Supply Rejection Ratio			85		dB
DIGITAL SUPPLIES	DVDD, DGND				
Digital Supply Range		3.3		5.5	V
Quiescent Current	Enabled		50		µA
	Disabled		0.6		µA
$+V_S$ to DGND Head Room			≥3.3		V

±5 V FET INPUT AMPLIFIER

T_A = 25°C, $+V_S$ = +5 V, $-V_S$ = −5 V, R_L = 1 kΩ, unless otherwise specified.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = −5, V_{OUT} = 100 mV p-p		26		MHz
	G = −5, V_{OUT} = 2 V p-p		24		MHz
Gain Bandwidth Product			175		MHz
Slew Rate	V_{OUT} = 2 V step, 10% to 90%		100		V/µs
Settling Time to 0.1%	G = −5, V_{OUT} = 2 V step		28		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion (HD2/HD3)	f = 100 kHz, V_{OUT} = 2 V p-p, G = −5		−106/−114		dBc
	f = 1 MHz, V_{OUT} = 2 V p-p, G = −5		−83/−93		dBc
Input Voltage Noise	f = 10 Hz		85		nV/√Hz
	f = 100 kHz		5		nV/√Hz
DC PERFORMANCE					
Input Offset Voltage			15	80	µV
Input Offset Voltage Drift	From −40°C to +85°C		0.1	1.6	µV/°C
	From 25°C to 85°C		0.1	1.0	µV/°C
Input Bias Current	At 25°C		±0.25	±1	pA
	At 85°C		±8	±25	pA
Input Bias Offset Current	At 25°C		±0.1	±0.8	pA
	At 85°C		±0.5		pA
Open-Loop Gain	V_{OUT} = ±2 V	106	115		dB
INPUT CHARACTERISTICS					
Input Resistance	Common mode		100		GΩ
Input Capacitance	Common mode		2		pF
	Differential mode		3		pF
Input Common-Mode Voltage Range	CMRR > 80 dB	−4.5		+3.8	V
	CMRR > 68 dB	−5		+3.9	V
Common-Mode Rejection Ratio	V_{CM} = ±3 V	92	115		V
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	V_{OUT} = V_S ± 10%		60		ns
Output Voltage Swing	G = +21, R_F = 1 kΩ, R_L open measured at FBx	−3.6 to +3.9	−4.05 to +4.07		V
	G = +21, R_F = 100 kΩ, R_L open measured at FBx	−4.7 to +4.8	−4.9 to +4.86		V
Linear Output Current	V_{OUT} = 2 V p-p, 60 dB SFDR		18		mA rms
Short-Circuit Current	Sinking/sourcing		41/45		mA
POWER SUPPLY					
Operating Range		3.3		12	V
Positive Power Supply Rejection Ratio		90	109		dB
Negative Power Supply Rejection Ratio		90	109		dB

±5 V INTERNAL SWITCHING NETWORK AND DIGITAL PINS

T_A = 25°C, $+V_S$ = +5 V, $-V_S$ = −5 V, unless otherwise specified. See Figure 1 for feedback and sampling switches notation.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FEEDBACK/SAMPLE ANALOG SWITCH						
Analog Signal Range			−5		+5	V
Switch On-Resistance						
Feedback	$R_{ON, FB}$	For S0 to S2, V_{CM} = 0 V		149	196	Ω
		T_A = 85°C		195		Ω
		For S3 to S5, V_{CM} = 0 V		149	196	Ω
		T_A = 85°C		195		Ω
Sampling	$R_{ON, S}$	For S6 to S8, V_{CM} = 0 V		297	356	Ω
		T_A = 85°C		390		Ω
		For S9 to S11, V_{CM} = 0 V		297	356	Ω
		T_A = 85°C		388		Ω
On-Resistance Match Between Channels						
Feedback Resistance	$\Delta R_{ON, FB}$	V_{CM} = 0 V		2	15	Ω
Sampling Resistance	$\Delta R_{ON, S}$	V_{CM} = 0 V		2	14	Ω
SWITCH LEAKAGE CURRENTS						
Sampling and Feedback Switch Off Leakage	$I_{S (OFF)}$			±0.5	±1.7	pA
		T_A = 85°C		±40	±120	pA
DYNAMIC CHARACTERISTICS						
Power-On Time	t_{ON}	DVDD = 5 V		76		ns
		DVDD = 3.3 V		80		ns
Power-Off Time	t_{OFF}	DVDD = 5 V		86		ns
		DVDD = 3.3 V		90		ns
Off Isolation		R_L = 50 Ω, f = 1 MHz				
Feedback Switches				−92		dB
Sampling Switches				−118		dB
Channel to Channel Crosstalk		R_L = 50 Ω, f = 1 MHz		−86		dB
Worst Case Switch Feedback Capacitance (Switch Off)	$C_{FB (OFF)}$			0.1		pF
THRESHOLD VOLTAGES FOR DIGITAL INPUT PINS		EN, MODE, DGND, $\overline{\text{LATCH}}$/P0, SCLK/P1, SDO/P2, SDI/P3, $\overline{\text{CS}}$/P4[1]				
Input High Voltage	V_{IH}	DVDD = 5 V	2.0			V
		DVDD = 3.3 V	1.5			V
Input Low Voltage	V_{IL}	DVDD = 5 V			1.4	V
		DVDD = 3.3 V			1.0	V
DIGITAL SUPPLIES		DVDD, DGND				
Digital Supply Range			3.3		5.5	V
Quiescent Current		Enabled		50		µA
		Disabled		0.6		µA
$+V_S$ to DGND Head Room				≥3.3		V

[1] When referring to a single function of a multifunction pin, only the portion of the pin name that is relevant to the specification is listed. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.

±5 V ADC DRIVER

T_A = 25°C, $+V_S$ = +5 V, $-V_S$ = −5 V, unless otherwise specified. See Figure 1 for the P1 and M1 amplifiers. R_L = 1 kΩ when differential, and R_L = 500 Ω when single-ended.

Table 4.

Parameter	Test Conditions/Comments[1]	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	When used differentially, V_{OUT} = 0.1 V p-p		38		MHz
	When used differentially, V_{OUT} = 2.0 V p-p		16		MHz
	When P1 is used, V_{OUT} = 50 mV p-p		55		MHz
	When P1 is used, V_{OUT} = 1.0 V p-p		17		MHz
	When M1 is used, V_{OUT} = 50 mV p-p		45		MHz
	When M1 is used, V_{OUT} = 1.0 V p-p		21		MHz
Overdrive Recovery Time	Positive recovery/negative recovery for P1		200/180		ns
	Positive recovery/negative recovery for M1		100/100		ns
Slew Rate	When differentially used, V_{OUT} = 2 V step		57		V/µs
	When P1 or M1 is single-ended, V_{OUT} = 1 V step		30		V/µs
Settling Time 0.1%	When used differentially, V_{OUT} = 2 V step		95		ns
	When P1 is used, V_{OUT} = 1 V step		80		ns
	When M1 is used, V_{OUT} = 1 V step		80		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion (HD2/HD3)	When used differentially, f_C = 100 kHz, V_{OUT} = 4 V p-p		−105/−109		dBc
	When used differentially, f_C = 1 MHz, V_{OUT} = 4 V p-p		−75/−73		dBc
	When P1 is used, f_C = 100 kHz, V_{OUT} = 2 V p-p		−112/−108		dBc
	When P1 is used, f_C = 1 MHz, V_{OUT} = 2 V p-p		−75/−73		dBc
	When M1 is used, f_C = 100 kHz, V_{OUT} = 2 V p-p		−98/−103		dBc
	When M1 is used, f_C = 1 MHz, V_{OUT} = 2 V p-p		−70/−69		dBc
Referred to Input (RTI) Voltage Noise	For P1, f = 10 Hz		55		nV/√Hz
	For P1, f = 100 kHz		5		nV/√Hz
Referred to Output (RTO) Voltage Noise	For P1 and M1, f = 10 Hz , measured at VOUT2		95		nV/√Hz
	For P1 and M1, f = 100 kHz, measured at VOUT2		16		nV/√Hz
Input Current Noise	f = 100 kHz, referred to P1		1.1		pA/√Hz
DC PERFORMANCE					
Output Offset Voltage	Differential		0.125	0.5	mV
Output Offset Voltage Drift	Differential		0.7	13	µV/°C
Input Offset Voltage	Single-ended, P1 only		50	180	µV
	Single-ended, M1 only		40	180	µV
Input Offset Voltage Drift	Single-ended, P1 only		0.2	4.75	µV/°C
	Single-ended, M1 only		0.4	3.6	µV/°C
Input Bias Current	P1 only at VIN1 pin		60	220	nA
	P1 only at RF1 pin		60	325	nA
	M1 at REF pin		60	200	nA
Input Offset Current	P1 only		60	260	nA
Open-Loop Gain	P1 only, V_{OUT} = ±2 V	102	112		dB
Gain	M1 only	1.99	1.9996	2.01	V/V
Gain Error		−0.5		+0.5	%
Gain Error Drift			0.6	1.9	ppm/°C
INPUT CHARACTERISTICS					
Input Resistance	VIN1 and REF		200		MΩ
Input Capacitance	VIN1 and REF		1.4		pF
Input Common-Mode Voltage Range		−5		+3.8	V
Common-Mode Rejection Ratio	For P1, V_{CM} = ±3.0 V	82	100		dB

Parameter	Test Conditions/Comments[1]	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = no load, single-ended	±4.8	±4.83		V
	R_L = 500 Ω, single-ended	±4.55	±4.6		V
Output Common-Mode Voltage Range		−5		+3.8	V
Linear Output Current	P1 or M1, V_{OUT} = 2 V p-p, 60 dB SFDR		18		mA rms
	Differential output, V_{OUT} = 4 V p-p, 60 dB SFDR		18		mA rms
Short Circuit Current	P1 or M1, sinking/sourcing		43/76		mA
Capacitive Load Drive	When used differentially at each VOUTx, 30% overshoot, V_{OUT} = 200 mV p-p		33		pF
	When P1/M1 is used, 30% overshoot, V_{OUT} = 100 mV p-p		47		pF
POWER SUPPLY					
Operating Range		3.3		12	V
Positive Power Supply Rejection Ratio	For P1	90	106		dB
	For M1	86	100		dB
Negative Power Supply Rejection Ratio	For P1	80	100		dB
	For M1	78	90		dB

[1] P1 and M1 within this table refer to the amplifiers shown in Figure 1.

5 V FULL SYSTEM

T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = 0 V, R_F = 1 kΩ differential, unless otherwise specified.

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = −5, V_{OUT} = 200 mV p-p		15		MHz
	G = −5, V_{OUT} = 1 V p-p		14		MHz
Slew Rate	V_{OUT} = 2 V step, 10% to 90%		30		V/µs
HARMONIC PERFORMANCE					
Harmonic Distortion (HD2/HD3)	G = −5, f_C = 100 kHz		−85/−94		dBc
	G = −5, f_C = 1 MHz		−66/−75		dBc
Input Voltage Noise	f = 10 Hz		92		nV/√Hz
	f = 100 kHz		4.4		nV/√Hz
DC PERFORMANCE					
Input Bias Current	At 25°C		±0.35	±1.6	pA
	At 85°C		±8.5	±30	pA
INPUT CHARACTERISTICS					
Input Resistance	Common mode		100		GΩ
Input Capacitance	Common mode		2		pF
	Differential mode		3		pF
Input Common-Mode Voltage Range	CMRR > 80 dB	0.5		3.8	V
	CMRR > 68 dB	0		3.9	V
Common-Mode Rejection	V_{CM} = ±0.5 V	88	94		dB
OUTPUT CHARACTERISTICS					
Linear Output Current	V_{OUT} = 1 V p-p, 60 dB SFDR		9		mA rms
Short-Circuit Current	Sinking/sourcing, R_L < 1 Ω		41/63		mA
Settling Time to 0.1%	G = −5, V_{OUT} = 2 V step		130		ns
POWER SUPPLY					
Operating Range		3.3		12	V
Quiescent Current	Enabled		8	9	mA
	M1 disabled (see Figure 1)		6.5		mA
	All disabled		2		µA
Positive Power Supply Rejection Ratio			86		dB
Negative Power Supply Rejection Ratio			80		dB
DIGITAL SUPPLIES (DVDD, DGND)	DVDD, DGND				
Digital Supply Range		3.3		5.5	V
Quiescent Current	Enabled		50		µA
	Disabled		0.6		µA
$+V_S$ to DGND Head Room			≥3.3		V

5 V FET INPUT AMPLIFIER

T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = 0 V, R_L = 1 kΩ, unless otherwise specified.

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = −5, V_{OUT} = 100 mV p-p		25		MHz
	G = −5, V_{OUT} = 1 V p-p		24		MHz
Gain Bandwidth Product			175		MHz
Slew Rate	V_{OUT} = 2 V step, 10% to 90%		56		V/µs
Settling Time to 0.1%	G = −5, V_{OUT} = 2 V step		60		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion (HD2/HD3)	f = 100 kHz, V_{OUT} = 1 V p-p, G = −5		−113/−117		dBc
	f = 1 MHz, V_{OUT} = 1 V p-p, G = −5		−82/−83		dBc
Input Voltage Noise	f = 10 Hz		92		nV/√Hz
	f = 100 kHz		4.4		nV/√Hz
DC PERFORMANCE					
Input Offset Voltage			25	80	µV
Input Offset Voltage Drift	From −40°C to +85°C		0.1	1.5	µV/°C
	From 25°C to 85°C		0.05	1	µV/°C
Input Bias Current	At 25°C		±0.35	±1.6	pA
	At 85°C		±8.5	±30	pA
Input Bias Offset Current	At 25°C		±0.25	±1.25	pA
	At 85°C		±0.4		pA
Open-Loop Gain	V_{OUT} = 1.5 V to 3.5 V	98	102		dB
INPUT CHARACTERISTICS					
Input Resistance	Common mode		100		GΩ
Input Capacitance	Common mode		2		pF
	Differential mode		3		pF
Input Common-Mode Voltage Range	CMRR > 80 dB	0.5		3.8	V
	CMRR > 68 dB	0		3.9	V
Common-Mode Rejection Ratio	V_{CM} = ± 0.5V	88	94		dB
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	V_{OUT} = V_S ± 10%, positive/negative		60/50		ns
Output Voltage Swing	G = +21, R_F = 1 kΩ, R_L open measured at FBx	1.15 to 3.46	0.86 to 3.66		V
	G = +21, R_F = 100 kΩ, R_L open measured at FBx	0.27 to 4.80	0.08 to 4.87		V
Linear Output Current	V_{OUT} = 1 V p-p, 60 dB SFDR		10		mA rms
Short-Circuit Current	Sinking/sourcing		32/38		mA
POWER SUPPLY					
Operating Range		3.3		12	V
Positive Power Supply Rejection Ratio		90	100		dB
Negative Power Supply Rejection Ratio		86	100		dB

5 V INTERNAL SWITCHING NETWORK AND DIGITAL PINS

T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = 0 V, unless otherwise specified. See Figure 1 for sampling and feedback switches position.

Table 7.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FEEDBACK/SAMPLE ANALOG SWITCH						
Analog Signal Range			0		5	V
Switch On Resistance						
Feedback	$R_{ON, FB}$	S0 to S2, V_{CM} = 2.5 V		308	390	Ω
		T_A = 85°C		382		Ω
		S3 to S5, V_{CM} = 2.5 V		308	390	Ω
		T_A = 85°C		384		Ω
Sampling	$R_{ON, S}$	S6 to S8, V_{CM} = 2.5 V		610	770	Ω
		T_A = 85°C		762		Ω
		S9 to S11, V_{CM} = 2.5 V		612	770	Ω
		T_A = 85°C		764		Ω
On-Resistance Match Between Channels						
Feedback Resistance	$\Delta R_{ON, FB}$	V_{CM} = 2.5 V		3	21	Ω
Sampling Resistance	$\Delta R_{ON, S}$	V_{CM} = 2.5 V		3	23	Ω
SWITCH LEAKAGE CURRENTS						
Sampling and Feedback Switch Off Leakage	$I_{S (OFF)}$			±0.4	±1.2	pA
		T_A = 85°C		±30	±80	pA
DYNAMIC CHARACTERISTICS						
Power-On Time	t_{ON}	DVDD = 3.3 V		105		ns
Power-Off Time	t_{OFF}	DVDD = 3.3 V		65		ns
Off Isolation		R_L = 50 Ω, f = 1 MHz				
Feedback Switches				−93		dB
Sampling Switches				−116		dB
Channel to Channel Crosstalk		R_L = 50 Ω, f = 1 MHz		−83		dB
Worst Case Switch Feedback Capacitance (Switch Off)	$C_{FB (OFF)}$			0.1		pF
THRESHOLD VOLTAGES FOR DIGITAL INPUT PINS		EN, MODE, DGND, $\overline{\text{LATCH}}$/P0, SCLK/P1, SDO/P2, SDI/P3, $\overline{\text{CS}}$/P4[1]				
Input High Voltage	V_{IH}	DVDD = 5 V	2.0			V
		DVDD = 3.3 V	1.5			V
Input Low Voltage	V_{IL}	DVDD = 5 V			1.4	V
		DVDD = 3.3 V			1.0	V
DIGITAL SUPPLIES		DVDD, DGND				
Digital Supply Range			3.3		5.5	V
Quiescent Current		Enabled		50		µA
		Disabled		0.6		µA
$+V_S$ to DGND Head Room				≥3.3		V

[1] When referring to a single function of a multifunction pin, only the portion of the pin name that is relevant to the specification is listed. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.

5 V ADC DRIVER

T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = 0 V, unless otherwise specified. See Figure 1 for the P1 and M1 amplifiers, R_L = 1 kΩ when differential, and R_L = 500 Ω when single-ended.

Table 8.

Parameter	Test Conditions/Comments[1]	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	When used differentially, V_{OUT} = 0.1 V p-p		33		MHz
	When used differentially, V_{OUT} = 2.0 V p-p		16		MHz
	When P1 is used, V_{OUT} = 50 mV p-p		47		MHz
	When P1 is used, V_{OUT} = 1.0 V p-p		16		MHz
	When M1 is used, V_{OUT} = 50 mV p-p		37		MHz
	When M1 is used, V_{OUT} = 1.0 V p-p		18		MHz
Overdrive Recovery Time	For P1, positive recovery/negative recovery		200/200		ns
	For M1, positive recovery/negative recovery		140/120		ns
Slew Rate	When differentially used, V_{OUT} = 2 V step		37		V/µs
	When P1 or M1 is single-ended, V_{OUT} = 1 V step		20		V/µs
Settling Time 0.1%	When used differentially, V_{OUT} = 2 V step		75		ns
	When P1 is used, V_{OUT} = 1 V step		60		ns
	When M1 is used, V_{OUT} = 1 V step		60		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion (HD2/HD3)	When used differentially, f_C = 100 kHz, V_{OUT} = 1 V p-p		−117/−116		dBc
	When used differentially, f_C = 1 MHz, V_{OUT} = 1 V p-p		−80/−85		dBc
	When P1 is used, f_C = 100 kHz, V_{OUT} = 500 mV p-p		−108/−115		dBc
	When P1 is used, f_C = 1 MHz, V_{OUT} = 500 mV p-p		−80/−83		dBc
	When M1 is used, f_C = 100 kHz, V_{OUT} = 500 mV p-p		−103/−107		dBc
	When M1 is used, f_C = 1 MHz, V_{OUT} = 500 mV p-p		−75/−78		dBc
Referred to Input (RTI) Voltage Noise	For P1, f = 10 Hz		60		nV/√Hz
	For P1, f = 100 kHz		5.2		nV/√Hz
Referred to Output (RTO) Voltage Noise	For P1and M1, f = 10 Hz, measured at VOUT2		140		nV/√Hz
	For P1 and M1, f = 100 kHz, measured at VOUT2		18		nV/√Hz
Input Current Noise	f = 100 kHz, referred to P1		1.1		pA/√Hz
DC PERFORMANCE					
Output Offset Voltage	Differential		0.15	0.75	mV
Input Offset Voltage Drift	Differential		0.6	16	µV/°C
Output Offset Voltage	Single-ended, P1 only		60	275	µV
	Single-ended, M1 only		70	250	µV
Input Offset Voltage Drift	Single-ended, P1 only		0.1	5.9	µV/°C
	Single-ended, M1 only		0.3	4.5	µV/°C
Input Bias Current	P1 only at VIN1 pin		60	230	nA
	P1 only at RF1 pin		60	350	nA
	M1 only at REF pin		60	200	nA
Input Offset Current	P1 only		60	270	nA
Open-Loop Gain	P1 only, V_{OUT} = 1.5 V to 3.5 V	94	100		dB
Gain	M1 only	1.99	1.9995	2.01	V/V
Gain Error		−0.5		+0.5	%
Gain Error Drift			0.6	3.4	ppm/°C

Parameter	Test Conditions/Comments[1]	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Resistance	VIN1 and REF		200		MΩ
Input Capacitance	VIN1 and REF		1.4		pF
Input Common-Mode Voltage Range		0		3.9	V
Common-Mode Rejection Ratio	For P1, V_{CM} = ±0.5 V	84	94		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = no load, single-ended	0.15 to 4.85	0.125 to 4.875		V
	R_L = 500 Ω, single-ended	0.28 to 4.72	0.24 to 4.76		V
Output Common-Mode Voltage Range		0		3.9	V
Linear Output Current	For P1or M1, V_{OUT} = 1 V p-p, 60 dB SFDR		4		mA rms
	Differential output, V_{OUT} = 1 V p-p, 60 dB SFDR		10		mA rms
Short-Circuit Current	For P1 or M1, sinking/sourcing		41/63		mA
Capacitive Load Drive	When used differentially at each VOUTx, 30% overshoot, V_{OUT} = 100 mV p-p		33		pF
	When P1/M1 is used, 30% overshoot, V_{OUT} = 50 mV p-p		47		pF
POWER SUPPLY					
Operating Range		3.3		12	V
Positive Power Supply Rejection Ratio	For P1	86	104		dB
	For M1	80	94		dB
Negative Power Supply Rejection Ratio	For P1	80	92		dB
	For M1	76	88		dB

[1] P1 and M1 within this table refer to the amplifiers shown in Figure 1.

TIMING SPECIFICATIONS

All input signals are specified with $t_R = t_F = 2$ ns (10% to 90% of DVDD) and timed from a voltage threshold level of $V_{TH} = 1.3$ V at DVDD = 3.3 V or $V_{TH} = 1.7$ V at DVDD = 5 V. Guaranteed by characterization; not production tested. See Figure 2 and Figure 3.

Table 9.

		DVDD = 3.3 V		DVDD = 5 V		
Parameter	**Description[1]**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_1	SCLK period.	20		20		ns
t_2	SCLK positive pulse width.	10		10		ns
t_3	SCLK negative pulse width.	10		10		ns
t_4	$\overline{CS}$ setup time. The time required to begin sampling data after $\overline{CS}$ goes low.	1		1		ns
t_5	$\overline{CS}$ hold time. The amount of time required for $\overline{CS}$ to be held low after the last data bit is sampled before bringing $\overline{CS}$ high. Data is latched on the $\overline{CS}$ rising edge. If $\overline{LATCH}$ is held low, data is also applied on the $\overline{CS}$ rising edge.	7		5		ns
t_6	$\overline{CS}$ positive pulse width. The amount of time required between consecutive words.	2		1		ns
t_7	Data setup time. The amount of time the data bit (SDI) must be set before sampling on the falling edge of SCLK.	1		1		ns
t_8	Data hold time. The amount of time SDI must be held after the falling edge of SCLK for valid data to be sampled.	2		2		ns
t_9	Data latched to the internal switches updated. The amount of time it takes from the latched data being applied until the internal switches are updated. $\overline{LATCH}$ disabled referenced from the rising edge of $\overline{CS}$. $\overline{LATCH}$ enabled referenced from the falling edge of $\overline{LATCH}$.		145		140	ns
t_{10}	$\overline{LATCH}$ negative pulse width.	3		3		ns
t_{11}[2]	SCLK rising edge to SDO valid. The amount of time between the SCLK rising edge and the valid SDO transitions (CL_{SDO}[3] = 20 pF).		15		10	ns
t_{12}	$\overline{CS}$ rising edge to the SCLK falling edge. The amount of time required to prevent a 25th SCLK edge from being recognized (only 24 bits allowed for valid word).	1		1		ns

[1] When referring to a single function of a multifunction pin, only the portion of the pin name that is relevant to the specification is listed. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.
[2] This is while in daisy-chain mode and in readback mode.
[3] CL_{SDO} is the capacitive load on the SDO output.

Timing Diagrams for Serial Mode

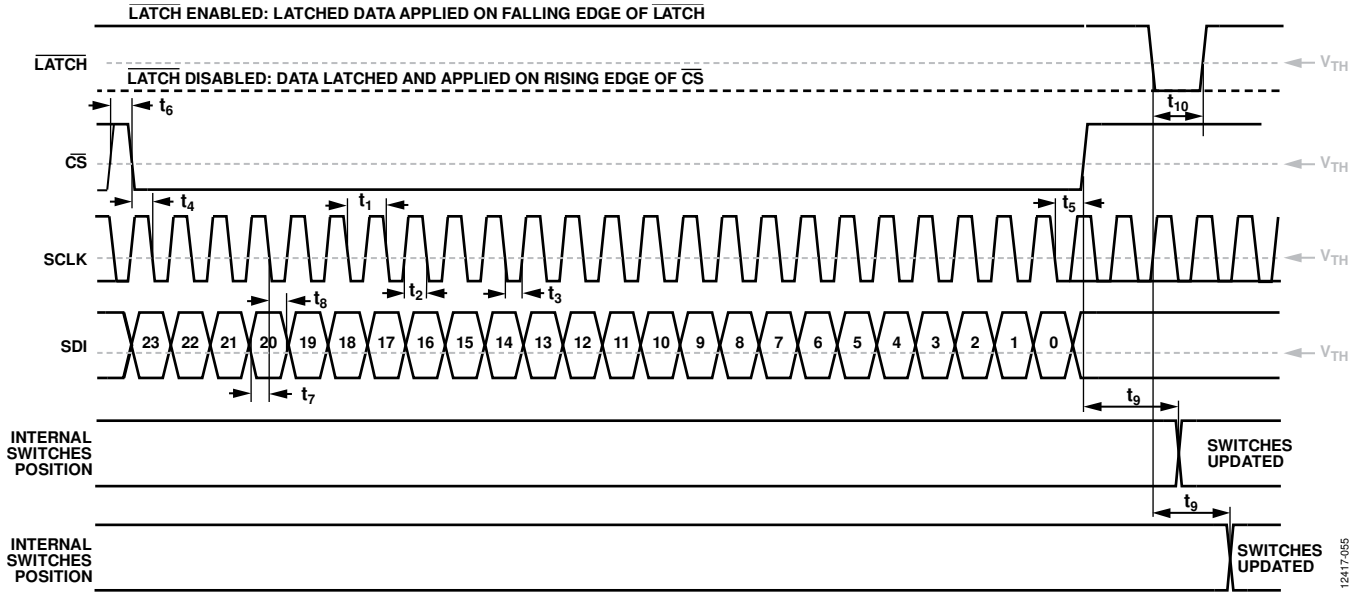

Figure 2. Write Operation

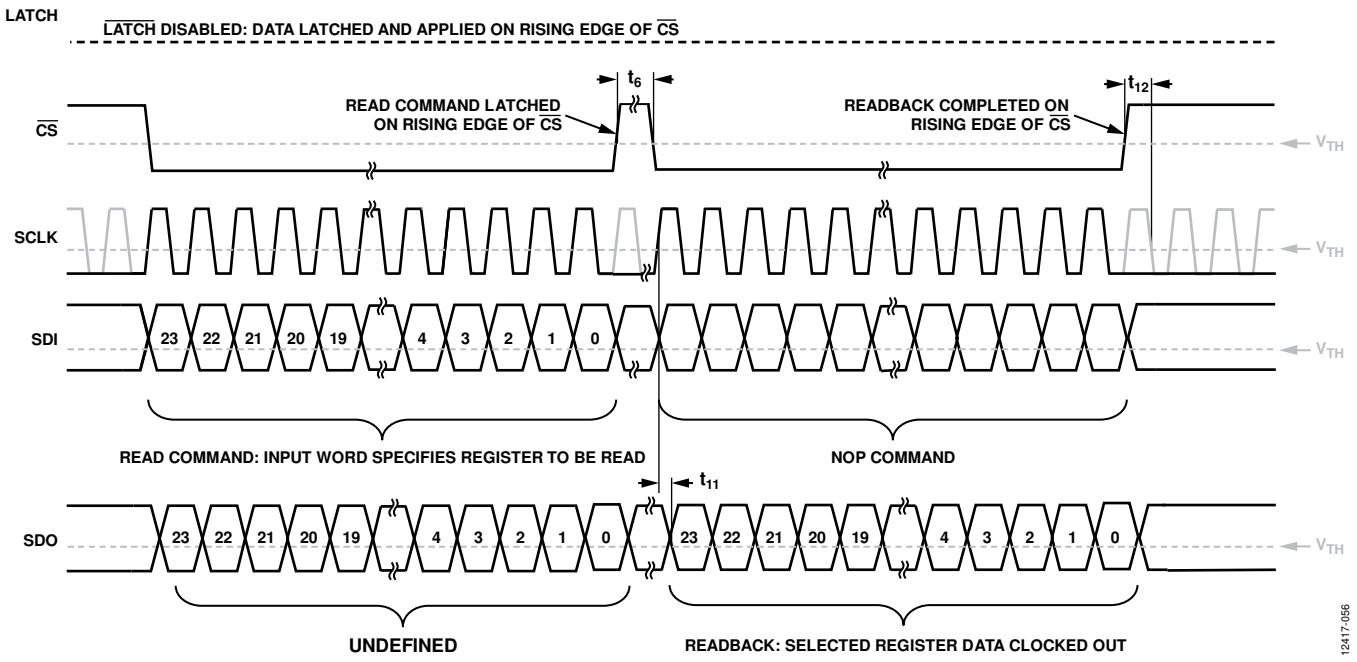

Figure 3. Read Operation

ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter	Rating
Analog Supply Voltage	14 V
Digital Supply Voltage	5.5 V
Power Dissipation	See Figure 4
Common-Mode Input Voltage	±Vs ± 0.3V
Differential Input Voltage	±0.7 V
Input Current (IN-N, IN-P, VIN1, RF1, and REF)	20 mA
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, θ_{JA} is specified for a device soldered in a circuit board for surface-mount packages. Table 11 lists the θ_{JA} for the ADA4350.

Table 11. Thermal Resistance

Package Type	θ_{JA}	Unit
28-Lead TSSOP	72.4	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the ADA4350 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4350. Exceeding a junction temperature of 175°C for an extended period can result in changes in silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the die due to the ADA4350 output load drive.

The quiescent power dissipation is the voltage between the supply pins ($\pm V_S$) multiplied by the quiescent current (I_S).

$$P_D = Quiescent\ Power + (Total\ Drive\ Power - Load\ Power)$$

$$P_D = \left(\pm V_S \times I_S\right) + \left(\frac{\pm V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

Consider rms output voltages. If R_L is referenced to $-V_S$, as in single-supply operation, the total drive power is $+V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = +V_S/4$ for R_L to midsupply for dual supplies and $V_{OUT} = +V_S/2$ for single supply.

$$P_D = \left(+V_S \times I_S\right) + \frac{\left(V_{OUT}\right)^2}{R_L}$$

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads and exposed pad from metal traces, through holes, ground, and power planes reduces θ_{JA}.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

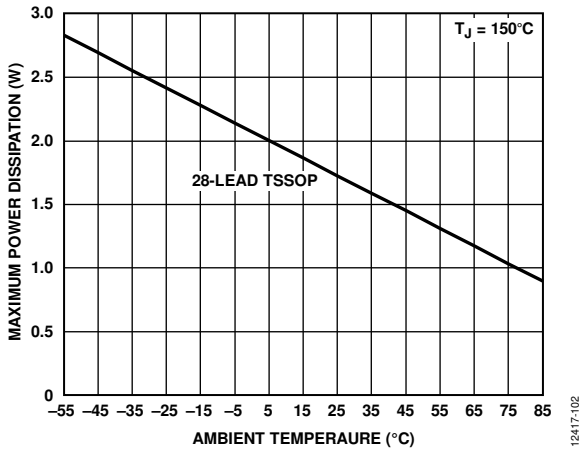

Figure 4. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

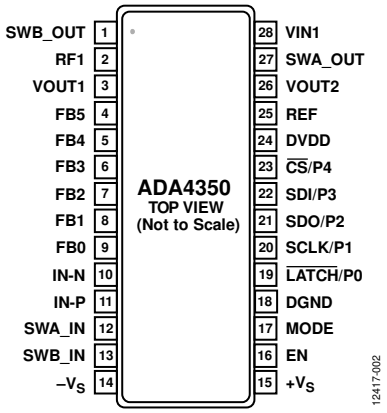

Figure 5. Pin Configuration

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SWB_OUT	Switch Group B (S3 to S5 and S9 to S11) Output.
2	RF1	Feedback Resistor for Output Differential Amplifier.
3	VOUT1	Differential Amplifier Output 1.
4	FB5	Feedback Pin 5 for FET Input Amplifier.
5	FB4	Feedback Pin 4 for FET Input Amplifier.
6	FB3	Feedback Pin 3 for FET Input Amplifier.
7	FB2	Feedback Pin 2 for FET Input Amplifier.
8	FB1	Feedback Pin 1 for FET Input Amplifier.
9	FB0	Feedback Pin 0 for FET Input Amplifier.
10	IN-N	FET Input Amplifier Inverting Input.
11	IN-P	FET Input Amplifier Noninverting Input.
12	SWA_IN	Switch Group A (S0 to S2 and S6 to S8) Input.
13	SWB_IN	Switch Group B (S3 to S5 and S9 to S11) Input.
14	$-V_S$	Analog Negative Supply.
15	$+V_S$	Analog Positive Supply.
16	EN	Enable Pin.
17	MODE	Mode Pin. Use this pin to switch between the SPI interface and the parallel interface.
18	DGND	Digital Ground.
19	$\overline{\text{LATCH}}$/P0	Latch Bit in the Serial Mode ($\overline{\text{LATCH}}$). Parallel Data Bit 0 in parallel mode (P0).
20	SCLK/P1	Digital Clock in Serial Mode (SCLK). Parallel Data Bit 1 in parallel mode (P1).
21	SDO/P2	Serial Data Out in Serial Mode (SDO). Parallel Data Bit 2 in parallel mode (P2).
22	SDI/P3	Serial Data In in Serial Mode (SDI). Parallel Data Bit 3 in parallel mode (P3).
23	$\overline{\text{CS}}$/P4	Select Bit in Serial Mode ($\overline{\text{CS}}$). Parallel Data Bit 4 in parallel mode (P4).
24	DVDD	Digital Positive Supply.
25	REF	Reference for the ADC Driver at M1.
26	VOUT2	Differential Amplifier Output 2.
27	SWA_OUT	Switch Group A (S0 to S2 and S6 to S8) Output.
28	VIN1	Differential Amplifier Noninverting Input.

TYPICAL PERFORMANCE CHARACTERISITICS

FULL SYSTEM

These plots are for the full system, which includes the FET input amplifier, the switching network, and the ADC driver. Unless otherwise stated, R_L = 1 kΩ differential. For Vs = ±5 V, DVDD = +5 V, and for Vs = +5 V (or ±2.5 V), DVDD = +3.3 V.

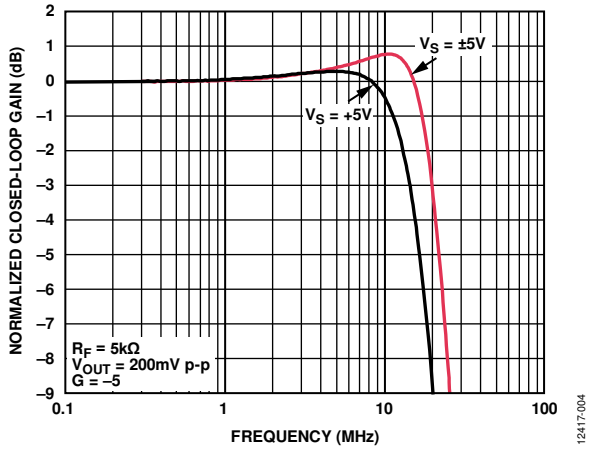

Figure 6. Small Signal Frequency Response for Various Supplies, See Test Circuit in Figure 49

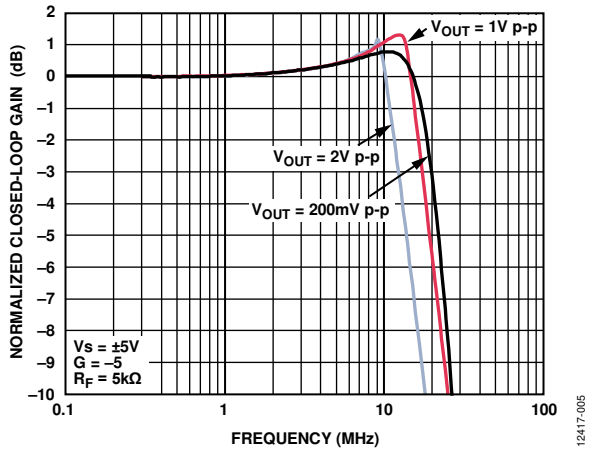

Figure 7. Frequency Response for Various Voltage Outputs, See Test Circuit in Figure 49

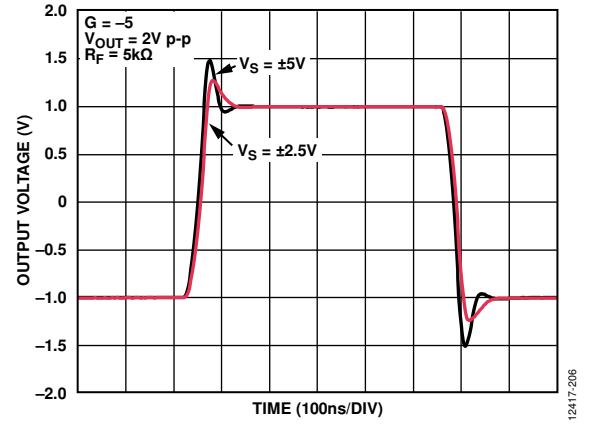

Figure 8. Large Signal Step Response, G = –5 for Various Supplies

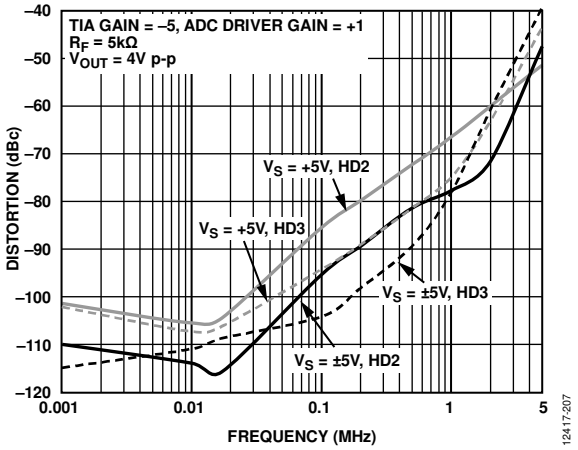

Figure 9. Harmonic Distortion vs. Frequency for Various Supplies, See Test Circuit in Figure 48

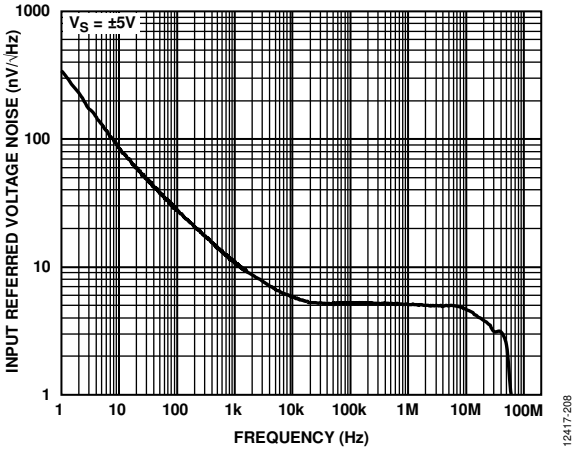

Figure 10. Input Referred Voltage Noise vs. Frequency

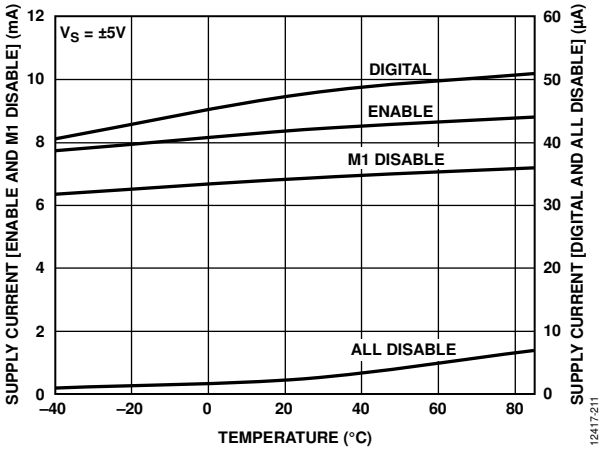

Figure 11. Supply Current vs. Temperature at Different Modes

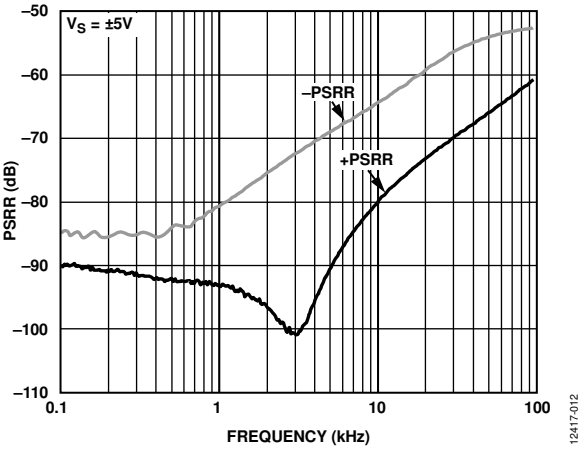

Figure 12. PSRR vs. Frequency

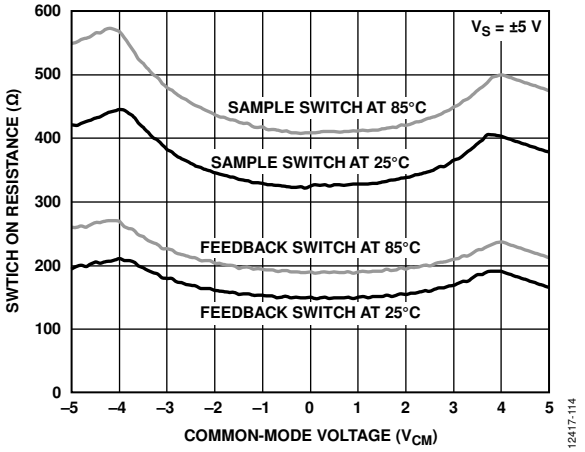

Figure 14. Switch On-Resistance vs. Common-Mode Voltage at Switches for Various Temperature

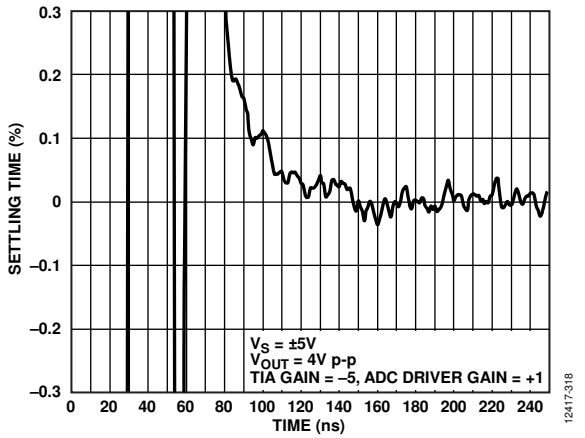

Figure 13. 0.1% Settling Time, See Test Circuit in Figure 49

FET INPUT AMPLIFIER

Unless otherwise stated, R_L = 1 kΩ. For Vs = ±5 V, DVDD = +5 V, and for Vs = ±2.5 V, DVDD = +3.3 V.

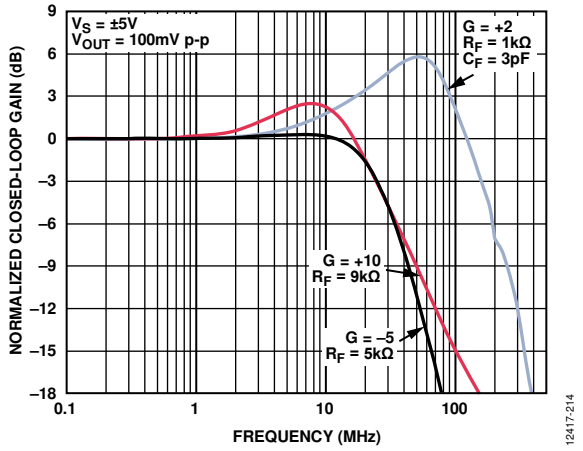

Figure 15. Small Signal Frequency Response for Various Gains, V_S = ±5 V, See Test Circuit Diagrams in Figure 50 and Figure 51

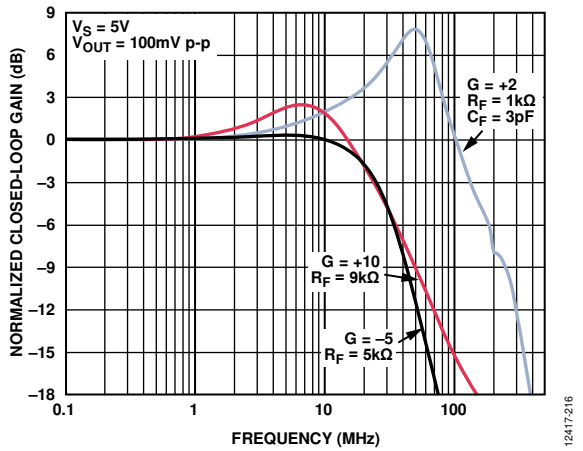

Figure 16. Small Signal Frequency Response for Various Gains, V_S = 5 V, See Test Circuit Diagrams in Figure 50 and Figure 51

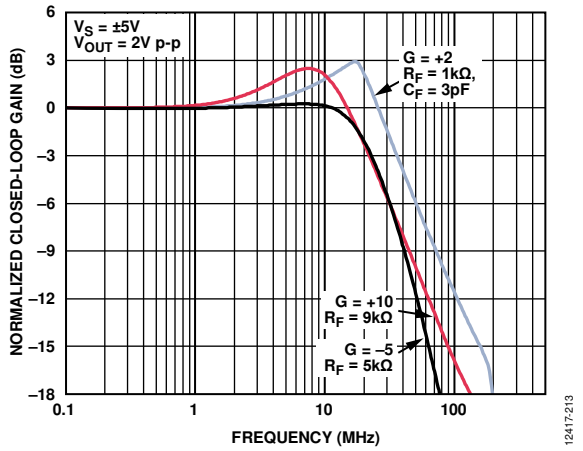

Figure 17. Large Signal Frequency Response for Various Gains, V_S = ±5 V, See Test Circuit Diagrams in Figure 50 and Figure 51

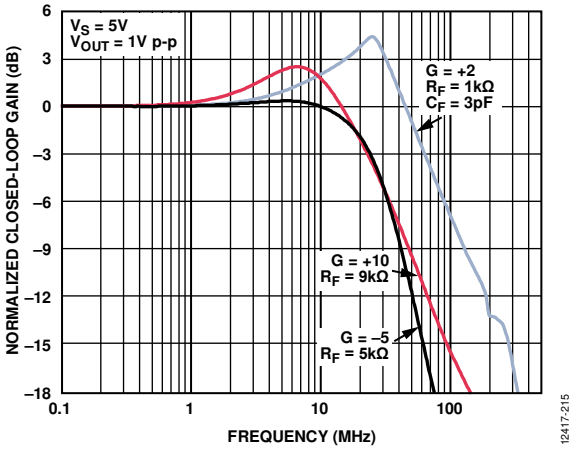

Figure 18. Large Signal Frequency Response for Various Gains, V_S = 5 V, See Test Circuit Diagrams in Figure 50 and Figure 51

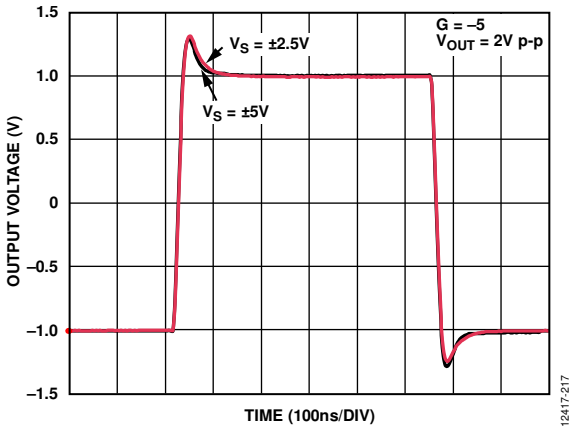

Figure 19. Large Signal Step Response for Various Supplies, G = –5

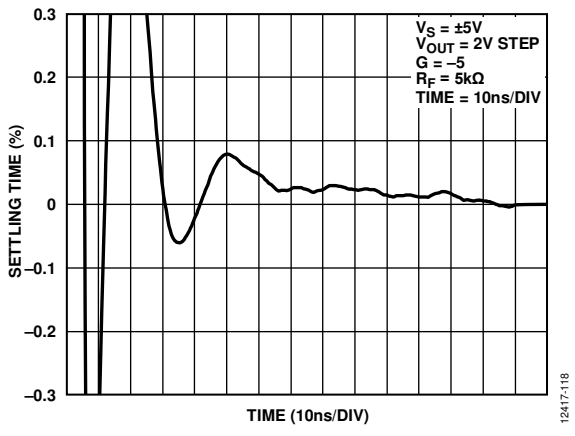

Figure 20. 0.1% Settling Time

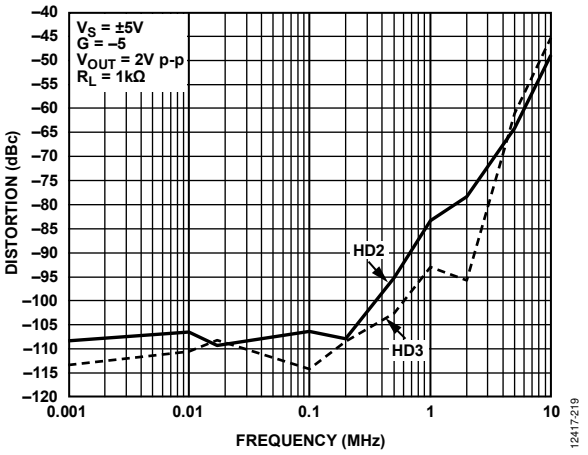

Figure 21. Distortion (HD2/HD3) vs. Frequency, G = –5

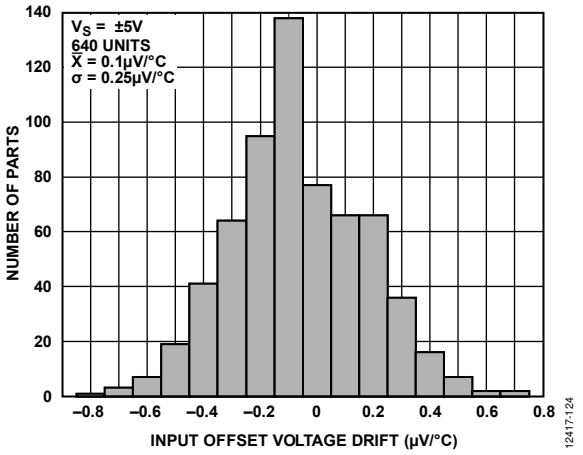

Figure 24. Input Offset Voltage Drift

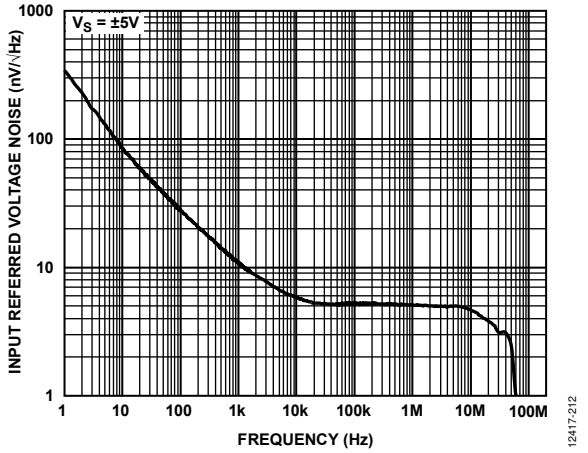

Figure 22. Input Voltage Noise

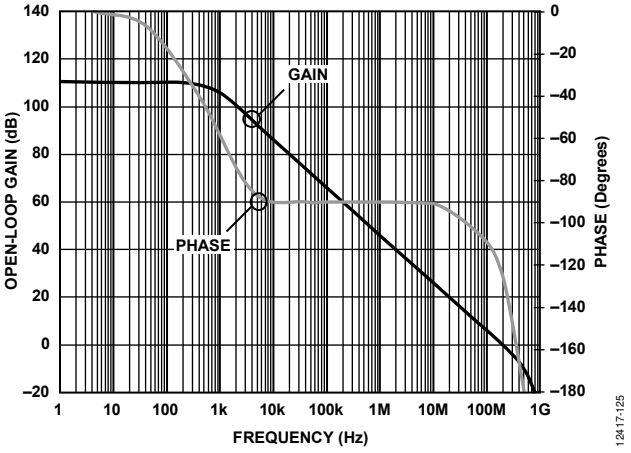

Figure 25. Open-Loop Gain and Phase vs. Frequency

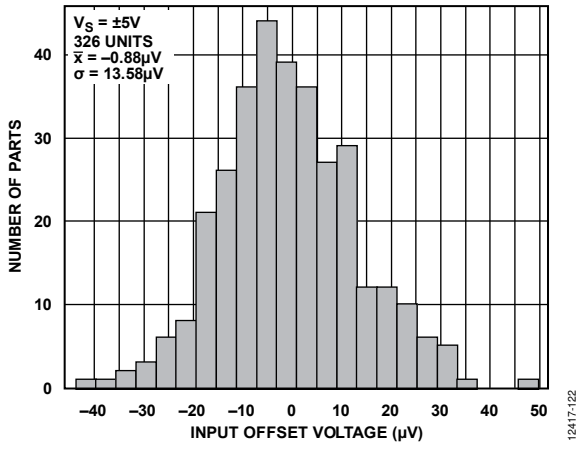

Figure 23. Input Offset Voltage

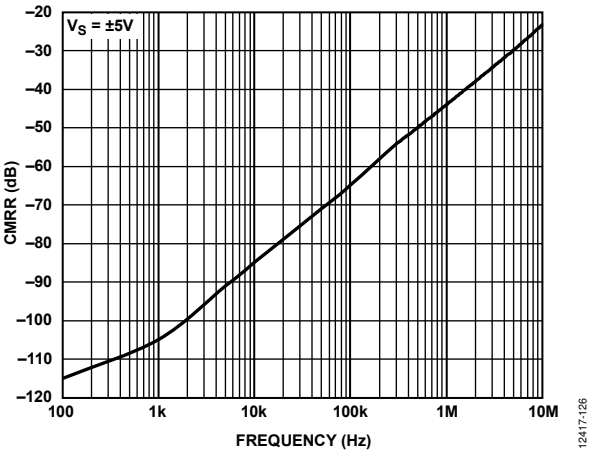

Figure 26. CMRR vs Frequency

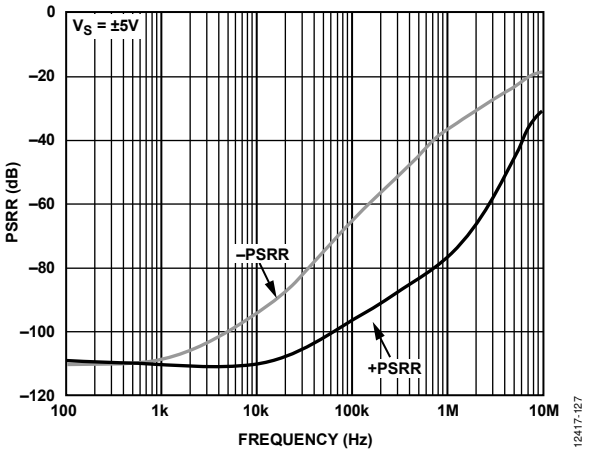

Figure 27. PSRR vs Frequency

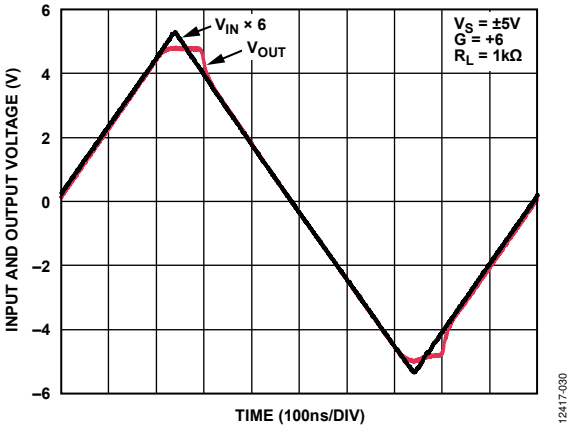

Figure 28. Output Overdrive Recovery when Used as an Amplifier

ADC DRIVER

Unless stated otherwise, R_L = 1 kΩ differential, and R_L = 500 Ω when single-ended. For V_S = ±5 V, DVDD = +5 V, and for V_S = +5 V (or ±2.5 V), DVDD = +3.3 V.

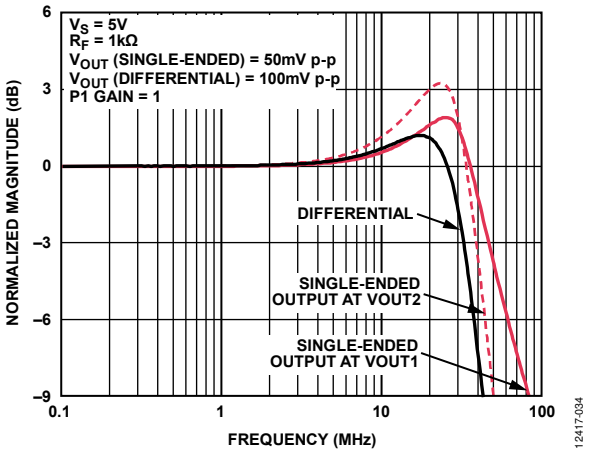

Figure 29. Small Signal Frequency Response, V_S = 5 V

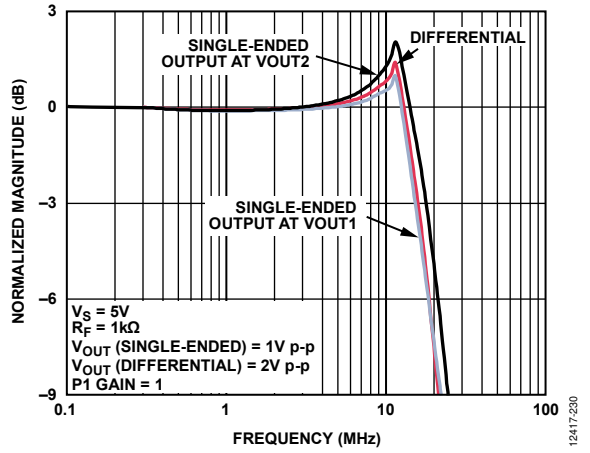

Figure 30. Large Signal Frequency Response, V_S = 5 V

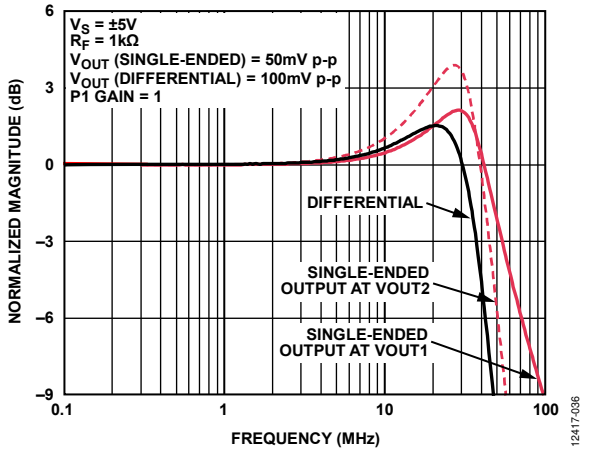

Figure 31. Small Signal Frequency Response, V_S = ±5 V

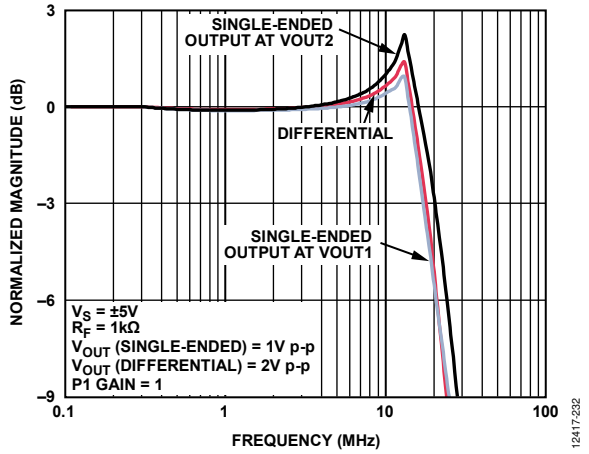

Figure 32. Large Signal Frequency Response, V_S =±5 V

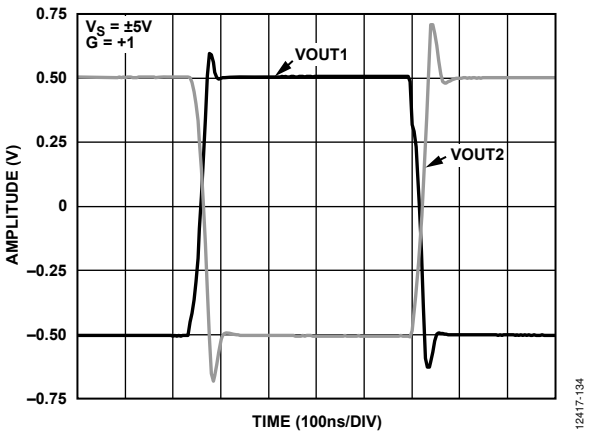

Figure 33. Large Signal Step Response (Single-Ended Output), V_S = ±5 V

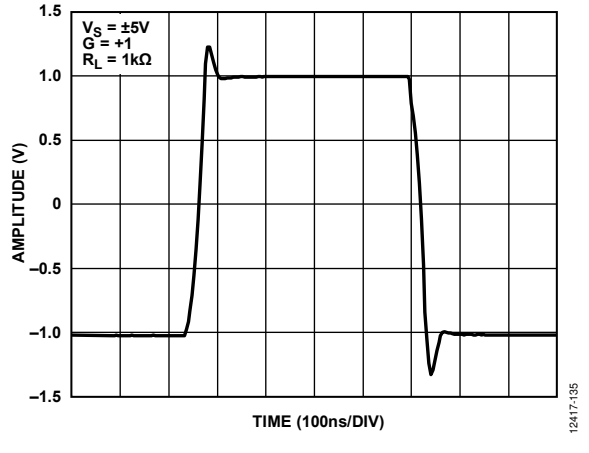

Figure 34. Large Signal Step Response (Differential Output), V_S = ±5 V

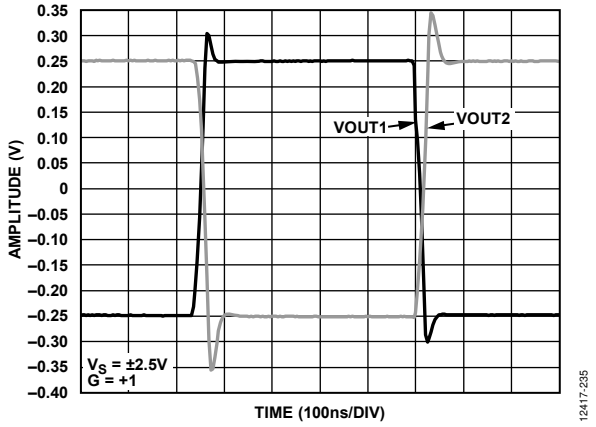

Figure 35. Large Signal Step Response (Single-Ended Output), V_S = ±2.5 V

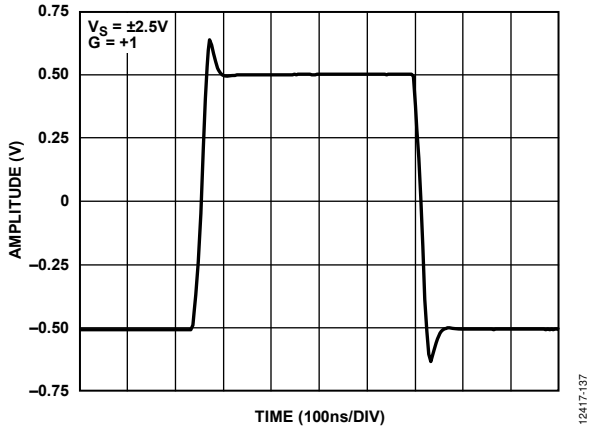

Figure 36. Large Signal Step Response (Differential Output), V_S = ±2.5 V

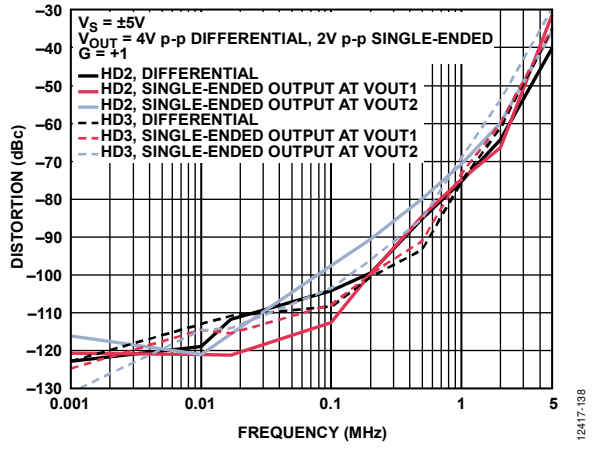

Figure 37. Harmonic Distortion vs. Frequency

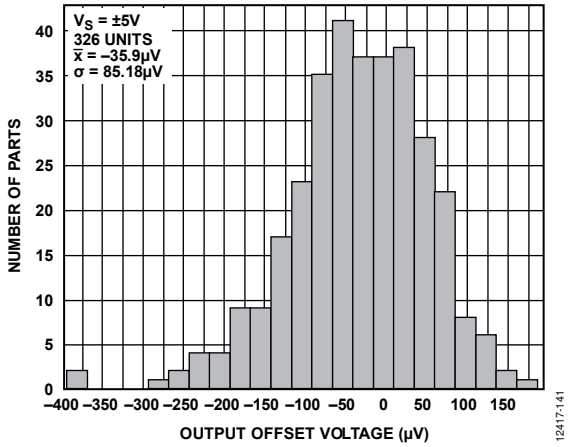

Figure 38. Differential Output Offset Voltage

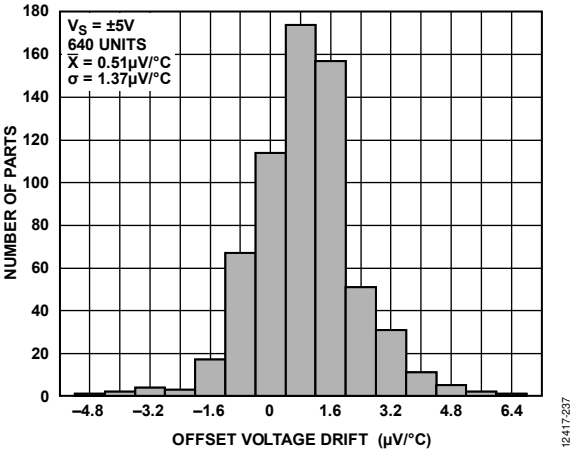

Figure 39. Differential Output Offset Voltage Drift

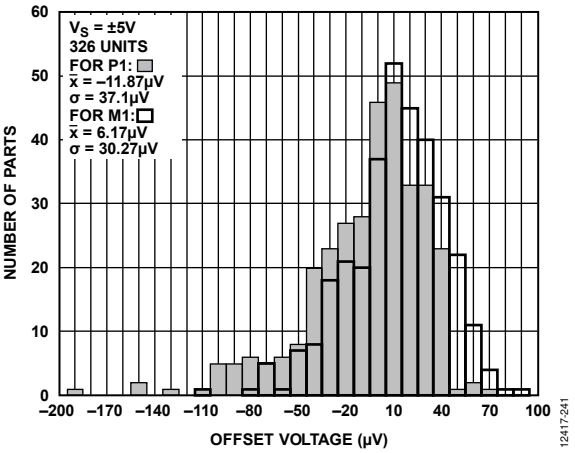

Figure 40. Single-Ended Output Offset Voltage

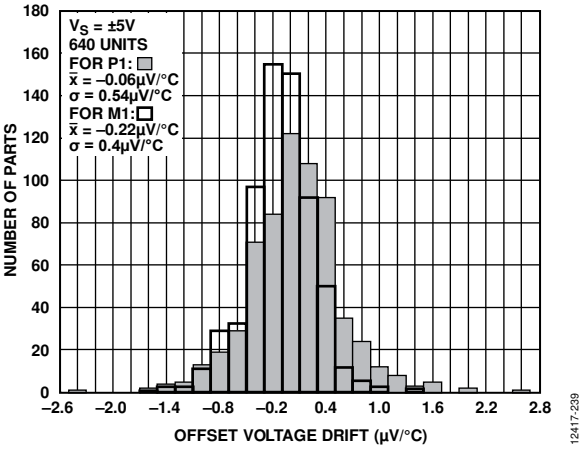

Figure 41. Single-Ended Offset Voltage Drift

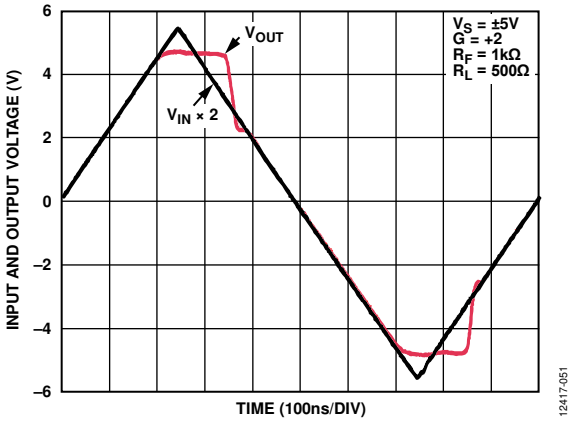

Figure 44. Output Overdrive Recovery (M1 Only)

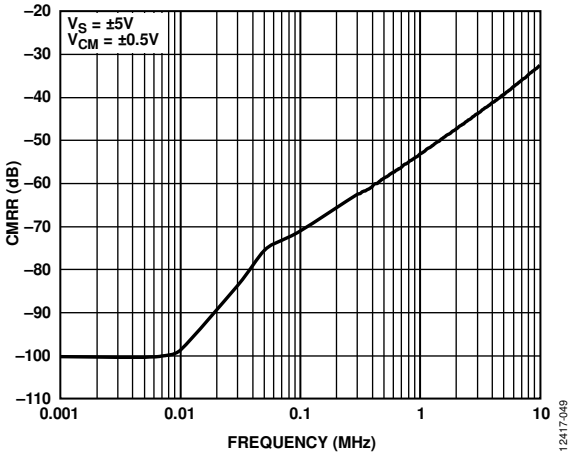

Figure 42. CMRR vs. Frequency

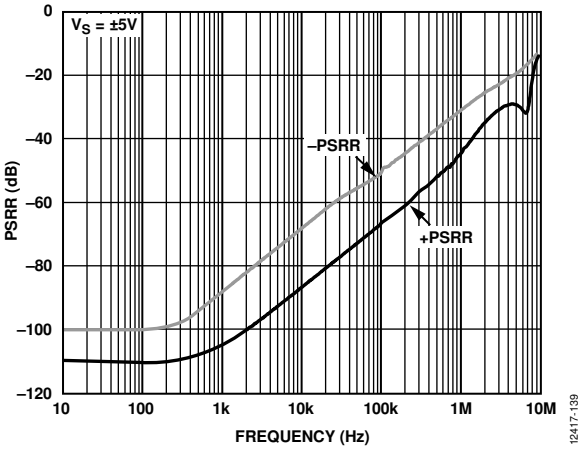

Figure 45. PSRR vs. Frequency (P1 Only)

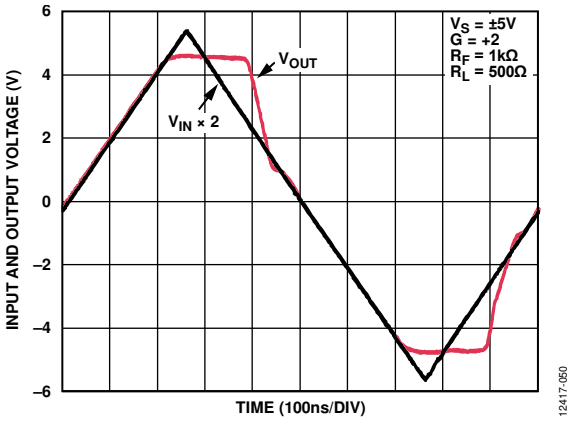

Figure 43. Output Overdrive Recovery (P1 Only)