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FEATURES

- Low offset voltage: 5 μ V maximum**
- Extremely low offset voltage drift: 22 nV/ $^{\circ}$ C maximum**
- Low voltage noise density: 5.8 nV/ $\sqrt{\text{Hz}}$ typical**
117 nV p-p typical from 0.1 Hz to 10 Hz
- Low input bias current: 50 pA typical**
- Unity-gain crossover: 3 MHz typical**
- Single-supply operation: input voltage range includes ground and rail-to-rail output**
- Wide range of operating voltages**
Single-supply operation: 4.5 V to 55 V
Dual-supply operation: ± 2.25 V to ± 27.5 V
- Integrated EMI filters**
- Unity-gain stable**

APPLICATIONS

- Inductance, capacitance, and resistance (LCR) meter/megohmmeter front-end amplifiers**
- Load cell and bridge transducers**
- Magnetic force balance scales**
- High precision shunt current sensing**
- Thermocouple/resistance temperature detector (RTD) sensors**
- Programmable logic controller (PLC) input and output amplifiers**

GENERAL DESCRIPTION

The ADA4522-1/ADA4522-2/ADA4522-4 are single/dual/quadruple channel, zero drift op amps with low noise and power, ground sensing inputs, and rail-to-rail output, optimized for total accuracy over time, temperature, and voltage conditions. The wide operating voltage and temperature ranges, as well as the high open-loop gain and very low dc and ac errors make the devices well suited for amplifying very small input signals and for accurately reproducing larger signals in a wide variety of applications.

The ADA4522-1/ADA4522-2/ADA4522-4 performance is specified at 5.0 V, 30 V, and 55 V power supply voltages. These devices operate over the range of 4.5 V to 55 V, and are excellent for applications using single-ended supplies of 5 V, 10 V, 12 V, and 30 V, or for applications using higher single supplies and dual supplies of ± 2.5 V, ± 5 V, and ± 15 V. The ADA4522-1/ADA4522-2/ADA4522-4 use on-chip filtering to achieve high immunity to electromagnetic interference (EMI).

The ADA4522-1/ADA4522-2/ADA4522-4 are fully specified over the extended industrial temperature range of -40°C to $+125^{\circ}\text{C}$ and are available in 8-lead MSOP, 8-lead SOIC, 14-lead SOIC, and 14-lead TSSOP packages.

Rev. E

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PIN CONNECTION DIAGRAM

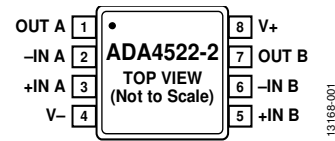


Figure 1. 8-Lead MSOP (RM Suffix) and 8-Lead SOIC (R Suffix) Pin Configuration

For the ADA4522-1 and ADA4522-4 pin connections and for more information about the pin connections for these products, see the Pin Configurations and Function Descriptions section.

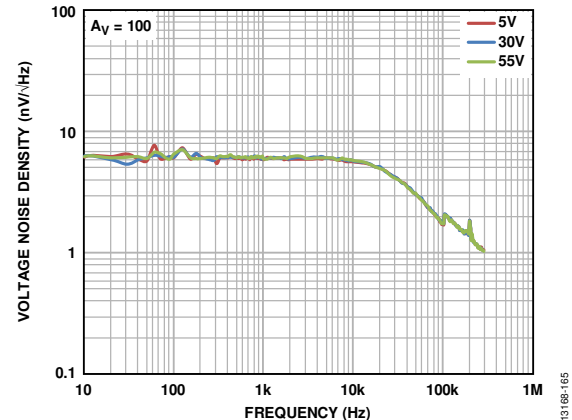


Figure 2. Voltage Noise Density vs. Frequency, $V_{SY} = \pm 15$ V

Table 1. Zero Drift Op Amps ($<0.1 \mu\text{V}/^{\circ}\text{C}$)

Supply Voltage	5 V	16 V	30 V	55 V
Single	ADA4528-1 AD8628 AD8538 ADA4051-1	AD8638	ADA4638-1	ADA4522-1
Dual	ADA4528-2 AD8629 AD8539 ADA4051-2	AD8639		ADA4522-2
Quad	AD8630			ADA4522-4

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REVISION HISTORY

10/2016—Rev. D to Rev. E

Changes to Figure 73..... 23

4/2016—Rev. C to Rev. D

Changed ADA4522-4 Pin 4 to V+ Throughout
 Changed ADA4522-4 Pin 11 to V- Throughout
 Changes to Figure 5 and Table 9..... 9

2/2016—Rev. B to Rev. C

Added ADA4522-1..... Universal
 Changes to Common-Mode Rejection Ratio Parameter and
 Supply Current per Amplifier Parameter, Table 2..... 3
 Changes to Offset Voltage Drift Parameter, and Supply Current
 per Amplifier Parameter, Table 3..... 4
 Changes to Offset Voltage Drift Parameter, Input Offset Current
 Parameter, and Supply Current per Amplifier Parameter,
 Table 4

1/2016—Rev. A to Rev. B

Updated Outline Dimensions

10/2015—Rev. 0 to Rev. A

Added ADA4522-4..... Universal
 Changes to General Description Section

5/2015—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5.0 V OPERATION

$V_{SY} = 5.0 \text{ V}$, $V_{CM} = V_{SY}/2$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_{SY}/2$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.7	5	μV
Offset Voltage Drift	TCV_{OS}			2.5	15	$\text{nV}/^\circ\text{C}$
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		50	150	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		80	250	pA
Input Voltage Range	IVR		0		3.5	V
Common-Mode Rejection Ratio	CMRR	ADA4522-1, ADA4522-2, $V_{CM} = 0 \text{ V to } 3.5 \text{ V}$ ADA4522-4, $V_{CM} = 0 \text{ V to } 3.5 \text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	135	155		dB
Large Signal Voltage Gain	A_V	$R_L = 10 \text{ k}\Omega$, $V_{OUT} = 0.5 \text{ V to } 4.5 \text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	130	145		dB
Input Resistance						
Differential Mode	R_{INDM}			30		$\text{k}\Omega$
Common Mode	R_{INCM}			100		$\text{G}\Omega$
Input Capacitance						
Differential Mode	C_{INDM}			7		pF
Common Mode	C_{INCM}			35		pF
OUTPUT CHARACTERISTICS						
Output Voltage						
High	V_{OH}	$R_L = 10 \text{ k}\Omega$ to $V_{SY}/2$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.97	4.98		V
Low	V_{OL}	$R_L = 10 \text{ k}\Omega$ to $V_{SY}/2$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.95	20	30	mV
Continuous Output Current	I_{OUT}	Dropout voltage = 1 V		14		mA
Short-Circuit Current Source	I_{SC+}	$T_A = 125^\circ\text{C}$		22		mA
Short-Circuit Current Sink	I_{SC-}	$T_A = 125^\circ\text{C}$		15		mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 1 \text{ MHz}$, $A_V = 1$		19		mA
			4			Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 4.5 \text{ V to } 5.5 \text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	150	160		dB
Supply Current per Amplifier	I_{SY}	ADA4522-2, ADA4522-4, $I_{OUT} = 0 \text{ mA}$ ADA4522-2, ADA4522-4, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ ADA4522-1, $I_{OUT} = 0 \text{ mA}$ ADA4522-1, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	145	830	900	μA
					950	μA
				840	910	μA
					970	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR+	$R_L = 10 \text{ k}\Omega$, $C_L = 50 \text{ pF}$, $A_V = 1$		1.4		$\text{V}/\mu\text{s}$
	SR-	$R_L = 10 \text{ k}\Omega$, $C_L = 50 \text{ pF}$, $A_V = 1$		1.3		$\text{V}/\mu\text{s}$

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Gain Bandwidth Product	GBP	$V_{IN} = 10\text{ mV p-p}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 100$		2.7		MHz
Unity-Gain Crossover	UGC	$V_{IN} = 10\text{ mV p-p}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		3		MHz
-3 dB Closed-Loop Bandwidth	$f_{-3\text{ dB}}$	$V_{IN} = 10\text{ mV p-p}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		6.5		MHz
Phase Margin	Φ_M	$V_{IN} = 10\text{ mV p-p}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		64		Degrees
Settling Time to 0.1%	t_s	$V_{IN} = 1\text{ V step}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		4		μs
Channel Separation	CS	$V_{IN} = 1\text{ V p-p}, f = 10\text{ kHz}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}$		98		dB
EMI Rejection Ratio of +IN/+IN x	EMIRR	$V_{IN} = 100\text{ mV peak}, f = 400\text{ MHz}$		72		dB
		$V_{IN} = 100\text{ mV peak}, f = 900\text{ MHz}$		80		dB
		$V_{IN} = 100\text{ mV peak}, f = 1800\text{ MHz}$		83		dB
		$V_{IN} = 100\text{ mV peak}, f = 2400\text{ MHz}$		85		dB
NOISE PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD + N	$A_V = 1, f = 1\text{ kHz}, V_{IN} = 0.6\text{ V rms}$		0.001		%
Bandwidth (BW) = 80 kHz				0.02		%
Bandwidth (BW) = 500 kHz						
Peak-to-Peak Voltage Noise	$e_{N\text{ p-p}}$	$A_V = 100, f = 0.1\text{ Hz to }10\text{ Hz}$		117		nV p-p
Voltage Noise Density	e_N	$A_V = 100, f = 1\text{ kHz}$		5.8		nV/ $\sqrt{\text{Hz}}$
Peak-to-Peak Current Noise	$i_{N\text{ p-p}}$	$A_V = 100, f = 0.1\text{ Hz to }10\text{ Hz}$		16		pA p-p
Current Noise Density	i_N	$A_V = 100, f = 1\text{ kHz}$		0.8		pA/ $\sqrt{\text{Hz}}$

ELECTRICAL CHARACTERISTICS—30 V OPERATION

$V_{SY} = 30\text{ V}, V_{CM} = V_{SY}/2\text{ V}, T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_{SY}/2$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1	5	μV
Offset Voltage Drift	TCV_{OS}	ADA4522-1, ADA4522-2 ADA4522-4		4	22	nV/ $^\circ\text{C}$
				5.3	25	nV/ $^\circ\text{C}$
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		50	150	pA
					500	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		3	300	nA
				80	400	pA
					500	pA
Input Voltage Range	IVR		0		28.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }28.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		145	160	dB
				140		dB
Large Signal Voltage Gain	A_V	$R_L = 10\text{ k}\Omega, V_{OUT} = 0.5\text{ V to }29.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		140	150	dB
				135		dB
Input Resistance	R_{INDM} R_{INCM}			30		k Ω
				400		G Ω
Input Capacitance	C_{INDM} C_{INCM}			7		pF
				35		pF
OUTPUT CHARACTERISTICS						
Output Voltage	V_{OH}	$R_L = 10\text{ k}\Omega\text{ to }V_{SY}/2$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	29.87	29.89		V
			29.80			V
Low	V_{OL}	$R_L = 10\text{ k}\Omega\text{ to }V_{SY}/2$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		110	130	mV
					200	mV
Continuous Output Current	I_{OUT}	Dropout voltage = 1 V		14		mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Short-Circuit Current Source	I_{SC+}	$T_A = 125^\circ\text{C}$		21		mA
Short-Circuit Current Sink	I_{SC-}	$T_A = 125^\circ\text{C}$		15		mA
Closed-Loop Output Impedance	Z_{OUT}	$T_A = 125^\circ\text{C}$ $f = 1\text{ MHz}, A_V = 1$		33		mA
				22		mA
				4		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 4.5\text{ V to }55\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	150	160		dB
Supply Current per Amplifier	I_{SY}	ADA4522-2, ADA4522-4, $I_{OUT} = 0\text{ mA}$ ADA4522-2, ADA4522-4, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ ADA4522-1, $I_{OUT} = 0\text{ mA}$ ADA4522-1, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	145	830	900	μA
					950	μA
				840	910	μA
					970	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR+	$R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		1.8		V/ μs
	SR-	$R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		0.9		V/ μs
Gain Bandwidth Product	GBP	$V_{IN} = 10\text{ mV p-p}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 100$		2.7		MHz
Unity-Gain Crossover	UGC	$V_{IN} = 10\text{ mV p-p}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		3		MHz
-3 dB Closed-Loop Bandwidth	$f_{-3\text{ dB}}$	$V_{IN} = 10\text{ mV p-p}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		6.5		MHz
Phase Margin	Φ_M	$V_{IN} = 10\text{ mV p-p}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		64		Degrees
Settling Time to 0.1%	t_s	$V_{IN} = 10\text{ V step}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		12		μs
Settling Time to 0.01%	t_s	$V_{IN} = 10\text{ V step}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		14		μs
Channel Separation	CS	$V_{IN} = 10\text{ V p-p}, f = 10\text{ kHz}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}$		98		dB
EMI Rejection Ratio of +IN/+IN x	EMIRR	$V_{IN} = 100\text{ mV peak}, f = 400\text{ MHz}$ $V_{IN} = 100\text{ mV peak}, f = 900\text{ MHz}$ $V_{IN} = 100\text{ mV peak}, f = 1800\text{ MHz}$ $V_{IN} = 100\text{ mV peak}, f = 2400\text{ MHz}$		72		dB
				80		dB
				83		dB
				85		dB
NOISE PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD + N	$A_V = 1, f = 1\text{ kHz}, V_{IN} = 6\text{ V rms}$		0.0005		%
BW = 80 kHz				0.004		%
BW = 500 kHz						
Peak-to-Peak Voltage Noise	$e_{N\text{ p-p}}$	$A_V = 100, f = 0.1\text{ Hz to }10\text{ Hz}$		117		nV p-p
Voltage Noise Density	e_N	$A_V = 100, f = 1\text{ kHz}$		5.8		nV/ $\sqrt{\text{Hz}}$
Peak-to-Peak Current Noise	$i_{N\text{ p-p}}$	$A_V = 100, f = 0.1\text{ Hz to }10\text{ Hz}$		16		pA p-p
Current Noise Density	i_N	$A_V = 100, f = 1\text{ kHz}$		0.8		pA/ $\sqrt{\text{Hz}}$

ELECTRICAL CHARACTERISTICS—55 V OPERATION

$V_{SY} = 55\text{ V}, V_{CM} = V_{SY}/2\text{ V}, T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_{SY}/2$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1.5	7	μV
Offset Voltage Drift	TCV_{OS}	ADA4522-1, ADA4522-2 ADA4522-4		6	30	nV/ $^\circ\text{C}$
				9	40	nV/ $^\circ\text{C}$
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		50	150	pA
					500	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ ADA4522-1, ADA4522-2, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ ADA4522-4, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		80	300	pA
					400	pA
					500	pA
					550	pA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Input Voltage Range	IVR		0		53.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 53.5\text{ V}$ $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	140	144		dB
Large Signal Voltage Gain	A_V	$R_L = 10\text{ k}\Omega$, $V_{OUT} = 0.5\text{ V to } 54.5\text{ V}$ $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	135	137		dB
Input Resistance						
Differential Mode	R_{INDM}			30		k Ω
Common Mode	R_{INCM}			1000		G Ω
Input Capacitance						
Differential Mode	C_{INDM}			7		pF
Common Mode	C_{INCM}			35		pF
OUTPUT CHARACTERISTICS						
Output Voltage						
High	V_{OH}	$R_L = 10\text{ k}\Omega$ to $V_{SY}/2$ $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	54.75	54.8		V
Low	V_{OL}	$R_L = 10\text{ k}\Omega$ to $V_{SY}/2$ $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	54.65	200	250	mV
Continuous Output Current	I_{OUT}	Dropout voltage = 1 V		14		mA
Short-Circuit Current Source	I_{SC+}	$T_A = 125^{\circ}\text{C}$		21		mA
Short-Circuit Current Sink	I_{SC-}	$T_A = 125^{\circ}\text{C}$		15		mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 1\text{ MHz}$, $A_V = 1$		32		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 4.5\text{ V to } 55\text{ V}$ $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	150	160		dB
Supply Current per Amplifier	I_{SY}	ADA4522-2, ADA4522-4, $I_{OUT} = 0\text{ mA}$ ADA4522-2, ADA4522-4, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ ADA4522-1, $I_{OUT} = 0\text{ mA}$ ADA4522-1, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	145	830	900	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR+	$R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_V = 1$		1.7		V/ μs
	SR-	$R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_V = 1$		0.8		V/ μs
Gain Bandwidth Product	GBP	$V_{IN} = 10\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_V = 100$		2.7		MHz
Unity-Gain Crossover	UGC	$V_{IN} = 10\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_V = 1$		3		MHz
-3 dB Closed-Loop Bandwidth	$f_{-3\text{ dB}}$	$V_{IN} = 10\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_V = 1$		6.5		MHz
Phase Margin	Φ_M	$V_{IN} = 10\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_V = 1$		64		Degrees
Settling Time to 0.1%	t_S	$V_{IN} = 10\text{ V step}$, $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_V = 1$		12		μs
Settling Time to 0.01%	t_S	$V_{IN} = 10\text{ V step}$, $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_V = 1$		14		μs
Channel Separation	CS	$V_{IN} = 10\text{ V p-p}$, $f = 10\text{ kHz}$, $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$		98		dB
EMI Rejection Ratio of +IN/+IN x	EMIRR	$V_{IN} = 100\text{ mV peak}$, $f = 400\text{ MHz}$ $V_{IN} = 100\text{ mV peak}$, $f = 900\text{ MHz}$ $V_{IN} = 100\text{ mV peak}$, $f = 1800\text{ MHz}$ $V_{IN} = 100\text{ mV peak}$, $f = 2400\text{ MHz}$		72		dB
NOISE PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD + N	$A_V = 1$, $f = 1\text{ kHz}$, $V_{IN} = 10\text{ V rms}$		0.0007		%
BW = 80 kHz				0.003		%
BW = 500 kHz						
Peak-to-Peak Voltage Noise	$e_{N\text{ p-p}}$	$A_V = 100$, $f = 0.1\text{ Hz to } 10\text{ Hz}$		117		nV p-p
Voltage Noise Density	e_N	$A_V = 100$, $f = 1\text{ kHz}$		5.8		nV/ $\sqrt{\text{Hz}}$
Peak-to-Peak Current Noise	$i_{N\text{ p-p}}$	$A_V = 100$, $f = 0.1\text{ Hz to } 10\text{ Hz}$		16		pA p-p
Current Noise Density	i_N	$A_V = 100$, $f = 1\text{ kHz}$		0.8		pA/ $\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	60 V
Input Voltage	(V ₋) – 300 mV to (V ₊) + 300 mV
Input Current ¹	±10 mA
Differential Input Voltage	±5 V
Output Short-Circuit Duration to Ground	Indefinite
Temperature Range	
Storage	–65°C to +150°C
Operating	–40°C to +125°C
Junction	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

¹ The input pins have clamp diodes to the power supply pins. Limit the input current to ±10 mA or less whenever input signals exceed the power supply rail by 300 mV.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages using a standard 4-layer JEDEC board.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP (RM-8)	194	38	°C/W
8-Lead SOIC (R-8)	122	41	°C/W
14-Lead TSSOP (RU-14)	112	43	°C/W
14-Lead SOIC (R-14)	115	36	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED.

Figure 3. ADA4522-1 Pin Configuration

Table 7. ADA4522-1 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5, 8	NIC	Not Internally Connected
2	-IN	Inverting Input
3	+IN	Noninverting Input
4	V-	Negative Supply Voltage
6	OUT	Output
7	V+	Positive Supply Voltage

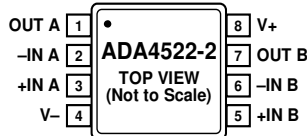


Figure 4. ADA4522-2 Pin Configuration

Table 8. ADA4522-2 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A
2	-IN A	Inverting Input, Channel A
3	+IN A	Noninverting Input, Channel A
4	V-	Negative Supply Voltage
5	+IN B	Noninverting Input, Channel B
6	-IN B	Inverting Input, Channel B
7	OUT B	Output, Channel B
8	V+	Positive Supply Voltage

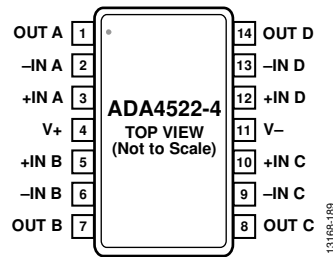


Figure 5. ADA4522-4 Pin Configuration

Table 9. ADA4522-4 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A
2	-IN A	Inverting Input, Channel A
3	+IN A	Noninverting Input, Channel A
4	V+	Positive Supply Voltage
5	+IN B	Noninverting Input, Channel B
6	-IN B	Inverting Input, Channel B
7	OUT B	Output, Channel B
8	OUT C	Output, Channel C
9	-IN C	Inverting Input, Channel C
10	+IN C	Noninverting Input, Channel C
11	V-	Negative Supply Voltage
12	+IN D	Noninverting Input, Channel D
13	-IN D	Inverting Input, Channel D
14	OUT D	Output, Channel D

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

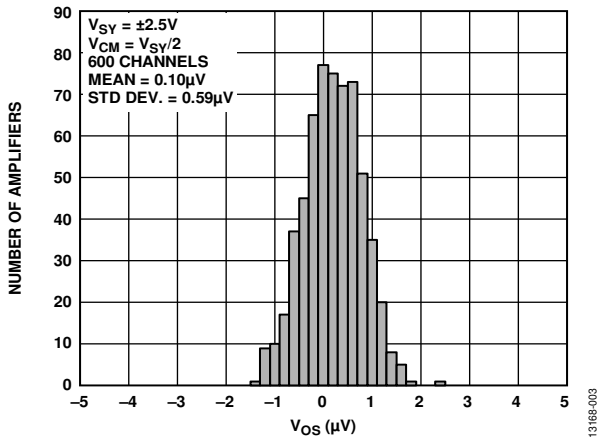


Figure 6. Input Offset Voltage Distribution, $V_{SY} = \pm 2.5V$

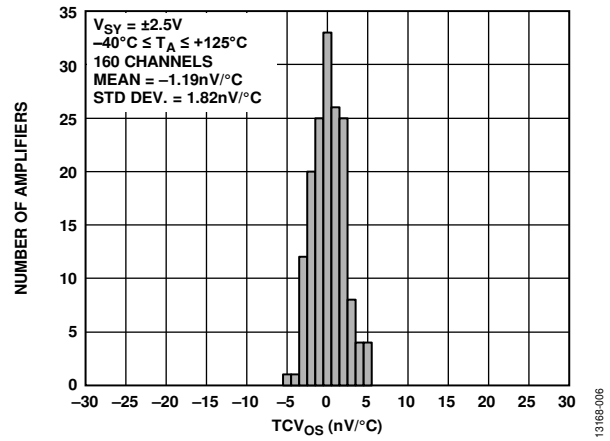


Figure 9. Input Offset Voltage Drift Distribution, $V_{SY} = \pm 2.5V$

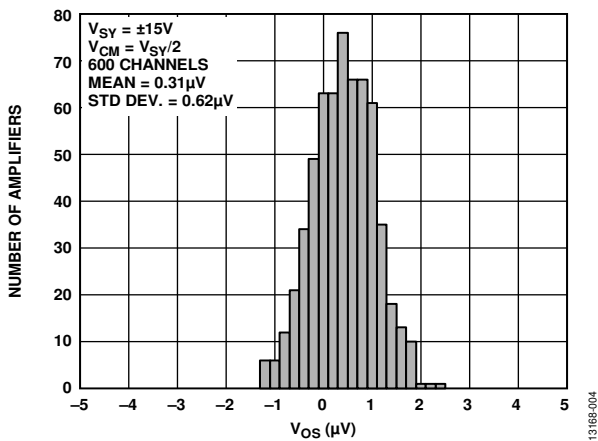


Figure 7. Input Offset Voltage Distribution, $V_{SY} = \pm 15V$

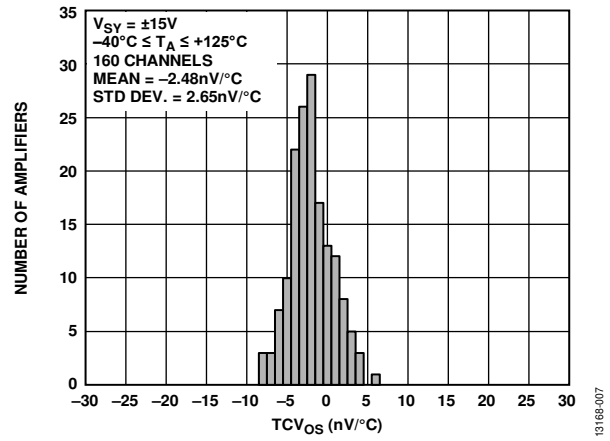


Figure 10. Input Offset Voltage Drift Distribution, $V_{SY} = \pm 15V$

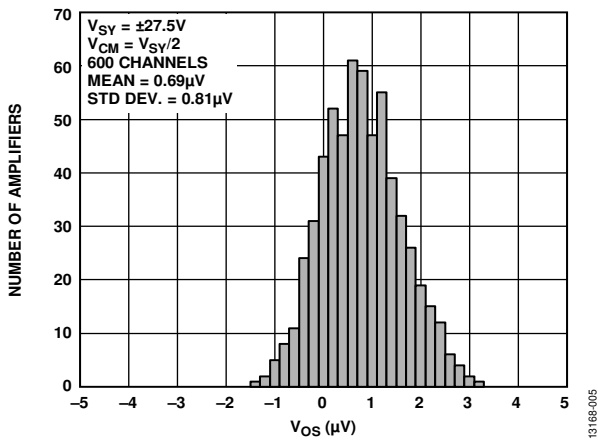


Figure 8. Input Offset Voltage Distribution, $V_{SY} = \pm 27.5V$

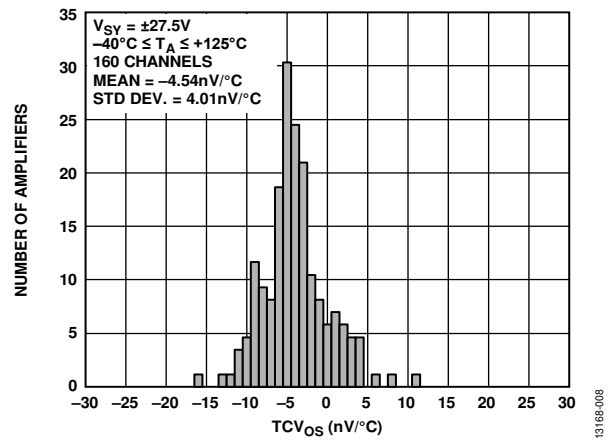


Figure 11. Input Offset Voltage Drift Distribution, $V_{SY} = \pm 27.5V$

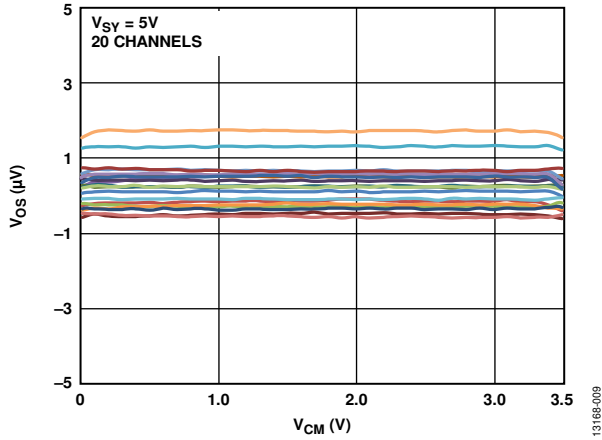


Figure 12. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), $V_{SY} = 5V$

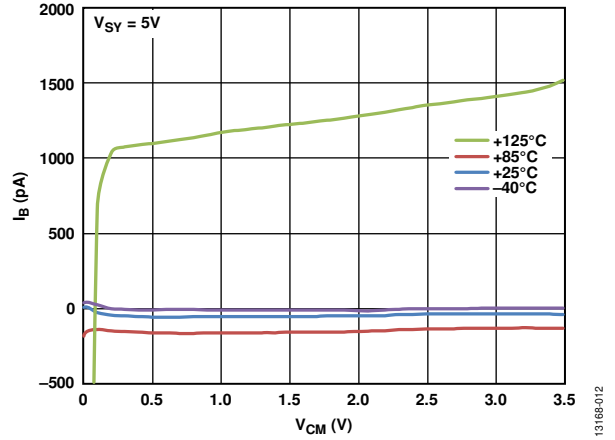


Figure 15. Input Bias Current (I_B) vs. Common-Mode Voltage (V_{CM}), $V_{SY} = 5V$

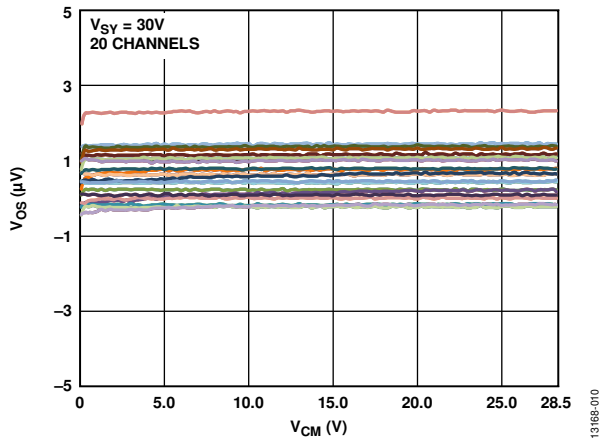


Figure 13. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), $V_{SY} = 30V$

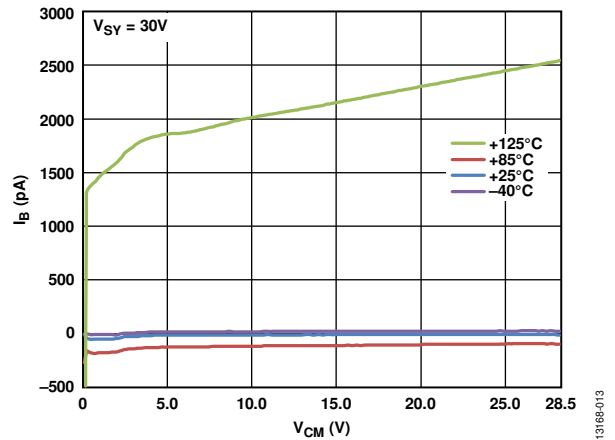


Figure 16. Input Bias Current (I_B) vs. Common-Mode Voltage (V_{CM}), $V_{SY} = 30V$

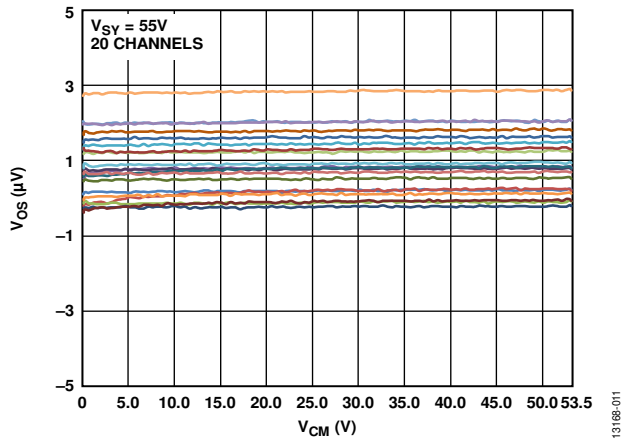


Figure 14. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), $V_{SY} = 55V$

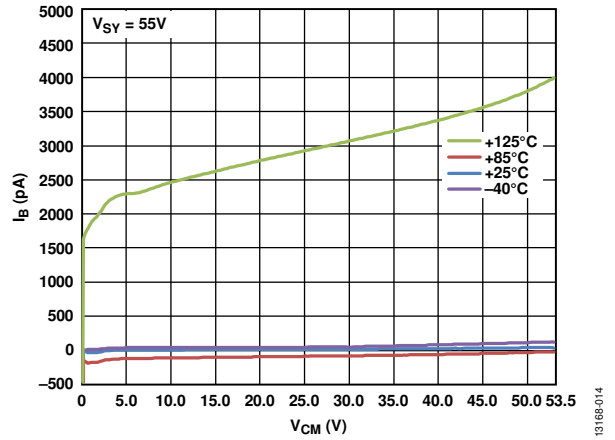


Figure 17. Input Bias Current (I_B) vs. Common-Mode Voltage (V_{CM}), $V_{SY} = 55V$

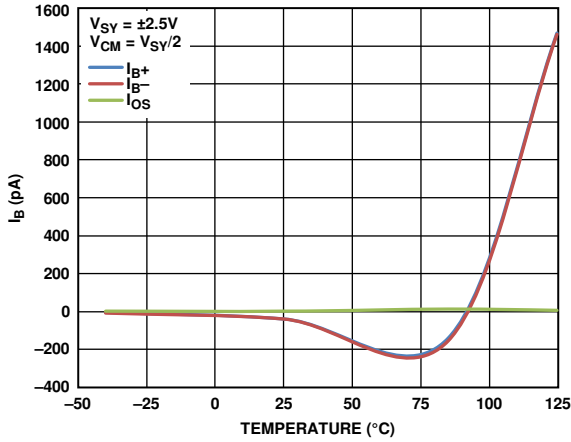


Figure 18. Input Bias Current (I_B) vs. Temperature, $V_{SY} = \pm 2.5V$

13168-015

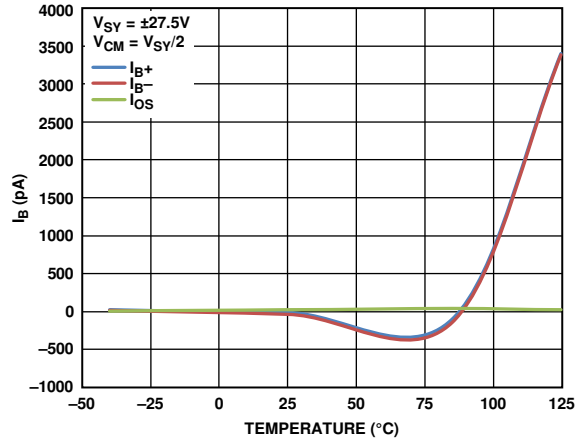


Figure 21. Input Bias Current (I_B) vs. Temperature, $V_{SY} = \pm 27.5V$

13168-016

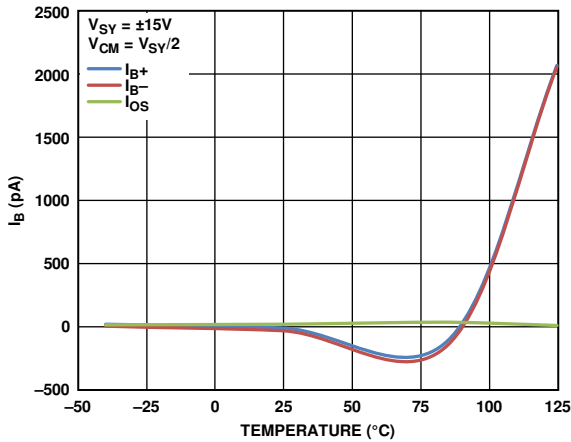


Figure 19. Input Bias Current (I_B) vs. Temperature, $V_{SY} = \pm 15V$

13168-017

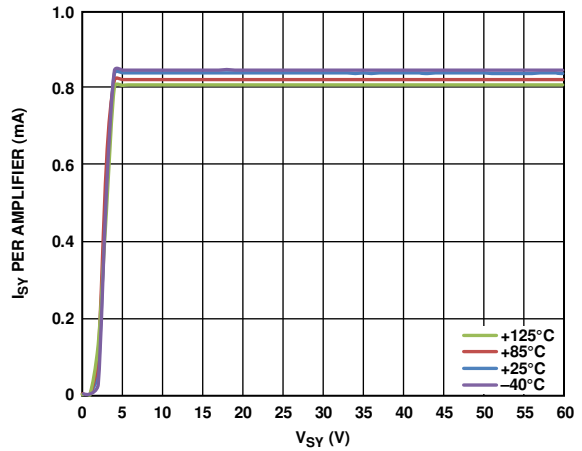


Figure 22. Supply Current (I_{SY}) per Amplifier vs. Supply Voltage (V_{SY})

13168-025

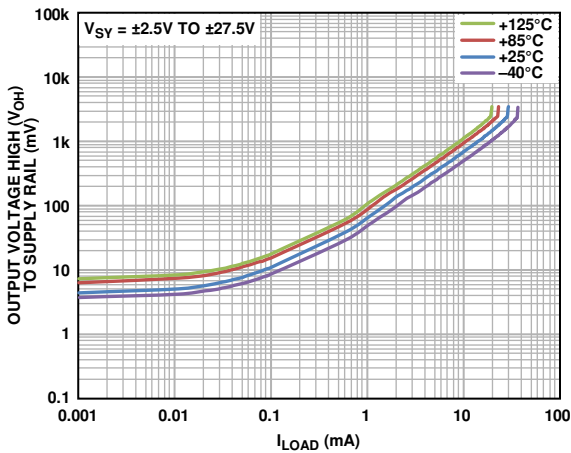


Figure 20. Output Voltage High (V_{OH}) to Supply Rail vs. Load Current (I_{LOAD})

13168-024

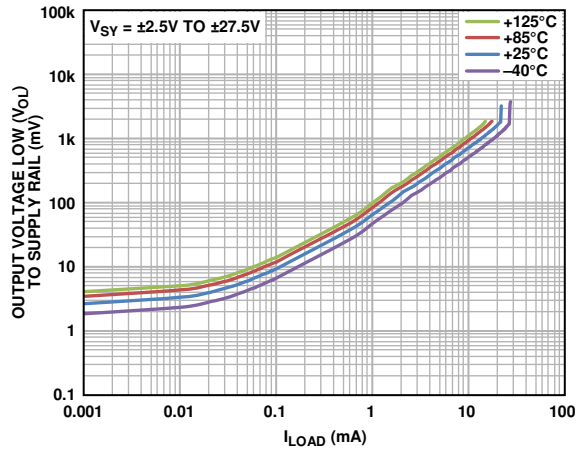


Figure 23. Output Voltage Low (V_{OL}) to Supply Rail vs. Load Current (I_{LOAD})

13168-027

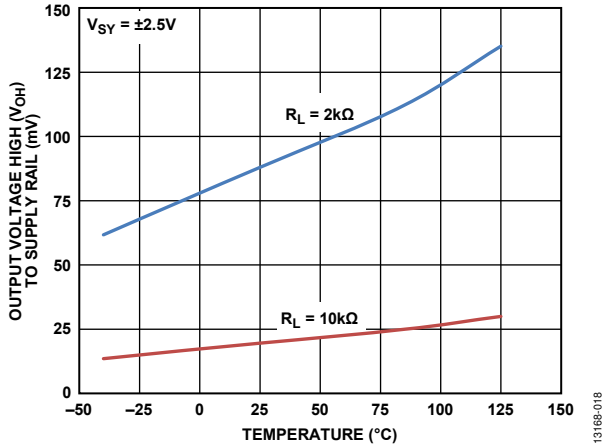


Figure 24. Output Voltage High (V_{OH}) to Supply Rail vs. Temperature, $V_{SY} = \pm 2.5V$

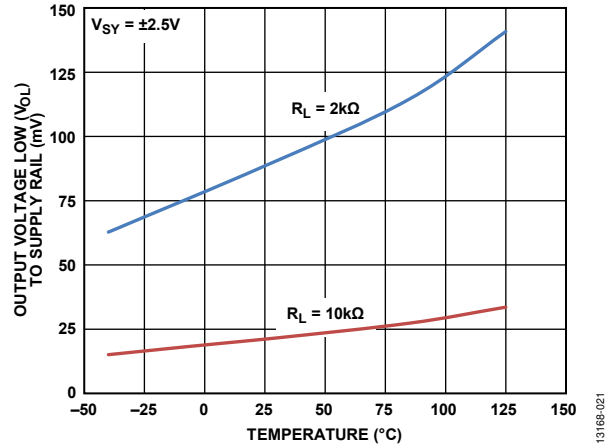


Figure 27. Output Voltage Low (V_{OL}) to Supply Rail vs. Temperature, $V_{SY} = \pm 2.5V$

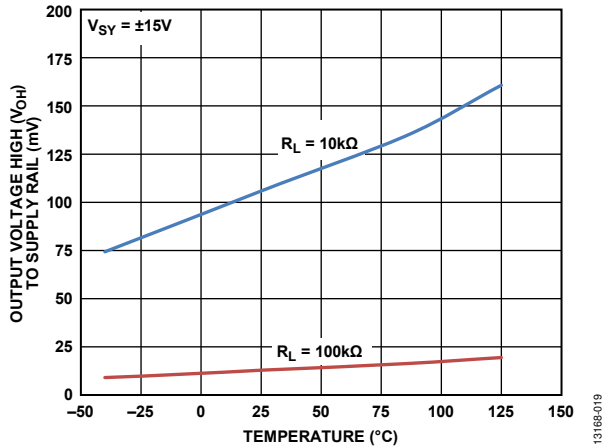


Figure 25. Output Voltage High (V_{OH}) to Supply Rail vs. Temperature, $V_{SY} = \pm 15V$

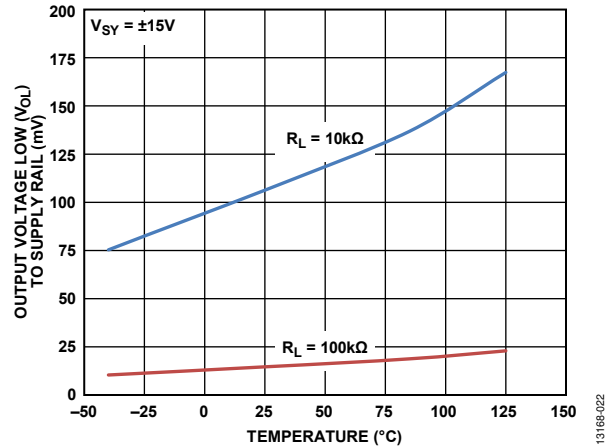


Figure 28. Output Voltage Low (V_{OL}) to Supply Rail vs. Temperature, $V_{SY} = \pm 15V$

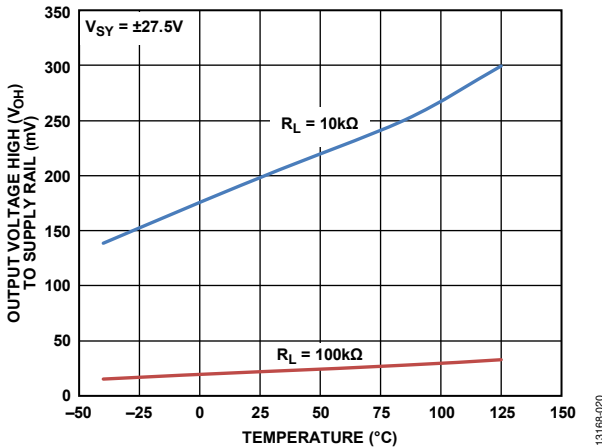


Figure 26. Output Voltage High (V_{OH}) to Supply Rail vs. Temperature, $V_{SY} = \pm 27.5V$

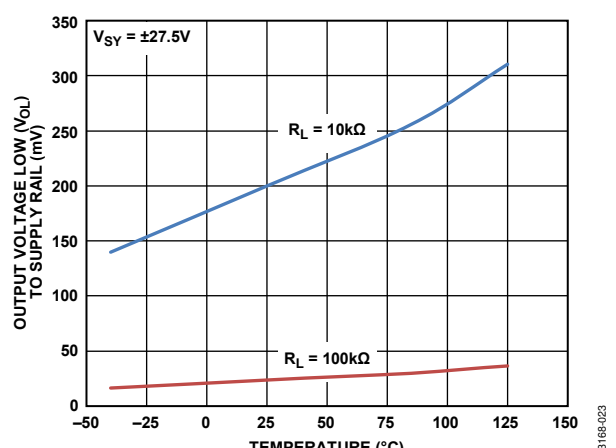


Figure 29. Output Voltage Low (V_{OL}) to Supply Rail vs. Temperature, $V_{SY} = \pm 27.5V$

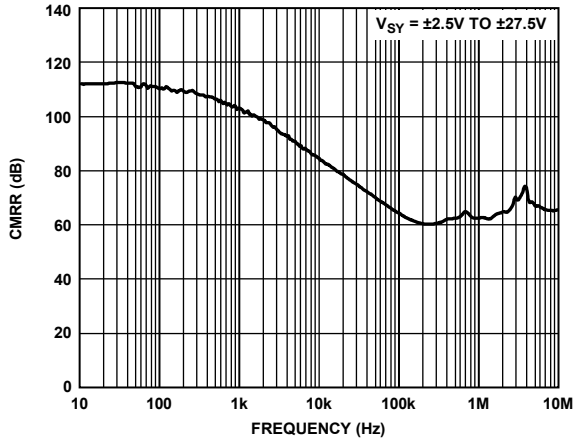


Figure 30. CMRR vs. Frequency

13168-030

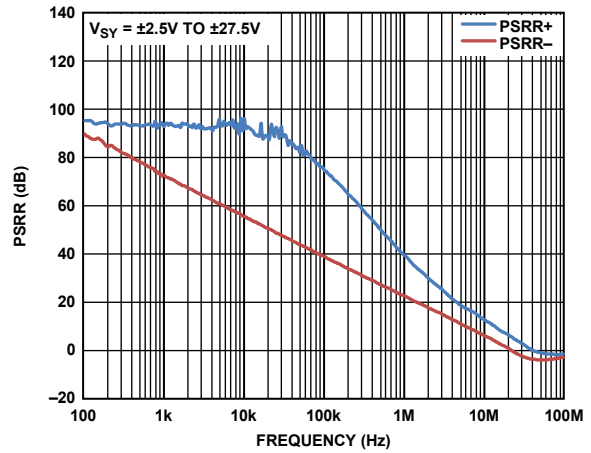


Figure 33. PSRR vs. Frequency

13168-032

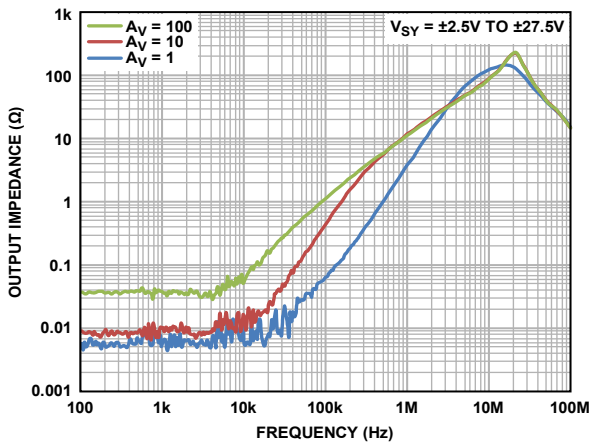


Figure 31. Closed-Loop Output Impedance vs. Frequency

13168-031

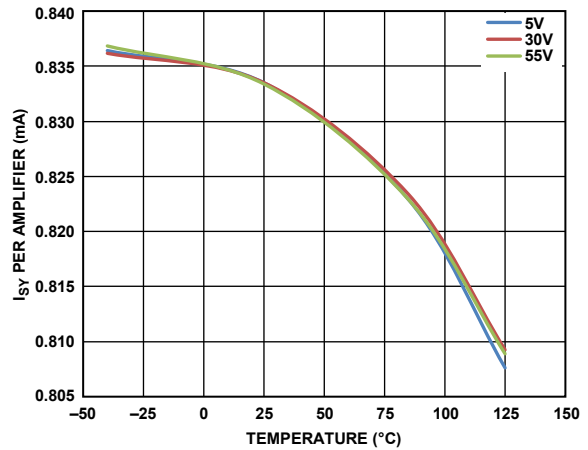


Figure 34. Supply Current (I_{SY}) per Amplifier vs. Temperature

13168-028

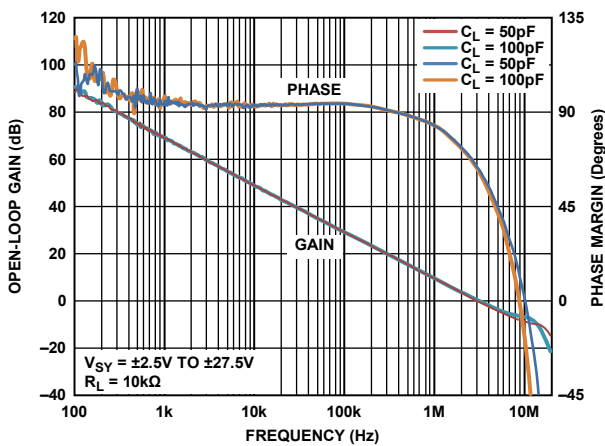


Figure 32. Open-Loop Gain and Phase Margin vs. Frequency

13168-026

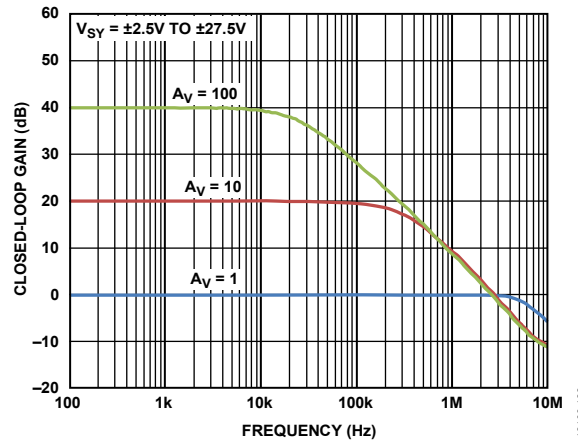


Figure 35. Closed-Loop Gain vs. Frequency

13168-133

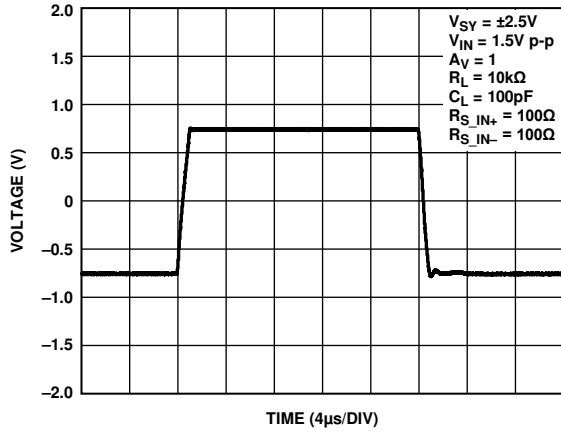


Figure 36. Large Signal Transient Response, $V_{SY} = \pm 2.5 V$

13168-034

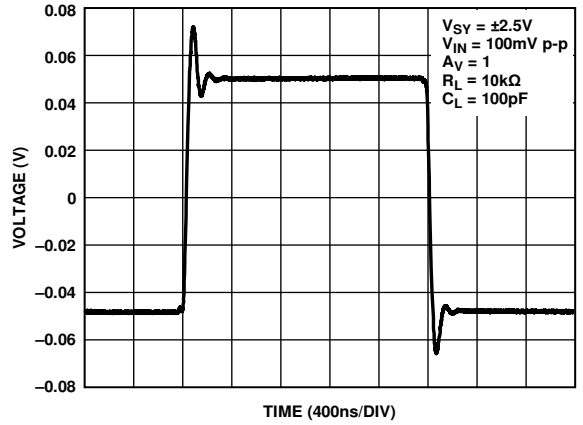


Figure 39. Small Signal Transient Response, $V_{SY} = \pm 2.5 V$

13168-037

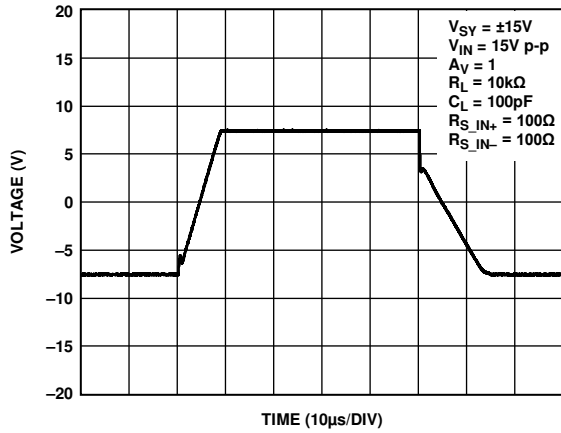


Figure 37. Large Signal Transient Response, $V_{SY} = \pm 15 V$

13168-035

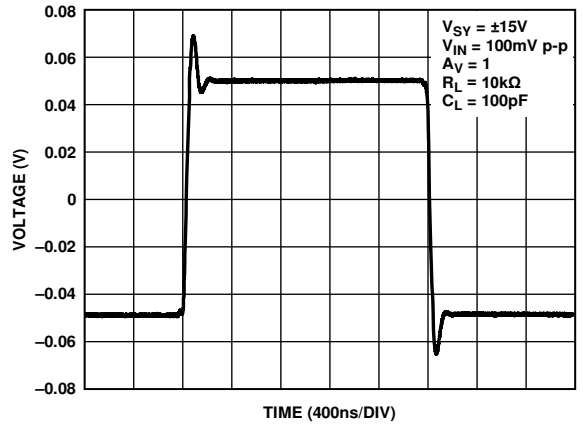


Figure 40. Small Signal Transient Response, $V_{SY} = \pm 15 V$

13168-038

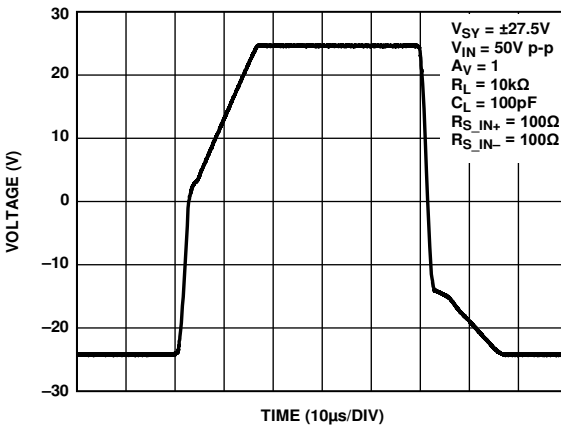


Figure 38. Large Signal Transient Response, $V_{SY} = \pm 27.5 V$

13168-036

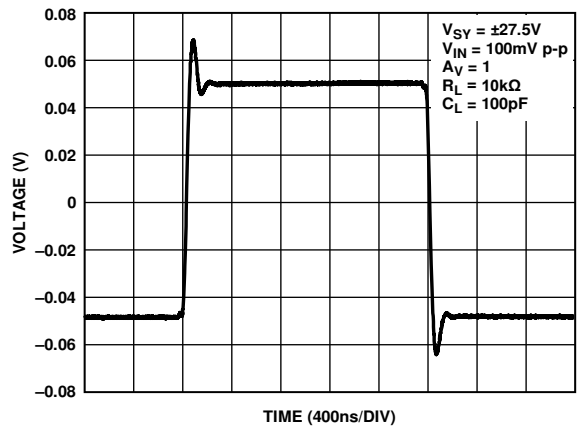


Figure 41. Small Signal Transient Response, $V_{SY} = \pm 27.5 V$

13168-039

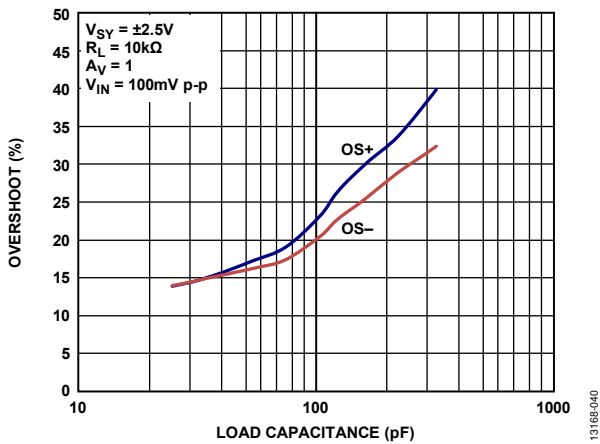


Figure 42. Small Signal Overshoot vs. Load Capacitance, $V_{SY} = \pm 2.5 V$

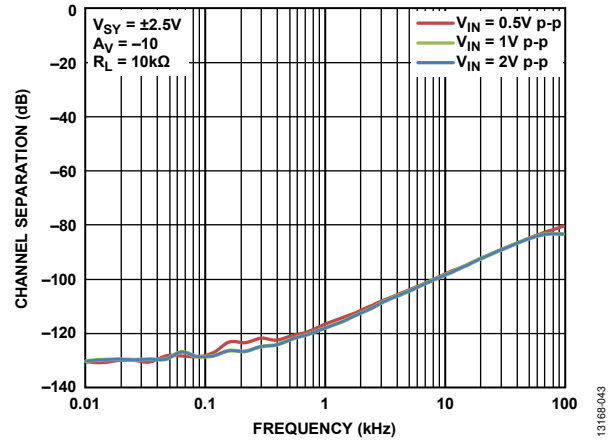


Figure 45. Channel Separation vs. Frequency, $V_{SY} = \pm 2.5 V$

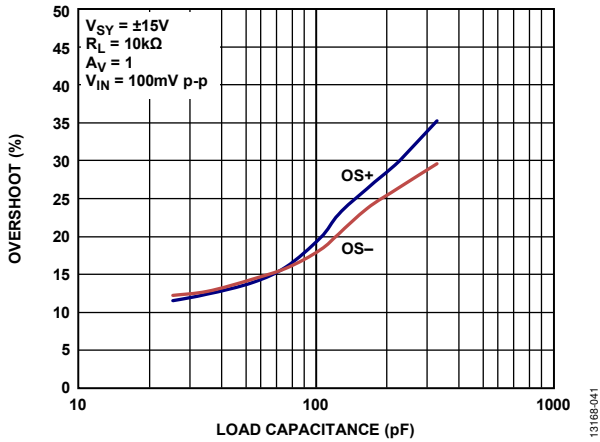


Figure 43. Small Signal Overshoot vs. Load Capacitance, $V_{SY} = \pm 15 V$

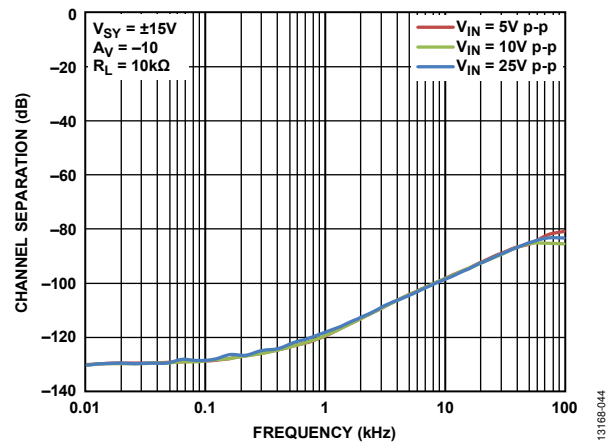


Figure 46. Channel Separation vs. Frequency, $V_{SY} = \pm 15 V$

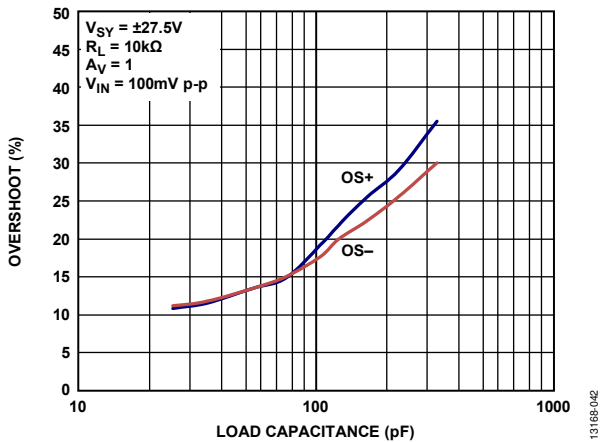


Figure 44. Small Signal Overshoot vs. Load Capacitance, $V_{SY} = \pm 27.5 V$

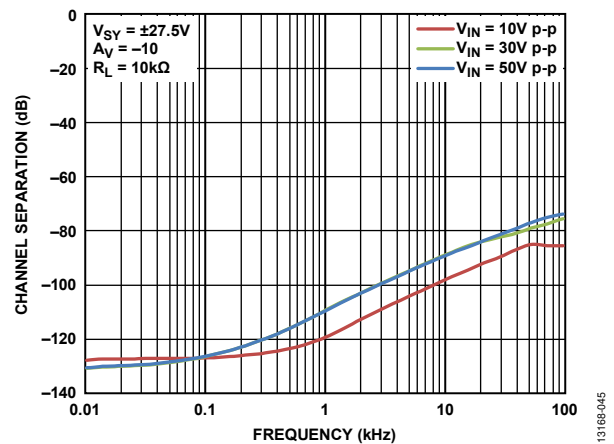


Figure 47. Channel Separation vs. Frequency, $V_{SY} = \pm 27.5 V$

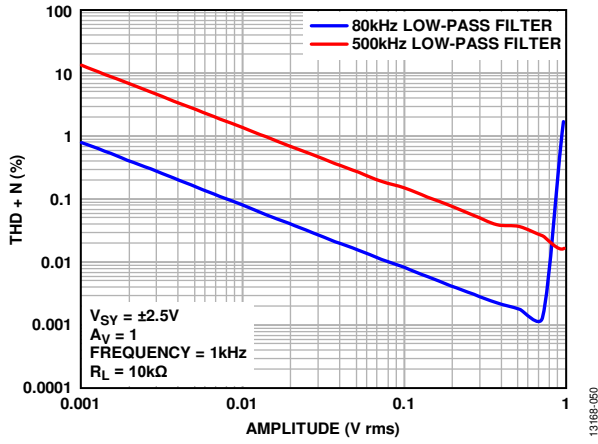


Figure 48. THD + N vs. Amplitude, $V_{SY} = \pm 2.5 V$

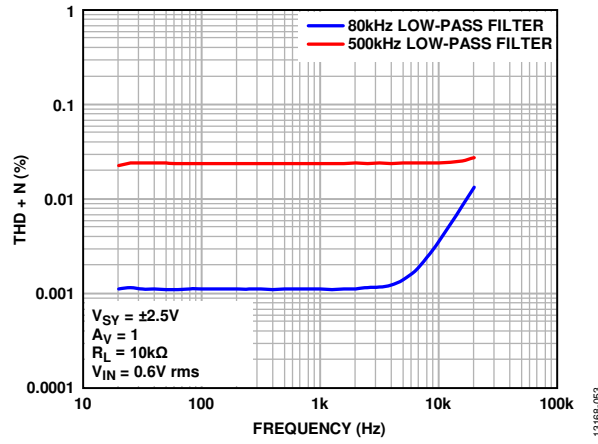


Figure 51. THD + N vs. Frequency, $V_{SY} = \pm 2.5 V$

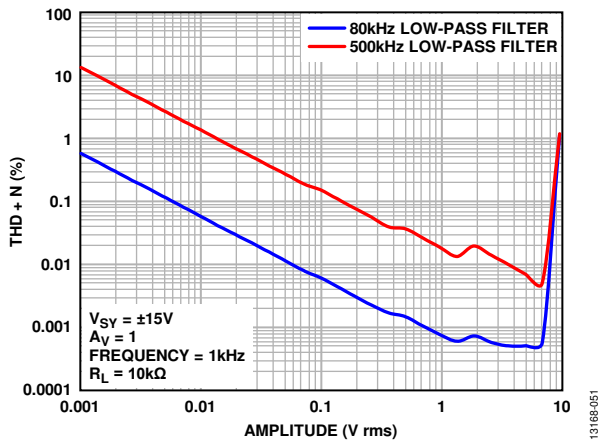


Figure 49. THD + N vs. Amplitude, $V_{SY} = \pm 15 V$

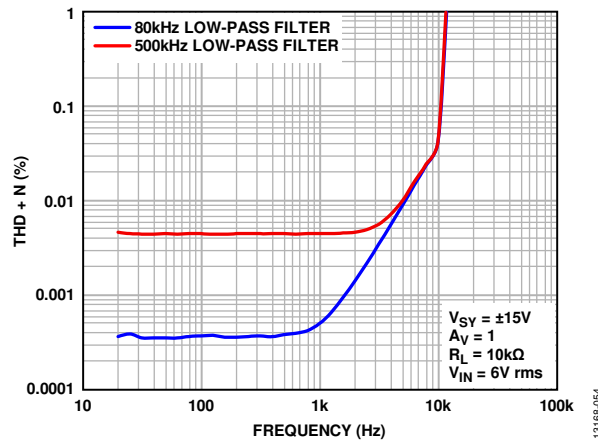


Figure 52. THD + N vs. Frequency, $V_{SY} = \pm 15 V$

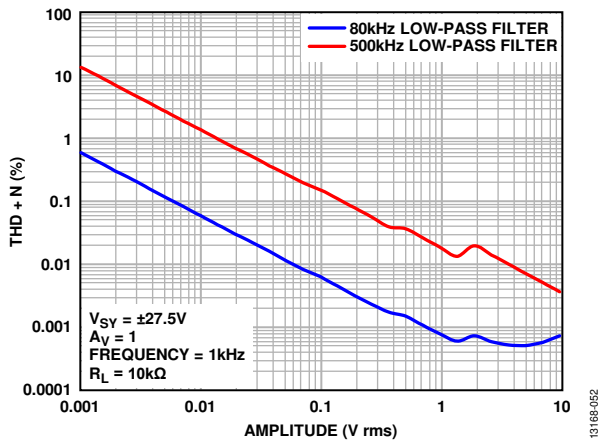


Figure 50. THD + N vs. Amplitude, $V_{SY} = \pm 27.5 V$

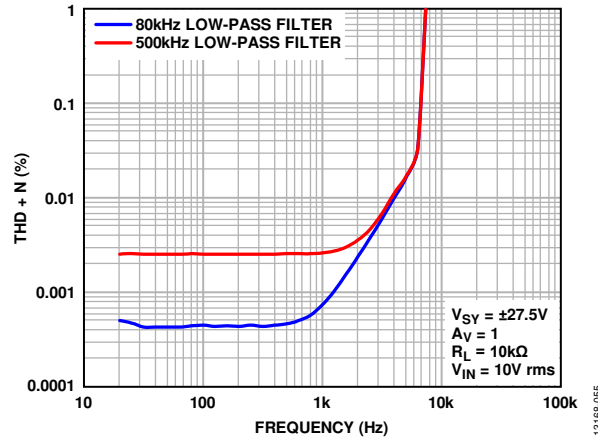


Figure 53. THD + N vs. Frequency, $V_{SY} = \pm 27.5 V$

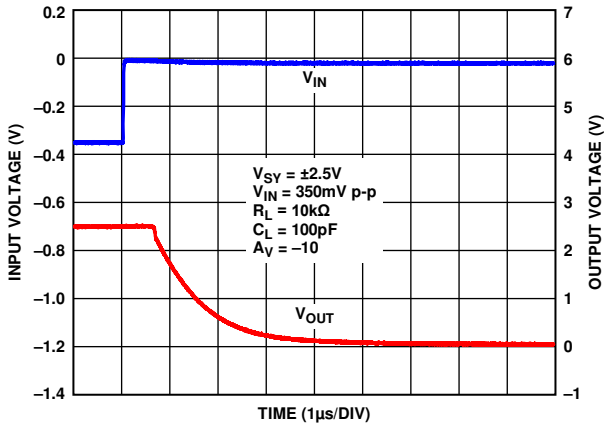


Figure 54. Positive Overload Recovery, $V_{SY} = \pm 2.5\text{ V}$

13168-056

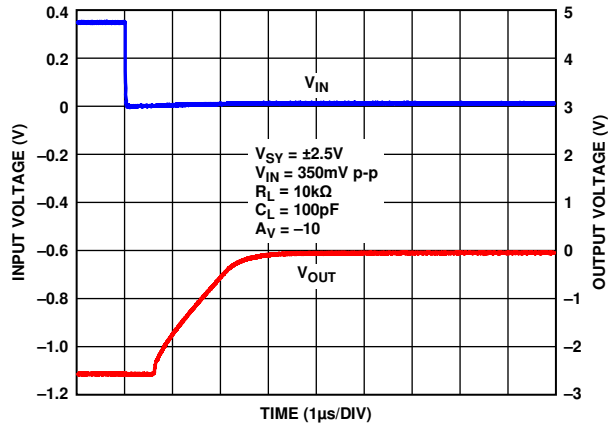


Figure 57. Negative Overload Recovery, $V_{SY} = \pm 2.5\text{ V}$

13168-059

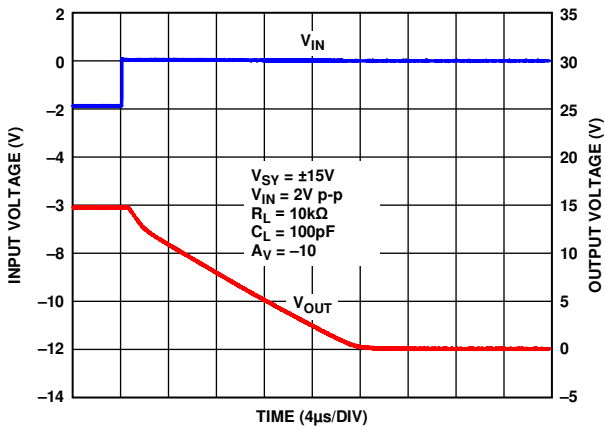


Figure 55. Positive Overload Recovery, $V_{SY} = \pm 15\text{ V}$

13168-057

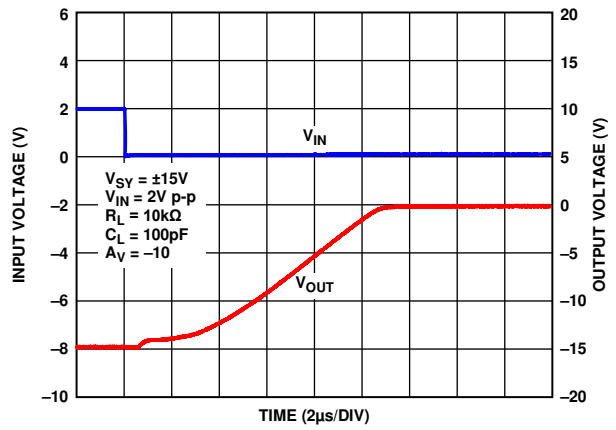


Figure 58. Negative Overload Recovery, $V_{SY} = \pm 15\text{ V}$

13168-060

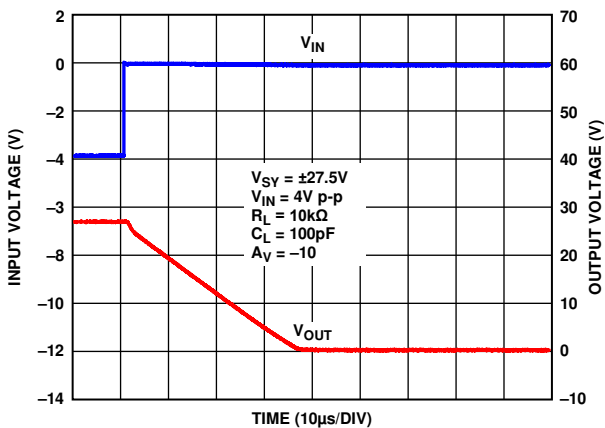


Figure 56. Positive Overload Recovery, $V_{SY} = \pm 27.5\text{ V}$

13168-058

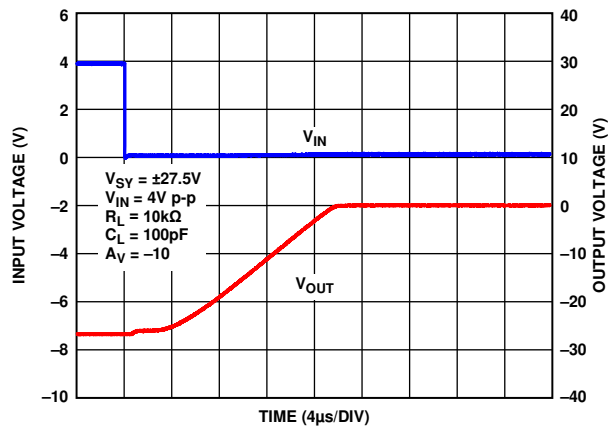


Figure 59. Negative Overload Recovery, $V_{SY} = \pm 27.5\text{ V}$

13168-061

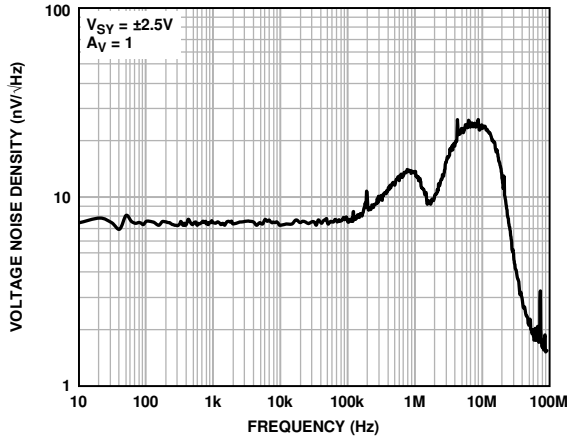


Figure 60. Voltage Noise Density vs. Frequency, $V_{SY} = \pm 2.5V$

13168-062

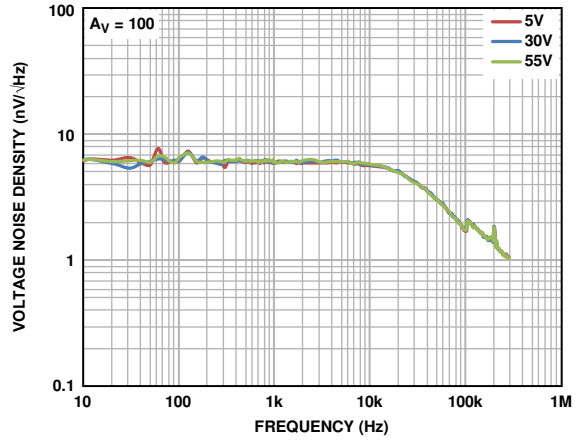


Figure 63. Voltage Noise Density vs. Frequency, $A_V = 100$

13168-065

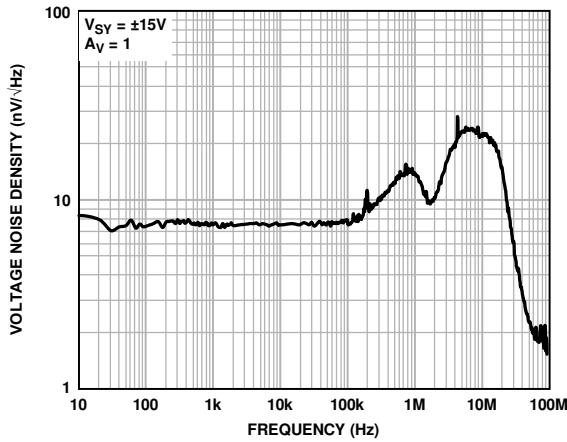


Figure 61. Voltage Noise Density vs. Frequency, $V_{SY} = \pm 15V$

13168-063

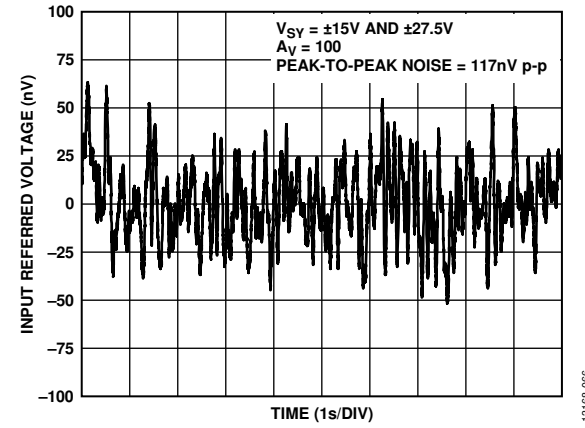


Figure 64. 0.1 Hz to 10 Hz Noise

13168-066

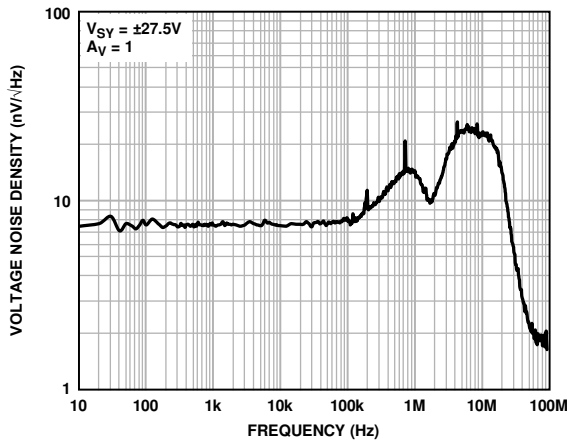


Figure 62. Voltage Noise Density vs. Frequency, $V_{SY} = \pm 27.5V$

13168-064

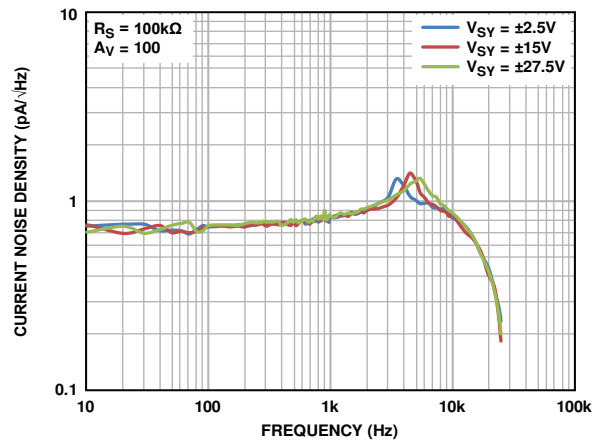


Figure 65. Current Noise Density vs. Frequency

13168-067

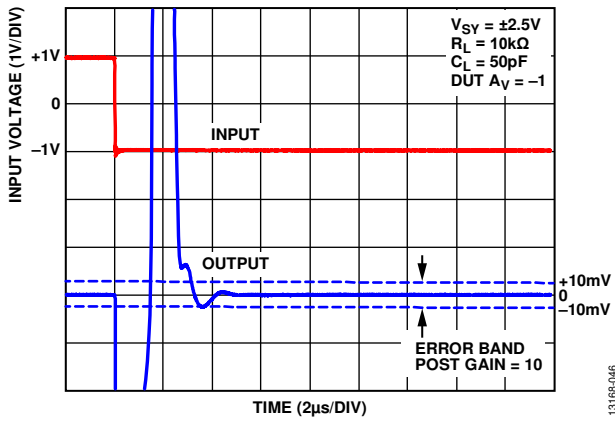


Figure 66. Negative Settling Time to 0.1%, $V_{SY} = \pm 2.5 V$

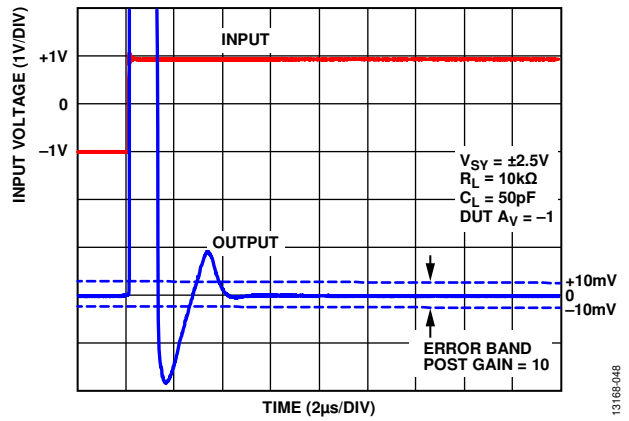


Figure 69. Positive Settling Time to 0.1%, $V_{SY} = \pm 2.5 V$

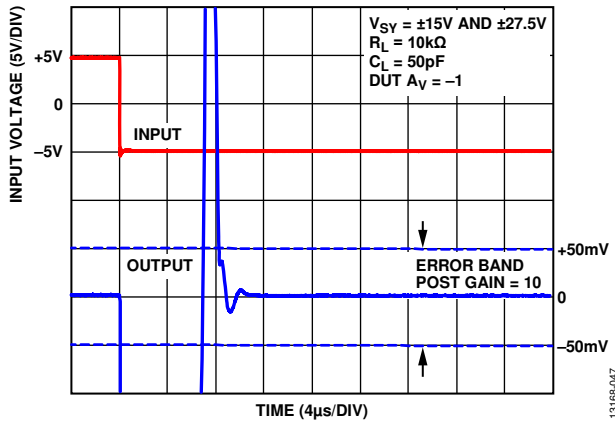


Figure 67. Negative Settling Time to 0.1%, $V_{SY} = \pm 15 V$ and $\pm 27.5 V$

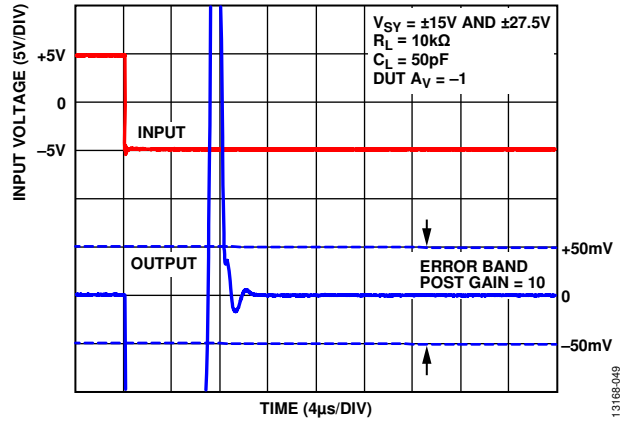


Figure 70. Positive Settling Time to 0.1%, $V_{SY} = \pm 15 V$ and $\pm 27.5 V$

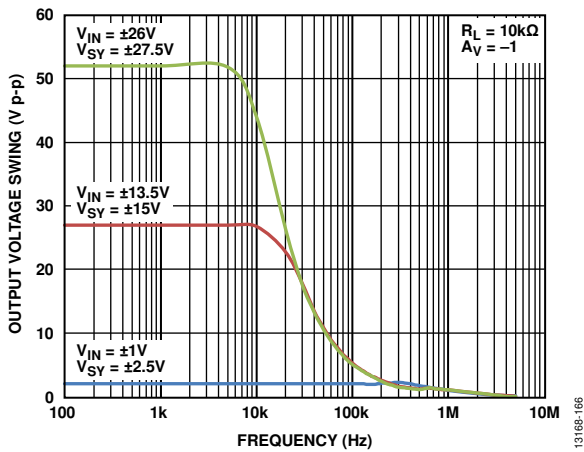


Figure 68. Output Voltage Swing vs. Frequency

THEORY OF OPERATION

The ADA4522-1/ADA4522-2/ADA4522-4 are single, dual, and quad, ultralow noise, high voltage, zero drift, rail-to-rail output operational amplifiers. They feature a chopping technique that offers an ultralow input offset voltage of 5 μV and an input offset voltage drift of 22 $\text{nV}/^\circ\text{C}$ maximum for the ADA4522-1 and ADA4522-2 and 25 $\text{nV}/^\circ\text{C}$ maximum for the ADA4522-4. Offset voltage errors due to common-mode voltage swings and power supply variations are also corrected by the chopping technique, resulting in a superb typical CMRR figure of 160 dB and a PSRR figure of 160 dB at a 30 V supply voltage.

The ADA4522-1/ADA4522-2/ADA4522-4 have wide operating voltages from $\pm 2.25\text{ V}$ (or 4.5 V) to $\pm 27.5\text{ V}$ (or 55 V). The devices are single supply amplifiers, where their input voltage range includes the lower supply rail. They also offer low voltage noise density of 5.8 $\text{nV}/\sqrt{\text{Hz}}$ (at $f = 1\text{ kHz}$, $A_V = 100$) and reduced $1/f$ noise component. These features are ideal for the amplification of low level signals in high precision applications. A few examples of such applications are weigh scales, high precision current sensing, high voltage buffers, and signal conditioning for temperature sensors, among others.

Figure 71 shows the ADA4522-1/ADA4522-2/ADA4522-4 architecture block diagram. The architecture consists of an input EMI filter and clamp circuitry, three gain stages (G_{m1} , G_{m2} , and G_{m3}), input and output chopping networks (CHOP_{IN} and

CHOP_{OUT}), a clock generator, offset and ripple correction loop circuitry, frequency compensation capacitors (C1, C2, and C3), and thermal shutdown circuitry.

An EMI filter and clamp circuit is implemented at the input front end to protect the internal circuitry against electrostatic discharge (ESD) stresses and high voltage transients. The ability of the amplifier to reject EMI is explained in detail in the EMI Rejection Ratio section.

CHOP_{IN} and CHOP_{OUT} are controlled by a clock generator and operate at 4.8 MHz. The input baseband signal is initially modulated by CHOP_{IN}. Next, CHOP_{OUT} demodulates the input signal and modulates the millivolt level input offset voltage and $1/f$ noise of the input transconductance amplifier, G_{m1} , to the chopping frequency at 4.8 MHz. The chopping networks remove the low frequency errors, but, in return, the networks introduce chopping artifacts at the chopping frequency. Therefore, an offset and ripple correction loop, operating at 800 kHz, is used. This frequency is the switching frequency of the amplifier. This circuitry reduces chopping artifacts, allowing the ADA4522-1/ADA4522-2/ADA4522-4 to have a high chopping frequency with minimal artifacts.

The thermal shutdown circuit shuts down the circuit when the die is overheated (see the Thermal Shutdown section for more information).

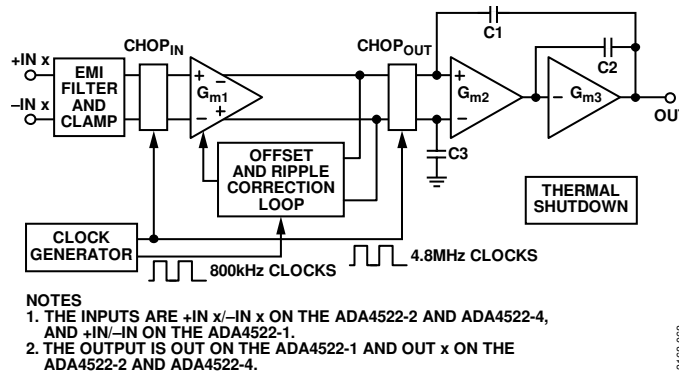


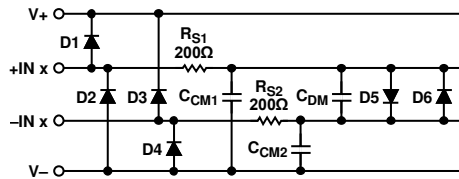
Figure 71. ADA4522-1/ADA4522-2/ADA4522-4 Architecture Block Diagram

ON-CHIP INPUT EMI FILTER AND CLAMP CIRCUIT

Figure 72 shows the input EMI filter and clamp circuit. The ADA4522-1/ADA4522-2/ADA4522-4 have internal ESD protection diodes (D1, D2, D3, and D4) that are connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse biased during normal operation. This protection scheme allows voltages as high as approximately 300 mV beyond the rails to be applied at the input of either terminal without causing permanent damage. See Table 5 in the Absolute Maximum Ratings section for more information.

The EMI filter is composed of two 200 Ω input series resistors (R_{S1} and R_{S2}), two common-mode capacitors (C_{CM1} and C_{CM2}), and a differential capacitor (C_{DM}). These RC networks set the -3 dB low-pass cutoff frequencies at 50 MHz for common-mode signals, and at 33 MHz for differential signals. After the EMI filter, back to back diodes (D5 and D6) are added to protect internal circuit devices from high voltage input transients. Each diode has about 1 V of forward turn on voltage. See the Large Signal Transient Response section for more information on the effect of high voltage input transient on the ADA4522-1/ADA4522-2/ADA4522-4.

As specified in the Absolute Maximum Ratings section (see Table 5), the maximum input differential voltage is limited to ±5 V. If more than ±5 V is applied, a continuous current larger than ±10 mA flows through one of the back to back diodes. This current compromises long-term reliability and can cause permanent damage to the device.



NOTES
 1. THE INPUTS ARE +IN x/-IN x ON THE ADA4522-2 AND ADA4522-4, AND +IN/-IN ON THE ADA4522-1.

Figure 72. Input EMI Filter and Clamp Circuit

THERMAL SHUTDOWN

The ADA4522-1/ADA4522-2/ADA4522-4 have internal thermal shutdown circuitry for each channel of the amplifier. The thermal shutdown circuitry prevents internal devices from being damaged by an overheat condition in the die. Overheating can occur due to a high ambient temperature, a high supply voltage, and/or high output currents. As specified in Table 5, take care to maintain the junction temperature below 150°C.

Two conditions affect junction temperature (T_J): the total power dissipation of the device (P_D) and the ambient temperature surrounding the package (T_A). Use the following equation to estimate the approximate junction temperature:

$$T_J = P_D \times \theta_{JA} + T_A \tag{1}$$

where θ_{JA} is the thermal resistance between the die and the ambient environment, as shown in Table 6.

The total power dissipation is the sum of quiescent power of the device and the power required to drive a load for all channels of an amplifier. The power dissipation per amplifier (P_{D,PER_AMP}) for sourcing a load is shown in Equation 2.

$$P_{D,PER_AMP} = (V_{SY+} - V_{SY-}) \times I_{SY_PER_AMP} + I_{OUT} \times (V_{SY+} - V_{OUT}) \tag{2}$$

When sinking current, replace (V_{SY+} - V_{OUT}) in Equation 2 with (V_{OUT} - V_{SY-}).

Also, take note to include the power dissipation of all channels of the amplifier when calculating the total power dissipation for the ADA4522-1/ADA4522-2/ADA4522-4.

The thermal shutdown circuitry does not guarantee the device to be free of permanent damage if the junction temperature exceeds 150°C. However, the internal thermal shutdown function may help avoid permanent damage or reduce the degree of damage. Each amplifier channel has thermal shutdown circuitry, composed of a temperature sensor with hysteresis.

As soon as the junction temperature reaches 190°C, the thermal shutdown circuitry shuts down the amplifier. Note that either one of the two thermal shutdown circuitries is activated; this activation disables the channel. When the amplifier is disabled, the output becomes open state and the quiescent current of the channel decreases to 0.1 mA. When the junction temperature cools down to 160°C, the thermal shutdown circuitry enables the amplifier and the quiescent current increases to its typical value.

When overheating in the die is caused by an undesirable excess amount of output current, the thermal shutdown circuit repeats its function. The junction temperature keeps increasing until it reaches 190°C and one of the channels is disabled. Then, the junction temperature cools down until it reaches 160°C, and the channel is enabled again. The process then repeats.

INPUT PROTECTION

When either input of the ADA4522-1/ADA4522-2/ADA4522-4 exceeds one of the supply rails by more than 300 mV, the ESD diodes mentioned in the On-Chip Input EMI Filter and Clamp Circuit section become forward-biased and large amounts of current begin to flow through them. Without current limiting, this excessive fault current causes permanent damage to the device. If the inputs are expected to be subject to overvoltage conditions, insert a resistor in series with each input to limit the input current to ±10 mA maximum. However, consider the resistor thermal noise effect on the entire circuit.

At a ±15 V supply voltage, the broadband voltage noise of the ADA4522-1/ADA4522-2/ADA4522-4 is approximately 5.8 nV/√Hz (at unity gain), and a 1 kΩ resistor has a thermal noise of 4 nV/√Hz. Adding a 1 kΩ resistor increases the total noise to 7 nV/√Hz.

SINGLE-SUPPLY AND RAIL-TO-RAIL OUTPUT

The ADA4522-1/ADA4522-2/ADA4522-4 are single-supply amplifiers, where their input voltage range includes the lower supply rail. This feature is ideal for applications where the input common-mode voltage is at the lower supply rail, for example, ground sensing. Conversely, the amplifier output is rail to rail. Figure 73 shows the input and output waveforms of the ADA4522-1/ADA4522-2/ADA4522-4 configured as a unity-gain buffer with a supply voltage of ± 15 V. With an input voltage of ± 15 V, the low output voltage tracks the input voltage, whereas the high output swing clamps/distorts when the input goes out of the input voltage range ($-15 \text{ V} \leq \text{IVR} \leq +13.5 \text{ V}$). However, the device does not exhibit phase reversal.

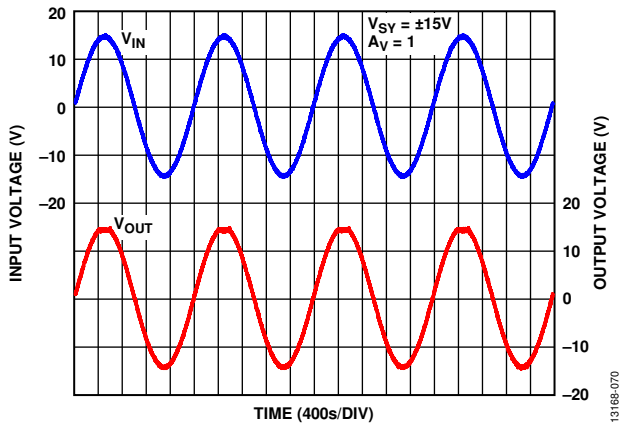


Figure 73. Input and Output Waveforms, No Phase Reversal

LARGE SIGNAL TRANSIENT RESPONSE

When the ADA4522-1/ADA4522-2/ADA4522-4 are configured in a closed-loop configuration with a large input transient (for example, a step input voltage), the internal back to back diodes may turn on. Consider a case where the amplifier is in unity-gain configuration with a step input waveform. This case is shown in Figure 74.

The noninverting input is driven by an input signal source and the inverting input is driven by the output of the amplifier. The maximum amplifier output current depends on the input step function and the external source resistance at the input terminals of the amplifier.

Case 1

If the external source resistance is low (for example, 100Ω in Figure 75) or if the input step function is large, the maximum amplifier output current is limited to the output short-circuit current as specified in the Specifications section. The maximum differential voltage between the input signal and the amplifier output is then limited by the maximum amplifier output current multiplied by the total input resistance (internal and external) and the turn-on voltage of the back to back diode (see Figure 72 for the input EMI filter and clamp circuit architecture).

When the noninverting input voltage changes with a step signal, the inverting input voltage (and, therefore, the output voltage) follows the change quickly until it reaches the maximum differen-

tial voltage between the input signal and amplifier output possible. The inverting input voltage then starts slewing with the slew rate specified in the Specifications section until it reaches its desired output. Therefore, as seen in Figure 74, there are two distinctive sections of the rising and falling edge of the output waveform. With this test condition, the amount and duration of the input/output current is limited and, therefore, does not damage the amplifier.

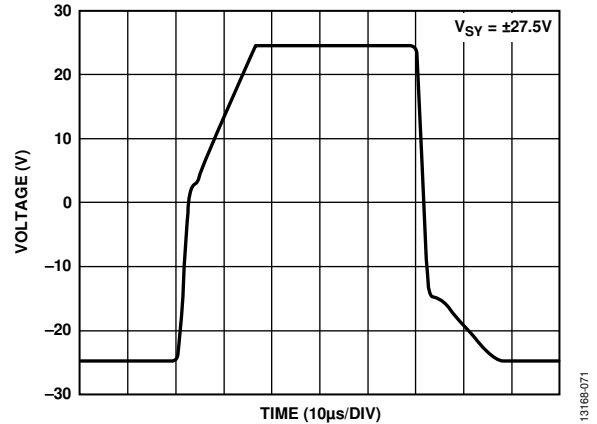


Figure 74. Large Signal Transient Response Example

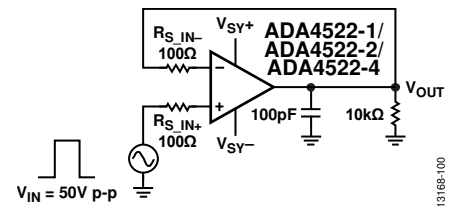


Figure 75. Circuit Diagram for Large Signal Transient Response

Case 2

If the external source resistance is high or if the input step function is small, the maximum output current is limited to the instantaneous difference between the input signal and amplifier output voltage (which is the change in the step function) divided by the source resistance. This maximum output current is less than the amplifier output short-circuit current. The maximum differential voltage between the input signal and the amplifier output is then equal to the step function. The output voltage slews until it reaches its desired output.

Therefore, if desired, reduce the input current by adding a larger external resistor between the signal source and the noninverting input. Similarly, to reduce output current, add an external resistor to the feedback loop between the inverting input and output. This large signal transient response issue is typically not a problem when the amplifier is configured in closed-loop gain, where the input signal source is usually much smaller and the gain and feedback resistors limit the current.

Back to back diodes are also implemented in many other amplifiers; these amplifiers show similar slewing behavior.

NOISE CONSIDERATIONS

1/f Noise

1/f noise, also known as pink noise or flicker noise, is inherent in semiconductor devices and increases as frequency decreases. At a low frequency, 1/f noise is a major noise contributor and causes a significant output voltage offset when amplified by the noise gain of the circuit. However, because the low frequency 1/f noise appears as a slow varying offset to the ADA4522-1/ADA4522-2/ADA4522-4, it is effectively reduced by the chopping technique. This technique allows the ADA4522-1/ADA4522-2/ADA4522-4 to have a much lower noise at dc and low frequency in comparison to standard low noise amplifiers that are susceptible to 1/f noise. Figure 64 shows the 0.1 Hz to 10 Hz noise to be only 117 nV p-p of noise.

Source Resistance

The ADA4522-1/ADA4522-2/ADA4522-4 are some of the lowest noise high voltage zero drift amplifiers with 5.8 nV/√Hz of voltage noise density at 1 kHz (A_v = 100). Therefore, it is important to consider the input source resistance of choice to maintain a total low noise. The total input referred broadband noise (e_{N total}) from any amplifier is primarily a function of three types of noise: input voltage noise, input current noise, and thermal (Johnson) noise from the external resistors.

These uncorrelated noise sources can be summed up in a root sum squared (rss) manner by using the following equation:

$$e_{N \text{ total}} = (e_N^2 + 4kTR_S + (i_N \times R_S)^2)^{1/2}$$

where:

e_N is the input voltage noise density of the amplifier (V/√Hz).

k is Boltzmann's constant (1.38 × 10⁻²³ J/K).

T is the temperature in Kelvin (K).

R_S is the total input source resistance (Ω).

i_N is the input current noise density of the amplifier (A/√Hz).

The total equivalent rms noise over a specific bandwidth is expressed as

$$e_{N \text{ RMS}} = e_{N \text{ total}} \sqrt{BW}$$

where BW is the bandwidth in hertz.

This analysis is valid for broadband noise calculation up to a decade before the switching frequency. If the bandwidth of concern includes the switching frequency, more complicated calculations must be made to include the effect of the increase in noise at the switching frequency.

With a low source resistance of R_S < 1 kΩ, the voltage noise of the amplifier dominates. As the source resistance increases, the thermal noise of R_S dominates. As the source resistance further increases, where R_S > 50 kΩ, the current noise becomes the main contributor of the total input noise.

Residual Ripple

As shown in Figure 60, Figure 61, and Figure 62, the ADA4522-1/ADA4522-2/ADA4522-4 have a flat noise spectrum density at lower frequencies and exhibits spectrum density bumps and peaks at higher frequencies.

The largest noise bump is centered at 6 MHz; this bump is due to the decrease in the input gain at higher frequencies. This decrease is a typical phenomenon and can also be seen in other amplifiers. In addition to the noise bump, a sharp peak due to the chopping networks is seen at 4.8 MHz. However, this magnitude is significantly reduced by the offset and ripple correction loop. Its magnitude may be different with different amplifier units or with different circuitries around the amplifier. This peak can potentially be hidden by the noise bump and, therefore, may not be detected.

The offset and ripple correction loop, designed to reduce the 4.8 MHz switching artifact, also creates a noise bump centered at 800 kHz and a noise peak on top of this noise bump. Although the magnitude of the bump is mostly constant, the magnitude of the 800 kHz peak is different from unit to unit. Some units may not exhibit the 800 kHz noise peak; however, for other units, peaks occur at multiple integrals of 800 kHz, such as 1.6 MHz or 2.4 MHz.

These noise peaks, albeit small in magnitude, can be significant when the amplifier has a closed-loop frequency that is higher than the chopping frequency. To suppress the noise spike to a desired level, either configure the amplifier in a high gain configuration or apply a post filter at the output of the amplifier.

Figure 76 shows the voltage noise density of the ADA4522-1/ADA4522-2/ADA4522-4 in various gain configurations. Note that the higher the gain, the lower the available bandwidth is. The earlier bandwidth roll-off effectively filters out the higher noise spectrum.

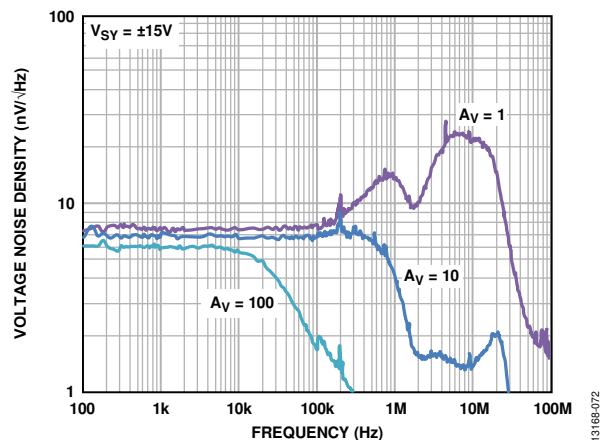


Figure 76. Voltage Noise Density with Various Gains

Figure 77 shows the voltage noise density of the ADA4522-1/ADA4522-2/ADA4522-4 without and with post filters at different frequencies. The post filter serves to roll off the bandwidth before the switching frequency. In this example, the noise peak at 800 kHz is about 38 nV/√Hz. With a post filter at 80 kHz, the noise peak is reduced to 4.1 nV/√Hz. With a post filter at 8 kHz, the noise peak is lower than the noise floor and cannot be detected.

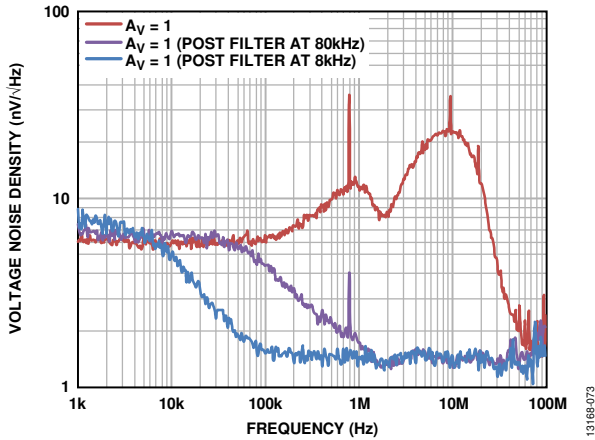


Figure 77. Voltage Noise Density with Post Filters

Current Noise Density

Figure 78 shows the current noise density of the ADA4522-1/ADA4522-2/ADA4522-4 at unity gain. At 1 kHz, the current noise density is about 1.3 pA/√Hz. The current noise density is determined by measuring the voltage noise due to current noise flowing through a resistor. Due to the low current noise density of the amplifier, the voltage noise is usually measured with a high value resistor; in this case, a 100 kΩ source resistor is used. However, the source resistor interacts with the input capacitance of the amplifier and board, causing the bandwidth to roll off. Note that Figure 78 shows the current noise density rolling off much earlier than the unity-gain bandwidth; this roll-off is expected.

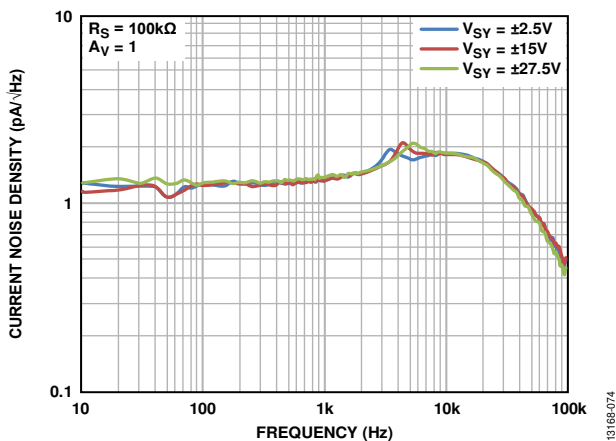


Figure 78. Current Noise Density at Gain = 1

EMI REJECTION RATIO

Circuit performance is often adversely affected by high frequency EMI. When the signal strength is low and transmission lines are long, an op amp must accurately amplify the input signals. However, all op amp pins—the noninverting input, inverting input, positive supply, negative supply, and output pins—are susceptible to EMI signals. These high frequency signals are coupled into an op amp by various means, such as conduction, near field radiation, or far field radiation. For example, wires and printed circuit board (PCB) traces can act as antennas and pick up high frequency EMI signals.

Amplifiers do not amplify EMI or RF signals due to their relatively low bandwidth. However, due to the nonlinearities of the input devices, op amps can rectify these out of band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

The ADA4522-1/ADA4522-2/ADA4522-4 have integrated EMI filters at their input stage. To describe the ability of the ADA4522-1/ADA4522-2/ADA4522-4 to perform as intended in the presence of electromagnetic energy, the electromagnetic interference rejection ratio (EMIRR) of the noninverting pin is specified in Table 2, Table 3, and Table 4 of the Specifications section. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20\log(V_{IN_PEAK}/\Delta V_{OS})$$

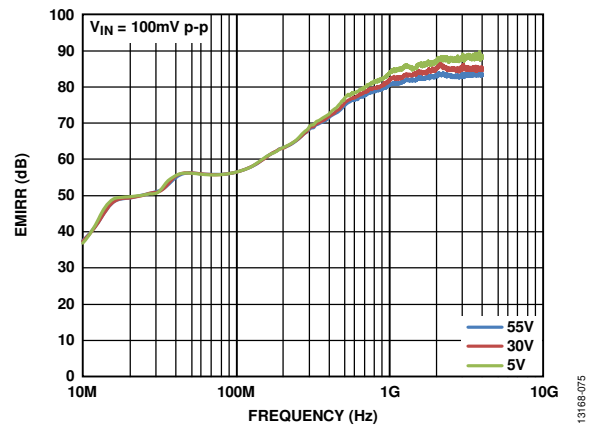


Figure 79. EMIRR vs. Frequency

CAPACITIVE LOAD STABILITY

The ADA4522-1/ADA4522-2/ADA4522-4 can safely drive capacitive loads of up to 250 pF in any configuration. As with most amplifiers, driving larger capacitive loads than specified may cause excessive overshoot and ringing, or even oscillation. A heavy capacitive load reduces the phase margin and causes the amplifier frequency response to peak. Peaking corresponds to overshooting or ringing in the time domain. Therefore, it is recommended that external compensation be used if the ADA4522-1/ADA4522-2/ADA4522-4 must drive a load exceeding 250 pF. This compensation is particularly important in the unity-gain configuration, which is the worst case for stability.