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30 V, 8 MHz, Low Bias Current, Single-Supply, RRO, Precision Op Amps

Data Sheet

ADA4622-1/ADA4622-2

FEATURES

Next generation of the AD820/AD822
Wide gain bandwidth product: 8 MHz typical
High slew rate: +23 V/μs/−18 V/μs typical
Low input bias current: ±10 pA maximum at T_A = 25°C
Low offset voltage
    A grade: ±0.8 mV maximum at T_A = 25°C
    B grade: ±0.35 mV maximum at T_A = 25°C
Low offset voltage drift
    A grade: ±2 μV/°C typical, ±15 μV/°C maximum
    B grade: ±2 μV/°C typical, ±5 μV/°C maximum
Input voltage range includes Pin V−
Rail-to-rail output
Electromagnetic interference rejection ratio (EMIRR)
    90 dB typical at f = 1000 MHz and f = 2400 MHz
Industry-standard package and pinouts

APPLICATIONS

High output impedance sensor interfaces
Photodiode sensor interfaces
Transimpedance amplifiers
ADC drivers
Precision filters and signal conditioning

GENERAL DESCRIPTION

The ADA4622-1/ADA4622-2 are the next generation of the AD820 and the AD822 single-supply, rail-to-rail output (RRO), precision junction field effect transistors (JFET) input op amps. The ADA4622-1/ADA4622-2 include many improvements that make them desirable as an upgrade without compromising the flexibility and ease of use that makes the AD820 and the AD822 useful for a wide variety of applications.

The input voltage range includes the negative supply and the output swings rail-to-rail. Input EMI filters increase the signal robustness in the face of closely located switching noise sources.

The speed, in terms of bandwidth and slew rate, increases along with a strong output drive to improve settling time performance and enable the devices to drive the inputs of modern single-ended, successive approximation register (SAR) analog-to-digital converters (ADCs).

PIN CONFIGURATIONS
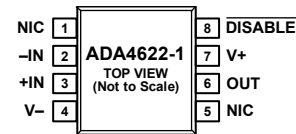
NOTES
1. NIC = NOT INTERNALLY CONNECTED.

Figure 1. 8-Lead SOIC Pin Configuration, ADA4622-1 (See the Pin Configurations and Function Descriptions Section for Additional Pin Configurations)
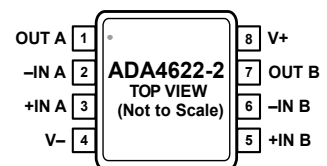

Figure 2. 8-Lead MSOP Pin Configuration, ADA4622-2 (See the Pin Configurations and Function Descriptions Section for Additional Pin Configurations)

Voltage noise is reduced; while keeping the supply current the same as the AD820 and the AD822, broadband noise is reduced by 25%, and 1/f is reduced by half. DC precision in the ADA4622-1/ADA4622-2 improved from the AD820 and the AD822 with half the offset and a maximum thermal drift specification added to the ADA4622-1/ADA4622-2. The common-mode rejection ratio (CMRR) is improved from the AD820 and the AD822 to make the ADA4622-1/ADA4622-2 more suitable when used in noninverting gain and difference amplifier configurations.

The ADA4622-1/ADA4622-2 are specified for operation over the extended industrial temperature range of −40°C to +125°C and operates from 5 V to 30 V with specifications at +5 V, ±5 V, and ±15 V. The ADA4622-1 is available in a 5-lead SOT-23 package and an 8-lead LFCSP package, and the ADA4622-2 is available in an 8-lead SOIC package, an 8-lead MSOP package, and an 8-lead LFCSP package.

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REVISION HISTORY

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS, V$_{SY}$ = ±15 V

Supply voltage (V$_{SY}$) = ±15 V, common-mode voltage (V$_{CM}$) = output voltage (V$_{OUT}$) = 0 V, T$_A$ = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V$_{OS}$					
A Grade				+0.04	±0.8	mV
		−40°C < T$_A$ < +125°C			±2	mV
B Grade				+0.04	±0.35	mV
ADA4622-1		−40°C < T$_A$ < +125°C			±1	mV
ADA4622-2		−40°C < T$_A$ < +125°C			±0.8	mV
Offset Voltage Match					±1	mV
Offset Voltage Drift	ΔV$_{OS}$/ΔT					
A Grade		−40°C < T$_A$ < +125°C		±2	±15	µV/°C
B Grade		−40°C < T$_A$ < +125°C		±2	±5	µV/°C
Input Bias Current	I$_B$			+2	±10	pA
		−40°C < T$_A$ < +125°C			±1.5	nA
		V$_{CM}$ = −15 V		−15		pA
Input Offset Current	I$_{OS}$				±10	pA
		−40°C < T$_A$ < +125°C			±0.5	nA
Input Voltage Range	IVR		−15.2		+14	V
Common-Mode Rejection Ratio	CMRR					
A Grade		V$_{CM}$ = −15 V to +12 V	84	100		dB
		−40°C < T$_A$ < +125°C	81			dB
B Grade		V$_{CM}$ = −15 V to +12 V	87	100		dB
		−40°C < T$_A$ < +125°C	85			dB
Large Signal Voltage Gain	A$_{VO}$	R$_L$ = 10 kΩ, V$_{OUT}$ = −14.5 V to +14.5 V	117	122		dB
		−40°C < T$_A$ < +125°C	109			dB
		R$_L$ = 1 kΩ, V$_{OUT}$ = −14 V to +14 V	102	110		dB
		−40°C < T$_A$ < +125°C	93			dB
Input Capacitance	C$_{INDM}$	Differential mode		0.4		pF
	C$_{INCM}$	Common mode		3.6		pF
Input Resistance	R$_{DIFF}$	Differential mode		10^{13}		Ω
	R$_{CM}$	Common mode		10^{13}		Ω
OUTPUT CHARACTERISTICS						
Output Voltage						
High	V$_{OH}$	I$_{SOURCE}$ = 1 mA	14.95	14.97		V
		−40°C < T$_A$ < +125°C	14.9			V
		I$_{SOURCE}$ = 15 mA	14.3	14.5		V
		−40°C < T$_A$ < +125°C	14.1			V
Low	V$_{OL}$	I$_{SINK}$ = 1 mA		−14.955	−14.935	V
		−40°C < T$_A$ < +125°C			−14.88	V
		I$_{SINK}$ = 15 mA		−14.685	−14.55	V
		−40°C < T$_A$ < +125°C			−14.25	V
Output Current	I$_{OUT}$	V$_{DROPOUT}$ < 1 V		20		mA
Short-Circuit Current	I$_{SC}$	Sourcing		42		mA
		Sinking		−51		mA
Closed-Loop Output Impedance	Z$_{OUT}$	f = 1 kHz, gain (A$_V$) = 1		0.1		Ω
		A$_V$ = 10		0.4		Ω
		A$_V$ = 100		3		Ω

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±4 V to ±18 V	87	103		dB
		−40°C < T_A < +125°C	81			dB
Supply Current per Amplifier	I_{SY}					
ADA4622-1				715	750	µA
		−40°C < T_A < +125°C			775	µA
ADA4622-2				665	700	µA
		−40°C < T_A < +125°C			725	µA
Shutdown Current		ADA4622-1 only		60		µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	V_{OUT} = ±12.5 V, R_L = 2 kΩ, load capacitor (C_L) = 100 pF, A_V = 1				
		Low to high transition		23		V/µs
		High to low transition		−18		V/µs
Gain Bandwidth Product	GBP	A_V = 100, C_L = 35 pF		8		MHz
Unity-Gain Crossover	UGC	A_V = 1		7		MHz
−3 dB Bandwidth	−3 dB	A_V = 1		15.5		MHz
Phase Margin	ΦM			53		Degrees
Settling Time	t_S	Input voltage (V_{IN}) = 10 V step, R_L = 2 kΩ, C_L = 15 pF, A_V = −1				
To 0.1%				1.5		µs
To 0.01%				2		µs
EMI REJECTION RATIO	EMIRR	V_{IN} = 100 mV p-p				
f = 1000 MHz				90		dB
f = 2400 MHz				90		dB
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	0.1 Hz to 10 Hz		0.75		µV p-p
Voltage Noise Density	e_N	f = 10 Hz		30		nV/√Hz
		f = 100 Hz		15		nV/√Hz
		f = 1 kHz		12.5		nV/√Hz
		f = 10 kHz		12		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		0.8		fA/√Hz
Total Harmonic Distortion + Noise	THD + N	A_V = 1, f = 10 Hz to 20 kHz, V_{IN} = 7 V rms at 1 kHz				
Bandwidth (BW) = 80 kHz				0.0003		%
BW = 500 kHz				0.00035		%
MATCHING SPECIFICATIONS						
Maximum Offset Voltage over Temperature				0.5		mV
Offset Voltage Temperature Drift				2.5		µV/°C
Input Bias Current				0.5	5	pA
CROSSTALK	C_S	R_L = 5 kΩ, V_{IN} = 20 V p-p				
f = 1 kHz				−112		dB
f = 100 kHz				−72		dB

ELECTRICAL CHARACTERISTICS, V$_{SY}$ = ±5 V

V$_{SY}$ = ±5 V, V$_{CM}$ = V$_{OUT}$ = 0 V, T$_A$ = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V$_{OS}$					
A Grade				+0.04	±0.8	mV
		−40°C < T$_A$ < +125°C			±2	mV
B Grade				+0.04	±0.35	mV
ADA4622-1		−40°C < T$_A$ < +125°C			±1	mV
ADA4622-2		−40°C < T$_A$ < +125°C			±0.8	mV
Offset Voltage Match					±1	mV
Offset Voltage Drift	ΔV$_{OS}$/ΔT					
A Grade		−40°C < T$_A$ < +125°C		±2	±15	µV/°C
B Grade		−40°C < T$_A$ < +125°C		±2	±5	µV/°C
Input Bias Current	I$_B$			+2	±10	pA
		−40°C < T$_A$ < +125°C			±1.5	nA
		V$_{CM}$ = V−		−5		pA
Input Offset Current	I$_{OS}$				±10	pA
		−40°C < T$_A$ < +125°C			±0.5	nA
Input Voltage Range	IVR		−5.2		+4	V
Common-Mode Rejection Ratio	CMRR					
A Grade		V$_{CM}$ = − 5 V to +2 V	75	91		dB
		−40°C < T$_A$ < +125°C	73			dB
B Grade		V$_{CM}$ = − 5 V to +2 V	78	91		dB
		−40°C < T$_A$ < +125°C	75			dB
Large Signal Voltage Gain	A$_{VO}$	R$_L$ = 10 kΩ, V$_{OUT}$ = −4.4 V to +4.4 V	113	118		dB
		−40°C < T$_A$ < +125°C	105			dB
		R$_L$ = 1 kΩ, V$_{OUT}$ = −4.4 V to +4.4 V	100	105		dB
		−40°C < T$_A$ < +125°C	91			dB
Input Capacitance	C$_{INDM}$	Differential mode		0.4		pF
	C$_{INCM}$	Common mode		3.6		pF
Input Resistance	R$_{DIFF}$	Differential mode		10^{13}		Ω
	R$_{CM}$	Common mode		10^{13}		Ω
OUTPUT CHARACTERISTICS						
Output Voltage						
High	V$_{OH}$	I$_{SOURCE}$ = 1 mA	4.95	4.97		V
		−40°C < T$_A$ < +125°C	4.9			V
		I$_{SOURCE}$ = 15 mA	4.3	4.51		V
		−40°C < T$_A$ < +125°C	4.1			V
Low	V$_{OL}$	I$_{SINK}$ = 1 mA		−4.955	−4.935	V
		−40°C < T$_A$ < +125°C			−4.88	V
		I$_{SINK}$ = 15 mA		−4.685	−4.55	V
		−40°C < T$_A$ < +125°C			−4.25	V
Output Current	I$_{OUT}$	V$_{DROPOUT}$ < 1 V		20		mA
Short-Circuit Current	I$_{SC}$	Sourcing		31		mA
		Sinking		−40		mA
Closed-Loop Output Impedance	Z$_{OUT}$	f = 1 kHz, A$_V$ = 1		0.1		Ω
		A$_V$ = 10		0.4		Ω
		A$_V$ = 100		4		Ω

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 4$ V to ± 18 V	87	103		dB
		$-40°C < T_A < +125°C$	81			dB
Supply Current per Amplifier	I_{SY}					
ADA4622-1				660	725	µA
		$-40°C < T_A < +125°C$			750	µA
ADA4622-2				610	675	µA
		$-40°C < T_A < +125°C$			700	µA
Shutdown Current		ADA4622-1 only		50		µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$V_{OUT} = \pm 3$ V, $R_L = 2$ kΩ, $C_L = 100$ pF, $A_V = 1$				
		Low to high transition		21		V/µs
		High to low transition		−16		V/µs
Gain Bandwidth Product	GBP	$A_V = 100$, $C_L = 35$ pF		7.8		MHz
Unity-Gain Crossover	UGC	$A_V = 1$		6.5		MHz
−3 dB Bandwidth	−3 dB	$A_V = 1$		10		MHz
Phase Margin	ΦM			50		Degrees
Settling Time	t_S	$V_{IN} = 8$ V step, $R_L = 2$ kΩ, $C_L = 15$ pF, $A_V = -1$				
To 0.1%				1.5		µs
To 0.01%				2		µs
EMI REJECTION RATIO	EMIRR	$V_{IN} = 100$ mV p-p				
f = 1000 MHz				90		dB
f = 2400 MHz				90		dB
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	0.1 Hz to 10 Hz		0.75		µV p-p
Voltage Noise Density	e_N	f = 10 Hz		30		nV/√Hz
		f = 100 Hz		15		nV/√Hz
		f = 1 kHz		12.5		nV/√Hz
		f = 10 kHz		12		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		0.8		pA/√Hz
Total Harmonic Distortion + Noise	THD + N	$A_V = 1$, f = 10 Hz to 20 kHz, $V_{IN} = 1.5$ V rms at 1 kHz				
BW = 80 kHz				0.0005		%
BW = 500 kHz				0.0008		%
MATCHING SPECIFICATIONS						
Maximum Offset Voltage over Temperature				0.5		mV
Offset Voltage Temperature Drift				2.5		µV/°C
Input Bias Current				0.5	5	pA
CROSSTALK	C_S	$R_L = 5$ kΩ, $V_{IN} = 6$ V p-p				
f = 1 kHz				−112		dB
f = 100 kHz				−72		dB

ELECTRICAL CHARACTERISTICS, V$_{SY}$ = 5 V

V$_{SY}$ = 5 V, V$_{CM}$ = 0 V, V$_{OUT}$ = V$_{SY}$/2, T$_A$ = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V$_{OS}$					
A Grade				+0.04	±0.8	mV
		−40°C < T$_A$ < +125°C			±2	mV
B Grade				+0.04	±0.35	mV
ADA4622-1		−40°C < T$_A$ < +125°C			±1	mV
ADA4622-2		−40°C < T$_A$ < +125°C			±0.8	mV
Offset Voltage Match					±1	mV
Offset Voltage Drift	ΔV$_{OS}$/ΔT					
A Grade		−40°C < T$_A$ < +125°C		±2	±15	µV/°C
B Grade		−40°C < T$_A$ < +125°C		±2	±5	µV/°C
Input Bias Current	I$_B$			2	±10	pA
		−40°C < T$_A$ < +125°C			±1.5	nA
Input Offset Current	I$_{OS}$				±10	pA
		−40°C < T$_A$ < +125°C			±0.5	nA
Input Voltage Range	IVR		−0.2		+4	V
Common-Mode Rejection Ratio	CMRR					
A Grade		V$_{CM}$ = 0 V to 2 V	70	87		dB
		−40°C < T$_A$ < +125°C	67			dB
B Grade		V$_{CM}$ = 0 V to 2 V	73	87		dB
		−40°C < T$_A$ < +125°C	70			dB
Large Signal Voltage Gain	A$_{VO}$	R$_L$ = 10 kΩ to V−, V$_{OUT}$ = 0.2 V to 4.6 V	110	115		dB
		−40°C < T$_A$ < +125°C	99			dB
		R$_L$ = 1 kΩ to V−, V$_{OUT}$ = 0.2 V to 4.6 V	96	104		dB
		−40°C < T$_A$ < +125°C	87			dB
Input Capacitance	C$_{INDM}$	Differential mode		0.4		pF
	C$_{INCM}$	Common mode		3.6		pF
Input Resistance	R$_{DIFF}$	Differential mode		10^{13}		Ω
	R$_{CM}$	Common mode		10^{13}		Ω
OUTPUT CHARACTERISTICS						
Output Voltage						
High	V$_{OH}$	I$_{SOURCE}$ = 1 mA	4.95	4.97		V
		−40°C < T$_A$ < +125°C	4.9			V
		I$_{SOURCE}$ = 15 mA	4.3	4.5		V
		−40°C < T$_A$ < +125°C	4.1			V
Low	V$_{OL}$	I$_{SINK}$ = 1 mA		−14.955	−14.935	V
		−40°C < T$_A$ < +125°C			−14.88	V
		I$_{SINK}$ = 15 mA		−14.69	−14.55	V
		−40°C < T$_A$ < +125°C			−14.25	V
Output Current	I$_{OUT}$	V$_{DROPOUT}$ < 1 V		20		mA
Short-Circuit Current	I$_{SC}$	Sourcing		27		mA
		Sinking		−35		mA
Closed-Loop Output Impedance	Z$_{OUT}$	f = 1 kHz, A$_V$ = 1		0.1		Ω
		A$_V$ = 10		0.6		Ω
		A$_V$ = 100		5		Ω

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 4 V to 15 V	80	95		dB
		−40°C < T_A < +125°C	74			dB
Supply Current per Amplifier	I_{SY}					
ADA4622-1				650	700	μA
		−40°C < T_A < +125°C			725	μA
ADA4622-2				600	650	μA
		−40°C < T_A < +125°C			675	μA
Shutdown Current		ADA4622-1 only		50		μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	V_{OUT} = 0.5 V to 3.5 V, R_L = 2 kΩ, C_L = 100 pF, A_V = 1				
		Low to high transition		20		V/μs
		High to low transition		−15		V/μs
Gain Bandwidth Product	GBP	A_V = 100, C_L = 35 pF		7.2		MHz
Unity-Gain Crossover	UGC	A_V = 1		6		MHz
−3 dB Bandwidth	−3 dB	A_V = 1		9		MHz
Phase Margin	ΦM			50		Degrees
Settling Time	t_S	V_{IN} = 4 V step, R_L = 2 kΩ, C_L = 15 pF, A_V = −1				
To 0.1%				1.5		μs
To 0.01%				2.0		μs
EMI REJECTION RATIO	EMIRR	V_{IN} = 100 mV p-p				
f = 1000 MHz				90		dB
f = 2400 MHz				90		dB
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	0.1 Hz to 10 Hz		0.75		μV p-p
Voltage Noise Density	e_N	f = 10 Hz		30		nV/√Hz
		f = 100 Hz		15		nV/√Hz
		f = 1 kHz		12.5		nV/√Hz
		f = 10 kHz		12		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		0.8		pA/√Hz
Total Harmonic Distortion + Noise	THD + N	A_V = 1, f = 10 Hz to 20 kHz, V_{IN} = 0.5 V rms at 1 kHz				
BW = 80 kHz				0.0025		%
BW = 500 kHz				0.0025		%
MATCHING SPECIFICATIONS						
Maximum Offset Voltage over Temperature				0.5		mV
Offset Voltage Temperature Drift				2.5		μV/°C
Input Bias Current				0.5	5	pA
CROSSTALK	C_S	R_L = 5 kΩ, V_{IN} = 3 V p-p				
f = 1 kHz				−112		dB
f = 100 kHz				−72		dB

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	(V−) − 0.3 V to (V+) + 0.2 V
Differential Input Voltage	36 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature, Soldering (10 sec)	300°C
ESD Rating, Human Body Model (HBM)	4 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 5. Thermal Resistance[1]

Package Type	θ_{JA}	θ_{JC}[2]	Unit
8-Lead SOIC			
1-Layer JEDEC Board	180	63	°C/W
2-Layer JEDEC Board	120	N/A	°C/W
8-Lead MSOP			
1-Layer JEDEC Board	265	115	°C/W
2-Layer JEDEC Board	185	N/A	°C/W
8-Lead LFCSP			
1-Layer JEDEC Board	272	63	°C/W
2-Layer JEDEC Board	145	N/A	°C/W
2-Layer JEDEC Board with 2 × 2 Vias	55	N/A	°C/W
5-Lead SOT-23			
1-Layer JEDEC Board	538	82	°C/W
2-Layer JEDEC Board	339	N/A	°C/W

[1] Thermal impedance simulated values are based on a JEDEC thermal test board. See JEDEC JESD51.
[2] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS
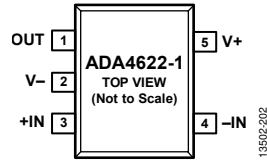
Figure 3. 5-Lead SOT-23 Pin Configuration, ADA4622-1

Table 6. 5-Lead SOT-23 Pin Function Descriptions, ADA4622-1

Pin No.	Mnemonic	Description
1	OUT	Output
2	V−	Negative Supply Voltage
3	+IN	Noninverting Input
4	−IN	Inverting Input
5	V+	Positive Supply Voltage
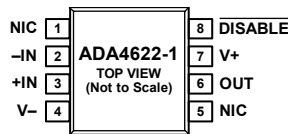
NOTES
1. NIC = NOT INTERNALLY CONNECTED.

Figure 4. 8-Lead SOIC Pin Configuration, ADA4622-1

Table 7. 8-Lead SOIC Pin Function Descriptions, ADA4622-1

Pin No.	Mnemonic	Description
1, 5	NIC	Not Internally Connected
2	−IN	Inverting Input
3	+IN	Noninverting Input
4	V−	Negative Supply Voltage
6	OUT	Output
7	V+	Positive Supply Voltage
8	$\overline{\text{DISABLE}}$	Disable Input (Active Low)
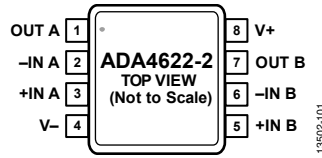
Figure 5. 8-Lead MSOP Pin Configuration, ADA4622-2
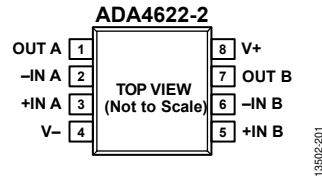
Figure 6. 8-Lead SOIC Pin Configuration, ADA4622-2

Table 8. 8-Lead MSOP and 8-Lead SOIC Pin Function Descriptions, ADA4622-2

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A
2	−IN A	Inverting Input, Channel A
3	+IN A	Noninverting Input, Channel A
4	V−	Negative Supply Voltage
5	+IN B	Noninverting Input, Channel B
6	−IN B	Inverting Input, Channel B
7	OUT B	Output, Channel B
8	V+	Positive Supply Voltage
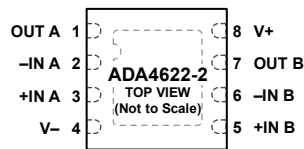
NOTES
1. IT IS RECOMMENDED TO CONNECT THE EXPOSED PAD TO THE V+ PIN.

Figure 7. 8-Lead LFCSP Pin Configuration, ADA4622-2

Table 9. 8-Lead LFCSP Pin Function Descriptions, ADA4622-2

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A.
2	−IN A	Inverting Input, Channel A.
3	+IN A	Noninverting Input, Channel A.
4	V−	Negative Supply Voltage.
5	+IN B	Noninverting Input, Channel B.
6	−IN B	Inverting Input, Channel B.
7	OUT B	Output, Channel B.
8	V+	Positive Supply Voltage.
	EPAD	Exposed Pad. It is recommended to connect the exposed pad to the V+ pin.

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, unless otherwise noted.
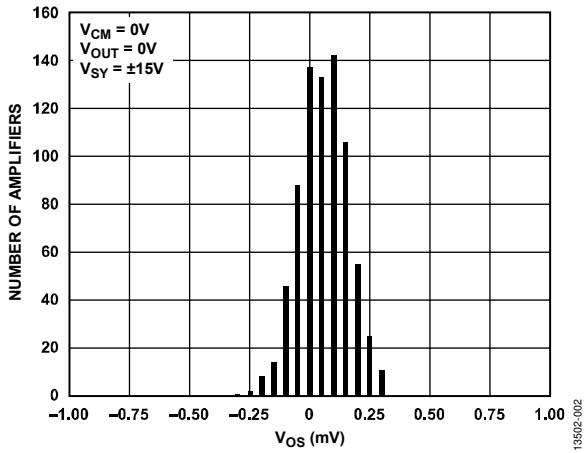
Figure 8. Input Offset Voltage (V_{OS}) Distribution, $V_{SY} = ±15 V$

Figure 9. Input Offset Voltage (V_{OS}) Distribution, $V_{SY} = ±5 V$

Figure 10. Input Offset Voltage (V_{OS}) Distribution, $V_{SY} = 5 V$
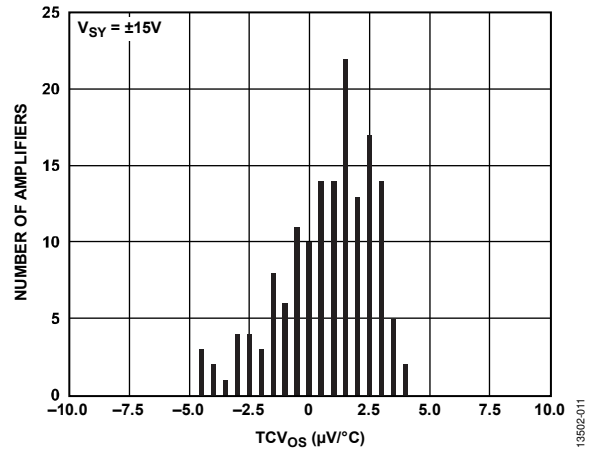
Figure 11. Input Offset Voltage Drift (TCV$_{OS}$) Distribution (−40°C to +85°C), $V_{SY} = ±15 V$
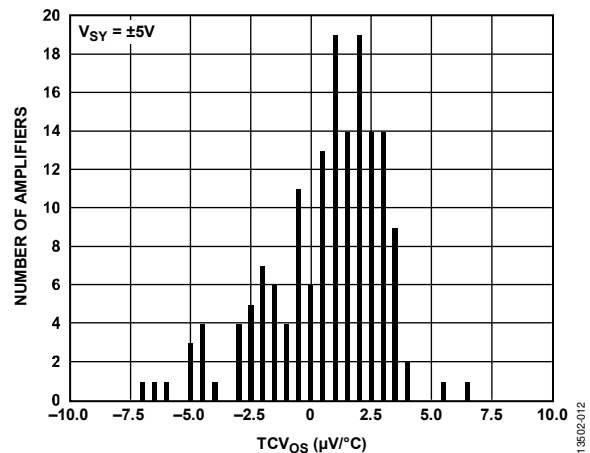
Figure 12. Input Offset Voltage Drift (TCV$_{OS}$) Distribution (−40°C to +125°C), $V_{SY} = ±5 V$
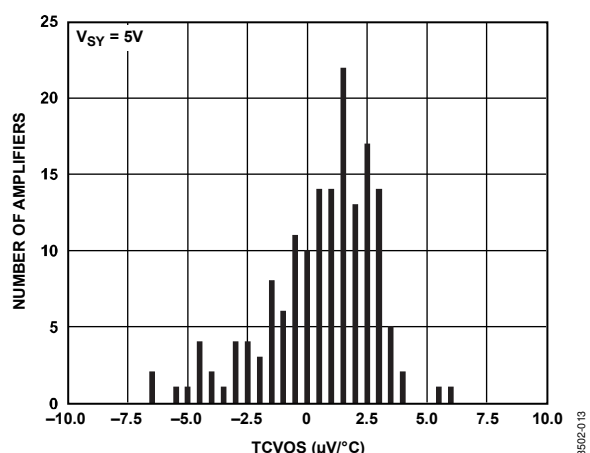
Figure 13. Input Offset Voltage Drift (TCV$_{OS}$) Distribution (−40°C to +125°C), $V_{SY} = 5 V$
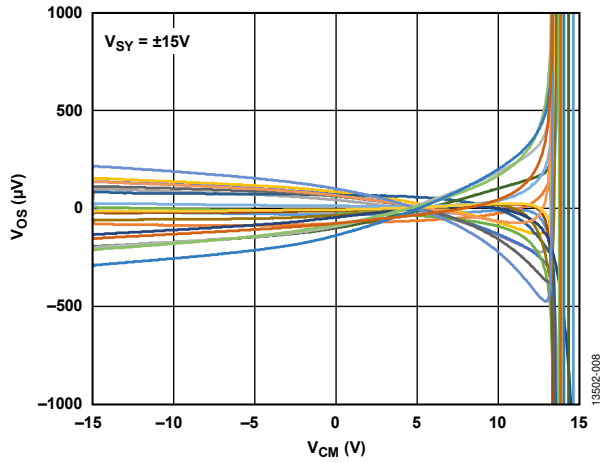
Figure 14. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), $V_{SY} = \pm15$ V

Figure 15. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), $V_{SY} = \pm5$ V

Figure 16. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), $V_{SY} = 5$ V
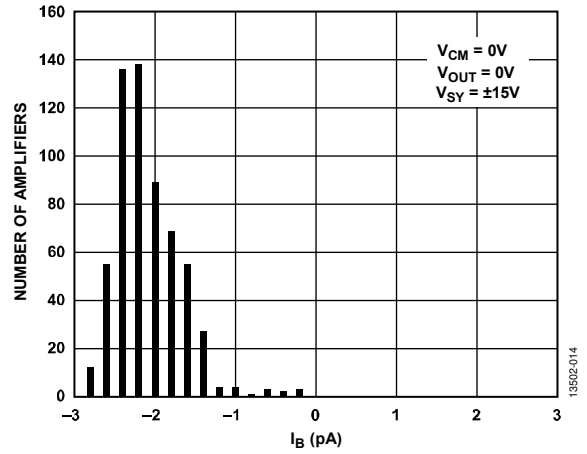
Figure 17. Input Bias Current (I_B) Distribution, $V_{SY} = \pm15$ V
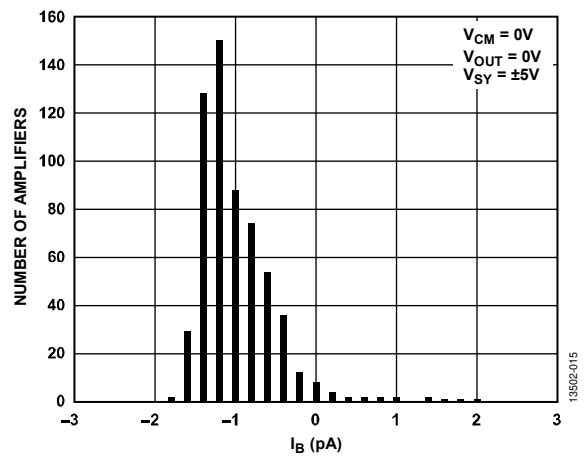
Figure 18. Input Bias Current (I_B) Distribution, $V_{SY} = \pm5$ V
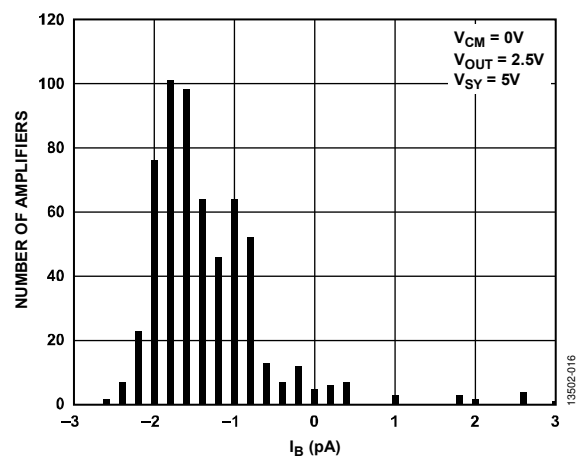
Figure 19. Input Bias Current (I_B) Distribution, $V_{SY} = 5$ V
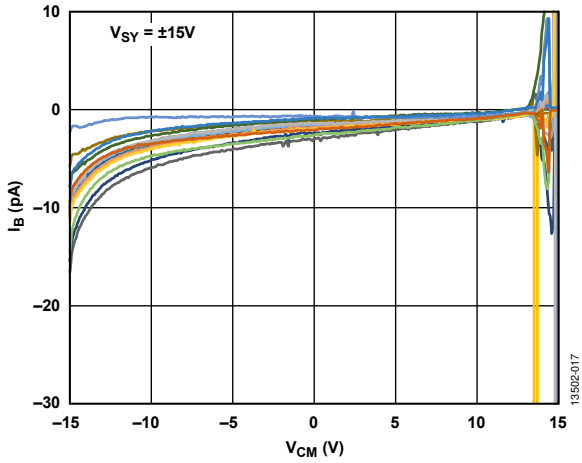
Figure 20. Input Bias Current (I_B) vs. Input Common-Mode Voltage (V_{CM}), $V_{SY} = ±15$ V

Figure 21. Input Bias Current (I_B) vs. Input Common-Mode Voltage (V_{CM}), $V_{SY} = ±5$ V

Figure 22. Input Bias Current (I_B) vs. Input Common-Mode Voltage (V_{CM}), $V_{SY} = 5$ V
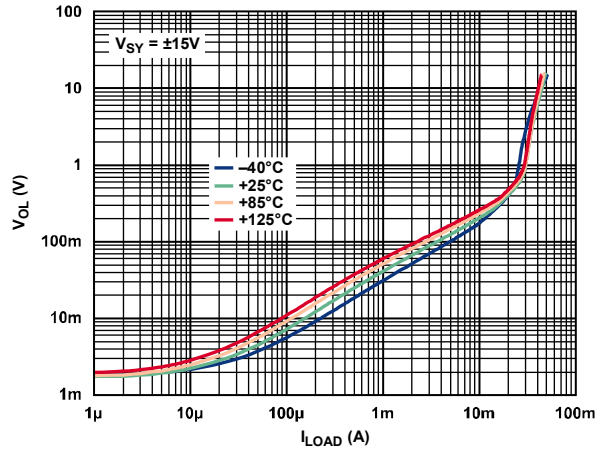
Figure 23. Output Voltage Low (V_{OL}) to Supply Rail vs. Load Current (I_{LOAD}) over Temperature, $V_{SY} = ±15$ V
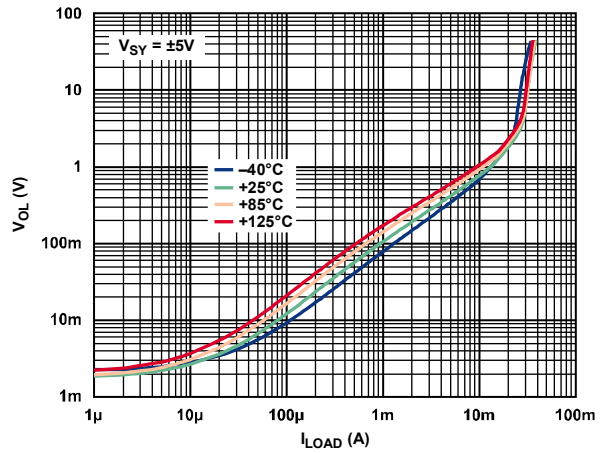
Figure 24. Output Voltage Low (V_{OL}) to Supply Rail vs. Load Current (I_{LOAD}) over Temperature, $V_{SY} = ±5$ V
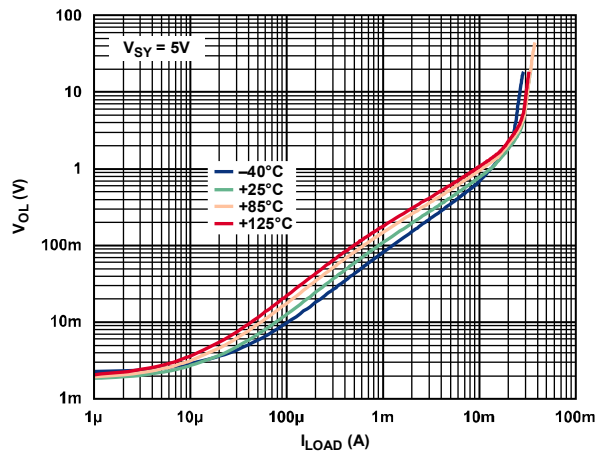
Figure 25. Output Voltage Low (V_{OL}) to Supply Rail vs. Load Current (I_{LOAD}) over Temperature, $V_{SY} = 5$ V
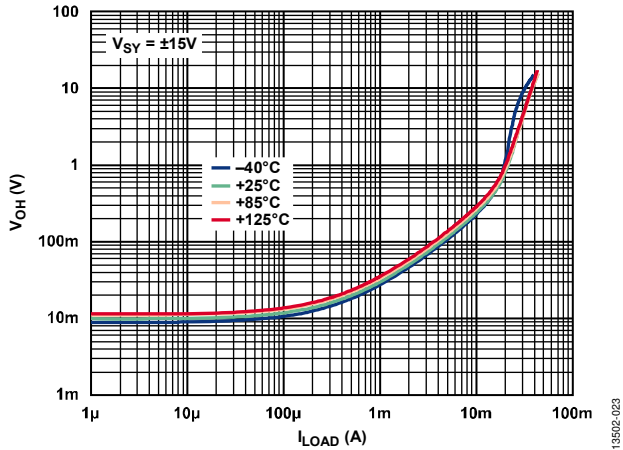
Figure 26. Output Voltage High (V_{OH}) to Supply Rail vs. Load Current (I_{LOAD}) over Temperature, $V_{SY} = \pm15$ V
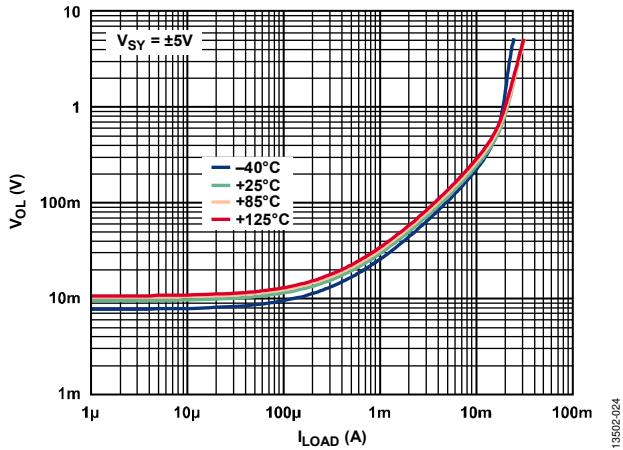
Figure 27. Output Voltage High (V_{OH}) to Supply Rail vs. Load Current (I_{LOAD}) over Temperature, $V_{SY} = \pm5$ V
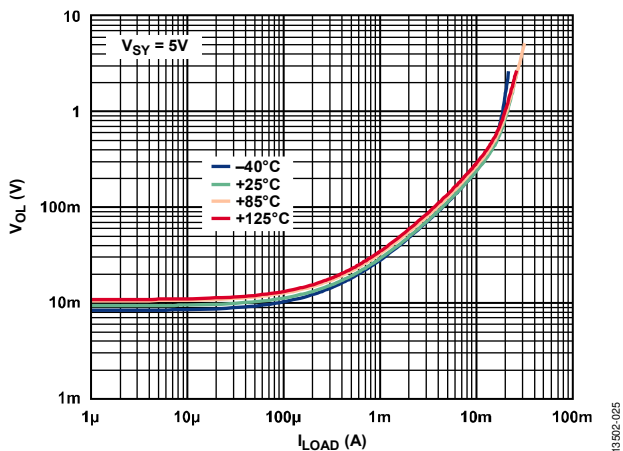
Figure 28. Output Voltage High (V_{OH}) to Supply Rail vs. Load Current (I_{LOAD}) over Temperature, $V_{SY} = 5$ V
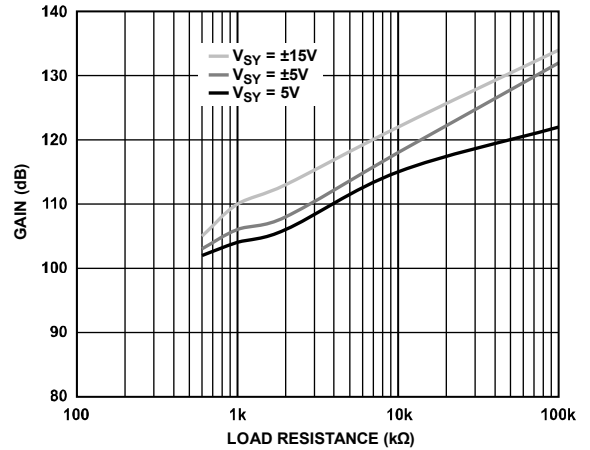
Figure 29. Open-Loop Gain (A_{VO}) vs. Load Resistance
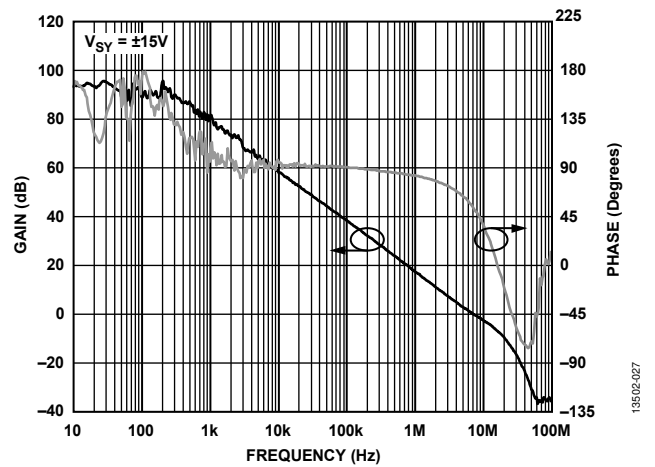
Figure 30. Open-Loop Gain and Phase vs. Frequency, $V_{SY} = \pm15$ V
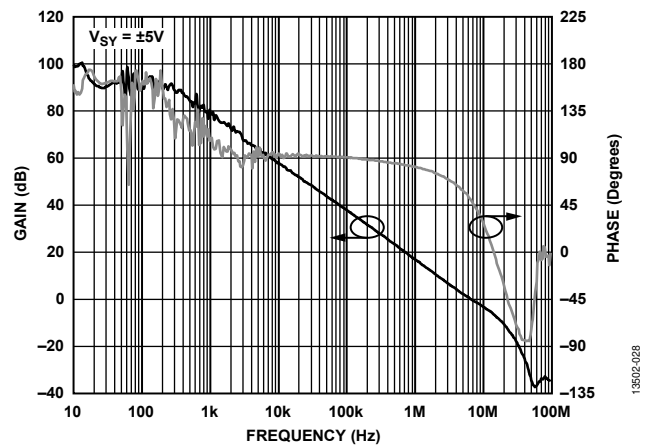
Figure 31. Open-Loop Gain and Phase vs. Frequency, $V_{SY} = \pm5$ V
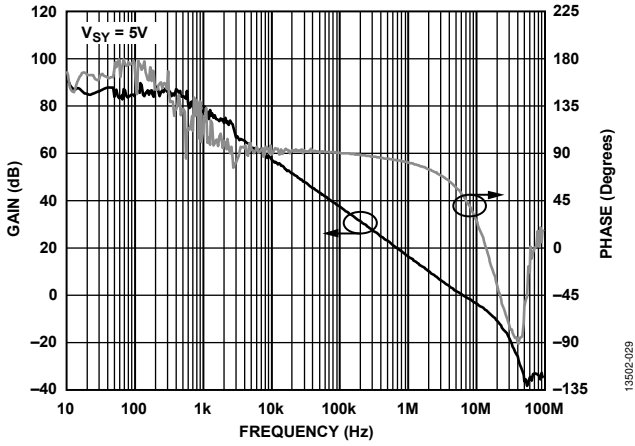
Figure 32. Open-Loop Gain and Phase vs. Frequency, V_{SY} = 5 V
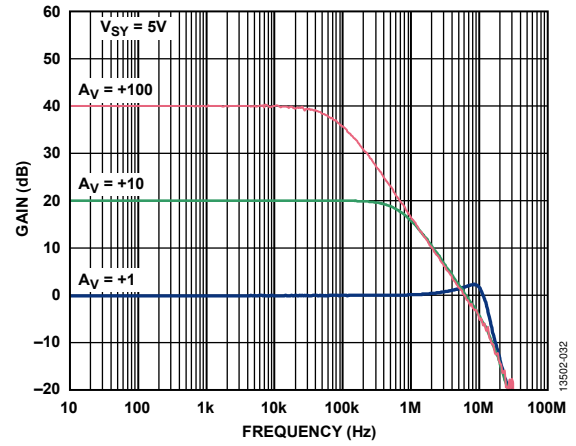
Figure 35. Closed-Loop Gain vs. Frequency, V_{SY} = 5 V
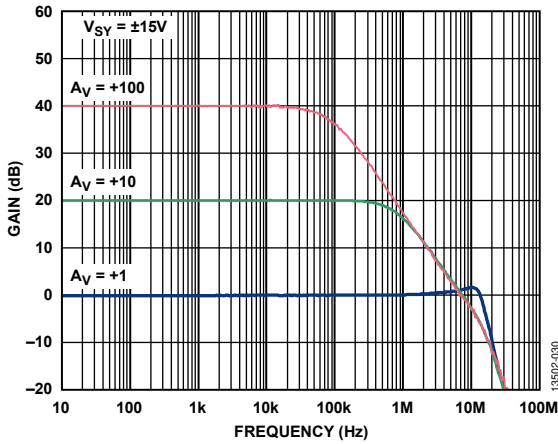
Figure 33. Closed-Loop Gain vs. Frequency, V_{SY} = ±15 V
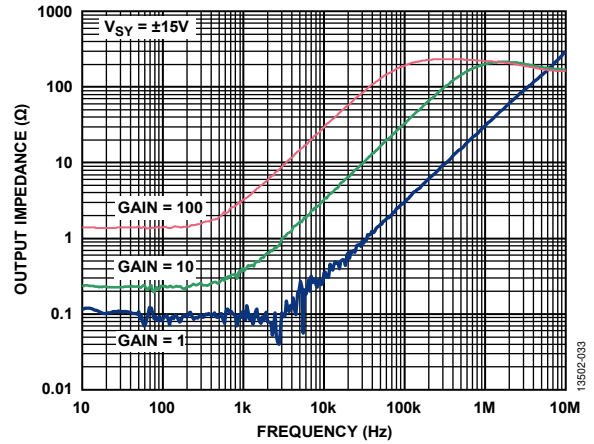
Figure 36. Output Impedance vs. Frequency, V_{SY} = ±15 V
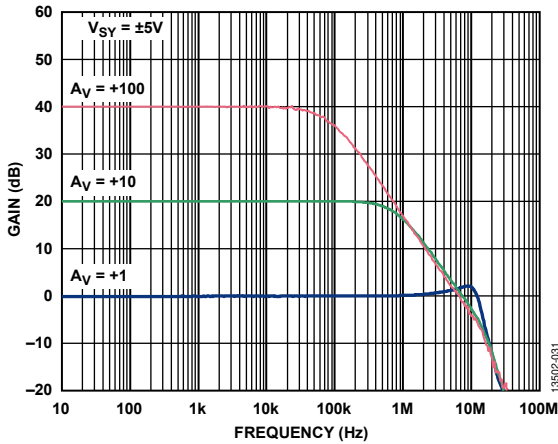
Figure 34. Closed-Loop Gain vs. Frequency, V_{SY} = ±5 V
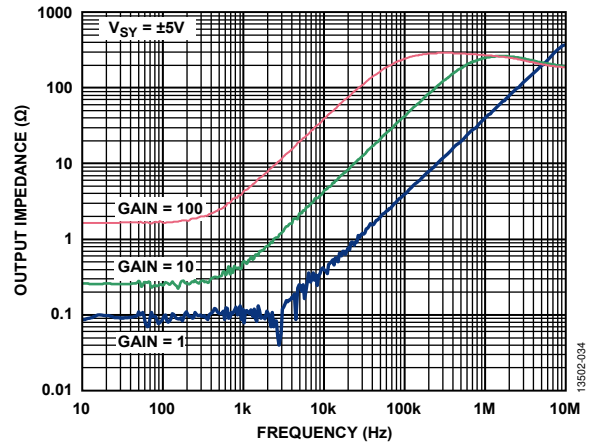
Figure 37. Output Impedance vs. Frequency, V_{SY} = ±5 V
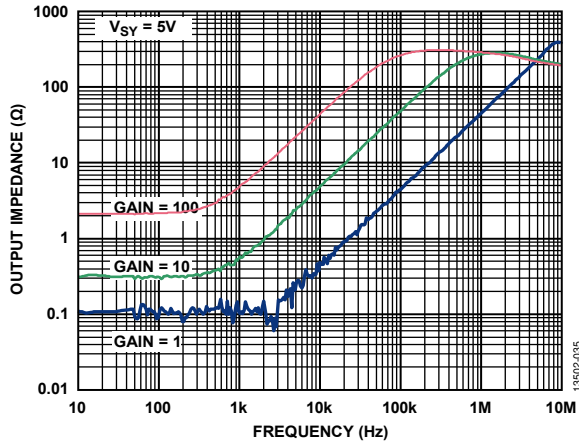
Figure 38. Output Impedance vs. Frequency, V_{SY} = 5 V
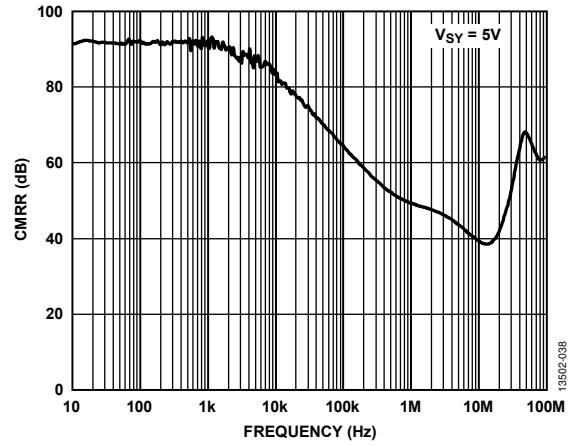
Figure 41. CMRR vs. Frequency, V_{SY} = 5 V
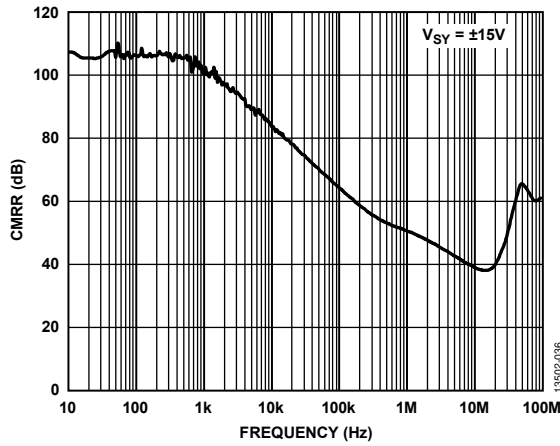
Figure 39. CMRR vs. Frequency, V_{SY} = ±15 V
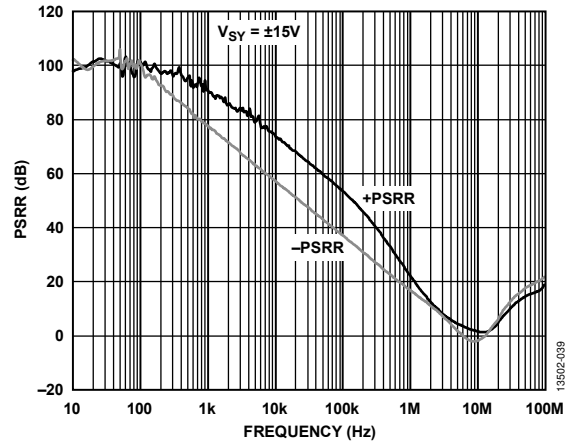
Figure 42. PSRR vs. Frequency, V_{SY} = ±15 V
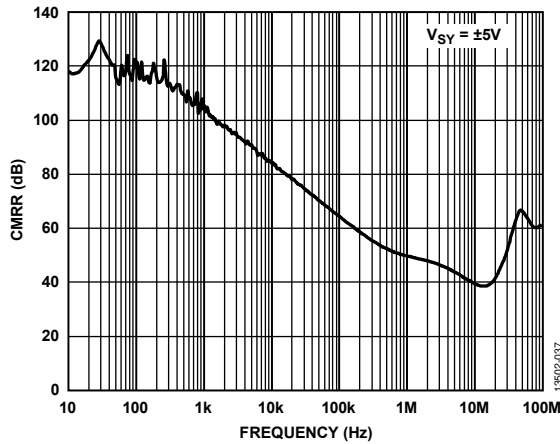
Figure 40. CMRR vs. Frequency, V_{SY} = ±5 V
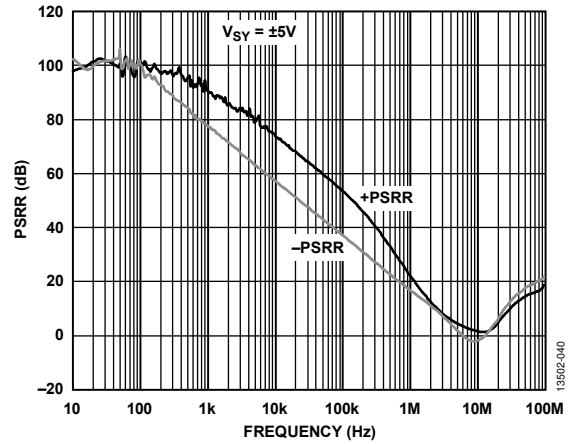
Figure 43. PSRR vs. Frequency, V_{SY} = ±5 V
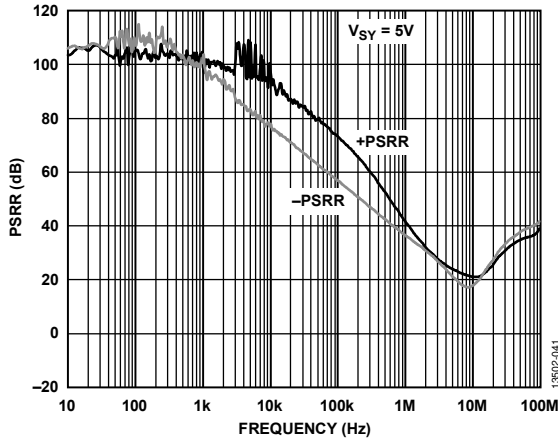
Figure 44. PSRR vs. Frequency, V_{SY} = 5 V
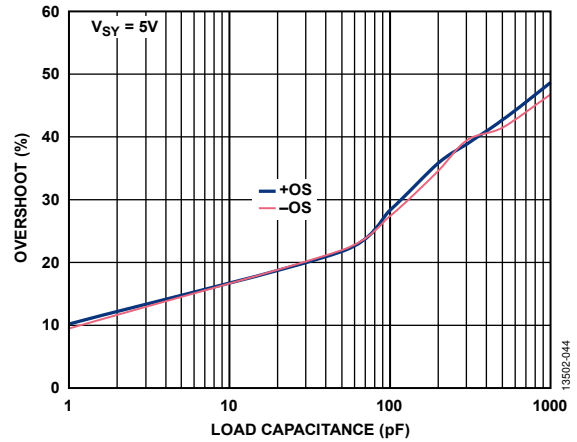
Figure 47. Small Signal Overshoot (OS) vs. Load Capacitance, V_{SY} = 5 V
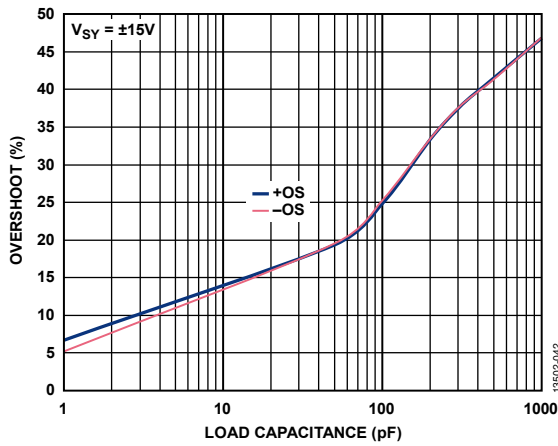
Figure 45. Small Signal Overshoot (OS) vs. Load Capacitance, V_{SY} = ±15 V
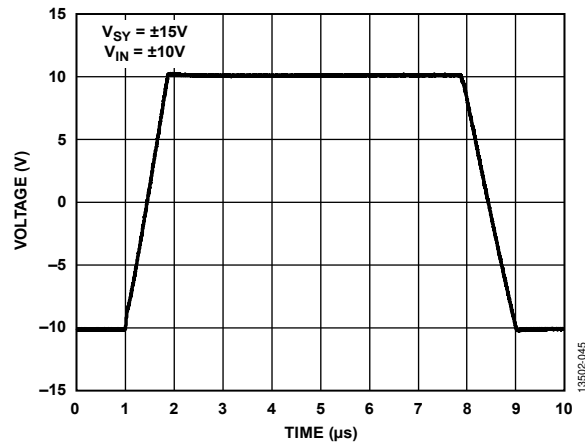
Figure 48. Large Signal Transient Response, V_{SY} = ±15 V
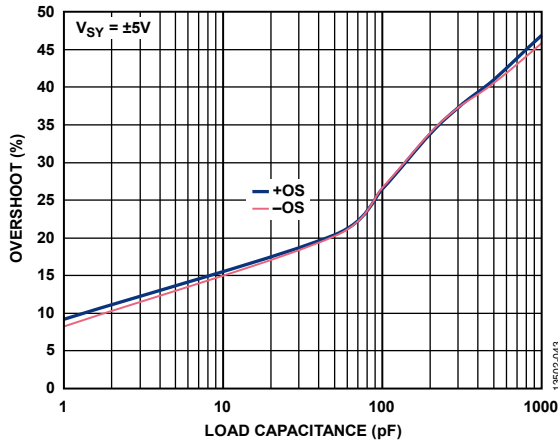
Figure 46. Small Signal Overshoot (OS) vs. Load Capacitance, V_{SY} = ±5 V
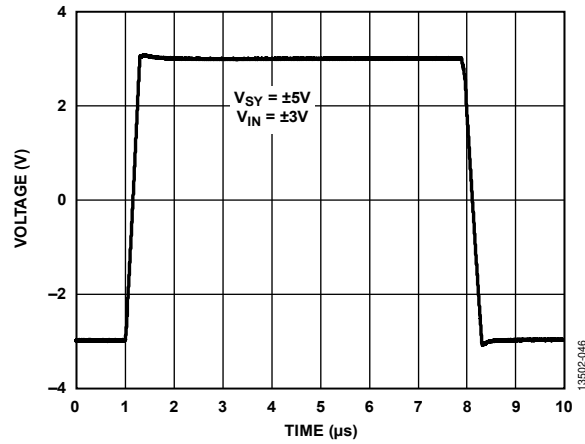
Figure 49. Large Signal Transient Response, V_{SY} = ±5 V
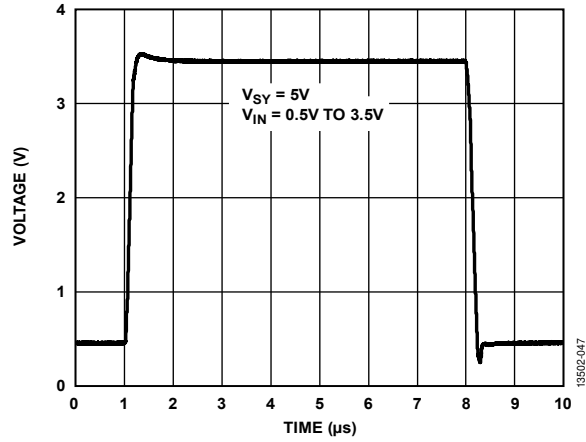
Figure 50. Large Signal Transient Response, V_SY = 5 V

Figure 51. Large Signal Transient Response, V_SY = ±2.5 V

Figure 52. Small Signal Transient Response, V_SY = ±15 V

Figure 53. Small Signal Transient Response, V_SY = ±5 V

Figure 54. Small Signal Transient Response, V_SY = 5 V
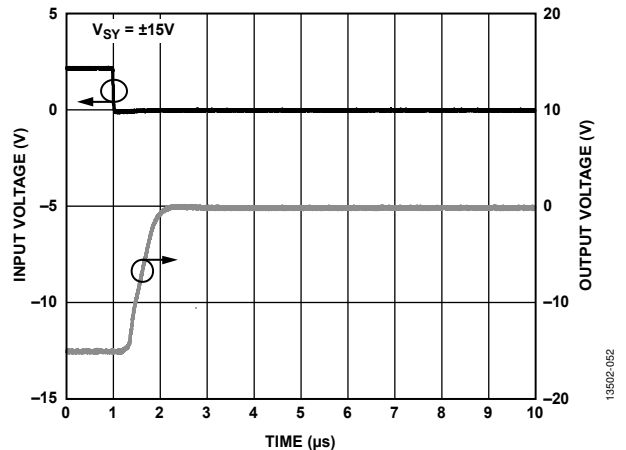
Figure 55. Negative Overload Recovery, A_V = −10, V_SY = ±15 V
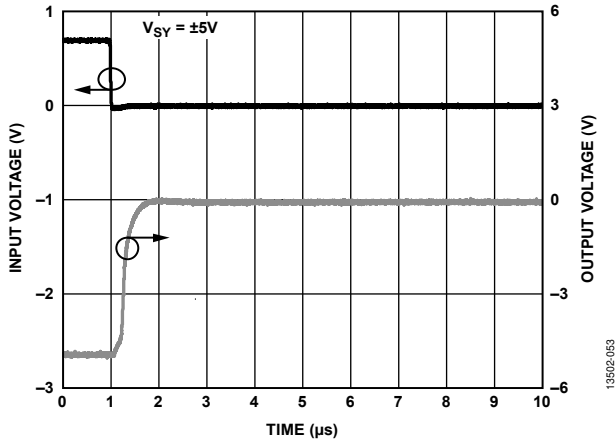
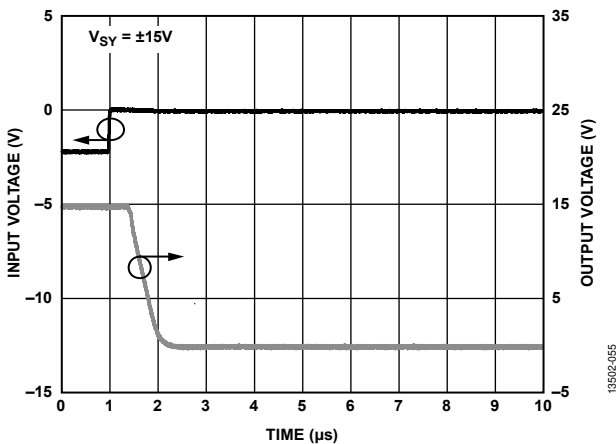Figure 56. Negative Overload Recovery, $A_V = -10$, $V_{SY} = \pm5$ V
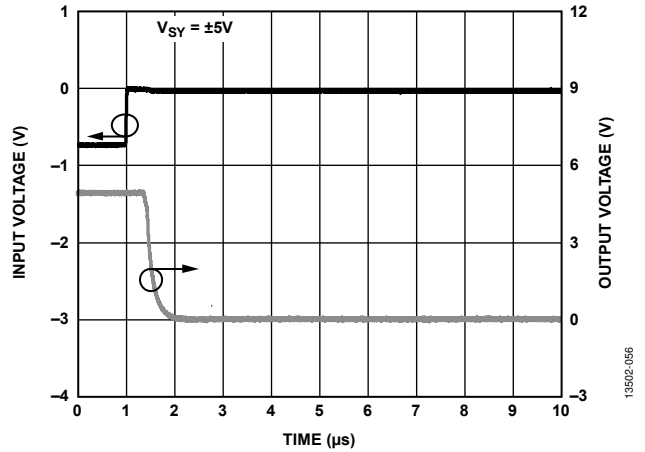
Figure 59. Positive Overload Recovery, $A_V = -10$, $V_{SY} = \pm5$ V
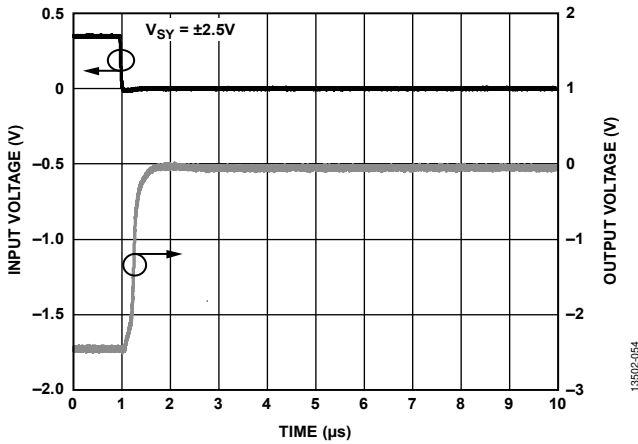
Figure 57. Negative Overload Recovery, $A_V = -10$, $V_{SY} = \pm2.5$ V
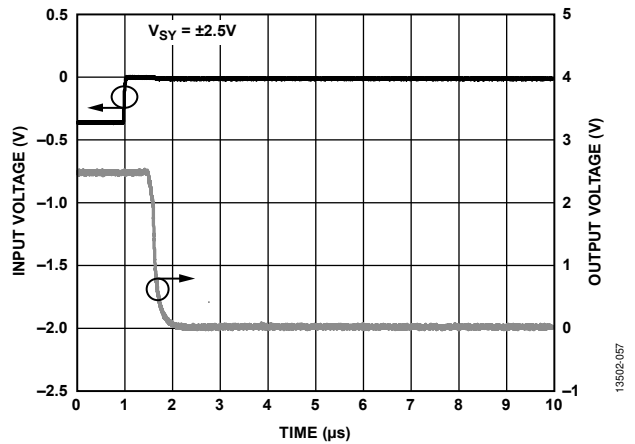
Figure 60. Positive Overload Recovery, $A_V = -10$, $V_{SY} = \pm2.5$ V

Figure 58. Positive Overload Recovery, $A_V = -10$, $V_{SY} = \pm15$ V
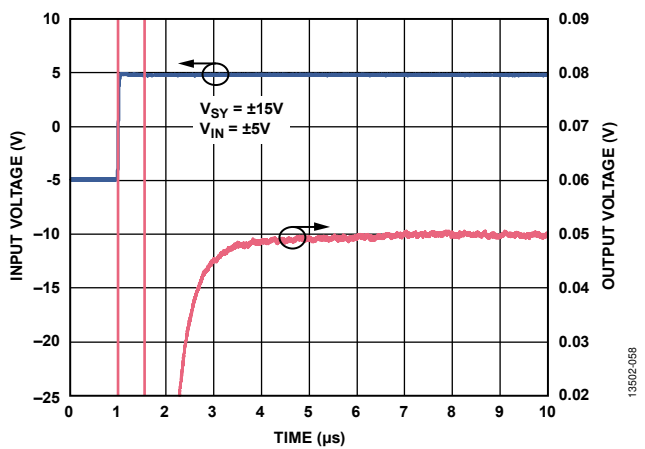
Figure 61. Positive Settling Time, $A_V = -10$, $V_{SY} = \pm15$ V
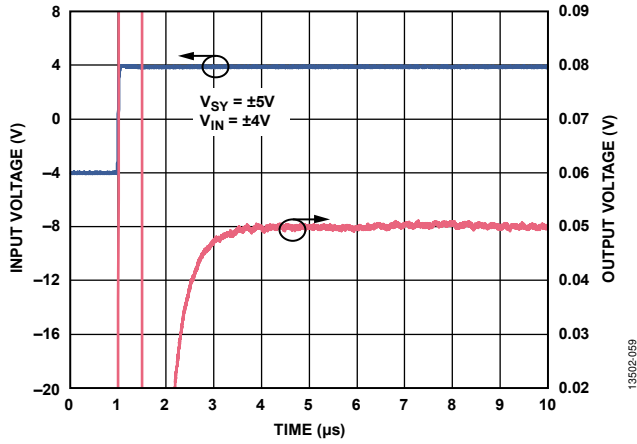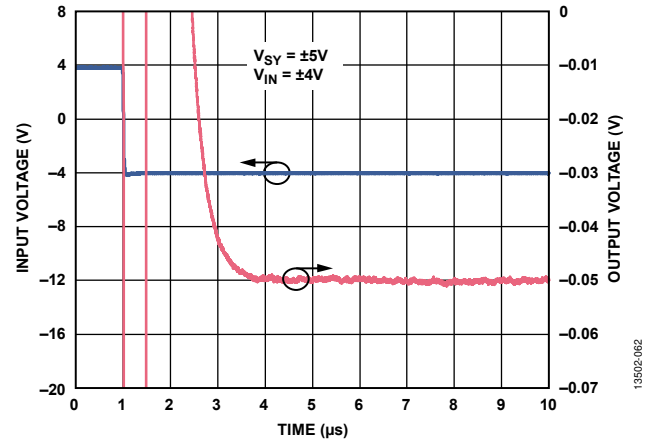
Figure 62. Positive Settling Time, $A_V = -10$, $V_{SY} = \pm 5$ V

Figure 65. Negative Setting Time, $A_V = -10$, $V_{SY} = \pm 5$ V
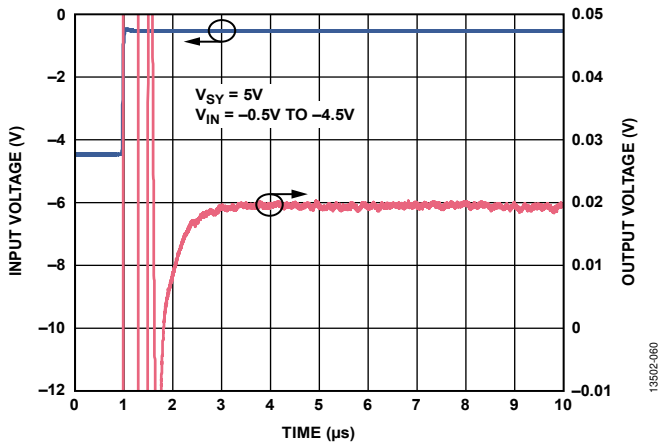
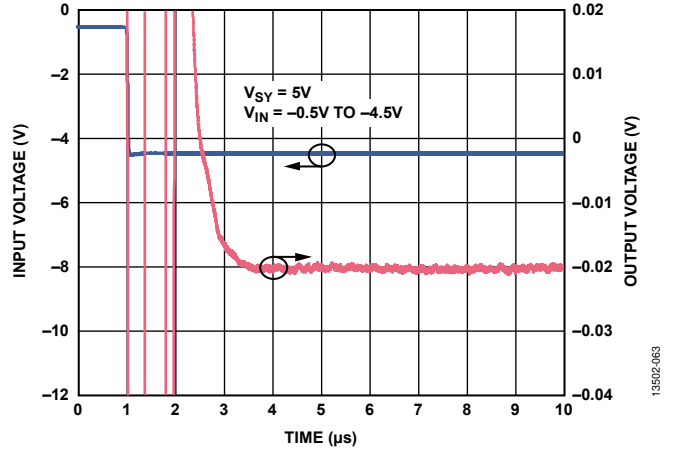Figure 63. Positive Settling Time, $A_V = -10$, $V_{SY} = 5$ V

Figure 66. Negative Setting Time, $A_V = -10$, $V_{SY} = 5$ V
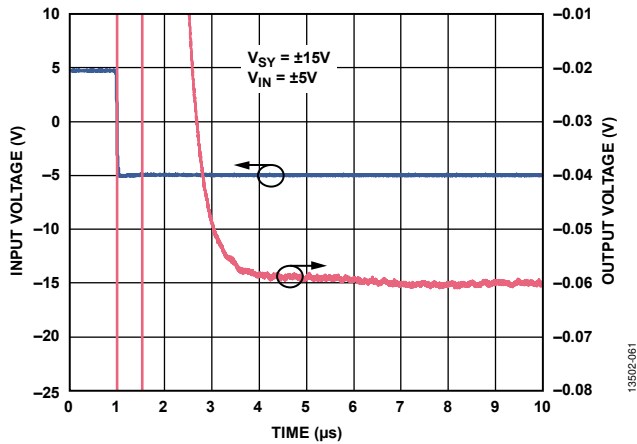

Figure 64. Negative Setting Time, $A_V = -10$, $V_{SY} = \pm 15$ V
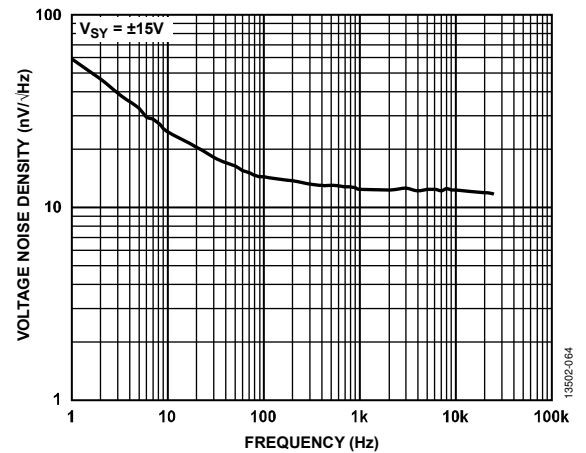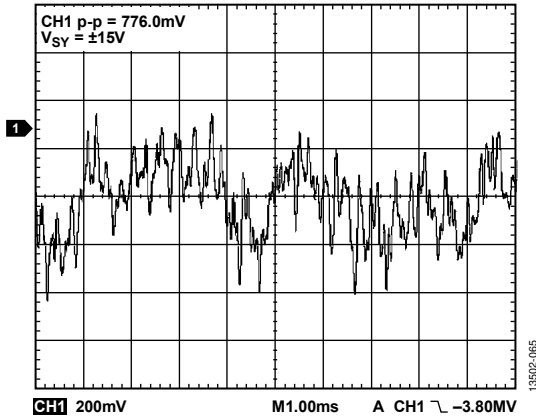

Figure 67. Voltage Noise Density, $V_{SY} = \pm 15$ V

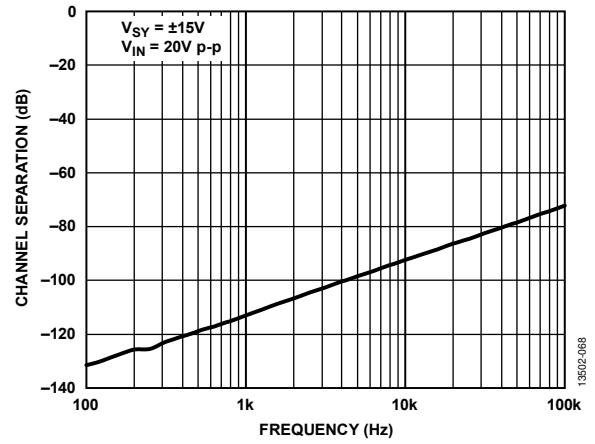Figure 68. 0.1 Hz to 10 Hz Noise, V_{SY} = ±15 V
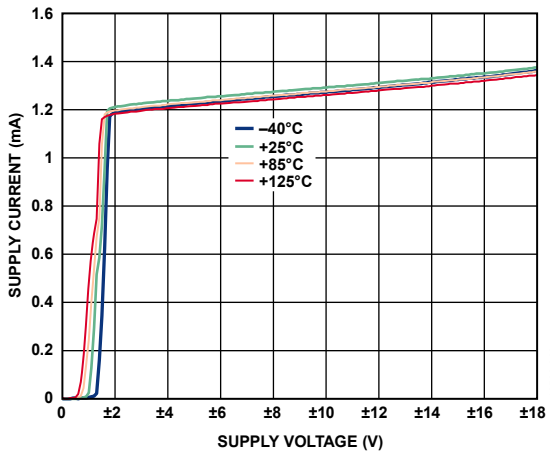

Figure 71. Channel Separation vs. Frequency, V_{SY} = ±15 V

Figure 69. Supply Current (I_{SY}) vs. Supply Voltage (V_{SY}) for Various Temperatures
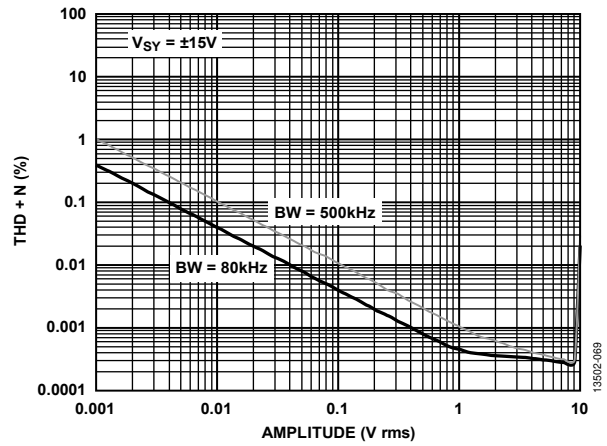

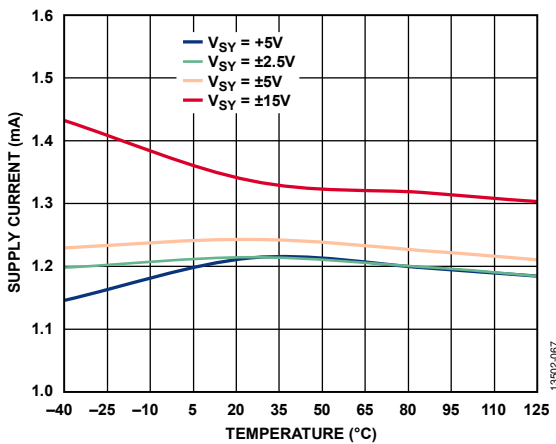Figure 72. THD + N vs. Amplitude, V_{SY} = ±15 V

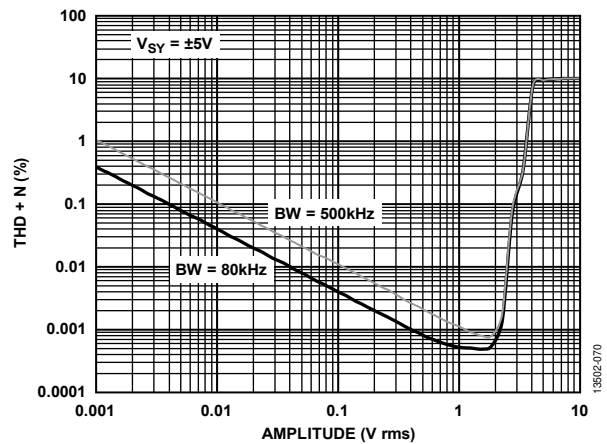Figure 70. Supply Current (I_{SY}) vs. Temperature for Various Supply Voltages

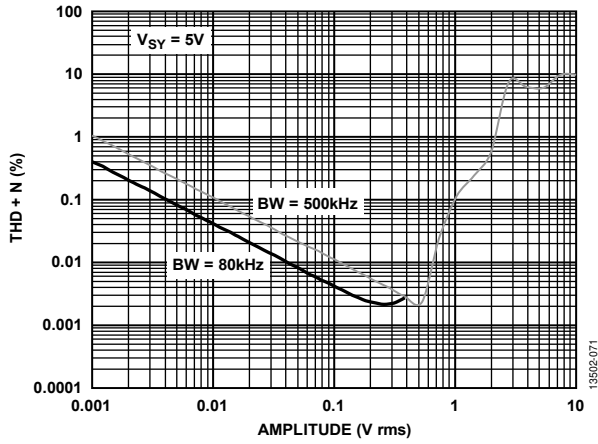Figure 73. THD + N vs. Amplitude, V_{SY} = ±5 V

Figure 74. THD + N vs. Amplitude, V_{SY} = 5 V
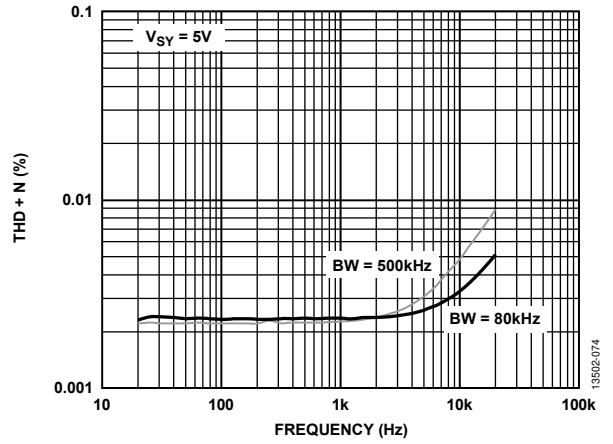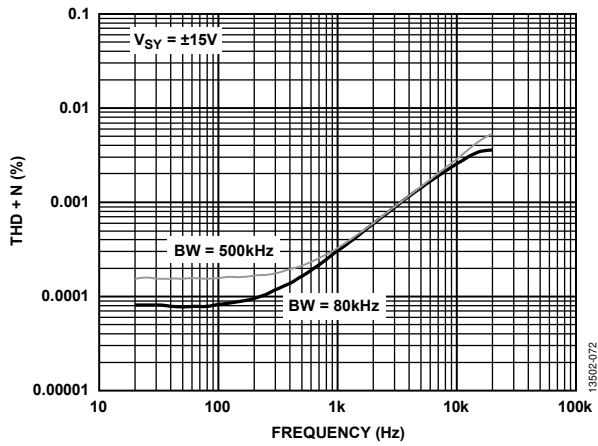

Figure 75. THD + N vs. Frequency, V_{SY} = ±15 V
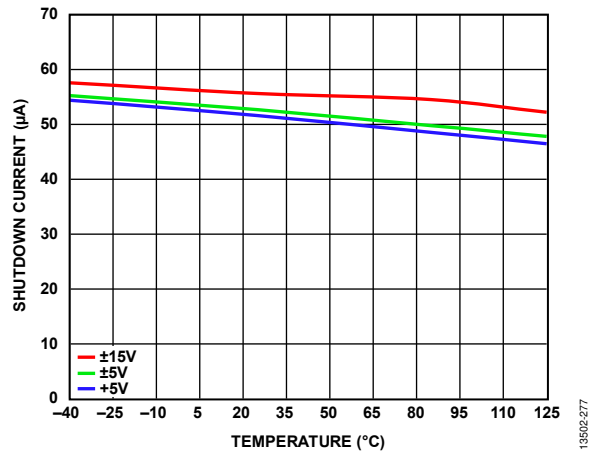

Figure 76. THD + N vs. Frequency, V_{SY} = ±5 V

Figure 77. THD + N vs. Frequency, V_{SY} = 5 V

Figure 78. Shutdown Current vs. Temperature
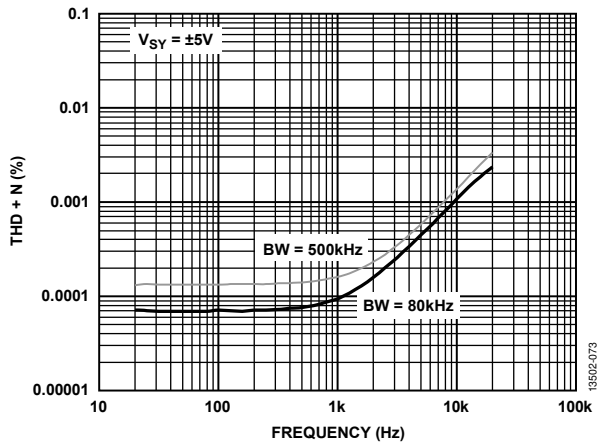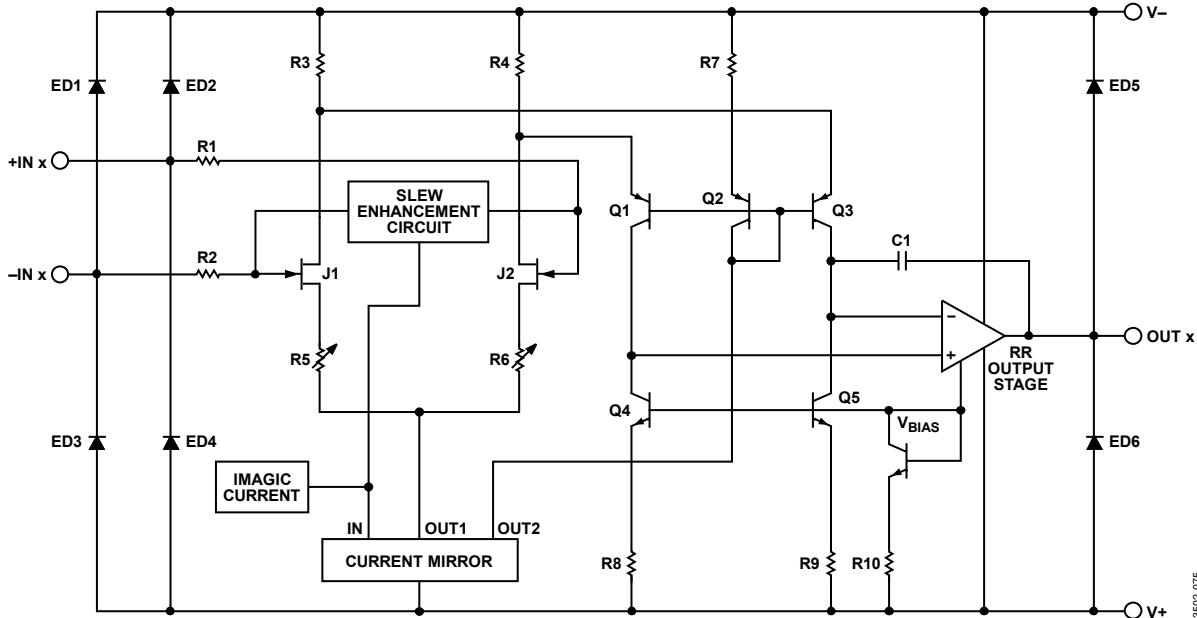
THEORY OF OPERATION

Figure 79. Simplified Circuit Diagram

INPUT CHARACTERISTICS

The ADA4622-1/ADA4622-2 input stage consists of N-channel, JFETs that provide low offset, low noise, and high impedance. The minimum input common-mode voltage extends from −0.2 mV below V− to 1 V less than V+. Driving the input closer to the positive rail causes loss of amplifier bandwidth and increased common-mode voltage error. Figure 80 shows the rounding of the output due to the loss of bandwidth. The input and output are superimposed.
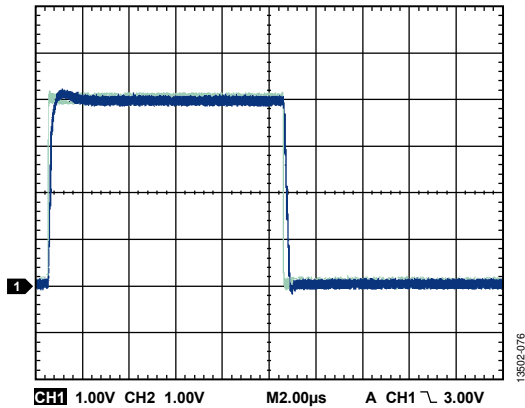

CH1 1.00V CH2 1.00V   M2.00µs   A CH1 ⌐ 3.00V

Figure 80. Bandwidth Limiting due to Headroom Requirements

The ADA4622-1/ADA4622-2 do not exhibit phase reversal for input voltages up to V+. For input voltages greater than V+, a 10 kΩ resistor in series with the noninverting input prevents phase reversal at the expense of higher noise (see Figure 81).

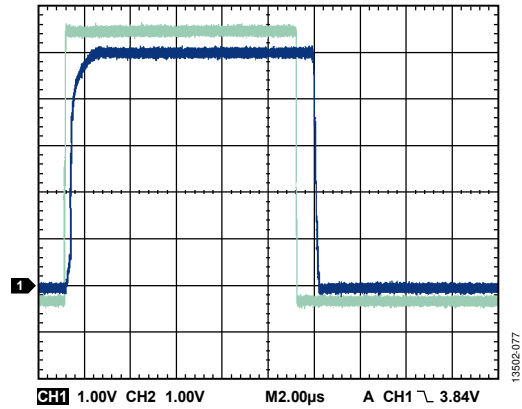CH1 1.00V CH2 1.00V   M2.00µs   A CH1 ⌐ 3.84V

Figure 81. No Phase Reversal

Because the input stage uses N-channel JFETs, the input current during normal operation is negative. However, the input bias current changes direction as the input voltage approaches V+ due to internal junctions becoming forward-biased (see Figure 82).
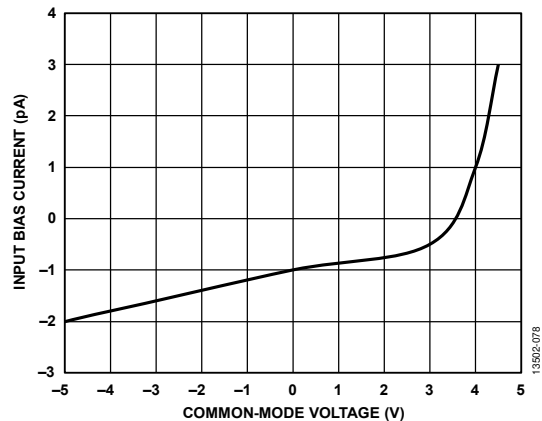

Figure 82. Input Bias Current vs. Common-Mode Voltage with ±5 V Supply

The [ADA4622-1](#)/[ADA4622-2](#) are designed for 12 nV/√Hz wideband input voltage noise density and maintain low noise performance at low frequencies (see Figure 83). This noise performance, along with the low input current as well as low current noise, means that the [ADA4622-1](#)/[ADA4622-2](#) contribute negligible noise for applications with a source resistance greater than 10 kΩ and at signal bandwidths greater than 1 kHz.
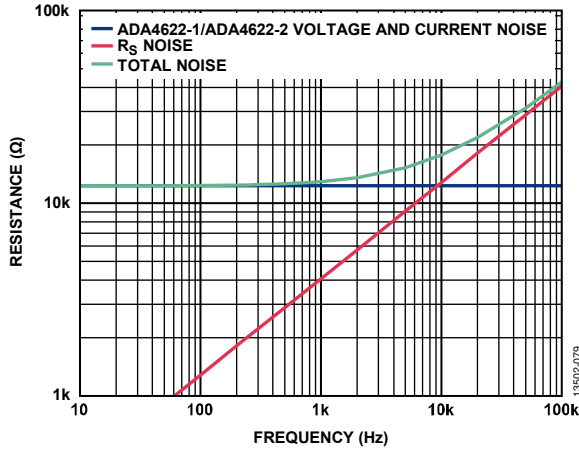

Figure 83. Total Noise vs. Source Resistance

Input Overvoltage Protection

The [ADA4622-1](#)/[ADA4622-2](#) have internal protective circuitry that allows voltages as high as 0.3 V beyond the supplies applied at the input of either terminal without causing damage. Use a current-limiting resistor in series with the input of the [ADA4622-1](#)/[ADA4622-2](#) if the input voltage exceeds 0.3 V beyond the supply rails of the amplifiers. If the overvoltage condition persists for more than a few seconds, damage to the amplifiers can result.

For higher input voltages, determine the resistor value by

$$\frac{V_{IN} - V_{SY}}{R_S} \leq 10 \text{ mA}$$

where:
V_{IN} is the input voltage.
V_{SY} is the voltage of either the V+ pin or the V− pin.
R_S is the series resistor.

With a very low input bias current of ±1.5 nA maximum up to 125°C, higher resistor values can be used in series with the inputs without introducing large offset errors. A 1 kΩ series resistor allows the [ADA4622-1](#)/[ADA4622-2](#) to withstand 10 V of continuous overvoltage and increases the noise by a negligible amount. A 5 kΩ resistor protects the inputs from voltages as high as 25 V beyond the supplies and adds less than 10 μV to the offset voltage of the amplifiers.

EMI Rejection Ratio

Figure 84 shows the EMI rejection ratio (EMIRR) vs. the frequency for the [ADA4622-1](#)/[ADA4622-2](#).
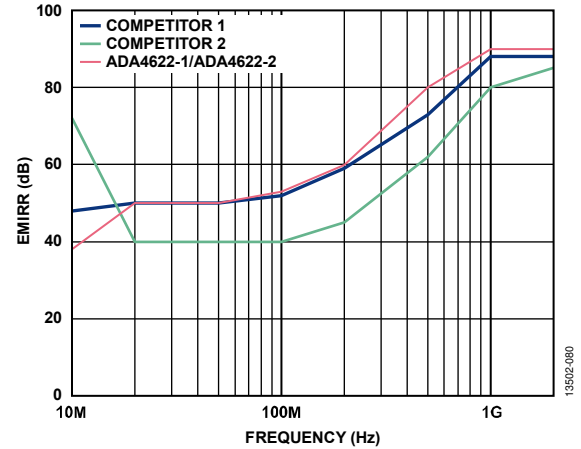

Figure 84. EMIRR vs. Frequency

OUTPUT CHARACTERISTICS

The [ADA4622-1](#)/[ADA4622-2](#) unique bipolar rail-to-rail output stage swings within 10 mV of the supplies with no external resistive load.

The [ADA4622-1](#)/[ADA4622-2](#) approximate output saturation resistance is 24 Ω, sourcing or sinking. Use the output impedance to estimate the output saturation voltage when driving heavier loads. As an example, when driving 5 mA, the saturation voltage from either rail is roughly 120 mV.

If the [ADA4622-1](#)/[ADA4622-2](#) output drives hard against the output saturation voltage, it recovers within 1.2 μs of the input, returning to the linear operating region of the amplifier (see Figure 55 and Figure 58).

Capacitive Load Drive Capability

Direct capacitive loads interact with the effective output impedance of the [ADA4622-1](#)/[ADA4622-2](#) to form an additional pole in the feedback loop of the amplifiers, which causes excessive peaking on the pulse response or loss of stability. The worst case condition is when the devices use a single 5 V supply in a unity-gain configuration. Figure 85 shows the pulse response of the [ADA4622-1](#)/[ADA4622-2](#) driving 500 pF directly.
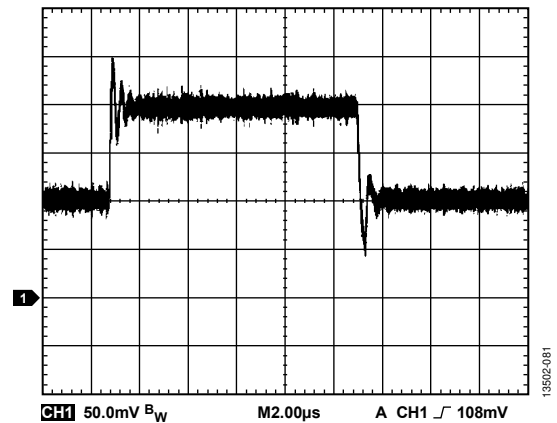

Figure 85. Pulse Response with 500 pF Load Capacitance