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Ultralow Power, Low Distortion, Fully Differential ADC Drivers

Data Sheet

ADA4940-1/ADA4940-2

FEATURES

- Small signal bandwidth: 260 MHz
- Ultralow power 1.25mA
- Extremely low harmonic distortion
  - −122 dB THD at 50 kHz
  - −96 dB THD at 1 MHz
- Low input voltage noise: 3.9 nV/√Hz
- 0.35 mV maximum offset voltage
- Balanced outputs
- Settling time to 0.1%: 34 ns
- Rail-to-rail output: $-V_S$ + 0.1 V to $+V_S$ − 0.1 V
- Adjustable output common-mode voltage
- Flexible power supplies: 3 V to 7 V (LFCSP)
- Disable pin to reduce power consumption
- ADA4940-1 is available in LFCSP and SOIC packages

APPLICATIONS

- Low power PulSAR®/SAR ADC drivers
- Single-ended-to-differential conversion
- Differential buffers
- Line drivers
- Medical imaging
- Industrial process controls
- Portable electronics

GENERAL DESCRIPTION

The ADA4940-1/ADA4940-2 are low noise, low distortion fully differential amplifiers with very low power consumption. They are an ideal choice for driving low power, high resolution, high performance SAR and Σ-Δ analog-to-digital converters (ADCs) with resolutions up to 16 bits from dc to 1 MHz on only 1.25 mA of quiescent current. The adjustable level of the output common-mode voltage allows the ADA4940-1/ADA4940-2 to match the input common-mode voltage of multiple ADCs. The internal common-mode feedback loop provides exceptional output balance, as well as suppression of even-order harmonic distortion products.

With the ADA4940-1/ADA4940-2, differential gain configurations are easily realized with a simple external feedback network of four resistors determining the closed-loop gain of the amplifier. The ADA4940-1/ADA4940-2 are fabricated using Analog Devices, Inc., SiGe complementary bipolar process, enabling them to achieve very low levels of distortion with an input voltage noise of only 3.9 nV/√Hz. The low dc offset and excellent dynamic performance of the ADA4940-1/ADA4940-2 make them well suited for a variety of data acquisition and signal processing applications.

FUNCTIONAL BLOCK DIAGRAMS

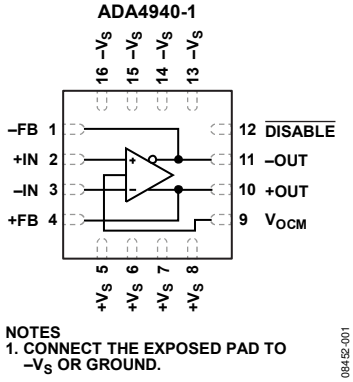

Figure 1. ADA4940-1

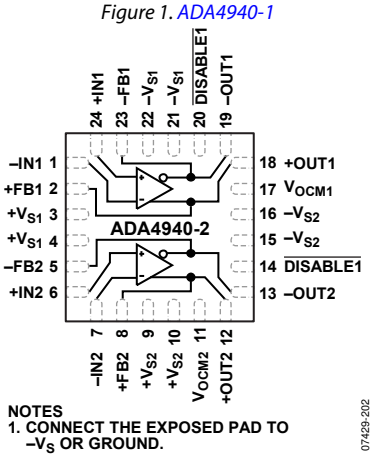

Figure 2. ADA4940-2

The ADA4940-1 is available in a 3 mm × 3 mm, 16-lead LFCSP and an 8-lead SOIC. The ADA4940-2 is available in a 4 mm × 4 mm, 24-lead LFCSP. The pinouts are optimized to facilitate printed circuit board (PCB) layout and minimize distortion. The ADA4940-1/ADA4940-2 are specified to operate over the −40°C to +125°C temperature range.

Table 1. Similar Products to ADA4940-1/ADA4940-2

Product	I_{SUPPLY} (mA)	Bandwidth (MHz)	Slew Rate (V/µs)	Noise (nV/√Hz)
AD8137	3	110	450	8.25
ADA4932-1	9	560	2800	3.6
ADA4941-1	2.2	31	22	5.1

Table 2. Complementary Products to ADA4940-1/ADA4940-2

Product	Power (mW)	Throughput (MSPS)	Resolution (Bits)	SNR (dB)
AD7982	7.0	1	18	98
AD7984	10.5	1.333	18	96.5
AD7621	65	3	16	88
AD7623	45	1.333	16	88

Rev. D
Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

5/2016—Rev. C to Rev. D

Changes to Figure 1 1
Deleted Figure 2 1
Added Figure 2; Renumbered Sequentially 1
Updated Outline Dimensions 29
Changes to Ordering Guide 30

9/2013—Rev. B to Rev. C

Updated Outline Dimensions 30
Changes to Ordering Guide 31

3/2012—Rev. A to Rev. B

Reorganized Layout ..... Universal
Added ADA4940-1 8-Lead SOIC Package ..... Universal
Changes to Features Section, Table 1, and Figure 1; Replaced Figure 2 1
Changed V_S = ±2 V(or +5 V) Section to V_S = +5 V Section 3
Changes to V_S = +5 V Section and Table 3 3
Changes to Table 4 and Table 5 4
Changes to V_S = 3 V Section and Table 6 5
Changes to Table 7 and Table 8 6
Added Figure 5 and Table 12, Renumbered Sequentially 9
Changes to Figure 7, Figure 8, and Figure 9 10
Added Figure 15 and Figure 18; Changes to Figure 13, Figure 14, and Figure 16 11
Changes to Figure 19 and Figure 20 12
Changes to Figure 25, Figure 26, and Figure 27; Added Figure 28, Figure 29, and Figure 30 13
Changes to Figure 31, Figure 32, Figure 33, Figure 34, Figure 35, and Figure 36 14
Changes to Figure 37, Figure38, Figure 39, and Figure 41 15
Changes to Figure 49, Figure 50, and Figure 51 17
Added Figure 55 and Figure 57 18
Changes to Differential V_{OS}, Differential CMRR, and V_{OCM} CMRR Section 20
Changes to Calculating the Input Impedance of an Application Circuit Section 23
Changes to Figure 71 25
Changes to Driving a High Precision ADC Section and Figure 73 26
Changed ADA4940-1 Example Section to ADA4940-1 LFCSP Example Section 27
Changes to Ordering Guide 29

12/2011—Rev. 0 to Rev. A

Changes to Features Section, General Description Section, and Table 1 1
Replaced Figure 1 and Figure 2 1
Changes to V_S = ±2.5 V (or +5 V) Section and Table 3 3
Changes to Table 6 5
Replaced Figure 7, Figure 8, Figure 9, and Figure 10 9
Replaced Figure 14, Figure 15, and Figure 17 10
Replaced Figure 24 and Figure 27 12
Changes to Figure 37 14
Replaced Figure 43 and Figure 46 15
Replaced Figure 53 18
Changes to Estimating the Output Noise Voltage Section, Table 14, Table 15, and Calculating the Input Impedance of an Application Circuit Section 21
Changes to Input Common-Mode Voltage Range Section 22
Changes to Driving a High Precision ADC Section and Figure 65 24

10/2011—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V

V_{OCM} = midsupply, R_F = R_G = 1 kΩ, $R_{L, dm}$ = 1 kΩ, T_A = 25°C, LFCSP package, unless otherwise noted. T_{MIN} to T_{MAX} = −40°C to +125°C. (See Figure 61 for the definition of terms.)

+D_{IN} or −D_{IN} to $V_{OUT, dm}$ Performance

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	$V_{OUT, dm}$ = 0.1 V p-p, G = 1		260		MHz
	$V_{OUT, dm}$ = 0.1 V p-p, G = 2		220		MHz
	$V_{OUT, dm}$ = 0.1 V p-p, G = 5		75		MHz
−3 dB Large Signal Bandwidth	$V_{OUT, dm}$ = 2 V p-p, G = 1		25		MHz
	$V_{OUT, dm}$ = 2 V p-p, G = 2		22		MHz
	$V_{OUT, dm}$ = 2 V p-p, G = 5		19		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT, dm}$ = 2 V p-p, G = 1 and G = 2		14.5		MHz
Slew Rate	$V_{OUT, dm}$ = 2 V step		95		V/µs
Settling Time to 0.1%	$V_{OUT, dm}$ = 2 V step		34		ns
Overdrive Recovery Time	G = 2, $V_{IN, dm}$ = 6 V p-p, triangle wave		86		ns
NOISE/HARMONIC PERFORMANCE					
HD2/HD3	$V_{OUT, dm}$ = 2 V p-p, f_C = 10 kHz		−125/−118		dBc
	$V_{OUT, dm}$ = 2 V p-p, f_C = 50 kHz		−123/−126		dBc
	$V_{OUT, dm}$ = 2 V p-p, f_C = 50 kHz, G = 2		−124/−117		dBc
	$V_{OUT, dm}$ = 2 V p-p, f_C = 1 MHz		−102/−96		dBc
	$V_{OUT, dm}$ = 2 V p-p, f_C = 1 MHz, G = 2		−100/−92		dBc
IMD3	$V_{OUT, dm}$ = 2 V p-p, f_1 = 1.9 MHz, f_2 = 2.1 MHz		−99		dBc
Input Voltage Noise	f = 100 kHz		3.9		nV/√Hz
Input Current Noise	f = 100 kHz		0.81		pA/√Hz
Crosstalk	$V_{OUT, dm}$ = 2 V p-p, f_C = 1 MHz		−110		dB
INPUT CHARACTERISTICS					
Input Offset Voltage	V_{IP} = V_{IN} = V_{OCM} = 0 V	−0.35	±0.06	+0.35	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		1.2		µV/°C
Input Bias Current		−1.6	−1.1		µA
Input Bias Current Drift	T_{MIN} to T_{MAX}		−4.5		nA/°C
Input Offset Current		−500	±50	+500	nA
Input Common-Mode Voltage Range			$-V_S$ − 0.2 to $+V_S$ − 1.2		V
Input Resistance	Differential		33		kΩ
	Common mode		50		MΩ
Input Capacitance			1		pF
Common-Mode Rejection Ratio (CMRR)	$\Delta V_{OS, dm}/\Delta V_{IN, cm}$, $\Delta V_{IN, cm}$ = ±1 V dc	86	119		dB
Open-Loop Gain		91	99		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Each single-ended output	$-V_S$ + 0.1 to $+V_S$ − 0.1	$-V_S$ + 0.07 to $+V_S$ − 0.07		V
Linear Output Current	f = 1 MHz, $R_{L, dm}$ = 22 Ω, SFDR = −60 dBc		46		mA peak
Output Balance Error	f = 1 MHz, $\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$		−65	−60	dB

V_{OCM} to $V_{OUT, cm}$ Performance

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	$V_{OUT, cm}$ = 0.1 V p-p		36		MHz
−3 dB Large Signal Bandwidth	$V_{OUT, cm}$ = 1 V p-p		29		MHz
Slew Rate	$V_{OUT, cm}$ = 1 V p-p		52		V/µs
Input Voltage Noise	f = 100 kHz		83		nV/√Hz
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V	0.99	1	1.01	V/V
V_{OCM} CHARACTERISTICS					
Input Common-Mode Voltage Range			$-V_S + 0.8$ to $+V_S - 0.7$		V
Input Resistance			250		kΩ
Offset Voltage	$V_{OS, cm} = V_{OUT, cm} - V_{OCM}$; $V_{IP} = V_{IN} = V_{OCM}$ = 0 V	−6	±1	+6	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		20		µV/°C
Input Bias Current		−7	+4	+7	µA
CMRR	$\Delta V_{OS, dm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V	86	100		dB

General Performance

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range	LFCSP	3		7	V
	SOIC	3		6	V
Quiescent Current per Amplifier	Enabled	1.05	1.25	1.38	mA
Quiescent Current Drift	T_{MIN} to T_{MAX}		4.25		µA/°C
	Disabled		13.5	28.5	µA
+PSRR	$\Delta V_{OS, dm}/\Delta V_S$, ΔV_S = 1 V p-p	80	90		dB
−PSRR	$\Delta V_{OS, dm}/\Delta V_S$, ΔV_S = 1 V p-p	80	96		dB
DISABLE ($\overline{\text{DISABLE}}$ PIN)					
$\overline{\text{DISABLE}}$ Input Voltage	Disabled		$\leq(-V_S + 1)$		V
	Enabled		$\geq(-V_S + 1.8)$		V
Turn-Off Time			10		µs
Turn-On Time			0.6		µs
$\overline{\text{DISABLE}}$ Pin Bias Current per Amplifier					
Enabled	$\overline{\text{DISABLE}}$ = +2.5 V		2	5	µA
Disabled	$\overline{\text{DISABLE}}$ = −2.5 V	−10	−5		µA
OPERATING TEMPERATURE RANGE		−40		+125	°C

V_S = 3 V

V_{OCM} = midsupply, $R_F = R_G$ = 1 kΩ, $R_{L, dm}$ = 1 kΩ, T_A = 25°C, LFCSP package, unless otherwise noted. T_{MIN} to T_{MAX} = −40°C to +125°C. (See Figure 61 for the definition of terms.)

+D_{IN} or −D_{IN} to $V_{OUT, dm}$ Performance

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	$V_{OUT, dm}$ = 0.1 V p-p		240		MHz
	$V_{OUT, dm}$ = 0.1 V p-p, G = 2		200		MHz
	$V_{OUT, dm}$ = 0.1 V p-p, G = 5		70		MHz
−3 dB Large Signal Bandwidth	$V_{OUT, dm}$ = 2 V p-p		24		MHz
	$V_{OUT, dm}$ = 2 V p-p, G = 2		20		MHz
	$V_{OUT, dm}$ = 2 V p-p, G = 5		17		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT, dm}$ = 0.1 V p-p		14		MHz
Slew Rate	$V_{OUT, dm}$ = 2 V step		90		V/µs
Settling Time to 0.1%	$V_{OUT, dm}$ = 2 V step		37		ns
Overdrive Recovery Time	G = 2, $V_{IN, dm}$ = 3.6 V p-p, triangle wave		85		ns
NOISE/HARMONIC PERFORMANCE					
HD2/HD3	$V_{OUT, dm}$ = 2 V p-p, f_C = 50 kHz (HD2/HD3)		−115/−121		dBc
	$V_{OUT, dm}$ = 2 V p-p, f_C = 1 MHz (HD2/HD3)		−104/−96		dBc
IMD3	$V_{OUT, dm}$ = 2 V p-p, f_1 = 1.9 MHz, f_2 = 2.1 MHz		−98		dBc
Input Voltage Noise	f = 100 kHz		3.9		nV/√Hz
Input Current Noise	f = 100 kHz		0.84		pA/√Hz
Crosstalk	$V_{OUT, dm}$ = 2 V p-p, f_C = 1 MHz		−110		dB
INPUT CHARACTERISTICS					
Input Offset Voltage	$V_{IP} = V_{IN} = V_{OCM}$ = 1.5 V	−0.4	±0.06	+0.4	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		1.2		µV/°C
Input Bias Current		−1.6	−1.1		µA
Input Bias Current Drift	T_{MIN} to T_{MAX}		−4.5		nA/°C
Input Offset Current		−500	±50	+500	nA
Input Common-Mode Voltage Range			$-V_S - 0.2$ to $+V_S - 1.2$		V
Input Resistance	Differential		33		kΩ
	Common mode		50		MΩ
Input Capacitance			1		pF
Common-Mode Rejection Ratio (CMRR)	$\Delta V_{OS, dm}/\Delta V_{IN, cm}$, $\Delta V_{IN, cm}$ = ±0.25 V dc	86	114		dB
Open-Loop Gain		91	99		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Each single-ended output	$-V_S + 0.08$ to $+V_S - 0.08$	$-V_S + 0.04$ to $+V_S - 0.04$		V
Linear Output Current	f = 1 MHz, $R_{L, dm}$ = 26 Ω, SFDR = −60 dBc		38		mA peak
Output Balance Error	f = 1 MHz, $\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$		−65	−60	dB

V_{OCM} to $V_{OUT, cm}$ Performance

Table 7.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	$V_{OUT, cm}$ = 0.1 V p-p		36		MHz
−3 dB Large Signal Bandwidth	$V_{OUT, cm}$ = 1 V p-p		26		MHz
Slew Rate	$V_{OUT, cm}$ = 1 V p-p		48		V/µs
Input Voltage Noise	f = 100 kHz		92		nV/√Hz
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$, ΔV_{OCM} = ±0.25 V	0.99	1	1.01	V/V
V_{OCM} CHARACTERISTICS					
Input Common-Mode Voltage Range			$-V_S + 0.8$ to $+V_S - 0.7$		V
Input Resistance			250		kΩ
Offset Voltage	$V_{OS, cm} = V_{OUT, cm} - V_{OCM}$; $V_{IP} = V_{IN} = V_{OCM}$ = 1.5 V	−7	±1	+7	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		20		µV/°C
Input Bias Current		−5	+1	+5	µA
CMRR	$\Delta V_{OS,dm}/\Delta V_{OCM}$, ΔV_{OCM} = ±0.25 V	80	100		dB

General Performance

Table 8.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range	LFCSP	3		7	V
	SOIC	3		6	V
Quiescent Current per Amplifier	Enabled	1	1.18	1.33	mA
	T_{MIN} to T_{MAX}		4.25		µA/°C
	Disabled		7	22	µA
+PSRR	$\Delta V_{OS, dm}/\Delta V_S$, ΔV_S = 0.25 V p-p	80	90		dB
−PSRR	$\Delta V_{OS, dm}/\Delta V_S$, ΔV_S = 0.25 V p-p	80	96		dB
DISABLE ($\overline{\text{DISABLE}}$ PIN)					
$\overline{\text{DISABLE}}$ Input Voltage	Disabled		$\leq(-V_S + 1)$		V
	Enabled		$\geq(-V_S + 1.8)$		V
Turn-Off Time			16		µs
Turn-On Time			0.6		µs
$\overline{\text{DISABLE}}$ Pin Bias Current per Amplifier					
Enabled	$\overline{\text{DISABLE}}$ = +3 V		0.3	1	µA
Disabled	$\overline{\text{DISABLE}}$ = 0 V	−6	−3		µA
OPERATING TEMPERATURE RANGE		−40		+125	°C

ABSOLUTE MAXIMUM RATINGS

Table 9.

Parameter	Rating
Supply Voltage	8 V
V_{OCM}	$\pm V_S$
Differential Input Voltage	1.2 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C
ESD	
Field Induced Charged Device Model (FICDM)	1250 V
Human Body Model (HBM)	2000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for the device soldered on a circuit board in still air.

Table 10.

Package Type	θ_{JA}	Unit
8-Lead SOIC (Single)/4-Layer Board	158	°C/W
16-Lead LFCSP (Single)/4-Layer Board	91.3	°C/W
24-Lead LFCSP (Dual)/4-Layer Board	65.1	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADA4940-1/ADA4940-2 packages is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4940-1/ADA4940-2. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power dissipation is the voltage between the supply pins ($\pm V_S$) times the quiescent current (I_S). The load current consists of the differential and common-mode currents flowing to the load, as well as currents flowing through the external feedback networks and internal common-mode feedback loop. The internal resistor tap used in the common-mode feedback loop places a negligible differential load on the output. Consider rms voltages and currents when dealing with ac signals.

Airflow reduces θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 8-lead SOIC (θ_{JA} = 158°C/W, single) the 16-lead LFCSP (θ_{JA} = 91.3°C/W, single) and 24-lead LFCSP (θ_{JA} = 65.1°C/W, dual) packages on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

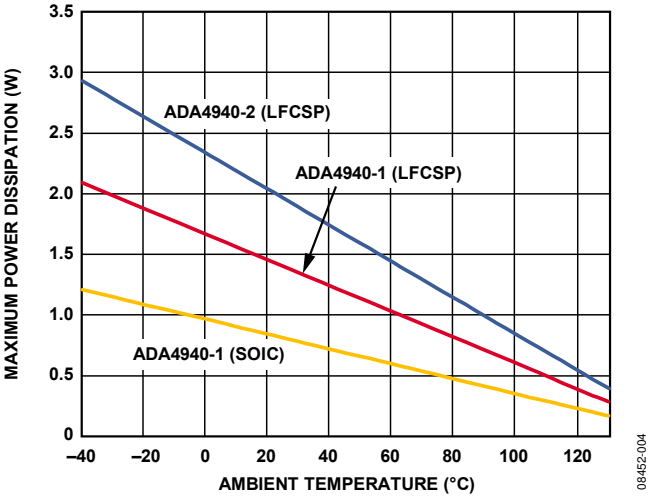

Figure 3. Maximum Safe Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

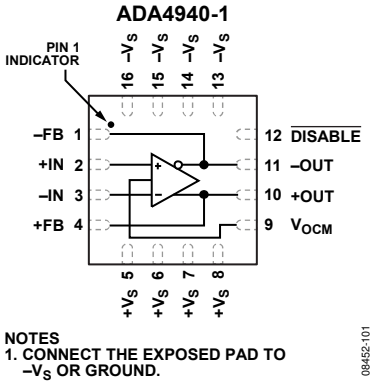

Figure 4. ADA4940-1 Pin Configuration (16-Lead LFCSP)

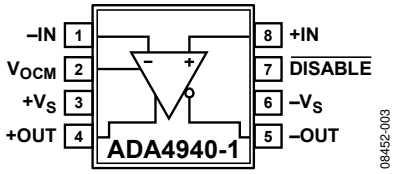

Figure 5. ADA4940-1 Pin Configuration (8-Lead SOIC)

Table 11. ADA4940-1 Pin Function Descriptions (16-Lead LFCSP)

Pin No.	Mnemonic	Description
1	−FB	Negative Output for Feedback Component Connection.
2	+IN	Positive Input Summing Node.
3	−IN	Negative Input Summing Node.
4	+FB	Positive Output for Feedback Component Connection.
5 to 8	$+V_S$	Positive Supply Voltage.
9	V_{OCM}	Output Common-Mode Voltage.
10	+OUT	Positive Output for Load Connection.
11	−OUT	Negative Output for Load Connection.
12	$\overline{\text{DISABLE}}$	Disable Pin.
13 to 16	$-V_S$	Negative Supply Voltage.
	Exposed pad (EPAD)	Connect the exposed pad to $-V_S$ or ground.

Table 12. ADA4940-1 Pin Function Descriptions (8-Lead SOIC)

Pin No.	Mnemonic	Description
1	−IN	Negative Input Summing Node
2	V_{OCM}	Output Common-Mode Voltage
3	$+V_S$	Positive Supply Voltage
4	+OUT	Positive Output for Load Connection
5	−OUT	Negative Output for Load Connection
6	$-V_S$	Negative Supply Voltage
7	$\overline{\text{DISABLE}}$	Disable Pin
8	+IN	Positive Input Summing Node

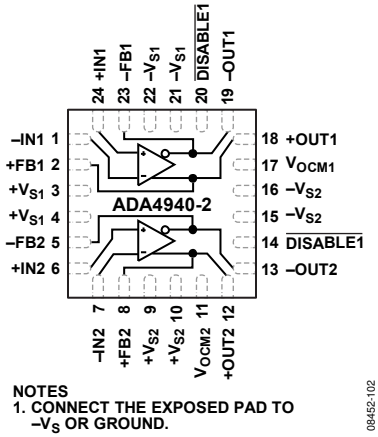

Figure 6. ADA4940-2 Pin Configuration (24-Lead LFCSP)

Table 13. ADA4940-2 Pin Function Descriptions (24-Lead LFCSP)

Pin No.	Mnemonic	Description
1	–IN1	Negative Input Summing Node 1.
2	+FB1	Positive Output Feedback Pin 1.
3, 4	$+V_{S1}$	Positive Supply Voltage 1.
5	–FB2	Negative Output Feedback Pin 2.
6	+IN2	Positive Input Summing Node 2.
7	–IN2	Negative Input Summing Node 2.
8	+FB2	Positive Output Feedback Pin 2.
9, 10	$+V_{S2}$	Positive Supply Voltage 2.
11	V_{OCM2}	Output Common-Mode Voltage 2.
12	+OUT2	Positive Output 2.
13	–OUT2	Negative Output 2.
14	$\overline{\text{DISABLE2}}$	Disable Pin 2.
15, 16	$-V_{S2}$	Negative Supply Voltage 2.
17	V_{OCM1}	Output Common-Mode Voltage 1.
18	+OUT1	Positive Output 1.
19	–OUT1	Negative Output 1.
20	$\overline{\text{DISABLE1}}$	Disable Pin 1.
21, 22	$-V_{S1}$	Negative Supply Voltage 1.
23	–FB1	Negative Output Feedback Pin 1.
24	+IN1	Positive Input Summing Node 1.
	Exposed pad (EPAD)	Connect the exposed pad to $-V_S$ or ground.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±2.5 V, G = 1, R_F = R_G = 1 kΩ, R_T = 52.3 Ω (when used), R_L = 1 kΩ, unless otherwise noted. See Figure 59 and Figure 60 for the test circuits.

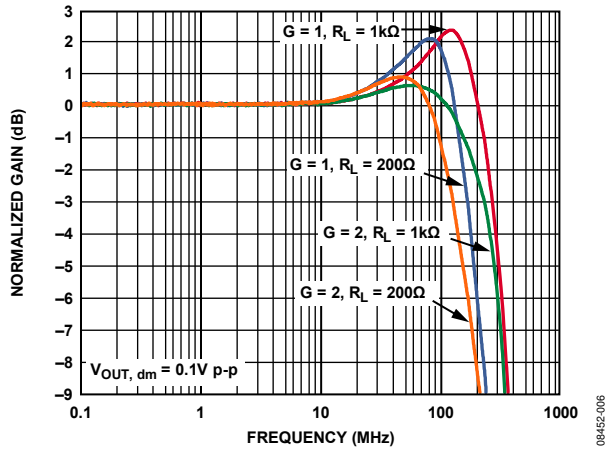

Figure 7. Small Signal Frequency Response for Various Gains and Loads (LFCSP)

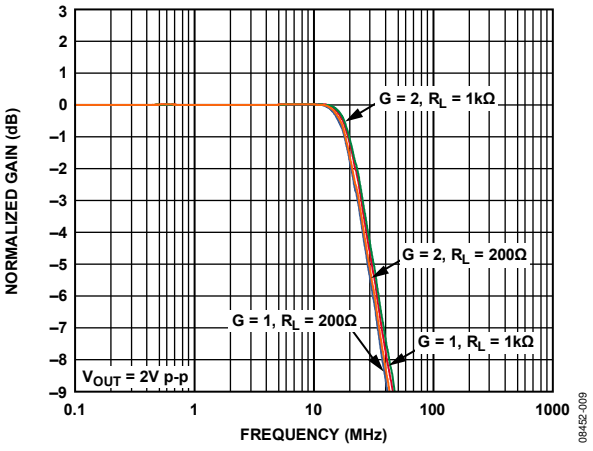

Figure 10. Large Signal Frequency Response for Various Gains and Loads

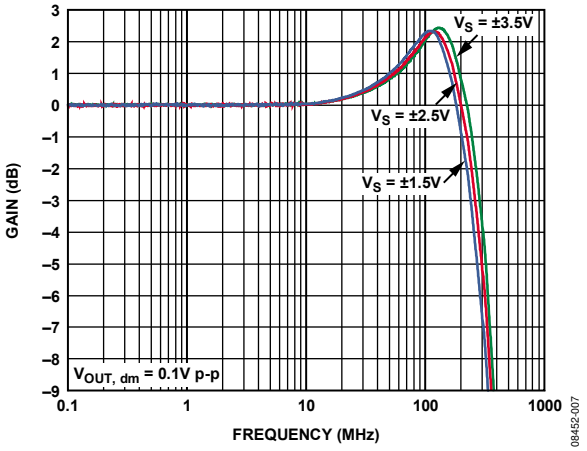

Figure 8. Small Signal Frequency Response for Various Supplies (LFCSP)

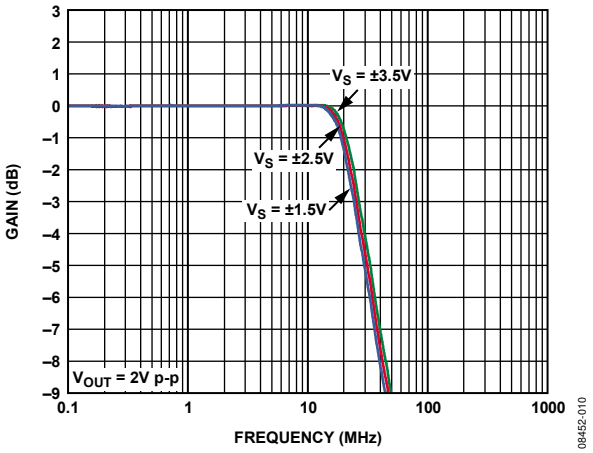

Figure 11. Large Signal Frequency Response for Various Supplies

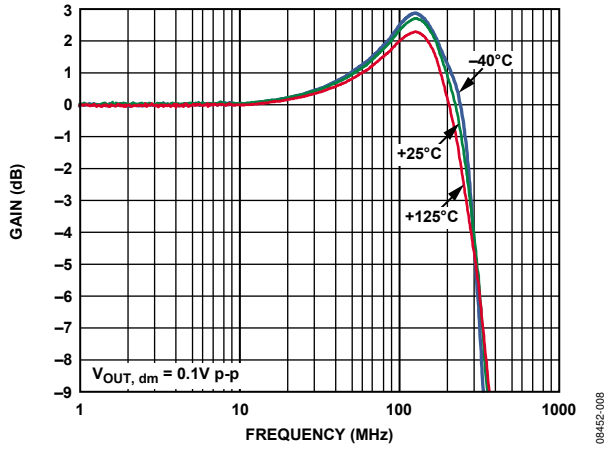

Figure 9. Small Signal Frequency Response for Various Temperatures (LFCSP)

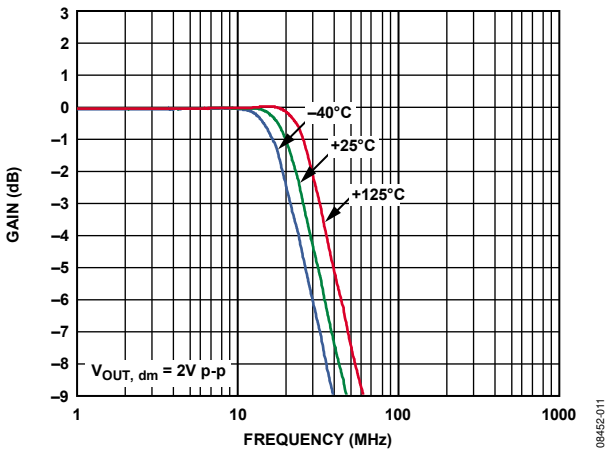

Figure 12. Large Signal Frequency Response for Various Temperatures

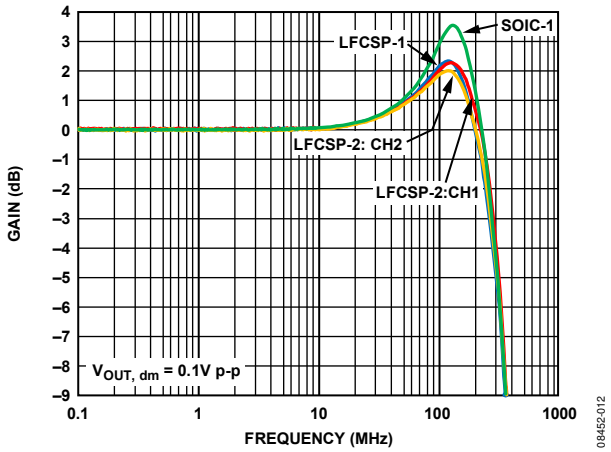

Figure 13. Small Signal Frequency Response for Various Packages

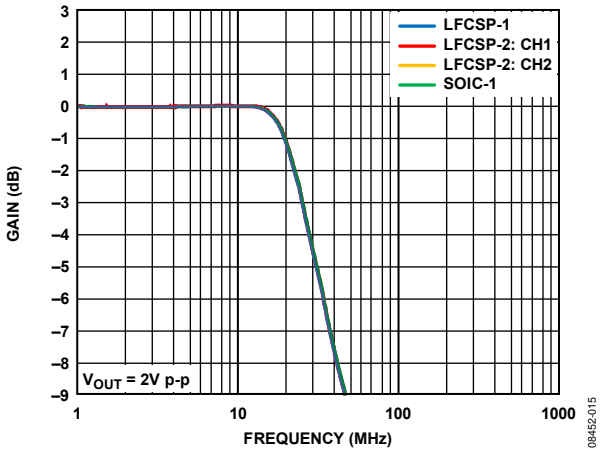

Figure 16. Large Signal Frequency Response for Various Packages

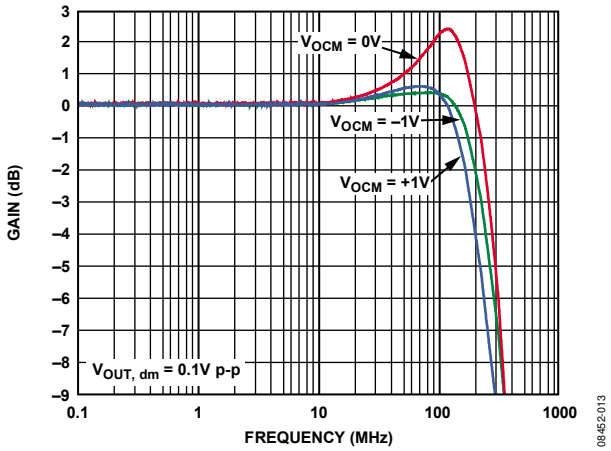

Figure 14. Small Signal Frequency Response at Various V_{OCM} Levels (LFCSP)

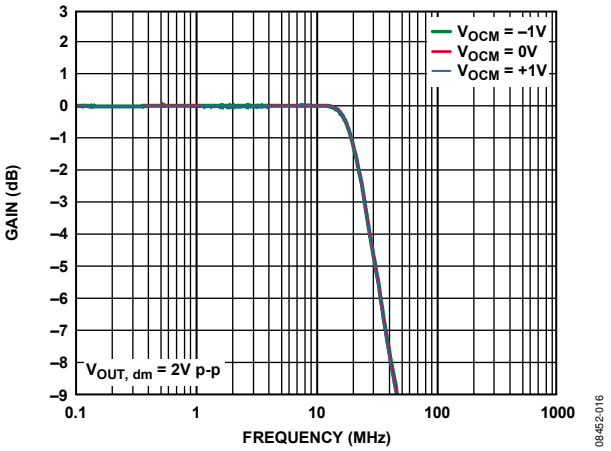

Figure 17. Large Signal Frequency Response at Various V_{OCM} Levels

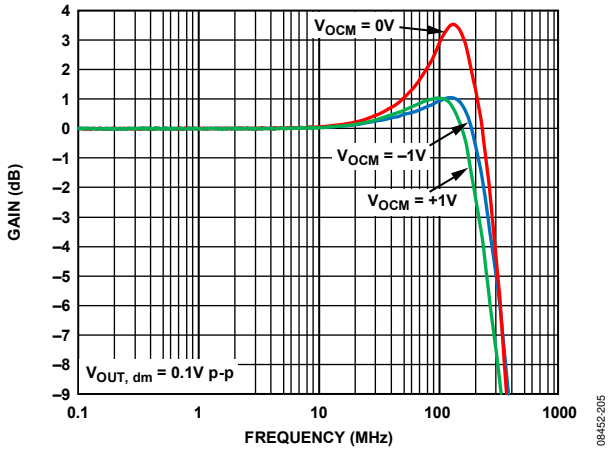

Figure 15. Small Signal Frequency Response for Various V_{OCM} (SOIC)

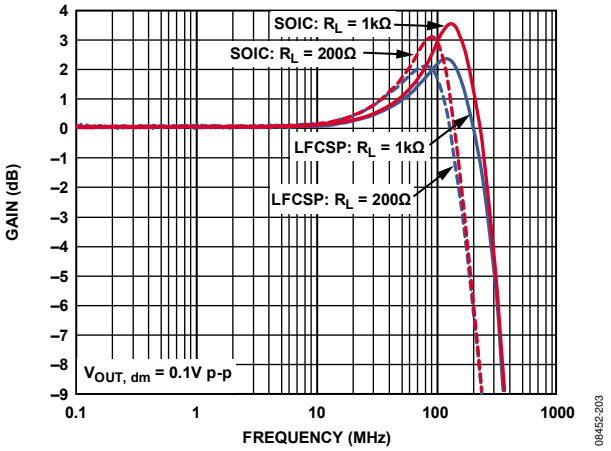

Figure 18. Small Signal Frequency Response for Various Packages and Loads

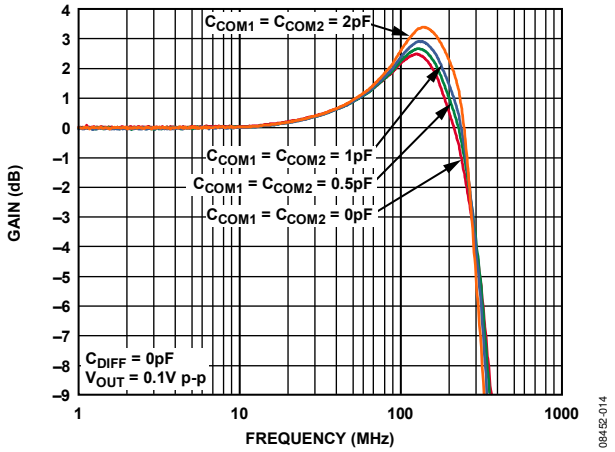

Figure 19. Small Signal Frequency Response for Various Capacitive Loads (LFCSP)

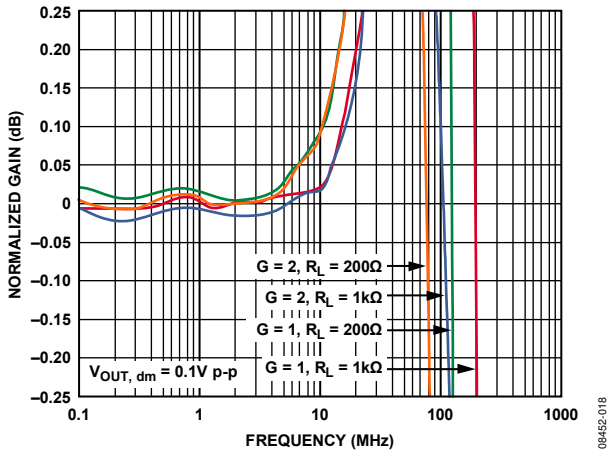

Figure 20. 0.1 dB Flatness Small Signal Frequency Response for Various Gains and Loads (LFCSP)

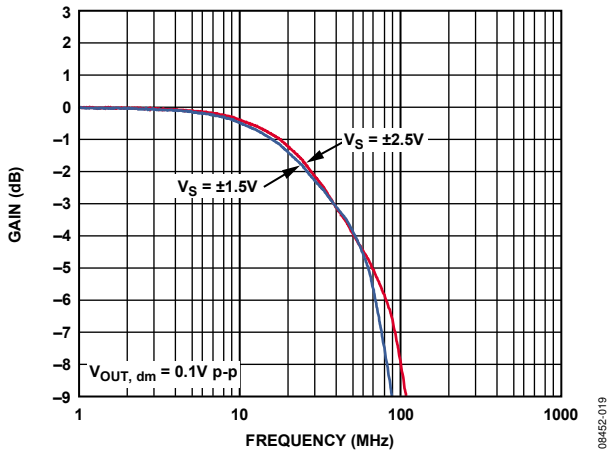

Figure 21. V_{OCM} Small Signal Frequency Response for Various Supplies

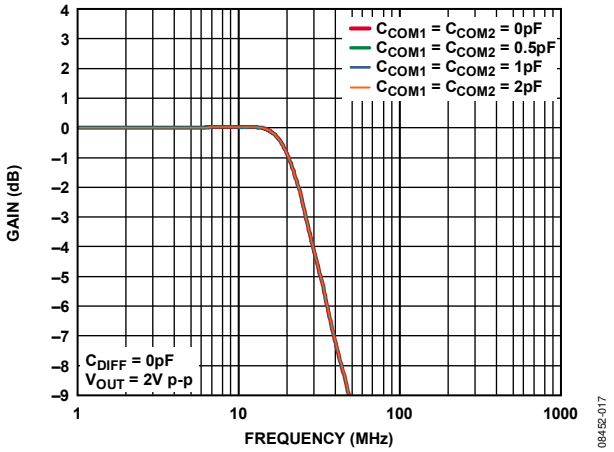

Figure 22. Large Signal Frequency Response for Various Capacitive Loads

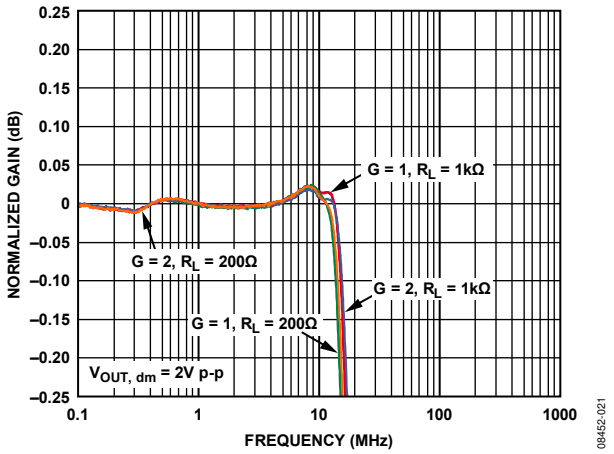

Figure 23. 0.1 dB Flatness Large Signal Frequency Response for Various Gains and Loads

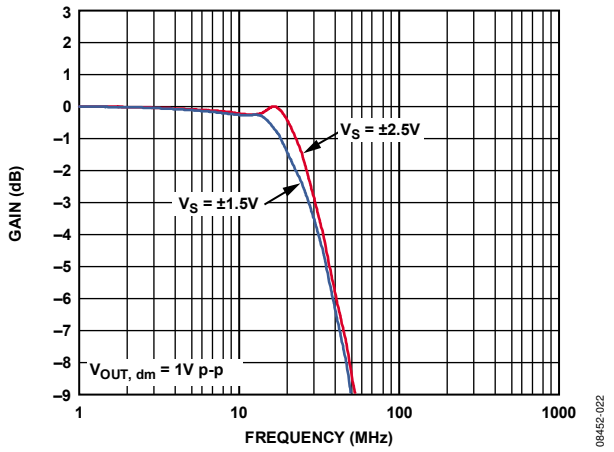

Figure 24. V_{OCM} Large Signal Frequency Response for Various Supplies

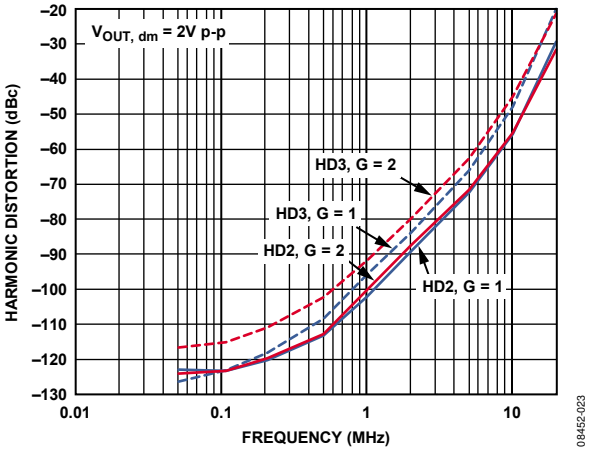

Figure 25. Harmonic Distortion vs. Frequency for Various Gains (LFCSP)

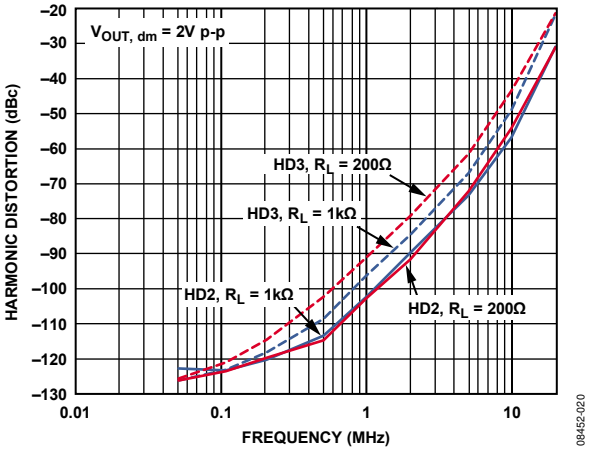

Figure 26. Harmonic Distortion vs. Frequency for Various Loads (LFCSP)

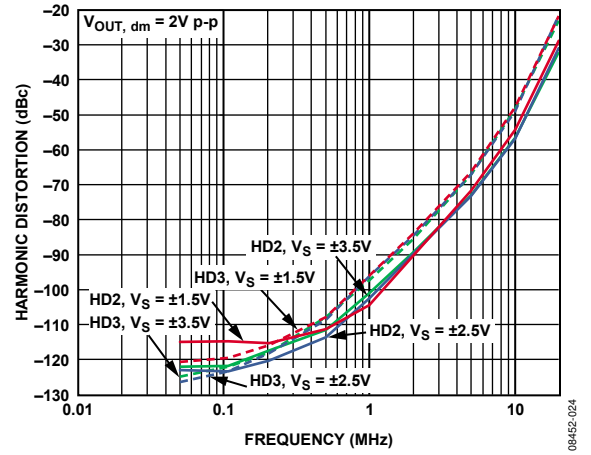

Figure 27. Harmonic Distortion vs. Frequency for Various Supplies (LFCSP)

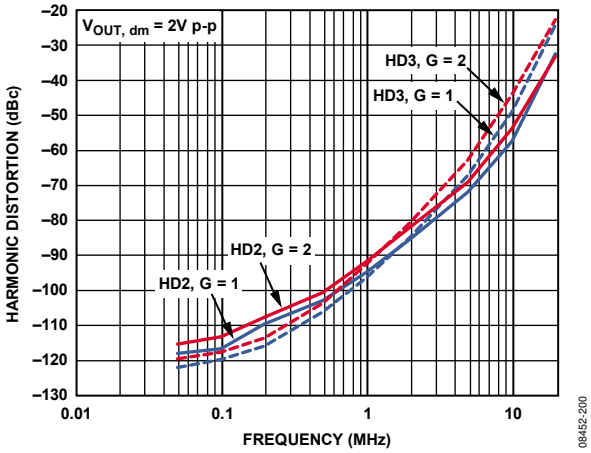

Figure 28. Harmonic Distortion vs. Frequency vs. Gain (SOIC)

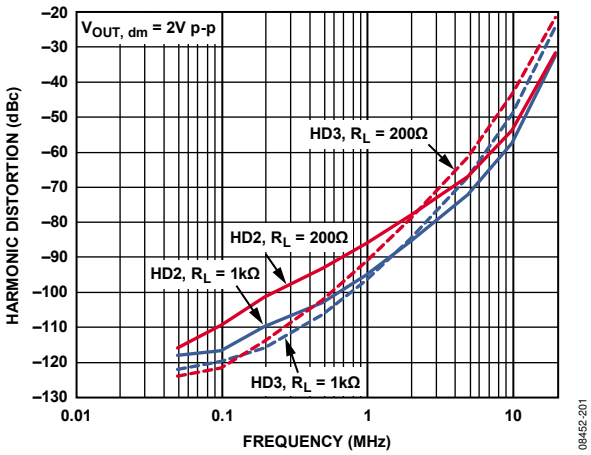

Figure 29. Harmonic Distortion vs. Frequency for Various Loads (SOIC)

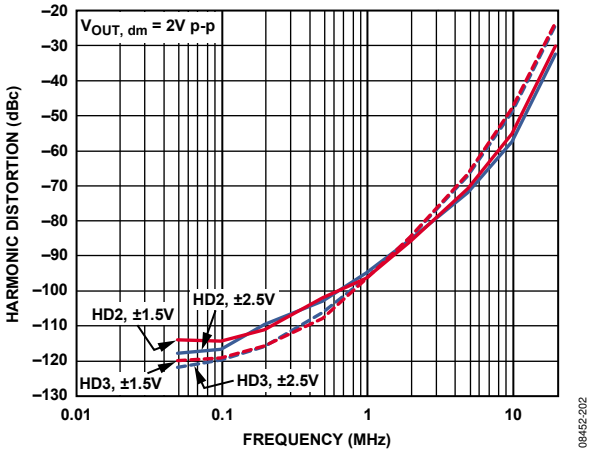

Figure 30. Harmonic Distortion vs. Frequency for Various Supplies (SOIC)

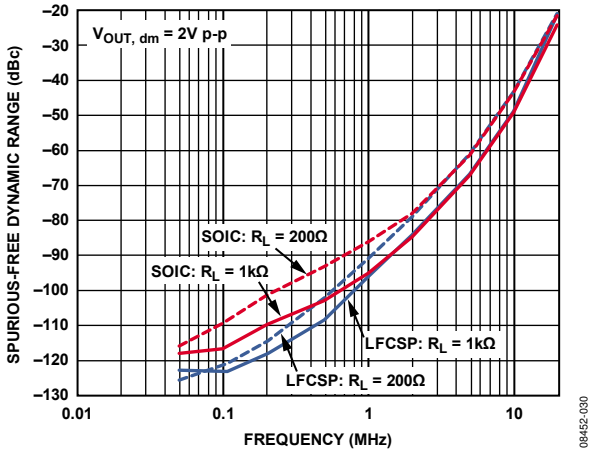

Figure 31. Spurious-Free Dynamic Range vs. Frequency at R_L = 200 Ω and R_L = 1 kΩ

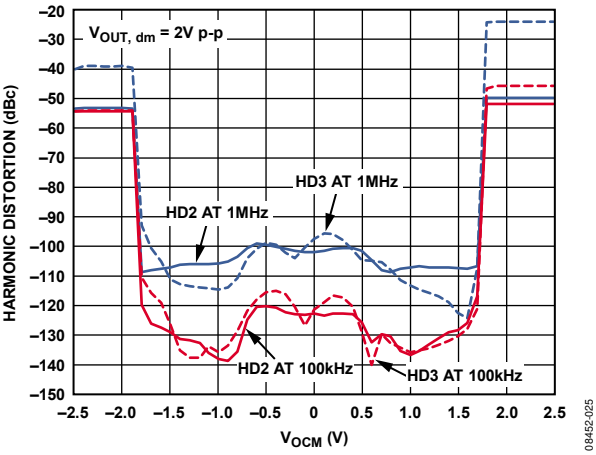

Figure 32. Harmonic Distortion vs. V_{OCM} for 100 kHz and 1 MHz, ±2.5 V Supplies (LFCSP)

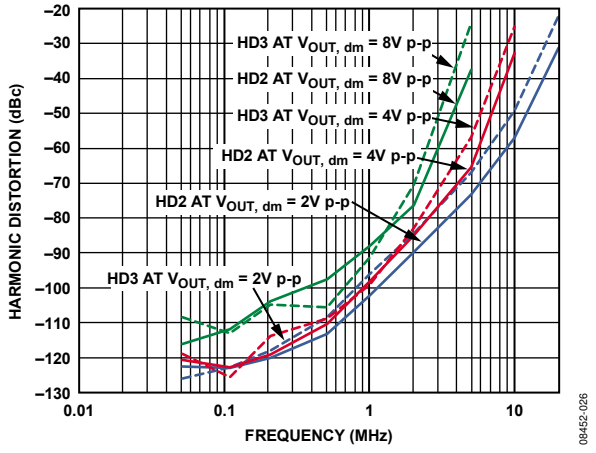

Figure 33. Harmonic Distortion vs. Frequency for Various $V_{OUT, dm}$ (LFCSP)

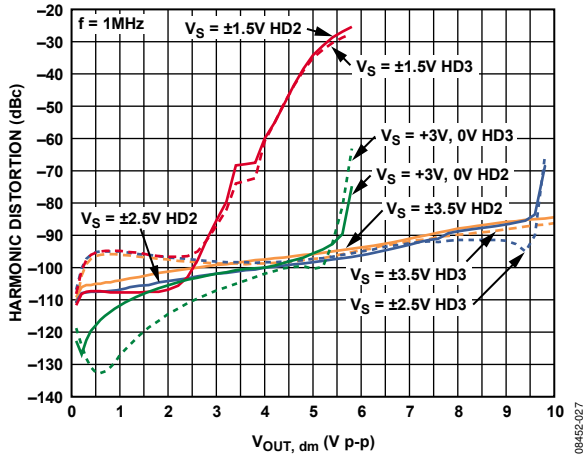

Figure 34. Harmonic Distortion vs. $V_{OUT, dm}$ for Various Supplies, f = 1 MHz (LFCSP)

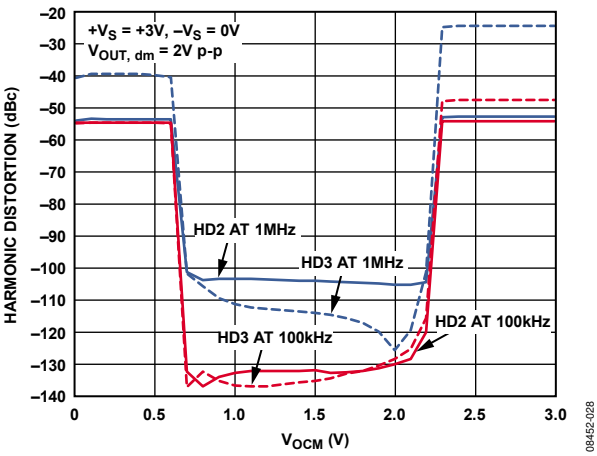

Figure 35. Harmonic Distortion vs. V_{OCM} for 100 kHz and 1 MHz, 3 V Supply (LFCSP)

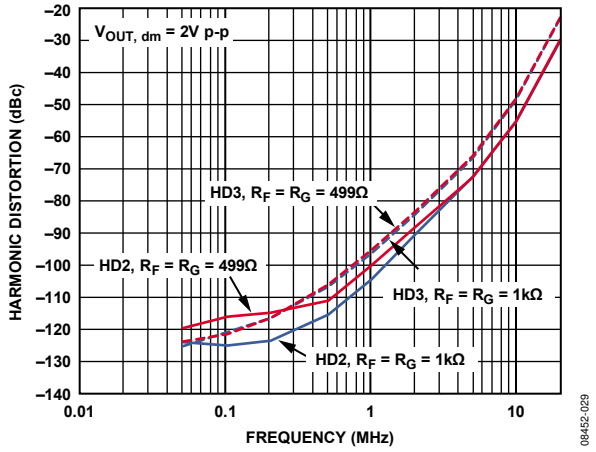

Figure 36. Harmonic Distortion vs. Frequency for Various R_F and R_G (LFCSP)

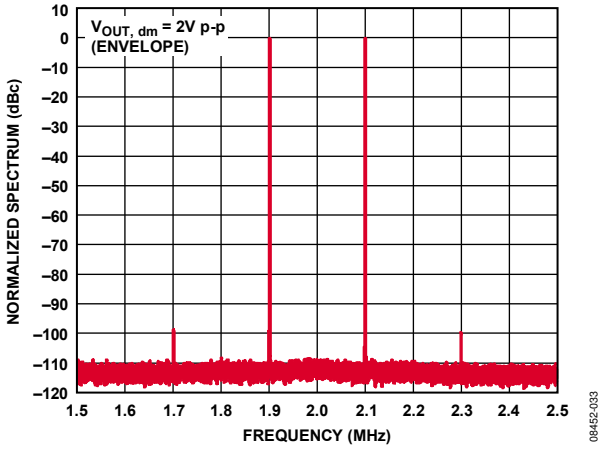

Figure 37. 2 MHz Intermodulation Distortion (LFCSP)

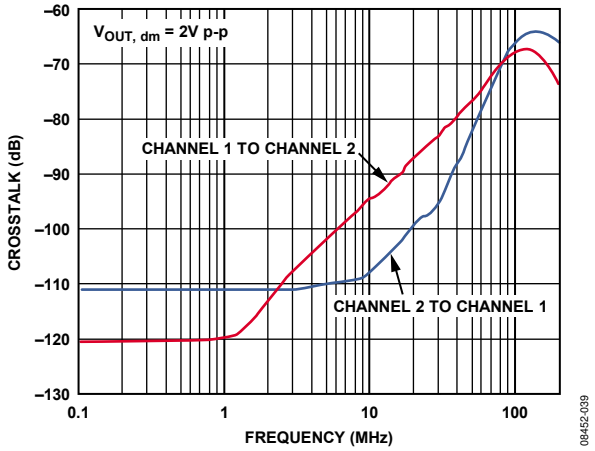

Figure 40. Crosstalk vs. Frequency, ADA4940-2

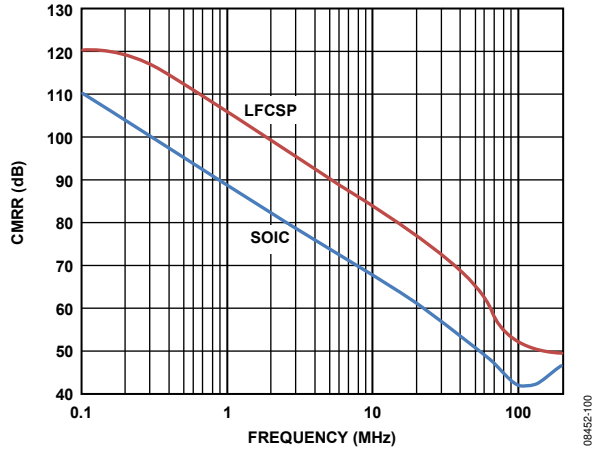

Figure 38. CMRR vs. Frequency

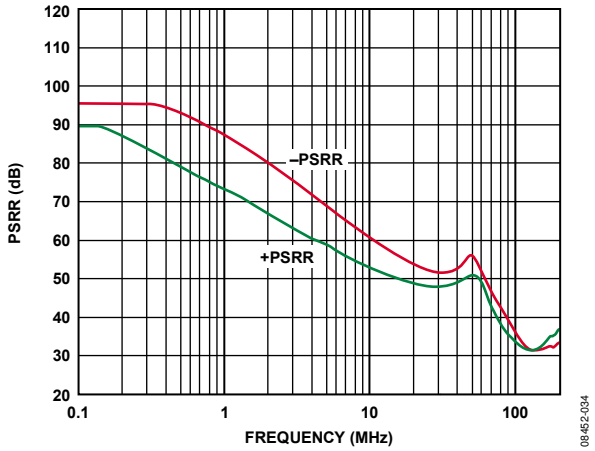

Figure 41. PSRR vs. Frequency

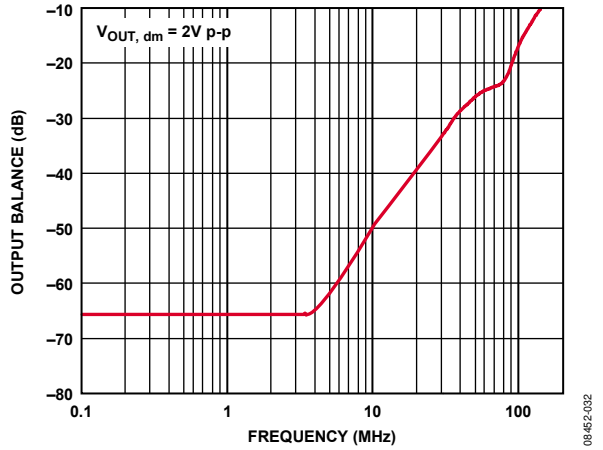

Figure 39. Output Balance vs. Frequency

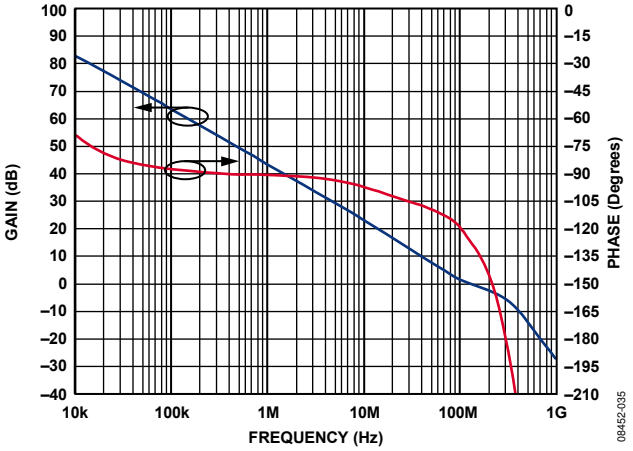

Figure 42. Open-Loop Gain and Phase vs. Frequency

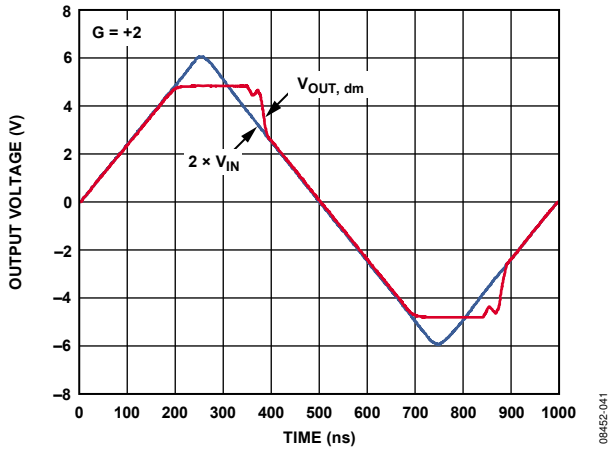

Figure 43. Output Overdrive Recovery, G = 2

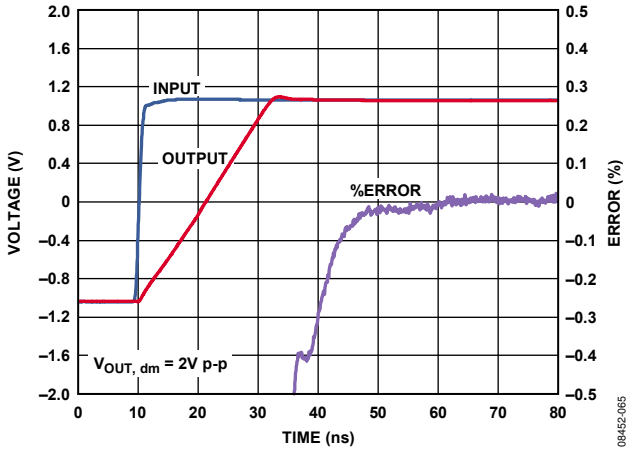

Figure 46. 0.1% Settling Time

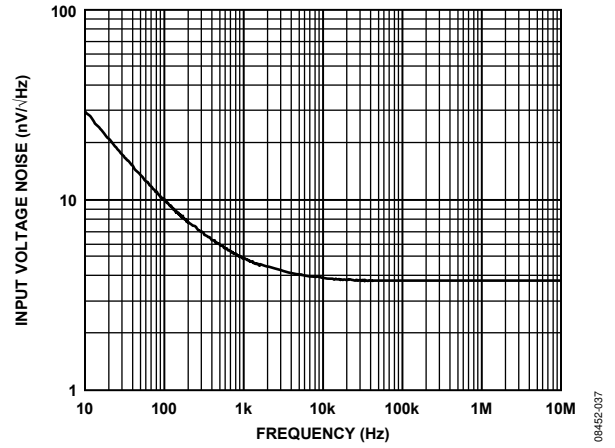

Figure 44. Voltage Noise Spectral Density, Referred to Input

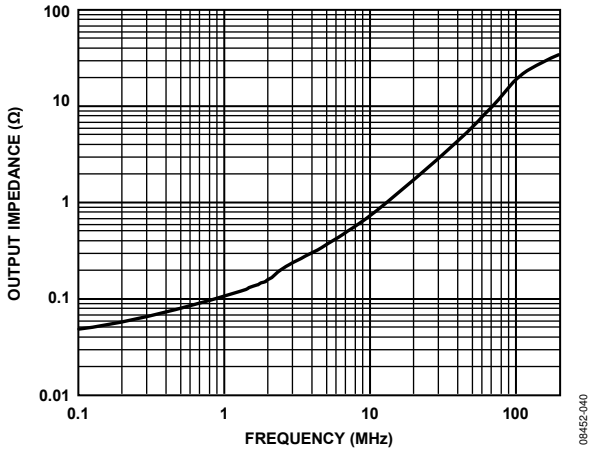

Figure 47. Closed-Loop Output Impedance Magnitude vs. Frequency, G = 1

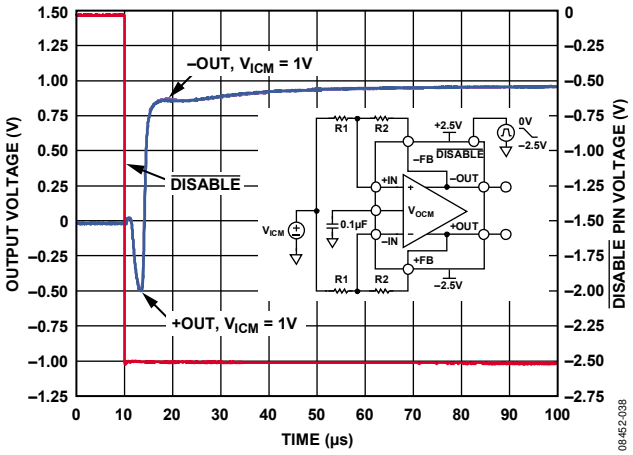

Figure 45. $\overline{DISABLE}$ Pin Turn-Off Time

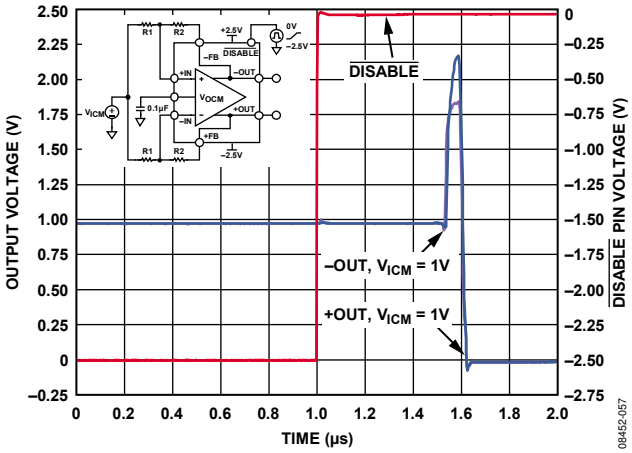

Figure 48. $\overline{DISABLE}$ Pin Turn-On Time

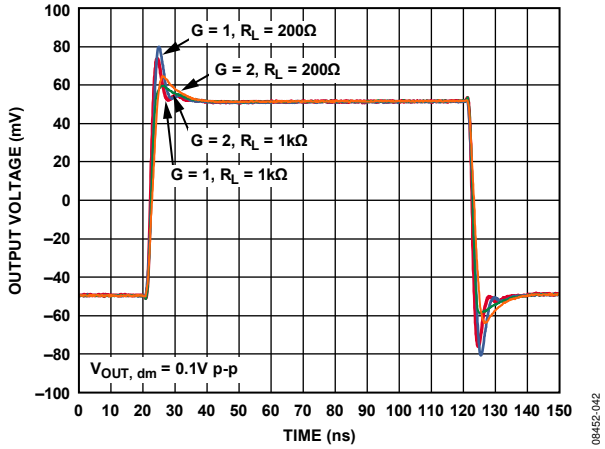

Figure 49. Small Signal Transient Response for Various Gains and Loads (LFCSP)

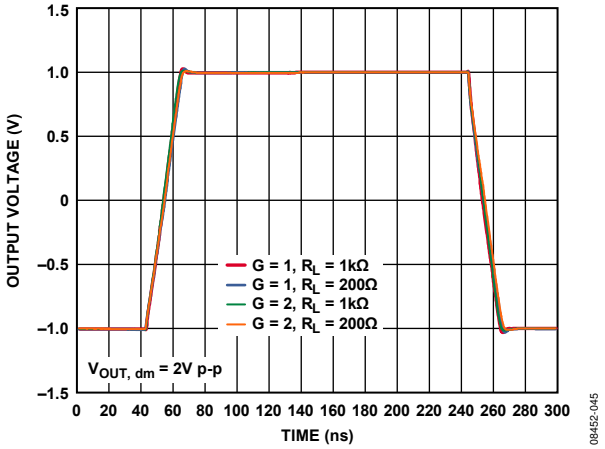

Figure 52. Large Signal Transient Response for Various Gains and Loads

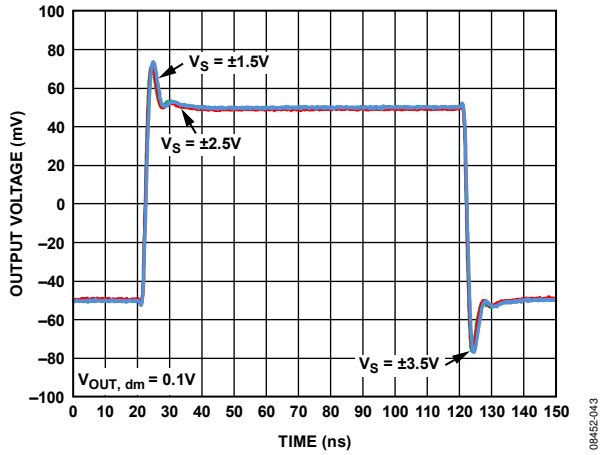

Figure 50. Small Signal Transient Response for Various Supplies (LFCSP)

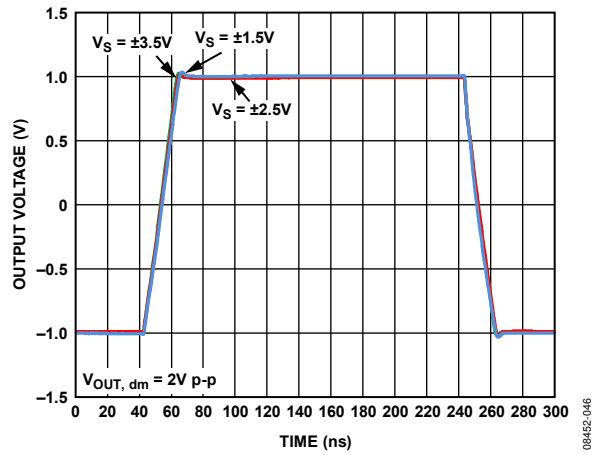

Figure 53. Large Signal Transient Response for Various Supplies

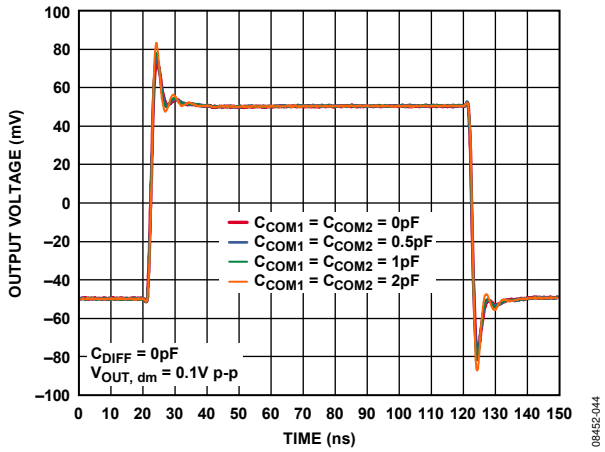

Figure 51. Small Signal Transient Response for Various Capacitive Loads (LFCSP)

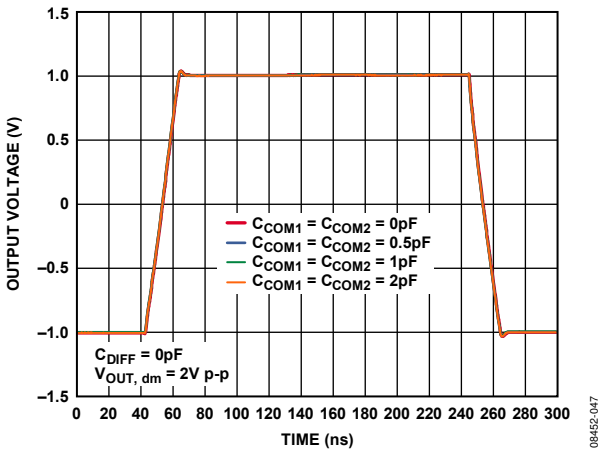

Figure 54. Large Signal Transient Response for Various Capacitive Loads

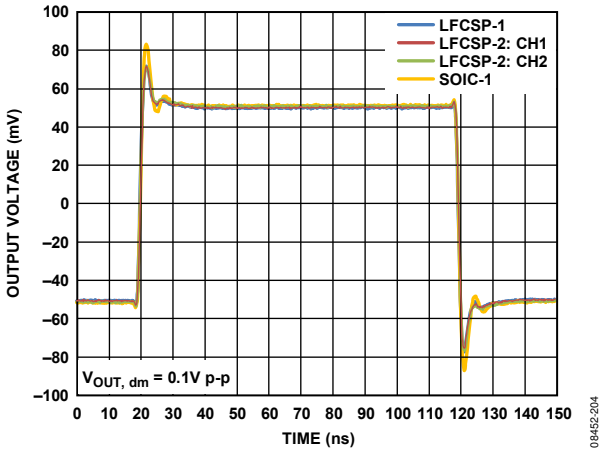

Figure 55. Small Signal Transient Response for Various Packages, C_L = 0 pF

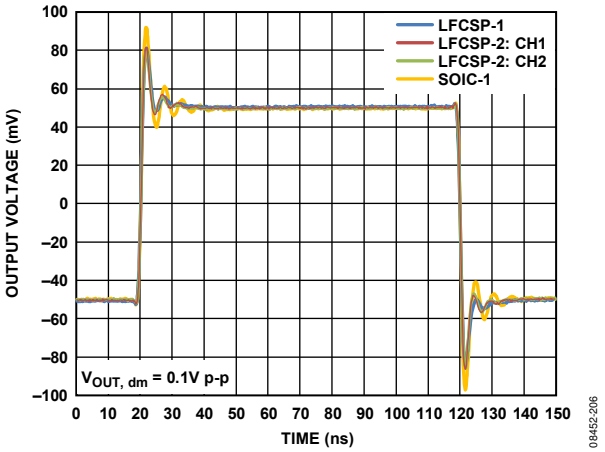

Figure 57. Small Signal Transient Response for Various Packages, C_L = 2 pF

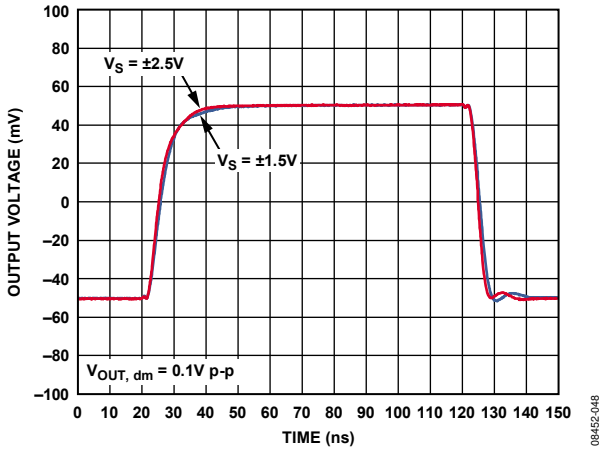

Figure 56. V_{OCM} Small Signal Transient Response

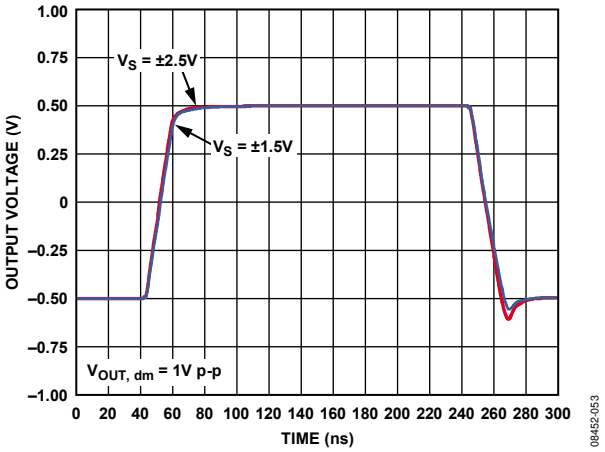

Figure 58. V_{OCM} Large Signal Transient Response

TEST CIRCUITS

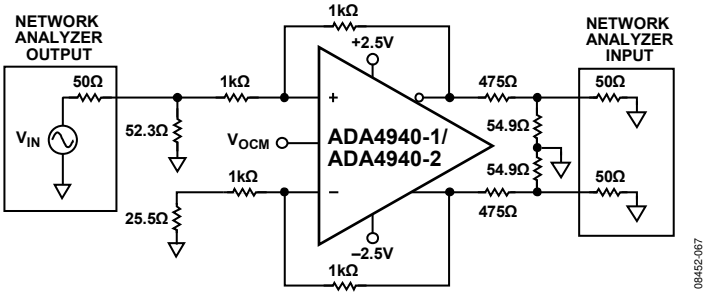

Figure 59. Equivalent Basic Test Circuit

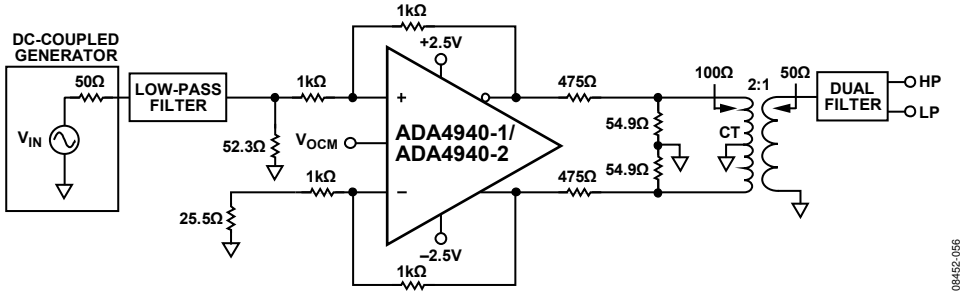

Figure 60. Test Circuit for Distortion Measurements

TERMINOLOGY

DEFINITION OF TERMS

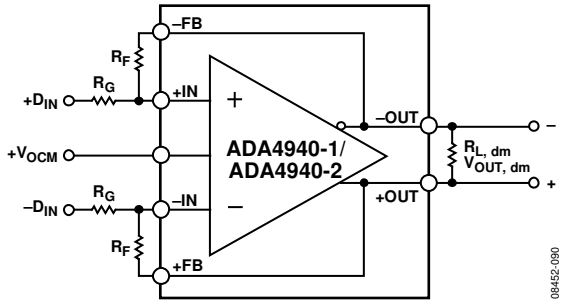

Figure 61. Circuit Definitions

Differential Voltage

Differential voltage refers to the difference between two node voltages. For example, the differential output voltage (or equivalently, output differential mode voltage) is defined as

$$V_{OUT,\,dm} = (V_{+OUT} - V_{-OUT})$$

where V_{+OUT} and V_{-OUT} refer to the voltages at the +OUT and −OUT terminals with respect to a common reference.

Similarly, the differential input voltage is defined as

$$V_{IN,\,dm} = (+D_{IN} - (-D_{IN}))$$

Common-Mode Voltage (CMV)

CMV refers to the average of two node voltages. The output common-mode voltage is defined as

$$V_{OUT,\,cm} = (V_{+OUT} + V_{-OUT})/2$$

Similarly, the input common-mode voltage is defined as

$$V_{IN,\,cm} = (+D_{IN} + (-D_{IN}))/2$$

Common-Mode Offset Voltage

The common-mode offset voltage is defined as the difference between the voltage applied to the V_{OCM} terminal and the common mode of the output voltage.

$$V_{OS,\,cm} = V_{OUT,\,cm} - V_{OCM}$$

Differential V_{OS}, Differential CMRR, and V_{OCM} CMRR

The differential mode and common-mode voltages each have their own error sources. The differential offset ($V_{OS,\,dm}$) is the voltage error between the +IN and −IN terminals of the amplifier. Differential CMRR reflects the change of $V_{OS,\,dm}$ in response to changes to the common-mode voltage at the input terminals $+D_{IN}$ and $-D_{IN}$.

$$CMRR_{DIFF} = \frac{\Delta V_{IN,\,cm}}{\Delta V_{OS,\,dm}}$$

V_{OCM} CMRR reflects the change of $V_{OS,\,dm}$ in response to changes to the common-mode voltage at the output terminals.

$$CMRR_{V_{OCM}} = \frac{\Delta V_{OCM}}{\Delta V_{OS,\,dm}}$$

Balance

Balance is a measure of how well the differential signals are matched in amplitude; the differential signals are exactly 180° apart in phase. By this definition, the output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage.

$$Output\ Balance\ Error = \left| \frac{V_{OUT,\,cm}}{V_{OUT,\,dm}} \right|$$

THEORY OF OPERATION

The ADA4940-1/ADA4940-2 are high speed, low power differential amplifiers fabricated on Analog Devices advanced dielectrically isolated SiGe bipolar process. They provide two closely balanced differential outputs in response to either differential or single-ended input signals. An external feedback network that is similar to a voltage feedback operational amplifier sets the differential gain. The output common-mode voltage is independent of the input common-mode voltage and is set by an external voltage at the V_{OCM} terminal. The PNP input stage allows input common-mode voltages between the negative supply and 1.2 V below the positive supply. A rail-to-rail output stage supplies a wide output voltage range. The $\overline{\text{DISABLE}}$ pin can reduce the supply current of the amplifier to 13.5 µA.

Figure 62 shows the ADA4940-1/ADA4940-2 architecture. The differential feedback loop consists of the differential transconductance G_{DIFF} working through the G_O output buffers and the R_F/R_G feedback networks. The common-mode feedback loop is set up with a voltage divider across the two differential outputs to create an output voltage midpoint and a common-mode transconductance, G_{CM}.

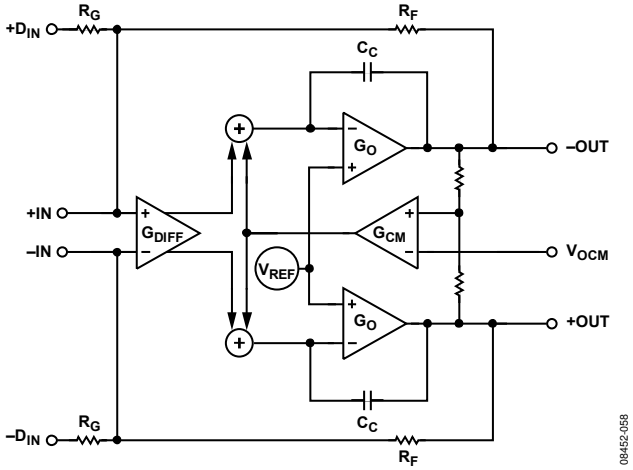

Figure 62. ADA4940-1/ADA4940-2 Architectural Block

The differential feedback loop forces the voltages at +IN and −IN to equal each other. This fact sets the following relationships:

$$\frac{+D_{IN}}{R_G} = -\frac{V_{-OUT}}{R_F}$$

$$\frac{-D_{IN}}{R_G} = -\frac{V_{+OUT}}{R_F}$$

Subtracting the previous equations gives the relationship that shows R_F and R_G setting the differential gain.

$$(V_{+OUT} - V_{-OUT}) = (+D_{IN} - (-D_{IN})) \times \frac{R_F}{R_G}$$

The common-mode feedback loop drives the output common-mode voltage that is sampled at the midpoint of the output voltage divider to equal the voltage at V_{OCM}. This results in the following relationships:

$$V_{+OUT} = V_{OCM} + \frac{V_{OUT,dm}}{2}$$

$$V_{-OUT} = V_{OCM} - \frac{V_{OUT,dm}}{2}$$

Note that the differential amplifier's summing junction input voltages, +IN and −IN, are set by both the output voltages and the input voltages.

$$V_{+IN} = +D_{IN}\left(\frac{R_F}{R_F + R_G}\right) + V_{-OUT}\left(\frac{R_G}{R_F + R_G}\right)$$

$$V_{-IN} = -D_{IN}\left(\frac{R_F}{R_F + R_G}\right) + V_{+OUT}\left(\frac{R_G}{R_F + R_G}\right)$$

APPLICATIONS INFORMATION

ANALYZING AN APPLICATION CIRCUIT

The ADA4940-1/ADA4940-2 use open-loop gain and negative feedback to force their differential and common-mode output voltages in such a way as to minimize the differential and common-mode error voltages. The differential error voltage is defined as the voltage between the differential inputs labeled +IN and −IN (see Figure 61). For most purposes, this voltage is zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to V_{OCM} is also zero. Starting from these two assumptions, any application circuit can be analyzed.

SETTING THE CLOSED-LOOP GAIN

Determine the differential mode gain of the circuit in Figure 61 by using the following equation:

$$\left|\frac{V_{OUT,dm}}{V_{IN,dm}}\right| = \frac{R_F}{R_G}$$

This assumes that the input resistors (R_G) and feedback resistors (R_F) on each side are equal.

ESTIMATING THE OUTPUT NOISE VOLTAGE

Estimate the differential output noise of the ADA4940-1/ADA4940-2 by using the noise model in Figure 63. The input-referred noise voltage density, v_{nIN}, is modeled as a differential input, and the noise currents, i_{nIN-} and i_{nIN+}, appear between each input and ground. The noise currents are assumed equal and produce a voltage across the parallel combination of the gain and feedback resistances. v_{nCM} is the noise voltage density at the V_{OCM} pin. Each of the four resistors contributes $(4kTR_x)^{1/2}$. Table 14 summarizes the input noise sources, the multiplication factors, and the output-referred noise density terms. For more noise calculation information, go to the Analog Devices Differential Amplifier Calculator (DiffAmpCalc™), click **ADIDiffAmpCalculator.zip**, and follow the on-screen prompts.

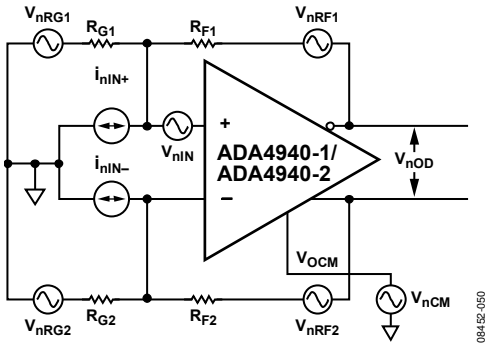

Figure 63. ADA4940-1/ADA4940-2 Noise Model

As with conventional op amp, the output noise voltage densities can be estimated by multiplying the input-referred terms at +IN and −IN by the appropriate output factor,

where:

$G_N = \frac{2}{(\beta_1 + \beta_2)}$ is the circuit noise gain.

$\beta_1 = \frac{R_{G1}}{R_{F1} + R_{G1}}$ and $\beta_2 = \frac{R_{G2}}{R_{F2} + R_{G2}}$ are the feedback factors.

When $R_{F1}/R_{G1} = R_{F2}/R_{G2}$, then $\beta 1 = \beta 2 = \beta$, and the noise gain becomes

$$G_N = \frac{1}{\beta} = 1 + \frac{R_F}{R_G}$$

Note that the output noise from V_{OCM} goes to zero in this case. The total differential output noise density, v_{nOD}, is the root-sum-square of the individual output noise terms.

$$v_{nOD} = \sqrt{\sum_{i=1}^{8} v_{nOi}^2}$$

Table 14. Output Noise Voltage Density Calculations

Input Noise Contribution	Input Noise Term	Input Noise Voltage Density	Output Multiplication Factor	Output-Referred Noise Voltage Density Term
Differential Input	v_{nIN}	v_{nIN}	G_N	$v_{nO1} = G_N (v_{nIN})$
Inverting Input	i_{nIN-}	$i_{nIN-} \times (R_{G2} \| R_{F2})$	G_N	$v_{nO2} = G_N [i_{nIN-} \times (R_{G2} \| R_{F2})]$
Noninverting Input	i_{nIN+}	$i_{nIN+} \times (R_{G1} \| R_{F1})$	G_N	$v_{nO3} = G_N [i_{nIN+} \times (R_{G1} \| R_{F1})]$
V_{OCM} Input	v_{nCM}	v_{nCM}	$G_N (\beta_1 - \beta_2)$	$v_{nO4} = G_N (\beta_1 - \beta_2)(v_{nCM})$
Gain Resistor R_{G1}	v_{nRG1}	$(4kTR_{G1})^{1/2}$	$G_N (1 - \beta_2)$	$v_{nO5} = G_N (1 - \beta_2)(4kTR_{G1})^{1/2}$
Gain Resistor R_{G2}	v_{nRG2}	$(4kTR_{G2})^{1/2}$	$G_N (1 - \beta_1)$	$v_{nO6} = G_N (1 - \beta_1)(4kTR_{G2})^{1/2}$
Feedback Resistor R_{F1}	v_{nRF1}	$(4kTR_{F1})^{1/2}$	1	$v_{nO7} = (4kTR_{F1})^{1/2}$
Feedback Resistor R_{F2}	v_{nRF2}	$(4kTR_{F2})^{1/2}$	1	$v_{nO8} = (4kTR_{F2})^{1/2}$

Table 15 and Table 16 list several common gain settings, recommended resistor values, input impedances, and output noise density for both balanced and unbalanced input configurations.

Table 15. Differential Ground-Referenced Input, DC-Coupled, R_L = 1 kΩ (See Figure 64)

Nominal Gain (dB)	R_F (Ω)	R_G (Ω)	$R_{IN, dm}$ (Ω)	Differential Output Noise Density (nV/√Hz)	RTI (nV/√Hz)
0	1000	1000	2000	11.3	11.3
6	1000	500	1000	15.4	7.7
10	1000	318	636	20.0	6.8
14	1000	196	392	27.7	5.5

Table 16. Single-Ended Ground-Referenced Input, DC-Coupled, R_S = 50 Ω, R_L = 1 kΩ (See Figure 65)

Nominal Gain (dB)	R_F (Ω)	R_G (Ω)	R_T (Ω)	$R_{IN, se}$ (Ω)	R_{G1} (Ω)[1]	Differential Output Noise Density (nV/√Hz)	RTI (nV/√Hz)
0	1000	1000	52.3	1333	1025	11.2	11.2
6	1000	500	53.6	750	526	15.0	7.5
10	1000	318	54.9	512	344	19.0	6.3
14	1000	196	59.0	337	223	25.3	5

[1] $R_{G1} = R_G + (R_S||R_T)$

IMPACT OF MISMATCHES IN THE FEEDBACK NETWORKS

Even if the external feedback networks (R_F/R_G) are mismatched, the internal common-mode feedback loop still forces the outputs to remain balanced. The amplitudes of the signals at each output remain equal and 180° out of phase. The input-to-output, differential mode gain varies proportionately to the feedback mismatch, but the output balance is unaffected.

As well as causing a noise contribution from V_{OCM}, ratio-matching errors in the external resistors result in a degradation of the ability of the circuit to reject input common-mode signals, much the same as for a four resistors difference amplifier made from a conventional op amp.

In addition, if the dc levels of the input and output common-mode voltages are different, matching errors result in a small differential mode, output offset voltage. When G = 1, with a ground-referenced input signal and the output common-mode level set to 2.5 V, an output offset of as much as 25 mV (1% of the difference in common-mode levels) can result if 1% tolerance resistors are used. Resistors of 1% tolerance result in a worst-case input CMRR of about 40 dB, a worst-case differential mode output offset of 25 mV due to the 2.5 V level-shift, and no significant degradation in output balance error.

CALCULATING THE INPUT IMPEDANCE OF AN APPLICATION CIRCUIT

The effective input impedance of a circuit depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, as shown in Figure 64, the input impedance ($R_{IN, dm}$) between the inputs ($+D_{IN}$ and $-D_{IN}$) is simply $R_{IN, dm} = 2 \times R_G$.

For an unbalanced, single-ended input signal (see Figure 65), the input impedance is

$$R_{IN, se} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right)$$

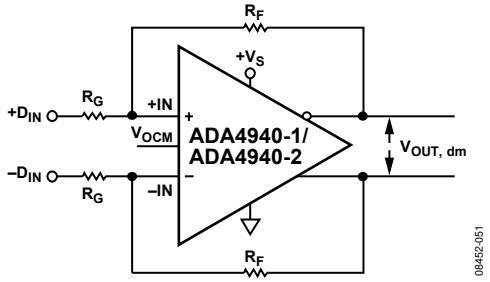

Figure 64. ADA4940-1/ADA4940-2 Configured for Balanced (Differential) Inputs

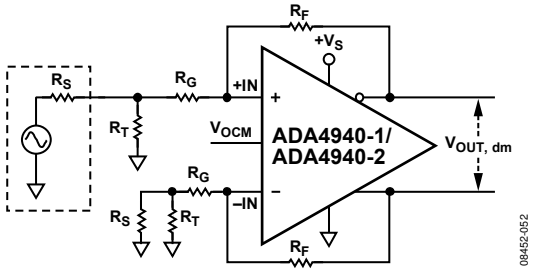

Figure 65. ADA4940-1/ADA4940-2 Configured for Unbalanced (Single-Ended) Input

The input impedance of the circuit is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor R_{G1}.

Terminating a Single-Ended Input

This section describes how to properly terminate a single-ended input to the ADA4940-1/ADA4940-2 with a gain of 1, R_F = 1 kΩ and R_G = 1 kΩ. An example using an input source with a terminated output voltage of 1 V p-p and source resistance of 50 Ω illustrates the three steps that must be followed. Because the terminated output voltage of the source is 1 V p-p, the open-circuit output voltage of the source is 2 V p-p. The source shown in Figure 66 indicates this open-circuit voltage.

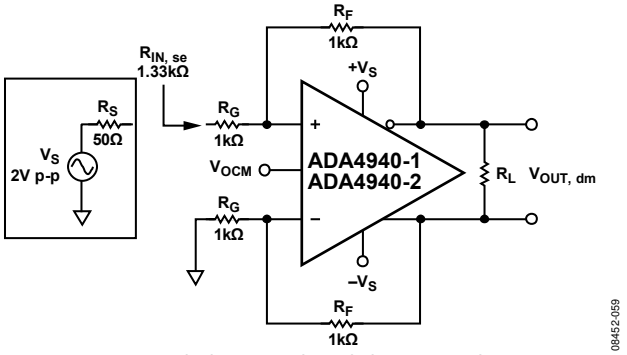

Figure 66. Calculating Single-Ended Input Impedance, R_{IN}

1. The input impedance is calculated by

$$R_{IN,se} = \left(\frac{R_G}{1-\frac{R_F}{2\times(R_G+R_F)}}\right) = \left(\frac{1000}{1-\frac{1000}{2\times(\ 1000\ +\ 1000)}}\right) = 1.33\ \text{k}\Omega$$

2. To match the 50 Ω source resistance, calculate the termination resistor, R_T, using $R_T||1.33\ \text{k}\Omega = 50\ \Omega$. The closest standard 1% value for R_T is 52.3 Ω.

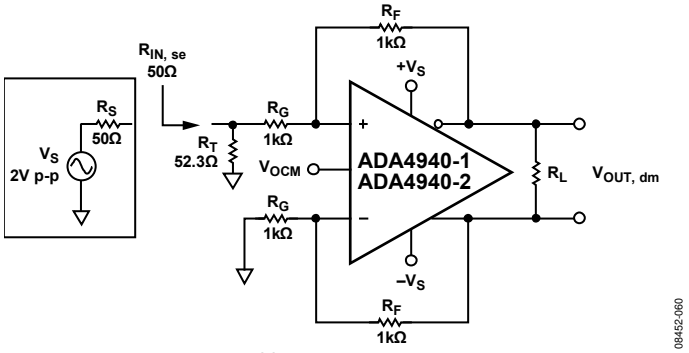

Figure 67. Adding Termination Resistor R_T

3. Figure 67 shows that the effective R_G in the upper feedback loop is now greater than the R_G in the lower loop due to the addition of the termination resistors. To compensate for the imbalance of the gain resistors, add a correction resistor (R_{TS}) in series with R_G in the lower loop. R_{TS} is the Thevenin equivalent of the source resistance, R_S, and the termination resistance, R_T, and is equal to $R_S||R_T$.

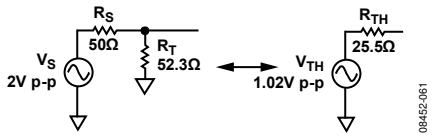

Figure 68. Calculating the Thevenin Equivalent

$R_{TS} = R_{TH} = R_S||R_T$ = 25.5 Ω. Note that V_{TH} is greater than 1 V p-p, which was obtained with R_T = 50 Ω. The modified circuit with the Thevenin equivalent (closest 1% value used for R_{TH}) of the terminated source and R_{TS} in the lower feedback loop is shown in Figure 69.

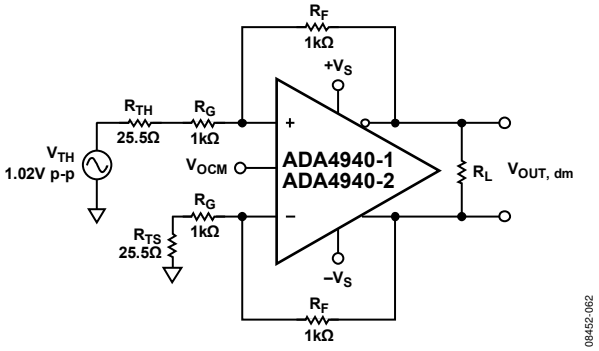

Figure 69. Thevenin Equivalent and Matched Gain Resistors

Figure 69 presents a tractable circuit with matched feedback loops that can be easily evaluated.

It is useful to point out two effects that occur with a terminated input. The first is that the value of R_G is increased in both loops, lowering the overall closed-loop gain. The second is that V_{TH} is a little larger than 1 V p-p, as it would be if R_T = 50 Ω. These two effects have opposite impacts on the output voltage, and for large resistor values in the feedback loops (~1 kΩ), the effects essentially cancel each other out. For small R_F and R_G, or high gains, however, the diminished closed-loop gain is not cancelled completely by the increased V_{TH}. This can be seen by evaluating Figure 69.

The desired differential output in this example is 1 V p-p because the terminated input signal was 1 V p-p and the closed-loop gain = 1. The actual differential output voltage, however, is equal to (1.02 V p-p)(1000/1025.5) = 0.996 V p-p. This is within the tolerance of the resistors, so no change to the feedback resistor, R_F, is required.

INPUT COMMON-MODE VOLTAGE RANGE

The ADA4940-1/ADA4940-2 input common-mode range is shifted down by approximately 1 V_{BE}, in contrast to other ADC drivers with centered input ranges, such as the ADA4939-1/ADA4939-2. The downward-shifted input common-mode range is especially suited to dc-coupled, single-ended-to-differential, and single-supply applications.

For ±2.5 V or +5 V supply operation, the input common-mode range at the summing nodes of the amplifier is specified as −2.7 V to +1.3 V or −0.2 V to 3.8 V, and is specified as −0.2 V to +1.8 V with a +3 V supply.