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Low Power, Three Electrode Electrocardiogram (ECG) Analog Front End

Data Sheet

ADAS1000-3/ADAS1000-4

FEATURES

Biopotential signals in; digitized signals out
3 acquisition (ECG) channels and one driven lead
Can be ganged for 8 electrode + RLD using master ADAS1000 or ADAS1000-1
AC and DC lead-off detection
Internal pace detection algorithm on 3 leads
Support for user's own pace
Thoracic impedance measurement (internal/external path)
Selectable reference lead
Scalable noise vs. power control, power-down modes
Low power operation from
11 mW (1 lead), 15 mW (3 leads)
Lead or electrode data available
Supports AAMI EC11:1991/(R)2001/(R)2007, AAMI EC38 R2007, EC13:2002/(R)2007, IEC60601-1 ed. 3.0 b:2005, IEC60601-2-25 ed. 2.0 :2011, IEC60601-2-27 ed. 2.0 b:2005, IEC60601-2-51 ed. 1.0 b: 2005
Fast overload recovery
Low or high speed data output rates
Serial interface SPI-/QSPI™-/DSP-compatible
56-lead LFCSP package (9 mm × 9 mm)
64-lead LQFP package (10 mm × 10 mm body size)

APPLICATIONS

ECG: monitor and diagnostic
Bedside patient monitoring, portable telemetry, Holter, AED, cardiac defibrillators, ambulatory monitors, pace maker programmer, patient transport, stress testing

GENERAL DESCRIPTION

The ADAS1000-3/ADAS1000-4 measure electro cardiac (ECG) signals, thoracic impedance, pacing artifacts, and lead-on/off status and output this information in the form of a data frame supplying either lead/vector or electrode data at programmable data rates. Its low power and small size make it suitable for portable, battery-powered applications. The high performance also makes it suitable for higher end diagnostic machines.

The ADAS1000-4 is a full-featured, 3-channel ECG including respiration and pace detection, while the ADAS1000-3 offers only ECG channels with no respiration or pace features.

The ADAS1000-3/ADAS1000-4 are designed to simplify the task of acquiring and ensuring quality ECG signals. They provide a low power, small data acquisition system for biopotential applications. Auxiliary features that aid in better quality ECG signal acquisition include: multichannel averaged driven lead, selectable reference drive, fast overload recovery, flexible respiration circuitry returning magnitude and phase information, internal pace detection algorithm operating on three leads, and the option of ac or dc lead-off detection. Several digital output options ensure flexibility when monitoring and analyzing signals. Value-added cardiac post processing is executed externally on a DSP, microprocessor, or FPGA.

Because ECG systems span different applications, the ADAS1000-3/ADAS1000-4 feature a power/noise scaling architecture where the noise can be reduced at the expense of increasing power consumption. Signal acquisition channels may be shut down to save power. Data rates can be reduced to save power.

To ease manufacturing tests and development as well as offer holistic power-up testing, the ADAS1000-3/ADAS1000-4 offer a suite of features, such as dc and ac test excitation via the calibration DAC and CRC redundancy testing in addition to readback of all relevant register address space.

The input structure is a differential amplifier input thereby allowing users a variety of configuration options to best suit their application.

The ADAS1000-3/ADAS1000-4 are available in two package options: either a 56-lead LFCSP or a 64-lead LQFP package; they are specified over −40°C to +85°C temperature range.

Rev. B
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REVISION HISTORY

1/15—Rev. A to Rev. B

Changed Frequency Range from 2.031 kHz (Typ) to 2.039 kHz (Typ); Table 2 7
Changes to Endnote 3; Table 3 and Changes to Table 4 10
Changes to Figure 16 18
Changes to Figure 39 and Figure 40 22
Changes to ECG Channel Section 28
Changes to Digital Lead Mode and Calculation Section and Electrode Mode: Common Electrode A and Common Electrode B Configuration Section; Added Figure 55; Renumbered Sequentially 29
Deleted Table 11; Renumbered Sequentially 29
Added Figure 56 and Figure 57 30
Added Figure 58 and Figure 59 31
Added Figure 60 32
Changes to Figure 61, Figure 62, and Figure 63 33
Changes to Lead-Off Detection Section 36
Added Figure 66 and Changes to Respiration (ADAS1000-4 Model Only) Section 37
Changes to External Respiration Path Section 39
Changes to Respiration Carrier Frequency Section; Added Table 13 and Table 14 40
Changes to Pacing Artifact Detection Function (ADAS1000-4 Only) Section 41
Changes to Table 15 42
Changes to Detection Algorithm Overview Section 43
Changes to Pace Edge Threshold, Pace Level Threshold, Pace Amplitude Threshold, Pace Validation Filters, and Pace Width Filter Sections 44
Changes to Evaluating Pace Detection Performance Section and Added Pace Width Section 45
Changes to Voltage Reference Section 57
Changes to Data Ready ($\overline{\text{DRDY}}$) Section 53
Changes to Secondary Serial Interface Section and Table 25 55
Changes to Bit 3, Table 28 58
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Changes to Example 1: Initialize the Device for ECG Capture and Start Streaming Data Section 74

1/13—Rev. 0 to Rev. A

Changes to Endnote 2, Table 1 3
Changes to Excitation Current Test Conditions/Comments 5
Added Table 3 9
Changes to Figure 36, Figure 37, and Figure 39 21
Changes to Respiration (ADAS1000-4 Model Only) Section and Figure 63 34
Changes to Figure 64 35
Changes to Figure 65 36
Added Evaluating Pace Detection Performance Section 40
Changes to Clocks Section 49
Changes to RESPAMP Bits Function Description, Table 29 55

11/12—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

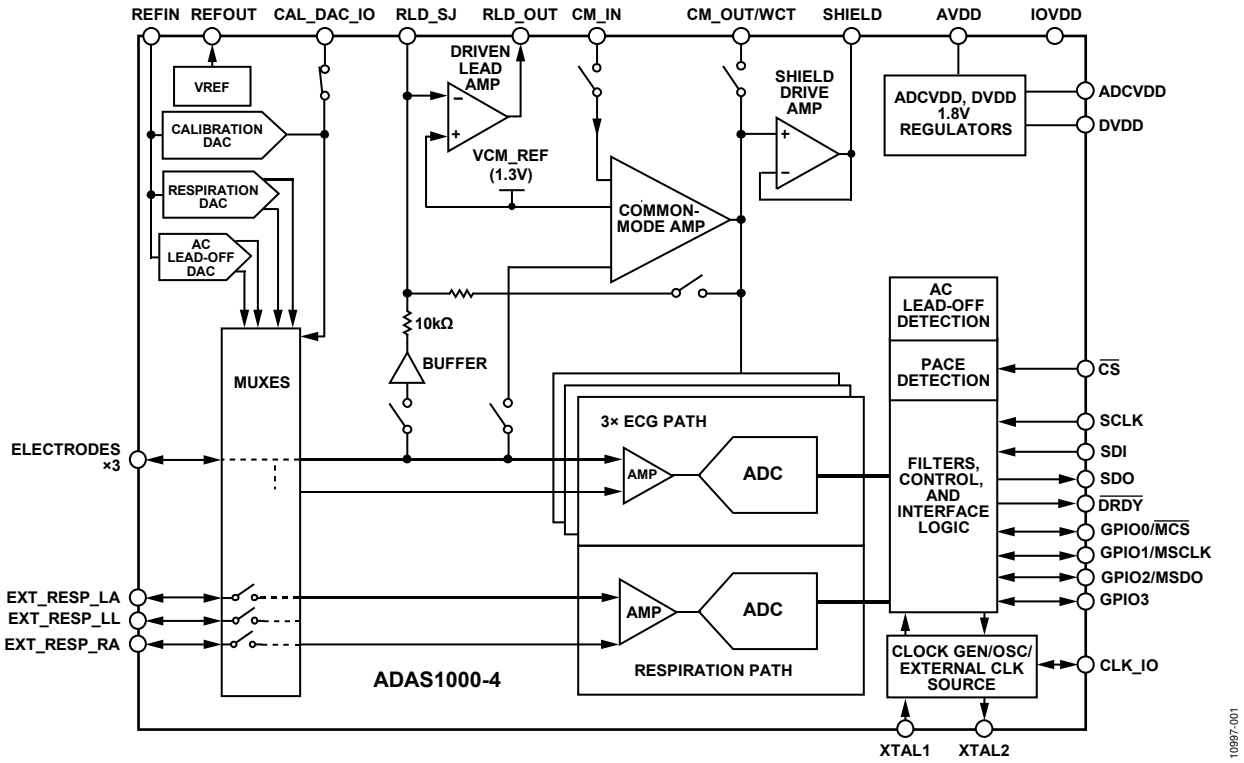


Figure 1. ADAS1000-4 3-Channel Full Featured Model

Table 1. Overview of Features Available from ADAS1000 Generics

Generic	ECG	Operation	Right Leg Drive	Respiration	Pace Detection	Shield Driver	Master Interface[1]	Package Option
ADAS1000	5 ECG channels	Master/slave	Yes	Yes	Yes	Yes	Yes	LFCSP, LQFP
ADAS1000-1	5 ECG channels	Master/slave	Yes			Yes	Yes	LFCSP
ADAS1000-2[2]	5 ECG channels	Slave						LFCSP, LQFP
ADAS1000-3	3 ECG channels	Master/slave	Yes			Yes	Yes	LFCSP, LQFP
ADAS1000-4	3 ECG channels	Master/slave	Yes	Yes	Yes	Yes	Yes	LFCSP, LQFP

[1] Master interface is provided for users wishing to utilize their own digital pace algorithm; see the Secondary Serial Interface section.
[2] This is a companion device for increased channel count purposes. It has a subset of features and is not intended for standalone use. It may be used in conjunction with any master device.

SPECIFICATIONS

AVDD = 3.3 V ± 5%, IOVDD = 1.65 V to 3.6 V, AGND = DGND = 0 V, REFIN tied to REFOUT, externally supplied crystal/clock = 8.192 MHz. Decoupling for reference and supplies as noted in the Power Supply, Grounding, and Decoupling Strategy section. T_A = −40°C to +85°C, unless otherwise noted. Typical specifications are mean values at T_A = 25°C.

For specified performance, internal ADCVDD and DVDD linear regulators have been used. They may be supplied from external regulators. ADCVDD = 1.8 V ± 5%, DVDD = 1.8 V ± 5%.

Front-end gain settings: GAIN 0 = ×1.4, GAIN 1 = ×2.1, GAIN 2 = ×2.8, GAIN 3 = ×4.2.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ECG CHANNEL					These specifications apply to the following pins: ECG1_LA, ECG2_LL, ECG3_RA, CM_IN (CE mode), EXT_RESP_xx pins when used in extend switch mode
Electrode Input Range					Independent of supply
	0.3	1.3	2.3	V	GAIN 0 (gain setting ×1.4)
	0.63	1.3	1.97	V	GAIN 1 (gain setting ×2.1)
	0.8	1.3	1.8	V	GAIN 2 (gain setting ×2.8)
	0.97	1.3	1.63	V	GAIN 3 (gain setting ×4.2)
Input Bias Current	−40	±1	+40	nA	Relates to each electrode input; over operating range; dc and ac lead-off are disabled
	−200		+200	nA	AGND to AVDD
Input Offset		−7		mV	Electrode/vector mode with VCM = VCM_REF GAIN 3
		−7		mV	GAIN 2
		−15		mV	GAIN 1
		−22		mV	GAIN 0
Input Offset Tempco[1]		±2		µV/°C	
Input Amplifier Input Impedance[2]		1‖10		GΩ‖pF	At 10 Hz
CMRR[2]	105	110		dB	51 kΩ imbalance, 60 Hz with ±300 mV differential dc offset; per AAMI/IEC standards; with driven leg loop closed
Crosstalk[1]		80		dB	Between channels
Resolution[2]		19		Bits	Electrode/vector mode, 2 kHz data rate, 24-bit data-word
		18		Bits	Electrode/vector mode, 16 kHz data rate, 24-bit data-word
		16		Bits	Electrode/analog lead mode, 128 kHz data rate, 16-bit data-word
Integral Nonlinearity Error		30		ppm	GAIN 0; all data rates
Differential Nonlinearity Error		5		ppm	GAIN 0
Gain[2]					Referred to input; (2 × VREF)/gain/(2^N − 1); Applies after factory calibration. User calibration adjusts this number.
GAIN 0 (×1.4)		4.9		µV/LSB	At 19-bit level in 2 kHz data rate
		9.81		µV/LSB	At 18-bit level in 16 kHz data rate
		39.24		µV/LSB	At 16-bit level in 128 kHz data rate
GAIN 1 (×2.1)		3.27		µV/LSB	At 19-bit level in 2 kHz data rate
		6.54		µV/LSB	At 18-bit level in 16 kHz data rate
		26.15		µV/LSB	At 16-bit level in 128 kHz data rate
GAIN 2 (×2.8)		2.45		µV/LSB	At 19-bit level in 2 kHz data rate
		4.9		µV/LSB	At 18-bit level in 16 kHz data rate
		19.62		µV/LSB	At 16-bit level in 128 kHz data rate
GAIN 3 (×4.2)		1.63		µV/LSB	No factory calibration for this gain setting At 19-bit level in 2 kHz data rate
		3.27		µV/LSB	At 18-bit level in 16 kHz data rate
		13.08		µV/LSB	At 16-bit level in 128 kHz data rate

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Gain Error	−1	+0.01	+1	%	GAIN 0 to GAIN 2, factory calibrated; programmable user or factory calibration option enables; factory gain calibration applies only to standard ECG interface
	−2	+0.1	+2	%	GAIN 3 setting, no factory calibration for this gain
Gain Matching	−0.1	+0.02	+0.1	%	GAIN 0 to GAIN 2
	−0.5	+0.1	+0.5	%	GAIN 3
Gain Tempco[1]		25		ppm/°C	
Input Referred Noise[1]					GAIN 2, 2 kHz data rate, see Table 4
Analog Lead Mode		6		µV p-p	0.5 Hz to 40 Hz; high performance mode
		10		µV p-p	0.05 Hz to 150 Hz; high performance mode
		12		µV p-p	0.05 Hz to 150 Hz; low power mode
Electrode Mode		11		µV p-p	0.05 Hz to 150 Hz; high performance mode
		12		µV p-p	0.05 Hz to 150 Hz; low power mode
Digital Lead Mode		14		µV p-p	0.05 Hz to 150 Hz; high performance mode
		16		µV p-p	0.05 Hz to 150 Hz; low power mode
Power Supply Sensitivity[2]		100		dB	At 120 Hz
Analog Channel Bandwidth[1]		65		kHz	
Dynamic Range[1]		104		dB	GAIN 0, 2 kHz data rate, −0.5 dBFS input signal, 10 Hz
Signal-to-Noise Ratio[1]		100		dB	−0.5 dB FS input signal
COMMON-MODE INPUT					CM_IN pin
Input Voltage Range	0.3		2.3	V	
Input Impedance[2]		1||10		GΩ||pF	
Input Bias Current	−40	±1	+40	nA	Over operating range; dc and ac lead-off disabled
	−200		+200	nA	AGND to AVDD
COMMON-MODE OUTPUT					CM_OUT pin
VCM_REF	1.28	1.3	1.32	V	Internal voltage; independent of supply
Output Voltage, VCM	0.3	1.3	2.3	V	No dc load
Output Impedance[1]		0.75		kΩ	Not intended to drive current
Short-Circuit Current[1]		4		mA	
Electrode Summation Weighting Error[2]		1		%	Resistor matching error
RESPIRATION FUNCTION (ADAS1000-4 ONLY)					These specifications apply to the following pins: EXT_RESP_LA, EXT_RESP_LL, EXT_RESP_RA and selected internal respiration paths (Lead I, Lead II, Lead III)
Input Voltage Range	0.3		2.3	V	AC-coupled, independent of supply
Input Voltage Range (Linear Operation)		1.8/gain		V p-p	Programmable gain (10 states)
Input Bias Current	−10	±1	+10	nA	Applies to EXT_RESP_xx pins over AGND to AVDD
Input Referred Noise[1]		0.85		µV rms	
Frequency[2]		46.5 to 64		kHz	Programmable frequency, see Table 30
Excitation Current					Respiration drive current corresponding to differential voltage programmed by the RESPAMP bits in the RESPCTL register; internal respiration mode, cable 5 kΩ/200 pF, 1.2 kΩ chest impedance
		64		µA p-p	Drive Range A
		32		µA p-p	Drive Range B[2]
		16		µA p-p	Drive Range C[2]
		8		µA p-p	Drive Range D[2]
Resolution[2]		24		Bits	Update rate 125 Hz
Measurement Resolution[1]		0.2		Ω	Cable <5 kΩ/200 pF per electrode, body resistance modeled as 1.2 kΩ
		0.02		Ω	No cable impedance, body resistance modeled as 1.2 kΩ
In-Amp Gain[1]		1 to 10			Digitally programmable in steps of 1
Gain Error			1	%	LSB weight for GAIN 0 setting
Gain Tempco[1]		25		ppm/C	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RIGHT LEG DRIVE/DRIVEN LEAD					
Output Voltage Range	0.2		AVDD − 0.2	V	
RLD_OUT Short-Circuit Current	−5	±2	+5	mA	External protection resistor required to meet regulatory patient current limits; output shorted to AVDD/AGND
Closed-Loop Gain Range[2]	25			V/V	
Slew Rate[2]		200		mV/ms	
Input Referred Noise[1]		8		μV p-p	0.05 Hz to 150 Hz
Amplifier GBP[2]		1.5		MHz	
DC LEAD-OFF					Internal current source, pulls up open ECG pins; programmable in 10 nA steps: 10 nA to 70 nA
Lead-Off Current Accuracy		±10		%	Of programmed value
High Threshold Level[1]		2.4		V	Inputs are compared to threshold levels; if inputs exceed levels, lead-off flag is raised
Low Threshold Level[1]		0.2		V	
Threshold Accuracy		25		mV	
AC LEAD-OFF					Programmable in 4 steps: 12.5 nA rms, 25 nA rms, 50 nA rms, 100 nA rms
Frequency Range		2.039		kHz	Fixed frequency
Lead-Off Current Accuracy		±10		%	Of programmed value, measured into low impedance
REFIN					
Input Range[2]	1.76	1.8	1.84	V	Channel gain scales directly with REFIN
Input Current		113		μA	Per active ADC
	450	675	950	μA	Three ECG channels and respiration enabled
REFOUT					On-chip reference voltage for ADC; not intended to drive other components reference inputs directly, must be buffered externally
Output Voltage, VREF	1.785	1.8	1.815	V	
Reference Tempco[1]		±10		ppm/°C	
Output Impedance[2]		0.1		Ω	
Short-Circuit Current[1]		4.5		mA	Short circuit to ground
Voltage Noise[1]		33		μV p-p	0.05 Hz to 150 Hz (ECG band)
		17		μV p-p	0.05 Hz to 5 Hz (respiration)
CALIBRATION DAC					Available on CAL_DAC_IO (output for master, input for slave)
DAC Resolution		10		Bits	
Full-Scale Output Voltage	2.64	2.7	2.76	V	No load, nominal FS output is 1.5 × REFOUT
Zero-Scale Output Voltage	0.24	0.3	0.36	V	No load
DNL	−1		+1	LSB	
Output Series Resistance[2]		10		kΩ	Not intended to drive low impedance load, used for slave CAL_DAC_IO configured as an input
Input Current		±5		nA	When used as an input
CALIBRATION DAC TEST TONE					
Output Voltage	0.9	1	1.1	mV p-p	Rides on common-mode voltage, VCM_REF = 1.3 V
Square Wave		1		Hz	
Low Frequency Sine Wave		10		Hz	
High Frequency Sine Wave		150		Hz	
SHIELD DRIVER					
Output Voltage Range	0.3		2.3	V	Rides on common-mode voltage (VCM)
Gain		1		V/V	
Offset Voltage	−20		+20	mV	
Short-Circuit Current		15	25	μA	Output current limited by internal series resistance
Stable Capacitive Load[2]			10	nF	
CRYSTAL OSCILLATOR					Applied to XTAL1 and XTAL2
Frequency[2]		8.192		MHz	
Start-Up Time[2]		15		ms	Internal startup

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK_IO					External clock source supplied to CLK_IO; this pin is configured as an input when the device is programmed as a slave
Operating Frequency[2]		8.192		MHz	
Input Duty Cycle[2]	20		80	%	
Output Duty Cycle[2]		50		%	
DIGITAL INPUTS					Applies to all digital inputs
Input Low Voltage, V_{IL}			0.3 × IOVDD	V	
Input High Voltage, V_{IH}	0.7 × IOVDD			V	
Input Current, I_{IH}, I_{IL}	−1		+1	µA	
	−20		+20	µA	$\overline{\text{RESET}}$ has an internal pull-up resistor
Pin Capacitance[2]		3		pF	
DIGITAL OUTPUTS					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 1 mA
Output High Voltage, V_{OH}	IOVDD − 0.4			V	I_{SOURCE} = −1 mA
Output Rise/Fall Time		4		ns	Capacitive load = 15 pF, 20% to 80%
DVDD REGULATOR					Internal 1.8 V regulator for DVDD
Output Voltage	1.75	1.8	1.85	V	
Available Current[1]		1		mA	Droop < 10 mV; for external device loading purposes
Short-Circuit Current Limit		40		mA	
ADCVDD REGULATOR					Internal 1.8 V regulator for ADCVDD; not recommended as a supply for other circuitry
Output Voltage	1.75	1.8	1.85	V	
Short-Circuit Current Limit		40		mA	
POWER SUPPLY RANGES[2]					
AVDD	3.15	3.3	5.5	V	
IOVDD	1.65		3.6	V	
ADCVDD	1.71	1.8	1.89	V	If applied by external 1.8 V regulator
DVDD	1.71	1.8	1.89	V	If applied by external 1.8 V regulator
POWER SUPPLY CURRENTS					
AVDD Standby Current		785	975	µA	
IOVDD Standby Current		1	60	µA	
EXTERNALLY SUPPLIED ADCVDD AND DVDD					All three channels enabled, RLD enabled, pace enabled
AVDD Current		2.4	4.1	mA	High performance mode
		2.2	4.1	mA	Low performance mode
		3.2		mA	High performance mode, respiration enabled
ADCVDD Current		4.5	6.5	mA	High performance mode
		3.3	5.5	mA	Low performance mode
		5.4		mA	High performance mode, respiration enabled
DVDD Current		2.0	4	mA	High performance mode
		1.1	3	mA	Low performance mode
		2.0		mA	High performance mode, respiration enabled
INTERNALLY SUPPLIED ADCVDD AND DVDD					All three channels enabled, RLD enabled, pace enabled
AVDD Current		9	12.6	mA	High performance mode
		6.6	9.6	mA	Low performance mode
		11	14.6	mA	High performance mode, respiration enabled
POWER DISSIPATION					All 3 channels enabled, RLD enabled, pace enabled
Externally Supplied ADCVDD and DVDD[3]					
Three Input Channels and RLD		19.6		mW	High performance (low noise)
		15.2		mW	Low power mode
Internally Supplied ADCVDD and DVDD					All three channels enabled, RLD enabled, pace enabled
Three Input Channels and RLD		29.7		mW	High performance (low noise)
		21.8		mW	Low power mode

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OTHER FUNCTIONS[4]					
Power Dissipation					
Respiration		7.6		mW	
Shield Driver		150		µW	
EXTERNALLY SUPPLIED ADCVDD AND DVDD					Two electrodes enabled for one lead measurement, RLD enabled, pace enabled
AVDD Current		1.9	3.7	mA	High performance mode
		1.7	3.7	mA	Low performance mode
ADCVDD Current		3.6	5.5	mA	High performance mode
		2.5	4.5	mA	Low performance mode
DVDD Current		1.7	4	mA	High performance mode
		0.9	3	mA	Low performance mode
INTERNALLY SUPPLIED ADCVDD AND DVDD					Two electrodes enabled for one lead measurement, RLD enabled, pace enabled
AVDD Current		7.3	10.7	mA	High performance mode
		5.3	8.2	mA	Low performance mode
POWER DISSIPATION					Two electrodes enabled for one lead measurement, RLD enabled, pace enabled
Externally Supplied ADCVDD and DVDD[3]					
Two Input Channels and RLD		15.8		mW	High performance (low noise)
		11.7		mW	Low power mode
Internally Supplied ADCVDD and DVDD					
Two Input Channels and RLD		24		mW	High performance (low noise)
		17.5		mW	Low power mode

[1] Guaranteed by characterization, not production tested.
[2] Guaranteed by design, not production tested.
[3] ADCVDD and DVDD can be powered from an internal LDO or, alternatively, can be powered from an external 1.8 V rail, which may result in a lower power solution.
[4] Pace is a digital function and incurs no power penalty.

NOISE PERFORMANCE

Table 3. Typical Input Referred Noise over a 0.5 sec Window (μV p-p)[1]

Mode	Data Rate[2]	GAIN 0 (×1.4) ±1 VCM	GAIN 1 (×2.1) ±0.67 VCM	GAIN 2 (×2.8) ±0.5 VCM	GAIN 3 (×4.2) ±0.3 VCM
Analog Lead Mode[3]					
High Performance Mode	2 kHz (0.5 Hz to 40 Hz)	8	6	5	4
	2 kHz (0.05 Hz to 150 Hz)	14	11	9	7.5

[1] Typical values measured at 25°C, not subject to production test.
[2] Data gathered using the 2 kHz packet/frame rate is measured over 0.5 seconds. The ADAS1000-3/ADAS1000-4 internal programmable low-pass filter is configured for either 40 Hz or 150 Hz bandwidth. The data is gathered and post processed using a digital filter of either 0.05 Hz or 0.5 Hz to provide data over noted frequency bands.
[3] Analog lead mode as shown in Figure 56.

Table 4. Typical Input Referred Noise (μV p-p)[1]

Mode	Data Rate[2]	GAIN 0 (×1.4) ±1 VCM	GAIN 1 (×2.1) ±0.67 VCM	GAIN 2 (×2.8) ±0.5 VCM	GAIN 3 (×4.2) ±0.3 VCM
Analog Lead Mode[3]					
High Performance Mode	2 kHz (0.5 Hz to 40 Hz)	12	8.5	6	5
	2 kHz (0.05 Hz to 150 Hz)	20	14.5	10	8.5
	2 kHz (0.05 Hz to 250 Hz)	27	18	14.5	10.5
	2 kHz (0.05 Hz to 450 Hz)	33.5	24	19	13.5
	16 kHz	95	65	50	39
	128 kHz	180	130	105	80
Low Power Mode	2 kHz (0.5 Hz to 40 Hz)	13	9.5	7.5	5.5
	2 kHz (0.05 Hz to 150 Hz)	22	15.5	12	9
	16 kHz	110	75	59	45
	128 kHz	215	145	116	85
Electrode Mode[4]					
High Performance Mode	2 kHz (0.5 Hz to 40 Hz)	13	9.5	8	5.5
	2 kHz (0.05 Hz to 150 Hz)	21	15	11	9
	2 kHz (0.05 Hz to 250 Hz)	26	19	15.5	11.5
	2 kHz (0.05 Hz to 450 Hz)	34.5	25	20.5	14.5
	16 kHz	100	70	57	41
	128 kHz	190	139	110	85
Low Power Mode	2 kHz (0.5 Hz to 40 Hz)	14	9.5	7.5	5.5
	2 kHz (0.05 Hz to 150 Hz)	22	15.5	12	9.5
	16 kHz	110	75	60	45
	128 kHz	218	145	120	88
Digital Lead Mode[5, 6]					
High Performance Mode	2 kHz (0.5 Hz to 40 Hz)	16	11	9	6.5
	2 kHz (0.05 Hz to 150 Hz)	25	19	15	10
	2 kHz (0.05 Hz to 250 Hz)	34	23	18	13
	2 kHz (0.05 Hz to 450 Hz)	46	31	24	17.5
	16 kHz	130	90	70	50
Low Power Mode	2 kHz (0.5 Hz to 40 Hz)	18	12.5	10	7
	2 kHz (0.05 Hz to 150 Hz)	30	21	16	11
	16 kHz	145	100	80	58

[1] Typical values measured at 25°C, not subject to production test.
[2] Data gathered using the 2 kHz packet/frame rate is measured over 20 seconds. The ADAS1000-3/ADAS1000-4 internal programmable low-pass filter is configured for either 40 Hz or 150 Hz bandwidth. The data is gathered and post processed using a digital filter of either 0.05 Hz or 0.5 Hz to provide data over noted frequency bands.
[3] Analog lead mode as shown in Figure 56.
[4] Single-ended input electrode mode as shown in Figure 59. Electrode mode refers to common electrode A, common electrode B, and single-ended input electrode configurations.
[5] Digital lead mode as shown in Figure 57.
[6] Digital lead mode is available in 2 kHz and 16 kHz data rates.

TIMING CHARACTERISTICS

Standard Serial Interface

AVDD = 3.3 V ± 5%, IOVDD = 1.65 V to 3.6 V, AGND = DGND = 0 V, REFIN tied to REFOUT, externally supplied crystal/clock = 8.192 MHz. T_A = −40°C to +85°C, unless otherwise noted. Typical specifications are mean values at T_A = 25°C.

Table 5.

	IOVDD				
Parameter[1]	**3.3 V**	**2.5 V**	**1.8 V**	**Unit**	**Description**
Output Rate[2]	2		128	kHz	Across specified IOVDD supply range; three programmable output data rates available as configured in FRMCTL register (see Table 37) 2 kHz, 16 kHz, 128 kHz; use skip mode for slower rates.
SCLK Cycle Time	25	40	50	ns min	See Table 21 for details on SCLK frequency vs. packet data/frame rates.
t_{CSSA}	8.5	9.5	12	ns min	$\overline{CS}$ valid setup time to rising SCLK.
t_{CSHA}	3	3	3	ns min	$\overline{CS}$ valid hold time to rising SCLK.
t_{CH}	8	8	8	ns min	SCLK high time.
t_{CL}	8	8	8	ns min	SCLK low time.
t_{DO}	8.5	11.5	20	ns typ	SCLK falling edge to SDO valid delay; SDO capacitance of 15 pF.
	11	19	24	ns max	
t_{DS}	2	2	2	ns min	SDI valid setup time from SCLK rising edge.
t_{DH}	2	2	2	ns min	SDI valid hold time from SCLK rising edge.
t_{CSSD}	2	2	2	ns min	$\overline{CS}$ valid setup time from SCLK rising edge.
t_{CSHD}	2	2	2	ns min	$\overline{CS}$ valid hold time from SCLK rising edge.
t_{CSW}	25	40	50	ns min	$\overline{CS}$ high time between writes (if used). Note that $\overline{CS}$ is an optional input, it may be tied permanently low. See a full description in the Serial Interfaces section.
t_{DRDY_CS}[2]	0	0	0	ns min	$\overline{DRDY}$ to $\overline{CS}$ setup time.
t_{CSO}	6	7	9	ns typ	Delay from $\overline{CS}$ assert to SDO active.
$\overline{RESET}$ Low Time[2]	20	20	20	ns min	Minimum pulse width; $\overline{RESET}$ is edge triggered.

[1] Guaranteed by characterization, not production tested.
[2] Guaranteed by design, not production tested.

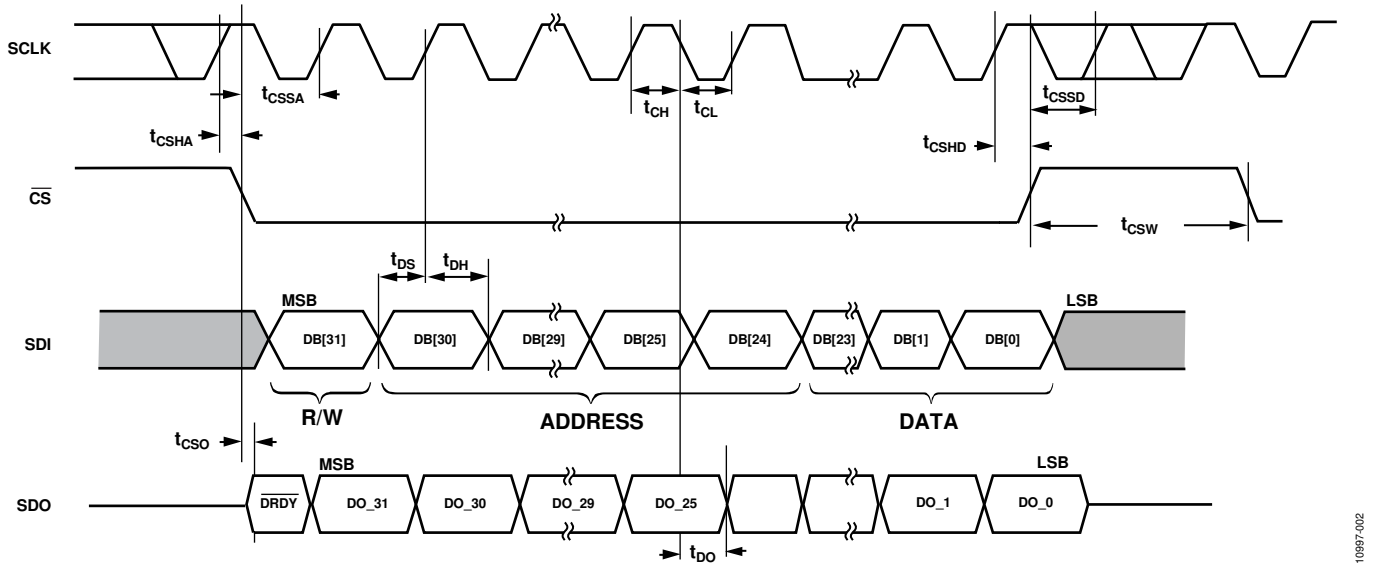


Figure 2. Data Read and Write Timing Diagram (CPHA = 1, CPOL = 1)

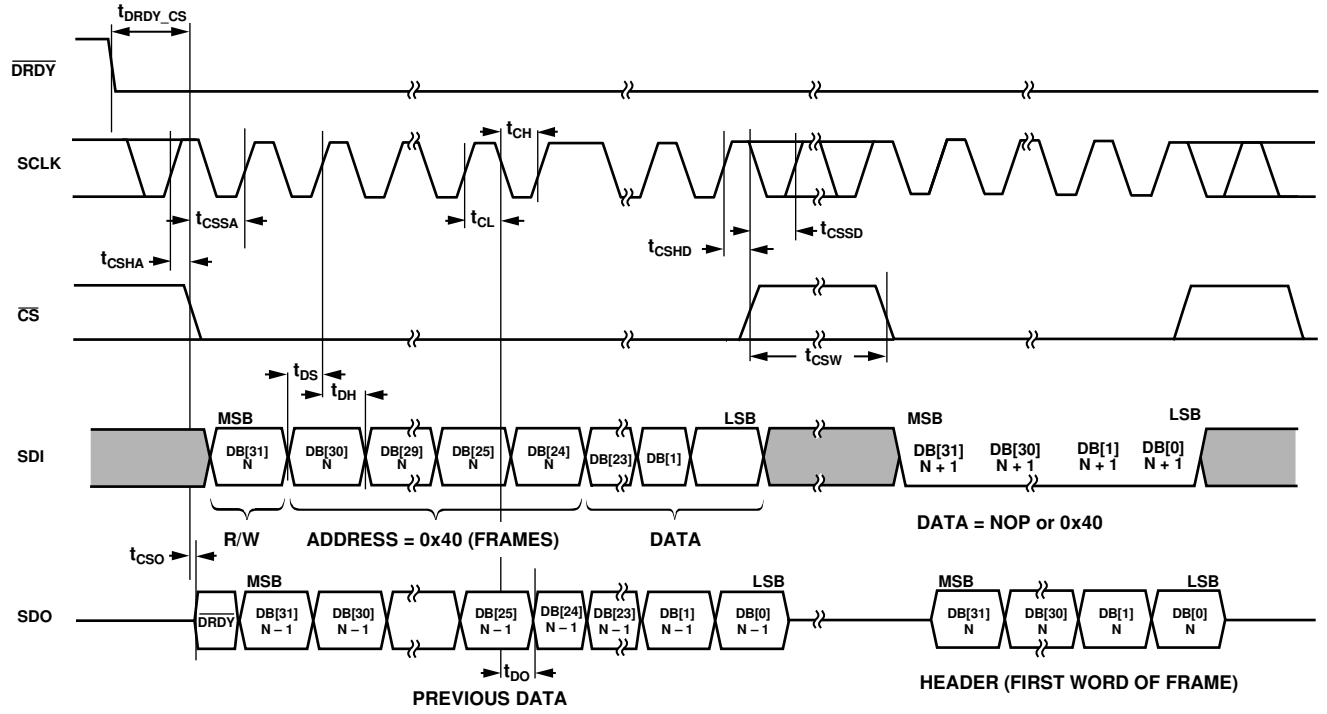


Figure 3. Starting Read Frame Data (CPHA = 1, CPOL = 1)

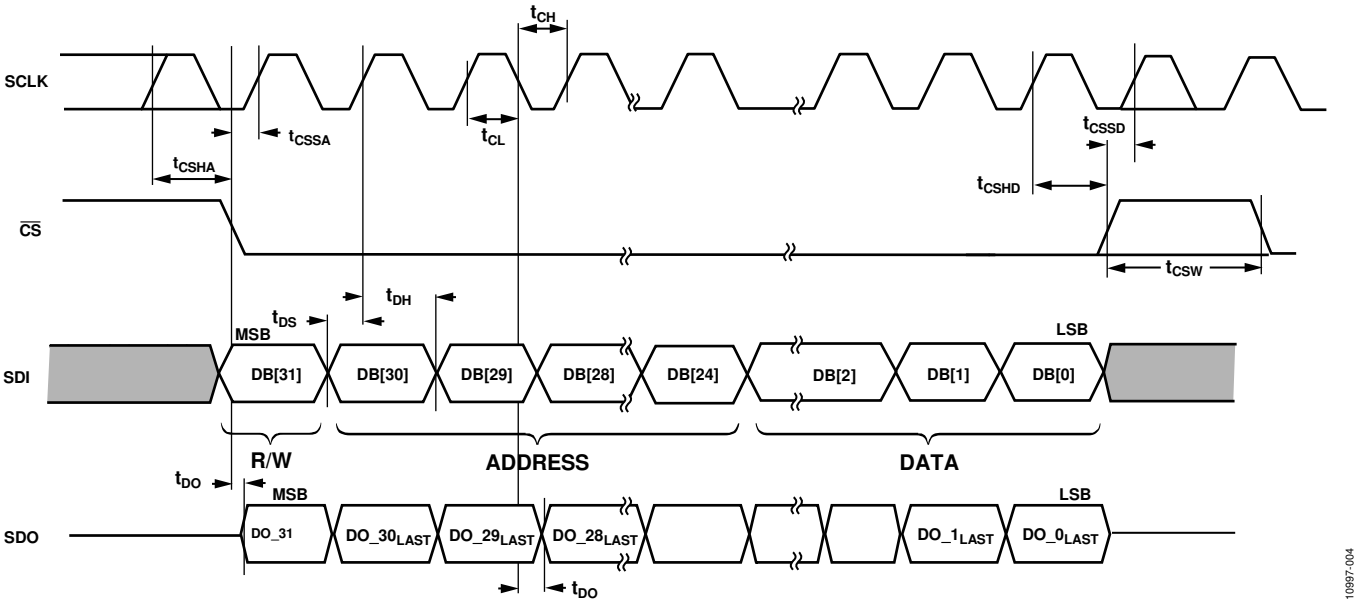


Figure 4. Data Read and Write Timing Diagram (CPHA = 0, CPOL = 0)

Secondary Serial Interface (Master Interface for Customer-Based Digital Pace Algorithm) ADAS1000-4 Only

AVDD = 3.3 V ± 5%, IOVDD = 1.65 V to 3.6 V, AGND = DGND = 0 V, REFIN tied to REFOUT, externally supplied crystal/clock = 8.192 MHz. T_A = −40°C to +85°C, unless otherwise noted. Typical specifications are mean values at T_A = 25°C. The following timing specifications apply for the master interface when the ECGCTL register is configured for high performance mode (ECGCTL[3] = 1), see Table 28.

Table 6.

Parameter[1]	Min	Typ	Max	Unit	Description
Output Frame Rate[2]		128		kHz	All five 16-bit ECG data-words are available at frame rate of 128 kHz only
f_{SCLK}[2]		2.5 × crystal frequency		MHz	Crystal frequency = 8.192 MHz
t_{MCSSA}		24.4		ns	$\overline{MCS}$ valid setup time
t_{MDO}		0		ns	MSCLK rising edge to MSDO valid delay
t_{MCSHD}		48.8		ns	$\overline{MCS}$ valid hold time from MSCLK falling edge
t_{MCSW}		2173		ns	$\overline{MCS}$ high time, SPIFW = 0, $\overline{MCS}$ asserted for entire frame as shown in Figure 5, and configured in Table 33
		2026		ns	$\overline{MCS}$ high time, SPIFW = 1, $\overline{MCS}$ asserted for each word in frame as shown in Figure 6 and configured in Table 33

[1] Guaranteed by characterization, not production tested.
[2] Guaranteed by design, not production tested.

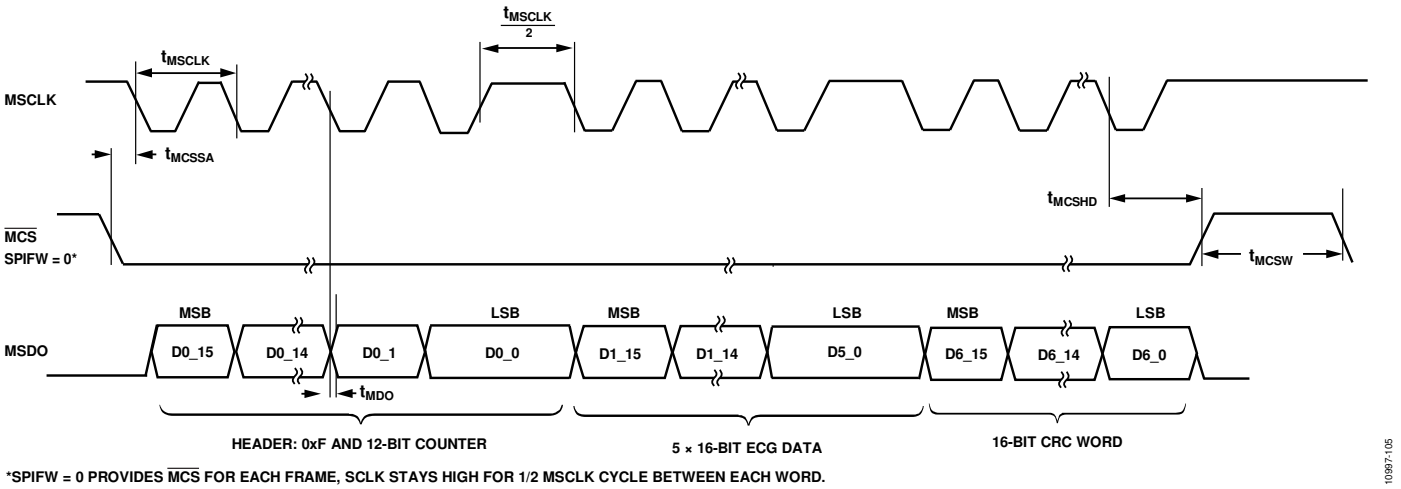


Figure 5. Data Read and Write Timing Diagram for SPIFW = 0, Showing Entire Packet Of Data (Header, 5 ECG Word = [ECG1, ECG2, ECG3 and 2 Words with Zeros], and CRC Word)

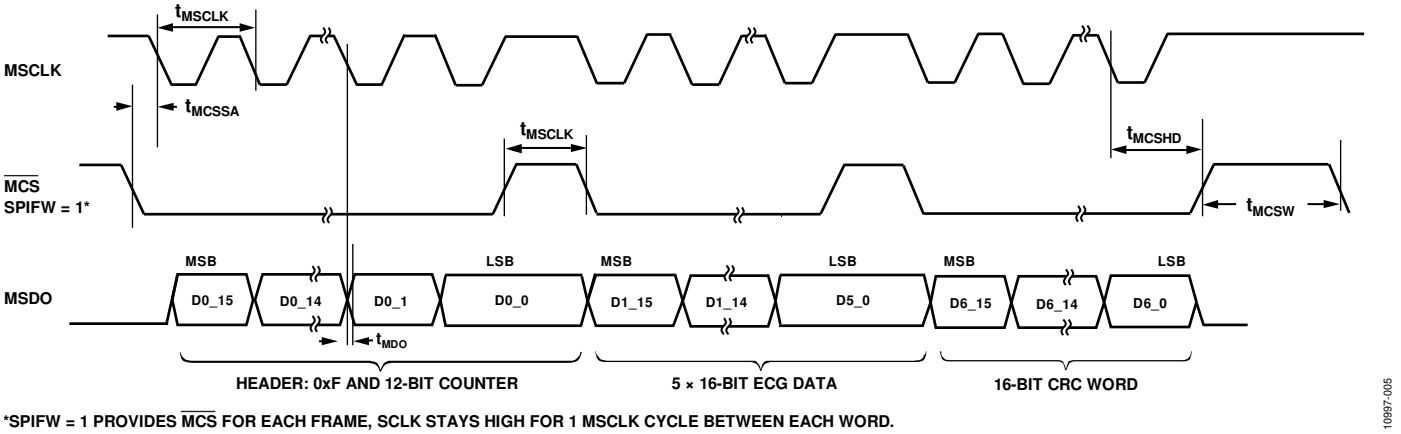


Figure 6. Data Read and Write Timing Diagram for SPIFW = 1, Showing Entire Packet Of Data (Header, 5 ECG Word = [ECG1, ECG2, ECG3 and 2 Words with Zeros], and CRC Word)

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
AVDD to AGND	−0.3 V to +6 V
IOVDD to DGND	−0.3 V to +6 V
ADCVDD to AGND	−0.3 V to +2.5 V
DVDD to DGND	−0.3 V to +2.5 V
REFIN/REFOUT to REFGND	−0.3 V to +2.1 V
ECG and Analog Inputs to AGND	−0.3 V to AVDD + 0.3 V
Digital Inputs to DGND	−0.3 V to IOVDD + 0.3 V
REFIN to ADCVDD	ADCVDD + 0.3 V
AGND to DGND	−0.3 V to + 0.3 V
REFGND to AGND	−0.3 V to + 0.3 V
ECG Input Continuous Current	±10 mA
Storage Temperature Range	−65°C to +125°C
Operating Junction Temperature Range	−40°C to +85°C
Reflow Profile	J-STD-20 (JEDEC)
Junction Temperature	150°C max
ESD	
HBM	2500 V
FICDM	1000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 8. Thermal Resistance[1]

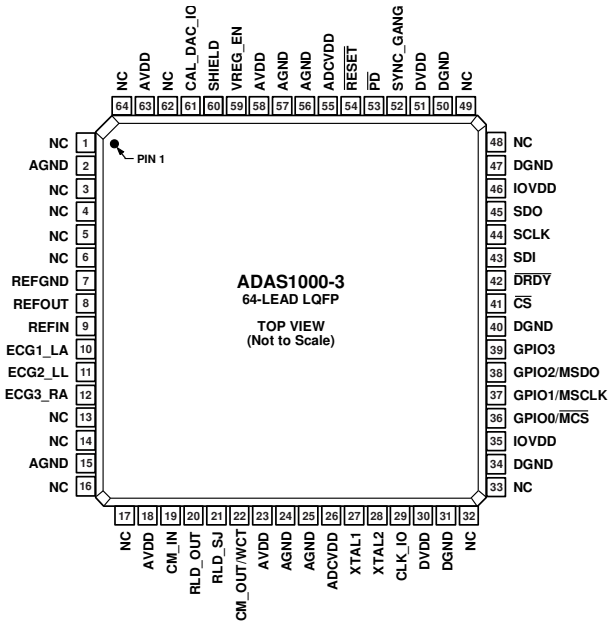
Package Type	θ_{JA}	Unit
56-Lead LFCSP	35	°C/W
64-Lead LQFP	42.5	°C/W

[1] Based on JEDEC standard 4-layer (2S2P) high effective thermal conductivity test board (JESD51-7) and natural convection.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

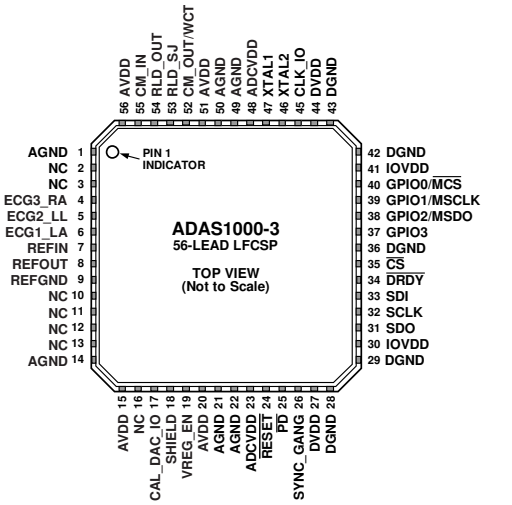
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT.

10997-007

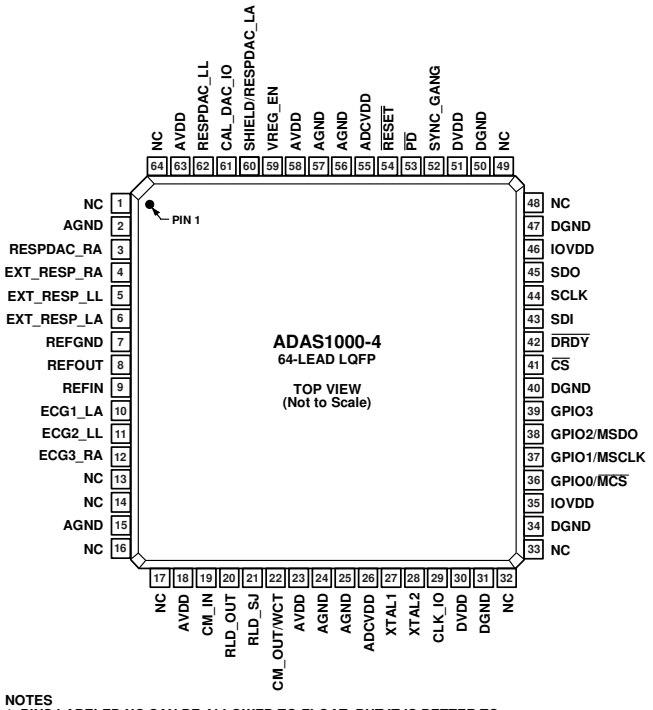
Figure 7. ADAS1000-3, 64-Lead LQFP Pin Configuration



NOTES
1. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT.
2. THE EXPOSED PAD IS ON THE TOP OF THE PACKAGE; IT IS CONNECTED TO THE MOST NEGATIVE POTENTIAL, AGND.

10997-006

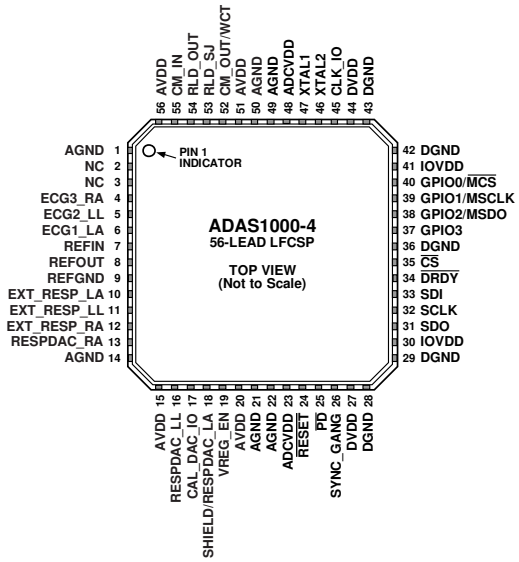
Figure 8. ADAS1000-3, 56-Lead LFCSP Pin Configuration



NOTES
1. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT.

10997-009

Figure 9. ADAS1000-4, 64-Lead LQFP Pin Configuration



NOTES
1. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT.
2. THE EXPOSED PAD IS ON THE TOP OF THE PACKAGE; IT IS CONNECTED TO THE MOST NEGATIVE POTENTIAL, AGND.

10997-008

Figure 10. ADAS1000-4, 56-Lead LFCSP Pin Configuration

Table 9. Pin Function Descriptions

ADAS1000-3 Pin No.		ADAS1000-4 Pin No.			
LQFP	**LFCSP**	**LQFP**	**LFCSP**	**Mnemonic**	**Description**
18, 23, 58, 63	15, 20, 51, 56	18, 23, 58, 63	15, 20, 51, 56	AVDD	Analog Supply. See recommendations for bypass capacitors in the Power Supply, Grounding, and Decoupling Strategy section.
35, 46	30, 41	35, 46	30, 41	IOVDD	Digital Supply for Digital Input/Output Voltage Levels. See recommendations for bypass capacitors in the Power Supply, Grounding, and Decoupling Strategy section.
26, 55	23, 48	26, 55	23, 48	ADCVDD	Analog Supply for ADC. There is an on-chip linear regulator providing the supply voltage for the ADCs. These pins are primarily provided for decoupling purposes; however, the pin may also be supplied by an external 1.8 V supply should the user wish to use a more efficient supply to minimize power dissipation. In this case, use the VREG_EN pin tied to ground to disable the ADCVDD and DVDD regulators. The ADCVDD pin should not be used to supply other functions. See recommendations for bypass capacitors in the Power Supply, Grounding, and Decoupling Strategy section.
30, 51	27, 44	30, 51	27, 44	DVDD	Digital Supply. There is an on-chip linear regulator providing the supply voltage for the digital core. These pins are primarily provided for decoupling purposes; however, the pin may also be overdriven supplied by an external 1.8 V supply should the user wish to use a more efficient supply to minimize power dissipation. In this case, use the VREG_EN pin tied to ground to disable the ADCVDD and DVDD regulators. See recommendations for bypass capacitors in the Power Supply, Grounding, and Decoupling Strategy section.
2, 15, 24, 25, 56, 57	1, 14, 21, 22, 49, 50	2, 15, 24, 25, 56, 57	1, 14, 21, 22, 49, 50	AGND	Analog Ground.
31, 34, 40, 47, 50	28, 29, 36, 42, 43	31, 34, 40, 47, 50	28, 29, 36, 42, 43	DGND	Digital Ground.
59	19	59	19	VREG_EN	Enables or disables the internal voltage regulators used for ADCVDD and DVDD. Tie this pin to AVDD to enable or tie this pin to ground to disable the internal voltage regulators.
10	6	10	6	ECG1_LA	Analog Input, Left Arm (LA).
11	5	11	5	ECG2_LL	Analog Input, Left Leg (LL).
12	4	12	4	ECG3_RA	Analog Input, Right Arm (RA).
		4	12	EXT_RESP_RA	Optional External Respiration Input.
		5	11	EXT_RESP_LL	Optional External Respiration Input.
		6	10	EXT_RESP_LA	Optional External Respiration Input.
		62	16	RESPDAC_LL	Optional Path for Higher Performance Respiration Resolution, Respiration DAC Drive, Negative Side 0.
		60	18	SHIELD/ RESPDAC_LA	Shared Pin (User-Configured). Output of Shield Driver (SHIELD). Optional Path for Higher Performance Respiration Resolution, Respiration DAC Drive, Negative Side 1 (RESPDAC_LA).
60	18			SHIELD	Output of Shield Driver.
		3	13	RESPDAC_RA	Optional Path for Higher Performance Respiration Resolution, Respiration DAC Drive, Positive Side.
22	52	22	52	CM_OUT/WCT	Common-Mode Output Voltage (Average of Selected Electrodes). Not intended to drive current.
19	55	19	55	CM_IN	Common-Mode Input.
21	53	21	53	RLD_SJ	Summing Junction for Right Leg Drive Amplifier.
20	54	20	54	RLD_OUT	Output and Feedback Junction for Right Leg Drive Amplifier.
61	17	61	17	CAL_DAC_IO	Calibration DAC Input/Output. Output for a master device, input for a slave. Not intended to drive current.
9	7	9	7	REFIN	Reference Input. For standalone mode, use REFOUT connected to REFIN. External 10 µF capacitors with ESR < 0.2 Ω in parallel with 0.1 µF bypass capacitors to GND are required and should be placed as close to the pin as possible. An external reference can be connected to REFIN.
8	8	8	8	REFOUT	Reference Output.
7	9	7	9	REFGND	Reference Ground. Connect to a clean ground.
27, 28	47, 46	27, 28	47, 46	XTAL1, XTAL2	External crystal connects between these two pins; external clock drive should be applied to CLK_IO. Each XTAL pin requires a 15 pF capacitor to ground.
29	45	29	45	CLK_IO	Buffered Clock Input/Output. Output for a master device; input for a slave. Powers up in high impedance.
41	35	41	35	$\overline{CS}$	Chip Select and Frame Sync, Active Low. $\overline{CS}$ can be used to frame each word or to frame the entire suite of data in framing mode.

ADAS1000-3 Pin No.		ADAS1000-4 Pin No.			
LQFP	**LFCSP**	**LQFP**	**LFCSP**	**Mnemonic**	**Description**
44	32	44	32	SCLK	Clock Input. Data is clocked into the shift register on a rising edge and clocked out on a falling edge.
43	33	43	33	SDI	Serial Data Input.
53	25	53	25	$\overline{PD}$	Power-Down, Active Low.
45	31	45	31	SDO	Serial Data Output. This pin is used for reading back register configuration data and for the data frames.
42	34	42	34	$\overline{DRDY}$	Digital Output. This pin indicates that conversion data is ready to be read back when low, busy when high. When reading packet data, the entire packet must be read to allow $\overline{DRDY}$ to return high.
54	24	54	24	$\overline{RESET}$	Digital Input. This pin has an internal pull-up resistor. This pin resets all internal nodes to their power-on reset values.
52	26	52	26	SYNC_GANG	Digital Input/Output (Output on Master, Input on Slave). Used for synchronization control where multiple devices are connected together. Powers up in high impedance.
36	40	36	40	GPIO0/$\overline{MCS}$	General-Purpose I/O or Master 128 kHz SPI $\overline{CS}$.
37	39	37	39	GPIO1/MSCLK	General-Purpose I/O or Master 128 kHz SPI SCLK.
38	38	38	38	GPIO2/MSDO	General-Purpose I/O or Master 128 kHz SPI SDO.
39	37	39	37	GPIO3	General-Purpose I/O.
1, 3, 4, 5, 6, 13, 14, 16, 17, 32, 33, 48, 49, 62, 64	2, 3, 10, 11, 12, 13, 16	1, 13, 14, 16, 17, 32, 33, 48, 49, 64	2, 3	NC	No connect. Do not connect to these pins (see Figure 7, Figure 8, Figure 9, and Figure 10).
	57		57	EPAD	Exposed Pad. The exposed pad is on the top of the package; it is connected to the most negative potential, AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

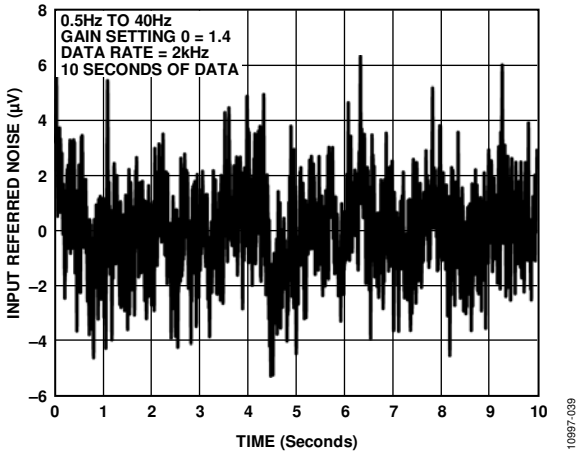


Figure 11. Input Referred Noise for 0.5 Hz to 40 Hz Bandwidth, 2 kHz Data Rate, GAIN 0 (1.4)

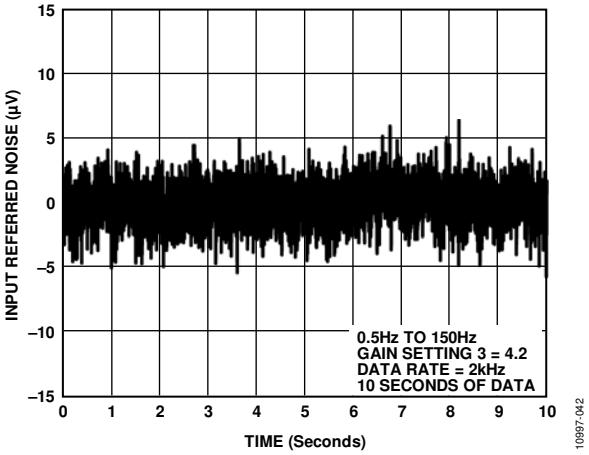


Figure 14. Input Referred Noise for 0.5 Hz to 150 Hz Bandwidth, 2 kHz Data Rate, GAIN 3 (4.2)

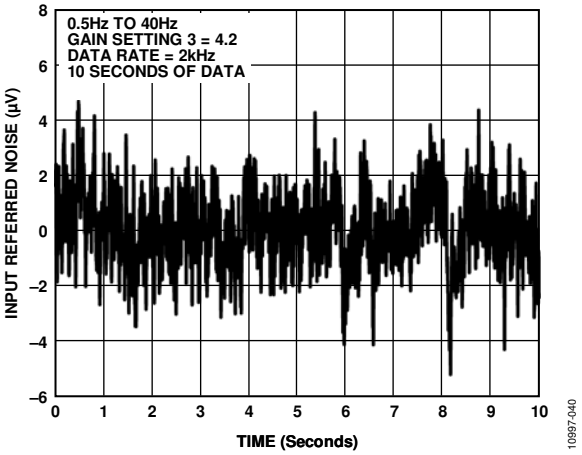


Figure 12. Input Referred Noise for 0.5 Hz to 40 Hz Bandwidth, 2 kHz Data Rate, GAIN 3 (4.2)

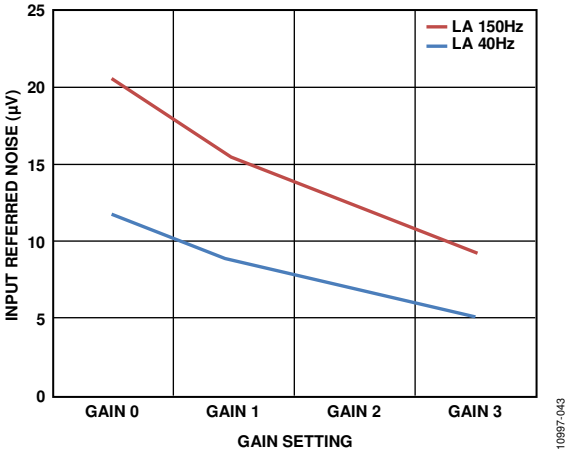


Figure 15. ECG Channel Noise Performance over a 0.5 Hz to 40 Hz or 0.5 Hz to 150 Hz Bandwidth vs. Gain Setting

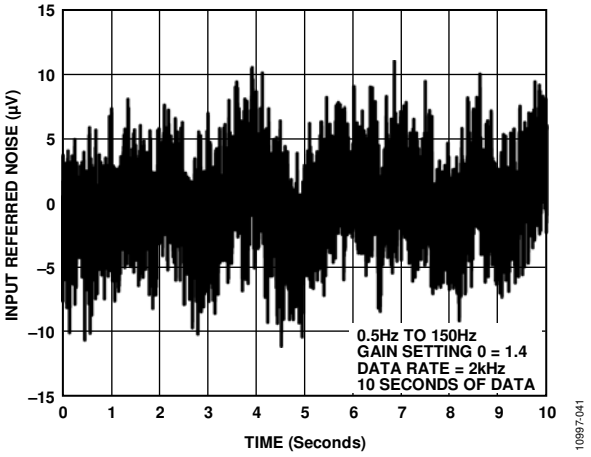


Figure 13. Input Referred Noise for 0.5 Hz to 150 Hz Bandwidth, 2 kHz Data Rate, GAIN 0 (1.4)

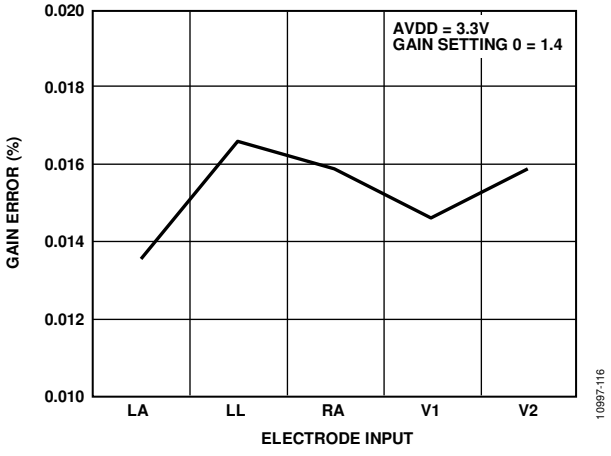


Figure 16. Typical Gain Error Across Channels

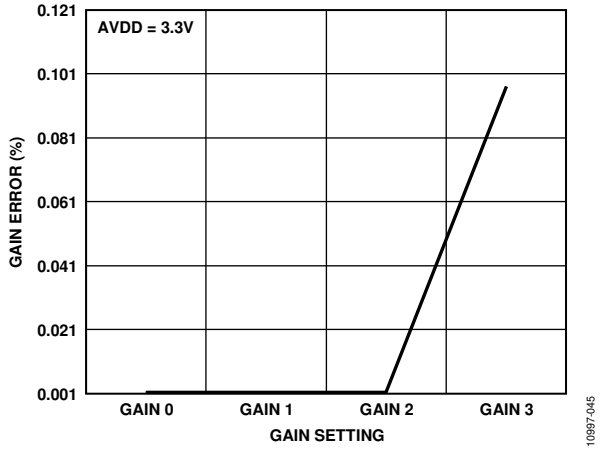


Figure 17. Typical Gain Error vs. Gain

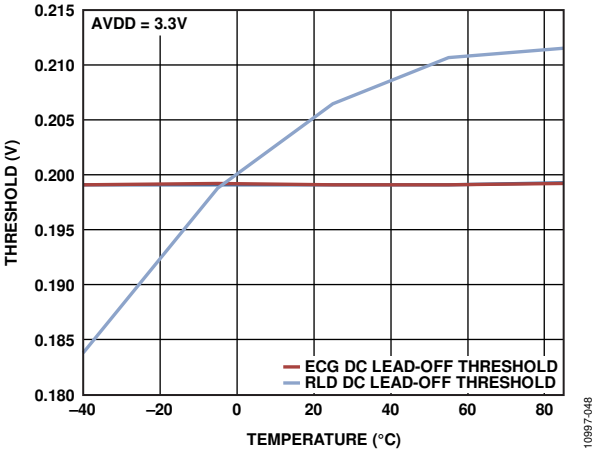


Figure 20. DC Lead-Off Comparator Low Threshold vs. Temperature

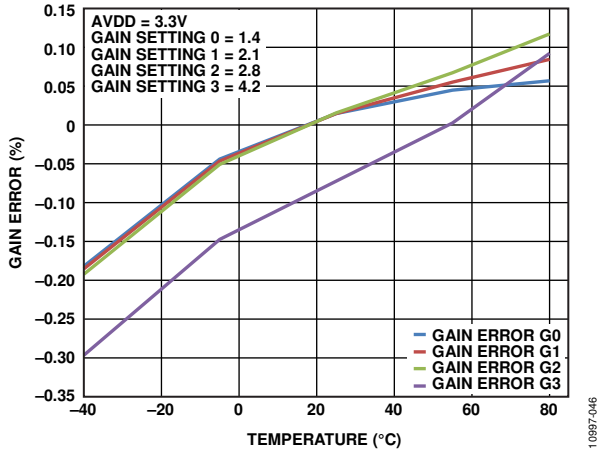


Figure 18. Typical Gain Error for All Gain Settings Across Temperature

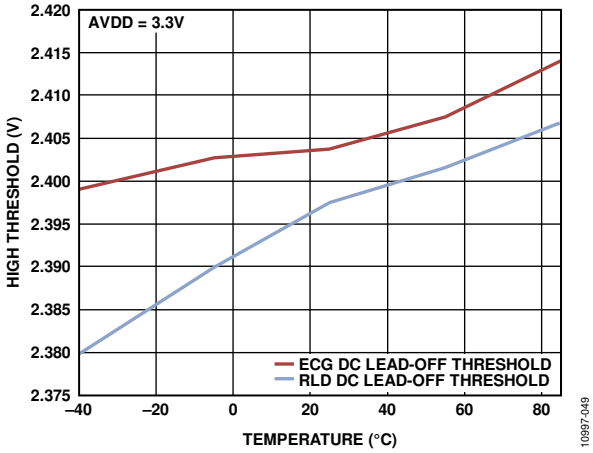


Figure 21. DC Lead-Off Comparator High Threshold vs. Temperature

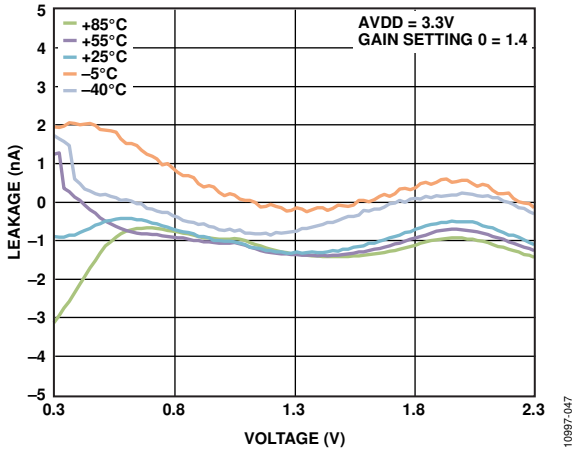


Figure 19. Typical ECG Channel Leakage Current over Input Voltage Range vs. Temperature

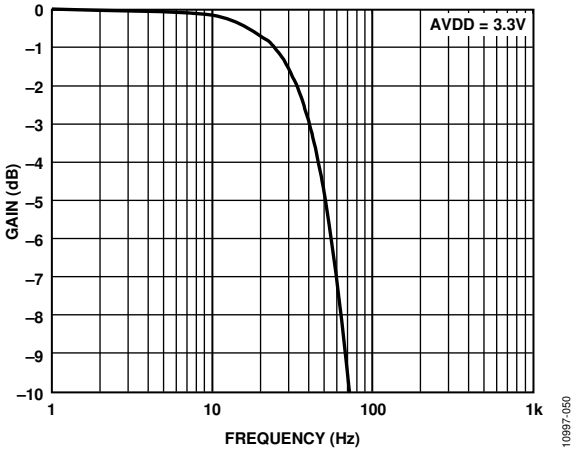


Figure 22. Filter Response with 40 Hz Filter Enabled, 2 kHz Data Rate; See Figure 72 for Digital Filter Overview

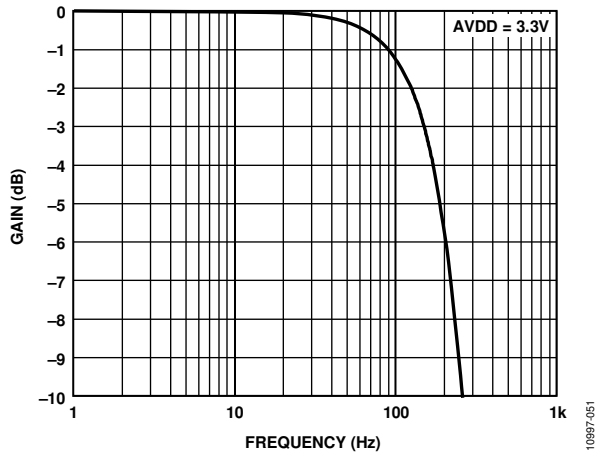


Figure 23. Filter Response with 150 Hz Filter Enabled, 2 kHz Data Rate; See Figure 72 for Digital Filter Overview

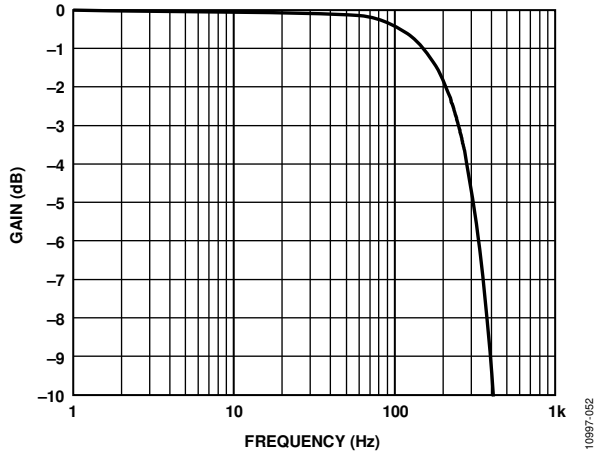


Figure 24. Filter Response with 250 Hz Filter Enabled, 2 kHz Data Rate; See Figure 72 for Digital Filter Overview

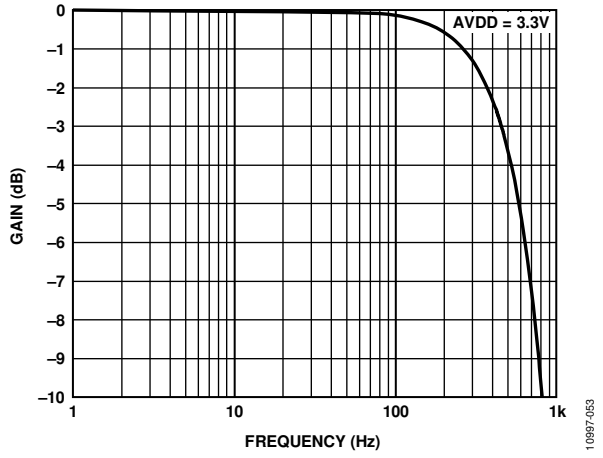


Figure 25. Filter Response with 450 Hz Filter Enabled, 2 kHz Data Rate; See Figure 72 for Digital Filter Overview

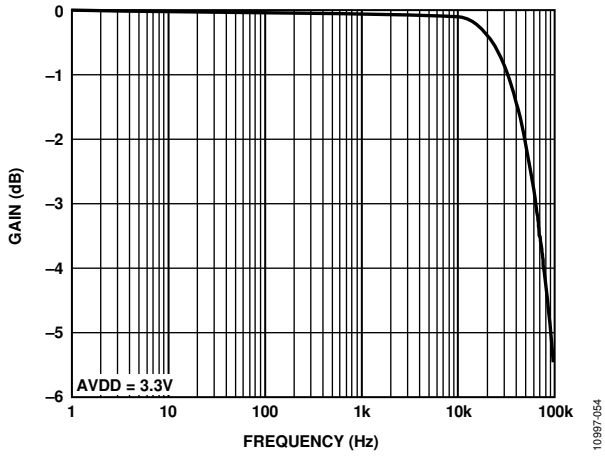


Figure 26. Analog Channel Bandwidth

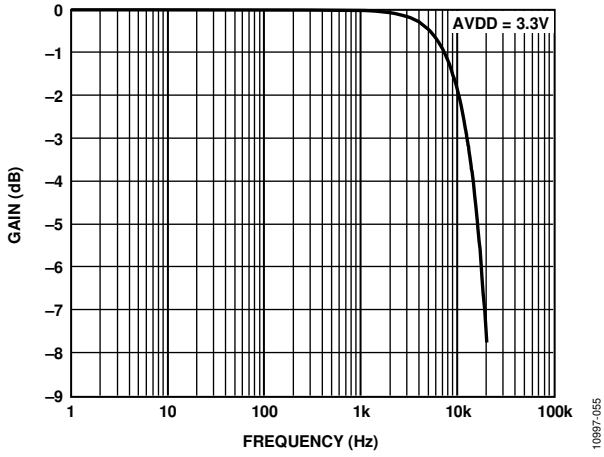


Figure 27. Filter Response Running at 128 kHz Data Rate; See Figure 72 for Digital Filter Overview

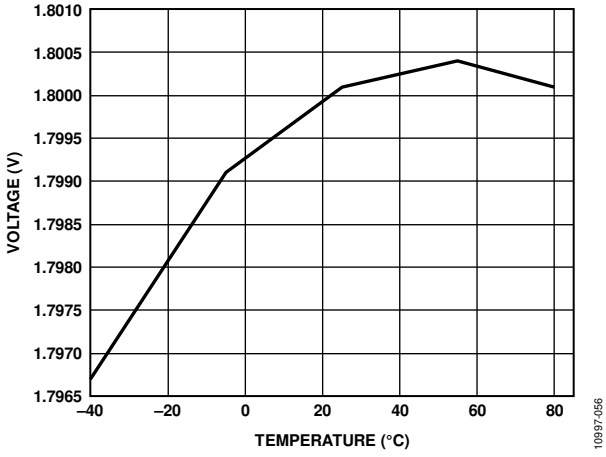


Figure 28. Typical Internal VREF vs. Temperature

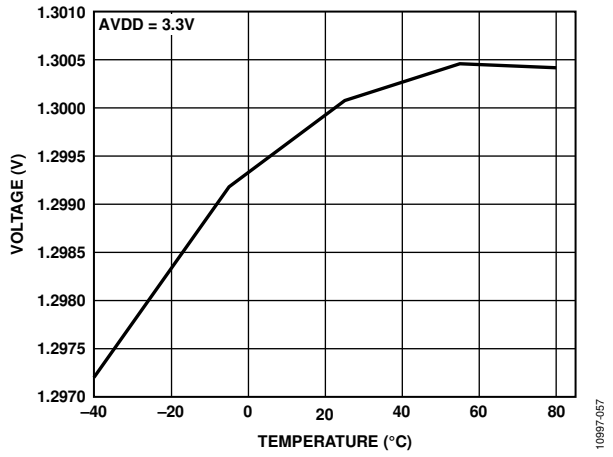


Figure 29. VCM_REF vs. Temperature

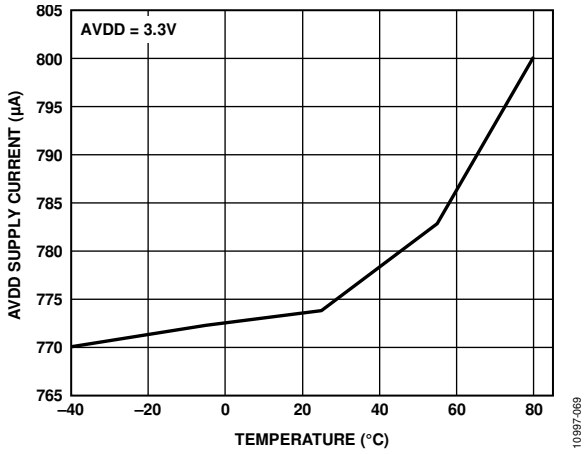


Figure 32. Typical AVDD Supply Current vs. Temperature in Standby Mode

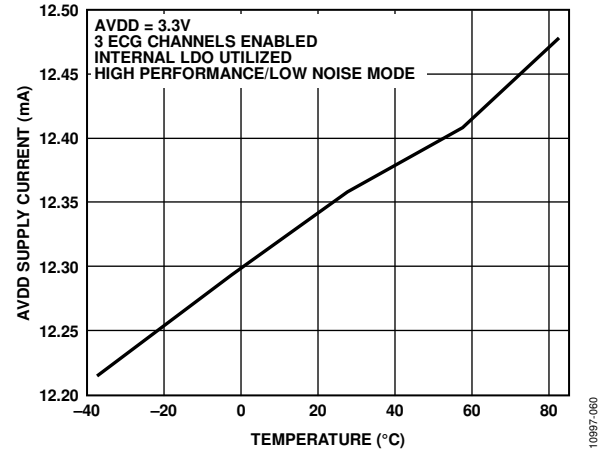


Figure 30. Typical AVDD Supply Current vs. Temperature, Using Internal ADVCDD/DVDD Supplies

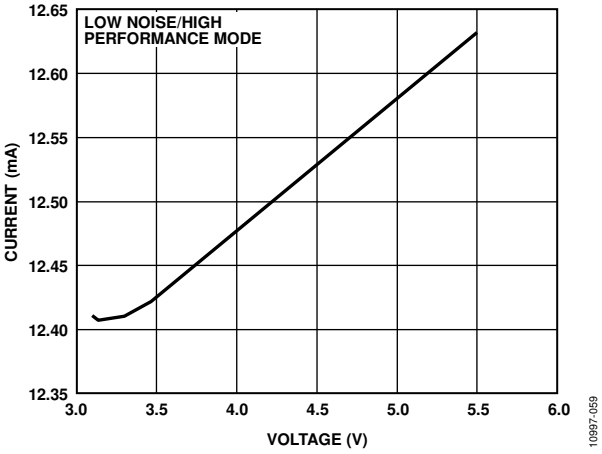


Figure 33. Typical AVDD Supply Current vs. AVDD Supply Voltage

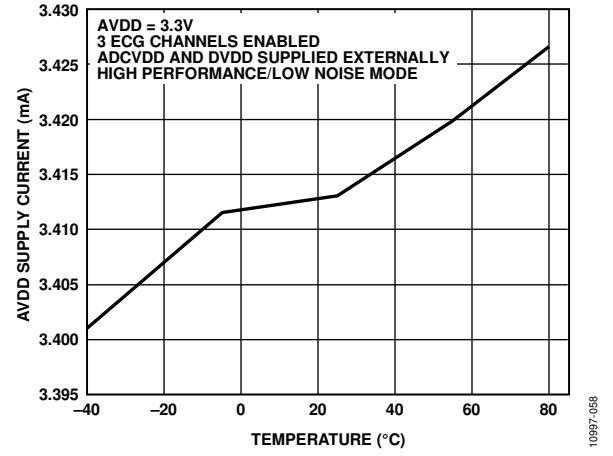


Figure 31. Typical AVDD Supply Current vs. Temperature, Using Externally Supplied ADVCDD/DVDD

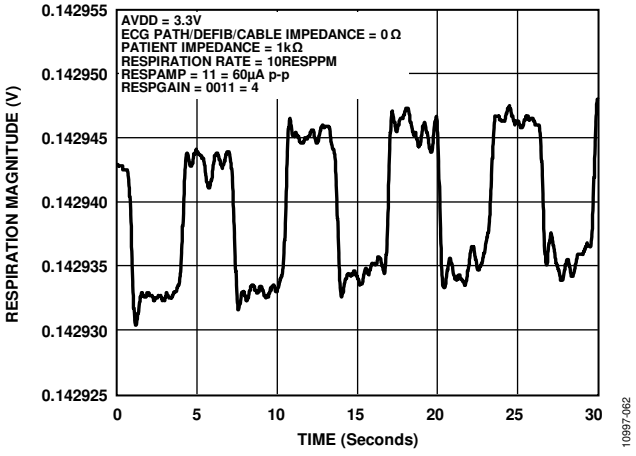


Figure 34. Respiration with 200 mΩ Impedance Variation, Using Internal Respiration Paths and Measured with a 0 Ω Patient Cable

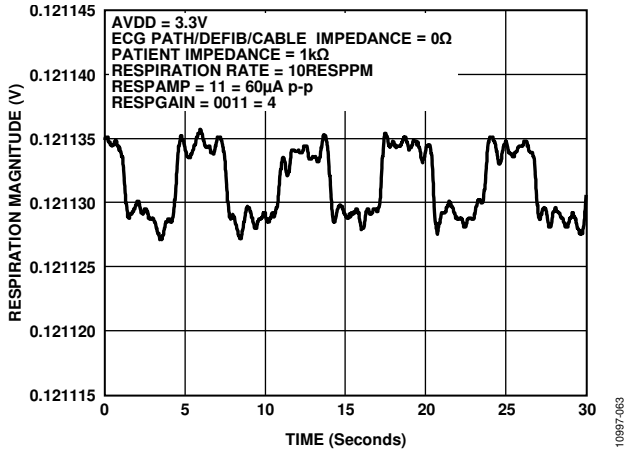


Figure 35. Respiration with 100 mΩ Impedance Variation, Using Internal Respiration Paths and Measured with a 0 Ω Patient Cable

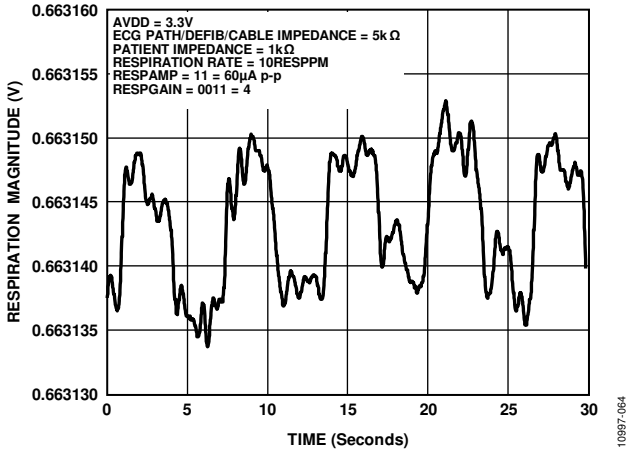


Figure 36. Respiration with 200 mΩ Impedance Variation, Using Internal Respiration Paths and Measured with a 5 kΩ Patient Cable

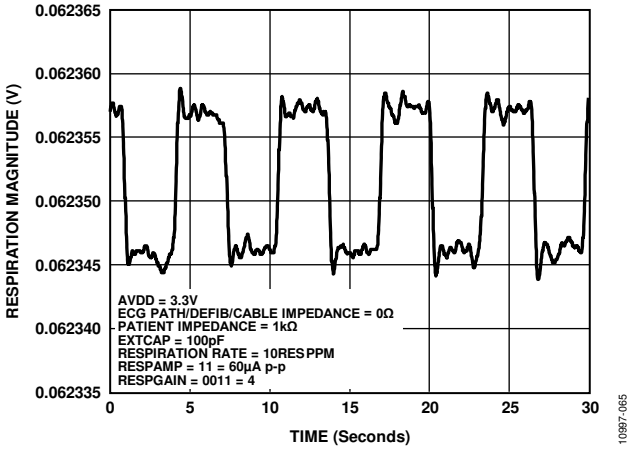


Figure 37. Respiration with 200 mΩ Impedance Variation, Using External Respiration DAC Driving a 100 pF External Capacitor and Measured with a 0 Ω Patient Cable

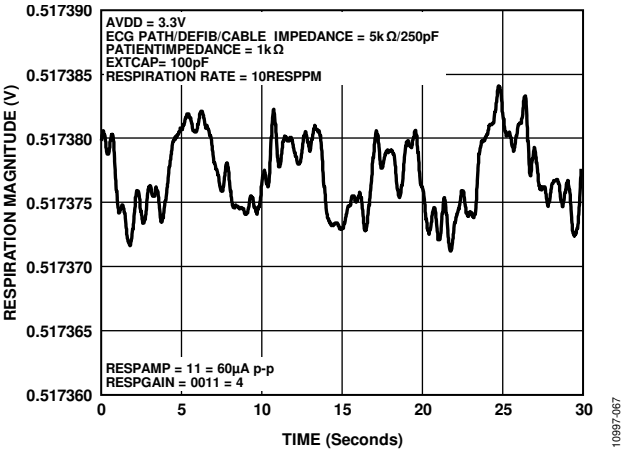


Figure 38. Respiration with 200 mΩ Impedance Variation, Using External Respiration DAC Driving a 100 pF External Capacitor and Measured with a 5 kΩ Patient Cable

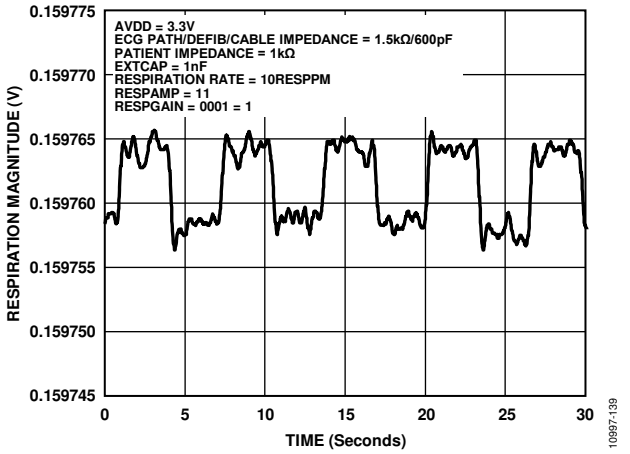


Figure 39. Respiration with 200 mΩ Impedance Variation, Using External Respiration DAC Driving a 1 nF External Capacitor and Measured with a 1.5 kΩ Patient Cable

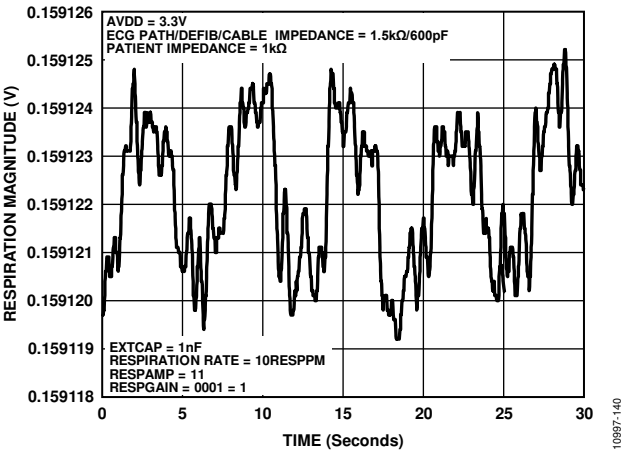


Figure 40. Respiration with 100 mΩ Impedance Variation, Using an External Respiration DAC Driving a 1 nF External Capacitor and Measured with a 1.5 kΩ Patient Cable

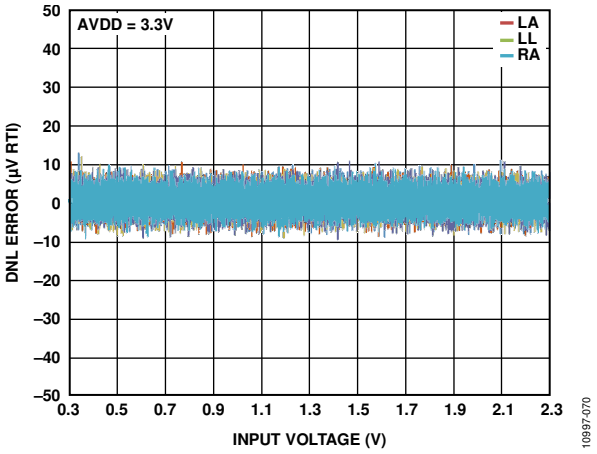


Figure 41. DNL Error vs. Input Voltage Range Across Electrodes at 25°C

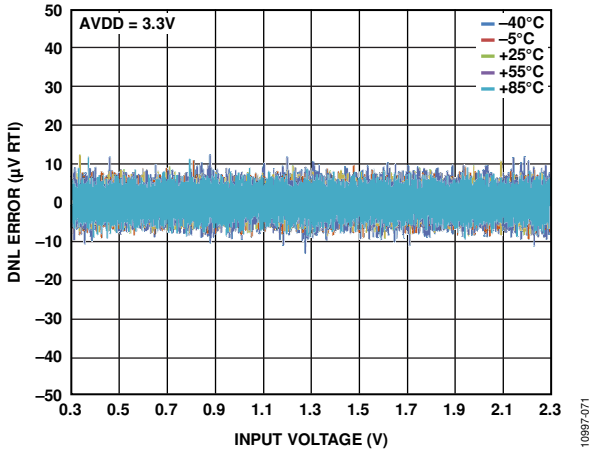


Figure 42. DNL Error vs. Input Voltage Range Across Temperature

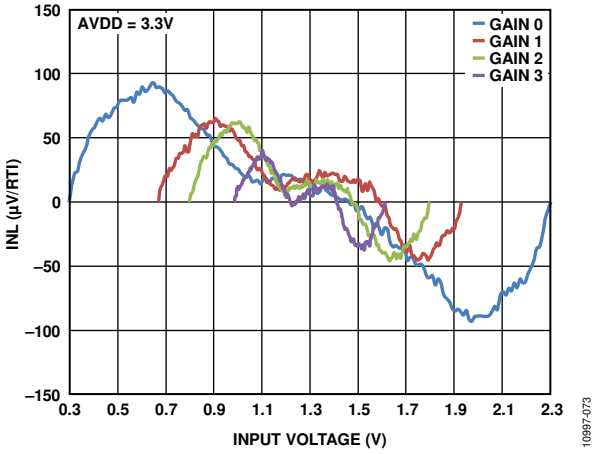


Figure 43. INL vs. Input Voltage Across Gain Setting for 2 kHz Data Rate

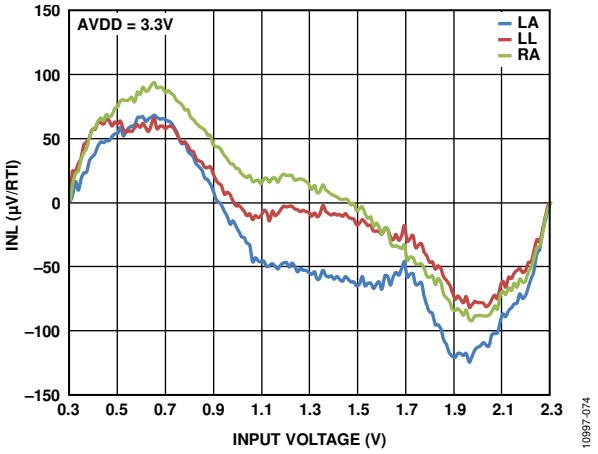


Figure 44. INL vs. Input Voltage Across Electrode Channel for 2 kHz Data Rate

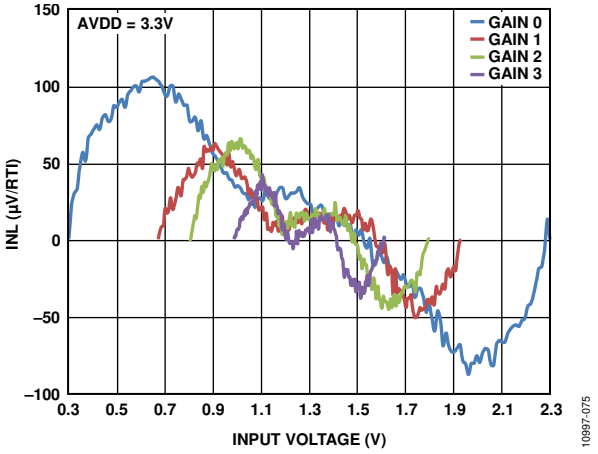


Figure 45. INL vs. Input Voltage Across Gain Setting for 16 kHz Data Rate

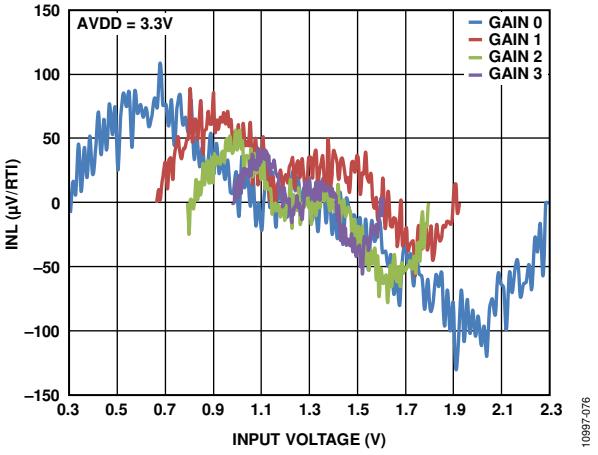


Figure 46. INL vs. Input Voltage Across Gain Setting for 128 kHz Data Rate

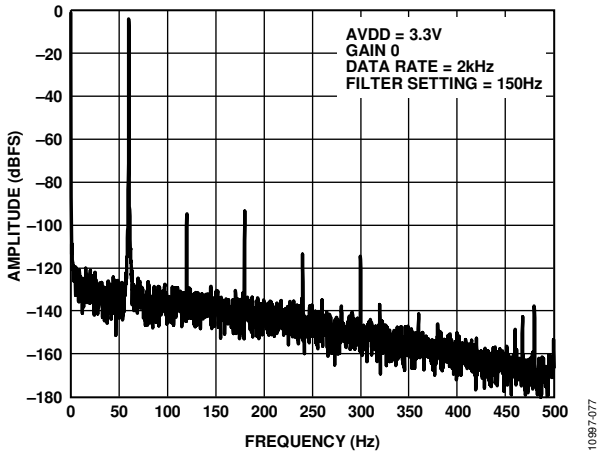


Figure 47. FFT with 60 Hz Input Signal

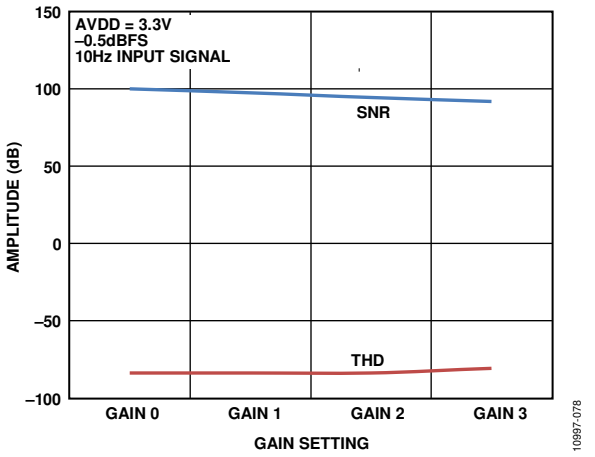


Figure 48. SNR and THD Across Gain Settings

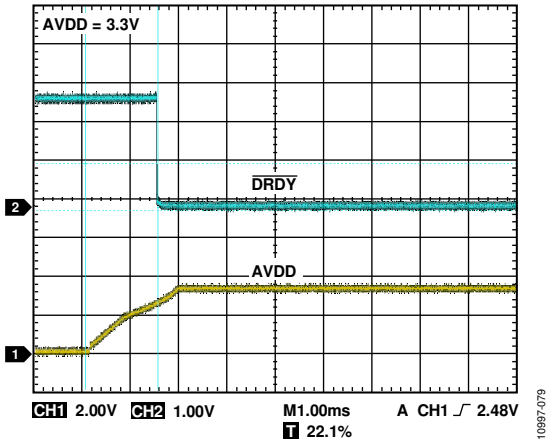


Figure 49. Power Up AVDD Line to $\overline{DRDY}$ Going Low (Ready)

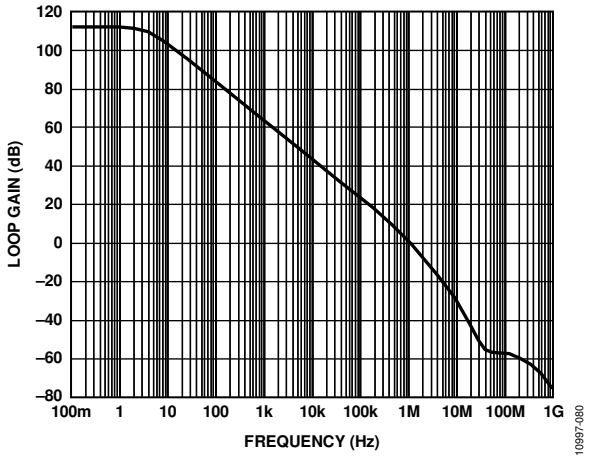


Figure 50. Open-Loop Gain Response of Right Leg Drive Amplifier Without Loading

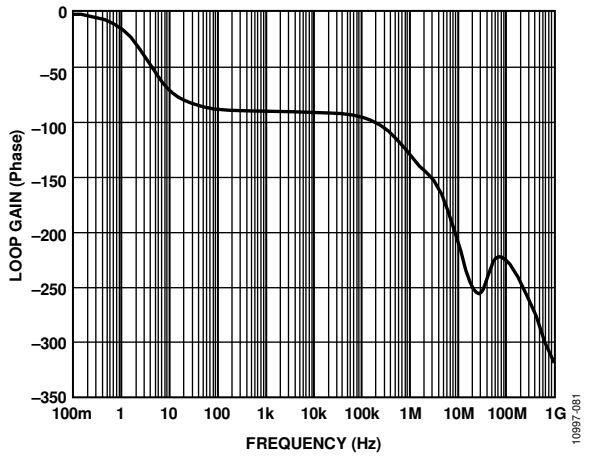


Figure 51. Open-Loop Phase Response of Right Leg Drive Amplifier Without Loading

APPLICATIONS INFORMATION

OVERVIEW

The ADAS1000-3/ADAS1000-4 are electro cardiac (ECG) front-end solutions targeted at a variety of medical applications. In addition to ECG measurements, the ADAS1000-3/ADAS1000-4 also measure thoracic impedance (respiration) and detect pacing artifacts, providing all the measured information to the host controller in the form of a data frame supplying either lead/vector or electrode data at programmable data rates. The ADAS1000-3/ADAS1000-4 are designed to simplify the task of acquiring ECG signals for use in both monitor and diagnostic applications. Value-added cardiac post processing may be executed externally on a DSP, microprocessor, or FPGA. The ADAS1000-3/ADAS1000-4 are designed for operation in both low power, portable telemetry applications and line powered systems; therefore, the parts offer power/noise scaling to ensure suitability to these varying requirements.

The devices also offer a suite of dc and ac test excitation via a calibration DAC feature and CRC redundancy checks in addition to readback of all relevant register address space.

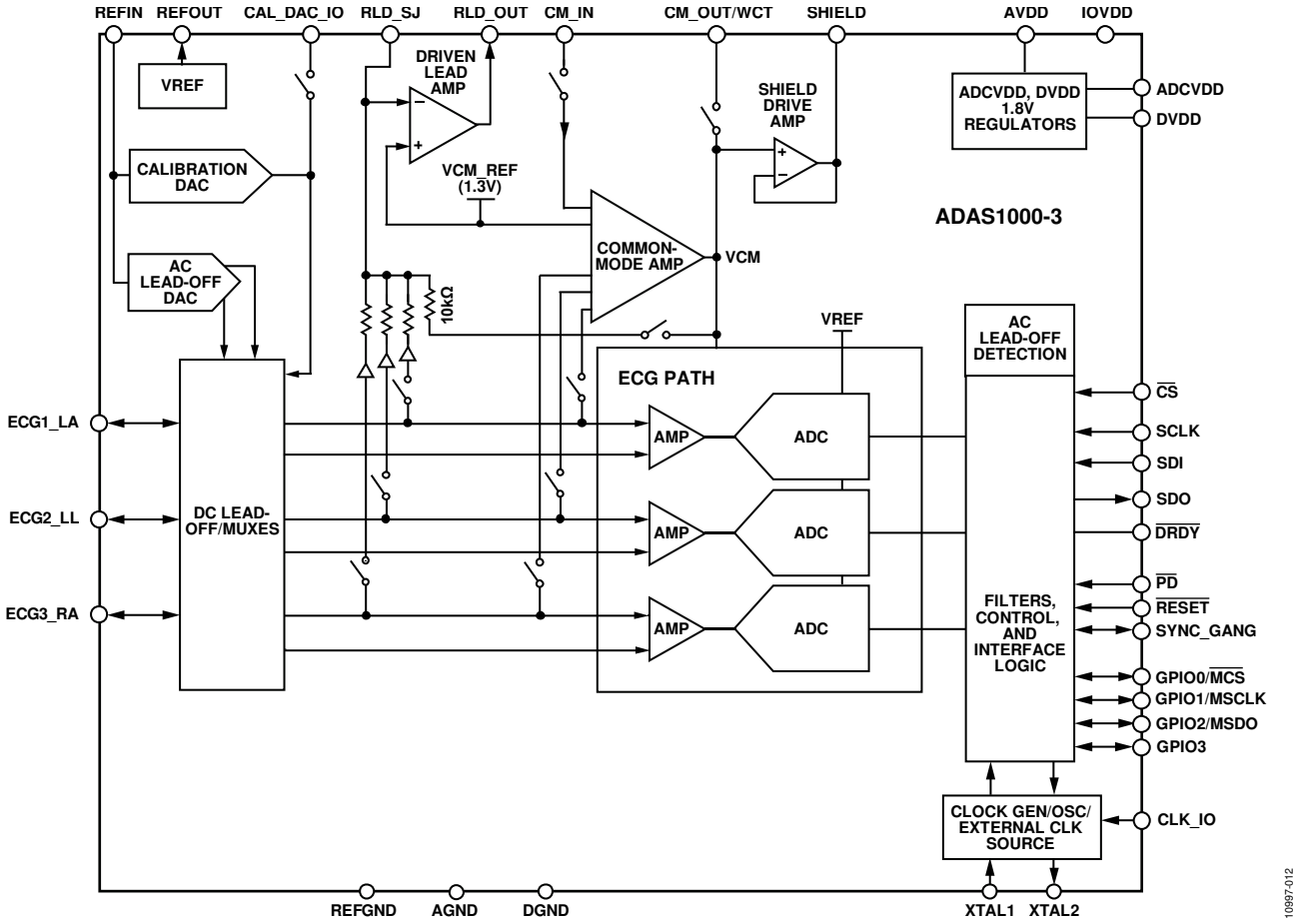


Figure 52. ADAS1000-3 Simplified Block Diagram