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FEATURES

- Ease of use—16-bit, 1 MSPS complete data acquisition system**
- High impedance, 8-channel input: >500 MΩ**
- Differential input voltage range: ±24.576 V maximum**
- High input common-mode rejection: >100 dB**
- User-programmable input ranges**
- Channel sequencer with individual channel gains**
- On-chip 4.096 V reference and buffer**
- Auxiliary input—direct interface to PuISAR ADC inputs**
- No latency or pipeline delay (SAR architecture)**
- Serial 4-wire, 1.8 V to 5 V SPI-/SPORT-compatible interface**
- LFCSP package (6 mm × 6 mm)**
- 40°C to +85°C industrial temperature range**

APPLICATIONS

- Multichannel data acquisition and system monitoring**
- Process control**
- Power line monitoring**
- Automated test equipment**
- Instrumentation**

GENERAL DESCRIPTION

The ADAS3022 is a complete 16-bit, 1 MSPS, successive approximation-based analog-to-digital data acquisition system, which is manufactured on Analog Devices, Inc., proprietary iCMOS® high voltage industrial process technology. The device integrates an 8-channel, low leakage multiplexer; a high impedance programmable gain instrumentation amplifier (PGIA) stage with high common-mode rejection; a precision, low drift 4.096 V reference

and buffer; and a 16-bit charge redistribution analog-to-digital converter (ADC) with successive approximation register (SAR) architecture. The ADAS3022 can resolve eight single-ended inputs or four fully differential inputs up to ±24.576 V when using ±15 V supplies. In addition, the device can accept the commonly used bipolar differential, bipolar single-ended, pseudo bipolar, or pseudo unipolar input signals, as shown in Table 1, thus enabling the use of almost any direct sensor interface.

The ADAS3022 simplifies design challenges by eliminating signal buffering, level shifting, amplification/attenuation, common-mode rejection, settling time, and any other analog signal conditioning challenge while allowing a smaller form factor, faster time to market, and lower cost.

Table 1. Typical Input Range Selection

Signal	Input Range, V _{IN}
Differential	
±1 V	±1.28 V
±2.5 V	±2.56 V
±5 V	±5.12 V
±10 V	±10.24 V
Single Ended ¹	
0 V to 1 V	±1.28 V
0 V to 2.5 V	±2.56 V
0 V to 5 V	±5.12 V
0 V to 10 V	±10.24 V

¹ See Figure 59 and Figure 60 in the Analog Inputs section for more information.

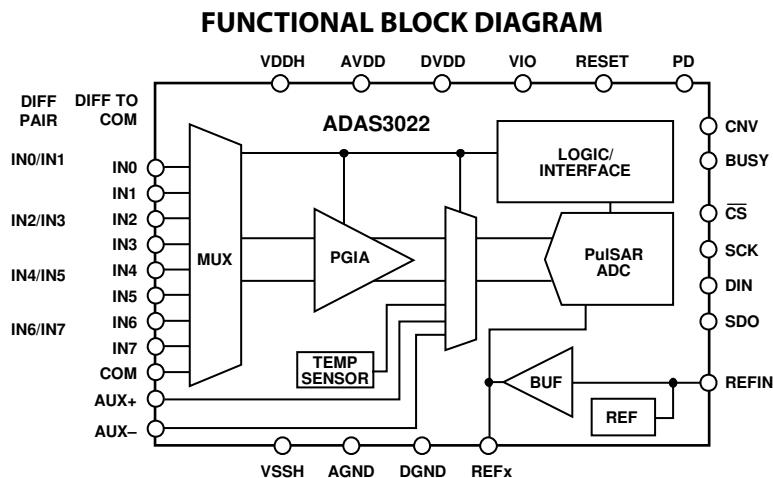


Figure 1.

Rev. C

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COMPARABLE PARTS

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EVALUATION KITS

- ADAS3022 Evaluation Kit

DOCUMENTATION

Data Sheet

- ADAS3022: 16-Bit, 1 MSPS, 8-Channel Data Acquisition System Data Sheet

User Guides

- UG-484: Evaluation Board for the ADAS3022 16-Bit, 8-Channel, 1 MSPS Data Acquisition System

TOOLS AND SIMULATIONS

- ADAS3022 FPGA Reference Design
- ADAS3022/ADAS3023 IBIS Model

REFERENCE DESIGNS

- CN0201

REFERENCE MATERIALS

Press

- Analog Devices' Data Acquisition IC Simplifies Industrial and Instrumentation Equipment Design

Technical Articles

- Exploring Different SAR ADC Analog Input Architectures
- Komplette Sensor-to-Bits-Lösung: Vereinfachte Entwicklung industrieller Datenerfassungssysteme
- Let's Compare SAR & Δ - Σ Converters for a Mux'd DAS (Planet Analog, 12/2013)
- Sensor-To-Bits: Simplifying DAQ Design

DESIGN RESOURCES

- ADAS3022 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADAS3022 EngineerZone Discussions.

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REVISION HISTORY

2/14—Rev. B to Rev. C

Change to Figure 49	19
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Added On Demand Conversion Mode Section and Table 12; Renumbered Sequentially.....	37
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4/13—Rev. A to Rev. B

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1/13—Rev. 0 to Rev. A

Removed Endnote 3 and Added T _A = 25°C to Gain Error Test Conditions/Comments, Table 2.....	3
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Added Figure 25 to Figure 28; Renumbered Sequentially	15
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11/12—Revision 0: Initial Version

SPECIFICATIONS

VDDH = 15 V ± 5%, VSSH = -15 V ± 5%, AVDD = DVDD = 5 V ± 5%, VIO = 1.8 V to AVDD, internal reference, V_{REF} = 4.096 V, f_s = 1 MSPS. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit ¹
RESOLUTION		16			Bits
ANALOG INPUTS—IN[7:0], COM					
Operating Input Voltage Range	V _{IN}	-VSSH + 2.5		VDDH - 2.5	V
Differential Input Voltage Range, V _{IN}	V _{IN+} - V _{IN-}				
	PGIA gain = 0.16, V _{IN} = 49.15 V p-p	-6V _{REF}		+6V _{REF}	V
	PGIA gain = 0.2, V _{IN} = 40.96 V p-p	-5V _{REF}		+5V _{REF}	V
	PGIA gain = 0.4, V _{IN} = 20.48 V p-p	-2.5V _{REF}		+2.5V _{REF}	V
	PGIA gain = 0.8, V _{IN} = 10.24 V p-p	-1.25V _{REF}		+1.25V _{REF}	V
	PGIA gain = 1.6, V _{IN} = 5.12 V p-p	-0.625V _{REF}		+0.625V _{REF}	V
	PGIA gain = 3.2, V _{IN} = 2.56 V p-p	-0.3125V _{REF}		+0.3125V _{REF}	V
	PGIA gain = 6.4, V _{IN} = 1.28 V p-p	-0.1563V _{REF}		+0.1563V _{REF}	V
Input Impedance	Z _{IN}	500			MΩ
Channel Off Leakage			±0.6		nA
Channel On Leakage			±0.02		nA
Common-Mode Voltage Range ²	V _{IN+} , V _{IN-} ; full-scale differential inputs				
	PGIA gain = 0.4	-5.12		+5.12	V
	PGIA gain = 0.8	-7.68		+7.68	V
	PGIA gain = 1.6	-8.96		+8.96	V
	PGIA gain = 3.2	-9.60		+9.60	V
	PGIA gain = 6.4	-9.92		+9.92	V
ANALOG INPUTS—AUX+, AUX-					
Differential Input Voltage Range		-V _{REF}		+V _{REF}	V
THROUGHPUT					
Conversion Rate	One channel/one pair	0		1000	kSPS
	Two channels/two pairs	0		500	kSPS
	Four channels/four pairs	0		250	kSPS
	Eight channels	0		125	kSPS
Transient Response	Full-scale step			520	ns
DC ACCURACY					
No Missing Codes		16			Bits
Integral Linearity Error	PGIA gain = 0.16, 0.2, 0.4, 0.8, 1.6	-2	±0.6	+2	LSB
	PGIA gain = 3.2	-3	±1.0	+3	LSB
	PGIA gain = 6.4	-5	±1.5	+5	LSB
Differential Linearity Error	PGIA gain = 0.16, 0.2, 0.4, 0.8, 1.6	-0.9	±0.6	+1.0	LSB
	PGIA gain = 3.2	-0.9	±0.75	+1.25	LSB
	PGIA gain = 6.4	-0.9	±0.75	+1.25	LSB
Transition Noise	External reference				
	PGIA gain = 0.16, 0.2, 0.4, 0.8, 1.6		5		LSB
	PGIA gain = 3.2		7		LSB
	PGIA gain = 6.4		11		LSB
Gain Error	External reference, all PGIA gains, T _A = 25°C	-9		+9	LSB
Gain Error Temperature Drift	External reference, all PGIA gains			0.1	ppm/°C
Offset Error	External reference, T _A = 25°C				
	PGIA gain = 0.16, 0.2, 0.4, 0.8	-3.0	+0.2	+3.0	LSB
	PGIA gain = 1.6	-4.0	+0.2	+4.0	LSB
	PGIA gain = 3.2	-7.5	+0.2	+7.5	LSB
	PGIA gain = 6.4	-12.5	+0.2	+12.5	LSB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit ¹
Offset Error Temperature Drift	External reference				
	PGIA gain = 0.16, 0.2, 0.4, 0.8		0.1	0.5	ppm/°C
	PGIA gain = 1.6		0.2	1.0	ppm/°C
	PGIA gain = 3.2		0.4	2.0	ppm/°C
Total Unadjusted Error	PGIA gain = 6.4		0.8	4.0	ppm/°C
	External reference, T _A = 25°C				
	PGIA gain = 0.16, 0.2, 0.4, 0.8, 1.6, 3.2	-9		+9	LSB
	PGIA gain = 6.4	-15		+15	LSB
AC ACCURACY³					
Signal-to-Noise Ratio (SNR)	f _{IN} = 10 kHz				
	PGIA gain = 0.16	90.0	91.5		dB
	PGIA gain = 0.2	90.0	91.5		dB
	PGIA gain = 0.4	89.5	91.5		dB
	PGIA gain = 0.8	89.0	91.0		dB
	PGIA gain = 1.6	88.0	89.7		dB
	PGIA gain = 3.2	86.0	86.8		dB
	PGIA gain = 6.4	83.0	84.5		dB
Signal-to-Noise-and-Distortion (SINAD)	f _{IN} = 10 kHz				
	PGIA gain = 0.16	88.0	90.0		dB
	PGIA gain = 0.2	88.0	90.0		dB
	PGIA gain = 0.4	88.5	91.0		dB
	PGIA gain = 0.8	88.5	90.5		dB
	PGIA gain = 1.6	87.5	89.5		dB
	PGIA gain = 3.2	85.5	86.5		dB
	PGIA gain = 6.4	82.5	84.0		dB
Dynamic Range	f _{IN} = 10 kHz, -60 dB input				
	PGIA gain = 0.16	91.0	92.0		dB
	PGIA gain = 0.2	91.0	92.0		dB
	PGIA gain = 0.4	90.5	91.5		dB
	PGIA gain = 0.8	90.0	91.0		dB
	PGIA gain = 1.6	89.0	90.0		dB
	PGIA gain = 3.2	86.0	87.0		dB
	PGIA gain = 6.4	83.5	85.0		dB
Total Harmonic Distortion	f _{IN} = 10 kHz, all PGIA gains		-100		dB
Spurious-Free Dynamic Range	f _{IN} = 10 kHz, all PGIA gains		101		dB
Channel-to-Channel Crosstalk	f _{IN} = 10 kHz, all channels inactive		-120		dB
Common-Mode Rejection Ratio (CMRR)	f _{IN} = 2 kHz				
	PGIA gain = 0.16, 0.2, 0.4, 0.8	90.0	110.0		dB
	PGIA gain = 1.6	90.0	105.0		dB
	PGIA gain = 3.2	90.0	98.0		dB
	PGIA gain = 6.4	90.0	98.0		dB
-3 dB Input Bandwidth	-40 dBFS		8		MHz
AUXILIARY ADC INPUT CHANNEL					
DC Accuracy	External reference				
Integral Nonlinearity Error		-1.5	±0.5	+1.5	LSB
Differential Nonlinearity Error		-0.8	±0.6	+1.0	LSB
Gain Error		-2.5	±0.2	+2.5	LSB
Offset Error		-5	±0.2	+5	LSB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit ¹
AC Performance	Internal reference				
Signal-to-Noise Ratio (SNR)		90.0	93.0		dB
Signal-to-Noise-and-Distortion (SINAD)		89.5	92.5		dB
Total Harmonic Distortion			-105		dB
Spurious-Free Dynamic Range (SFDR)			110		dB
INTERNAL REFERENCE					
REFx Output Voltage	$T_A = 25^\circ\text{C}$	4.088	4.096	4.104	V
REFx Output Current	$T_A = 25^\circ\text{C}$		250		μA
REFx Temperature Drift	REFEN = 1		± 5		ppm/ $^\circ\text{C}$
	REFEN = 0		± 1		ppm/ $^\circ\text{C}$
REFx Line Regulation	AVDD = 5 V \pm 5%				
Internal Reference			20		$\mu\text{V/V}$
Buffer Only			4		$\mu\text{V/V}$
REFIN Output Voltage ⁴	$T_A = 25^\circ\text{C}$	2.495	2.500	2.505	V
Turn-On Settling Time	$C_{\text{REFIN}}, C_{\text{REF1}}, C_{\text{REF2}} = 10 \mu\text{F}$ and $0.1 \mu\text{F}$		100		ms
EXTERNAL REFERENCE					
Voltage Range	REFx input	4.000	4.096	4.104	V
	REFIN input (buffered)		2.5	2.505	V
Current Drain	$V_{\text{REF}} = 4.096 \text{ V}$		100		μA
TEMPERATURE SENSOR					
Output Voltage	$T_A = 25^\circ\text{C}$		275		mV
Temperature Sensitivity			800		$\mu\text{V}/^\circ\text{C}$
DIGITAL INPUTS					
Logic Levels					
V_{IL}	$V_{\text{IO}} > 3 \text{ V}$	-0.3		$+0.3 \times V_{\text{IO}}$	V
V_{IH}	$V_{\text{IO}} > 3 \text{ V}$	$0.7 \times V_{\text{IO}}$		$V_{\text{IO}} + 0.3$	V
V_{IL}	$V_{\text{IO}} \leq 3 \text{ V}$	-0.3		$+0.1 \times V_{\text{IO}}$	V
V_{IH}	$V_{\text{IO}} \leq 3 \text{ V}$	$0.9 \times V_{\text{IO}}$		$V_{\text{IO}} + 0.3$	V
I_{IL}		-1		+1	μA
I_{IH}		-1		+1	μA
DIGITAL OUTPUTS ⁵					
Data Format			Twos complement		
V_{OL}	$I_{\text{SINK}} = +500 \mu\text{A}$			0.4	V
V_{OH}	$I_{\text{SOURCE}} = -500 \mu\text{A}$	$V_{\text{IO}} - 0.3$			V
POWER SUPPLIES	PD = 0				
VIO		1.8		AVDD + 0.3	V
AVDD		4.75	5	5.25	V
DVDD		4.75	5	5.25	V
VDDH ⁶	VDDH > input voltage + 2.5 V	14.25	15	15.75	V
VSSH ⁶	VSSH < input voltage - 2.5 V	-15.75	-15	-14.25	V
I_{VDDH}	PGIA gain = 0.16		3.0	3.5	mA
	PGIA gain = 0.2		3.0	3.5	mA
	PGIA gain = 0.4		3.5	4.0	mA
	PGIA gain = 0.8		5.0	5.5	mA
	PGIA gain = 1.6		8.5	9.5	mA
	PGIA gain = 3.2		15.5	17.5	mA
	PGIA gain = 6.4		15.5	17.5	mA
	All PGIA gains, PD = 1		100		μA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit ¹
I _{VSSH}	PGIA gain = 0.16	-3.0	-2.5		mA
	PGIA gain = 0.2	-3.0	-2.5		mA
	PGIA gain = 0.4	-3.5	-3.0		mA
	PGIA gain = 0.8	-5.5	-4.5		mA
	PGIA gain = 1.6	-9.5	-8.0		mA
	PGIA gain = 3.2	-17.5	-15		mA
	PGIA gain = 6.4	-17.5	-15		mA
	All PGIA gains, PD = 1		10		μA
I _{AVDD}	PGIA gain = 6.4, reference buffer enabled		18	21.0	mA
	All other PGIA gains, reference buffer enabled		16	19.0	mA
	PGIA gain = 6.4, reference buffer disabled		14	17.5	mA
	All other PGIA gains, reference buffer disabled		12	16.0	mA
I _{DVDD}	All PGIA gains, PD = 1		100		μA
	All PGIA gains, PD = 0		2.5	3.5	mA
I _{VIO}	All PGIA gains, PD = 1		10		μA
	VIO = 3.3 V, PD = 0		0.30	1.2	mA
Power Supply Sensitivity At T _A = 25°C	PD = 1		10		μA
	External reference				
	PGIA gain = 0.16, 0.2, 0.4, 0.8; VDDH/VSSH ± 5%		±0.5		LSB
	PGIA gain = 3.2, VDDH/VSSH ± 5%		±1.0		LSB
	PGIA gain = 6.4, VDDH/VSSH ± 5%		±2.0		LSB
	PGIA gain = 0.16, AVDD/DVDD ± 5%		±0.6		LSB
	PGIA gain = 0.2, AVDD/DVDD ± 5%		±0.8		LSB
	PGIA gain = 0.4, AVDD/DVDD ± 5%		±1.0		LSB
	PGIA gain = 0.8, AVDD/DVDD ± 5%		±1.5		LSB
	PGIA gain = 1.6, AVDD/DVDD ± 5%		±2.0		LSB
PGIA gain = 3.2, AVDD/DVDD ± 5%		±3.5		LSB	
PGIA gain = 6.4, AVDD/DVDD ± 5%		±7.0		LSB	
TEMPERATURE RANGE					
Specified Performance	T _{MIN} to T _{MAX}	-40		+85	°C

¹ LSB means least significant bit and changes depending on the voltage range. See the Programmable Gain section for the LSB size.

² The common-mode voltage (V_{CM}) range for a PGIA gain of 0.16 or 0.2 is 0 V.

³ All ac accuracy specifications expressed in decibels are referred to a full-scale input FSR and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

⁴ This is the output from the internal band gap reference.

⁵ There is no pipeline delay. Conversion results are available immediately after a conversion is complete.

⁶ The differential input common-mode voltage (V_{CM}) range changes according to the maximum input range selected and the high voltage power supplies (VDDH and VSSH). Note that the specified operating input voltage of any input pin requires 2.5 V of headroom from the VDDH and VSSH supplies; therefore, (VSSH + 2.5 V) ≤ INx/COM ≤ (VDDH - 2.5 V).

TIMING SPECIFICATIONS

VDDH = 15 V ± 5%, VSSH = -15 V ± 5%, AVDD = DVDD = 5 V ± 5%, VIO = 1.8 V to AVDD, internal reference, VREF = 4.096 V, f_s = 1 MSPS. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
Time Between Conversions	t _{CYC}				
Warp Mode, ¹ CMS = 0		1		1000	μs
Normal Mode (Default), CMS = 1		1.1			μs
Conversion Time: CNV Rising Edge to Data Available	t _{CONV}				
Warp Mode, CMS = 0			825		ns
Normal Mode (Default), CMS = 1			925	1000	ns
Auxiliary ADC Input Channel Acquisition Time	t _{ACQ}	600			ns
CNV Pulse Width	t _{CH}	10			ns
CNV High to Hold Time (Aperture Delay)	t _{AD}		2		ns
CNV High to Busy Delay	t _{CBD}			520	ns
Safe Data Access Time During Conversion	t _{DDC}			500	ns
Quiet Conversion Time (BUSY High)	t _{QUIET}				
Warp Mode, CMS = 0				400	ns
Normal Mode (Default), CMS = 1				500	ns
Data Access During Quiet Conversion Time	t _{DDCA}				
Warp Mode, CMS = 0				200	ns
Normal Mode (Default), CMS = 1				300	ns
SCK Period	t _{SCK}	15			ns
SCK Low Time	t _{SCKL}	5			ns
SCK High Time	t _{SCKH}	5			ns
SCK Falling Edge to Data Valid	t _{SDOH}	4			ns
SCK Falling Edge to Data Valid Delay	t _{SDOD}				
VIO > 4.5 V				12	ns
VIO > 3.0 V				18	ns
VIO > 2.7 V				24	ns
VIO > 2.3 V				25	ns
VIO > 1.8 V				37	ns
$\overline{\text{CS}}$ /RESET/PD Low to SDO	t _{EN}				
VIO > 4.5 V				15	ns
VIO > 3.0 V				16	ns
VIO > 2.7 V				18	ns
VIO > 2.3 V				23	ns
VIO > 1.8 V				28	ns
$\overline{\text{CS}}$ /RESET/PD High to SDO High Impedance	t _{DIS}			25	ns
DIN Valid Setup Time from SCK Rising Edge	t _{DINS}	4			ns
DIN Valid Hold Time from SCK Rising Edge	t _{DINH}	4			ns
CNV Rising to $\overline{\text{CS}}$	t _{CCS}	5			ns
RESET/PD High Pulse	t _{RH}	5			ns

¹ Exceeding the maximum time has an effect on the accuracy of the conversion (see the Conversion Modes section).

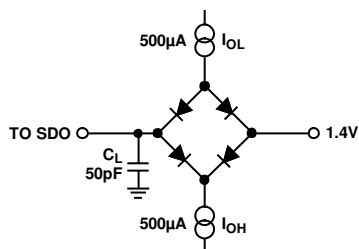
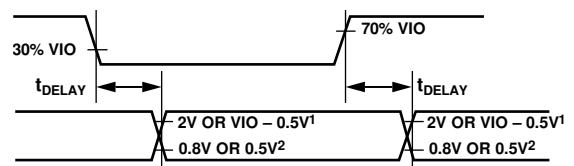
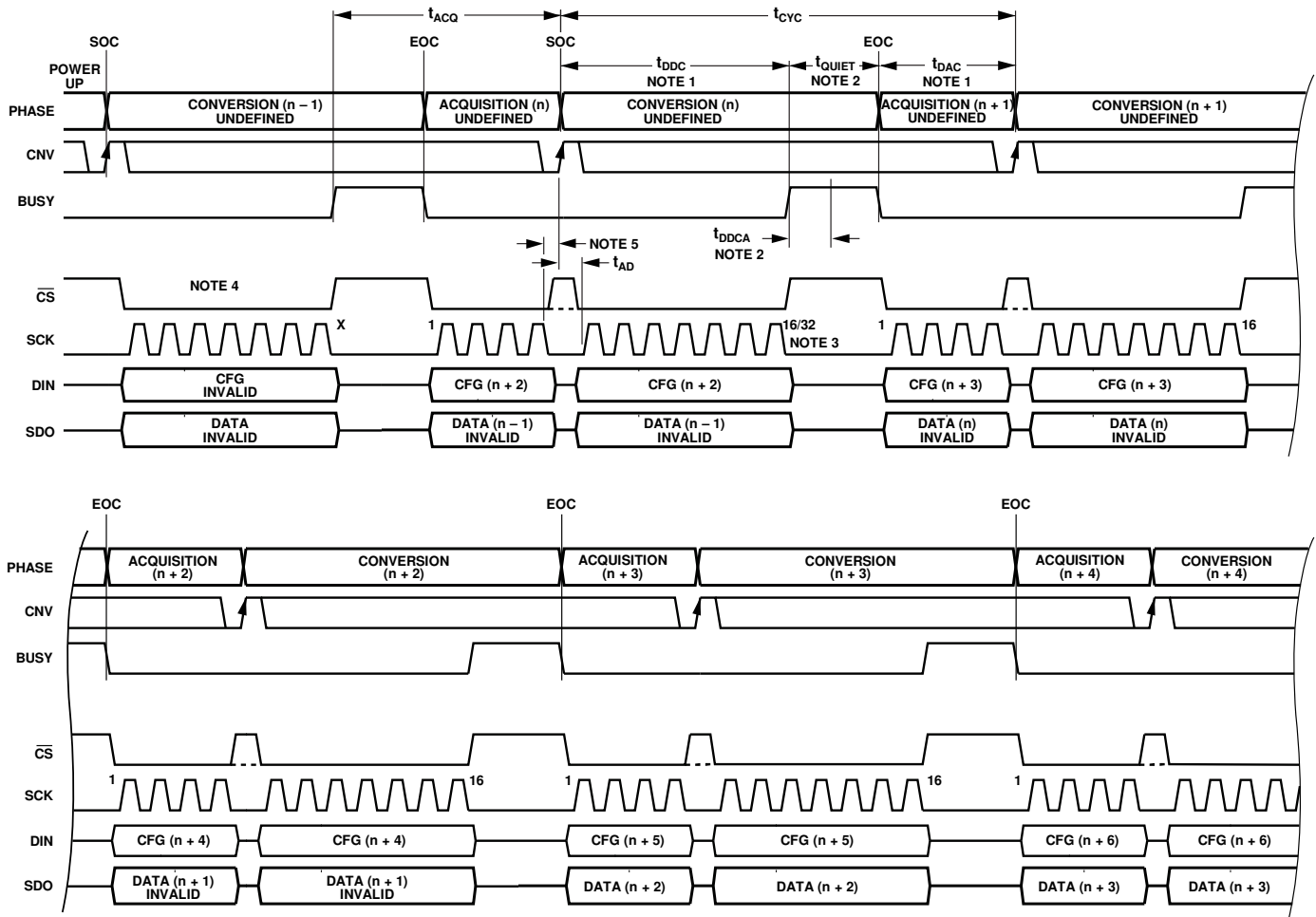


Figure 2. Load Circuit for Digital Interface Timing



¹ 12V IF VIO > 2.5V; VIO - 0.5V IF VIO < 2.5V.
² 0.8V IF VIO > 2.5V; 0.5V IF VIO < 2.5V.

Figure 3. Voltage Levels for Timing



NOTES

1. DATA ACCESS CAN OCCUR DURING A CONVERSION (t_{Ddc}), AFTER A CONVERSION (t_{Dac}), OR BOTH DURING AND AFTER A CONVERSION. THE CONVERSION RESULT AND THE CFG REGISTER ARE UPDATED AT THE END OF A CONVERSION (EOC).
2. DATA ACCESS CAN ALSO OCCUR UP TO t_{Ddca} WHILE BUSY IS ACTIVE (SEE THE DIGITAL INTERFACE SECTION FOR DETAILS). ALL OF THE BUSY TIME CAN BE USED TO ACQUIRE DATA.
3. A TOTAL OF 16 SCK FALLING EDGES IS REQUIRED FOR A CONVERSION RESULT. AN ADDITIONAL 16 EDGES ARE REQUIRED TO READ BACK THE CFG RESULT ASSOCIATED WITH THE CURRENT CONVERSION.
4. CS CAN BE HELD LOW OR CONNECTED TO CNV. CS WITH FULL INDEPENDENT CONTROL IS SHOWN IN THIS FIGURE.
5. FOR OPTIMAL PERFORMANCE, DATA ACCESS SHOULD NOT OCCUR DURING THE SAMPLING EDGE. A MINIMUM TIME OF THE APERTURE DELAY (t_{Ad}) SHOULD ELAPSE PRIOR TO DATA ACCESS.

Figure 4. General Timing Diagram

10616-028

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Analog Inputs/Outputs	
INx, COM to AGND	VSSH – 0.3 V to VDDH + 0.3 V
AUX+, AUX– to AGND	–0.3 V to AVDD + 0.3 V
REFx to AGND	AGND – 0.3 V to AVDD + 0.3 V
REFIN to AGND	AGND – 0.3 V to +2.7 V
REFN to AGND	±0.3 V
Ground Voltage Differences	
AGND, RGND, DGND	±0.3 V
Supply Voltages	
VDDH to AGND	–0.3 V to +16.5 V
VSSH to AGND	+0.3 V to –16.5 V
AVDD, DVDD, VIO to AGND	–0.3 V to +7 V
ACAP, DCAP, RCAP to GND	–0.3 V to +2.7 V
Digital Inputs/Outputs	
CNV, DIN, SCK, RESET, PD, $\overline{\text{CS}}$ to DGND	–0.3 V to VIO + 0.3 V
SDO, BUSY to DGND	–0.3 V to VIO + 0.3 V
Internal Power Dissipation	2 W
Junction Temperature	125°C
Storage Temperature Range	–65°C to +125°C
θ_{JA} Thermal Impedance	44.1°C/W
θ_{JC} Thermal Impedance	0.28°C/W

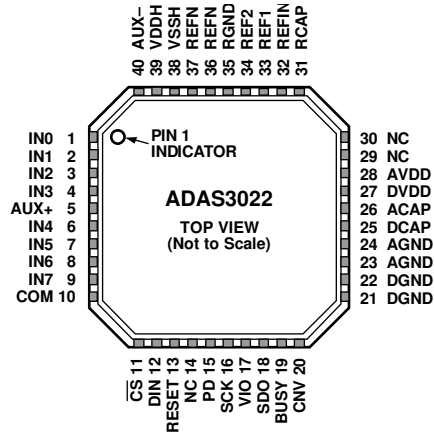
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES
1. NC = NO CONNECT. THIS PIN IS NOT INTERNALLY CONNECTED.
 2. THE EXPOSED PADDLE SHOULD BE CONNECTED TO VSSH.

Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type ¹	Description
1 to 4	IN0 to IN3	AI	Input Channel 0 to Input Channel 3.
5	AUX+	AI	Auxiliary Input Channel Positive Input.
6 to 9	IN4 to IN7	AI	Input Channel 4 to Input Channel 7.
10	COM	AI	IN[7:0] Common Channel Input. The IN[7:0] input channels can be referenced to a common point. The maximum voltage on this pin is ± 10.24 V for all PGIA gains except for a PGIA gain of 0.16, in which case the maximum voltage on this pin is ± 12.228 V. AUX+ and AUX- are not referenced to COM.
11	\overline{CS}	DI	Chip Select. Active low signal. Enables the digital interface for writing and reading data. Use this pin when sharing the serial bus. For a dedicated ADAS3022 serial interface, \overline{CS} can be tied to DGND or CNV to simplify the interface.
12	DIN	DI	Data Input. Serial data input used for writing the 16-bit configuration word (CFG) that is latched on SCK rising edges. CFG is an internal register that is updated on the rising edge of the end of a conversion, which is the falling edge of BUSY. The configuration register can be written to during and after a conversion.
13	RESET	DI	Asynchronous Reset. A low-to-high transition resets the ADAS3022. The current conversion, if active, is aborted and CFG is reset to the default state.
14, 29, 30	NC	NC	No Connect. This pin is not connected internally.
15	PD	DI	Power-Down. A low-to-high transition powers down the ADAS3022, minimizing the bias current. Note that this pin must be held high until the user is ready to power on the device; after powering on the device, the user must wait 100 ms until the reference is enabled and then wait for the completion of two dummy conversions before the device is ready to convert. See the Power-Down Mode section for more information.
16	SCK	DI	Serial Clock Input. The DIN and SDO data sent to and from the ADAS3022 are synchronized with SCK.
17	VIO	P	Digital Interface Supply. Nominally, this supply should be at the same voltage as the supply of the host interface: 1.8 V, 2.5 V, 3.3 V, or 5 V.
18	SDO	DO	Serial Data Output. The conversion result is output on this pin and is synchronized to SCK falling edges. The conversion result is output in twos complement format.
19	BUSY	DO	Busy Output. An active high signal on this pin indicates that a conversion is in process. Reading or writing data during the quiet conversion phase (t_{QUIET}) may cause incorrect bit decisions.
20	CNV	DI	Convert Input. A conversion is initiated on the rising edge of this pin.
21, 22	DGND	P	Digital Ground. Connect these pins to the system digital ground plane.
23, 24	AGND	P	Analog Ground. Connect these pins to the system analog ground plane.
25	DCAP	P	Internal 2.5 V Digital Regulator Output. Decouple this internally regulated output using a 10 μ F capacitor and a 0.1 μ F local capacitor.
26	ACAP	P	Internal 2.5 V Analog Regulator Output. This regulator supplies power to the internal ADC core and all of the supporting analog circuits with the exception of the internal reference. Decouple this internally regulated output using a 10 μ F capacitor and a 0.1 μ F local capacitor.

Pin No.	Mnemonic	Type ¹	Description
27	DVDD	P	Digital 5 V Supply. Decouple this supply using a 10 μ F capacitor and a 0.1 μ F local capacitor.
28	AVDD	P	Analog 5 V Supply. Decouple this supply using a 10 μ F capacitor and a 0.1 μ F local capacitor.
31	RCAP	P	Internal 2.5 V Analog Regulator Output. This regulator supplies power to the internal reference. Decouple this pin using a 1 μ F capacitor connected to RCAP and a 0.1 μ F local capacitor.
32	REFIN	AI/O	Internal 2.5 V Band Gap Reference Output, Reference Buffer Input, or Reference Power-Down Input. See the Voltage Reference Input/Output section for more information.
33, 34	REF1, REF2	AI/O	Reference Input/Output. Regardless of the reference method, these pins need individual decoupling using external 10 μ F ceramic capacitors connected as close to REF1, REF2, and REFN as possible. See the Voltage Reference Output/Input section for more information. REF1 and REF2 must be tied together externally.
35	RGND	P	Reference Supply Ground. Connect this pin to the system analog ground plane.
36, 37	REFN	P	Reference Input/Output Ground. Connect the 10 μ F capacitors on REF1 and REF2 to these pins, and connect these pins to the system analog ground plane.
38	VSSH	P	High Voltage Analog Negative Supply. Nominally, the supply of this pin should be -15 V. Decouple this pin using a 10 μ F capacitor and a 0.1 μ F local capacitor.
39	VDDH	P	High Voltage Analog Positive Supply. Nominally, the supply of this pin should be $+15$ V. Decouple this pin using a 10 μ F capacitor and a 0.1 μ F local capacitor.
40	AUX– EPAD	AI	Auxiliary Input Channel Negative Input. Exposed Paddle. The exposed paddle should be connected to VSSH.

¹AI = analog input, AI/O = analog input/output, DI = digital input, DO = digital output, and P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

VDDH = 15 V, VSSH = -15 V, AVDD = DVDD = 5 V, VIO = 1.8 V to AVDD, unless otherwise noted.

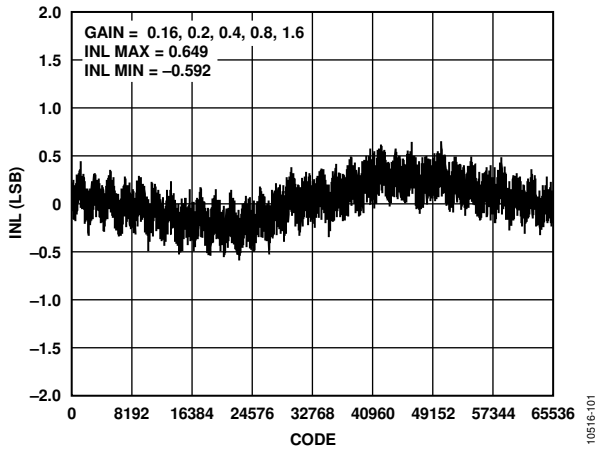


Figure 6. Integral Nonlinearity vs. Code, PGIA Gain = 0.16, 0.2, 0.4, 0.8, and 1.6

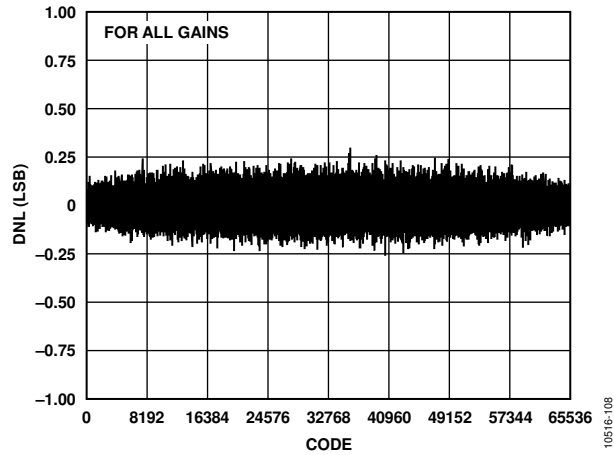


Figure 9. Differential Nonlinearity vs. Code for All PGIA Gains

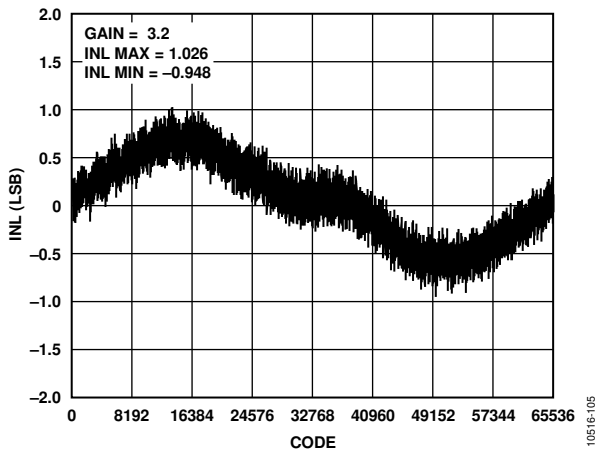


Figure 7. Integral Nonlinearity vs. Code, PGIA Gain = 3.2

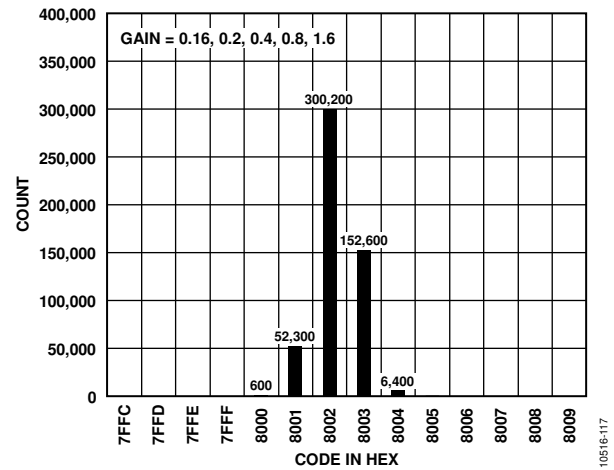


Figure 10. Histogram of a DC Input at Code Center, PGIA Gain = 0.16, 0.2, 0.4, 0.8, and 1.6

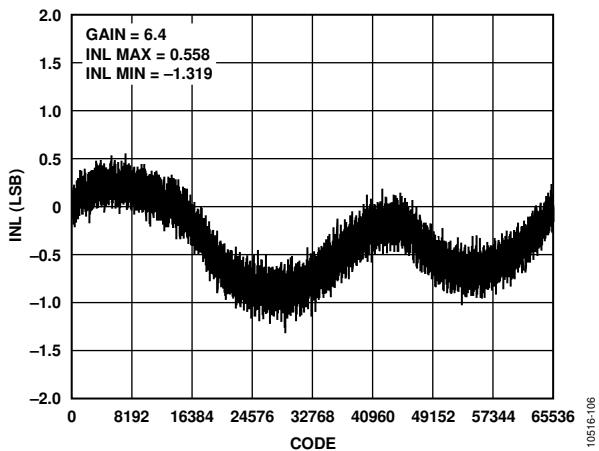


Figure 8. Integral Nonlinearity vs. Code, PGIA Gain = 6.4

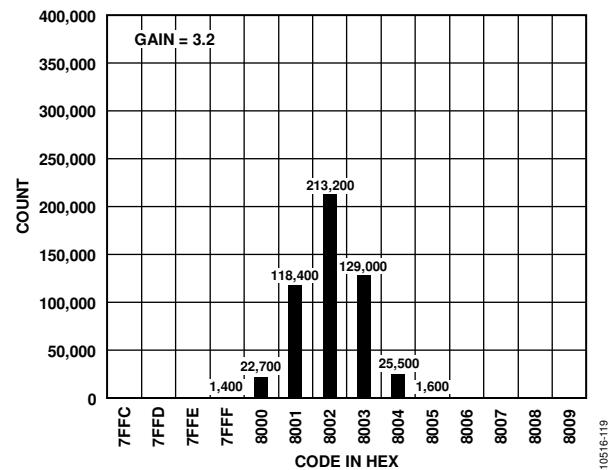


Figure 11. Histogram of a DC Input at Code Center, PGIA Gain = 3.2

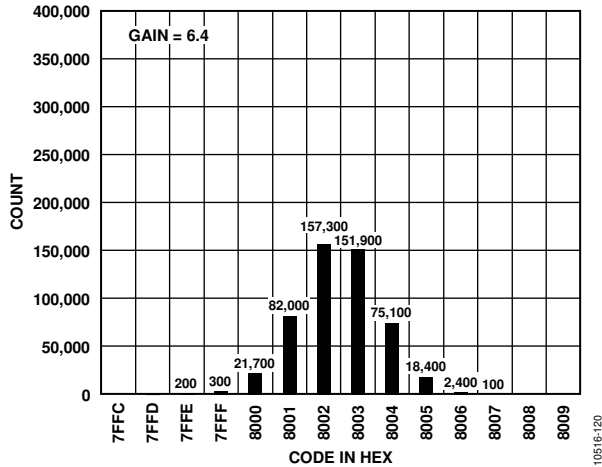


Figure 12. Histogram of a DC Input at Code Center, PGA Gain = 6.4

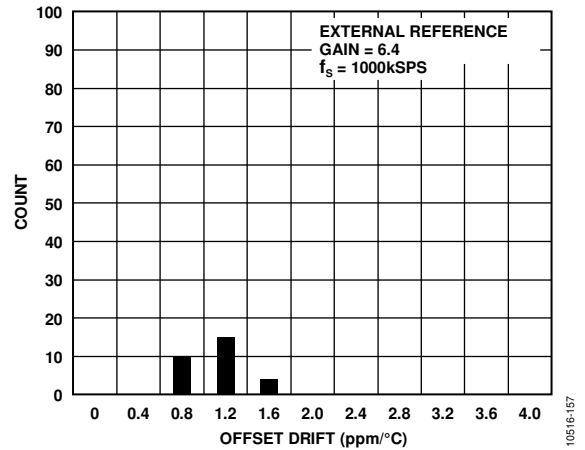


Figure 15. Offset Drift, PGA Gain = 6.4

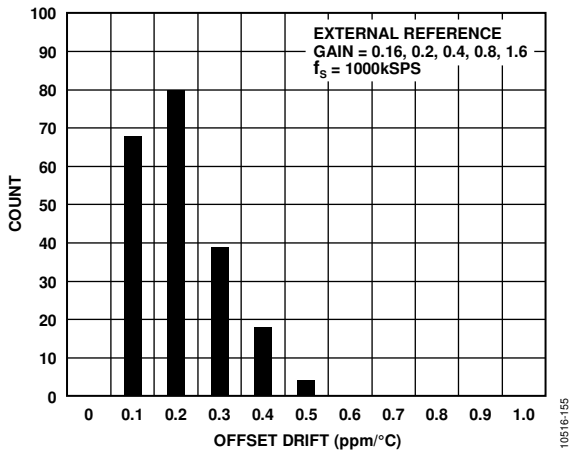


Figure 13. Offset Drift, PGA Gain = 0.16, 0.2, 0.4, 0.8, and 1.6

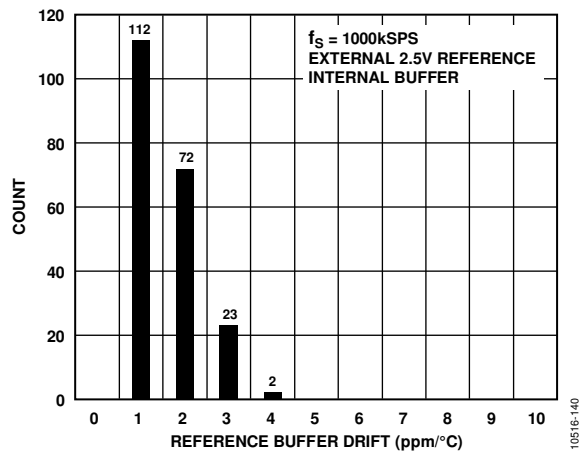


Figure 16. Reference Buffer Drift, External Reference

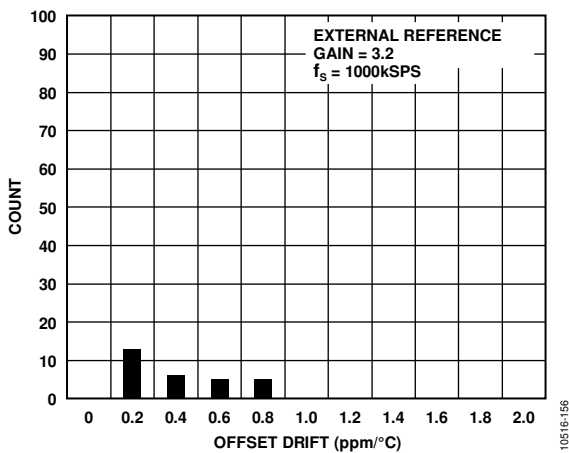


Figure 14. Offset Drift, PGA Gain = 3.2

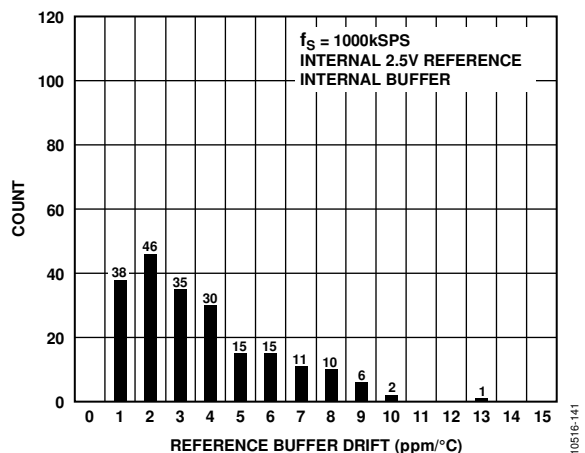


Figure 17. Reference Buffer Drift, Internal Reference

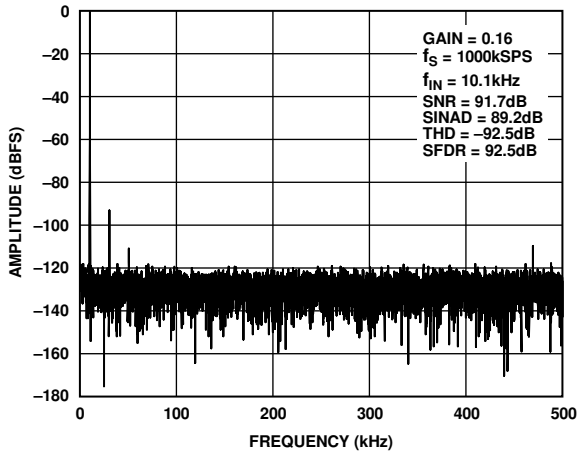


Figure 18. 10 kHz FFT, PGIA Gain = 0.16

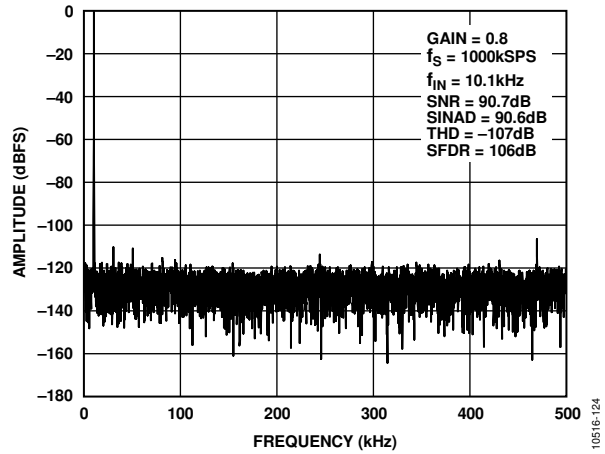


Figure 21. 10 kHz FFT, PGIA Gain = 0.8

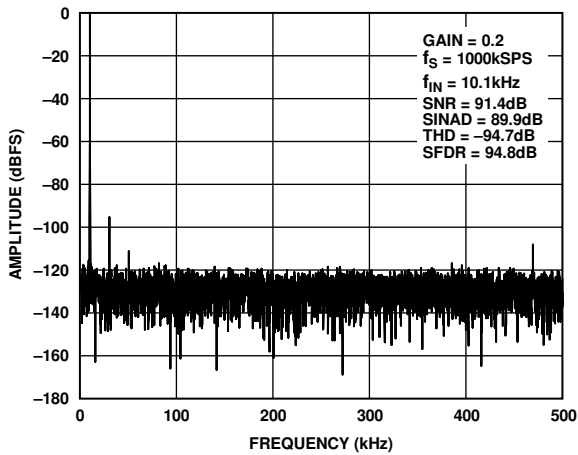


Figure 19. 10 kHz FFT, PGIA Gain = 0.2

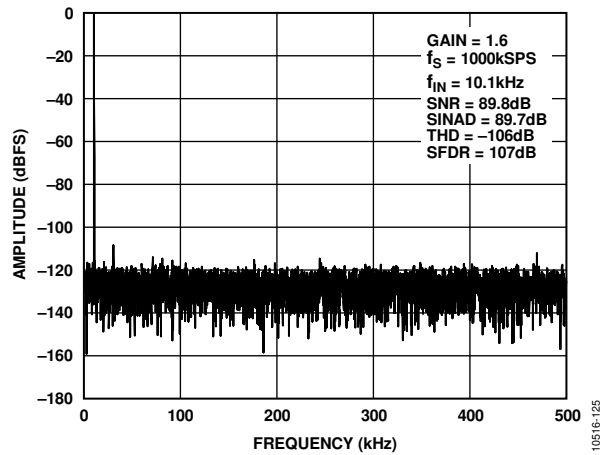


Figure 22. 10 kHz FFT, PGIA Gain = 1.6

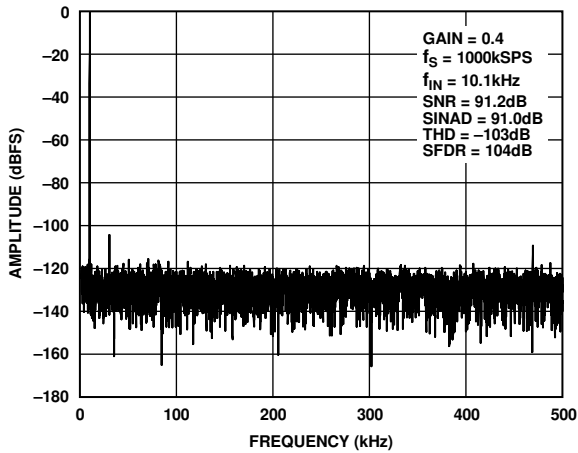


Figure 20. 10 kHz FFT, PGIA Gain = 0.4

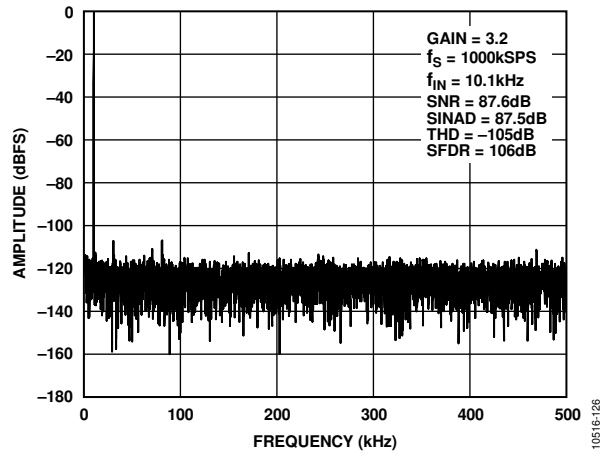


Figure 23. 10 kHz FFT, PGIA Gain = 3.2

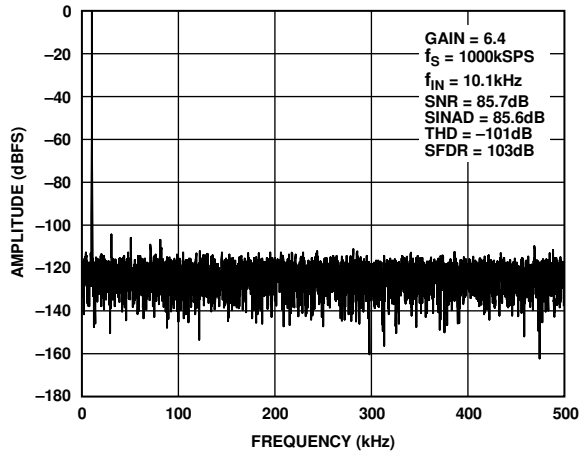


Figure 24. 10 kHz FFT, PGIA Gain = 6.4

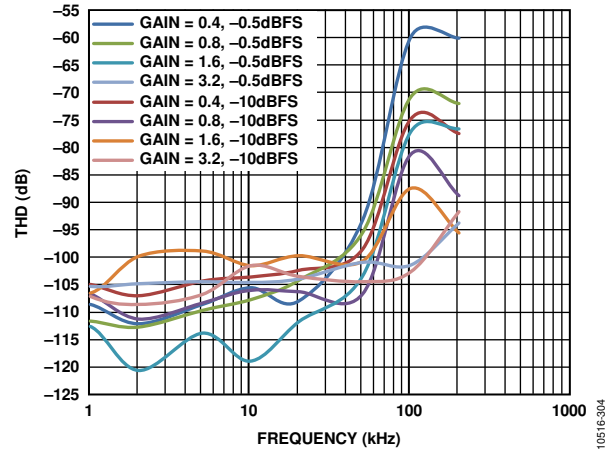


Figure 27. THD vs. Frequency

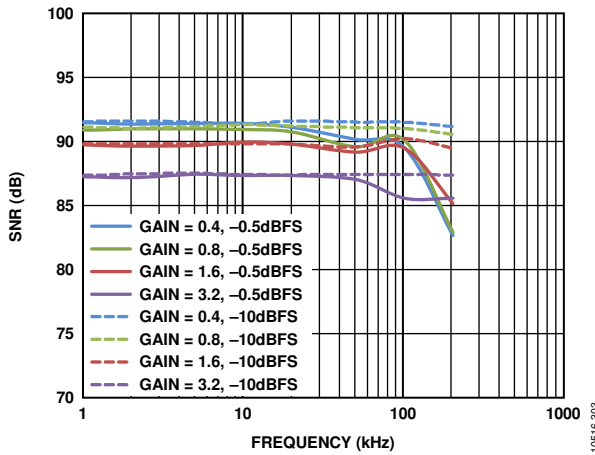


Figure 25. SNR vs. Frequency

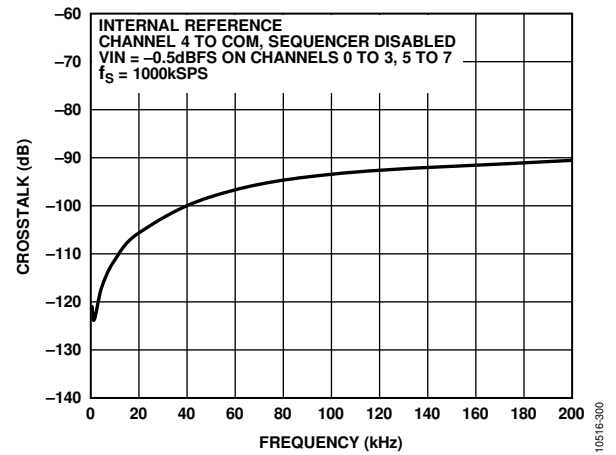


Figure 28. Crosstalk vs. Frequency

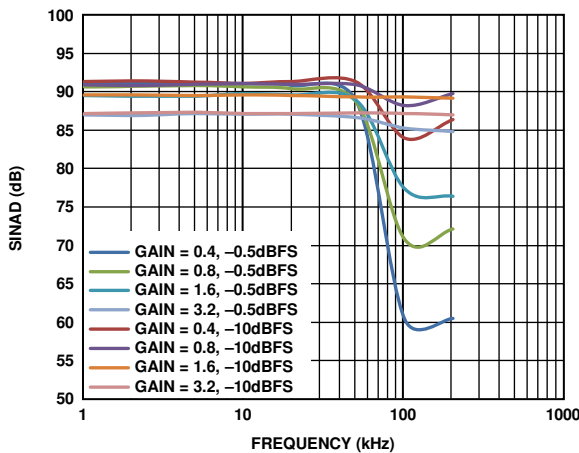


Figure 26. SINAD vs. Frequency

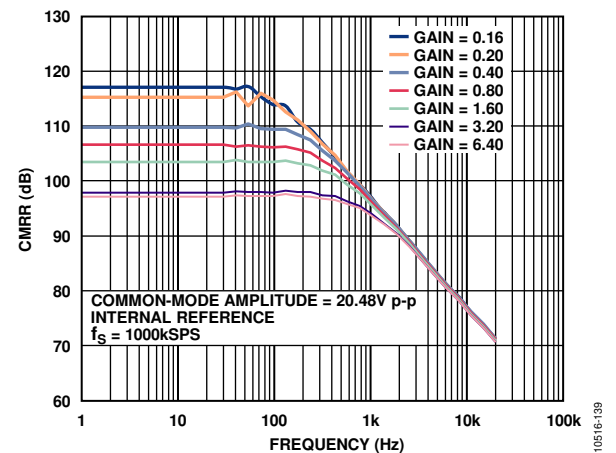


Figure 29. CMRR vs. Frequency

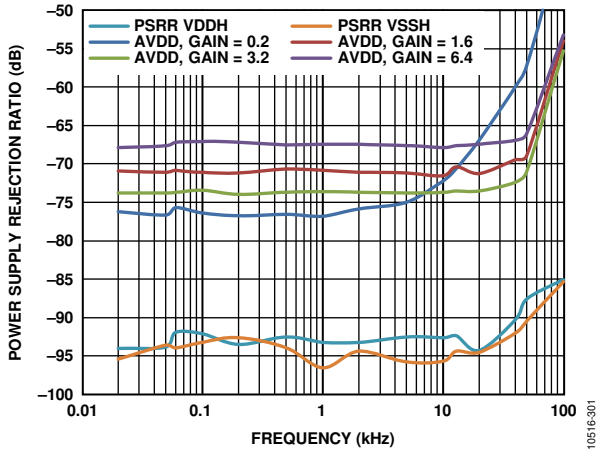


Figure 30. PSRR vs. Frequency

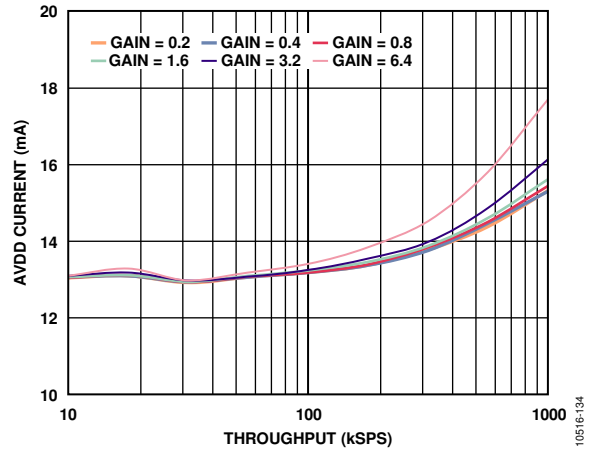


Figure 33. AVDD Current vs. Throughput, Internal Reference

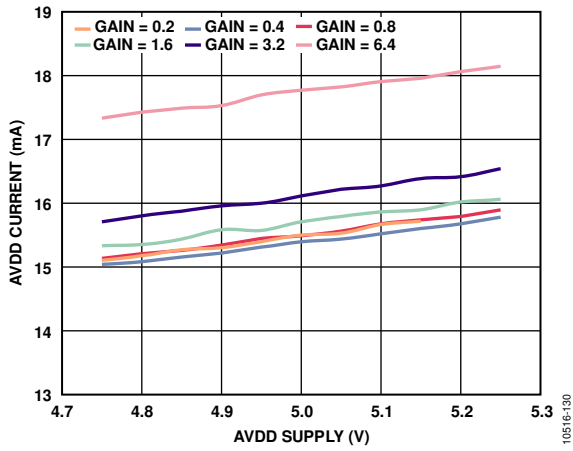


Figure 31. AVDD Current vs. Supply, Internal Reference

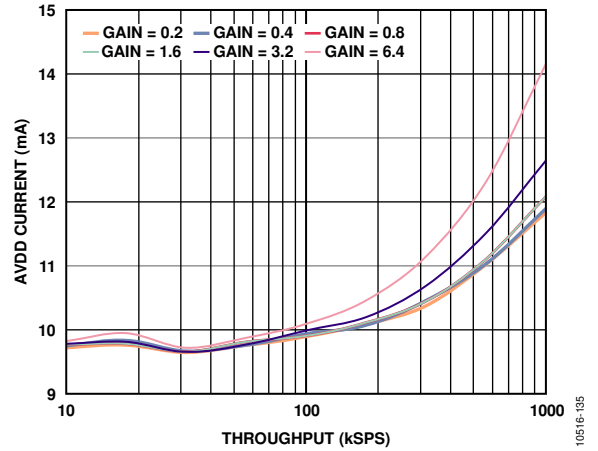


Figure 34. AVDD Current vs. Throughput, External Reference

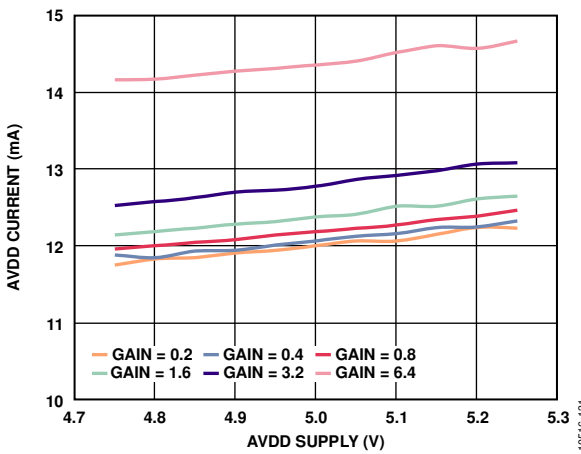


Figure 32. AVDD Current vs. Supply, External Reference

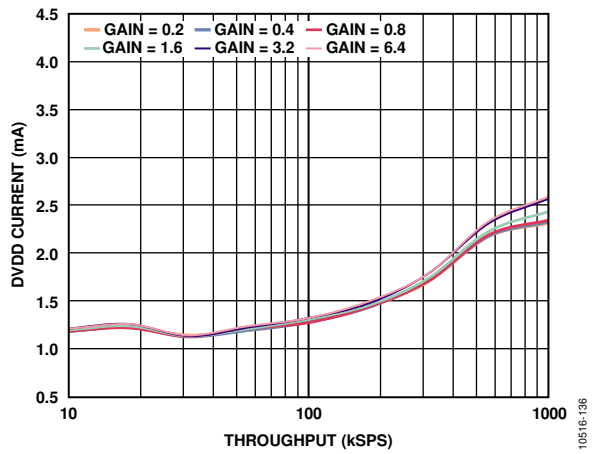


Figure 35. DVDD Current vs. Throughput

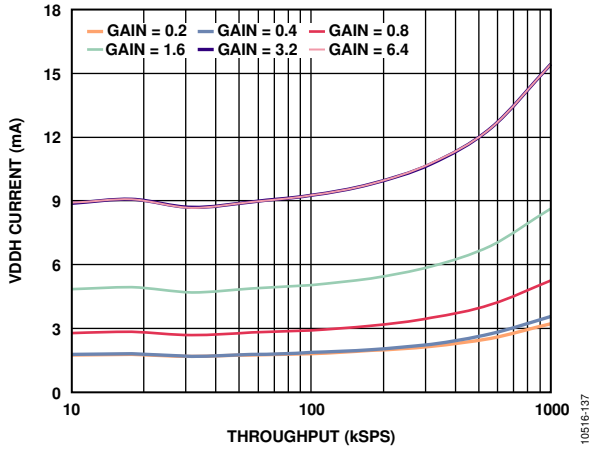


Figure 36. VDDH Current vs. Throughput

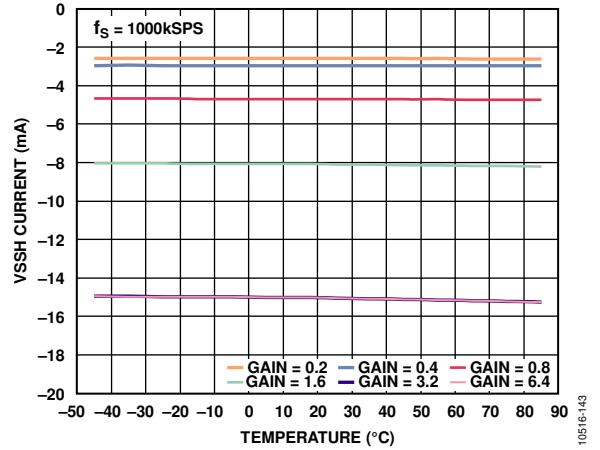


Figure 39. VSSH Current vs. Temperature

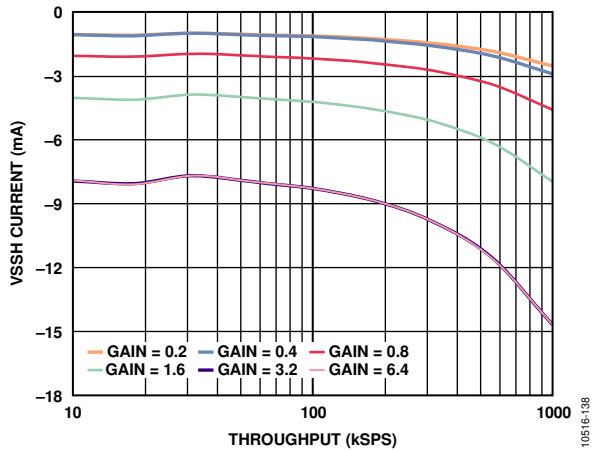


Figure 37. VSSH Current vs. Throughput

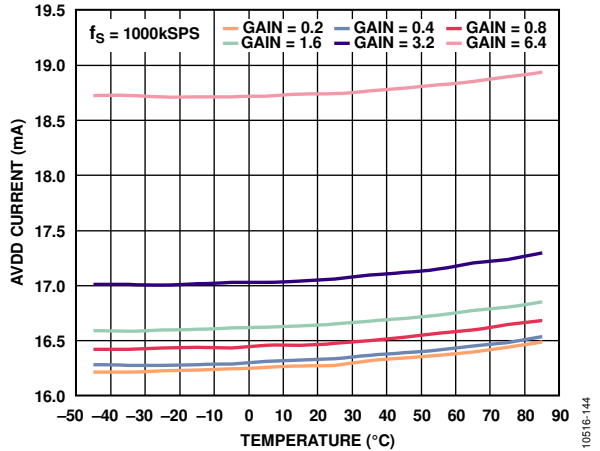


Figure 40. AVDD Current vs. Temperature

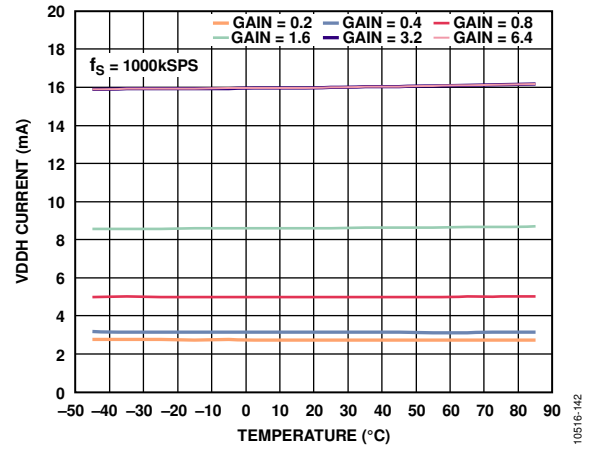


Figure 38. VDDH Current vs. Temperature

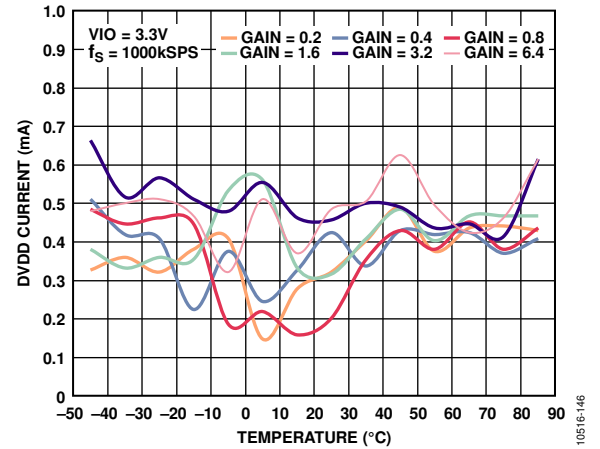


Figure 41. DVDD Current vs. Temperature

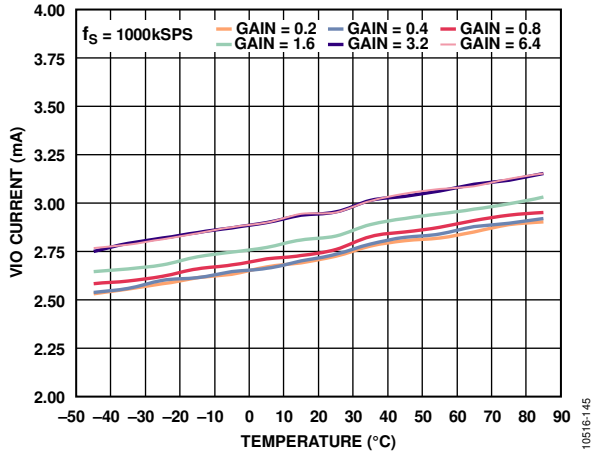


Figure 42. VIO Current vs. Temperature

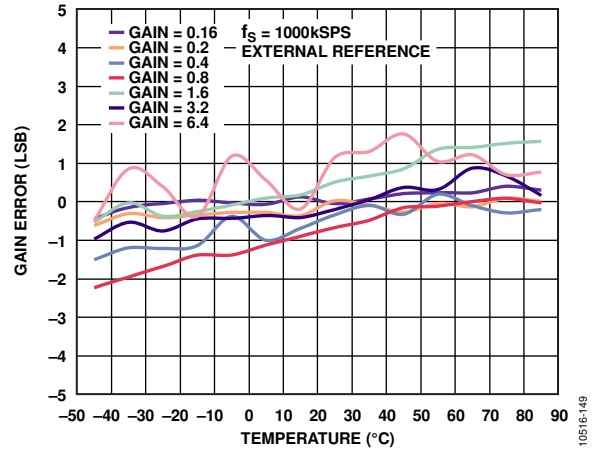


Figure 45. Gain Error vs. Temperature

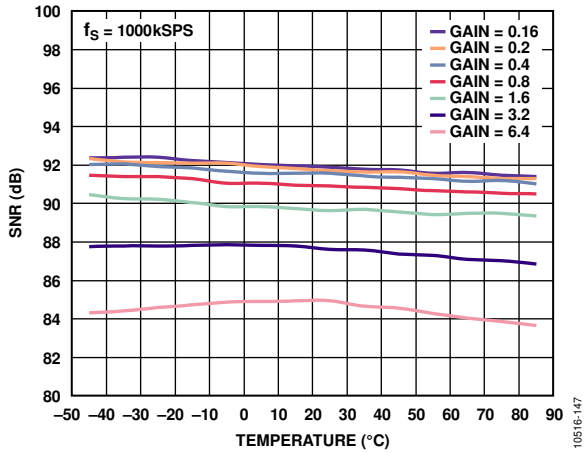


Figure 43. SNR vs. Temperature

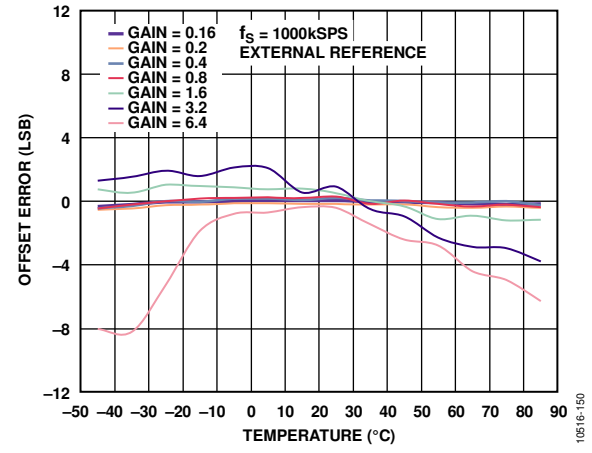


Figure 46. Offset Error vs. Temperature

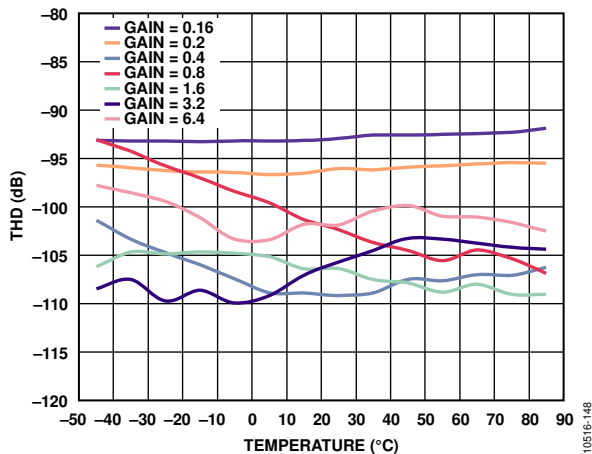


Figure 44. THD vs. Temperature

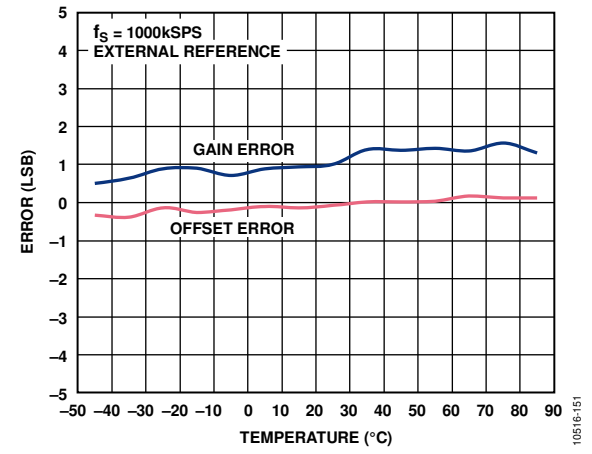


Figure 47. Offset and Gain Errors of the AUX ADC Channel Pair vs. Temperature

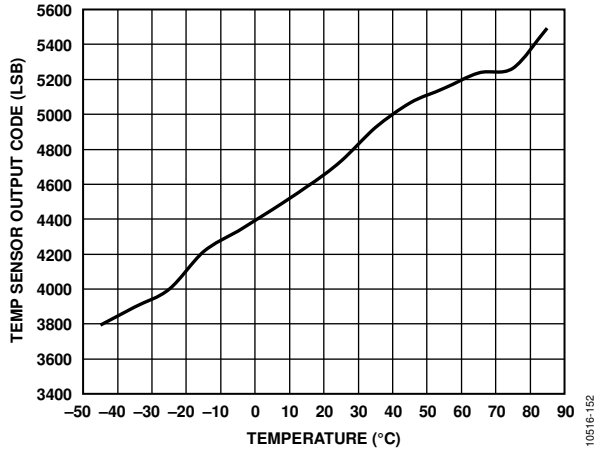


Figure 48. Temperature Sensor Output Code vs. Temperature

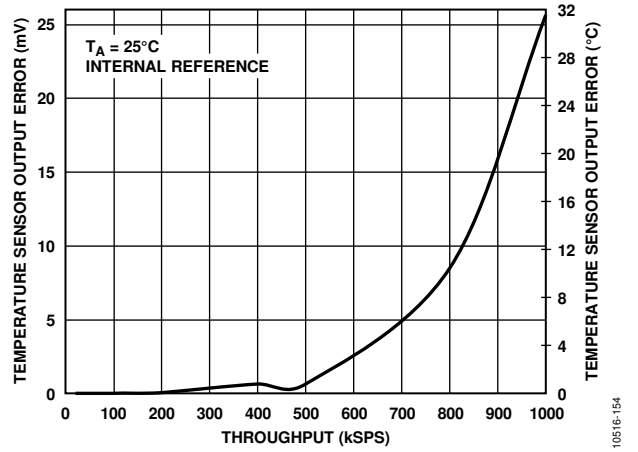


Figure 50. Temperature Sensor Output Error vs. Throughput

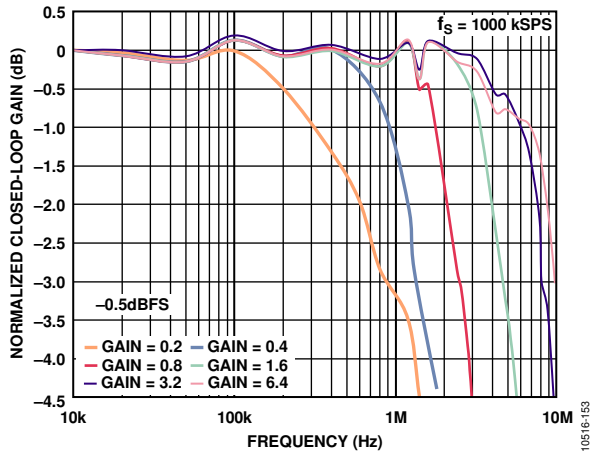


Figure 49. Large Signal Frequency Response vs. Gain

TERMINOLOGY

Operating Input Voltage Range

Operating input voltage range is the maximum input voltage range, including the common-mode voltage, allowed on the input channels IN[7:0] and COM.

Differential Input Voltage Range

Differential input voltage range is the maximum differential full-scale input range. The value changes according to the programmable gain setting.

Channel Off Leakage

Channel off leakage is the leakage current with the channel off.

Channel On Leakage

Channel on leakage is the leakage current with the channel on.

Charge Injection

Charge injection is a measure of the glitch impulse that is transferred through the analog input pin into the source when the sample is taken and/or the multiplexer is switched.

Common-Mode Rejection Ratio (CMRR)

CMRR is the ratio of the amplitude of a signal referred to input in the converted result to the amplitude of the modulation common to a pair of inputs and is expressed in decibels. CMRR is a measure of the ability of the [ADAS3022](#) to reject signals, such as power line noise, that are common to the inputs. This specification is for a 2 kHz sine wave of 20.48 V p-p applied to both channels of an input pair.

Transient Response

Transient response is a measure of the time required for the [ADAS3022](#) to properly acquire the input after a full-scale step function is applied to the system.

Least Significant Bit (LSB)

LSB is the smallest increment that can be represented by a converter. For a fully differential input ADC with N bits of resolution, the LSB expressed in volts is

$$LSB (V) = \frac{2V_{REF}}{2^N}$$

Integral Nonlinearity (INL) Error

INL refers to the deviation of each individual code from a line drawn from negative full scale to positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 53).

Differential Nonlinearity (DNL) Error

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error

Offset error is the deviation of the actual MSB transition from the ideal MSB transition point. The ideal MSB transition occurs at an input level ½ LSB above analog ground.

Gain Error

The last transition (from 111 ... 10 to 111 ... 11) for an analog voltage should occur 1½ LSB below the nominal full scale. The gain error is the deviation expressed in LSB (or as a percentage of the full-scale range) of the actual level of the last transition from the ideal level after the offset error is removed. Closely related to this parameter is the full-scale error (also expressed in LSB or as a percentage of the full-scale range), which includes the effects of the offset error.

Total Unadjusted Error (TUE)

TUE is the deviation of each code from an ideal transfer function and is a combination of all error contributors, including non-linearity, offset error, and gain error. TUE for the [ADAS3022](#) is expressed as the maximum deviation in LSB or as a percentage of the full-scale range.

Aperture Delay

Aperture delay is a measure of the acquisition performance. It is the time between the rising edge of the CNV input and the point at which the input signal is held for a conversion.

Dynamic Range

Dynamic range is the ratio of the rms value of the full-scale signal to the total rms noise measured with the inputs shorted together. The value for the dynamic range is expressed in decibels.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion Ratio (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, expressed in decibels, between the rms amplitude of the input signal and the peak spurious signal.

Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is a measure of the level of crosstalk between any channel and all other channels. The crosstalk is measured by applying a dc input to the channel under test and applying a full-scale, 10 kHz sine wave signal to all other channels. The crosstalk is the amount of signal that leaks into the test channel and is expressed in decibels.

Reference Voltage Temperature Coefficient

Reference voltage temperature coefficient is derived from the typical shift of output voltage at 25°C on a sample of parts at the maximum and minimum reference output voltage (V_{REF}) measured at T_{MIN} , T (25°C), and T_{MAX} . The value is expressed in ppm/°C as

$$TCV_{REF} \text{ (ppm/°C)} = \frac{V_{REF} (Max) - V_{REF} (Min)}{V_{REF} (25°C) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:

$V_{REF} (Max)$ is the maximum reference output voltage at T_{MIN} , T (25°C), or T_{MAX} .

$V_{REF} (Min)$ is the minimum reference output voltage at T_{MIN} , T (25°C), or T_{MAX} .

$V_{REF} (25°C)$ is the reference output voltage at 25°C.

$T_{MAX} = +85°C$.

$T_{MIN} = -40°C$.

THEORY OF OPERATION

OVERVIEW

The ADAS3022 is the first system on a single chip that integrates the typical components used in a data acquisition system in one easy to use, programmable device. This single-chip solution is capable of converting up to 1,000,000 samples per second (1 MSPS) of aggregate throughput. The ADAS3022 features

- High impedance inputs
- High common-mode rejection
- 8-channel, low crosstalk multiplexer (mux)
- Programmable gain instrumentation amplifier (PGIA) with seven selectable differential input ranges from ± 0.64 V to ± 24.576 V
- 16-bit PulSAR[®] ADC with no missing codes
- Internal, precision, low drift 4.096 V reference and buffer
- Temperature sensor
- Channel sequencer

The ADAS3022 uses an Analog Devices patented high voltage iCMOS[®] process, allowing up to a ± 24.576 V differential input voltage range when using ± 15 V supplies, which makes the device suitable for industrial applications.

The device is housed in a small, 6 mm \times 6 mm, 40-lead LFCSP and can operate over the industrial temperature range (-40°C to $+85^{\circ}\text{C}$). A typical discrete multichannel data acquisition system containing similar circuitry would require at least three times more space on the circuit board. Therefore, advantages of

the ADAS3022 solution include reduced footprint and less complex design requirements, which also results in faster time to market and lower cost.

ADAS3022 OPERATION

As shown in Figure 51, the ADAS3022 internal analog circuitry consists of a high impedance, low leakage multiplexer and a programmable gain instrumentation amplifier that can accept full-scale differential voltages of ± 0.64 V, ± 1.28 V, ± 2.56 V, ± 5.12 V, ± 10.24 V, ± 20.48 V, and ± 24.576 V. The ADAS3022 can be configured to use up to eight single-ended input channels or four pairs of channels, that is, 125 kSPS per channel for eight channels or effectively 250 kSPS for four channel pairs. The device can also provide a relative temperature measurement using the internal temperature sensor. In addition, the differential auxiliary channel pair (AUX+ and AUX-) is provided with the specified input range of $\pm V_{REF}$. This option bypasses the mux and PGIA stages, allowing direct access to the SAR ADC core.

Reducing the number of channels or pairs increases the throughput rate by an amount proportional to the reciprocal of the number of sampled channels multiplied by the aggregate throughput:

$$1/(\text{Number of Channels or Pairs}) \times 1000 \text{ kSPS}$$

For a single channel or channel pair, the maximum throughput rate is 1 MSPS. For all eight channels, the AUX channel pair, and the temperature sensor, the throughput rate of a given channel decreases to 100 kSPS.

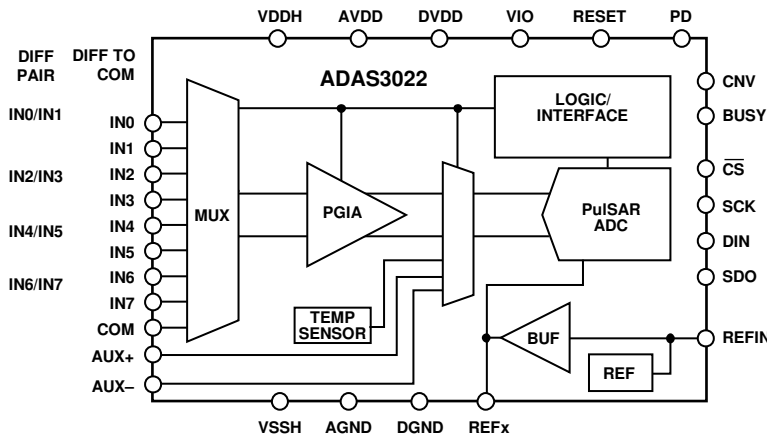


Figure 51. ADAS3022 Simplified Block Diagram

The ADAS3022 offers true high impedance inputs in a differential structure and rejects common-mode signals present on the inputs. The ADAS3022 architecture does not require any of the additional input buffers (op amps) that are usually required to condition the input signal and drive the ADC inputs when using switched capacitor-based successive approximation register (SAR) analog-to-digital converters (ADCs).

The inputs are multiplexed to the PGIA using a high voltage multiplexer with low charge injection and very low leakage. The inputs can be configured for a single-ended to common point (COM) measurement or can be paired for up to four fully differential inputs with independent gain settings. This requires using the advanced sequencer or programming sequential configuration words with the desired gain for each pair. The digitally controlled, programmable gain is used to select one of seven voltage input ranges (see Table 7).

When the sequencer option is used, an on-chip sequencer scans channels in order and offers independent input voltage ranges for each channel (see the On Demand Conversion Mode section). In this mode, a single configuration word initiates the sequencer to scan repeatedly without the need to rewrite the register. After the last channel is scanned, the ADAS3022 automatically begins at IN0 again and repeats the sequence until a word is written to stop the sequencer or the asynchronous RESET is asserted. Additionally, if changes are made to certain configuration bits, the sequencer is reset to IN0.

The PulsAR-based ADC core is capable of converting 1 MSPS from a single rising edge on the convert start input (CNV). The conversion results are available in twos complement format and are presented on the serial data output (SDO). The digital interface uses a dedicated chip select pin (CS) to transfer data to and from the ADAS3022 and also provides a BUSY indicator, asynchronous RESET, and power-down (PD) inputs.

The ADAS3022 on-chip reference uses an internal temperature compensated 2.5 V output band gap reference and a precision buffer amplifier to provide the 4.096 V high precision system reference.

All of the bits in Table 11 are configured through a serial (SPI-compatible), 16-bit configuration register (CFG). Configuration and conversion results can be read after or during a conversion, or the readback option can be disabled.

The ADAS3022 requires a minimum of three power supplies: +5 V, +15 V, and -15 V. On-chip low dropout regulators provide the necessary 2.5 V system voltages and must be decoupled externally via dedicated pins (ACAP, DCAP, and RCAP). The ADAS3022 can be interfaced to any 1.8 V to 5 V digital logic family using the dedicated VIO logic level voltage supply (see Table 9).

A rising edge on CNV initiates a conversion and changes the state of the ADAS3022 from track to hold. In this state, the ADAS3022 performs analog signal conditioning. When the signal conditioning is complete, the ADAS3022 returns to the track state while at the same time quantizing the sample. This two-part process satisfies the necessary settling time requirement while achieving a fast throughput rate of up to 1 MSPS with 16-bit accuracy.

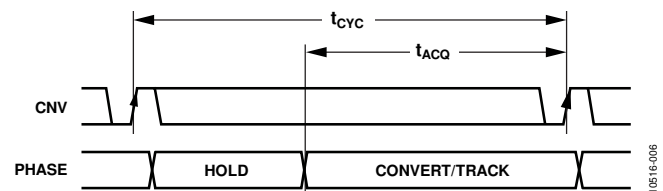


Figure 52. ADAS3022 System Timing

Regardless of the type of signal (differential or single-ended, antiphase or nonantiphase, symmetric or asymmetric), the ADAS3022 converts all signals present on the enabled inputs in a differential fashion, like an industry-standard difference or instrumentation amplifier.

The conversion result is available after the conversion is complete and can be read back at any time before the end of the next conversion. Reading back data should be avoided during the quiet period, as indicated by BUSY being active high. Because the ADAS3022 has an on-board conversion clock, the serial clock (SCK) is not required for the conversion process. It is only required to present results to the user.

TRANSFER FUNCTION

The ideal transfer characteristics of the ADAS3022 are shown in Figure 53. With the inputs configured for differential input ranges, the data output is twos complement, as described in Table 6.

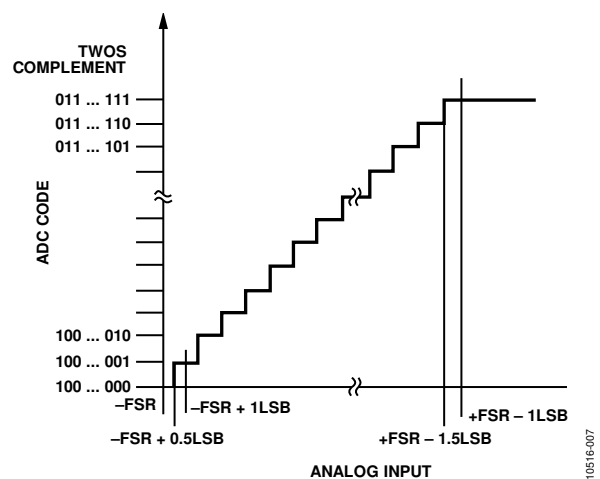


Figure 53. ADC Ideal Transfer Function

Table 6. Output Codes and Ideal Input Voltages

Description	Differential Analog Inputs, $V_{REF} = 4.096\text{ V}$	Digital Output Code (Twos Complement, Hex)
FSR - 1 LSB	$(32,767 \times V_{REF}) / (32,768 \times \text{PGIA gain})$	0x7FFF
Midscale + 1 LSB	$V_{REF} / (32,768 \times \text{PGIA gain})$	0x0001
Midscale	0	0x0000
Midscale - 1 LSB	$-(V_{REF} / (32,768 \times \text{PGIA gain}))$	0xFFFF
-FSR + 1 LSB	$-(32,767 \times V_{REF}) / (32,768 \times \text{PGIA gain})$	0x8001
-FSR	$-V_{REF} \times \text{PGIA gain}$	0x8000

TYPICAL APPLICATION CONNECTION DIAGRAM

As shown in Figure 54, the ADP1613 is used in an inexpensive SEPIC-Ćuk topology, which is an ideal candidate for providing the ADAS3022 with the necessary high voltage $\pm 15\text{ V}$ robust supplies (at 20 mA) and low output ripple (3 mV maximum) from an external 5 V supply. The ADP1613 satisfies the specification requirements of the ADAS3022 with minimal external components while achieving greater than 86% of efficiency. Refer to the CN-0201 circuit note for complete information about this test setup.

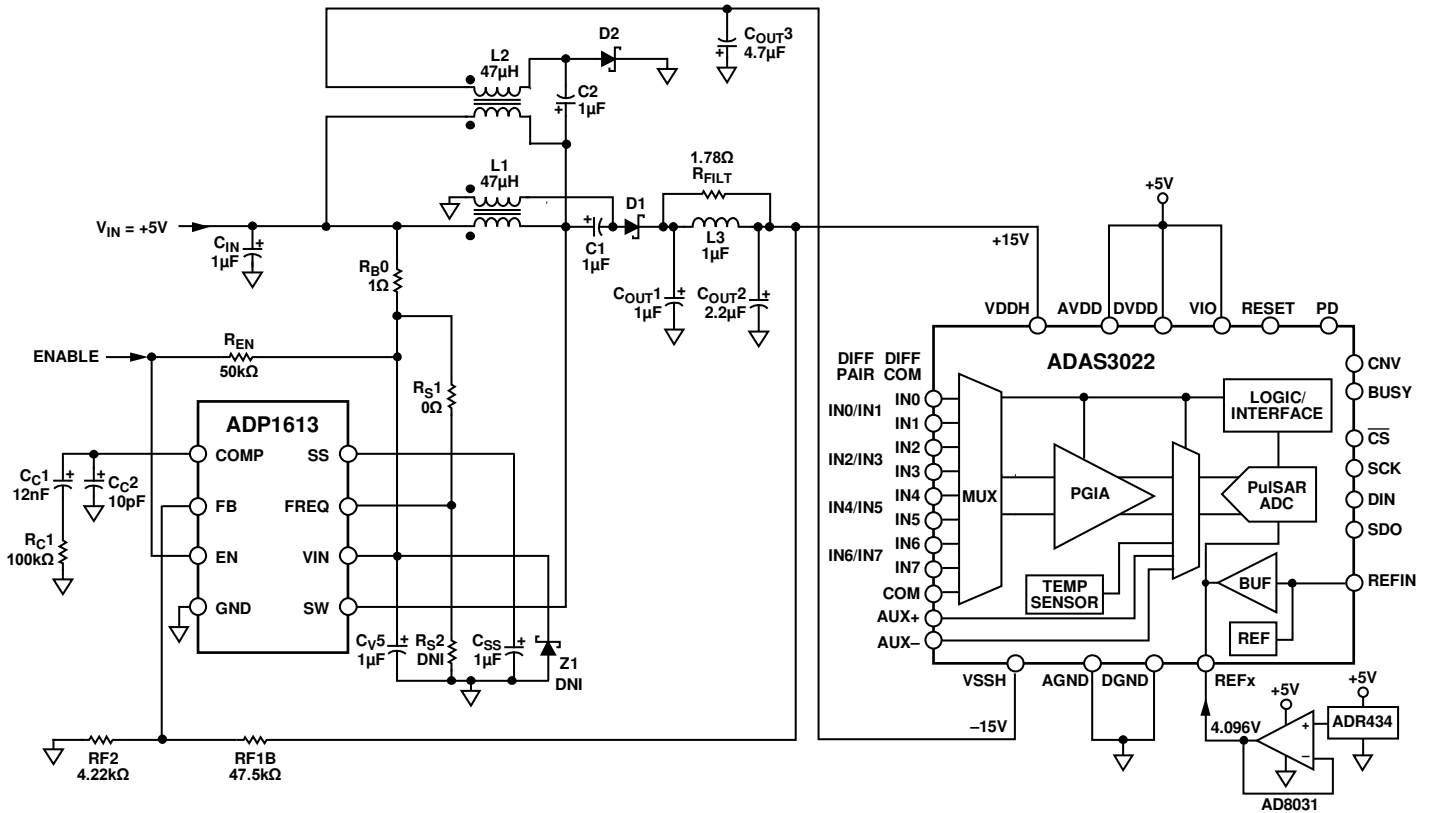


Figure 54. Complete 5 V, Single-Supply, 8-Channel Multiplexed Data Acquisition System with PGIA