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600 MHz Dual Integrated DCL with PPMU, VHH Drive Capability, Level Setting DACs, and On-Chip Calibration Engine

Data Sheet

ADATE318

FEATURES

- 600 MHz/1200 Mbps data rate
- 3-level driver with high-Z and reflection clamps
- Window and differential comparators
- ±25 mA active load
- Per pin PPMU with −2.0 V to +6.5 V range
- Low leakage mode (typically 4 nA)
- Integrated 16-bit DACs with offset and gain correction
- High speed operating voltage range: −1.5 V to +6.5 V
- Dedicated VHH output pin range: 0.0 V to 13.5 V
- 1.1 W power dissipation per channel
- Driver
  - 3-level voltage range: −1.5 V to +6.5 V
  - Precision trimmed output resistance
  - Unterminated swing: 200 mV minimum to 8 V maximum
  - 725 ps minimum pulse width, VIH − VIL = 2.0 V
- Comparator
  - Differential and single-ended window modes
  - >1.2 GHz input equivalent bandwidth
- Load
  - ±25 mA current range
- Per pin PPMU (PPMU)
  - Force voltage/compliance range: −2.0 V to +6.5 V
  - 5 current ranges: 40 mA, 1 mA, 100 µA, 10 µA, 2 µA
  - External sense input for system PMU
  - Go/no-go comparators
- Levels
  - Fully integrated 16-bit DACs
  - On-chip gain and offset calibration registers and add/multiply engine
- Package
  - 84-lead 10 mm × 10 mm LFCSP (0.4 mm pitch)

APPLICATIONS

- Automatic test equipment
- Semiconductor test systems
- Board test systems
- Instrumentation and characterization equipment

GENERAL DESCRIPTION

The ADATE318 is a complete, single-chip ATE solution that performs the pin electronics functions of driver, comparator, and active load (DCL), four quadrant, per pin, parametric measurement unit (PPMU). It has VHH drive capability per chip to support flash memory testing applications and integrated 16-bit DACs with an on-chip calibration engine to provide all necessary dc levels for operation of the part.

The driver features three active states: data high, data low, and terminate mode, as well as a high impedance inhibit state. The inhibit state, in conjunction with the integrated dynamic clamps, facilitates the implementation of a high speed active termination. The output voltage capability is −1.5 V to +6.5 V to accommodate a wide range of ATE and instrumentation applications.

The ADATE318 can be used as a dual, single-ended drive/receive channel or as a single differential drive/receive channel. Each channel of the ADATE318 features a high speed window comparator as well as a programmable threshold differential comparator for differential ATE applications. A four quadrant PPMU is also provided per channel.

All dc levels for DCL and PPMU functions are generated by 24 on-chip 16-bit DACs. To facilitate accurate levels programming, the ADATE318 contains an integrated calibration function to correct gain and offset errors for each functional block. Correction coefficients can be stored on chip, and any values written to the DACs are automatically adjusted using the appropriate correction factors.

The ADATE318 uses a serial programmable interface (SPI) bus to program all functional blocks, DACs, and on-chip calibration constants. It also has an on-chip temperature sensor and over/undervoltage fault clamps for monitoring and reporting the device temperature and any output pin or PPMU voltage faults that may occur during operation.

Rev. B
Document Feedback

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4/2011—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

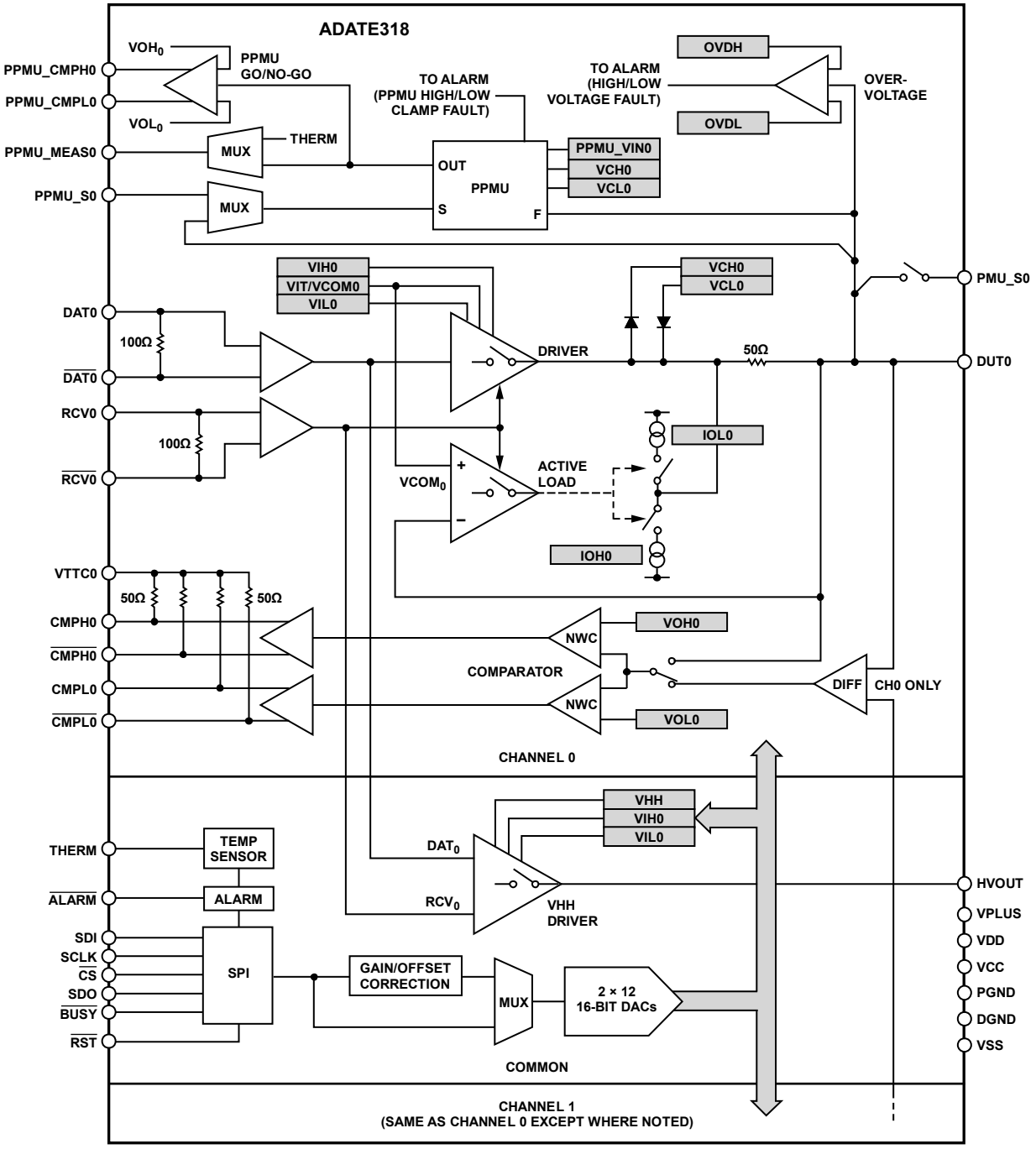


Figure 1.

SPECIFICATIONS

VDD = +10.0 V, VCC = +2.5 V, VSS = −6.0 V, VPLUS = +16.75 V, VTTCx = +1.2 V, VREF = 5.000 V, VREFGND = 0.000 V. All test conditions are as defined in Table 32. All specified values are at T_J = 50°C, where T_J corresponds to the internal temperature sensor reading (THERM pin), unless otherwise noted. Temperature coefficients are measured around T_J = 50° ± 20°C, unless otherwise noted. Typical values are based on statistical mean of design, simulation analyses, and/or limited bench evaluation data. Typical values are neither tested nor guaranteed. See Table 16 for an explanation of test levels.

Table 1. Detailed Electrical Specifications

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
TOTAL FUNCTION						
Output Leakage Current, DCL Disable						
PPMU Range E	−10.0	±4.0	+10.0	nA	P	−2.0 V < VDUTx < +6.5 V, PPMU and DCL disabled, PPMU Range E, VCL = −2.5 V, VCH = +7.5 V
PPMU Range A, Range B, Range C, and Range D		±4.0		nA	C_T	−2.0 V < VDUTx < +6.5 V, PPMU and DCL disabled, PPMU Range A, Range B, Range C, Range D, VCL = −2.5 V, VCH = +7.5 V
Output Leakage Current, Driver High-Z Mode	−2		+2	µA	P	−2.0 V < VDUTx < +7.0 V, PPMU disabled and DCL enabled, RCVx active, VCL = −2.5 V, VCH = +7.5 V
DUTx Pin Capacitance		1.2		pF	S	Drive VIT = 0.0 V
DUTx Pin Voltage Range	−2.0		+7.0	V	D	
POWER SUPPLIES						
Total Supply Range, VPLUS to VSS		22.75	23.55	V	D	
VPLUS Supply, VPLUS	15.90	16.75	17.60	V	D	Defines dc PSR conditions
Positive Supply, VDD	9.5	10.0	10.5	V	D	Defines dc PSR conditions
Negative Supply, VSS	−6.3	−6.0	−5.7	V	D	Defines dc PSR conditions
Logic Supply, VCC	2.3	2.5	3.5	V	D	Defines dc PSR conditions
Comparator Output Termination, VTTCx	0.5	1.2	3.3	V	D	
VPLUS Supply Current, VPLUS		1.1	2.5	mA	P	VHH pin disabled
	4.75	13.28	16.25	mA	P	VHH pin enabled, RCVx active, no load, VHH programmed level = 13.0 V
Logic Supply Current, VCC	−125	1	+125	µA	P	Quiescent (SPI is static); VCC = 2.5 V
		7.5		mA	S	Current drawn during clocked portion of device reset sequence
Termination Supply Current, VTTCx	30	45	50	mA	P	
Positive Supply Current, VDD	90	99	115	mA	P	Load power-down (IOH = IOL = 0 mA)
Negative Supply Current, VSS	155	172	185	mA	P	Load power-down (IOH = IOL = 0 mA)
Total Power Dissipation	1.9	2.1	2.3	W	P	Load power-down (IOH = IOL = 0 mA)
Positive Supply Current, VDD	145	174	210	mA	P	Load active off (IOH = IOL = 25 mA)
Negative Supply Current, VSS	210	246	280	mA	P	Load active off (IOH = IOL = 25 mA)
Total Power Dissipation	3.0	3.3	3.6	W	P	Load active off (IOH = IOL = 25 mA)
Positive Supply Current, VDD		167		mA	C_T	Load active off (IOH = IOL = 25 mA), calibrated
Negative Supply Current, VSS		238		mA	C_T	Load active off (IOH = IOL = 25 mA), calibrated
Total Power Dissipation		3.2		W	C_T	Load active off (IOH = IOL = 25 mA), calibrated
Positive Supply Current, VDD		109		mA	C_T	Load power-down, PPMU standby
Negative Supply Current, VSS		183		mA	C_T	Load power-down, PPMU standby
Total Power Dissipation		2.3		W	C_T	Load power-down, PPMU standby

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
TEMPERATURE MONITOR						
Temperature Sensor Gain		10		mV/K	D	
Temperature Sensor Accuracy over Temperature Range		±6		K	C_T	
VREF INPUT REFERENCE						
DAC Reference Input Voltage Range (VREF Pin)	4.950	5.000	5.050	V	D	Provided externally: VREF pin = +5.000 V VREFGND pin = 0.000 V (not referenced to V_{DUTGND})
Input Bias Current			100	µA	P	Tested with 5.000 V applied
DUTGND INPUT						
Input Voltage Range, Referenced to AGND	−0.1		+0.1	V	D	
Input Bias Current	−100		+100	µA	P	Tested at −100 mV and +100 mV

Table 2. Driver (VIH − VIL ≥ 100 mV to Meet DC and AC Performance Specifications)

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
DC SPECIFICATIONS						
High-Speed Differential Input Characteristics						
High Speed Input Termination Resistance: DATx, RCVx	92	100	108	Ω	P	Impedance between each pair of DATx and RCVx pins; push 4 mA into positive pin, force 0.8 V on negative pin, measure voltage between pins; calculate resistance (ΔV/ΔI)
Input Voltage Differential: DATx, RCVx	0.2	0.4	1.0	V	D	0.2 V < V_{DM} < 1.0 V
Input Voltage Range: DATx, RCVx	0.0		3.3	V	D	0.0 V < (V_{CM} ± V_{DM}/2) < 3.3 V
Output Characteristics						
Output High Range, VIH	−1.4		+6.5	V	D	
Output Low Range, VIL	−1.5		+6.4	V	D	
Output Term Range, VIT	−1.5		+6.5	V	D	
Functional Amplitude (VIH – VIL)	0.0	8.0		V	D	
DC Output Current Limit Source	75		130	mA	P	Drive high, VIH = +6.5 V, short DUTx pin to −1.5 V, measure current
DC Output Current Limit Sink	−130		−75	mA	P	Drive low, VIL = −1.5 V, short DUTx pin to +6.5 V, measure current
Output Resistance, ±40 mA	46	48.6	51	Ω	P	ΔVDUT/ΔIDUT; source: VIH = 3.0 V, IDUT = +1 mA, +40 mA; sink: VIL = 0.0 V, IDUT = −1 mA, −40 mA
DC ACCURACY						VIH tests with VIL = −2.5 V, VIT = −2.5 V VIL tests with VIH = +7.5 V, VIT = +7.5 V VIT tests with VIL = −2.5 V, VIH = +7.5 V, unless otherwise specified
VIH, VIL, VIT Offset Error	−500		+500	mV	P	Measured at DAC Code 0x4000 (0 V), uncalibrated
VIH, VIL, VIT Offset Tempco		±625		µV/°C	C_T	
VIH, VIL, VIT Gain	1.0		1.1	V/V	P	Gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (5 V); based on ideal DAC transfer functions (see Table 21)
VIH, VIL, VIT Gain Tempco		±40		ppm/°C	C_T	
VIH, VIL, VIT DNL		±1		mV	C_T	After two point gain/offset calibration; calibration points at 0x4000 (0 V) output; 0xC000 (+5 V) output; measured over full specified output range
VIH, VIL, VIT INL	−7		+7	mV	P	After two point gain/offset calibration; applies to nominal VDD = +10.0 V supply case only

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
VIH, VIL, VIT Resolution		153		µV	D	
DUTGND Voltage Accuracy	−7	±2	+7	mV	P	Over ±0.1 V range; measured at end points of VIH, VIL, and VIT functional range
DC Levels Interaction						DC interaction on VIL, VIH, and VIT output level while other driver DAC levels are varied
VIH vs. VIL		±0.2		mV	C_T	Monitor interaction on VIH = +6.5 V; sweep VIL = −1.5 V to +6.4 V, VIT = +1.0 V
VIH vs. VIT		±1		mV	C_T	Monitor interaction on VIH = +6.5 V; sweep VIT = −1.5 V to +6.5 V, VIL = 0.0 V
VIL vs. VIH		±0.2		mV	C_T	Monitor interaction on VIL = −1.5 V; sweep VIH = −1.4 V to +6.5 V, VIT = +1.0 V
VIL vs. VIT		±1		mV	C_T	Monitor interaction on VIL = −1.5 V; sweep VIT = −1.5 V to +6.5 V, VIH = +2.0 V
VIT vs. VIH		±1		mV	C_T	Monitor interaction on VIT = +1.0 V; sweep VIH = −1.4 V to +6.5 V, VIL = −1.5 V
VIT vs. VIL		±1		mV	C_T	Monitor interaction on VIT = +1.0 V; sweep VIL = −1.5 V to +6.4 V, VIH = +6.5 V
Overall Voltage Accuracy		±8		mV	C_T	VIH − VIL ≥ 100 mV; sum of INL, dc interaction, DUTGND, and tempco errors over ±5°C, after calibration
VIH, VIL, VIT DC PSRR		±10		mV/V	C_T	Measured at calibration points
AC SPECIFICATIONS						All ac specifications performed after calibration
Rise/Fall Times						Toggle DATx
0.2 V Programmed Swing, T_{RISE}		215		ps	C_B	20% to 80%, VIH = 0.2 V, VIL = 0.0 V, terminated
0.2 V Programmed Swing, T_{FALL}		277		ps	C_B	20% to 80%, VIH = 0.2 V, VIL = 0.0 V, terminated
0.5 V Programmed Swing, T_{RISE}		218		ps	C_B	20% to 80%, VIH = 0.5 V, VIL = 0.0 V, terminated
0.5 V Programmed Swing, T_{FALL}		274		ps	C_B	20% to 80%, VIH = 0.5 V, VIL = 0.0 V, terminated
1.0 V Programmed Swing, T_{RISE}	150	222	320	ps	P	20% to 80%, VIH = 1.0 V, VIL = 0.0 V, terminated
1.0 V Programmed Swing, T_{FALL}	150	283	320	ps	P	20% to 80%, VIH = 1.0 V, VIL = 0.0 V, terminated
2.0 V Programmed Swing, T_{RISE}		297		ps	C_B	20% to 80%, VIH = 2.0 V, VIL = 0.0 V, terminated
2.0 V Programmed Swing, T_{FALL}		322		ps	C_B	20% to 80%, VIH = 2.0 V, VIL = 0.0 V, terminated
3.0 V Programmed Swing, T_{RISE}		447		ps	C_B	20% to 80%, VIH = 3.0 V, VIL = 0.0 V, terminated
3.0 V Programmed Swing, T_{FALL}		397		ps	C_B	20% to 80%, VIH = 3.0 V, VIL = 0.0 V, terminated
5.0 V Programmed Swing, T_{RISE}		1117		ps	C_B	10% to 90%, VIH = 5.0 V, VIL = 0.0 V, unterminated
5.0 V Programmed Swing, T_{FALL}		798		ps	C_B	10% to 90%, VIH = 5.0 V, VIL = 0.0 V, unterminated
Rise to Fall Matching		−25		ps	C_B	Rise to fall within one channel, VIH = 2.0 V, VIL = 0.0 V, terminated
		−61		ps	C_B	Rise to fall within one channel; VIH = 1.0 V, VIL = 0.0 V, terminated
Minimum Pulse Width						Toggle DATx
0.5 V Programmed Swing		725		ps	C_B	VIH = 0.5 V, VIL = 0.0 V, terminated, timing error less than +69/−33 ps
		725		ps	C_B	VIH = 0.5 V, VIL = 0.0 V, terminated, less than 10% amplitude loss
Maximum Toggle Rate		2040		Mbps	C_B	VIH = 0.5 V, VIL = 0.0 V, terminated, less than 10% loss at 50% duty
1.0 V Programmed Swing		725		ps	C_B	VIH = 1.0 V, VIL = 0.0 V, terminated, timing error less than +58/−35 ps
		725		ps	C_B	VIH = 1.0 V, VIL = 0.0 V, terminated, less than 10% amplitude loss

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
Maximum Toggle Rate		2040		Mbps	C_B	VIH = 1.0 V, VIL = 0.0 V, terminated, less than 10% loss at 50% duty
2.0 V Programmed Swing		725		ps	C_B	VIH = 2.0 V, VIL = 0.0 V, terminated, timing error less than +80/−48 ps
		725		ps	C_B	VIH = 2.0 V, VIL = 0.0 V, terminated, less than 10% amplitude loss
Maximum Toggle Rate		1400		Mbps	C_B	VIH = 2.0 V, VIL = 0.0 V, terminated, less than 10% loss at 50% duty
3.0 V Programmed Swing		900		ps	C_B	VIH = 3.0 V, VIL = 0.0 V, terminated, timing error less than +50/−83 ps
		900		ps	C_B	VIH = 3.0 V, VIL = 0.0 V, terminated, less than 10% amplitude loss
Maximum Toggle Rate		1100		Mbps	C_B	VIH = 3.0 V, VIL = 0.0 V, terminated, less than 10% amplitude loss at 50% duty cycle
Dynamic Performance, Drive (VIH to VIL)						Toggle DATx
Propagation Delay Time		1.26		ns	C_B	VIH = 2.0 V, VIL = 0.0 V, terminated
Propagation Delay Tempco		1.4		ps/°C	C_B	VIH = 2.0 V, VIL = 0.0 V, terminated
Delay Matching, Edge to Edge		43		ps	C_B	VIH = 2.0 V, VIL = 0.0 V, terminated, rising vs. falling
Delay Matching, Channel to Channel		32		ps	C_B	VIH = 2.0 V, VIL = 0.0 V, terminated, rising vs. rising, falling vs. falling
Delay Change vs. Duty Cycle		−28		ps	C_B	VIH = 2.0 V, VIL = 0.0 V, terminated, 5% to 95% duty cycle
Overshoot and Undershoot		−116		mV	C_B	VIH = 2.0 V, VIL = 0.0 V, terminated, driver CLC set to 0
Settling Time (VIH to VIL)						Toggle DATx
To Within 3% of Final Value		1.7		ns	C_B	VIH = 2.0 V, VIL= 0.0 V, terminated
To Within 1% of Final Value		45		ns	C_B	VIH = 2.0 V, VIL= 0.0 V, terminated
Dynamic Performance, VTerm (VIH or VIL to/from VIT)						Toggle RCVx
Propagation Delay Time		1.39		ns	C_B	VIH = 2.0 V, VIT = 1.0 V, VIL = 0.0 V, terminated
Propagation Delay Tempco		2.3		ps/°C	C_B	VIH = 2.0 V, VIT = 1.0 V, VIL = 0.0 V, terminated
Transition Time, Active to VIT		310		ps	C_B	20% to 80%, VIH = 2.0 V, VIT = 1.0 V, VIL = 0.0 V, terminated
Transition Time, VIT to Active		329		ps	C_B	20% to 80%, VIH = 2.0 V, VIT = 1.0 V, VIL = 0.0 V, terminated
Dynamic Performance, Inhibit (VIH or VIL to/from Inhibit)						Toggle RCVx
Transition Time, Inhibit to Active		357		ps	C_B	20% to 80%, VIH = +1.0 V, VIL = −1.0 V, terminated
Transition Time, Active to Inhibit		1.34		ns	C_B	20% to 80%, VIH = +1.0 V, VIL = −1.0 V, terminated
Prop Delay, Inhibit to VIH		2.6		ns	C_B	VIH = +1.0 V, VIL = −1.0 V, terminated; measured from RCVx input crossing to DUTx pin output 50%
Prop Delay, Inhibit to VIL		2.8		ns	C_B	VIH = +1.0 V, VIL = −1.0 V, terminated
Prop Delay Matching, Inhibit to VIL vs. Inhibit to VIH		52		ps	C_B	VIH = +1.0 V, VIL = −1.0 V, terminated
Prop Delay, VIH to Inhibit		2.29		ns	C_B	VIH = +1.0 V, VIL = −1.0 V, terminated, measured from RCVx input crossing to DUTx pin output 50%
Prop Delay, VIL to Inhibit		2.02		ns	C_B	VIH = +1.0 V, VIL = −1.0 V, terminated
I/O Spike		24		mV pk-pk	C_B	VIH = 0.0 V, VIL = 0.0 V, terminated
Driver Pre-Emphasis (CLC)						
Pre-Emphasis Amplitude Rising		35		%	C_B	VIH = 2.0 V, VIL = 0.0 V, terminated, DRV_CLC_x[15:13] = 7
		14		%	C_B	VIH = 2.0 V, VIL = 0.0 V, terminated, DRV_CLC_x[15:13] = 0
Pre-Emphasis Amplitude Falling		24		%	C_B	VIH = 2.0 V, VIL = 0.0 V, terminated, DRV_CLC_x[15:13] = 7
		16		%	C_B	VIH = 2.0 V, VIL = 0.0 V, terminated, DRV_CLC_x[15:13] = 0

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
Pre-Emphasis Resolution		2		%	D	
Pre-Emphasis Time Constant		0.8		ns	C_B	VIH = 2.0 V, VIL = 0.0 V, terminated

Table 3. Reflection Clamp (Clamp Accuracy Specifications Apply Only When VCH − VCL > 0.8 V)

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
VCH/VCL PROGRAMMABLE RANGE	−2.5		+7.5	V	D	DC specifications apply over full functional range unless noted.
VCH						
VCH Functional Range	−1.2		+7.0	V	D	
VCH Offset Error	−300		+300	mV	P	Driver high-Z, sinking 1 mA, measured at DAC Code 0x4000, uncalibrated.
VCH Offset Tempco		±0.5		mV/°C	C_T	
VCH Gain	1.0		1.1	V/V	P	Driver high-Z, sinking 1 mA, gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (5 V), based on ideal DAC transfer function (see Table 21).
VCH Gain Tempco		±30		ppm/°C	C_T	
VCH Resolution		153		µV	D	
VCH DNL		±1		mV	C_T	Driver high-Z, sinking 1 mA, after two point gain/offset calibration; calibration points at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (5 V), measured over functional clamp range.
VCH INL	−20		+20	mV	P	Driver high-Z, sinking 1 mA, after two point gain/offset calibration; calibration points at 0x4000 (0 V) and 0xC000 (5 V), measured over functional clamp range.
VCL						
VCL Functional Range	−2		+6.2	V	D	
VCL Offset Error	−300		+300	mV	P	Driver high-Z, sourcing 1 mA, measured at DAC Code 0x4000, uncalibrated.
VCL Offset Tempco		±0.5		mV/°C	C_T	
VCL Gain	1.0		1.1	V/V	P	Drive high-Z, sourcing 1 mA, gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (5 V), based on ideal DAC transfer function (see Table 21).
VCL Gain Tempco		±30		ppm/°C	C_T	
VCL Resolution		153		µV	D	
VCL DNL		±1		mV	C_T	Driver high-Z, sourcing 1 mA, after two point gain/offset calibration; calibration points at 0x4000 (0 V) and 0xC000 (+5 V), measured over functional clamp range.
VCL INL	−20		+20	mV	P	Driver high-Z, sourcing 1 mA, after two point gain/offset calibration; calibration points at 0x4000 (0 V) and 0xC000 (+5 V), measured over functional clamp range.
DC Clamp Current Limit, VCH	−120		−75	mA	P	Driver high-Z, VCH = 0 V, VCL = −2.0 V, VDUTx = +5.0 V.
DC Clamp Current Limit, VCL	+75		+120	mA	P	Driver high-Z, VCH = +6.0 V, VCL = +5.0 V, VDUTx = 0.0 V.
DUTGND Voltage Accuracy	−7	±2	+7	mV	P	Over ±0.1 V range, measured at end points of VCH and VCL functional range.

Table 4. Normal Window Comparator (NWC) (Unless Otherwise Specified: VOH Tests at VOL = −1.5 V, VOL Tests at VOH = +6.5 V, Specifications Apply to Both Comparators)

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
DC SPECIFICATIONS						
Input Voltage Range	−1.5		+6.5	V	D	
Differential Voltage Range	±0.1		±8.0	V	D	
Comparator Input Offset Voltage	−250		+250	mV	P	Measured at DAC Code 0x4000 (0V), uncalibrated
Input Offset Voltage Tempco		±100		µV/°C	C_T	
Gain	1.0		1.1	V/V	P	Gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (5 V); based on ideal DAC transfer function (see Table 21)
Gain Tempco		±25		ppm/°C	C_T	
Threshold Resolution		153		µV	D	
Threshold DNL		±1		mV	C_T	Measured over −1.5 V to +6.5 V functional range after two point gain/offset calibration; calibration points at 0x4000 (0 V) and 0xC000 (5 V)
Threshold INL	−7		+7	mV	P	Measured over −1.5 V to +6.5 V functional range after two point gain/offset calibration; calibration points at 0x4000 (0 V) and 0xC000 (5 V)
DUTGND Voltage Accuracy	−7	±2	+7	mV	P	Over ±0.1 V range; measured at end points of VOH and VOL functional range
Uncertainty Band		5		mV	C_B	VDUTx = 0 V, sweep comparator threshold to determine the uncertainty band
Maximum Programmable Hysteresis		96		mV	C_B	
Hysteresis Resolution		5		mV	D	Calculated over hystersis control Code 10 to Code 31
DC PSRR		±5		mV/V	C_T	Measured at calibration points
Digital Output Characteristics						
Internal Pull-Up Resistance to Comparator, VTTC	46	50	54	Ω	P	Pull 1 mA and 10 mA from Logic 1 leg and measure ΔV to calculate resistance; measured ΔV/9 mA; done for both comparator logic states
Comparator Termination Voltage, VTTC	0.5	1.2	3.3	V	D	
Common Mode Voltage		VTTC − 0.3		V	C_T	Measured with 100 Ω differential termination
	VTTC − 0.5		VTTC	V	P	Measured with no external termination
Differential Voltage		250		mV	C_T	Measured with 100 Ω differential termination
	450	500	550	mV	P	Measured with no external termination
Rise/Fall Times, 20% to 80%		166		ps	C_B	Measured with 50 Ω to external termination voltage (VTTC)
AC SPECIFICATIONS						All ac specifications performed after dc level calibration, input transition time of ~200 ps, 20% to 80%, measured with 50 Ω to external termination voltage (VTTC); peaking set to CLC = 2, unless otherwise specified
Propagation Delay, Input to Output		0.93		ns	C_B	VDUTx: 0 V to 1.0 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.5 V
Propagation Delay Tempco		1.6		ps/°C	C_B	VDUTx: 0 V to 1.0 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.5 V
Propagation Delay Matching High Transition to Low Transition		7		ps	C_B	VDUTx: 0 V to 1.0 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.5 V
Propagation Delay Matching High to Low Comparator		7		ps	C_B	VDUTx: 0 V to 1.0 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.5 V

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
Propagation Delay Dispersion						
Slew Rate 400 ps vs. 1 ns (20% to 80%)		19		ps	C_B	VDUTx: 0 V to 0.5 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.25 V
Overdrive 250 mV vs. 1.0 V		40		ps	C_B	For 250 mV, VDUTx: 0 V to 0.5 V swing; for 1.0 V, VDUTx: 0 V to 1.25 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.25 V
1 V Pulse Width 0.7 ns, 1 ns, 5 ns, 10 ns		+2/− 17		ps	C_B	VDUTx: 0 V to 1.0 V swing at~32.0 MHz; driver term mode, VIT = 0.0 V, comparator threshold = 0.5 V
0.5 V Pulse Width 0.6 ns, 1 ns, 5 ns, 10 ns		+3/− 24		ps	C_B	VDUTx: 0 V to 0.5 V swing at~32.0 MHz, driver term mode, VIT = 0.0 V; comparator threshold = 0.25 V
Duty Cycle 5% to 95%		21		ps	C_B	VDUTx: 0 V to 1.0 V swing at~32.0 MHz; driver term mode, VIT =0.0 V, comparator threshold = 0.5 V
Minimum Detectable Pulse Width		0.5		ns	C_B	VDUTx: 0 V to 1.0 V swing at 32.0 MHz, driver term mode, VIT = 0.0 V; greater than 50% output differential amplitude
Input Equivalent Bandwidth, Terminated		1520		MHz	C_B	VDUTx: 0 V to 1.0 V swing; driver term mode, VIT = 0.0 V, CLC = 2; as measured by shmoo plot; $f_{EQUIV} = 0.22/\sqrt{(t_{MEAS}^2 - t_{DUT}^2)}$
ERT High-Z Mode, 3 V, 20% to 80%		721		ps	C_B	VDUTx: 0 V to 3.0 V swing, driver high-Z as measured by shmoo plot; $f_{EQUIV} = 0.22/\sqrt{(t_{MEAS}^2 - t_{DUT}^2)}$
Comparator Pre-Emphasis (CLC)						
CLC Amplitude Range		16		%	C_B	VDUTx: 0 V to 1.0 V swing, driver term mode, VIT = 0.0 V, comparator pre-emphasis set to maximum
CLC Resolution		2.3		% per bit	C_B	3-bit amplitude control
Pre-Emphasis Time Constant		4.3		ns	C_B	VDUTx: 0 V to 1.0 V swing, driver term mode, VIT = 0.0 V, comparator pre-emphasis set to maximum

Table 5. Differential Mode Comparator (DMC) (Unless Otherwise Specified: VOH Tests at VOL = −1.1 V, VOL Tests at VOH = +1.1 V)

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
DC SPECIFICATIONS						
Input Voltage Range	−1.5		+6.5	V	D	
Functional Differential Range	±0.05		±1.1	V	D	
Maximum Differential Input			±8	V	D	
Input Offset Voltage	−250		+250	mV	P	Offset extrapolated from measurements at DAC Code 0x2666 (−1 V) and DAC Code 0x599A (+1 V), with V_{CM} = 0 V
Offset Voltage Tempco		±150		µV/°C	C_T	
Gain	1.0		1.1	V/V	P	Gain derived from measurements at DAC Code 0x2666 (−1 V) and DAC Code 0x599A (+1 V), based on ideal DAC transfer function (see Table 21)
Gain Tempco		±25		ppm/°C	C_T	
VOH, VOL Resolution		153		µV	D	
VOH, VOL DNL		±1		mV	C_T	After two point gain/offset calibration, V_{CM} = 0.0 V, calibration points at 0x2666 (−1 V) and 0x599A (+1 V)
VOH, VOL INL	−7		+7	mV	P	After two point gain/offset calibration, measured over VOH/VOL range of −1.1 V to +1.1 V, V_{CM} = 0.0 V; calibration points at 0x2666 (−1 V) and 0x599A (+1 V)
Uncertainty Band		7		mV	C_B	VDUTx = 0 V; sweep comparator threshold to determine the uncertainty band

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
Maximum Programmable Hysteresis		117		mV	C_B	
Hysteresis Resolution		5.6		mV	D	Calculated over hystersis control Code 10 to Code 31
CMRR	−1		+1	mV/V	P	Offset measured at V_{CM} = −1.5 V and +6.5 V with V_{DM} = 0.0 V, offset error change
DC PSRR		±5		mV/V	C_T	Measured at calibration points
AC SPECIFICATIONS						All ac specifications performed after dc level calibration, unless noted; input transition time ~200 ps, 20% to 80%, measured with 50 Ω to external termination voltage (VTTC), peaking set to CLC = 2, unless otherwise specified
Propagation Delay, Input to Output		0.83		ns	C_B	VDUT0 = 0 V, VDUT1: −0.5 V to +0.5 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.0 V, repeat for other channel
Propagation Delay Tempco		2.6		ps/°C	C_B	VDUT0 = 0 V, VDUT1: −0.5 V to +0.5 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.0 V, repeat for other channel
Propagation Delay Matching, High Transition to Low Transition		15		ps	C_B	VDUT0 = 0 V, VDUT1: −0.5 V to +0.5 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.0 V, repeat for other channel
Propagation Delay Matching, High to Low Comparator		17		ps	C_B	VDUT0 = 0 V, VDUT1: −0.5 V to +0.5 V swing, driver term mode, VIT = 0.0 V, comparator threshold = 0.0 V, repeat for other channel
Propagation Delay Change (Dispersion) With Respect To						
Slew Rate: 400 ps and 1 ns (20% to 80%)		31		ps	C_B	VDUT0 = 0.0 V; VDUT1: −0.5 V to +0.5 V swing; driver term mode, VIT = 0.0 V; comparator threshold = 0.0 V, repeat for other channel
Overdrive: 250 mV and 750 mV		32		ps	C_B	VDUT0 = 0.0 V; for 250 mV: VDUT1: 0 V to 0.5 V swing; for 750 mV: VDUT1: 0 V to 1.0 V swing; driver term mode, VIT = 0.0 V; comparator threshold = −0.25 V; repeat for other channel with comparator threshold = +0.25 V
1 V Pulse Width: 0.7 ns, 1 ns, 5 ns, 10 ns		+1/− 21		ps	C_B	VDUT0 = 0.0 V; VDUT1: −0.5 V to +0.5 V swing at 32 MHz; driver term mode, VIT = 0.0 V; comparator threshold = 0.0 V; repeat for other channel
0.5 V Pulse Width: 0.6 ns, 1 ns, 5 ns, 10 ns		+1/− 31		ps	C_B	VDUT0 = 0.0 V; VDUT1: −0.25 V to +0.25 V swing at 32 MHz; driver term mode, VIT = 0.0 V; comparator threshold = 0.0 V; repeat for other channel
Duty Cycle: 5% to 95%		18		ps	C_B	VDUT0 = 0.0 V; VDUT1: −0.5 V to +0.5 V swing at 32 MHz; driver term mode, VIT = 0.0 V; comparator threshold = 0.0 V; repeat for other channel
Minimum Detectable Pulse Width		0.5		ns	C_B	VDUT0 = 0.0 V; VDUT1: −0.5 V to +0.5 V swing at 32 MHz; driver term mode, VIT = 0.0 V; comparator threshold = 0.0 V; greater than 50% output differential amplitude; repeat for other channel
Input Equivalent Bandwidth, Terminated		1038		MHz	C_B	VDUT0 = 0.0 V; VDUT1: −0.5 V to +0.5 V swing; driver term mode, VIT = 0.0 V; comparator threshold = 0.0 V, CLC = 2 as measured by shmoo; repeat for other channel
Comparator Pre-Emphasis (CLC)						
CLC Amplitude Range		11		%	C_B	VDUT0 = 0.0 V; VDUT1: −0.8 V to +0.8 V swing, driver term mode, VIT = 0.0 V; comparator threshold = 0.0 V; comparator CLC set to maximum; repeat for other channel
CLC Resolution		1.6		% per bit	C_B	3-bit amplitude control
Pre-Emphasis Time Constant		4.8		ns	C_B	VDUT0 = 0.0 V; VDUT1: −0.8 V to +0.8 V swing, driver term mode, VIT = 0.0 V; comparator threshold = 0.0 V; comparator CLC set to maximum; repeat for other channel

Table 6. Active Load

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
DC SPECIFICATIONS						Load active on, RCVx active, unless otherwise noted
Input Characteristics						
VCOM Voltage Range	−1.5		+6.5	V	D	| IOL and IOH | ≤ 1 mA
	−1.0		+5.5	V	D	| IOL and IOH | ≤ 25 mA
VCOM Offset	−200		+200	mV	P	Measured at DAC Code 0x4000, uncalibrated
VCOM Offset Tempco		±25		µV/°C	C_T	
VCOM Gain	1.0		1.1	V/V	P	Gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (+5 V), based on ideal DAC transfer function (see Table 21)
VCOM Gain Tempco		±25		ppm/°C	C_T	
VCOM Resolution		153		µV	D	
VCOM DNL		±1		mV	C_T	IOH = IOL = 12.5 mA; after two point gain/offset calibration; measured over VCOM range of −1.5 V to +6.5 V; calibration points at 0x4000 (0 V) and 0xC000 (+5 V)
VCOM INL	−7		+7	mV	P	IOH = IOL = 12.5 mA; after two point gain/offset calibration; measured at end points of VCOM functional range
DUTGND Voltage Accuracy	−7	±2	+7	mV	P	Over ±0.1 V range
Output Characteristics						
Maximum Source Current	25			mA	D	−1.5 V to +5.5 V DUT range
IOL Offset	−600		+600	µA	P	IOH = −2.5 mA, VCOM = 1.5 V, VDUTx = 0.0 V; offset extrapolated from measurements at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA)
IOL Offset Tempco		±1		µA/°C	C_T	
IOL Gain Error	0		25	%	P	IOH = −2.5 mA, VCOM = 1.5 V, VDUTx = 0.0 V; gain derived from measurements at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA); based on ideal DAC transfer function (see Table 21 and Table 22)
IOL Gain Tempco		±25		ppm/°C	C_T	
IOL Resolution		763		nA	D	
IOL DNL		±4		µA	C_T	IOH = −2.5 mA, VCOM = 1.5 V, VDUTx = 0.0 V; after two point gain/offset calibration; measured over IOL range, 0 mA to 25 mA; calibrated at Code 0x451F (1 mA) and Code 0xA666 (20 mA)
IOL INL	−100	±20	+100	µA	P	IOH = −2.5 mA, VCOM = 1.5 V, VDUTx = 0.0 V; after two point gain/offset calibration
IOL 90% Commutation Voltage		0.25	0.4	V	P	IOH = IOL = 25 mA, VCOM = 2.0 V; measure IOL reference at VDUTx = −1.0 V; measure IOL current at VDUTx = 1.6 V; check >90% of reference current
IOL 90% Commutation Voltage		0.1		V	C_T	IOH = IOL = 1 mA, VCOM = 2.0 V; measure IOL reference at VDUTx = −1.0 V; measure IOL current at VDUTx = 1.9 V; check >90% of reference current
Maximum Sink Current	25			mA	D	−1.0 V to +6.5 V output range
IOH Offset	−600		+600	µA	P	IOL = −2.5 mA, VCOM = 1.5 V, VDUTx = 3.0 V; offset extrapolated from measurements at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA)
IOH Offset Tempco		±1		µA/°C	C_T	
IOH Gain Error	0		25	%	P	IOL = −2.5 mA, VCOM = 1.5 V, VDUTx = 3.0 V; gain derived from measurements at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA); based on ideal DAC transfer function (see Table 21 and Table 22)

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
IOH Gain Tempco		±25		ppm/°C	C_T	
IOH Resolution		763		nA	D	
IOH DNL		±4		µA	C_T	IOL = −2.5 mA, VCOM = 1.5 V, VDUTx = 3.0 V; after two point gain/offset calibration; measured over IOH range, 0 mA to 25 mA; calibrated at Code 0x451F (1 mA) and Code 0xA666 (20 mA)
IOH INL	−100	±25	+100	µA	P	IOL = −2.5 mA, VCOM = 1.5 V, VDUTx = 3.0 V; after two point gain/offset calibration
IOH 90% Commutation Voltage		0.25	0.4	V	P	IOH = IOL = 25 mA, VCOM = 2.0 V; measure IOH reference at VDUTx = 5.0 V; measure IOH current at VDUTx = 2.4 V; ensure >90% of reference current
		0.1		V	C_T	IOH = IOL = 1 mA, VCOM = 2.0 V; measure IOH reference at VDUTx = 5.0 V; measure IOH current at VDUTx = 2.1 V; ensure >90% of reference current
AC SPECIFICATIONS						All ac specifications performed after dc level calibration unless noted; load active on
Dynamic Performance						
Propagation Delay, Load Active On to Load Active Off; 50%, 90%		3.1		ns	C_B	Toggle RCVx; DUTx terminated 50 Ω to GND; IOL = IOH = 20 mA, VIH = VIL = 0 V; VCOM = +1.5 V for IOL and −1.5 V for IOH; measured from 50% point of RCVx − $\overline{\text{RCVx}}$ to 90% point of final output; repeat for drive low and drive high
Propagation Delay, Load Active Off to Load Active On; 50%, 90%		4.1		ns	C_B	Toggle RCVx; DUTx terminated 50 Ω to GND; IOL = IOH = 20 mA, VIH = VIL = 0 V; VCOM = +1.5 V for IOL and −1.5 V for IOH; measured from 50% point of RCVx − $\overline{\text{RCVx}}$ to 90% point of final output; repeat for drive low and drive high
Propagation Delay Matching		1.0		ns	C_B	Toggle RCVx; DUTx terminated 50 Ω to GND; IOL = IOH = 20 mA, VIH = VIL = 0 V; VCOM = +1.5 V for IOL and −1.5 V for IOH; active on vs. active off; repeat for drive low and drive high
Load Spike		106		mV pk-pk	C_B	Toggle RCVx; DUTx terminated 50 Ω to GND; IOL = IOH = 0 mA, VIH = VIL = 0 V; VCOM = +1.5 V for IOL and −1.5 V for IOH; repeat for drive low and drive high
Settling Time to 90%		1.6		ns	C_B	Toggle RCVx; DUTx terminated 50 Ω to GND; IOL = IOH = 20 mA, VIH = VIL = 0 V; VCOM = +1.5 V for IOL and −1.5 V for IOH; measured at 90% of final value

Table 7. PPMU (PPMU Enabled in FV, DCL Disabled)

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
FORCE VOLTAGE						
Current Range A	−40		+40	mA	D	
Current Range B	−1		+1	mA	D	
Current Range C	−100		+100	µA	D	
Current Range D	−10		+10	µA	D	
Current Range E	−2		+2	µA	D	
Voltage Range at Output						
Range A	−2.0		+5.75	V	D	Output range for full-scale source and sink.
	−2.0		+6	V	D	Output range for ±25 mA.
Range B, Range C, Range D, and Range E	−2.0		+6.5	V	D	Output range for full-scale source and sink.
Offset						
Range C	−100		+100	mV	P	Measured at DAC Code 0x4000 (0 V).
All Ranges		±10		mV	C_T	Measured at DAC Code 0x4000 (0 V).
Offset Tempco, All Ranges		±25		µV/°C	C_T	

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
Gain						
Range C	1.0		1.1	V/V	P	Gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (5 V); based on ideal DAC transfer function (see Table 21 and Table 23).
All Ranges		1.05		V/V	C_T	Gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (5 V); based on ideal DAC transfer function (see Table 21 and Table 23).
Gain Tempco, All Ranges		±25		ppm/°C	C_T	Gain derived from measurements at DAC Code 0x4000 (0V) and DAC Code 0xC000 (5 V); calibration point 0x4000 (0 V) and 0xC000 (+5 V) output.
INL						
Range A		±1		mV	CT	After two point gain/offset calibration, output range of −2.0 V to +5.75 V, PPMU Current Range A only.
Range C	−1.7		+1.7	mV	P	After two point gain/offset calibration; output range of −2.0 V to +6.5 V.
Range B, Range D, and Range E		±1		mV	C_T	After two point gain/offset calibration, output range of −2.0 V to +6.5 V.
Compliance vs. Current Load						
Range A		±40		mV	C_T	Force −2.0 V; measure voltage while sinking zero and full-scale current; measure ΔV; force +5.75 V; measure voltage while sourcing zero and full-scale current; measure ΔV.
		±25		mV	C_T	Force −2.0 V; measure voltage while sinking zero and 25 mA current; measure ΔV; force +6 V; measure voltage while sourcing zero and 25 mA current; measure ΔV.
Range B, Range C, Range D, and Range E		±1		mV	C_T	Force −2.0 V; measure voltage while sinking zero and full-scale current; measure ΔV; force +6.5 V; measure voltage while sourcing zero and full-scale current; measure ΔV.
Current Limit, Source and Sink All Ranges	120	140	180	%FS	P	Sink: force −2.0 V, short DUTx to +6.5 V; source: force +6.5 V, short DUTx to −2.0 V; repeat for each current range; example: Range A FS = 40 mA, 120% FS = 48 mA 180% FS = 72 mA
DUTGND Voltage Accuracy	−7	±2	+7	mV	P	Over ±0.1 V range; measured at endpoints of PPMU_VINFV functional range (see Figure 136).
MEASURE CURRENT						PPMU enabled in FIMI, DCL disabled.
DUTx Pin Voltage Range at Full Current						
Range A	−2.0		+5.75	V	D	
Range B, Range C, Range D, and Range E	−2.0		+6.5	V	D	
Zero-Current Offset, Range B	−2		+2	%FSR	P	Interpolated from measurements sourcing and sinking 80% FSR current each range; FSR = 80 mA for Range A, 2 mA for Range B, 200 µA for Range C, 20 µA for Range D, 4 µA for Range E (see Table 21 and Table 23).
All Ranges		±0.5		%FSR	C_T	See Table 21 and Table 23.
Zero-Current Offset Tempco, Range A		±0.001		%FSR/°C	C_T	See Table 21 and Table 23.

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
Range B, Range C, and Range D		±0.001		%FSR/°C	C_T	
Range E		±0.002		%FSR/°C	C_T	
Gain Error						
Range B	−30		+5	%	P	Based on measurements sourcing and sinking, 80% FSR current.
All Ranges		−10		%	C_T	Based on measurements sourcing and sinking, 80% FSR current.
Gain Tempco						
Range A		±50		ppm/°C	C_T	
Range B, Range C, Range D, and Range E		±25		ppm/°C	C_T	
INL						
Range A		±0.0125		%FSR	C_T	Range A, after two point gain/offset calibration at ±80% FSR current; measured over FSR output of −40 mA to +40 mA.
Range B	−0.03		+0.03	%FSR	P	After two point gain/offset calibration at ±80% FSR current; measured over FSR output of −1 mA to +1 mA.
Range C, Range D, and Range E		±0.01		%FSR	C_T	After two point gain/offset calibration at ±80% FSR current; measured over each FSR output for Range C, Range D, and Range E.
DUTx Pin Voltage Rejection	−1.2		+1.2	µA	P	Range B, FVMI, force −1 V and 5 V into load of 0.5 mA, measure ΔI reported at PPMU_MEASx pin.
DUTGND Voltage Accuracy	−7	±2	+7	mV	P	Over ±0.1 V range (see Figure 136).
FORCE CURRENT						PPMU enabled in FIMI, DCL disabled.
DUTx Pin Voltage Range in Range A	−2.0		+5.75	V	D	At full-scale source and sink current.
	−2.0		+6	V	D	At 25 mA source and sink current.
DUTx Pin Voltage Range at Full Current, Range B, Range C, Range D, and Range E	−2.0		+6.5	V	D	
Zero-Current Offset, All Ranges	−14.5		+14.5	%FSR	P	Extrapolated from measurements at Code 0x4CCC and Code 0xB333 for each range (see Table 21 and Table 23).
Zero-Current Offset Tempco		±0.002		%FSR/°C	C_T	
Gain Error, All Ranges	−5		+25	%	P	Derived from measurements at Code 0x4CCC and Code 0xB333 for each range (see Table 21 and Table 23).
Gain Tempco						
Range A		±50		ppm/°C	C_T	Significant PPMU self-heating effects in Range A can influence gain drift/tempco measurements.
Range B, Range C, Range D, and Range E		±25		ppm/°C	C_T	
INL						
Range A	−0.12	±0.02	+0.12	%FSR	P	After two point gain/offset calibration; measured over FSR output of −40 mA to +40 mA.
Range B, Range C, and Range D	−0.03		+0.03	%FSR	P	After two point gain/offset calibration; measured over FSR output; repeat for Range B, Range C, and Range D.

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
Range E	−0.045		+0.045	%FSR	P	After two point gain/offset calibration; measured over FSR output.
Force Current Compliance vs. Voltage Load						
Range A	−0.3		+0.3	%FSR	P	Force positive full-scale current driving −2.0 V and +5.75 V; measure ΔI at DUTx pin; force negative full-scale current driving −2.0 V and +5.75 V; measure ΔI at DUTx pin.
	−0.3		+0.3	%FSR	P	Force +25 mA driving −2.0 V and +6.0 V; measure ΔI at DUTx pin; force −25 mA driving −2.0 V and +6.0 V; measure ΔI at DUTx pin.
	−0.06		+0.06	%FSR	P	Force positive full-scale current driving 0.0 V and +4.0 V; measure ΔI at DUTx pin; force negative full-scale current driving 0.0 V and +4.0 V; measure ΔI at DUTx pin.
Range B and Range C	−0.3		+0.3	%FSR	P	Force positive full-scale current driving −2.0 V and +6.5 V; measure ΔI at DUTx pin; force negative full-scale current driving −2.0 V and +6.5 V; measure ΔI at DUTx pin.
	−0.06		+0.06	%FSR	P	Force positive full-scale current driving 0.0 V and +4.0 V; measure ΔI at DUTx pin; force negative full-scale current driving 0.0 V and +4.0 V; measure ΔI at DUTx pin.
Range D	−0.3		+0.3	%FSR	P	Force positive full-scale current driving −2.0 V and +6.5 V; measure ΔI at DUTx pin; force negative full-scale current driving −2.0 V and +6.5 V; measure ΔI at DUTx pin; allows for 10 nA of DUTx pin leakage.
Range E	−0.85		+0.85	%FSR	P	Force positive full-scale current driving −2.0 V and +6.5 V; measure ΔI at DUTx pin; force negative full-scale current driving −2.0 V and +6.5 V; measure ΔI at DUTx pin; allows for 10 nA of DUTx pin leakage.
MEASURE VOLTAGE						PPMU enabled, FVMV, DCL disabled.
Voltage Range	−2.0		+6.5	V	D	
Offset	−25		+25	mV	P	Range B, VDUTx = 0 V; offset = (PPMU_MEAS − VDUTx).
Offset Tempco		±10		µV/°C	C_T	
Gain	0.98		1.02	V/V	P	Range B, gain derived from measurements at VDUTx = 0.0 V and +5.0 V.
Gain Tempco		±1		ppm/°C	C_T	
INL	−1.7		+1.7	mV	P	Range B, measured over −2.0 V to +6.5 V.
Measure Pin DC Characteristics						
Output Range	−2.0		+6.5	V	D	
DC Output Current			4	mA	D	
Output Impedance			200	Ω	P	PPMU enabled in FVMV, DCL disabled; Source resistance: PPMU force +6.5 V with 0 mA, +4 mA load Sink resistance: PPMU force −2.0 V with 0 mA, −4 mA load Resistance = ΔV/ΔI at PPMU_MEAS pin.
Output Leakage Current When Tristated	−1		+1	µA	P	Tested at −2.0 V and +6.5 V.

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
Output Short-Circuit Current	−25		+25	mA	P	PPMU enabled in FVMV, DCL disabled; Source: PPMU force +6.5 V, PPMU_MEAS to −2.0 V Sink: PPMU force −2.0 V, PPMU_MEAS to +6.5 V
PPMU_MEASx Pin, Output Capacitance		2		pF	S	
PPMU_MEASx Pin, Load Capacitance		100		pF	S	Maximum load capacitance.
VOLTAGE CLAMPS						PPMU enabled in FIMI, DCL disabled, PPMU clamps enabled; clamp accuracy specifications apply only when VCH > VCL.
Low Clamp Range (VCL)	−2.0		+4.0	V	D	
High Clamp Range (VCH)	0.0		+6.5	V	D	
Positive Clamp Voltage Droop	−300	±1	+300	mV	P	ΔV seen at DUTx pin, Range A, VCH = +5.0 V, VCL = −1 V; PPMU force 5 mA and 40 mA into open.
Negative Clamp Voltage Droop	−300	±1	+300	mV	P	ΔV seen at DUTx pin, Range A, VCH = +5.0 V, VCL = −1 V, PPMU force −5 mA and 40 mA into open.
Offset, PPMU Clamp VCH/VCL	−300		+300	mV	P	Range B, PPMU force ±0.5 mA into open; VCH measured at DAC Code 0x4000 (0 V) with VCL at Code 0x0000 (−2.5 V); VCL measured at DAC Code 0x4000 (0 V) with VCH at 0xFFFF (+7.5 V).
Offset Tempco, PPMU Clamp VCH/VCL		±0.5		mV/°C	C_T	
Gain, PPMU Clamp VCH/VCL	1.0		1.2	V/V	P	Range B, PPMU force ±0.5 mA into open; VCH gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (+5.0 V) with VCL at Code 0x0000 (−2.5 V); VCL gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xA666 (+4.0 V) with VCH at 0xFFFF (+7.5 V).
Gain Tempco, PPMU Clamp VCH/VCL		±25		ppm/°C	C_T	
INL, PPMU Clamp VCH/VCL	−20		+20	mV	P	Range B, PPMU force ±0.5 mA into open, after two point gain/offset calibration; measured over PPMU clamp functional range.
DUTGND Voltage Accuracy	−7	±2	+7	mV	P	Over ±0.1 V range; measured at end points of clamp functional range.
SETTLING/SWITCHING TIMES						
Force Voltage Settling Time to 0.1% of Final Value						
Range A, 200 pF and 2000 pF Load		10		µs	S	PPMU enabled in FV, Range A, DCL disabled; program VIN steps from 0 V to 0.5 V and 5.0 V.
Range B, 200 pF and 2000 pF Load		12		µs	S	PPMU enabled in FV, Range B, DCL disabled; program VIN steps from 0 V to 0.5 V and 5.0 V.
Range C, 200 pF and 2000 pF Load		32		µs	S	PPMU enabled in FV, Range C, DCL disabled; program VIN steps from 0 V to 0.5 V and 5.0 V.
Force Voltage Settling Time to 1.0% of Final Value						
Range A, 200 pF & 2000 pf Load		8.1		µs	C_B	PPMU enabled in FV, Range A, DCL disabled; program VIN steps from 0 V to 5.0 V.
Range B, 200 pF and 2000 pf Load		8.1		µs	C_B	PPMU enabled in FV, Range B, DCL disabled; program VIN steps from 0 V to 5.0 V.
Range C, 200 pF and 2000 pf Load		8.1		µs	C_B	PPMU enabled in FV, Range C, DCL disabled; program VIN steps from 0 V to 5.0 V.

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
Range A, 200 pF and 2000 pf Load		2.5		µs	C_B	PPMU enabled in FV, Range A, DCL disabled; program VIN steps from 0 V to 0.5 V.
Range B, 200 pF and 2000 pf Load		6.3		µs	C_B	PPMU enabled in FV, Range B, DCL disabled; program VIN steps from 0 V to 0.5 V.
Range C, 200 pF and 2000 pf Load		8.1		µs	C_B	PPMU enabled in FV, Range C, DCL disabled; program VIN steps from 0 V to 0.5 V.
Force Current Settling Time to 0.1% of Final Value						
Range A, 200 pF in Parallel with 120 Ω		16		µs	S	PPMU enabled in FI, Range A, DCL disabled; program VIN step of 0 mA to 40 mA.
Range B, 200 pF in Parallel with 1.5 KΩ		10		µs	S	PPMU enabled in FI, Range B, DCL disabled; program VIN step of 0 mA to 1 mA.
Range C, 200 pF in Parallel with 15.0 KΩ		40		µs	S	PPMU enabled in FI, Range C, DCL disabled; program VIN step of 0 mA to 100 µA.
Force Current Settling Time to 1.0% of Final Value						
Range A, 200 pF in Parallel with 120 Ω		8.1		µs	C_B	PPMU enabled in FI, Range A, DCL disabled; program VIN step of 0 mA to 40 mA.
Range B, 200 pF in Parallel with 1.5 KΩ		7.5		µs	C_B	PPMU enabled in FI, Range B, DCL disabled; program VIN step of 0 mA to 1 mA.
Range C, 200 pF in Parallel with 15.0 KΩ		8.1		µs	C_B	PPMU enabled in FI, Range C, DCL disabled; program VIN step of 0 mA to 100 µA.
INTERACTION and CROSSTALK						
Measure Voltage Channel-to-Channel Crosstalk		±0.01		%FSR	C_T	0.01% × 8.5 V = 0.85 mV, PPMU enabled in FIMV, DCL disabled; CHx under test: Range B, forcing 0 mA into 0 V load; other channel: Range A, sweep 0 mA to 40 mA into 0 V load; report ΔV of PPMU_MEASx pin under test.
Measure Current Channel-to-Channel Crosstalk		±0.01		%FSR	C_T	0.01% × 5.0 V = 0.5 mV, PPMU enabled in FVMI, DCL disabled; CHx under test: Range E, forcing 0 V into 0 mA current load; other channel: Range E, sweep −2.0 V to +6.5 V into 0 mA current load; report ΔV of PPMU_MEASx pin under test.

Table 8. PPMU_Go/No-Go Comparators

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
Compare Voltage Range	−2.0		+6.5	V	D	
Input Offset Voltage	−250		+250	mV	P	Measured at DAC Code 0x4000 (0 V)
Input Offset Voltage Tempco		±50		µV/°C	C_T	
Gain	1.0		1.1	V/V	P	Gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (+5.0 V)
Gain Tempco		±25		ppm/°C	C_T	Applies at m = 1.0 and c = 0.0
Comparator Threshold Resolution		153		µV	D	
Comparator Threshold DNL		±1		mV	C_T	After two point gain/offset calibration; measured over VOH/VOL range − 2.0 V to +6.5 V; calibration points at 0x4000 (0 V) and 0xC000 (+5 V)
Comparator Threshold INL	−7		+7	mV	P	After two point gain/offset calibration; measured at end points of VOH and VOL functional range
DUTGND Voltage Accuracy	−7	±2	+7	mV	P	Over ±0.1 V range

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
Comparator Uncertainty Band		1.6		mV	C_B	Sweep comparator threshold to determine uncertainty (oscillation) band
DC Hysteresis		<1		mV	C_B	Sweep comparator threshold
COMPARATOR OUTPUTS						PPMU_CMPH*x*, PPMU_CMPLx
Output Logic High	VDD/4 − 0.5		VDD/4 + 0.5	V	P_F	Sourcing 100 µA
Output Logic Low	0		0.5	V	P_F	Sinking 100 µA

Table 9. PPMU_Sense Pin

Parameter	Min	Typ	Max	Unit	Test Level	Condition
PMU_Sx (SYSTEM PMU) SENSE PIN CHARACTERISTICS						
Voltage Range	−2.0		+7.0	V	D	DCL high-Z compliance range is −2.0 V to +7.0 V
Ext Sense Switch R_{ON}			2.5	kΩ	P	Push 0.5 mA into PMU_Sx with switch closed and DUTx pin at 0 V; calculate R = V/0.0005
Leakage	−2		+2	nA	P	Tested at −2.0 V and +7.0 V, switch open
Pin Capacitance (PMU_Sx)		0.5		pF	S	Switch open
PPMU_Sx (INTERNAL PPMU) SENSE PIN CHARACTERISTICS						
Voltage Range	−2.0		+6.5	V	D	PPMU input select in all states
Leakage	−2		+2	nA	P	Tested at −2.0 V and +6.5 V
Max Load Capacitance		2		nF	S	

Table 10. Serial Programmable Interface (SPI) (SDI, $\overline{\text{RST}}$, $\overline{\text{CS}}$, SCLK, SDO, $\overline{\text{BUSY}}$)

Parameter	Min	Typ	Max	Unit	Test Level	Condition
Input Logic High	1.8		VCC	V	P_F	SDI, $\overline{\text{RST}}$, $\overline{\text{CS}}$, SCLK.
Input Logic Low	0		0.7	V	P_F	
Input Bias Current	−10	±1	+10	µA	P	Tested at 0.0 V and VCC volts.
SCLK Clock Rate	0.5		50	MHz	D	
SCLK Pulse Width, Minimum		9		ns	C_T	
SCLK Crosstalk on DUTx Pin		30		mV	C_B	DCL disabled; PPMU FV enabled and forcing 0.0 V.
Serial Output Logic High	VCC − 0.5		VCC	V	P_F	SDO; sourcing 2 mA.
Serial Output Logic Low	0		0.5	V	P_F	Sinking 2 mA.
$\overline{\text{BUSY}}$ Pull-Up Voltage	2.3	2.5	3.5	V	D	$\overline{\text{BUSY}}$ is an open drain output that pulls low when the SPI requires additional SCLK cycles.
$\overline{\text{BUSY}}$ Active Voltage		0.2	0.8	V	P_F	$\overline{\text{BUSY}}$ active, sinking 2 mA.

Table 11. VHH Driver (VHH Mode Enabled, RCV Active)

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
VHH BUFFER						VHH mode enabled, RCVx active
Voltage Range	0.0		13.5	V	D	
Output High	13.5			V	P	VHH level = full scale, sourcing 15 mA
Output Low			5.9	V	P	VHH level = zero-scale, sinking 15 mA
Extrapolated Offset	−500		+500	mV	P	Extrapolated from measurements at DAC Code 0x8000 (+7 V) and DAC Code 0xC000 (+12 V)
Extrapolated Offset Tempco		±0.5		mV/°C	C_T	
Gain	2		2.2	V/V	P	Gain derived from measurements at DAC Code 0x8000 (+7 V) and DAC Code 0xC000 (+12 V); based on ideal DAC transfer function (see Table 21)
Gain Tempco		±25		ppm/°C	C_T	
Resolution		305		µV	D	
INL	−25		+25	mV	P	VHH mode enabled, RCVx active; after two point gain/offset calibration; measured over +5.9 V to +13.5 V; calibrate at Code 0x8000 (+7 V) and Code 0xC000 (+12 V)
DUTGND Voltage Accuracy		±4		mV	C_T	Over ±0.1 V range; measured at end points of VHH functional range
Output Resistance			10	Ω	P	ΔV/ΔI; VHH mode enabled, RCVx active; Source: VHH = +10.0 V, I = 0 mA, +15 mA Sink: VHH = +6.5 V, I = 0 mA, −15 mA
DC Output Current Limit Source	+60		+100	mA	P	VHH mode enabled, RCVx active; VHH = +13.5 V, short HVOUT pin to +5.9 V, measure current
DC Output Current Limit Sink	−100		−60	mA	P	VHH mode enabled, RCVx active, VHH = 5.9 V, short HVOUT pin to 13.5 V, measure current
VHH Rise Time (from VIL or VIH to VHH)		163		ns	C_B	20% to 80%, VHH mode enabled, toggle RCVx: VHH = 13.5 V, VIL = 0.0 V, VIH = 3.0 V, DATx = high; VHH = 13.5 V, VIL = 3.0 V, VIH = 4.0 V, DATx = low
VHH Fall Time (from VHH to VIL or VIH)		30		ns	C_B	20% to 80%, VHH mode enabled, toggle RCVx; VHH = 13.5 V, VIL = 0.0 V, VIH = 3.0 V, DATx = high; VHH = 13.5 V, VIL = 3.0 V, VIH = 4.0 V, DATx = low
Preshoot, Overshoot, and Undershoot		±40.0		mV	C_B	VHH mode enabled, toggle RCVx; VHH = 13.5 V, VIL = 0.0 V, VIH = 3.0 V, DATx = high; VHH = 13.5 V, VIL = 3.0 V, VIH = 4.0 V, DATx = low
VIL/VIH DRIVE FUNCTION						VHH mode enabled, RCVx inactive
Voltage Range	−0.1		+6.5	V	D	
Offset Voltage	−500		+500	mV	P	Measured at DAC Code 0x4000 (0 V), for DATx = high and DATx = low
Offset Voltage Tempco		1		mV/°C	C_T	
Gain	1.0		1.1	V/V	P	Gain derived from measurements at DAC Code 0x4000 (0 V) and DAC Code 0xC000 (5 V); based on ideal DAC transfer function (see Table 21)
Gain Tempco		±75		ppm/°C	C_T	
Resolution		153		µV	D	
INL	−20		+20	mV	P	VHH mode enabled, RCVx inactive; after two point gain/offset calibration; measured over −0.1 V to +6.0 V; calibrate at Code 0x4000 (0 V) and Code 0xC000 (+5.0 V)

Parameter	Min	Typ	Max	Unit	Test Level	Conditions
DUTGND Voltage Accuracy		±2		mV	C_T	Over ±0.1 V range; measured at end points of VIH and VIL functional range
Output Resistance	46	48	50	Ω	P	ΔV/ΔI; VHH mode enabled, RCVx inactive; Source: VIH = +3.0 V, I = +1 mA, +50 mA; Sink: VIL = +2.0 V; I = −1 mA, −50 mA
DC Output Current Limit Source	60		100	mA	P	VHH mode enabled, RCVx inactive, VIH = +6.0 V, short HVOUT pin to −0.1 V, DATx high, measure current
DC Output Current Limit Sink	−100		−60	mA	P	VHH mode enabled, RCVx inactive, VIL = −0.1 V, short HVOUT pin to +6.0 V, DATx low, measure current
Rise Time, VIL to VIH		6.4		ns	C_B	20% to 80%, VHH mode enabled, RCVx inactive, VIL = 0.0 V, VIH = 3.0 V, R_{LOAD} > 500 Ω, toggle DATx
Fall Time, VIH to VIL		7.3		ns	C_B	20% to 80%, VHH mode enabled, RCVx inactive, VIL = 0.0 V, VIH = 3.0 V, R_{LOAD} > 500 Ω, toggle DATx
Preshoot, Overshoot, and Undershoot		±30		mV	C_B	VHH mode enabled, RCVx inactive, VIL = 0.0 V, VIH = 3.0 V, R_{LOAD} > 500 Ω, toggle DATx

Table 12. Alarm Functions

Parameter	Min	Typ	Max	Unit	Test Level	Condition
DC CHARACTERISTICS						
Overvoltage Detect (OVD)						See Figure 137
Programmable Voltage Range	−2.5		+7.5	V	D	
Uncalibrated Error at −2.0 V	−200		+200	mV	P	Measured at DAC Code 0x0CCC (−2.0 V); OVD comparators not guaranteed to function as specified if VDUTx is outside absolute maximum voltage range
Uncalibrated Error at +7.0 V	−450		+450	mV	P	Measured at DAC Code 0xF333 (+7.0 V)
Offset Voltage Tempco		±0.5		mV/°C	C_T	Gain derived from measurements at DAC Code 0x4000 and DAC Code 0xC000
Gain		1.045		V/V	C_T	
Hysteresis		125		mV	C_T	
Thermal Alarm						See Figure 137
Setpoint Error		±10		°C	C_T	Relative to default value, 100°C
Thermal Hysteresis		−15		°C	C_T	
PPMU Clamp Alarm						See Figure 137 and Table 29 for electrical characteristics
$\overline{\text{ALARM}}$ Output Characteristics						
Off State Leakage		10	500	nA	P	Disable alarm, apply 2.5 V to $\overline{\text{ALARM}}$ pin, measure leakage current
Max On Voltage at100 µA		0.1	0.7	V	P	Activate alarm, force 100 µA into $\overline{\text{ALARM}}$ pin, measure active alarm voltage
Propagation Delay		1.5		µs	C_B	For OVD_HI: VDUTx: 0 V to 6 V swing, OVDH = +3.0 V, OVDL = −1.0 V For OVD_LO: VDUTx: 0 V to 6 V swing, OVDH = +7.0 V, OVDL= +3.0 V

SPI TIMING DETAILS

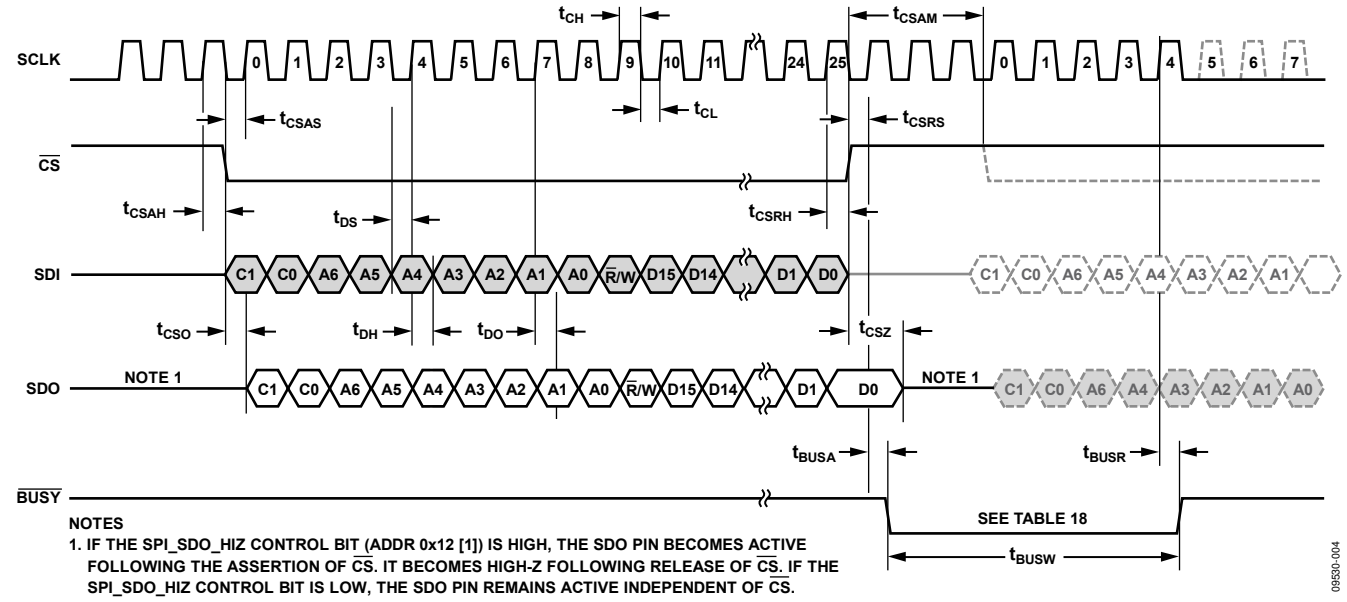


Figure 2. SPI Detailed Read/Write Timing Diagram

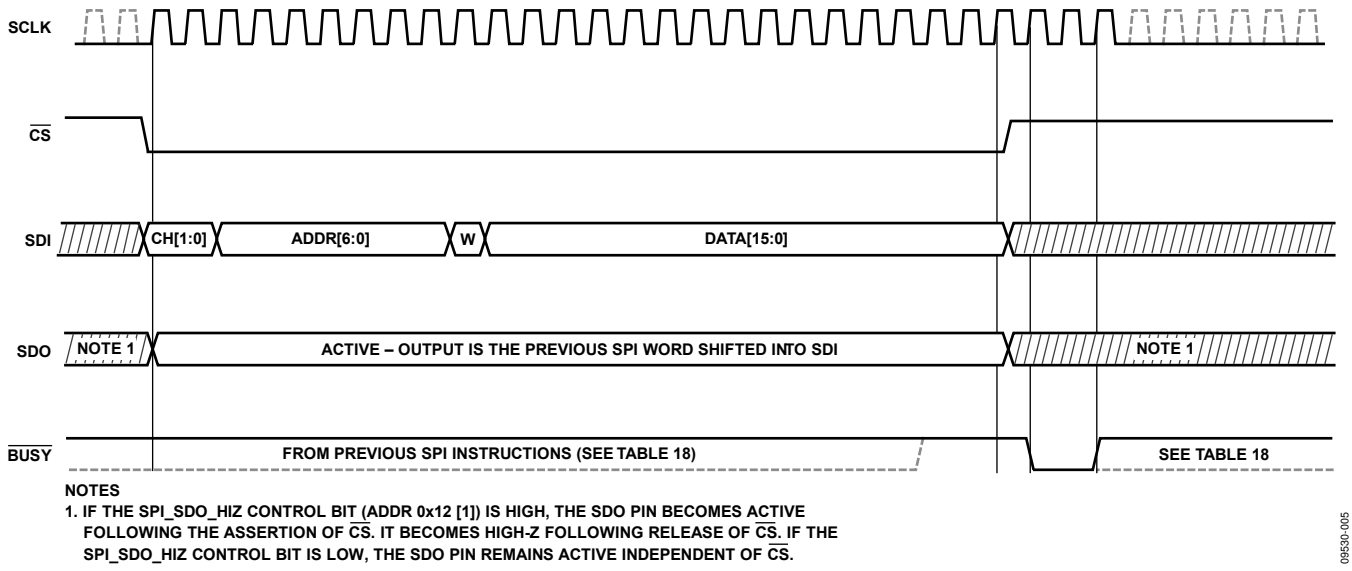


Figure 3. SPI Write Instruction

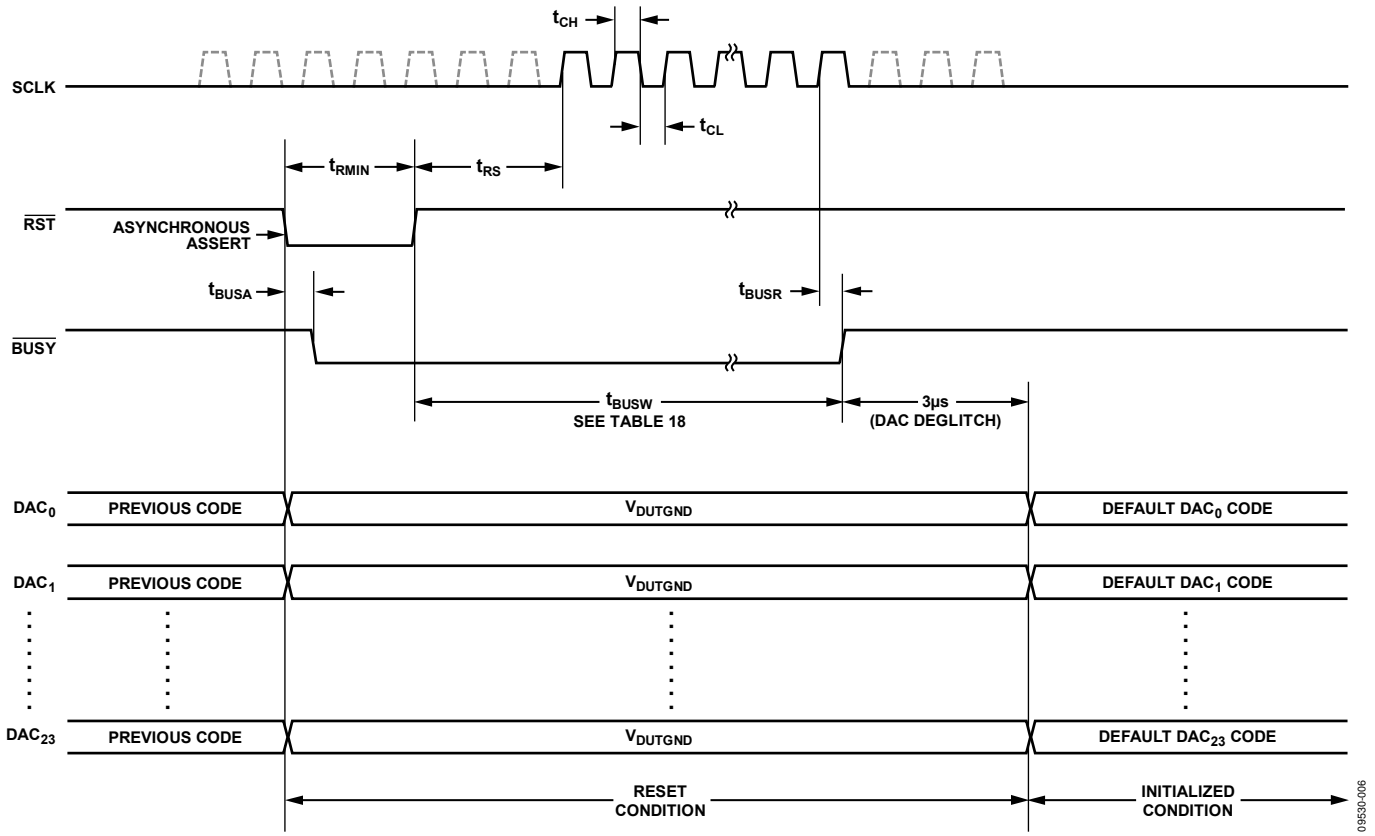


Figure 4. SPI Detailed Hardware Reset Timing Diagram

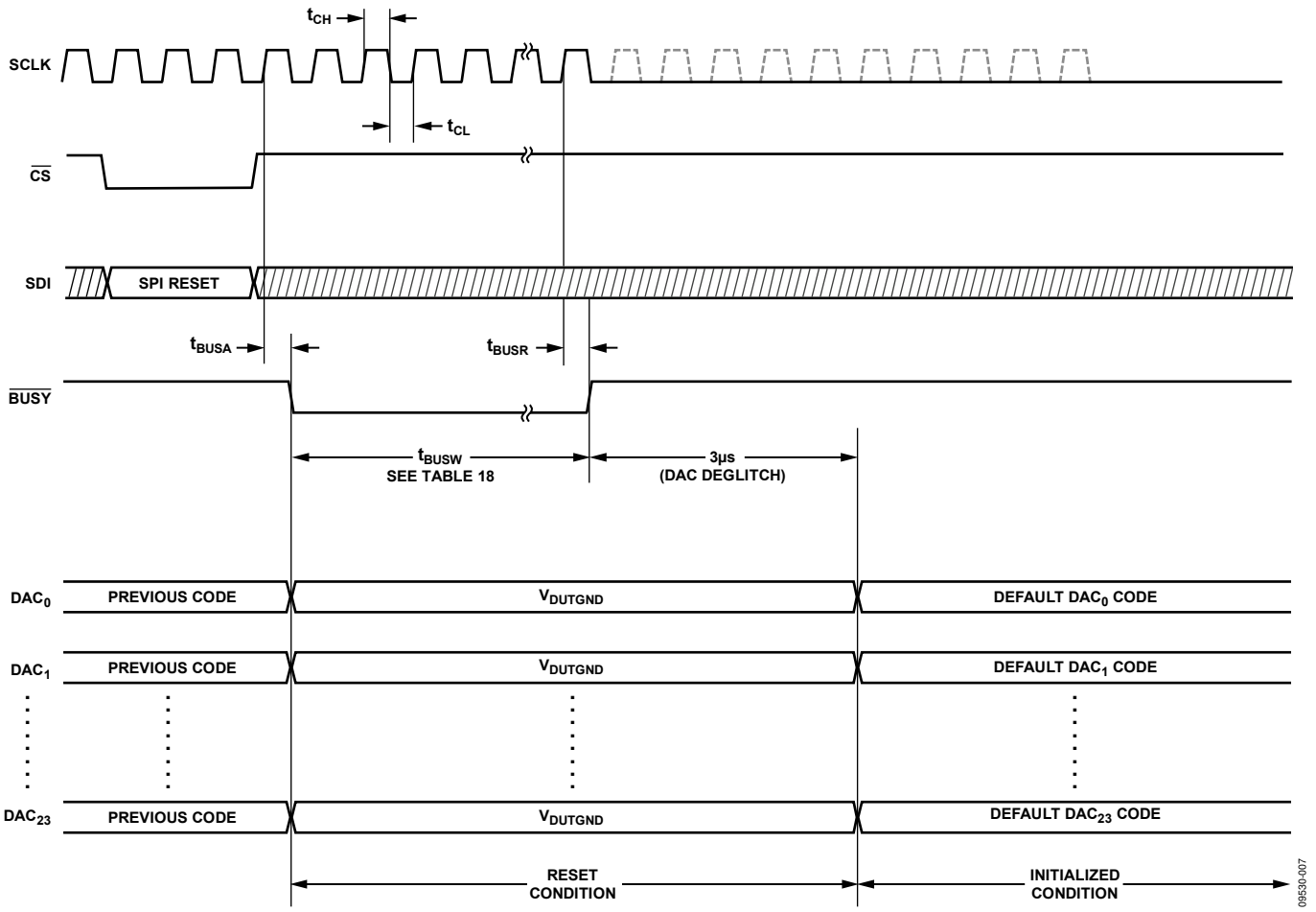
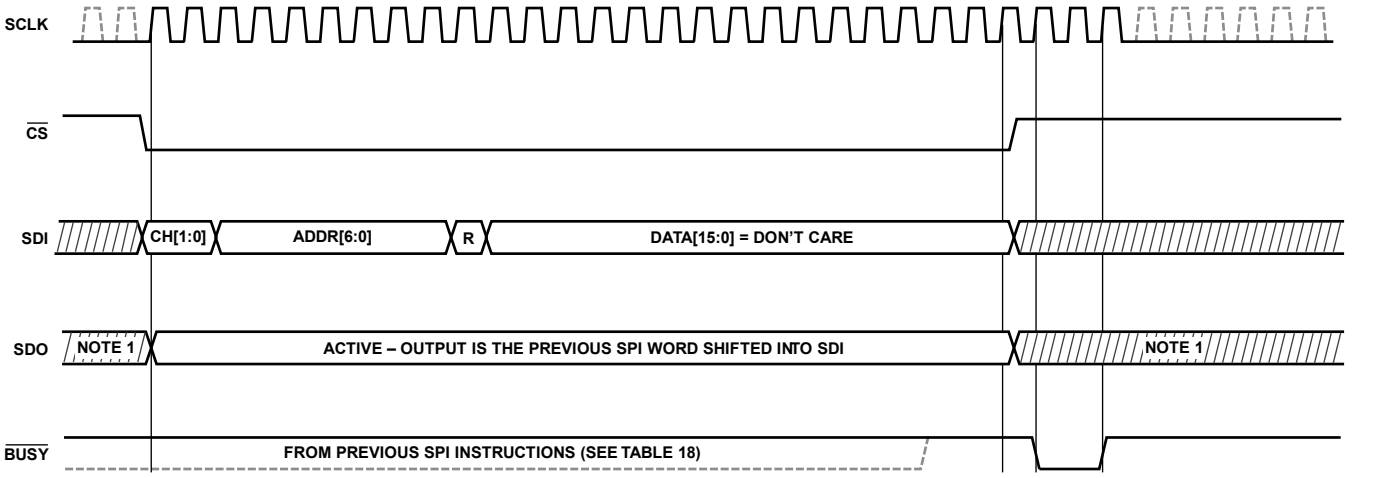
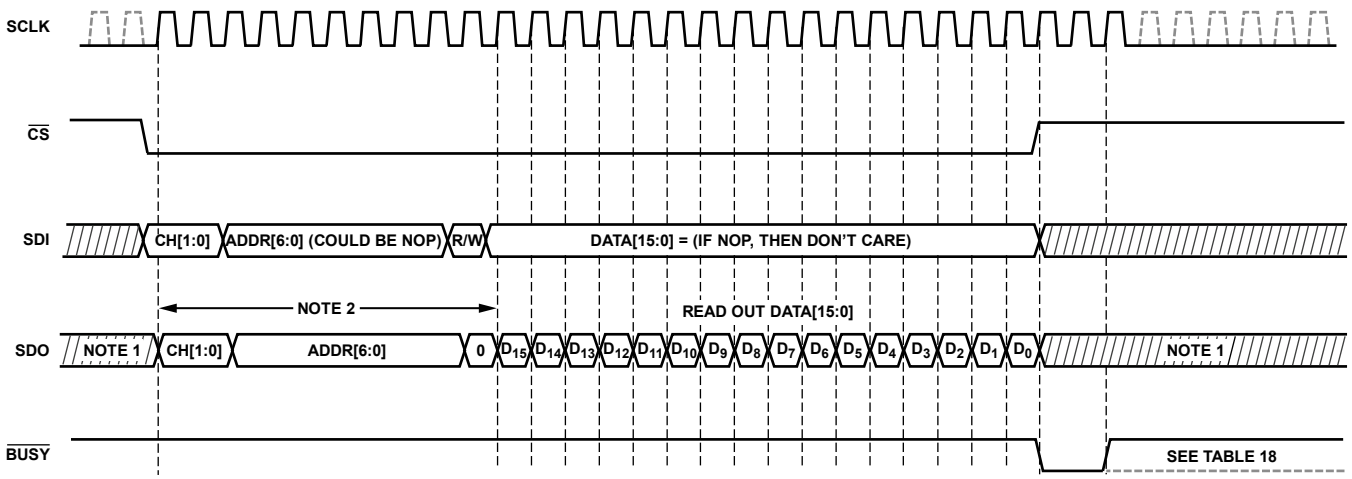


Figure 5. SPI Detailed Software Reset Timing Diagram



NOTES
1. IF THE SPI_SDO_HIZ CONTROL BIT (ADDR 0x12 [1]) IS HIGH, THE SDO PIN BECOMES ACTIVE FOLLOWING THE ASSERTION OF CS. IT BECOMES HIGH-Z FOLLOWING RELEASE OF CS. IF THE SPI_SDO_HIZ CONTROL BIT IS LOW, THE SDO PIN ALWAYS REMAINS ACTIVE INDEPENDENT OF CS.

Figure 6. SPI Read Request Instruction (Prior to Readout)



NOTES
1. IF THE SPI_SDO_HIZ CONTROL BIT (ADDR 0x12 [1]) IS HIGH, THE SDO PIN BECOMES ACTIVE FOLLOWING THE ASSERTION OF CS. IT BECOMES HIGH-Z FOLLOWING RELEASE OF CS. IF THE SPI_SDO_HIZ CONTROL BIT IS LOW, THE SDO PIN REMAINS ACTIVE INDEPENDENT OF CS.
2. THE FIRST 10 BITS OF SDO FOLLOWING A READ REQUEST ECHO ADDRESS AND CHANNEL BITS OF THE PRECEDING REQUEST. THE R/W BIT POSITION IS SET LOW. THE FOLLOWING 16 BITS CONTAIN DATA FROM THE REQUESTED ADDRESS AND CHANNEL.

09530-069

Figure 7. SPI Readout Instruction (Subsequent to Read Request)