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1.25 GHz Dual Integrated DCL with PPMU, Level Setting DACs, and On-Chip Calibration Registers

Data Sheet

ADATE320

FEATURES

- 1.25 GHz, 2.5 Gbps data rate
- 3-level driver with high-Z and reflection clamps
- Window and differential comparators
- ±25 mA active load
- Per pin parametric measurement unit (PMU) with a −1.5 V to +4.5 V range
- Low leakage mode (typically <5 nA)
- Integrated 16-bit DACs with offset and gain correction
- 1.2 W power dissipation per channel (ADATE320)
- 1.3 W power dissipation per channel (ADATE320-1)
- Driver
  - Voltage range: −1.5 V to +4.5 V
  - Precision trimmed termination: 50.0 Ω
  - Unterminated swing: 50 mV minimum to 6.0 V maximum
  - 400 ps minimum pulse width, 1.0 V programmed swing
  - 25 ps deterministic jitter
- Comparator
  - Differential and single-ended window modes
  - 100 ps equivalent input rise/fall time (ERT/EFT)
  - 250 mV current mode logic (CML) outputs (ADATE320)
  - 400 mV CML outputs (ADATE320-1)
- Load
- Per pin PMU (PPMU)
  - Force voltage/compliance range: −1.5 V to +4.5 V
  - 5 current ranges
    - ±40 mA, ±1 mA, ±100 µA, ±10 µA, ±2 µA
  - Dedicated go/no-go comparators
- DC levels
  - Fully integrated and dedicated 16-bit DACs
  - On-chip gain and offset calibration registers with automatic add/multiply function
- 84-lead, 10 mm × 10 mm LFCSP (0.4 mm pitch)

APPLICATIONS

- Automatic test equipment (ATE)
- Semiconductor/board test systems
- Instrumentation and characterization equipment

GENERAL DESCRIPTION

The ADATE320 is a complete, single-chip ATE solution that performs the pin electronics functions of a driver, comparator, and active load (DCL), and a four quadrant per pin parametric measurement unit (PPMU). Dedicated 16-bit digital-to-analog converters (DACs) with on-chip calibration registers provide all the necessary dc levels for operation of the device.

The driver features three active modes: high, low, and terminate, as well as a high impedance inhibit state. The inhibit state, in conjunction with the integrated dynamic clamps, facilitates significant attenuation of transmission line reflections when the driver is not actively terminating the line. The open-circuit drive capability is −1.5 V to +4.5 V to accommodate a standard range of ATE and instrumentation applications.

The ADATE320 can be used as a dual, single-ended pin electronics channel or as a single differential channel. In addition to per channel high speed window comparators, the ADATE320 provides a programmable threshold differential comparator for differential ATE applications.

All dc levels for DCL and PPMU functions are generated by dedicated, on-chip, 16-bit DACs. To facilitate the programming of accurate levels, the ADATE320 includes an integrated calibration function to correct for the gain and offset errors of each functional block. Correction coefficients can be stored on chip, and any values written to the DACs adjust automatically using the appropriate correction factors.

The ADATE320 uses a serial programmable interface (SPI) bus to program all functional blocks, DACs, and on-chip calibration constants. It also has an on-chip temperature sensor and overvoltage/undervoltage fault clamps that monitor and report the device temperature and any output pin or transient PPMU voltage faults that may occur during operation.

The ADATE320 is available in two options. The standard option has high speed comparator outputs with 250 mV output swing. The ADATE320-1 has 400 mV output swing. See the Ordering Guide for more information.

Rev. B

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ADATE320* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- ADATE320: 1.25 GHz Dual Integrated DCL with PPMU, Level Setting DACs, and On-Chip Calibration Registers Data Sheet

DESIGN RESOURCES

- ADATE320 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADATE320 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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10/2015—Revision A: Initial Version

FUNCTIONAL BLOCK DIAGRAM

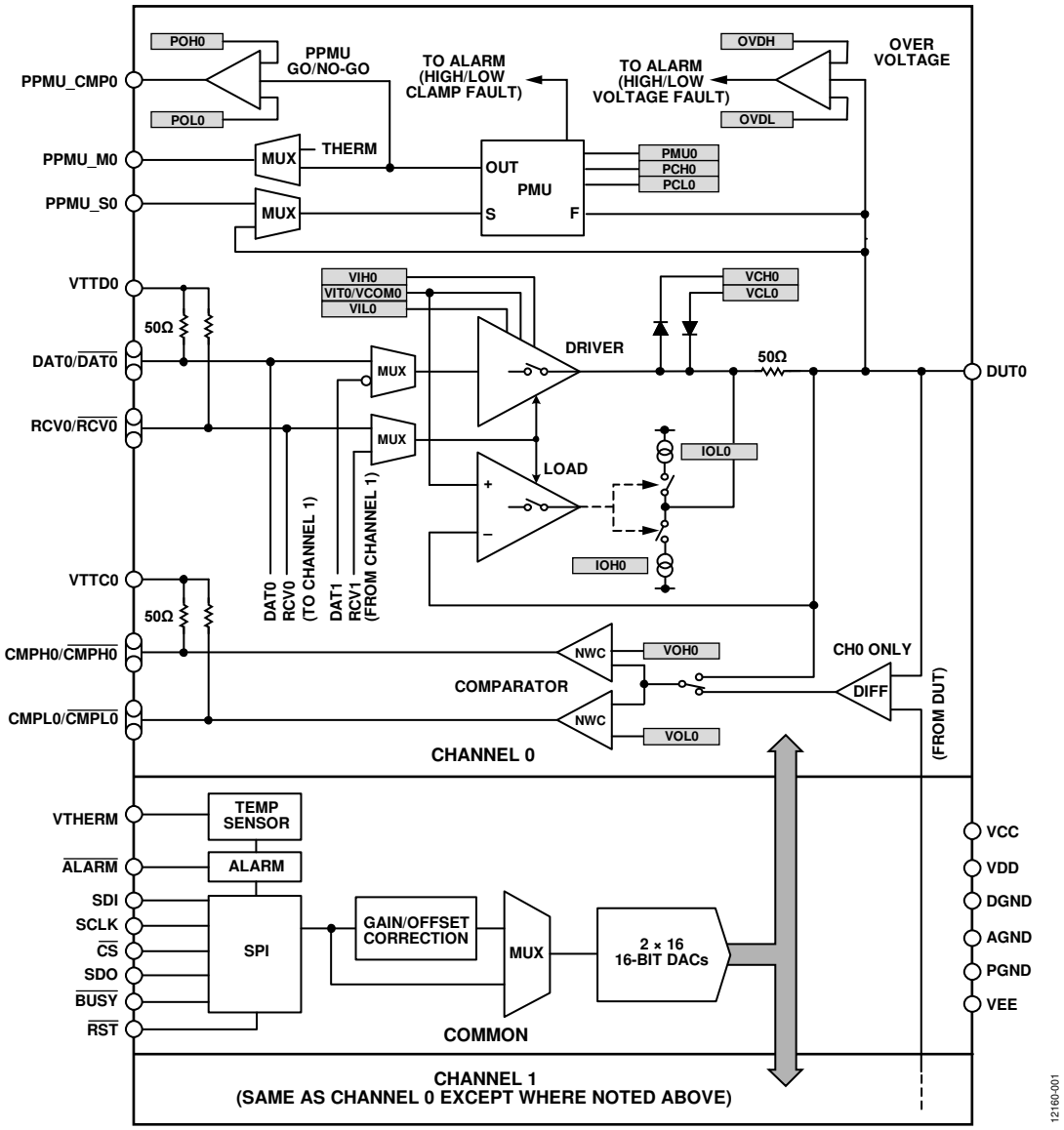


Figure 1.

SPECIFICATIONS

V_{CC} = 8.0 V, V_{DD} = 1.8 V, V_{EE} = −5.0 V, V_{TTCx} = V_{TTDx} = 1.2 V, V_{REF} = 2.500 V, V_{REFGND} = 0.000 V. All default test conditions are as defined in Table 30. All specified values are at T_J = 60°C, where T_J corresponds to the typical internal temperature sensor reading (VTHERM pin), unless otherwise noted. Temperature coefficients are measured around T_J = 40°C, 60°C, 80°C, and 100°C. Typical values are based on the statistical mean of the design, simulation analyses, and/or limited bench evaluation data. Typical values are neither tested nor guaranteed. Test level codes are defined in the Explanation of Test Levels section.

ELECTRICAL SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DUTx PIN CHARACTERISTICS						
Output Leakage Current						
DCL Disable						
PPMU Range E	−10.0	+5.0	+10.0	nA	P	−1.5 V < V_{DUTx} < +4.5 V, PPMU and DCL disabled, PPMU Range E, VCLx = −2.5 V, VCHx = +7.5 V
PPMU Range A to Range D		5.0		nA	C_T	−1.5 V < V_{DUTx} < +4.5 V, PPMU and DCL disabled, PPMU Range A, Range B, Range C, and Range D, VCLx = −2.5 V, VCHx = +7.5 V
Driver High-Z Mode	−0.4		+0.4	µA	P	−1.5 V < V_{DUTx} < +4.5 V, PPMU disabled and DCL enabled, RCV active, VCLx = −2.5 V, VCHx = +7.5 V
Capacitance		0.4		pF	S	Drive VITx = 0.0 V
Voltage Range	−1.5		+4.5	V	D	
POWER SUPPLIES						Power measured with the DUTx pin high-Z, 10 K to 0.0 V
Positive DCL Supply, V_{CC}	7.6	8.0	8.4	V	D	Defines dc power supply rejection (PSR) conditions
Negative DCL Supply, V_{EE}	−5.25	−5.0	−4.75	V	D	Defines dc PSR conditions
Digital Supply, V_{DD}	1.7	1.8	1.9	V	D	
Comparator Termination, V_{TTCx}	0.5	1.2	1.8	V	D	VTTC0 is not electrically connected to VTTC1
Driver Termination, V_{TTDx}	0.0	1.2	1.8	V	D	VTTD0 is not electrically connected to VTTD1
Positive DCL Supply Current, I_{CC}						Load and PPMU power-down
ADATE320	145	169	185	mA	P	
ADATE320-1	145	169	185	mA	P	
Negative DCL Supply Current, I_{EE}						Load and PPMU power-down
ADATE320	190	222	235	mA	P	
ADATE320-1	220	247	265	mA	P	
Digital Core Supply Current, I_{DD}	−125	+10	+125	µA	P	Quiescent (SPI is static)
Comparator Termination Supply Current, V_{TTCx}						0.5 V ≤ V_{TTCx} ≤ 1.8 V
ADATE320		41		mA	C_T	
ADATE320-1		66		mA	C_T	
Driver Termination Supply Current, V_{TTDx}		0		mA	C_T	0.0 V ≤ V_{TTDx} ≤ 1.8 V, (DATx + $\overline{DATx}$)/2 = (RCVx + $\overline{RCVx}$)/2 = V_{TTDx}
Total Power Dissipation						Load and PPMU power-down
ADATE320	2.10	2.52	2.75	W	P	
ADATE320-1	2.25	2.66	2.90	W	P	

DRIVER SPECIFICATIONS

VIH − VIL ≥ 100 mV to meet dc and ac performance specifications.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						
High Speed Differential Input Characteristics						
High Speed Input Termination Resistance: DATx/$\overline{\text{DATx}}$, RCVx/$\overline{\text{RCVx}}$	48	50	52	Ω	P	Impedance between VTTDx and respective DATx and RCVx pins; force 4 mA into each pin, measure voltage from VTTDx; calculate resistance (ΔV/ΔI)
Input Voltage Range: DATx/$\overline{\text{DATx}}$, RCVx/$\overline{\text{RCVx}}$	0.0		1.8	V	P_F	
Input Voltage Differential	0.2	0.4	1.0	V	P_F	|DATx − $\overline{\text{DATx}}$|, |RCVx − $\overline{\text{RCVx}}$|
Output Characteristics						
Output Range						
High, VIH	−1.4		+4.5	V	D	
Low, VIL	−1.5		+4.4	V	D	
Output Term Range, VIT	−1.5		+4.5	V	D	
Functional Amplitude (VIH − VIL)	0.05		6.0	V	D	
DC Output Current Limit						
Source	75		120	mA	P	Drive high, VIH = 4.5 V, V_{DUTx} = −2.0 V, measure current
Sink	−120		−75	mA	P	Drive low, VIL = −1.5 V, V_{DUTx} = 5.0 V, measure current
Output Resistance, ±40 mA	46	48.5	52	Ω	P	$\Delta V_{DUTx}/\Delta I_{DUTx}$; source: VIHx = 3.0 V, I_{DUTx} = 1 mA, 40 mA; sink: VIL = 0.0 V, I_{DUTx} = −1 mA, −40 mA
DC ACCURACY						VIH tests with VIL = −2.5 V, VIT = −2.5 V; VIL tests with VIH = 7.5 V, VIT = 7.5 V; VIT tests with VIL = −2.5 V, VIH = 7.5 V, unless otherwise noted within this parameter
VIH, VIL, VIT						
Offset Error	−500		+500	mV	P	Measured at DAC Code 0x4000 (0.0 V), uncalibrated
Offset Temperature Coefficient (TC)		±200		µV/°C	C_T	
Gain	1.0		1.1	V/V	P	Gain derived from measurement at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V); based on an ideal DAC transfer function (see Table 24)
Gain TC		±50		ppm/°C	C_T	
Differential Nonlinearity (DNL)		±250		µV	C_T	After two-point gain/offset calibration; calibration points at 0x4000 (0.0 V) output; 0x8CCC (3.0 V); measured over full specified output range
Integral Nonlinearity (INL) Focused Range	−5		+5	mV	P	After two-point gain/offset calibration; calibration points at 0x4000 (0.0 V) and 0x8CCC (3.0 V); measured over −0.5 V to +3.5 V output range
INL Full Range	−20		+20	mV	P	After two-point gain/offset calibration; calibration points at 0x4000 (0.0 V) and 0x8CCC (3.0 V); measured over full specified output range
Resolution		153		µV	D	
DUTGND Voltage Accuracy	−5	±1	+5	mV	P	Over ±0.1 V range; measured over −0.5 V to +3.5 V focused driver output range
DC Levels Interaction						DC interaction on VIL, VIH, and VIT output levels while other driver DAC levels are varied
VIH vs. VIL		±1.0		mV	C_T	Monitor interaction on VIH = +4.5 V; sweep VIL = −1.5 V to +4.4 V, VIT = +1.0 V
VIH vs. VIT		±1.0		mV	C_T	Monitor interaction on VIH = +4.5 V; sweep VIT = −1.5 V to +4.5 V, VIL = 0.0 V
VIL vs. VIH		±1.0		mV	C_T	Monitor interaction on VIL = −1.5 V; sweep VIH = −1.4 V to +4.5 V, VIT = +1.0 V

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
VIL vs. VIT		±1.0		mV	C_T	Monitor interaction on VIL = −1.5 V; sweep VIT = −1.5 V to +4.5 V, VIH = +2.0 V
VIT vs. VIH		±2.0		mV	C_T	Monitor interaction on VIT = 1.0 V; sweep VIH = −1.4 V to +4.5 V, VIL = −1.5 V
VIT vs. VIL		±2.0		mV	C_T	Monitor interaction on VIT = 1.0 V; sweep VIL = −1.5 V to +4.4 V, VIH = +4.5 V
Overall Voltage Accuracy Focused Range		±5		mV	C_T	VIH − VIL ≥ 100 mV; sum of INL, dc interaction, DUTGND and TC errors over ±5°C, after calibration
VIH, VIL, VIT DC PSR		+15		mV/V	C_T	Measured at calibration points, see Table 1 for power supply ranges
AC SPECIFICATIONS						All ac specifications performed after dc calibration
Rise/Fall Times						Toggle DATx, VIL = 0.0 V, terminated
0.2 V Programmed Swing						
t_{RISE}		150		ps	C_B	20% to 80%, VIH = 0.2 V
t_{FALL}		170		ps	C_B	20% to 80%, VIH = 0.2 V
0.5 V Programmed Swing						
t_{RISE}		150		ps	C_B	20% to 80%, VIH = 0.5 V
t_{FALL}		170		ps	C_B	20% to 80%, VIH = 0.5 V
1.0 V Programmed Swing						
t_{RISE}		150		ps	C_B	20% to 80%, VIH = 1.0 V
t_{FALL}		170		ps	C_B	20% to 80%, VIH = 1.0 V
2.0 V Programmed Swing						
t_{RISE}	120	160	230	ps	P	20% to 80%, VIH = 2.0 V
t_{FALL}	120	180	230	ps	P	20% to 80%, VIH = 2.0 V
4.0 V Programmed Swing						
t_{RISE}		320		ps	C_B	10% to 90%, VIH = 4.0 V, unterminated
t_{FALL}		320		ps	C_B	10% to 90%, VIH = 4.0 V, unterminated
t_{RISE} to t_{FALL} Mismatch		−20		ps	C_B	$t_{RISE} - t_{FALL}$ (20% to 80%) within one channel, VIH = 2.0 V, VIL = 0.0 V, terminated
Trailing Edge Timing Error						Toggle DATx
Programmed Swing						VIL = 0.0 V, terminated, 400 ps ≤ pulse width (PW) ≤ 10 ns
0.2 V		±15		ps	C_B	VIH = 0.2 V
0.5 V		±15		ps	C_B	VIH = 0.5 V
1.0 V		±15		ps	C_B	VIH = 1.0 V
2.0 V		±15		ps	C_B	VIH = 2.0 V
Maximum Toggle Rate						Toggle DATx
Programmed Swing						VIL = 0.0 V, terminated ≤10% amplitude loss
0.2 V		2.8		Gbps	C_B	VIH = 0.2 V
0.5 V		3.2		Gbps	C_B	VIH = 0.5 V
1.0 V		3.2		Gbps	C_B	VIH = 1.0 V
2.0 V		2.8		Gbps	C_B	VIH = 2.0 V
Dynamic Performance						Toggle DATx, drive VIL to/from VIH
Propagation Delay						VIH = 2.0 V, VIL = 0.0 V, terminated
Time		750		ps	C_B	
TC		2		ps/°C	C_T	
Delay Matching						VIH = 2.0 V, VIL = 0.0 V, terminated
Edge to Edge		10		ps	C_B	$t_{LH0} - t_{HL0}$; $t_{LH1} - t_{HL1}$
Channel to Channel		35		ps	C_B	$t_{LH0} - t_{LH1}$; $t_{HL0} - t_{HL1}$
Delay Change vs. Duty Cycle		±7		ps	C_B	VIH = 2.0 V, VIL = 0.0 V, terminated, 1 MHz, 5% to 95%
Overshoot and Undershoot		50		mV	C_B	VIH = 2.0 V, VIL = 0.0 V, terminated, minimum driver CLC
Settling Time (VIH to VIL)						Toggle DATx
To Within 3% of Final Value		1		ns	C_B	VIH = 2.0 V, VIL = 0.0 V, from 50% crossing, terminated
To Within 1% of Final Value		10		ns	C_B	VIH = 2.0 V, VIL = 0.0 V, from 50% crossing, terminated

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
Dynamic Performance						
Drive Active to/from VIT						Toggle RCVx, VIH = 2.0 V, VIT = 1.0 V, VIL = 0.0 V, terminated
Transition Time						20% to 80%
Active to VIT		200		ps	C_B	
VIT to Active		170		ps	C_B	
Propagation Delay		1.0		ns	C_B	
TC		2		ps/°C	C_T	
Drive Active to/from Inhibit						Toggle RCVx, VIH = 1.0 V, VIL = −1.0 V, terminated
Transition Time						20% to 80%
Inhibit to Active		250		ps	C_B	
Active to Inhibit		850		ps	C_B	
Propagation Delay						
Inhibit to VIH		2.1		ns	C_B	
Inhibit to VIL		2.5		ns	C_B	
Matching Inhibit to VIL vs. Inhibit to VIH		0.4		ns	C_B	
VIH to Inhibit		2.5		ns	C_B	
VIL to Inhibit		2.1		ns	C_B	
Input/Output Spike		125		mV p-p	C_B	VIH = 0.0 V, VIL = 0.0 V, terminated, toggle RCVx
Cable Loss Compensation (CLC)						VIH = 2.0 V, VIL = 0.0 V, terminated
Amplitude		20		%	C_B	Maximum CLC setting
Resolution		3		Bits	D	
Time Constant 1		400		ps	S	Maximum CLC setting
Time Constant 2		1.5		ns	S	Maximum CLC setting

REFLECTION CLAMP SPECIFICATIONS

Clamp accuracy specifications apply only when VCHx − VCLx > 0.8 V.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
VCH						
Functional Range	−0.5		+5.0	V	D	
Offset Error	−300		+300	mV	P	Driver high-Z, sinking 1 mA, measured at DAC Code 0x4000 (0.0 V), uncalibrated
Offset TC		±0.25		mV/°C	C_T	
Gain	1.0		1.1	V/V	P	Driver high-Z, sinking 1 mA, gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V), based on an ideal DAC transfer function (see Table 24)
Gain TC		±25		ppm/°C	C_T	
Resolution		153		µV	D	
DNL		±250		µV	C_T	Driver high-Z, sinking 1 mA, after two-point gain/offset calibration; calibration points at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V), measured over the functional range
INL	−20		+20	mV	P	Driver high-Z, sinking 1 mA, after two-point gain/offset calibration; calibration points at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V), measured over the functional range
VCL						
Functional Range	−2.0		+3.5	V	D	
Offset Error	−300		+300	mV	P	Driver high-Z, sourcing 1 mA, measured at DAC Code 0x4000 (0.0 V), uncalibrated
Offset TC		±0.25		mV/°C	C_T	

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
Gain	1.0		1.1	V/V	P	Drive high-Z, sourcing 1 mA, gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V), based on an ideal DAC transfer function (see Table 24)
Gain TC		±25		ppm/°C	C_T	
Resolution		153		µV	D	
DNL		±250		µV	C_T	Drive high-Z, sourcing 1 mA, after two-point gain/offset calibration; calibration points at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V), measured over the functional range
INL	−20		+20	mV	P	Drive high-Z, sourcing 1 mA, after two-point gain/offset calibration; calibration points at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V), measured over the functional range
DC CLAMP CURRENT LIMIT						Drive high-Z
VCHx	−105		−60	mA	P	VCHx = −1.0 V, VCLx = −2.0 V, V_{DUTx} = 4.5 V
VCLx	+60		+105	mA	P	VCHx = 5.0 V, VCLx = 4.0 V, V_{DUTx} = −1.5 V
DUTGND VOLTAGE ACCURACY	−10	±2	+10	mV	P	Over ±0.1 V range, measured at end points of VCHx and VCLx functional range

NORMAL WINDOW COMPARATOR (NWC) SPECIFICATIONS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						
Input Voltage Range	−1.5		+4.5	V	D	
Differential Voltage Range	±0.1		±6.0	V	D	
Input Offset Voltage	−250		+250	mV	P	Measured at DAC Code 0x4000 (0.0 V); uncalibrated
Input Offset Voltage TC		±150		µV/°C	C_T	
Gain	1.0		1.1	V/V	P	Gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V); based on an ideal DAC transfer function (see Table 24)
Gain TC		±10		ppm/°C	C_T	
Threshold Resolution		153		µV	D	
Threshold DNL		±0.25		mV	C_T	Measured over −1.5 V to +4.5 V functional range after two-point gain/offset calibration; calibration points at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
Threshold INL						After two-point gain/offset calibration; calibration points at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
Focused Range	−5		+5	mV	P	Measured over −0.5 V to +3.5 V range
Full Range	−7		+7	mV	P	Measured over −1.5 V to +4.5 V range
DUTGND Voltage Accuracy	−5	±1	+5	mV	P	Over ±0.1 V range; measured over −0.5 V to +3.5 V focused NWC input range
Uncertainty Band		10		mV	C_B	V_{DUTx} = 0.0 V, sweep comparator threshold to determine the uncertainty band
Programmable Hysteresis		100		mV	C_B	
Hysteresis Resolution		4		Bits	D	
DC PSR		±5		mV/V	C_T	Measured at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V) calibration points
Digital Output Characteristics						
Internal Pull-up Resistance to Comparator, VTTCx	46	50	54	Ω	P	Source 1 mA and 10 mA from the output pin in high state, measure ΔV to calculate resistance; R = ΔV/9 mA; repeat for all output pins

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
Common-Mode Voltage						Measured relative to V_{TTCx}, with 100 Ω differential termination
ADATE320		−250		mV	C_T	
ADATE320-1		−400		mV	C_T	
Differential Mode Voltage						Measured differentially
100 Ω Differential Termination						
ADATE320		250		mV	C_T	
ADATE320-1		400		mV	C_T	
No External Termination						
ADATE320	450	500	550	mV	P	
ADATE320-1	700	800	900	mV	P	
AC SPECIFICATIONS						Unless otherwise specified, all ac tests are performed after dc levels calibration; input transition time: 50 ps 20% to 80%; outputs terminated 50 Ω to 0.0 V; comparator CLC set to ¼ scale (010)
Rise/Fall Times, 20% to 80%		100		ps	C_B	Measured with 50 Ω to 0.0 V
Propagation Delay		580		ps	C_B	V_{DUTx} = 0.0 V to 1.0 V swing, drive term mode, VIT = 0.0 V, comparator threshold = 0.5 V
Propagation Delay TC		1		ps/°C	C_T	V_{DUTx} = 0.0 V to 1.0 V swing, drive term mode, VIT = 0.0 V, comparator threshold = 0.5 V
Propagation Delay Matching High Transition to Low Transition		10		ps	C_B	V_{DUTx} = 0.0 V to 1.0 V swing, drive term mode, VIT = 0.0 V, comparator threshold = 0.5 V
Propagation Delay Matching High to Low Comparator		10		ps	C_B	V_{DUTx} = 0.0 V to 1.0 V swing, drive term mode, VIT = 0.0 V, comparator threshold = 0.5 V
Propagation Delay Dispersion						Drive term mode, VIT = 0.0 V
Slew Rate: 400 ps vs. 1.0 ns (20% to 80%)		20		ps	C_B	V_{DUTx} = 0.0 V to 0.5 V swing, comparator threshold = 0.25 V
Overdrive: 250 mV vs. 1.0 V		25		ps	C_B	For 250 mV: V_{DUTx}: 0.0 V to 0.50 V swing; for 1.0 V: V_{DUTx}: 0.0 V to 1.25 V swing, comparator threshold = 0.25 V
1.0 V Pulse Width: 0.4 ns, 0.5 ns, 1 ns, 5 ns, 10 ns		25		ps	C_B	V_{DUTx} = 0.0 V to 1.0 V swing, 32 MHz, comparator threshold = 0.5 V
0.5 V Pulse Width: 0.4 ns, 0.5 ns, 1 ns, 5 ns, 10 ns		25		ps	C_B	V_{DUTx} = 0.0 V to 0.5 V swing, 32 MHz, comparator threshold = 0.25 V
Duty Cycle: 5% to 95%		10		ps	C_B	V_{DUTx} = 0.0 V to 1.0 V swing, 32 MHz, comparator threshold = 0.5 V
Minimum Detectable Pulse Width		200		ps	C_B	V_{DUTx} = 0.0 V to 1.0 V swing, 32 MHz, greater than 50% output differential amplitude
Input Equivalent Rise/Fall Time, 1.0 V, Terminated		110		ps	C_B	V_{DUTx} = 0.0 V to 1.0 V swing, drive term mode, VIT = 0.0 V, CLC = 010, measured from digitized plot, 20% to 80% transition time of digitized plot is root-sum square (RSS) of input equivalent rise/fall and 50 ps input stimulus
Input Equivalent Rise/Fall Time, 2.0 V, Unterminated		500		ps	C_B	V_{DUTx} = 0.0 V to 2.0 V swing, drive high-Z, measured from digitized plot, 20% to 80% transition time of digitized plot is root-sum square (RSS) of input equivalent rise/fall and 50 ps input stimulus
Cable Loss Compensation (CLC)						V_{DUTx} = 0.0 V to 1.0 V swing, drive term mode, VIT = 0.0 V, maximum CLC setting
CLC Amplitude		20		%	C_B	
CLC Resolution		3		Bits	D	
CLC Time Constant 1		280		ps	S	
CLC Time Constant 2		4.8		ns	S	

DIFFERENTIAL MODE COMPARATOR (DMC) SPECIFICATIONS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						VOHx tests at VOLx = −1.5 V, VOLx tests at VOHx = 1.5 V
Input Voltage Range	−1.5		+4.5	V	D	
Functional Differential Range	±0.05		±1.1	V	D	
Maximum Differential Input			±6.0	V	D	
Input Offset Voltage	−250		+250	mV	P	Offset interpolated from measurements at DAC Code 0x2666 (−1.0 V) and DAC Code 0x5999 (1.0 V), with V_{CM} = 0.0 V
Input Offset Voltage TC		±150		µV/°C	C_T	
Gain	1.0		1.1	V/V	P	Gain derived from measurements at DAC Code 0x2666 (−1.0 V) and DAC Code 0x5999 (1.0 V); based on an ideal DAC transfer function (see Table 24)
Gain TC		±40		ppm/°C	C_T	
VOHx, VOLx Resolution		153		µV	D	
VOHx, VOLx DNL		±250		µV	C_T	After two-point gain/offset calibration; V_{CM} = 0.0 V; calibration points at DAC Code 0x2666 (−1.0 V) and DAC Code 0x5999 (1.0 V)
VOHx, VOLx INL	−8		+8	mV	P	After two-point gain/offset calibration; V_{CM} = 0.0 V; calibration points DAC Code 0x2666 (−1.0 V) and DAC Code 0x5999 (1.0 V), measured over VOHx/VOLx range of −1.1 V to +1.1 V
Uncertainty Band		11		mV	C_B	V_{DUTx} = 0.0 V, sweep comparator threshold to determine the uncertainty band
Programmable Hysteresis		200		mV	C_B	
Hysteresis Resolution		4		Bits	D	
Common-Mode Rejection Ratio (CMRR)	−1.0		+1.0	mV/V	P	ΔOffset measured at V_{CM} = −1.5 V and +4.5 V, V_{DM} = 0.0 V
DC PSR		±5		mV/V	C_T	ΔOffset measured at V_{CM} = 0.0 V, V_{DM} = calibration points DAC Code 0x2666 (−1.0 V) and DAC Code 0x5999 (1.0 V)
AC SPECIFICATIONS						All ac tests are performed after dc levels calibration; input transition time = 50 ps 20% to 80%; outputs terminated 50 Ω to VTTCx, comparator CLC set to ¼ scale (010)
Propagation Delay		580		ps	C_B	V_{DUT0} = 0.0 V, V_{DUT1} = −0.5 V to +0.5 V swing, drive termination mode, VIT = 0.0 V, comparator threshold = 0.0 V, repeat with VDUTx inputs reversed
Propagation Delay TC		2		ps/°C	C_T	V_{DUT0} = 0.0 V, V_{DUT1} = −0.5 V to +0.5 V swing, drive termination mode, VIT = 0.0 V, comparator threshold = 0.0 V, repeat with VDUTx inputs reversed
Propagation Delay Matching High Transition to Low Transition		15		ps	C_B	V_{DUT0} = 0.0 V, V_{DUT1} = −0.5 V to +0.5 V swing, drive termination mode, VIT = 0.0 V, comparator threshold = 0.0 V, repeat with VDUTx inputs reversed
Propagation Delay Matching High to Low Comparator		15		ps	C_B	V_{DUT0} = 0.0 V, V_{DUT1} = −0.5 V to +0.5 V swing, drive termination mode, VIT = 0.0 V, comparator threshold = 0.0 V, repeat with VDUTx inputs reversed
Propagation Delay Dispersion						V_{DUT0} = 0.0 V, VIT = 0.0 V, drive termination mode, repeat with VDUTx inputs reversed
Slew Rate: 400 ps vs. 1 ns (20% to 80%)		30		ps	C_B	V_{DUT1} = −0.5 V to +0.5 V swing, comparator threshold = 0.0 V
Overdrive: 250 mV vs. 750 mV		25		ps	C_B	For 250 mV: V_{DUT1} = 0.0 V to 0.5 V swing; for 750 mV: V_{DUT1} = 0.0 V to 1.0 V swing, comparator threshold = −0.25 V, repeat with VDUTx inputs reversed with comparator threshold = +0.25 V
1.0 V Pulse Width: 0.7 ns, 1.0 ns, 5.0 ns, 10 ns		25		ps	C_B	V_{DUT1} = −0.5 V to +0.5 V swing, 32 MHz, comparator threshold = 0.0 V
0.5 V Pulse Width: 0.6 ns, 1.0 ns, 5.0 ns, 10 ns		25		ps	C_B	V_{DUT1} = −0.25 V to +0.25 V swing, 32 MHz, comparator threshold = 0.0 V

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
Duty Cycle: 5% to 95%		5		ps	C_B	V_{DUT1} = −0.5 V to +0.5 V swing, 32 MHz, comparator threshold = 0.0 V
Minimum Detectable Pulse Width		200		ps	C_B	V_{DUT0} = 0.0 V, V_{DUT1} = −0.5 V to +0.5 V swing, 32 MHz, drive term mode, VIT = 0.0 V, comparator threshold = 0.0 V, greater than 50% output differential amplitude, repeat with VDUTx inputs reversed
Input Equivalent Rise/Fall Time		110		ps	C_B	V_{DUT0} = 0.0 V, V_{DUT1} = −0.5 V to +0.5 V swing, drive term mode, VIT = 0.0 V, comparator threshold = 0.0 V, CLC = ¼ scale, measured from digitized plot, $t = \sqrt{(t_{CMP}^2 - t_{IN}^2)}$
Cable Loss Compensation (CLC)						V_{DUT0} = 0.0 V, V_{DUT1} = −0.8 V to +0.8 V swing, drive term mode, VIT = 0.0 V, comparator threshold = 0.0 V, comparator CLC set to maximum CLC setting, repeat with VDUTx inputs reversed
CLC Amplitude		20		%	C_B	
CLC Resolution		3		Bits	D	
CLC Time Constant 1		280		ps	S	
CLC Time Constant 2		4.8		ns	S	

ACTIVE LOAD SPECIFICATIONS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						Load in active on state, RCVx active
Input Characteristics						
Active Load Commutation Voltage (VCOMx) Range	−1.5		+4.5	V	D	IOHx = IOLx = 1 mA, VDUTx open circuit
VCOMx Offset	−200		+200	mV	P	Measured at DAC Code 0x4000 (0.0 V), uncalibrated
VCOMx Offset TC		±100		µV/°C	C_T	
VCOMx Gain	1.0		1.1	V/V	P	Gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
VCOMx Gain TC		±20		ppm/°C	C_T	
VCOMx Resolution		153		µV	D	
VCOMx DNL		±250		µV	C_T	IOHx = IOLx = 12.5 mA, after two-point gain/offset calibration; measured over VCOMx range −1.5 V to +4.5 V; calibration points DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
VCOMx INL						IOHx = IOLx = 12.5 mA; after two-point gain/offset calibration; calibration points DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
Focused Range	−5		+5	mV	P	Measured over VCOMx range of −0.5 V to +3.5 V
Full Range	−10		+10	mV	P	Measured over VCOMx range of −1.5 V to +4.5 V
DUTGND Voltage Accuracy	−5	±1	+5	mV	P	Over ±0.1 V range; measured over −0.5 V to +3.5 V focused VCOMx range
Output Characteristics						
Maximum Source Current (IOLx)	25			mA	D	$V_{DUTx} \leq$ 3.5 V (a compliance limit is set by a 50 Ω internal resistor as illustrated in Figure 142)
IOLx Offset	−600		+600	µA	P	IOHx = −2.5 mA, VCOMx = 1.5 V, V_{DUTx} = 0.0 V; offset extrapolated from measurements at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA)
IOLx Offset TC		±1		µA/°C	C_T	
IOLx Gain Error	0		+25	%	P	IOHx = −2.5 mA, VCOMx = 1.5 V, V_{DUTx} = 0.0 V; gain derived from measurements at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA); based on an ideal dc transfer function
IOLx Gain TC		±100		ppm/°C	C_T	

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
IOLx Resolution		763		nA	D	
IOLx DNL		±1.25		µA	C_T	IOHx = −2.5 mA, VCOMx = 1.5 V, V_{DUTx} = 0.0 V; after two-point gain/offset calibration; measured over IOLx range 0 mA to 25 mA; calibrated at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA)
IOLx INL	−100		+100	µA	P	IOHx = −2.5 mA, VCOM = 1.5 V, V_{DUTx} = 0.0 V, after two-point gain/offset calibration
IOLx 90% Commutation Voltage		0.25	0.4	V	P	IOHx = IOLx = 25 mA, VCOM = 2.0 V, measure IOLx reference at V_{DUTx} = −1.0 V, measure IOLx current at V_{DUTx} = 1.6 V, check > 90% of reference current
		0.1		V	C_T	IOHx = IOLx = 1 mA, VCOM = 2.0 V, measure IOLx reference at V_{DUTx} = −1.0 V, measure IOLx current at V_{DUTx} = 1.9 V, check > 90% of reference current
Maximum Sink Current (IOHx)	25			mA	D	$V_{DUTx} \geq$ −0.5 V (a compliance limit is set by a 50 Ω internal resistor as illustrated in Figure 142)
IOHx Offset	−600		+600	µA	P	IOLx = −2.5 mA, VCOM = 1.5 V, V_{DUTx} = 3.0 V, offset extrapolated from measurements at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA)
IOHx Offset TC		±1		µA/°C	C_T	
IOHx Gain Error	0		+25	%	P	IOLx = −2.5 mA, VCOM = 1.5 V, V_{DUTx} = 3.0 V, gain derived from measurements at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA); based on an ideal DAC transfer function
IOHx Gain TC		±100		ppm/°C	C_T	
IOHx Resolution		763		nA	D	
IOHx DNL		±1.25		µA	C_T	IOLx = −2.5 mA, VCOM = 1.5 V, V_{DUTx} = 3.0 V, after two-point gain/offset calibration; measured over IOHx range of 0 mA to 25 mA; calibrated at DAC Code 0x451F (1 mA) and DAC Code 0xA666 (20 mA)
IOHx INL	−100		+100	µA	P	IOLx = −2.5 mA, VCOM = 1.5 V, V_{DUTx} = 3.0 V, after two-point gain/offset calibration
IOHx 90% Commutation Voltage		0.25	0.4	V	P	IOHx = IOLx = 25 mA, VCOM = 2.0 V, measure IOHx reference at V_{DUTx} = 4.0 V, measure IOHx current at V_{DUTx} = 2.4 V, ensure > 90% of reference current
		0.1		V	C_T	IOHx = IOLx = 1 mA, VCOM = 2.0 V, measure IOHx reference at V_{DUTx} = 4.0 V, measure IOHx current at V_{DUTx} = 2.1 V_{DUTx}, ensure > 90% of reference current
AC SPECIFICATIONS						All ac measurements are performed after dc calibration unless noted, load active on
Dynamic Performance						Toggle RCVx; DUTx terminated 50 Ω to 0.0 V; IOLx = IOHx = 20 mA, VIH = VIL = 0.0 V; VCOM = +1.5 V for IOLx and −1.5 V for IOHx
Propagation Delay, Load Active On to Load Active Off		1.7		ns	C_B	Measured from zero crossing of RCVx − $\overline{\text{RCVx}}$ to 50% of final output value; repeat for drive low and drive high
Propagation Delay, Load Active Off to Load Active On		2.9		ns	C_B	Measured from zero crossing of RCVx − $\overline{\text{RCVx}}$ to 50% of final output value; repeat for drive low and drive high
Propagation Delay Matching		1.2		ns	C_B	Active on vs. active off; repeat for drive low and drive high
Load Spike		140		mV	C_B	Repeat for drive low and drive high
Settling Time to Within 5%		2.5		ns	C_B	Measured from output crossing 50% final value to output within 5% final value

PPMU SPECIFICATIONS

PPMU enabled in force voltage mode unless noted.

Table 7.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
FORCE VOLTAGE (FV)						
Current Range A	−40		+40	mA	D	
Current Range B	−1		+1	mA	D	
Current Range C	−100		+100	µA	D	
Current Range D	−10		+10	µA	D	
Current Range E	−2		+2	µA	D	
FV Range at Output, Range A	−1.0		+4.0	V	D	Output range for full-scale source/sink
	−1.5		+4.5	V	D	Output range for ±25 mA or less
FV Range at Output, Range B, Range C, Range D, and Range E	−1.5		+4.5	V	D	Output range for full-scale source/sink
FV Offset, Range C	−100		+100	mV	P	Measured at DAC Code 0x4000 (0.0 V) in Range C
FV Offset, All Ranges		±30		mV	C_T	Measured at DAC Code 0x4000 (0.0 V) applies to all other ranges
FV Offset TC, All Ranges		±100		µV/°C	C_T	Measured at DAC Code 0x4000 (0.0 V)
FV Gain, Range C	1.0		1.1	V/V	P	Gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V); based on an ideal DAC transfer function
FV Gain, All Ranges		1.05		V/V	C_T	Gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V); based on an ideal DAC transfer function
FV Gain TC, All Ranges		±10		ppm/°C	C_T	Gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
FV INL						
Range A		±1.5		mV	C_T	After two-point gain/offset calibration, output range of −1.5 V to +4.5 V; calibration points DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V), PPMU Current Range A
Range C, Focused Range	−1.7		+1.7	mV	P	After two-point gain/offset calibration, output range of −0.5 V to +3.5 V; calibration points DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
Range C, Full Range	−5		+5	mV	P	After two-point gain/offset calibration, output range of −1.5 V to +4.5 V; calibration points DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
Range B, Range D, and Range E		±1.0		mV	C_T	After two-point gain/offset calibration, output range of −1.5 V to +4.5 V; calibration points DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
FV Compliance vs. Source/Sink Current, Range A (±40 mA)		±1		mV	C_T	Force −1.0 V; measure voltage while sinking 0.0 mA and full-scale current; measure ΔV; force 4.0 V; measure voltage while sourcing 0.0 mA and full-scale current; measure ΔV
FV Compliance vs. Source/Sink Current, Range A (±25 mA)		±1		mV	C_T	Force −1.5 V; measure voltage while sinking 0.0 mA and 25 mA; measure ΔV; force 4.5 V; measure voltage while sourcing 0.0 mA and 25 mA; measure ΔV

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
FV Compliance vs. Source/Sink Current, Range B, Range C, Range D, and Range E		±1		mV	C_T	Force −1.5 V; measure voltage while sinking 0.0 mA and full-scale current; measure ΔV; force 4.5 V; measure voltage while sourcing 0.0 mA and full-scale current; measure ΔV
DUTGND Voltage Accuracy	−5	±1	+5	mV	P	Over ±0.1 V range; measured over −0.5 V to +3.5 V focused PPMU output range
FORCE CURRENT (FI)						PPMU enabled in force current/measure current (FIMI)
DUTx Pin Voltage Range, Range A	−1.0		+4.0	V	D	Full-scale source and sink current
	−1.5		+4.5	V	D	DUTx pin source and sink 25 mA or less
DUTx Pin Voltage Range, Range B, Range C, Range D, and Range E	−1.5		+4.5	V	D	Full-scale source and sink current
Zero-Current Offset, All Ranges	−14.5		+14.5	% FSR	P	Interpolated from measurements at PPMU DAC Code 0x4CCC (−80% FS) and DAC Code 0xB333 (80% FS) for each range
Zero-Current Offset TC		±0.02		% FSR/°C	C_T	
Gain Error, All Ranges	0		30	%	P	Derived from measurements at PPMU DAC Code 0x4CCC (−80% FS) and DAC Code 0xB333 (80% FS) for each range
Gain Drift						
Range A		±50		ppm/°C	C_T	PPMU self heating effects in Range A can influence gain drift measurements
Range B		±50		ppm/°C	C_T	
Range C, Range D, and Range E		±50		ppm/°C	C_T	
INL						After two-point gain/offset calibration
Range A	−0.12		+0.12	% FSR	P	Measured over FSR output of Range A (±40 mA)
Range B, Range C, and Range D	−0.04		+0.04	% FSR	P	Measured over FSR output of Range B (±1 mA), Range C (±100 µA), and Range D (±10 µA)
Range E	−0.045		+0.045	% FSR	P	Measured over FSR output of Range E (±2 µA)
FI Compliance vs. Voltage Load						
Range A	−0.3		+0.3	% FSR	P	Force positive full-scale current driving −1.0 V and +4.0 V, measure ΔI at DUTx pin; force negative full-scale current driving −1.0 V and +4.0 V, measure ΔI at DUTx pin
	−0.1		+0.1	% FSR	P	Force positive full-scale current driving 0.0 V and 3.0 V, measure ΔI at DUTx pin; force negative full-scale current driving 0.0 V and 3.0 V, measure ΔI at DUTx pin
Range B and Range C	−0.3		+0.3	% FSR	P	Force positive full-scale current driving −1.5 V and +4.5 V, measure ΔI at DUTx pin; force negative full-scale current driving −1.5 V and +4.5 V, measure ΔI at DUTx pin
	−0.06		+0.06	% FSR	P	Force positive full-scale current driving 0.0 V and 3.0 V, measure ΔI at DUTx pin; force negative full-scale current driving 0.0 V and 3.0 V, measure ΔI at DUTx pin
Range D	−0.3		+0.3	% FSR	P	Force positive full-scale current driving −1.5 V and +4.5 V, measure ΔI at DUTx pin; force negative full-scale current driving −1.5 V and +4.5 V, measure ΔI at DUTx pin
Range E	−0.85		+0.85	% FSR	P	Force positive full-scale current driving −1.5 V and +4.5 V, measure ΔI at DUTx pin; force negative full-scale current driving −1.5 V and +4.5 V, measure ΔI at DUTx pin; allows 10 nA DUTx pin leakage

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
MEASURE VOLTAGE (MV)						PPMU enabled, force voltage/measure voltage (FVMV)
Range	−1.5		+4.5	V	D	
Offset	−25		+25	mV	P	Range B, V_{DUTx} = 0.0 V, offset = (PPMU_Mx − V_{DUTx})
Offset TC		±50		µV/°C	C_T	
Gain	0.98		1.02	V/V	P	Range B, derived from measurements at V_{DUTx} = 0.0 V and 3.0 V
Gain TC		±5		ppm/°C	C_T	
INL	−1.7		+1.7	mV	P	Range B, measured over −1.5 V to +4.5 V
MEASURE CURRENT (MI)						PPMU enabled in FIMI
DUTx Pin Voltage Range						Full-scale source and sink current
Range A	−1.0		+4.0	V	D	
Range B, Range C, Range D, and Range E	−1.5		+4.5	V	D	
Zero-Current Offset						
Range B	−4		+4	%FSR	P	Interpolated from measurements sourcing and sinking 80% FS current each range; for example, 2% FSR is 40 µA in Range B
All Ranges		±0.5		%FSR	C_T	
Zero-Current Offset TC						
Range A		±0.01		%FSR/°C	C_T	
Range B, Range C, and Range D		±0.01		%FSR/°C	C_T	
Range E		±0.02		%FSR/°C	C_T	
Gain Error						Derived from measurements sourcing and sinking 80% FS current
Range B	−30		+5	%	P	
All Ranges		−10		%	C_T	
Gain TC						
Range A		±50		ppm/°C	C_T	
Range B, Range C, and Range D		±50		ppm/°C	C_T	
Range E		±50		ppm/°C	C_T	
INL						After two-point gain/offset calibration at ±80% FS current
Range A		±0.02		%FSR	C_T	Measured over FSR output of −40 mA to +40 mA
Range B	−0.02		+0.02	%FSR	P	Measured over FSR output of −1 mA to +1 mA
Range C, Range D, and Range E		±0.01		%FSR	C_T	Measured over FSR output of Range C, Range D, and Range E
DUTx Pin Voltage Rejection	−1.3		+1.3	µA	P	Range B, FVMI, force −1.0 V and +4.0 V into 0.5 mA load, measure ΔI reported at PPMU_Mx pin
DUTGND Voltage Accuracy	−5	±1	+5	mV	P	Over ±0.1 V range
MEASURE PIN DC CHARACTERISTICS						
Output Range	−1.5		+5.0	V	D	
Output Impedance			200	Ω	P	PPMU enabled in FVMV, source resistance: PPMU force 4.5 V into 0.0 mA, −1.0 mA, sink resistance: PPMU force −1.5 V into 0.0 mA, 1.0 mA, resistance = ΔV/ΔI at PPMU_Mx pin
Output Leakage Current When Tristated	−1		+1	µA	P	Tested at −1.7 V and +5.2 V
Output Short Circuit Current	−10		+10	mA	P	PPMU enabled in FVMV, source: PPMU force +4.5 V, PPMU_Mx = −1.5 V, sink: PPMU force −1.5 V, PPMU_Mx = 5.0 V

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
PPMU_Mx Pin, Parasitic Output Capacitance			2	pF	S	Parasitic capacitance contributed by pin
PPMU_Mx Pin, External Load Capacitance	100			pF	S	External capacitance tolerated by pin (exceeding this value may cause instability)
PPMU VOLTAGE CLAMPS (FI)						PPMU enabled in FIMI, PPMU clamps enabled; clamp accuracy applies only when |PCHx − PCLx| ≥ 1.0 V
Low Voltage Clamp Range (PCLx)	−1.5		+3.5	V	D	
High Voltage Clamp Range (PCHx)	−0.5		+4.5	V	D	
Offset, Voltage Clamps (PCHx/PCLx)	−300		+300	mV	P	Range B, PPMU force ±0.5 mA into open; PCHx measured at DAC Code 0x4000 (0.0 V) with PCLx at DAC Code 0x0000 (−2.5 V); PCLx measured at DAC Code 0x4000 (0.0 V) with PCHx at DAC Code 0xFFFF (+7.5 V)
Offset TC, Voltage Clamps (PCHx/PCLx)		±0.5		mV/°C	C_T	
Gain, Voltage Clamps (PCHx/PCLx)	1.0		1.1	V/V	P	Range B, PPMU force ±0.5 mA into open; PCHx gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V) with PCLx at DAC Code 0x0000 (−2.5 V); PCLx gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V) with PCHx at DAC Code 0xFFFF (7.5 V)
Gain TC, Voltage Clamps (PCHx/PCLx)		±25		ppm/°C	C_T	
INL, Voltage Clamps (PCHx/PCLx)	−20		+20	mV	P	Range B, PPMU force ±0.5 mA into open after two-point gain/offset calibration; measured over PPMU clamp functional range
Positive Voltage Clamp, Voltage Droop (Source)	−50		+50	mV	P	ΔV at DUTx pin, Range A, PCHx = +4.0 V, PCLx = −1.0 V, PPMU force 5.0 mA and 40 mA into open circuit, calibrated
Negative Voltage Clamp, Voltage Droop (Sink)	−50		+50	mV	P	ΔV at DUTx pin, Range A, PCHx = +4.0 V, PCLx = −1.0 V, PPMU force −5.0 mA and −40 mA into open circuit, calibrated
DUTGND Voltage Accuracy	−5	±1	+5	mV	P	Over ±0.1 V range; measured at end points of clamp functional range
PPMU CURRENT CLAMPS (FV)						PPMU enabled in FVMV, dc accuracy of the current clamps only applies over the following conditions: 30% FS ≤ PCHx ≤ 100% FS or −100% FS ≤ PCLx ≤ −30% FS
Functional Range						
Low Current Clamp (PCLx)	−120		−20	%FS	S	For example, −120% FS in Range A is −48 mA and −20% FS in Range A is −8 mA
High Current Clamp (PCHx)	20		120	%FS	S	For example, 20% FS in Range A is 8 mA and 120% FS in Range A is 48 mA
DC Accuracy Range						
Low Current Clamp (PCLx)	−100		−30	%FS	D	For example, −100% FS in Range A is −40 mA and −30% FS in Range A is −12 mA
High Current Clamp (PCHx)	30		100	%FS	D	For example, 30% FS in Range A is 12 mA and 100% FS in Range A is 40 mA
Static Current Limit, Source and Sink, All Ranges	±120	±140	±160	%FS	P	PCLx at DAC Code 0x0000 (−2.5 V), PCHx at DAC Code 0xFFFF (7.5 V), sink: force −1.5 V, short DUTx to 4.5 V, source: force 4.5 V, short DUTX to −1.5 V
Offset, Current Clamps (PCHx/PCLx)	−10		+10	%FSR	P	All ranges; PPMU force ±1.0 V into 0.0 V[1]
Offset TC, Current Clamps (PCHx/PCLx)		±0.02		%FSR/°C	C_T	All ranges

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
Gain Error, Current Clamps (PCHx/PCLx)	0		30	%	P	All ranges; PPMU force ±1.0 V into 0.0 V[2]
Gain TC, Current Clamps (PCHx/PCLx)		±50		ppm/°C	C_T	All ranges
INL, Current Clamps (PCHx/PCLx)	−0.15		+0.15	%FSR	P	All ranges; PPMU force ±1.0 V into 0.0 V, after two-point gain/offset calibration; PCHx calibration at DAC Code 0xA000 (3.75 V or 50% FS) and DAC Code 0xB333 (4.50 V or 80% FS); PCLx calibration at DAC Code 0x6000 (1.25 V or −50% FS) and DAC Code 0x4CCC (0.50 V or −80% FS); measured over dc accuracy range
Current Droop						
Low Current Clamp (PCLx), Sink	−2		+2	%FSR	P	PCLx = 0.5 V (−80% FS), PCHx = 4.5 V (80% FS), PPMU force −0.5 V and +3.5 V into V_{DUTx} = 4.5 V, measure ΔI at the DUTx pin in Range A
High Current Clamp (PCHx), Source	−2		+2	%FSR	P	PCLx = 0.5 V (−80% FS), PCHx = 4.5 V (80% FS), PPMU force −0.5 V and +3.5 V into V_{DUTx} = −1.5 V, measure ΔI at the DUTx pin in Range A
SETTLING/SWITCHING TIMES						
FV Settling Time to 0.1% of Final Value						
Range A, 200 pF and 2000 pF Load		20		µs	S	PPMU enabled in FV, Range A, step from 0.0 V to 4.0 V
Range B, 200 pF and 2000 pF Load		25		µs	S	PPMU enabled in FV, Range B, DCL disabled, step from 0.0 V to 4.0 V
Range C, 200 pF Load		25		µs	S	PPMU enabled in FV, Range C, DCL disabled, step from 0.0 V to 4.0 V
Range C, 2000 pF Load		65		µs	S	PPMU enabled in FV, Range C, DCL disabled, step from 0.0 V to 4.0 V
FV Settling Time to 1.0% of Final Value						
Range A, 200 pF and 2000 pF Load		16		µs	C_B	PPMU enabled in FV, Range A, DCL disabled, step from 0.0 V to 4.0 V
Range B, 200 pF and 2000 pF Load		14		µs	C_B	PPMU enabled in FV, Range B, DCL disabled, step from 0.0 V to 4.0 V
Range C, 200 pF and 2000 pF Load		18		µs	C_B	PPMU enabled in FV, Range C, DCL disabled enabled, step from 0.0 V to 4.0 V
FI Settling Time to 0.1% of Final Value						
Range A, 200 pF in Parallel with 120 Ω		16		µs	S	PPMU enabled in FI, Range A, DCL disabled, step from 0.0 mA to 40 mA
Range B, 200 pF in Parallel with 1.5 kΩ		10		µs	S	PPMU enabled in FI, Range B, DCL disabled, step from 0.0 mA to 1 mA
Range C, 200 pF in Parallel with 15.0 kΩ		40		µs	S	PPMU enabled in FI, Range C, DCL disabled, step from 0.0 mA to 100 µA
FI Settling Time to 1.0% of Final Value						
Range A, 200 pF in Parallel with 120 Ω		8		µs	C_B	PPMU enabled in FI, Range A, DCL disabled, step from 0.0 mA to 40 mA
Range B, 200 pF in Parallel with 1.5 kΩ		8		µs	C_B	PPMU enabled in FI, Range B, DCL disabled, step from 0.0 mA to 1 mA
Range C, 200 pF in Parallel with 15.0 kΩ		8		µs	C_B	PMU enabled in FI, Range C, DCL disabled, step from 0.0 mA to 100 µA

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
INTERACTION AND CROSSTALK						
Measure Voltage Channel to Channel Crosstalk		10		µV	C_T	PPMU enabled in FIMV, Range B, channel under test: force 0.0 mA into 0.0 V; other channel: force 0.0 mA into V_{DUTx}; sweep V_{DUTx} from −1.5 V to +4.5 V; measure ΔV at PPMU_Mx under test
Measure Current Channel to Channel Crosstalk		0.0001		%FSR	C_T	PPMU enabled in FVMI, Range B; channel under test: force 0.0 V into open circuit; other channel: force 0.0 V into I_{DUTx}; sweep I_{DUTx} from −1.0 mA to +1.0 mA; measure ΔV at PPMU_Mx under test

[1] PCHx offset is derived from measurements at DAC Code 0xA000 (3.75 V or 50% FS) and DAC Code 0xB333 (4.50 V or 80% FS), with PCLx at DAC Code 0x0000 (−2.5 V). PCLx offset is derived from measurements at DAC Code 0x6000 (1.25 V or −50% FS) and DAC Code 0x4CCC (0.50 V or −80% FS), with PCHx at DAC Code 0xFFFF (7.5 V).
[2] PCHx gain is derived from the measurements at DAC Code 0xA000 (3.75 V or 50% FS) and DAC Code 0xB333 (4.50 V or 80% FS), with PCLx at DAC Code 0x0000 (−2.5 V). PCLx gain is derived from measurements at DAC Code 0x6000 (1.25 V or −50% FS) and DAC Code 0x4CCC (0.50 V or −80% FS), with PCHx at DAC Code 0xFFFF (7.5 V). For example, the ideal gain is ±FS per 2.5 V in all ranges; in Range B, the ideal gain is ±400 µA/V; therefore, 30% error is ±520 µA/V.

PPMU GO/NO-GO COMPARATORS SPECIFICATIONS

Table 8.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						
Compare Voltage Range	−1.5		+5.0	V	D	
Input Offset Voltage	−250		+250	mV	P	Measured at DAC Code 0x4000 (0 V)
Input Offset Voltage TC		±100		µV/°C	C_T	
Gain	1.0		1.1	V/V	P	Gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
Gain TC		±10		ppm/°C	C_T	Gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
Comparator Threshold Resolution		153		µV	D	
Comparator Threshold DNL		±250		µV	C_T	After two-point calibration; measured over POHx/POLx range −1.5 V to +5.0 V; calibration points DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
Comparator Threshold INL	−7		+7	mV	P	After two-point calibration; measured over POHx/POLx range −1.5 V to +5.0 V; calibration points DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V)
DUTGND Voltage Accuracy	−5	±1	+5	mV	P	Over ±0.1 V range

PPMU EXTERNAL SENSE PINS SPECIFICATIONS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						
Voltage Range	−1.5		+4.5	V	D	PPMU input select, in all states
Leakage	−2	0.0	+2	nA	P	Tested at −1.5 V and +4.5 V
Maximum Load Capacitance	2000			pF	S	Capacitive load tolerated at DUTx sense pins

VREF, VREFGND, AND DUTGND REFERENCE INPUT PINS SPECIFICATIONS

Table 10.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						
VREF Input Voltage Range	2.475	2.500	2.525	V	D	Provided externally, V_{REF} = 2.500 V, V_{REFGND} = 0.000 V
VREF Input Bias Current			10	µA	P	Tested with 2.500 V applied
DUTGND Input Voltage Range, Referenced to AGND	−0.1		+0.1	V	D	
DUTGND Input Bias Current	−10		+10	µA	P	Tested at −100 mV and +100 mV

TEMPERATURE MONITOR SPECIFICATIONS

Table 11.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						
Temperature Sensor Gain		10		mV/K	D	3.00 V at room temperature, 300 K (23°C)
Temperature Sensor Accuracy		±10		°C	C_T	20°C < T_C < 80°C, $V_{CCTHERM}$ only (T_J = T_C)

ALARM FUNCTIONS SPECIFICATIONS

Table 12.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						
Overvoltage Alarm High, OVDH						
Functional Voltage Range	−1.0		+5.0	V	D	OVDL DAC set to DAC Code 0x0000 (−2.5 V)
Uncalibrated Error at −1.0 V	−300		+200	mV	P	Includes 5% uncalibrated gain ±250 mV offset
Uncalibrated Error at 5.0 V	0		500	mV	P	Includes 5% uncalibrated gain ±250 mV offset
Offset Voltage TC		±0.5		mV/°C	C_T	
Gain		1.05		V/V	C_T	Gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V); based on an ideal DAC transfer function (see Table 24)
Hysteresis		140		mV	C_T	Hysteresis is only applied coming out of alarm
Overvoltage Alarm Low, OVDL						
Functional Voltage Range	−2.0		+4.0	V	D	OVDH DAC set to DAC Code 0xFFFF (7.5 V)
Uncalibrated Error at −2.0 V	−350		+150	mV	P	Includes 5% uncalibrated gain ±250 mV offset
Uncalibrated Error at 4.0 V	−50		+450	mV	P	Includes 5% uncalibrated gain ±250 mV offset
Offset Voltage TC		±0.5		mV/°C	C_T	
Gain		1.05		V/V	C_T	Gain derived from measurements at DAC Code 0x4000 (0.0 V) and DAC Code 0x8CCC (3.0 V); based on an ideal DAC transfer function (see Table 24)
Hysteresis		140		mV	C_T	Hysteresis is only applied coming out of alarm
Thermal Alarm						
Setpoint Error		±10		°C	C_T	Relative to default alarm value, T_J = 100°C
Thermal Hysteresis		15		°C	C_T	

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
$\overline{\text{ALARM}}$ Output Characteristics						
Off State Leakage		10	500	nA	P	Disable alarm, apply V_{DD} to $\overline{\text{ALARM}}$ pin, and measure leakage current
Maximum On Voltage at 200 µA		0.1	0.7	V	P	$\overline{\text{ALARM}}$ pin asserted, force 200 µA into pin and measure voltage
AC SPECIFICATIONS						
Propagation Delay		0.5		µs	C_B	For OVDH: V_{DUTx} = 0.0 V to 4.5 V step, OVDH = 4.0 V, OVDL = −1.0 V; for OVDL: V_{DUTx} = 0.0 V to −1.5 V step, OVDH = 4.0 V, OVDL = −1.0 V

SERIAL PROGRAMMABLE INTERFACE (SPI) SPECIFICATIONS

Table 13.

Parameter	Min	Typ	Max	Unit	Test Level	Test Conditions/Comments
DC SPECIFICATIONS						
Input Voltage						$\overline{\text{RST}}$, $\overline{\text{CS}}$, SCLK, SDI
Logic High	V_{DD} − 0.7		V_{DD}	V	P_F	
Logic Low	0.0		0.7	V	P_F	
Input Bias Current	−10	1	+10	µA	P	Tested at 0.0 V and V_{DD}; $\overline{\text{RST}}$ tested at V_{DD}; $\overline{\text{RST}}$ has an internal 50 kΩ pull-up to V_{DD}
SCLK Crosstalk on DUTx Pin		1		mV	C_B	DCL disabled, PPMU forcing 0.0 V
Serial Output						
Logic High	V_{DD} − 0.5		V_{DD}	V	P_F	SDO, sourcing 2 mA
Logic Low	0.0		0.5	V	P_F	Sinking 2 mA
$\overline{\text{BUSY}}$ Output Characteristics						Open-drain output
Off State Leakage		10	500	nA	P	$\overline{\text{BUSY}}$ pin not asserted, apply V_{DD} to pin and measure leakage current
Maximum On Voltage at 2 mA		0.01	0.7	V	P	$\overline{\text{BUSY}}$ pin asserted, force 2 mA into pin and measure voltage

SPI TIMING SPECIFICATIONS

Table 14.

Parameter	Symbol	Min	Typ	Max	Unit	Test Level	Description
SCLK Operating Frequency	f_{CLK}		50		MHz	P_F	
		0.5		100	MHz	S	
SCLK High Time	t_{CH}	4.5			ns	S	
SCLK Low Time	t_{CL}	4.5			ns	S	
$\overline{\text{CS}}$ to SCLK Setup at Assert	t_{CSAS}	1.5			ns	S	Setup time of $\overline{\text{CS}}$ assert to next rising edge of SCLK.
$\overline{\text{CS}}$ to SCLK Hold at Assert	t_{CSAH}	1.5			ns	S	Hold time of $\overline{\text{CS}}$ assert to next rising edge of SCLK.
$\overline{\text{CS}}$ to SCLK Setup at Release	t_{CSRS}	1.5			ns	S	Setup time of $\overline{\text{CS}}$ release to next rising edge of SCLK.
$\overline{\text{CS}}$ to SCLK Hold at Release	t_{CSRH}	1.5			ns	S	Hold time of $\overline{\text{CS}}$ release to next rising edge of SCLK. This parameter is only critical if the number of SCLK cycles from previous release of $\overline{\text{CS}}$ is the minimum specified by the t_{CSAM} parameter.
$\overline{\text{CS}}$ Assert to SDO Active	t_{CSO}	0		4	ns	S	Delay time from $\overline{\text{CS}}$ assert to SDO active state.
$\overline{\text{CS}}$ Release to SDO High-Z	t_{CSZ}	0		11	ns	S	Delay from $\overline{\text{CS}}$ release to SDO high-Z state, strongly influenced by external SDO pin loading.
$\overline{\text{CS}}$ Release to Next Assert	t_{CSAM}	3			Cycles	D	Minimum release time of $\overline{\text{CS}}$ between consecutive assertions of $\overline{\text{CS}}$. This parameter is specified in units of SCLK cycles, more specifically in terms of rising edges of the SCLK input.

Parameter	Symbol	Min	Typ	Max	Unit	Test Level	Description
SDI to SCLK Setup	t_{DS}	3			ns	S	Setup time of SDI data prior to next rising edge of SCLK.
SDI to SCLK Hold	t_{DH}	4			ns	S	Hold time of SDI data following previous rising edge of SCLK.
SCLK to Valid SDO	t_{DO}	0		6	ns	S	Propagation delay from rising edge of SCLK to valid SDO data.
$\overline{BUSY}$ Assert from $\overline{CS}$/$\overline{RST}$	t_{BUSA}	0		6	ns	S	Propagation delay from first rising SCLK following valid $\overline{CS}$ release (or $\overline{RST}$ release in the case of hardware reset) to $\overline{BUSY}$ assert.
$\overline{BUSY}$ Width	t_{BUSW}						
Following $\overline{CS}$		3		21	Cycles	D	Delay time from first rising SCLK after valid $\overline{CS}$ release to $\overline{BUSY}$ release. Satisfies the requirements detailed in the SPI Clock Cycles and the Pin section, except following $\overline{RST}$ or software reset.
Following $\overline{RST}$		744			Cycles	D	Delay time from first rising SCLK after $\overline{RST}$ release (or valid $\overline{CS}$ release in the case of software reset) to $\overline{BUSY}$ release. Satisfies the requirement of synchronous reset sequence detailed in the SPI Clock Cycles and the Pin section.
$\overline{BUSY}$ Release from SCLK	t_{BUSR}	0		10	ns	S	Propagation delay from qualifying SCLK edge to $\overline{BUSY}$ release.
Width of $\overline{RST}$ Assert	t_{RMIN}	5			ns	S	Minimum width of asynchronous $\overline{RST}$ assert, 5 pF external loading.
$\overline{RST}$ to SCLK Setup at Assert	t_{RS}	1.5			ns	S	Minimum setup time of $\overline{RST}$ release to next rising edge of SCLK.
SCLK Cycles per SPI Word	t_{SPI}	29			Cycles	D	Minimum number of SCLK rising edge cycles required per valid SPI operation, including the minimum t_{CSAM} requirement between consecutive $\overline{CS}$ assertions.
Internal DAC Settling to Within ±2 mV from $\overline{BUSY}$ Release	t_{DAC}		10		µs	C_B	Settling time of internal analog DAC levels to within ±2 mV. Settling time is relative to the release of $\overline{BUSY}$.[1]

[1] The overall settling time may be dominated by the characteristics of an analog block (such as the PPMU or driver) and its respective mode setting (such as Range A or Range B).

SPI TIMING DIAGRAMS

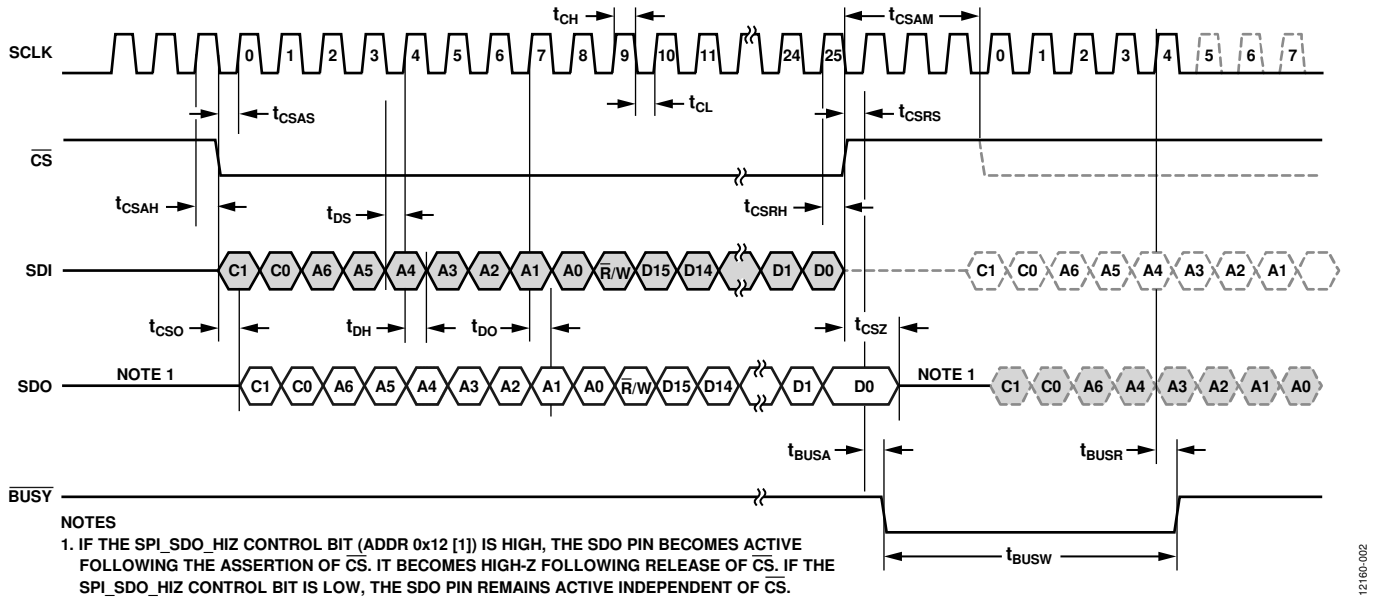


Figure 2. SPI Detailed Read/Write Timing Diagram

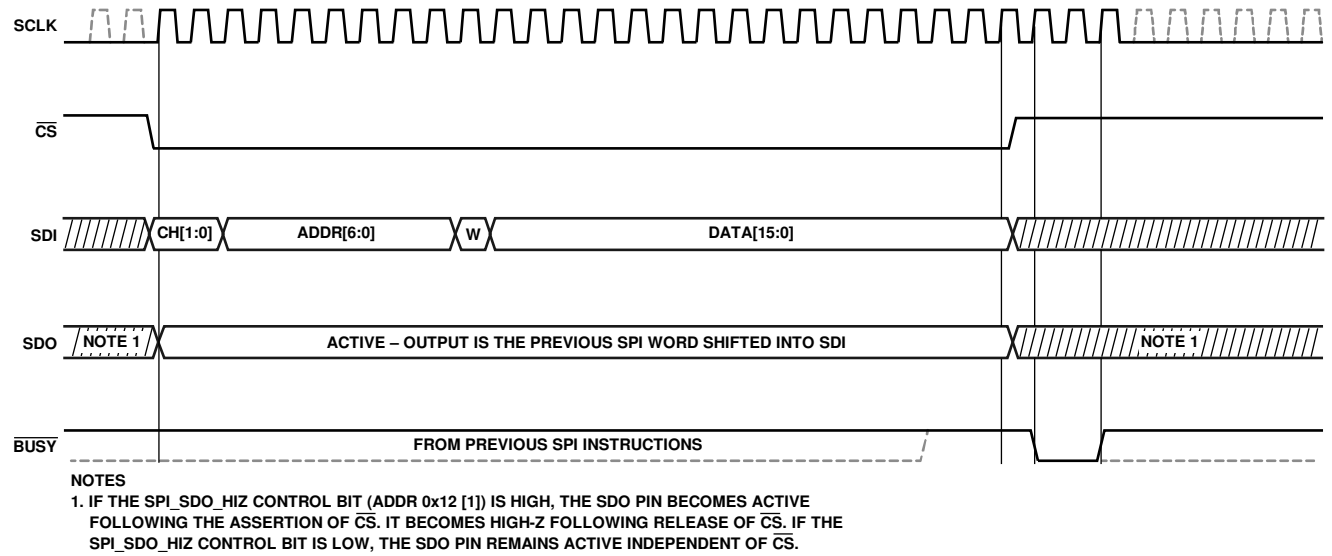


Figure 3. SPI Write Instruction Timing Diagram

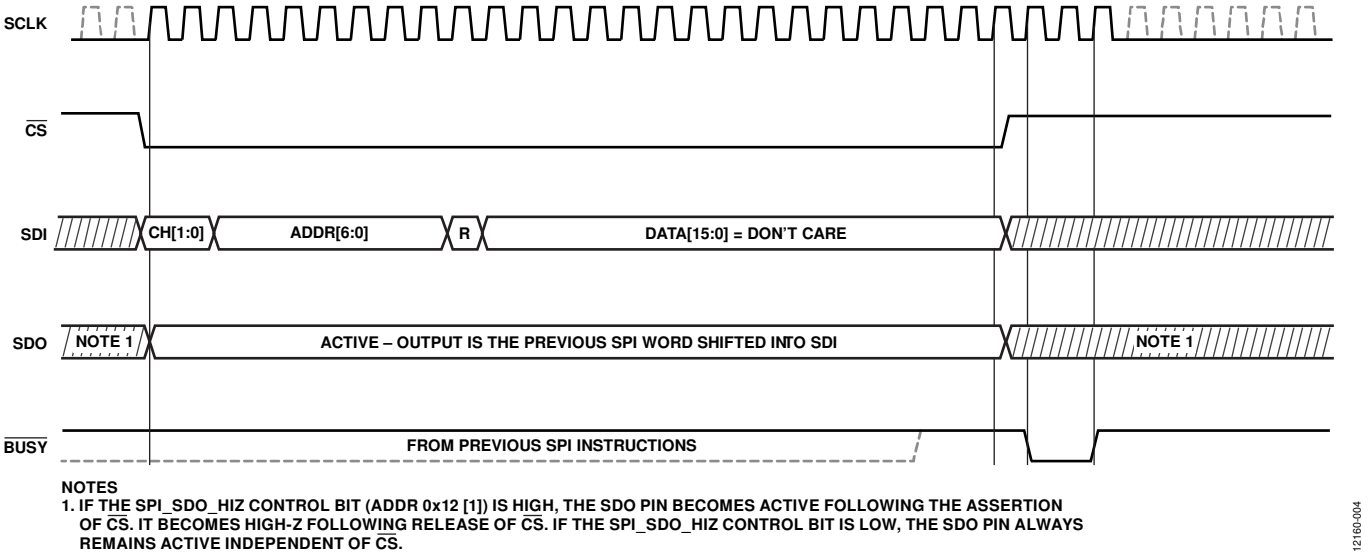
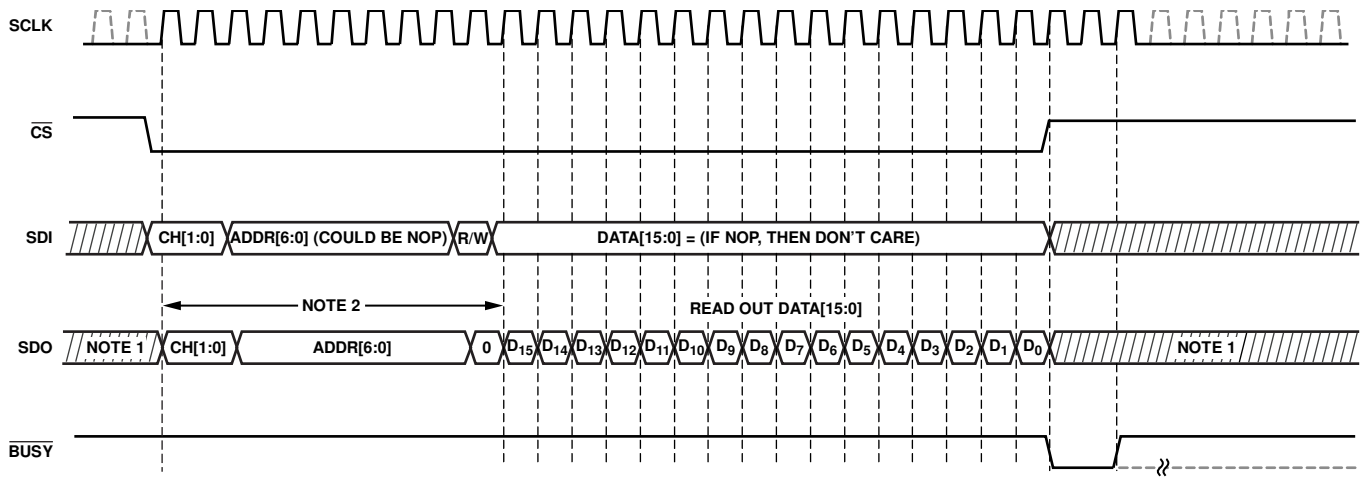


Figure 4. SPI Read Request Instruction Timing Diagram (Prior to Readout Instruction)



NOTES
1. IF THE SPI_SDO_HIZ CONTROL BIT (ADDR 0x12 [1]) IS HIGH, THE SDO PIN BECOMES ACTIVE FOLLOWING THE ASSERTION OF $\overline{CS}$. IT BECOMES HIGH-Z FOLLOWING RELEASE OF $\overline{CS}$. IF THE SPI_SDO_HIZ CONTROL BIT IS LOW, THE SDO PIN REMAINS ACTIVE INDEPENDENT OF $\overline{CS}$.
2. THE FIRST 10 BITS OF SDO FOLLOWING A READ REQUEST ECHO ADDRESS AND CHANNEL BITS OF THE PRECEDING REQUEST. THE R/W BIT POSITION IS SET LOW. THE FOLLOWING 16 BITS CONTAIN DATA FROM THE REQUESTED ADDRESS AND CHANNEL.

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Figure 5. SPI Readout Instruction Timing Diagram (Subsequent to Read Request Instruction)

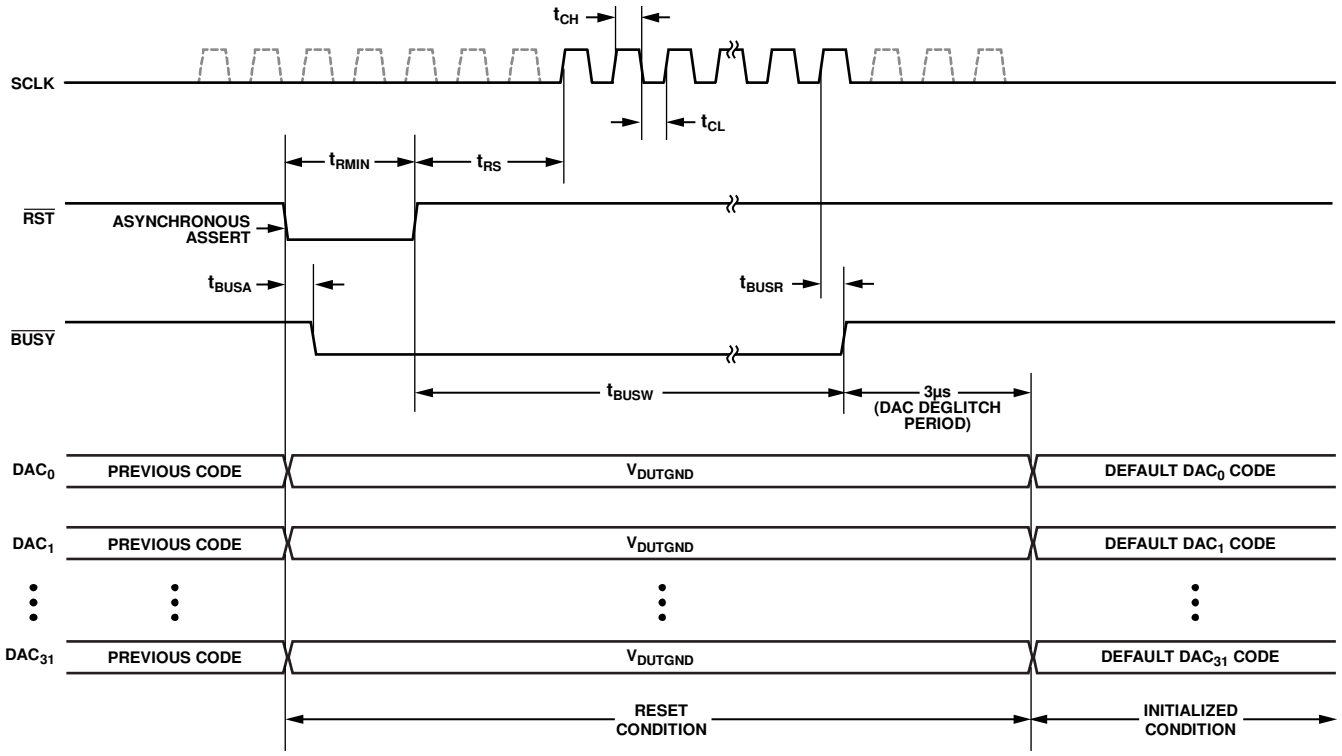

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Figure 6. SPI Detailed Hardware Reset Timing Diagram

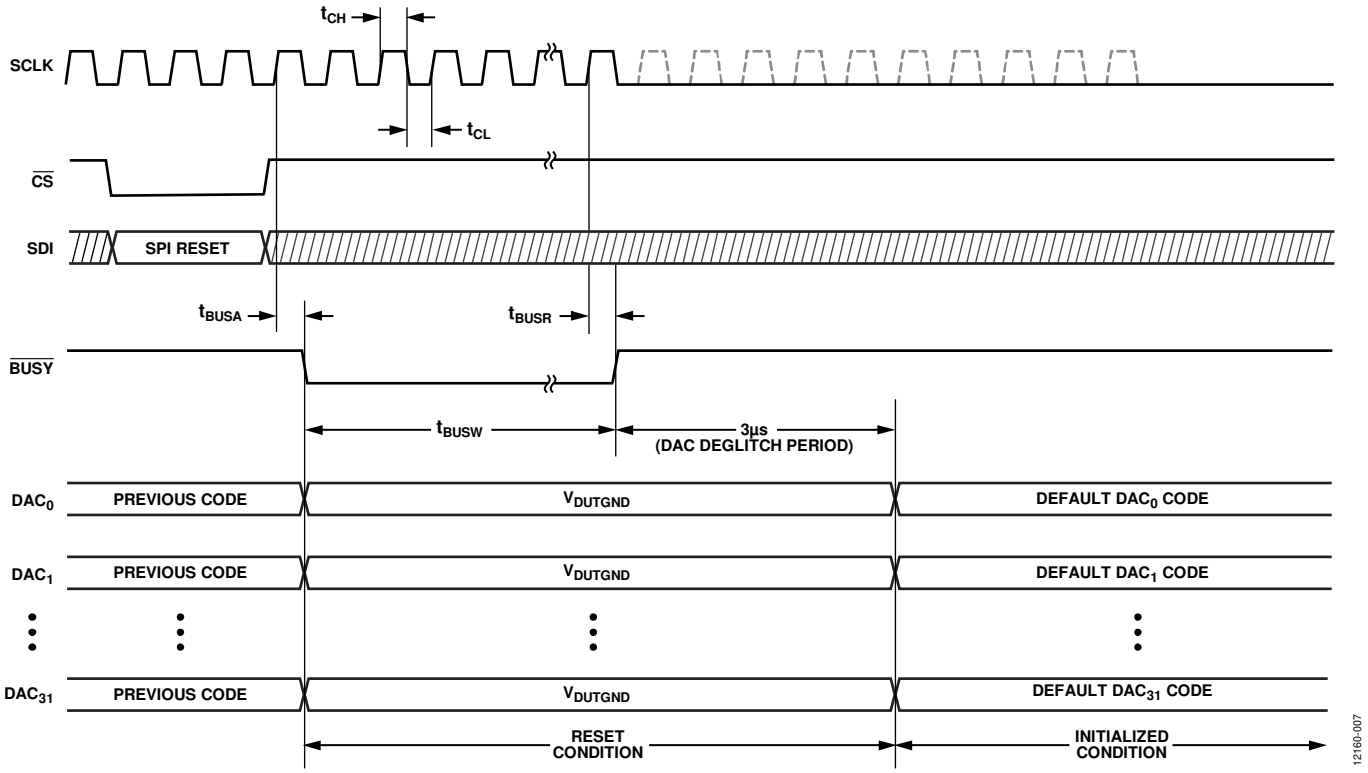

Figure 7. SPI Detailed Software Reset Timing Diagram