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Stereo, Low Power, 96 kHz, 24-Bit Audio Codec with Integrated PLL

ADAU1361

FEATURES

24-bit stereo audio ADC and DAC: >98 dB SNR
Sampling rates from 8 kHz to 96 kHz
Low power: 7 mW record, 7 mW playback, 48 kHz at 1.8 V
6 analog input pins, configurable for single-ended or differential inputs
Flexible analog input/output mixers
Stereo digital microphone input
Analog outputs: 2 differential stereo, 2 single-ended stereo, 1 mono headphone output driver
PLL supporting input clocks from 8 MHz to 27 MHz
Analog automatic level control (ALC)
Microphone bias reference voltage
Analog and digital I/O: 1.8 V to 3.65 V
I²C and SPI control interfaces
Digital audio serial data I/O: stereo and time-division multiplexing (TDM) modes
Software-controllable clickless mute
Software power-down
32-lead, 5 mm × 5 mm LFCSP
−40°C to +85°C operating temperature range

APPLICATIONS

Smartphones/multimedia phones
Digital still cameras/digital video cameras
Portable media players/portable audio players
Phone accessories products

GENERAL DESCRIPTION

The ADAU1361 is a low power, stereo audio codec that supports stereo 48 kHz record and playback at 14 mW from a 1.8 V analog supply. The stereo audio ADCs and DACs support sample rates from 8 kHz to 96 kHz as well as a digital volume control. The ADAU1361 is ideal for battery-powered audio and telephony applications.

The record path includes an integrated microphone bias circuit and six inputs. The inputs can be mixed and muxed before the ADC, or they can be configured to bypass the ADC. The ADAU1361 includes a stereo digital microphone input.

The ADAU1361 includes five high power output drivers (two differential and three single-ended), supporting stereo headphones, an earpiece, or other output transducer. AC-coupled or capless configurations are supported. Individual fine level controls are supported on all analog outputs. The output mixer stage allows for flexible routing of audio.

The serial control bus supports the I²C and SPI protocols. The serial audio bus is programmable for I²S, left-/right-justified, and TDM modes. A programmable PLL supports flexible clock generation for all standard integer rates and fractional master clocks from 8 MHz to 27 MHz.

FUNCTIONAL BLOCK DIAGRAM

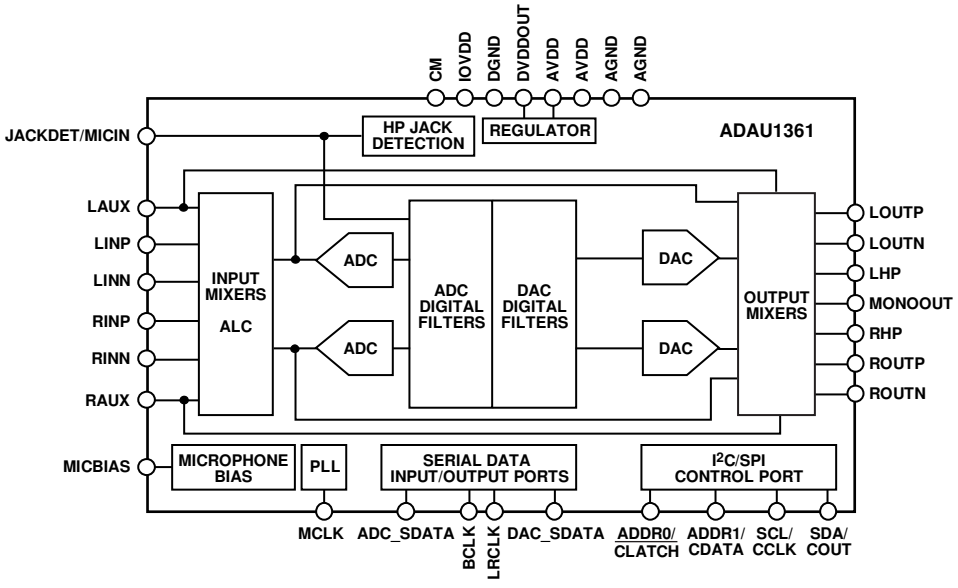

Figure 1.

Rev. C

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADAU1361 Evaluation Board
- ADUSB2EBZ Evaluation Board

DOCUMENTATION

Application Notes

- AN-1006: Using the EVAL-ADUSB2EBZ
- AN-1056: Capless Headphone Virtual Ground Short-Circuit Protection for the ADAU1361 and ADAU1761 Low Power Codecs

Data Sheet

- ADAU1361: Stereo, Low Power, 96 kHz, 24-BitAudio Codec with Integrated PLL Data Sheet

User Guides

- UG-119: Evaluation Board User Guide for ADAU1361

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADAU1361 Sound CODEC Linux Driver

TOOLS AND SIMULATIONS

- SigmaDSP Processors: Software and Tools
- ADAU1361/ADAU1761 IBIS Models

DESIGN RESOURCES

- ADAU1361 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADAU1361 EngineerZone Discussions.

SAMPLE AND BUY

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1/09—Revision 0: Initial Version

SPECIFICATIONS

Supply voltage (AVDD) = 3.3 V, T_A = 25°C, master clock = 12.288 MHz (48 kHz f_S, 256 × f_S mode), input sample rate = 48 kHz, measurement bandwidth = 20 Hz to 20 kHz, word width = 24 bits, C_{LOAD} (digital output) = 20 pF, I_{LOAD} (digital output) = 2 mA, V_{IH} = 2 V, V_{IL} = 0.8 V, unless otherwise noted. Performance of all channels is identical, exclusive of the interchannel gain mismatch and interchannel phase deviation specifications.

ANALOG PERFORMANCE SPECIFICATIONS

Specifications guaranteed at 25°C (ambient).

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTERS	ADC performance excludes mixers and PGA				
ADC Resolution	All ADCs		24		Bits
Digital Attenuation Step			0.375		dB
Digital Attenuation Range			95		dB
INPUT RESISTANCE					
Single-Ended Line Input	−12 dB gain		83		kΩ
	0 dB gain		21		kΩ
	6 dB gain		10.5		kΩ
PGA Inverting Inputs	−12 dB gain		84.5		kΩ
	0 dB gain		53		kΩ
	35.25 dB gain		2		kΩ
PGA Noninverting Inputs	All gains		105		kΩ
SINGLE-ENDED LINE INPUT					
Full-Scale Input Voltage (0 dB)	Scales linearly with AVDD		AVDD/3.3		V rms
	AVDD = 1.8 V		0.55 (1.56)		V rms (V p-p)
	AVDD = 3.3 V		1.0 (2.83)		V rms (V p-p)
Dynamic Range	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		94		dB
	AVDD = 3.3 V		99		dB
No Filter (RMS)	AVDD = 1.8 V		91		dB
	AVDD = 3.3 V		96		dB
Total Harmonic Distortion + Noise	−1 dBFS				
	AVDD = 1.8 V		−88		dB
	AVDD = 3.3 V		−90		dB
Signal-to-Noise Ratio					
With A-Weighted Filter (RMS)	AVDD = 1.8 V		94		dB
	AVDD = 3.3 V		99		dB
No Filter (RMS)	AVDD = 1.8 V		91		dB
	AVDD = 3.3 V		96		dB
Gain per Step			3		dB
Total Gain Range		−12		+6	dB
Mute Attenuation			−87		dB
Interchannel Gain Mismatch			0.005		dB
Offset Error			0		mV
Gain Error			−12		%
Interchannel Isolation			68		dB
Power Supply Rejection Ratio	CM capacitor = 20 µF				
	100 mV p-p @ 217 Hz		65		dB
	100 mV p-p @ 1 kHz		67		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
PSEUDO-DIFFERENTIAL PGA INPUT					
Full-Scale Input Voltage (0 dB)	Scales linearly with AVDD		AVDD/3.3		V rms
	AVDD = 1.8 V		0.55 (1.56)		V rms (V p-p)
	AVDD = 3.3 V		1.0 (2.83)		V rms (V p-p)
Dynamic Range	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		92		dB
	AVDD = 3.3 V		98		dB
No Filter (RMS)	AVDD = 1.8 V		90		dB
	AVDD = 3.3 V		95		dB
Total Harmonic Distortion + Noise	−1 dBFS				
	AVDD = 1.8 V		−88		dB
	AVDD = 3.3 V		−89		dB
Signal-to-Noise Ratio					
With A-Weighted Filter (RMS)	AVDD = 1.8 V		92		dB
	AVDD = 3.3 V		98		dB
No Filter (RMS)	AVDD = 1.8 V		90		dB
	AVDD = 3.3 V		95		dB
Volume Control Step	PGA gain		0.75		dB
Volume Control Range	PGA gain	−12		+35.25	dB
PGA Boost			20		dB
Mute Attenuation			−87		dB
Interchannel Gain Mismatch			0.005		dB
Offset Error			0		mV
Gain Error			−14		%
Interchannel Isolation			83		dB
Common-Mode Rejection Ratio	100 mV rms, 1 kHz		65		dB
	100 mV rms, 20 kHz		65		dB
FULL DIFFERENTIAL PGA INPUT	Differential PGA inputs				
Full-Scale Input Voltage (0 dB)	Scales linearly with AVDD		AVDD/3.3		V rms
	AVDD = 1.8 V		0.55 (1.56)		V rms (V p-p)
	AVDD = 3.3 V		1.0 (2.83)		V rms (V p-p)
Dynamic Range	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		92		dB
	AVDD = 3.3 V		98		dB
No Filter (RMS)	AVDD = 1.8 V		90		dB
	AVDD = 3.3 V		95		dB
Total Harmonic Distortion + Noise	−1 dBFS				
	AVDD = 1.8 V		−70		dB
	AVDD = 3.3 V		−78		dB
Signal-to-Noise Ratio					
With A-Weighted Filter (RMS)	AVDD = 1.8 V		92		dB
	AVDD = 3.3 V		98		dB
No Filter (RMS)	AVDD = 1.8 V		90		dB
	AVDD = 3.3 V		95		dB
Volume Control Step	PGA gain		0.75		dB
Volume Control Range	PGA gain	−12		+35.25	dB
PGA Boost			20		dB
Mute Attenuation			−87		dB
Interchannel Gain Mismatch			0.005		dB
Offset Error			0		mV
Gain Error			−14		%

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Interchannel Isolation			83		dB
Common-Mode Rejection Ratio	100 mV rms, 1 kHz		65		dB
	100 mV rms, 20 kHz		65		dB
MICROPHONE BIAS	MBIEN = 1				
Bias Voltage					
0.65 × AVDD	AVDD = 1.8 V, MBI = 1		1.17		V
	AVDD = 3.3 V, MBI = 1		2.145		V
0.90 × AVDD	AVDD = 1.8 V, MBI = 0		1.62		V
	AVDD = 3.3 V, MBI = 0		2.97		V
Bias Current Source	AVDD = 3.3 V, MBI = 0, MPERF = 1			3	mA
Noise in the Signal Bandwidth	AVDD = 3.3 V, 1 kHz to 20 kHz				
	MBI = 0, MPERF = 0		42		nV/√Hz
	MBI = 0, MPERF = 1		85		nV/√Hz
	MBI = 1, MPERF = 0		25		nV/√Hz
	MBI = 1, MPERF = 1		37		nV/√Hz
DIGITAL-TO-ANALOG CONVERTERS	DAC performance excludes mixers and headphone amplifier				
DAC Resolution	All DACs		24		Bits
Digital Attenuation Step			0.375		dB
Digital Attenuation Range			95		dB
DAC TO LINE OUTPUT					
Full-Scale Output Voltage (0 dB)	Scales linearly with AVDD		AVDD/3.3		V rms
	AVDD = 1.8 V		0.50 (1.41)		V rms (V p-p)
	AVDD = 3.3 V		0.92 (2.60)		V rms (V p-p)
Analog Volume Control Step	Line output volume control		0.75		dB
Analog Volume Control Range	Line output volume control	−57	1	+6	dB
Mute Attenuation			−87		dB
Dynamic Range	20 Hz to 20 kHz, −60 dB input, line output mode				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		96		dB
	AVDD = 3.3 V		101		dB
No Filter (RMS)	AVDD = 1.8 V		93.5		dB
	AVDD = 3.3 V		98		dB
Total Harmonic Distortion + Noise	−1 dBFS, line output mode				dB
	AVDD = 1.8 V		−90		dB
	AVDD = 3.3 V		−92		dB
Signal-to-Noise Ratio	Line output mode				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		96		dB
	AVDD = 3.3 V		101		dB
No Filter (RMS)	AVDD = 1.8 V		93.5		dB
	AVDD = 3.3 V		98		dB
Power Supply Rejection Ratio	CM capacitor = 20 µF				
	100 mV p-p @ 217 Hz		56		dB
	100 mV p-p @ 1 kHz		70		dB
Gain Error			3		%
Interchannel Gain Mismatch			0.005		dB
Offset Error			0		mV
Interchannel Isolation	1 kHz, 0 dBFS input signal		100		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DAC TO HEADPHONE/EARPIECE OUTPUT	P_O = output power per channel				
Full-Scale Output Voltage (0 dB)	Scales linearly with AVDD		AVDD/3.3		V rms
	AVDD = 1.8 V		0.50 (1.41)		V rms (V p-p)
	AVDD = 3.3 V		0.92 (2.60)		V rms (V p-p)
Total Harmonic Distortion + Noise	−4 dBFS				
16 Ω load	AVDD = 1.8 V, P_O = 6.4 mW		−76		dB
	AVDD = 3.3 V, P_O = 21.1 mW		−82		dB
32 Ω load	AVDD = 1.8 V, P_O = 3.8 mW		−82		dB
	AVDD = 3.3 V, P_O = 10.6 mW		−82		dB
Power Supply Rejection Ratio	CM capacitor = 20 µF				
	100 mV p-p @ 217 Hz		56		dB
	100 mV p-p @ 1 kHz		67		dB
Interchannel Isolation	1 kHz, 0 dBFS input signal, 32 Ω load, AVDD = 3.3 V				
	Referred to GND		73		dB
	Referred to CM (capless headphone mode)		50		dB
REFERENCE					
Common-Mode Reference Output	CM pin		AVDD/2		V

POWER SUPPLY SPECIFICATIONS

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLIES					
Voltage	DVDDOUT		1.56		V
	AVDD	1.8	3.3	3.65	V
	IOVDD	1.63	3.3	3.65	V
Digital I/O Current (IOVDD = 1.8 V)	20 pF capacitive load on all digital pins				
Slave Mode	f_S = 48 kHz		0.25		mA
	f_S = 96 kHz		0.48		mA
	f_S = 8 kHz		0.07		mA
Master Mode	f_S = 48 kHz		0.62		mA
	f_S = 96 kHz		1.23		mA
	f_S = 8 kHz		0.11		mA
Digital I/O Current (IOVDD = 3.3 V)	20 pF capacitive load on all digital pins				
Slave Mode	f_S = 48 kHz		0.48		mA
	f_S = 96 kHz		0.9		mA
	f_S = 8 kHz		0.13		mA
Master Mode	f_S = 48 kHz		1.51		mA
	f_S = 96 kHz		3		mA
	f_S = 8 kHz		0.27		mA
Analog Current (AVDD)	See Table 3				

TYPICAL CURRENT CONSUMPTION

Master clock = 12.288 MHz, input sample rate = 48 kHz, input tone = 1 kHz, normal power management settings, ADC input @ −1 dBFS, DAC input @ 0 dBFS. For total power consumption, add the IOVDD current listed in Table 2.

Table 3.

Operating Voltage	Audio Path	Clock Generation	Typical AVDD Current Consumption (mA)
AVDD = IOVDD = 3.3 V	Record stereo differential to ADC	Direct MCLK	5.24
		Integer PLL	6.57
	DAC stereo playback to line output (10 kΩ)	Direct MCLK	5.55
		Integer PLL	6.90
	DAC stereo playback to headphone (16 Ω)	Direct MCLK	55.5
		Integer PLL	56.8
	DAC stereo playback to headphone (32 Ω)	Direct MCLK	30.9
		Integer PLL	32.25
	DAC stereo playback to capless headphone (32 Ω)	Direct MCLK	56.75
		Integer PLL	58
	Record aux stereo bypass to line output (10 kΩ)	Direct MCLK	1.9
		Integer PLL	3.3
AVDD = IOVDD = 1.8 V	Record stereo differential to ADC	Direct MCLK	4.25
		Integer PLL	5.55
	DAC stereo playback to line output (10 kΩ)	Direct MCLK	4.7
		Integer PLL	5.7
	DAC stereo playback to headphone (16 Ω)	Direct MCLK	30.81
		Integer PLL	32
	DAC stereo playback to headphone (32 Ω)	Direct MCLK	18.3
		Integer PLL	19.5
	DAC stereo playback to capless headphone (32 Ω)	Direct MCLK	32.6
		Integer PLL	33.7
	Record aux stereo bypass to line output (10 kΩ)	Direct MCLK	1.9
		Integer PLL	3.07

TYPICAL POWER MANAGEMENT MEASUREMENTS

Master clock = 12.288 MHz, integer PLL, input sample rate = 48 kHz, input tone = 1 kHz. Pseudo-differential input to ADCs, DACs to line output with 10 kΩ load. ADC input @ −1 dBFS, DAC input @ 0 dBFS. In Table 4, the mixer boost and power management conditions are set for MXBIAS[1:0], ADCBIAS[1:0], HPBIAS[1:0], and DACBIAS[1:0]. RBIAS[1:0] and PBIAS[1:0] do not have an extreme power saving mode and are therefore set for power saving mode in the extreme power saving rows in Table 4.

Table 4.

Operating Voltage	Power Management Setting	Mixer Boost Setting	Typical AVDD Current Consumption (mA)	Typical ADC THD + N (dB)	Typical Line Output THD + N (dB)
AVDD = IOVDD = 3.3 V	Normal (default)	Normal operation	9.6	−91	−92.5
		Boost Level 1	9.75	−91.5	−92.5
		Boost Level 2	9.92	−91.5	−92.5
		Boost Level 3	10.25	−91.5	−92.5
	Extreme power saving	Normal operation	7.09	−84.5	−87
		Boost Level 1	7.19	−84.8	−87.1
		Boost Level 2	7.29	−84.8	−87.1
		Boost Level 3	7.49	−85	−87.1
	Power saving	Normal operation	7.67	−89.5	−90
		Boost Level 1	7.77	−89.5	−90
		Boost Level 2	7.86	−89.8	−90
		Boost Level 3	8.07	−89.8	−90
	Enhanced performance	Normal operation	10.55	−91	−93.5
		Boost Level 1	10.74	−91	−93.5
		Boost Level 2	10.93	−91	−93.5
		Boost Level 3	11.33	−91	−93.5
AVDD = IOVDD = 1.8 V	Normal (default)	Normal operation	8.1	−88	−91.2
		Boost Level 1	8.26	−88	−91.2
		Boost Level 2	8.41	−88	−91.2
		Boost Level 3	8.73	−88	−91.2
	Extreme power saving	Normal operation	5.73	−85	−86
		Boost Level 1	5.82	−85.4	−86
		Boost Level 2	5.91	−85.5	−86
		Boost Level 3	6.1	−85.5	−86
	Power saving	Normal operation	6.27	−86	−89.4
		Boost Level 1	6.36	−86.1	−89.5
		Boost Level 2	6.46	−86.3	−89.5
		Boost Level 3	6.65	−86.3	−89.5
	Enhanced performance	Normal operation	9.01	−88	−91.5
		Boost Level 1	9.2	−88	−91.5
		Boost Level 2	9.38	−88	−91.5
		Boost Level 3	9.76	−88	−91.5

DIGITAL FILTERS

Table 5.

Parameter	Mode	Factor	Min	Typ	Max	Unit
ADC DECIMATION FILTER	All modes, typ @ 48 kHz					
Pass Band		0.4375 f_S		21		kHz
Pass-Band Ripple				±0.015		dB
Transition Band		0.5 f_S		24		kHz
Stop Band		0.5625 f_S		27		kHz
Stop-Band Attenuation				67		dB
Group Delay		22.9844/f_S		479		µs
DAC INTERPOLATION FILTER						
Pass Band	48 kHz mode, typ @ 48 kHz	0.4535 f_S		22		kHz
	96 kHz mode, typ @ 96 kHz	0.3646 f_S		35		kHz
Pass-Band Ripple	48 kHz mode, typ @ 48 kHz				±0.01	dB
	96 kHz mode, typ @ 96 kHz				±0.05	dB
Transition Band	48 kHz mode, typ @ 48 kHz	0.5 f_S		24		kHz
	96 kHz mode, typ @ 96 kHz	0.5 f_S		48		kHz
Stop Band	48 kHz mode, typ @ 48 kHz	0.5465 f_S		26		kHz
	96 kHz mode, typ @ 96 kHz	0.6354 f_S		61		kHz
Stop-Band Attenuation	48 kHz mode, typ @ 48 kHz			69		dB
	96 kHz mode, typ @ 96 kHz			68		dB
Group Delay	48 kHz mode, typ @ 48 kHz	25/f_S		521		µs
	96 kHz mode, typ @ 96 kHz	11/f_S		115		µs

DIGITAL INPUT/OUTPUT SPECIFICATIONS

−40°C < T_A < +85°C, IOVDD = 3.3 V ± 10%.

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT SPECIFICATIONS					
Input Voltage High (V_{IH})		0.7 × IOVDD			V
Input Voltage Low (V_{IL})				0.3 × IOVDD	V
Input Leakage					
Pull-Ups/Pull-Downs Disabled	I_{IH} @ V_{IH} = 3.3 V	−0.17		+0.17	µA
	I_{IL} @ V_{IL} = 0 V	−0.17		+0.17	µA
	I_{IL} @ V_{IL} = 0 V (MCLK pin)	−13.5		−0.5	µA
Pull-Ups Enabled	I_{IH} @ V_{IH} = 3.3 V	−0.7		+0.7	µA
	I_{IL} @ V_{IL} = 0 V	−13.5		−0.5	µA
Pull-Downs Enabled	I_{IH} @ V_{IH} = 3.3 V	2.7		8.3	µA
	I_{IL} @ V_{IL} = 0 V	−0.18		+0.18	µA
Input Capacitance				5	pF
OUTPUT SPECIFICATIONS					
Output Voltage High (V_{OH})	I_{OH} = 2 mA @ 3.3 V, 0.85 mA @ 1.8 V	0.8 × IOVDD			V
Output Voltage Low (V_{OL})	I_{OL} = 2 mA @ 3.3 V, 0.85 mA @ 1.8 V			0.1 × IOVDD	V

DIGITAL TIMING SPECIFICATIONS

−40°C < T_A < +85°C, IOVDD = 3.3 V ± 10%.

Table 7. Digital Timing

Parameter	Limit		Unit	Description
	t_{MIN}	t_{MAX}		
MASTER CLOCK				
t_{MP}	74	488	ns	MCLK period, 256 × f_S mode.
t_{MP}	37	244	ns	MCLK period, 512 × f_S mode.
t_{MP}	24.7	162.7	ns	MCLK period, 768 × f_S mode.
t_{MP}	18.5	122	ns	MCLK period, 1024 × f_S mode.
SERIAL PORT				
t_{BIL}	5		ns	BCLK pulse width low.
t_{BIH}	5		ns	BCLK pulse width high.
t_{LIS}	5		ns	LRCLK setup. Time to BCLK rising.
t_{LIH}	5		ns	LRCLK hold. Time from BCLK rising.
t_{SIS}	5		ns	DAC_SDATA setup. Time to BCLK rising.
t_{SIH}	5		ns	DAC_SDATA hold. Time from BCLK rising.
t_{SODM}		50	ns	ADC_SDATA delay. Time from BCLK falling in master mode.
SPI PORT				
f_{CCLK}		10	MHz	CCLK frequency.
t_{CCPL}	10		ns	CCLK pulse width low.
t_{CCPH}	10		ns	CCLK pulse width high.
t_{CLS}	5		ns	$\overline{\text{CLATCH}}$ setup. Time to CCLK rising.
t_{CLH}	10		ns	$\overline{\text{CLATCH}}$ hold. Time from CCLK rising.
t_{CLPH}	10		ns	$\overline{\text{CLATCH}}$ pulse width high.
t_{CDS}	5		ns	CDATA setup. Time to CCLK rising.
t_{CDH}	5		ns	CDATA hold. Time from CCLK rising.
t_{COD}		50	ns	COUT three-stated. Time from $\overline{\text{CLATCH}}$ rising.
I²C PORT				
f_{SCL}		400	kHz	SCL frequency.
t_{SCLH}	0.6		µs	SCL high.
t_{SCLL}	1.3		µs	SCL low.
t_{SCS}	0.6		µs	Setup time; relevant for repeated start condition.
t_{SCH}	0.6		µs	Hold time. After this period, the first clock is generated.
t_{DS}	100		ns	Data setup time.
t_{SCR}		300	ns	SCL rise time.
t_{SCF}		300	ns	SCL fall time.
t_{SDR}		300	ns	SDA rise time.
t_{SDF}		300	ns	SDA fall time.
t_{BFT}	0.6		µs	Bus-free time. Time between stop and start.
DIGITAL MICROPHONE				R_{LOAD} = 1 MΩ, C_{LOAD} = 14 pF.
t_{DCF}		10	ns	Digital microphone clock fall time.
t_{DCR}		10	ns	Digital microphone clock rise time.
t_{DDV}	22	30	ns	Digital microphone delay time for valid data.
t_{DDH}	0	12	ns	Digital microphone delay time for data three-stated.

DIGITAL TIMING DIAGRAMS

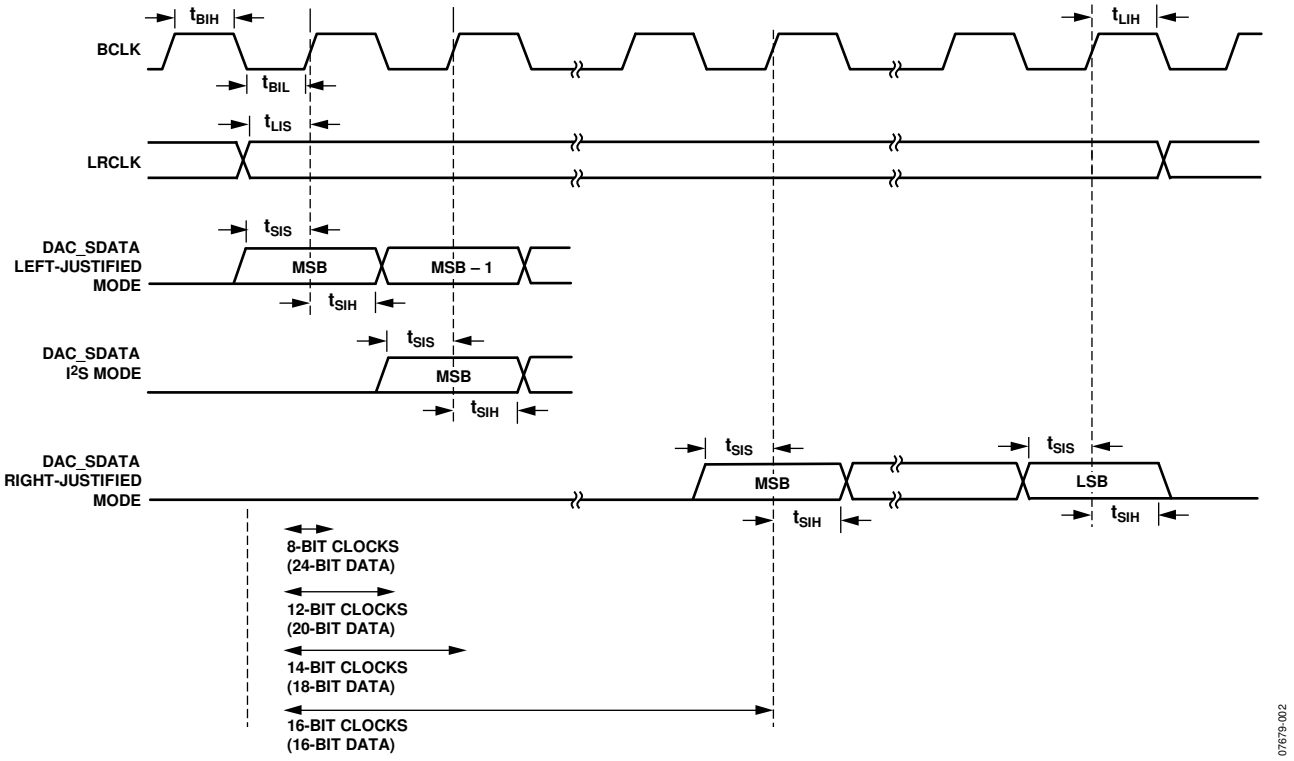

Figure 2. Serial Input Port Timing

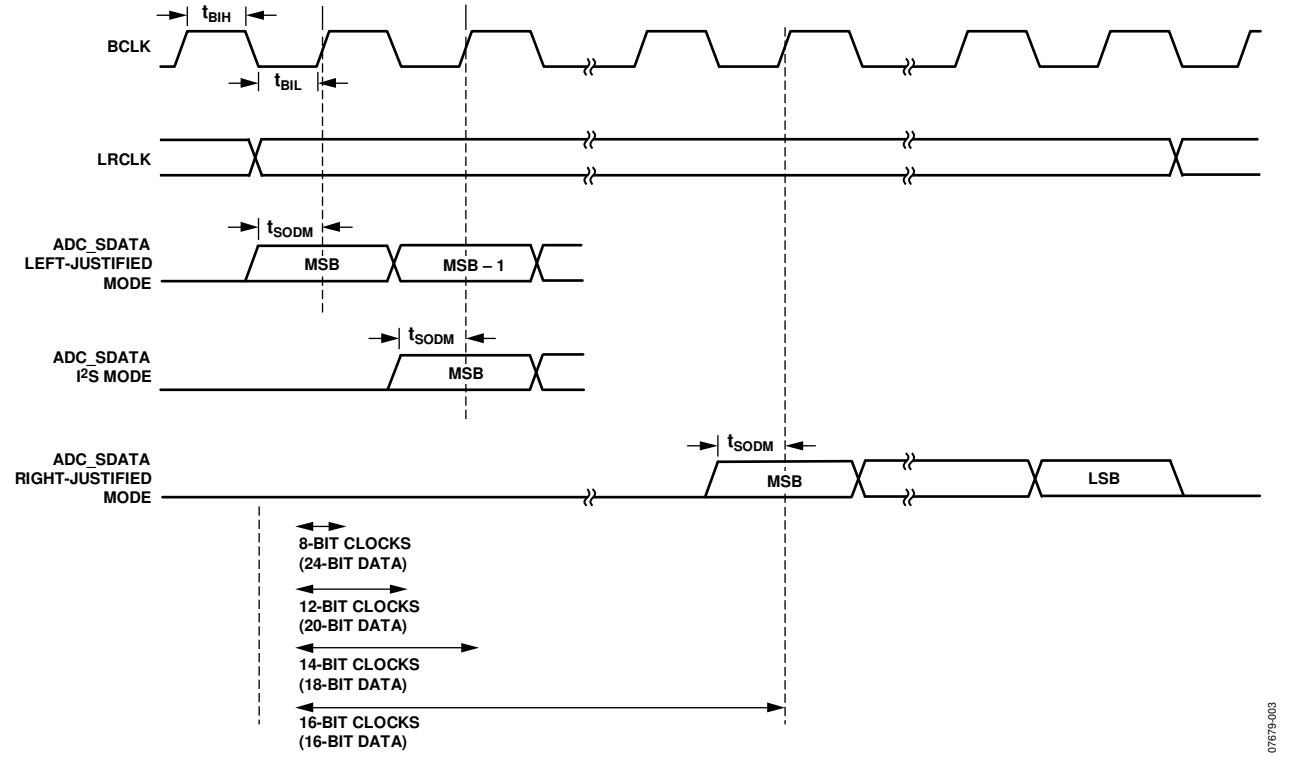

Figure 3. Serial Output Port Timing

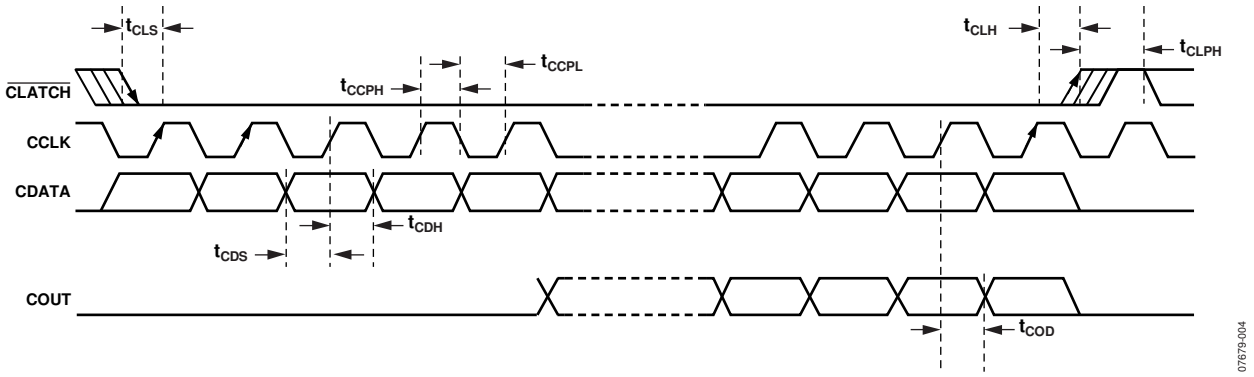

Figure 4. SPI Port Timing

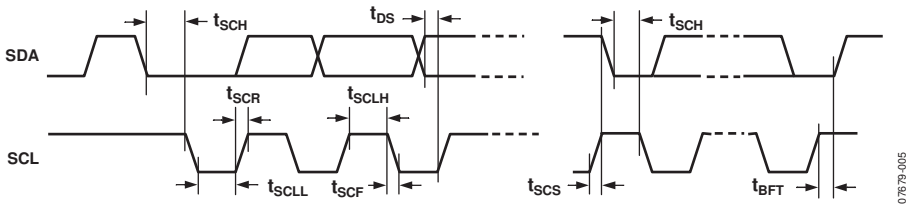

Figure 5. I²C Port Timing

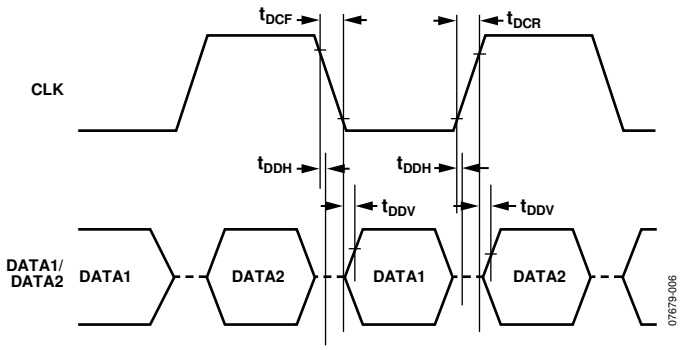

Figure 6. Digital Microphone Timing

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Power Supply (AVDD)	−0.3 V to +3.65 V
Input Current (Except Supply Pins)	±20 mA
Analog Input Voltage (Signal Pins)	−0.3 V to AVDD + 0.3 V
Digital Input Voltage (Signal Pins)	−0.3 V to IOVDD + 0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} represents thermal resistance, junction-to-ambient; θ_{JC} represents thermal resistance, junction-to-case. All characteristics are for a 4-layer board.

Table 9. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP	50.1	17	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

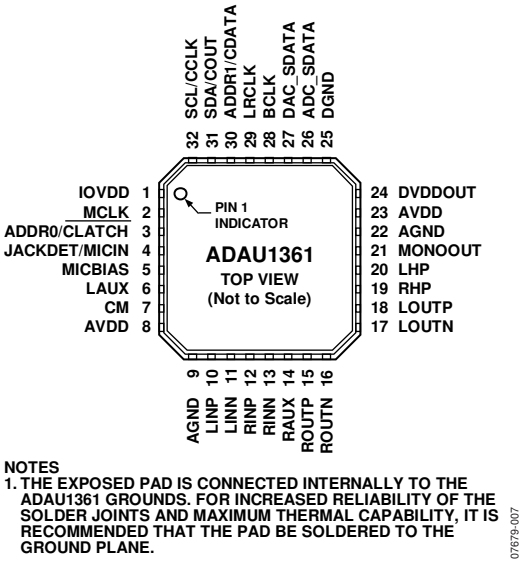

Figure 7. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	IOVDD	PWR	Supply for Digital Input and Output Pins. The digital output pins are supplied from IOVDD, which also sets the highest input voltage that should be seen on the digital input pins. IOVDD should be set between 1.8 V and 3.3 V. The current draw of this pin is variable because it is dependent on the loads of the digital outputs. IOVDD should be decoupled to DGND with a 100 nF capacitor and a 10 µF capacitor.
2	MCLK	D_IN	External Master Clock Input.
3	ADDR0/$\overline{\text{CLATCH}}$	D_IN	I^2C Address Bit 0 (ADDR0). SPI Latch Signal ($\overline{\text{CLATCH}}$). Must go low at the beginning of an SPI transaction and high at the end of a transaction. Each SPI transaction can take a different number of CCLKs to complete, depending on the address and read/write bit that are sent at the beginning of the SPI transaction.
4	JACKDET/MICIN	D_IN	Detect Insertion/Removal of Headphone Plug (JACKDET). Digital Microphone Stereo Input (MICIN).
5	MICBIAS	A_OUT	Bias Voltage for Electret Microphone.
6	LAUX	A_IN	Left Channel Single-Ended Auxiliary Input. Biased at AVDD/2.
7	CM	A_OUT	AVDD/2 V Common-Mode Reference. A 10 µF to 47 µF standard decoupling capacitor should be connected between this pin and AGND to reduce crosstalk between the ADCs and DACs. This pin can be used to bias external analog circuits, as long as they are not drawing current from CM (for example, the noninverting input of an op amp).
8	AVDD	PWR	1.8 V to 3.65 V Analog Supply for DAC and Microphone Bias. This pin should be decoupled locally to AGND with a 100 nF capacitor.
9	AGND	PWR	Analog Ground. The AGND and DGND pins can be tied together on a common ground plane. AGND should be decoupled locally to AVDD with a 100 nF capacitor.
10	LINP	A_IN	Left Channel Noninverting Input or Single-Ended Input 0. Biased at AVDD/2.
11	LINN	A_IN	Left Channel Inverting Input or Single-Ended Input 1. Biased at AVDD/2.
12	RINP	A_IN	Right Channel Noninverting Input or Single-Ended Input 2. Biased at AVDD/2.
13	RINN	A_IN	Right Channel Inverting Input or Single-Ended Input 3. Biased at AVDD/2.
14	RAUX	A_IN	Right Channel Single-Ended Auxiliary Input. Biased at AVDD/2.
15	ROUTP	A_OUT	Right Line Output, Positive. Biased at AVDD/2.
16	ROUTN	A_OUT	Right Line Output, Negative. Biased at AVDD/2.
17	LOUTN	A_OUT	Left Line Output, Negative. Biased at AVDD/2.
18	LOUTP	A_OUT	Left Line Output, Positive. Biased at AVDD/2.

Pin No.	Mnemonic	Type[1]	Description
19	RHP	A_OUT	Right Headphone Output. Biased at AVDD/2.
20	LHP	A_OUT	Left Headphone Output. Biased at AVDD/2.
21	MONOOUT	A_OUT	Mono Output or Virtual Ground for Capless Headphone. Biased at AVDD/2 when set as mono output.
22	AGND	PWR	Analog Ground. The AGND and DGND pins can be tied together on a common ground plane. AGND should be decoupled locally to AVDD with a 100 nF capacitor.
23	AVDD	PWR	1.8 V to 3.3 V Analog Supply for ADC, Output Driver, and Input to Digital Supply Regulator. This pin should be decoupled locally to AGND with a 100 nF capacitor.
24	DVDDOUT	PWR	Digital Core Supply Decoupling Point. The digital supply is generated from an on-board regulator and does not require an external supply. DVDDOUT should be decoupled to DGND with a 100 nF capacitor and a 10 µF capacitor.
25	DGND	PWR	Digital Ground. The AGND and DGND pins can be tied together on a common ground plane. DGND should be decoupled to DVDDOUT and to IOVDD with 100 nF capacitors and 10 µF capacitors.
26	ADC_SDATA	D_OUT	ADC Serial Output Data.
27	DAC_SDATA	D_IN	DAC Serial Input Data.
28	BCLK	D_IO	Serial Data Port Bit Clock.
29	LRCLK	D_IO	Serial Data Port Frame Clock.
30	ADDR1/CDATA	D_IN	I^2C Address Bit 1 (ADDR1). SPI Data Input (CDATA).
31	SDA/COUT	D_IO	I^2C Data (SDA). This pin is a bidirectional open-collector input/output. The line connected to this pin should have a 2 kΩ pull-up resistor. SPI Data Output (COUT). This pin is used for reading back registers and memory locations. It is three-state when an SPI read is not active.
32	SCL/CCLK	D_IN	I^2C Clock (SCL). This pin is always an open-collector input when in I^2C control mode. The line connected to this pin should have a 2 kΩ pull-up resistor. SPI Clock (CCLK). This pin can run continuously or be gated off between SPI transactions.
EP	Exposed Pad		Exposed Pad. The exposed pad is connected internally to the ADAU1361 grounds. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the ground plane. See the Exposed Pad PCB Design section for more information.

[1] A_IN = analog input, A_OUT = analog output, D_IN = digital input, D_IO = digital input/output, D_OUT = digital output, PWR = power.

TYPICAL PERFORMANCE CHARACTERISTICS

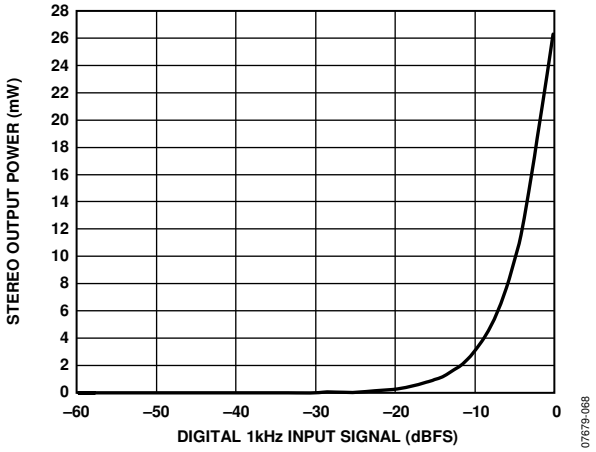

Figure 8. Headphone Amplifier Power vs. Input Level, 16 Ω Load

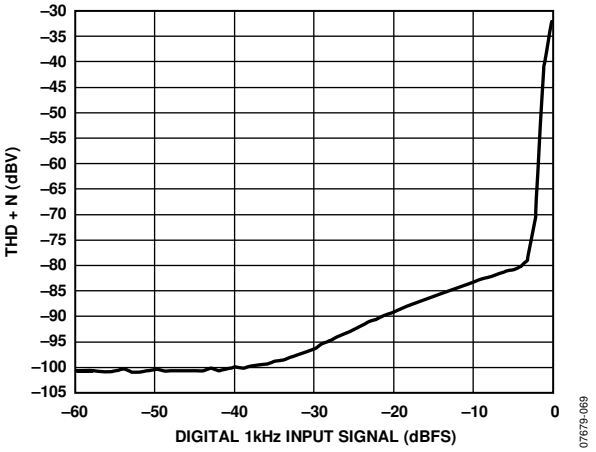

Figure 11. Headphone Amplifier THD + N vs. Input Level, 16 Ω Load

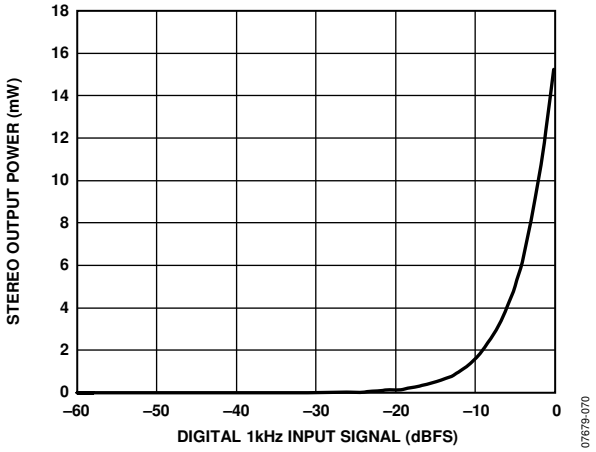

Figure 9. Headphone Amplifier Power vs. Input Level, 32 Ω Load

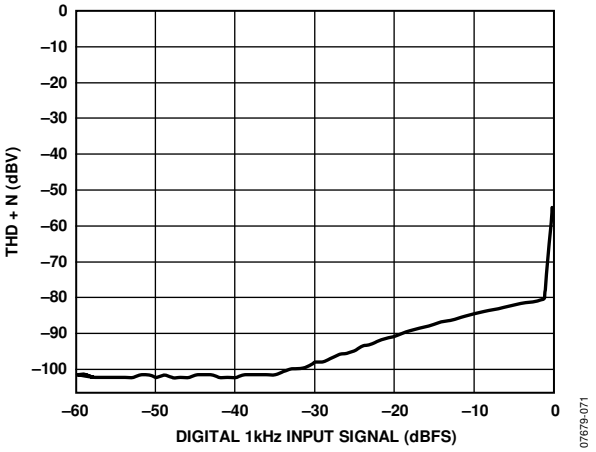

Figure 12. Headphone Amplifier THD + N vs. Input Level, 32 Ω Load

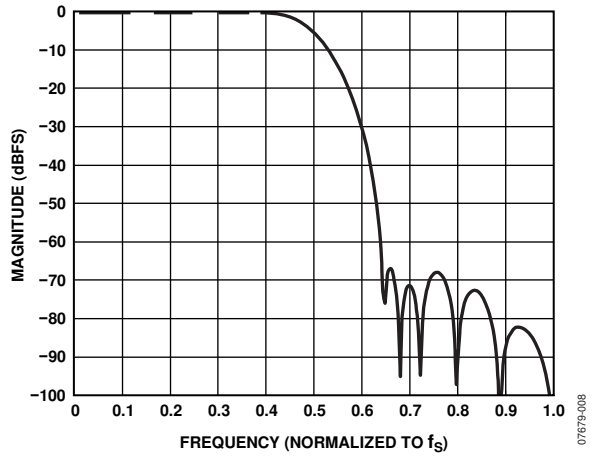

Figure 10. ADC Decimation Filter, 64× Oversampling, Normalized to f_S

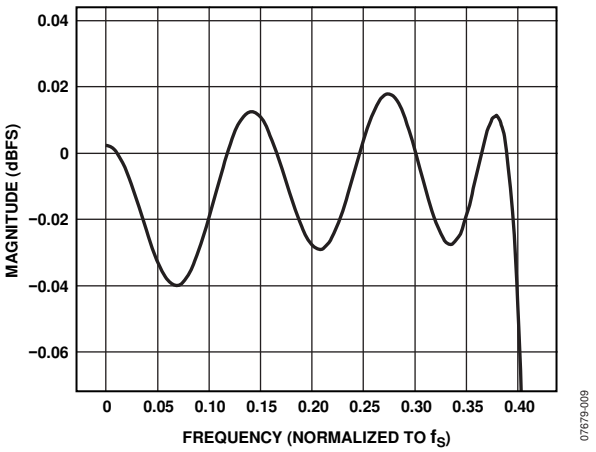

Figure 13. ADC Decimation Filter Pass-Band Ripple, 64× Oversampling, Normalized to f_S

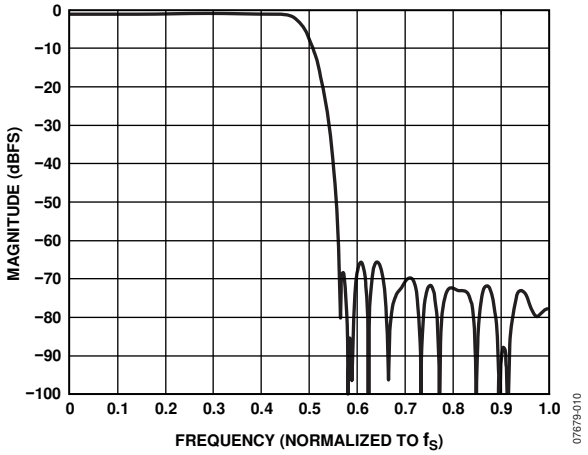

Figure 14. ADC Decimation Filter, 128× Oversampling, Normalized to f_S

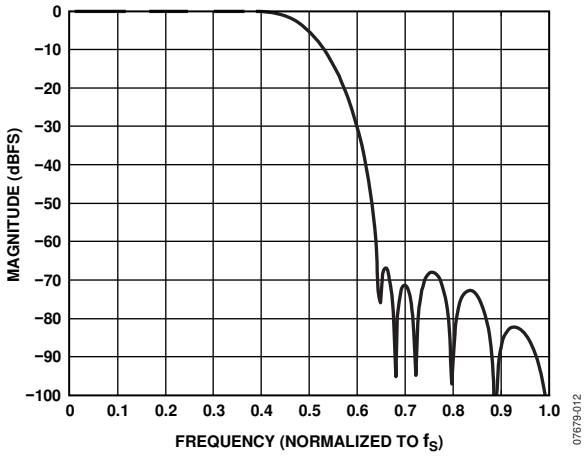

Figure 15. ADC Decimation Filter, 128× Oversampling, Double-Rate Mode, Normalized to f_S

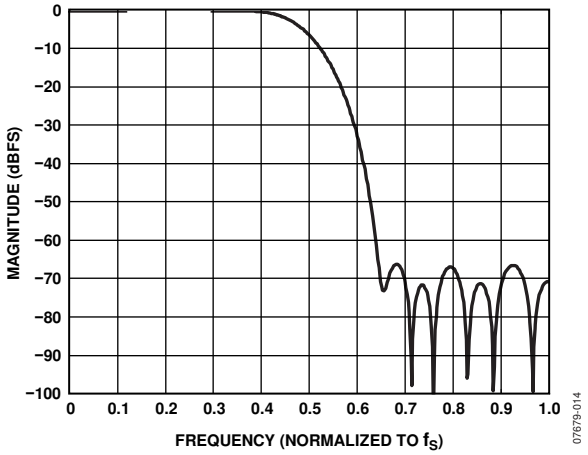

Figure 16. DAC Interpolation Filter, 64× Oversampling, Double-Rate Mode, Normalized to f_S

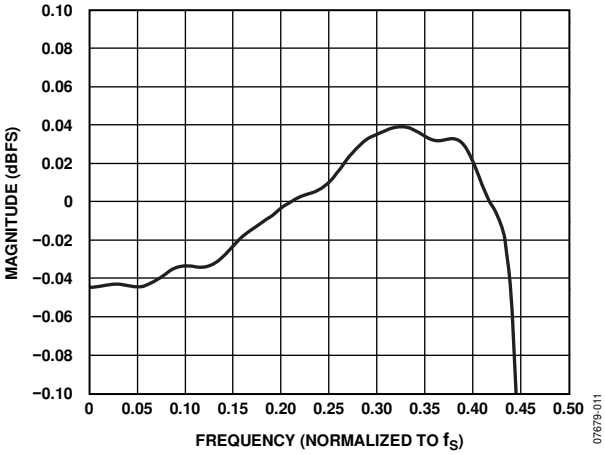

Figure 17. ADC Decimation Filter Pass-Band Ripple, 128× Oversampling, Normalized to f_S

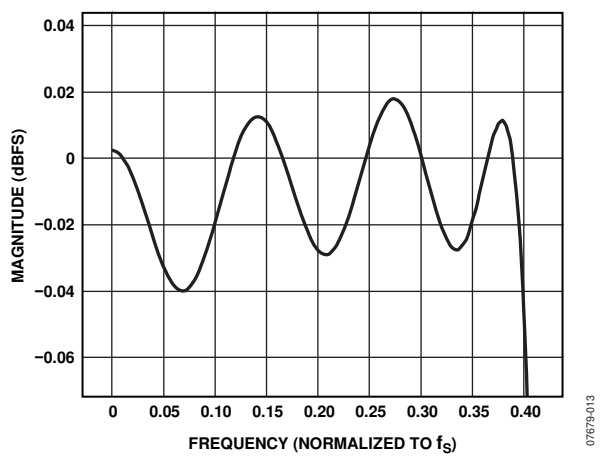

Figure 18. ADC Decimation Filter Pass-Band Ripple, 128× Oversampling, Double-Rate Mode, Normalized to f_S

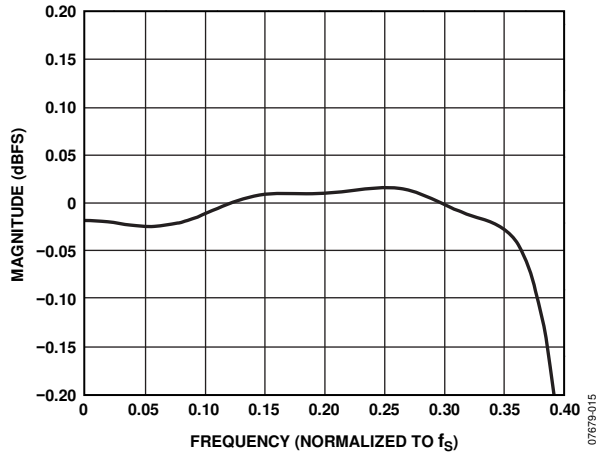

Figure 19. DAC Interpolation Filter Pass-Band Ripple, 64× Oversampling, Double-Rate Mode, Normalized to f_S

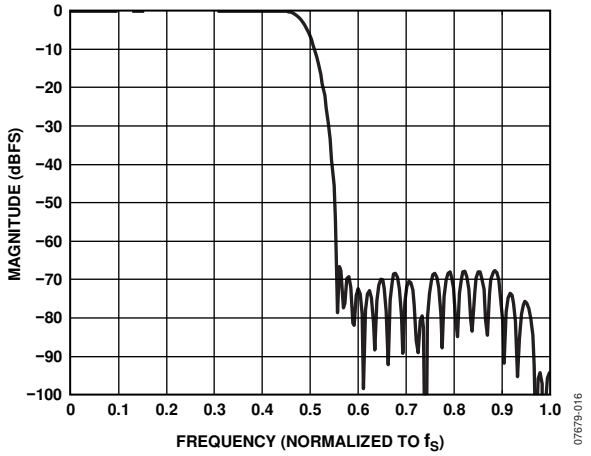

Figure 20. DAC Interpolation Filter, 128× Oversampling, Normalized to f_S

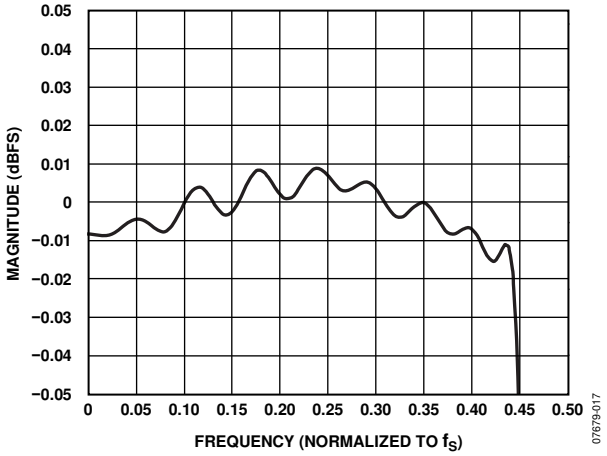

Figure 23. DAC Interpolation Filter Pass-Band Ripple, 128× Oversampling, Normalized to f_S

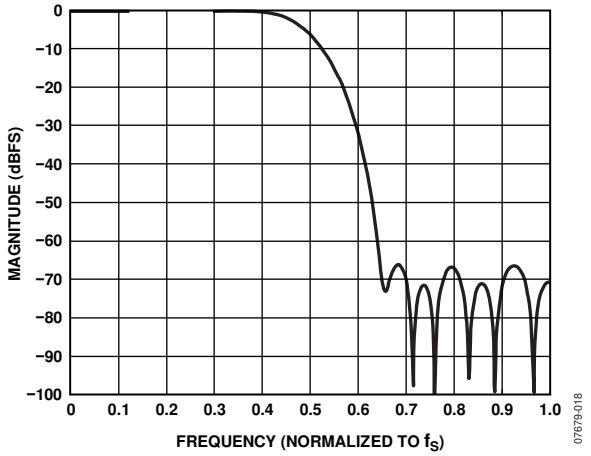

Figure 21. DAC Interpolation Filter, 128× Oversampling, Double-Rate Mode, Normalized to f_S

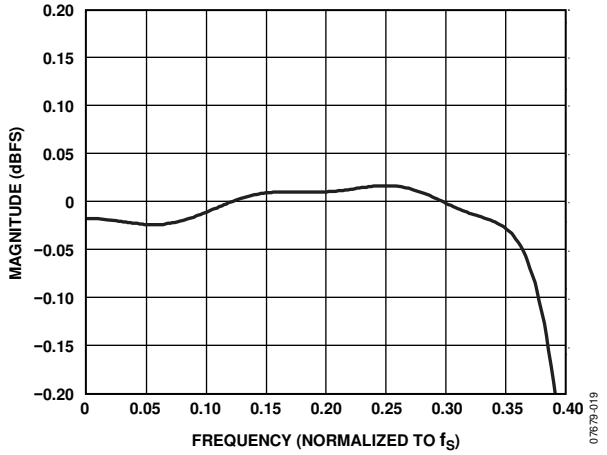

Figure 24. DAC Interpolation Filter Pass-Band Ripple, 128× Oversampling, Double-Rate Mode, Normalized to f_S

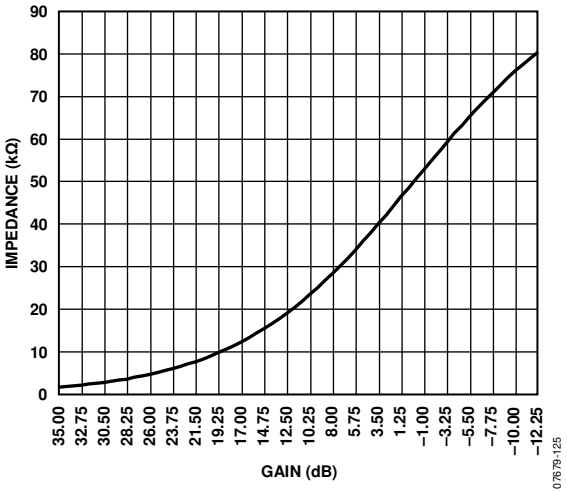

Figure 22. Input Impedance vs. Gain for Analog Inputs

SYSTEM BLOCK DIAGRAMS

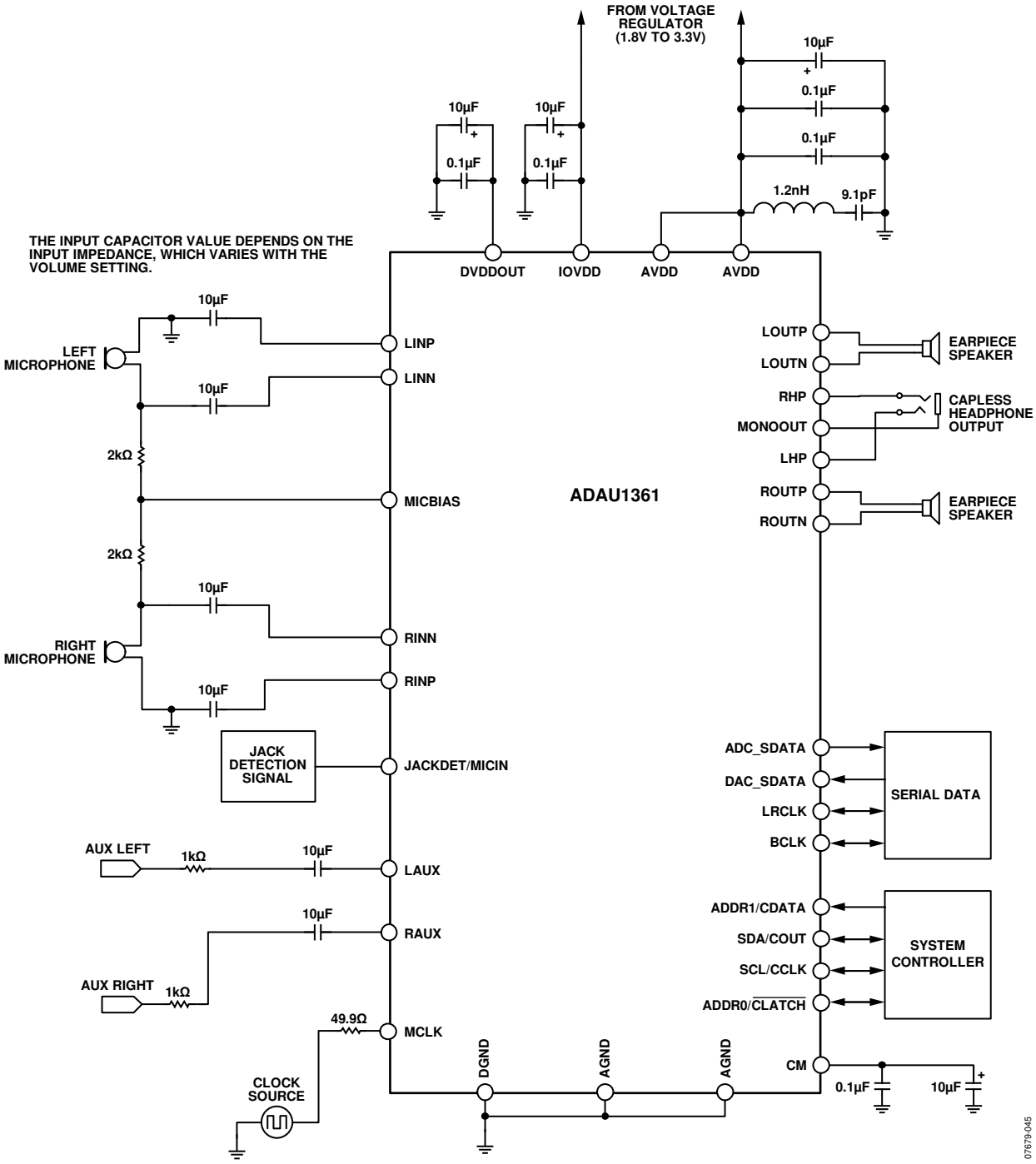

Figure 25. System Block Diagram

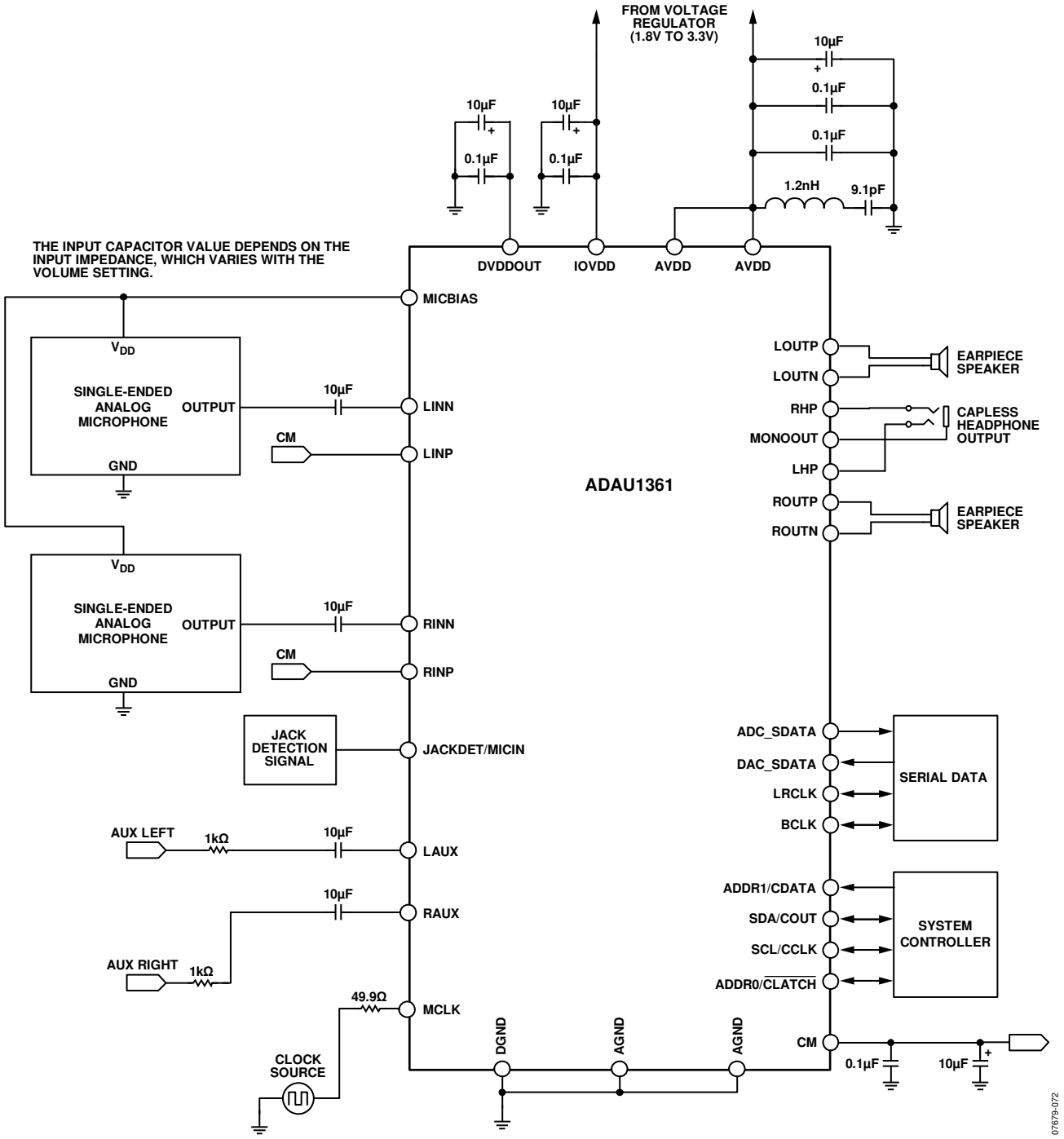

Figure 26. System Block Diagram with Analog Microphones

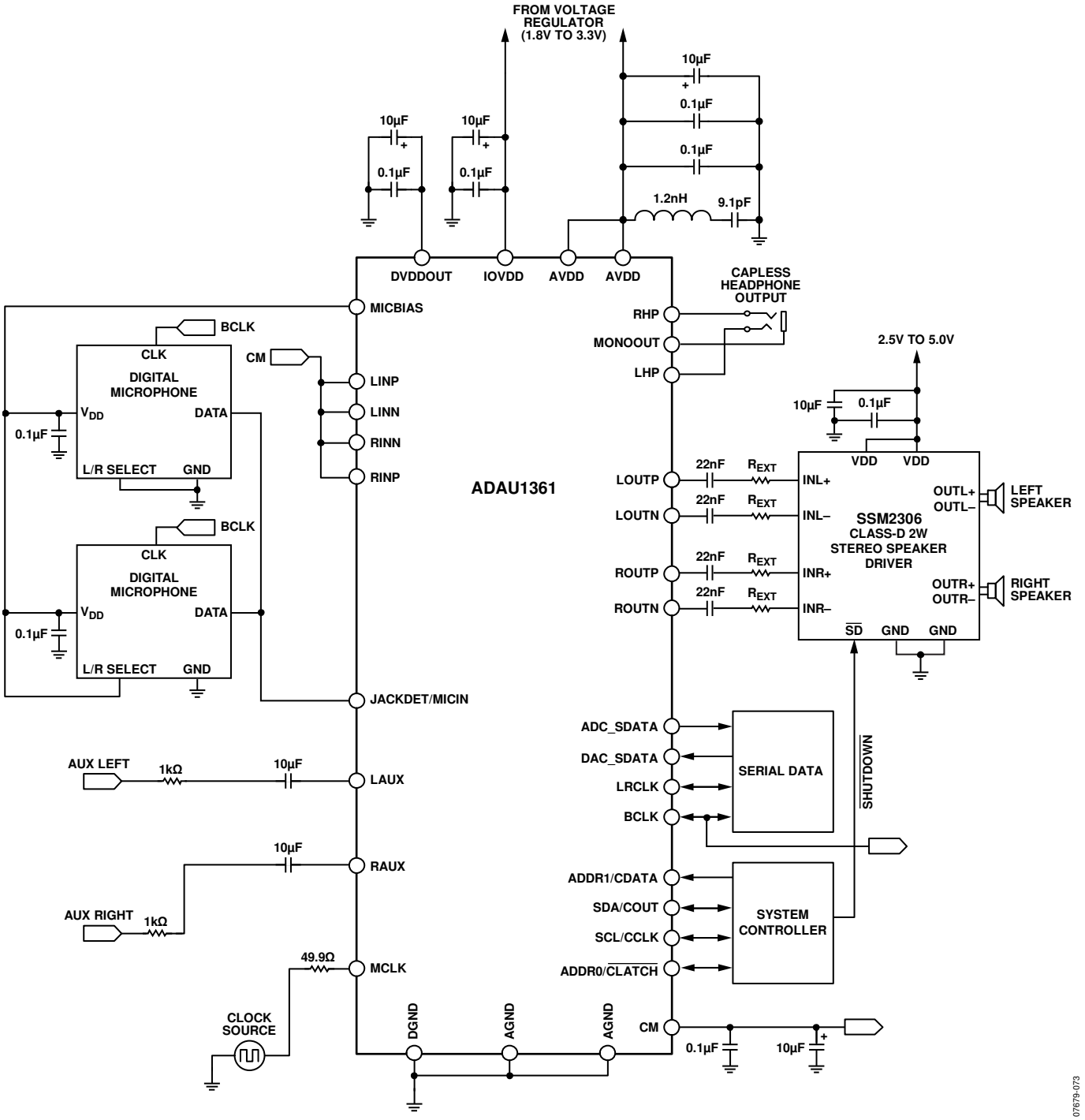

Figure 27. System Block Diagram with Digital Microphones and SSM2306 Class-D Speaker Driver

THEORY OF OPERATION

The ADAU1361 is an audio codec that offers high quality audio, low power, and small package size. The stereo ADC and stereo DAC each have an SNR of at least +98 dB and a THD + N of at least −90 dB. The serial data port is compatible with I²S, left-justified, right-justified, and TDM modes for interfacing to digital audio data. The operating voltage range is 1.8 V to 3.65 V, with an on-board regulator generating the internal digital supply voltage.

The record signal path includes very flexible input configurations that can accept differential and single-ended analog microphone inputs as well as a digital microphone input. A microphone bias pin provides seamless interfacing to electret microphones. Input configurations can accept up to six single-ended analog signals or variations of stereo differential or stereo single-ended signals with two additional auxiliary single-ended inputs. Each input signal has its own programmable gain amplifier (PGA) for volume adjustment and can be routed directly to the playback path output mixers, bypassing the ADCs. An automatic level control (ALC) can also be implemented to keep the recording volume constant.

The ADCs and DACs are high quality, 24-bit Σ-Δ converters that operate at selectable 64× or 128× oversampling ratios. The base sampling rate of the converters is set by the input clock rate and can be further scaled with the converter control register settings. The converters can operate at sampling frequencies from 8 kHz to 96 kHz. The ADCs and DACs also include very fine-step digital volume controls.

The playback path allows input signals and DAC outputs to be mixed into various output configurations. Headphone drivers are available for a stereo headphone output, and the other output pins are capable of differentially driving an earpiece speaker. Capless headphone outputs are possible with the use of the mono output as a virtual ground connection. The stereo line outputs can be used as either single-ended or differential outputs and as an optional mix-down mono output.

The ADAU1361 can generate its internal clocks from a wide range of input clocks by using the on-board fractional PLL. The PLL accepts inputs from 8 MHz to 27 MHz.

The ADAU1361 is provided in a small, 32-lead, 5 mm × 5 mm LFCSP with an exposed bottom pad.

STARTUP, INITIALIZATION, AND POWER

This section describes the procedure for properly starting up the ADAU1361. The following sequence provides a high level approach to the proper initiation of the system.

1. Apply power to the ADAU1361.
2. Lock the PLL to the input clock (if using the PLL).
3. Enable the core clock.
4. Load the register settings.

POWER-UP SEQUENCE

The ADAU1361 uses a power-on reset (POR) circuit to reset the registers upon power-up. The POR monitors the DVDDOUT pin and generates a reset signal whenever power is applied to the chip. During the reset, the ADAU1361 is set to the default values documented in the register map (see the Control Registers section). Typically, with a 10 µF capacitor on AVDD, the POR takes approximately 14 ms.

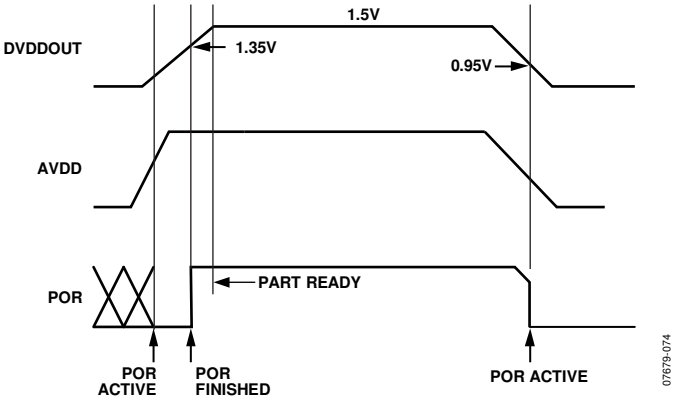

Figure 28. Power-On Reset Sequence

The PLL lock time is dependent on the MCLK rate. Typical lock times are provided in Table 11.

Table 11. PLL Lock Times

PLL Mode	MCLK Frequency	Lock Time (Typical)
Fractional	8 MHz	3.5 ms
Fractional	12 MHz	3.0 ms
Integer	12.288 MHz	2.96 ms
Fractional	13 MHz	2.4 ms
Fractional	14.4 MHz	2.4 ms
Fractional	19.2 MHz	2.98 ms
Fractional	19.68 MHz	2.98 ms
Fractional	19.8 MHz	2.98 ms
Fractional	24 MHz	2.95 ms
Integer	24.576 MHz	2.96 ms
Fractional	26 MHz	2.4 ms
Fractional	27 MHz	2.4 ms

POWER REDUCTION MODES

Sections of the ADAU1361 chip can be turned on and off as needed to reduce power consumption. These include the ADCs, the DACs, and the PLL.

In addition, the control registers can be used to configure some functions for power saving, normal, or enhanced performance operation. See the Control Registers section for more information.

The digital filters of the ADCs and DACs can each be set to oversampling ratios of 64× or 128× (default). Setting the oversampling ratios to 64× for these filters lowers power consumption with a minimal impact on performance. See the Digital Filters section for specifications; see the Typical Performance Characteristics section for graphs of these filters.

DIGITAL POWER SUPPLY

The digital power supply for the ADAU1361 is generated from an internal regulator. This regulator generates a 1.5 V supply internally. The only external connection to this regulator is the DVDDOUT bypassing point. A 100 nF capacitor and a 10 µF capacitor should be connected between this pin and DGND.

INPUT/OUTPUT POWER SUPPLY

The power for the digital output pins is supplied from IOVDD, and this pin also sets the highest input voltage that should be seen on the digital input pins. IOVDD should be set between 1.8 V and 3.3 V; no digital input signal should be at a voltage level higher than the one on IOVDD. The current draw of this pin is variable because it depends on the loads of the digital outputs. IOVDD should be decoupled to DGND with a 100 nF capacitor and a 10 µF capacitor.

CLOCK GENERATION AND MANAGEMENT

The ADAU1361 uses a flexible clocking scheme that enables the use of many different input clock rates. The PLL can be bypassed or used, resulting in two different approaches to clock management. For more information about clocking schemes, PLL configuration, and sampling rates, see the Clocking and Sampling Rates section.

Case 1: PLL Is Bypassed

If the PLL is bypassed, the core clock is derived directly from the MCLK input. The rate of this clock must be set properly in Register R0 (clock control register, Address 0x4000) using the INFREQ[1:0] bits. When the PLL is bypassed, supported external clock rates are 256 × f_S, 512 × f_S, 768 × f_S, and 1024 × f_S, where f_S is the base sampling rate. The core clock of the chip is off until the core clock enable bit (COREN) is asserted.