Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Quad ADC, Dual DAC, Low Latency, Low Power Codec

Data Sheet

ADAU1372

FEATURES

- Low latency, 24-bit ADCs and DACs
  - 102 dB SNR (through PGA and ADC with A-weighted filter)
  - 107 dB dynamic range (through DAC and headphone with A-weighted filter)
- Serial port sample rates from 8 kHz to 192 kHz
- 4 single-ended analog inputs, configurable as microphone or line inputs
- Dual stereo digital microphone inputs
- Stereo analog audio output, single-ended or differential, configurable as either line output or headphone driver
- PLL supporting any input clock rate from 8 MHz to 27 MHz
- Full-duplex, asynchronous sample rate converters (ASRCs)
- Power supplies
  - Analog and digital input/output of 1.8 V to 3.3 V
- Low power (15.5 mW)
- I²C and SPI control interfaces for flexibility
- 5 multipurpose pins supporting dual stereo digital microphone inputs, mute, push-button volume controls

APPLICATIONS

- Handsets, headsets, and headphones
- Bluetooth® handsets, headsets, and headphones
- Personal navigation devices
- Digital still and video cameras

GENERAL DESCRIPTION

The ADAU1372 is a codec with four inputs and two outputs, which incorporates asynchronous sample rate converters. Optimized for low latency and low power, the ADAU1372 is ideal for headsets, handsets, and headphones. The ADAU1372 has built-in programmable gain amplifiers (PGAs); thus, with the addition of just a few passive components and a crystal, the ADAU1372 provides a solution for headset audio needs, microphone preamplifiers, ADCs, DACs, headphone amplifiers, and serial ports for connections to an external DSP.

Note that throughout this data sheet, multifunction pins, such as SCL/SCLK, are referred to either by the entire pin name or by a single function of the pin, for example, SCLK, when only that function is relevant.

FUNCTIONAL BLOCK DIAGRAM

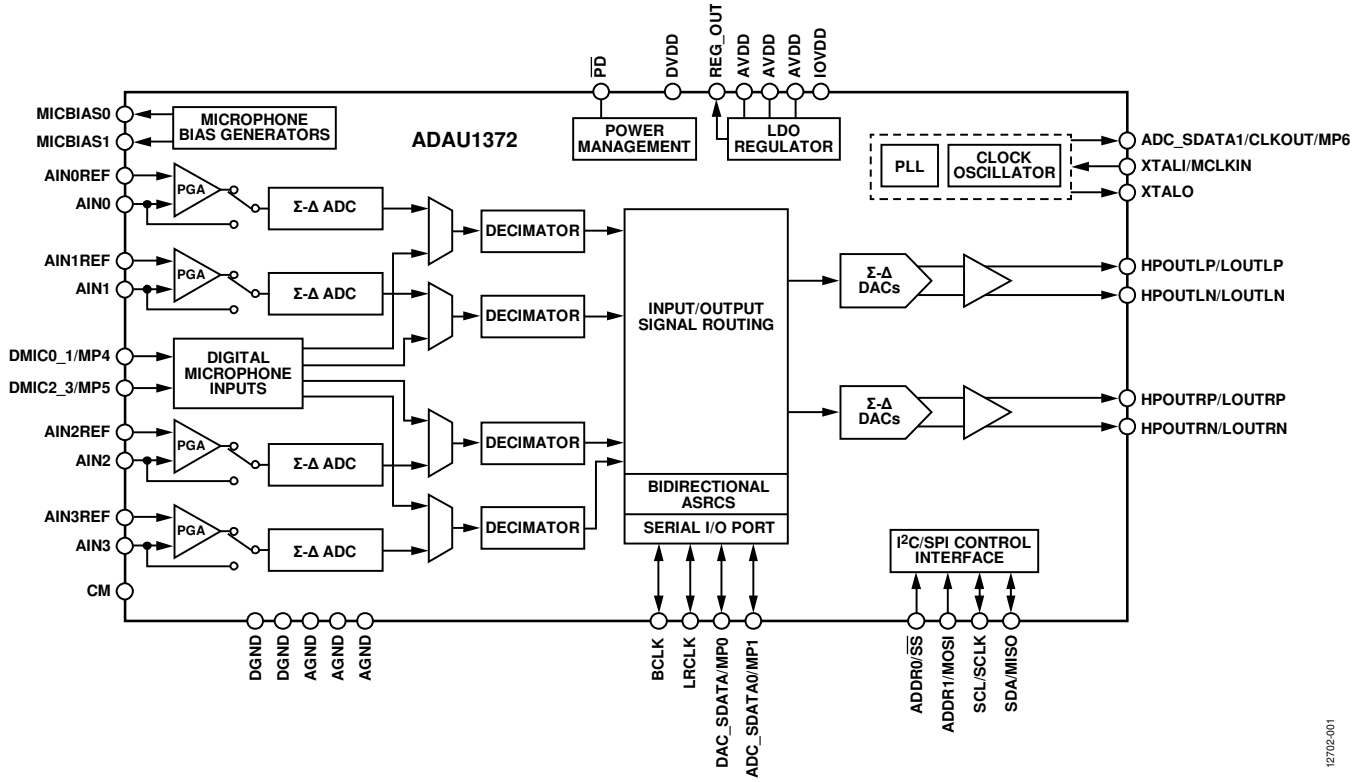

Figure 1.

Rev. 0 **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 ©2014 Analog Devices, Inc. All rights reserved.
Technical Support www.analog.com

ADAU1372* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADAU1372 Evaluation Board

DOCUMENTATION

Data Sheet

- ADAU1372: Quad ADC, Dual DAC, Low Latency, Low Power Codec

User Guides

- UG-807: Evaluating the ADAU1372 Quad ADC, Dual DAC, Low Latency, Low Power Codec

TOOLS AND SIMULATIONS

- ADAU1372 IBIS Model

DESIGN RESOURCES

- ADAU1372 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADAU1372 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

12/14—Revision 0: Initial Version

SPECIFICATIONS

Master clock = 12.288 MHz, serial input sample rate = 48 kHz, measurement bandwidth = 20 Hz to 20 kHz, word width = 24 bits, ambient temperature = 25°C, outputs line loaded with 10 kΩ.

ANALOG PERFORMANCE SPECIFICATIONS

Supply voltages AVDD = IOVDD = 1.8 V, DVDD = 1.1 V, unless otherwise noted, PLL disabled, direct master clock.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTERS (ADCs)					
ADC Resolution	All ADCs		24		Bits
Digital Attenuation Step			0.375		dB
Digital Attenuation Range			95		dB
INPUT RESISTANCE	Gain settings do not include 10 dB gain from PGA_x_BOOST settings; this additional gain does not affect input impedance; PGA_POP_DISx = 1				
Single-Ended Line Input	0 dB gain		14.3		kΩ
PGA Inputs	−12 dB gain		32.0		kΩ
	0 dB gain		20		kΩ
	+35.25 dB gain		0.68		kΩ
SINGLE-ENDED LINE INPUT	PGA_ENx = 0, PGA_x_BOOST = 0, PGA_POP_DISx = 1				
Full-Scale Input Voltage	Scales linearly with AVDD		AVDD/3.63		V rms
	AVDD = 1.8 V		0.49		V rms
	AVDD = 1.8 V		1.38		V p-p
	AVDD = 3.3 V		0.90		V rms
	AVDD = 3.3 V		2.54		V p-p
Dynamic Range[1]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		97		dB
	AVDD = 3.3 V		102		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V		94		dB
	AVDD = 3.3 V		99		dB
Signal-to-Noise Ratio (SNR)[2]					
With A-Weighted Filter (RMS)	AVDD = 1.8 V		98		dB
	AVDD = 3.3 V		103		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V		96		dB
	AVDD = 3.3 V		100		dB
Interchannel Gain Mismatch			40		mdB
Total Harmonic Distortion + Noise (THD + N)	20 Hz to 20 kHz, −1 dBFS input				
	AVDD = 1.8 V		−90		dB
	AVDD = 3.3 V		−94		dB
Offset Error			±0.1		mV
Gain Error			±0.2		dB
Interchannel Isolation	CM capacitor = 22 µF		100		dB
Power Supply Rejection Ratio (PSRR)	CM capacitor = 22 µF, 100 mV p-p at 1 kHz		55		dB
SINGLE-ENDED PGA INPUT	PGA_ENx = 1, PGA_x_BOOST = 0				
Full-Scale Input Voltage	Scales linearly with AVDD		AVDD/3.63		V rms
	AVDD = 1.8 V		0.49		V rms
	AVDD = 1.8 V		1.38		V p-p
	AVDD = 3.3 V		0.90		V rms
	AVDD = 3.3 V		2.54		V p-p
Dynamic Range[1]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		96		dB
	AVDD = 3.3 V		102		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V		94		dB
	AVDD = 3.3 V		99		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
THD + N	20 Hz to 20 kHz, −1 dBFS input				
	AVDD = 1.8 V		−88		dB
	AVDD = 3.3 V		−90		dB
SNR[2]					
With A-Weighted Filter (RMS)	AVDD = 1.8 V		96		dB
	AVDD = 3.3 V		102		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V		94		dB
	AVDD = 3.3 V		99		dB
PGA Gain Variation					
With −12 dB Setting	Standard deviation		0.05		dB
With +35.25 dB Setting	Standard deviation		0.15		dB
PGA Boost	PGA_x_BOOST		10		dB
PGA Mute Attenuation	PGA_MUTEx		−65		dB
Interchannel Gain Mismatch			0.005		dB
Offset Error			0		mV
Gain Error			±0.2		dB
Interchannel Isolation			83		dB
PSRR	CM capacitor = 22 µF, 100 mV p-p at 1 kHz		63		dB
MICROPHONE BIAS	MIC_ENx = 1				
Bias Voltage					
0.65 × AVDD	AVDD = 1.8 V, MIC_GAINx = 1		1.16		V
	AVDD = 3.3 V, MIC_GAINx = 1		2.12		V
0.90 × AVDD	AVDD = 1.8 V, MIC_GAINx = 0		1.63		V
	AVDD = 3.3 V, MIC_GAINx = 0		2.97		V
Bias Current Source				3	mA
Output Impedance			1		Ω
MICBIASx Isolation	MIC_GAINx = 0		95		dB
	MIC_GAINx = 1		99		dB
Noise in the Signal Bandwidth[3]	20 Hz to 20 kHz				
AVDD = 1.8 V					
	MIC_GAINx = 0		27		nV/√Hz
	MIC_GAINx = 1		16		nV/√Hz
AVDD = 3.3 V					
	MIC_GAINx = 0		35		nV/√Hz
	MIC_GAINx = 1		19		nV/√Hz
DIGITAL-TO-ANALOG CONVERTERS (DACs)					
DAC Resolution	All DACs		24		Bits
Digital Attenuation Step			0.375		dB
Digital Attenuation Range			95		dB
DAC SINGLE-ENDED OUTPUT	Single-ended operation, HPOUTLP/LOUTLP and HPOUTRP/LOUTRP pins				
Full-Scale Output Voltage	Scales linearly with AVDD		AVDD/3.4		V rms
	AVDD = 1.8 V		0.53		V rms
	AVDD = 1.8 V, 0 dBFS		1.50		V p-p
	AVDD = 3.3 V		0.97		V rms
	AVDD = 3.3 V, 0 dBFS		2.74		V p-p
Mute Attenuation			−72		dB
Line Output Mode					
Dynamic Range[1]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		100		dB
	AVDD = 3.3 V		104		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V		97		dB
	AVDD = 3.3 V		101		dB
SNR[2]	20 Hz to 20 kHz				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		100		dB
	AVDD = 3.3 V		104		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V		98		dB
	AVDD = 3.3 V		102		dB
Interchannel Gain Mismatch			20		mdB
THD + N	20 Hz to 20 kHz, −1 dBFS input				dB
	AVDD = 1.8 V		−93		dB
	AVDD = 3.3 V		−94		dB
Gain Error			±0.1		dB
Headphone Mode					
Dynamic Range[1]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		100		dB
	AVDD = 3.3 V		104		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V		97		dB
	AVDD = 3.3 V		101		dB
SNR[2]	20 Hz to 20 kHz				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		100		dB
	AVDD = 3.3 V		104		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V		98		dB
	AVDD = 3.3 V		102		dB
Interchannel Gain Mismatch			50		mdB
THD + N	20 Hz to 20 kHz, −1 dBFS input				
32 Ω Load	AVDD = 1.8 V, output power = 6.7 mW		−77		dB
	AVDD = 3.3 V, output power = 22.4 mW		−80		dB
24 Ω Load	AVDD = 1.8 V, output power = 8.9 mW		−76		dB
	AVDD = 3.3 V, output power = 30 mW		−79		dB
16 Ω Load	AVDD = 1.8 V, output power = 13 mW		−74		dB
	AVDD = 3.3 V, output power = 44 mW		−77		dB
Gain Error			±0.1		dB
Headphone Output Power					
32 Ω Load	AVDD = 1.8 V, <0.1% THD + N		8.4		mW
	AVDD = 3.3 V, <0.1% THD + N		28.1		mW
24 Ω Load	AVDD = 1.8 V, <0.1% THD + N		11.2		mW
	AVDD = 3.3 V, <0.1% THD + N		37.4		mW
16 Ω Load	AVDD = 1.8 V, <0.1% THD + N		16.25		mW
	AVDD = 3.3 V, <0.1% THD + N		55.8		mW
Offset Error			±0.1		mV
Interchannel Isolation	1 kHz, 0 dBFS input signal		100		dB
PSRR	CM capacitor = 22 µF, 100 mV p-p at 1 kHz		70		dB
DAC DIFFERENTIAL OUTPUT	Differential operation				
Full-Scale Output Voltage	Scales linearly with AVDD		AVDD/1.7		V rms
	AVDD = 1.8 V		1.06		V rms
	AVDD = 1.8 V, 0 dBFS input		3.00		V p-p
	AVDD = 3.3 V		1.94		V rms
	AVDD = 3.3 V, 0 dBFS input		5.49		V p-p
Mute Attenuation			−72		dB
Line Output Mode					
Dynamic Range[1]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		104		dB
	AVDD = 3.3 V		107		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V		101		dB
	AVDD = 3.3 V		105		dB
SNR[2]	20 Hz to 20 kHz				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		105		dB
	AVDD = 3.3 V		108		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V		102		dB
	AVDD = 3.3 V		105		dB
Interchannel Gain Mismatch			20		mdB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
THD + N	20 Hz to 20 kHz, −1 dBFS input				dB
	AVDD = 1.8 V		−96		dB
	AVDD = 3.3 V		−96		dB
Gain Error	Line output mode		±0.25		dB
Headphone Mode					
Dynamic Range[1]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		104		dB
	AVDD = 3.3 V		107		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V		102		dB
	AVDD = 3.3 V		104		dB
SNR[2]	20 Hz to 20 kHz				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		105		dB
	AVDD = 3.3 V		108		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V		103		dB
	AVDD = 3.3 V		106		dB
Interchannel Gain Mismatch			75		mdB
THD + N					
32 Ω Load	−1 dBFS, AVDD = 1.8 V, output power = 27 mW		−75		dB
	−1 dBFS, AVDD = 3.3 V, output power = 90 mW		−83		dB
24 Ω Load	−2 dBFS, AVDD = 1.8 V, output power = 28 mW		−75		dB
	−1 dBFS, AVDD = 3.3 V, output power = 118 mW		−77		dB
16 Ω Load	−3 dBFS, AVDD = 1.8 V, output power = 33 mW		−75		dB
	−1 dBFS, AVDD = 3.3 V, output power = 175 mW		−83		dB
Gain Error			±0.25		dB
Headphone Output Power					
32 Ω Load	AVDD = 1.8 V, <0.1% THD + N		32.5		mW
	AVDD = 3.3 V, <0.1% THD + N		111.8		mW
24 Ω Load	AVDD = 1.8 V, <0.1% THD + N		37.6		mW
	AVDD = 3.3 V, <0.1% THD + N		148.3		mW
16 Ω Load	AVDD = 1.8 V, <0.1% THD + N		41.5		mW
	AVDD = 3.3 V, <0.1% THD + N		189.2		mW
Offset Error			±0.1		mV
Interchannel Isolation	1 kHz, 0 dBFS input signal		100		dB
PSRR	CM capacitor = 22 µF, 100 mV p-p at 1 kHz		73		dB
CM REFERENCE	CM pin				
Common-Mode Reference Output			AVDD/2		V
Common-Mode Source Impedance			5		kΩ
REGULATOR					
Line Regulation			1		mV/V
Load Regulation			6		mV/mA

[1] Dynamic range is the ratio of the sum of the noise and harmonic power in the band of interest with a −60 dBFS signal present to the full-scale power level in decibels.
[2] SNR is the ratio of the sum of all noise power in the band of interest with no signal present to the full-scale power level in decibels.
[3] These specifications are tested with a 4.7 µF decoupling capacitor and 5.0 kΩ load on the MICBIASx pins.

CRYSTAL AMPLIFIER SPECIFICATIONS

Supply voltages AVDD = IOVDD = 1.8 V, DVDD = 1.1 V, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
Jitter		270	500	ps
Frequency Range	8		27	MHz
Load Capacitance			20	pF

DIGITAL INPUT/OUTPUT SPECIFICATIONS

−40°C < T_A < +85°C, IOVDD = 3.3 V ± 10% and 1.8 V − 5%/+10%.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT/OUTPUT					
Input Voltage					
High (V_{IH})	IOVDD = 3.3 V	2.0			V
	IOVDD = 1.8 V	1.1			V
Low (V_{IL})	IOVDD = 3.3 V			0.8	V
	IOVDD = 1.8 V			0.45	V
Input Leakage	IOVDD = 3.3 V, I_{IH} at V_{IH} = 2.0 V			10	µA
	I_{IL} at V_{IL} = 0.8 V			10	µA
	IOVDD = 1.8 V, I_{IH} at V_{IH} = 1.1 V			10	µA
	I_{IL} at V_{IL} = 0.45 V			10	µA
Output Voltage					
High (V_{OH})					
Low Drive Strength	I_{OH} = 1 mA	IOVDD − 0.6			V
High Drive Strength	I_{OH} = 3 mA	IOVDD − 0.6			V
Low (V_{OL})					
Low Drive Strength	I_{OL} = 1 mA			0.4	V
High Drive Strength	I_{OL} = 3 mA			0.4	V
Input Capacitance				5	pF

POWER SUPPLY SPECIFICATIONS

Supply voltages AVDD = IOVDD = 1.8 V, DVDD = 1.1 V, unless otherwise noted, PLL disabled, direct master clock.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLIES					
AVDD Voltage		1.71	1.8	3.63	V
DVDD Voltage		1.045	1.1	1.98	V
IOVDD Voltage		1.71	1.8	3.63	V
Digital Input/Output Current with IOVDD = 1.8 V	Crystal oscillator enabled				
Slave Mode	f_S = 8 kHz		0.32		mA
	f_S = 48 kHz		0.35		mA
	f_S = 192 kHz		0.49		mA
Master Mode	f_S = 8 kHz		0.35		mA
	f_S = 48 kHz		0.53		mA
	f_S = 192 kHz		1.18		mA
Power-Down			0		µA
Digital Input/Output Current with IOVDD = 3.3 V	Crystal oscillator enabled				
Slave Mode	f_S = 8 kHz		1.99		mA
	f_S = 48 kHz		2.05		mA
	f_S = 192 kHz		2.28		mA
Master Mode	f_S = 8 kHz		2.05		mA
	f_S = 48 kHz		2.4		mA
	f_S = 192 kHz		3.62		mA
Power-Down			7		µA
Analog Current (AVDD)	See Table 5				
Power-Down	AVDD = 1.8 V		0.6		µA
	AVDD = 3.3 V		13.6		µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DISSIPATION					
Operation	f_S = 192 kHz (see conditions in Table 5)				
All Supplies			15.5		mW
Digital Input/Output Supply			0.7		mW
Analog Supply	Includes regulated DVDD current		14.8		mW
Power-Down, All Supplies			1		µW

TYPICAL POWER CONSUMPTION

Unless otherwise noted, IOVDD = 1.8 V, AVDD = 1.8 V, master clock = 12.288 MHz, f_S = 192 kHz; on-board regulator enabled and set to 1.2 V, PLL enabled, two ADCs with PGA enabled and two ADCs configured for line input, no input signal. ADC0 and ADC1 are routed to ADC_SDATA0 and ADC_SDATA0 is externally routed back into the DAC_SDATA input. The serial port is set to slave. Two DACs are configured for differential line output operation; DAC outputs are unloaded. Both MICBIAS0 and MICBIAS1 are enabled. For total power consumption, add IOVDD at the 8 kHz slave current listed in Table 4.

Table 5.

Operating Voltage	Power Management Setting	Typical AVDD Power Consumption (mA)	Typical ADC THD + N (dB)	Typical HP Output THD + N (dB)
AVDD = IOVDD = 3.3 V	Normal (default)	11.5	−93	−87.5
	Extreme power saving	9.4	−93	−86.5
	Power saving	9.8	−93	−86.5
	Enhanced performance	12.65	−93	−90.5
AVDD = IOVDD = 1.8 V	Normal (default)	9.37	−86	−91
	Extreme power saving	7.40	−84.5	−87
	Power saving	7.78	−84.5	−87.5
	Enhanced performance	10.4	−86	−94.5

DIGITAL FILTERS

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SAMPLE RATE CONVERTER					
Pass Band	LRCLK < 63 kHz	0		0.475 × f_S	kHz
	63 kHz < LRCLK <130 kHz	0		0.4286 × f_S	kHz
	LRCLK > 130 kHz	0		0.4286 × f_S	kHz
Pass-Band Ripple	Upsampling, 96 kHz	−0.27		+0.05	dB
	Upsampling, 192 kHz	−0.06		+0.05	dB
	Downsampling, 96 kHz	0		0.07	dB
	Downsampling, 192 kHz	0		0.07	dB
Input/Output Frequency Range		8		192	kHz
Dynamic Range			100		dB
THD + N			−90		dB
Startup Time				15	ms

DIGITAL TIMING SPECIFICATIONS

−40°C < T_A < +85°C, IOVDD = 1.71 V to 3.63 V, DVDD = 1.045 V to 1.98 V.

Table 7. Digital Timing

Parameter	t_{MIN}	t_{MAX}	Unit	Description
MASTER CLOCK				
t_{MP}	37	125	ns	MCLKIN period; 8 MHz to 27 MHz input clock using PLL
t_{MCLK}	77	82	ns	Internal MCLK period; direct MCLK and PLL output divided by 2
SERIAL PORT				
t_{BL}	40		ns	BCLK low pulse width (master and slave modes)
t_{BH}	40		ns	BCLK high pulse width (master and slave modes)
t_{LS}	10		ns	LRCLK setup; time to BCLK rising (slave mode)
t_{LH}	10		ns	LRCLK hold; time from BCLK rising (slave mode)
t_{SS}	5		ns	DAC_SDATA setup; time to BCLK rising (master and slave modes)
t_{SH}	5		ns	DAC_SDATA hold; time from BCLK rising (master and slave modes)
t_{TS}		10	ns	BCLK falling to LRCLK timing skew (master mode)
t_{SOD}	0	34	ns	ADC_SDATAx delay; time from BCLK falling (master and slave modes)
t_{SOTD}		30	ns	BCLK falling to ADC_SDATAx driven in time-division multiplexing (TDM) tristate mode
t_{SOTX}		30	ns	BCLK falling to ADC_SDATAx tristate in TDM tristate mode
SPI PORT				
f_{SCLK}		6.25	MHz	SCLK frequency
t_{CCPL}	80		ns	SCLK pulse width low
t_{CCPH}	80		ns	SCLK pulse width high
t_{CLS}	5		ns	$\overline{SS}$ setup; time to SCLK rising
t_{CLH}	100		ns	$\overline{SS}$ hold; time from SCLK rising
t_{CLPH}	80		ns	$\overline{SS}$ pulse width high
t_{CDS}	10		ns	MOSI setup; time to SCLK rising
t_{CDH}	10		ns	MOSI hold; time from SCLK rising
t_{COD}		101	ns	MISO delay; time from SCLK falling
I²C PORT				
f_{SCL}		400	kHz	SCL frequency
t_{SCLH}	0.6		µs	SCL high
t_{SCLL}	1.3		µs	SCL low
t_{SCS}	0.6		µs	SCL rise setup time (to SDA falling), relevant for repeated start condition
t_{SCR}		250	ns	SCL and SDA rise time, C_{LOAD} = 400 pF
t_{SCH}	0.6		µs	SCL fall hold time (from SDA falling), relevant for start condition
t_{DS}	100		ns	SDA setup time (to SCL rising)
t_{SCF}		250	ns	SCL fall time; C_{LOAD} = 400 pF
t_{SDF}		250	ns	SDA fall time; C_{LOAD} = 400 pF; not shown in Figure 5
t_{BFT}	0.6		µs	SCL rise setup time (to SDA rising), relevant for stop condition
MULTIPURPOSE AND POWER-DOWN PINS				
t_{GIL}		1.5 × 1/f_S	µs	MPx input latency; time until high or low value is read
t_{RLPW}	20		ns	$\overline{PD}$ low pulse width
DIGITAL MICROPHONE				
t_{CF}		20	ns	Digital microphone clock fall time
t_{CR}		20	ns	Digital microphone clock rise time
t_{DS}	40			Digital microphone valid data start time
t_{DE}		0	ns	Digital microphone valid data end time

Digital Timing Diagrams

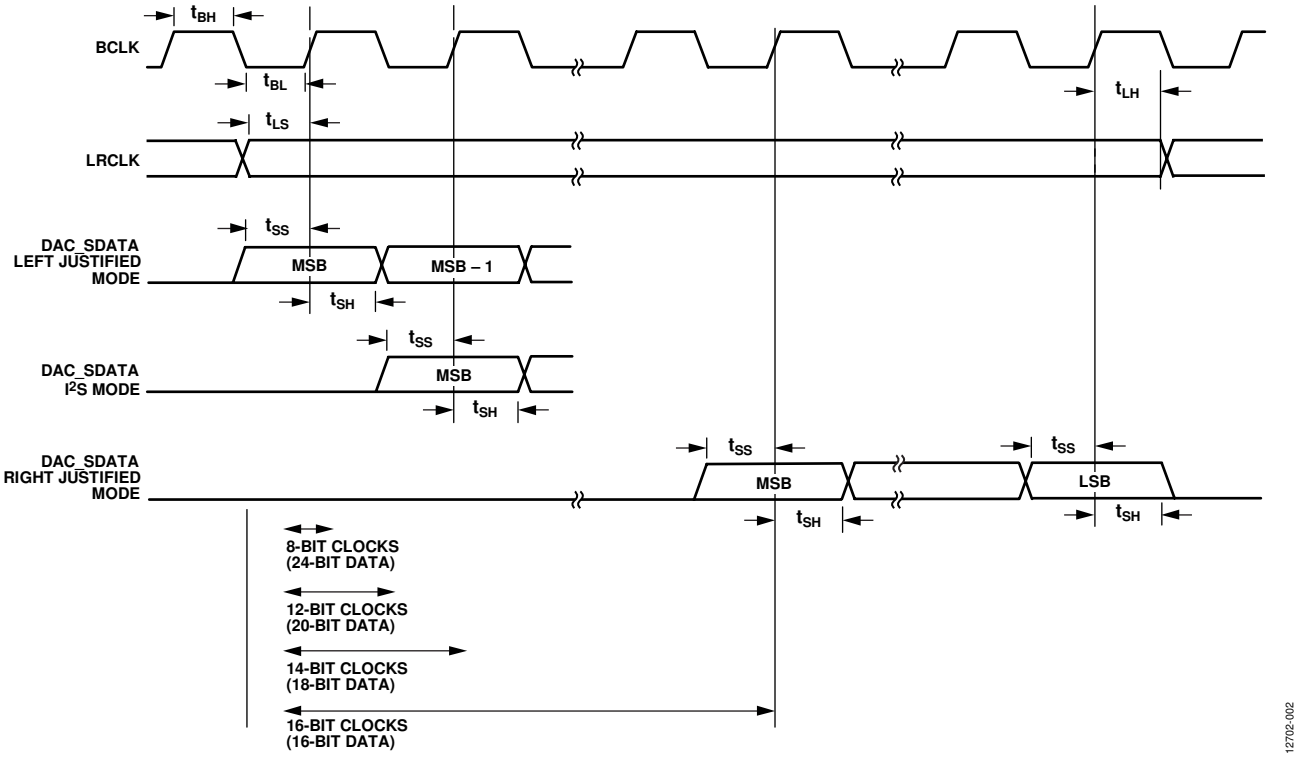

Figure 2. Serial Input Port Timing

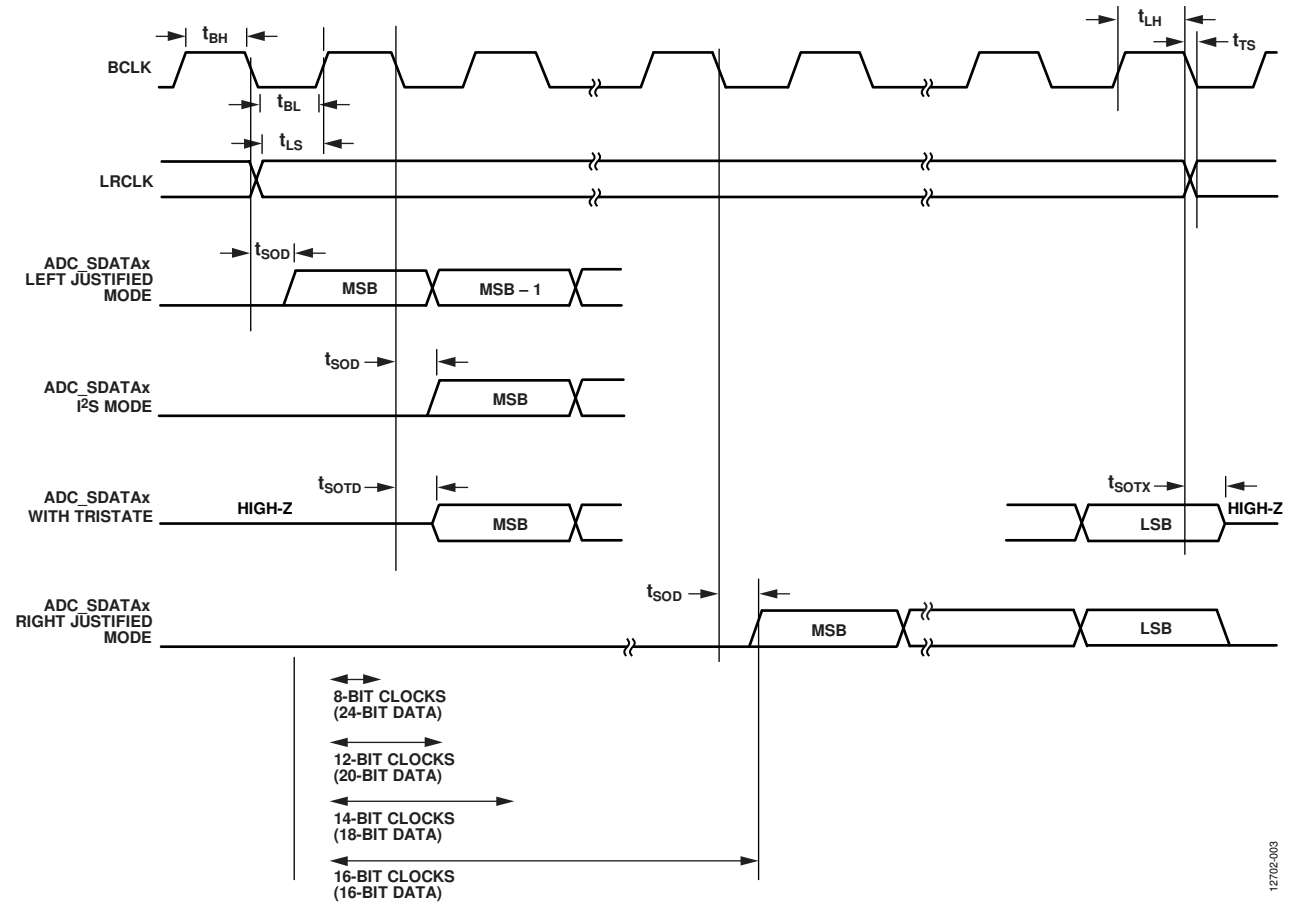

Figure 3. Serial Output Port Timing

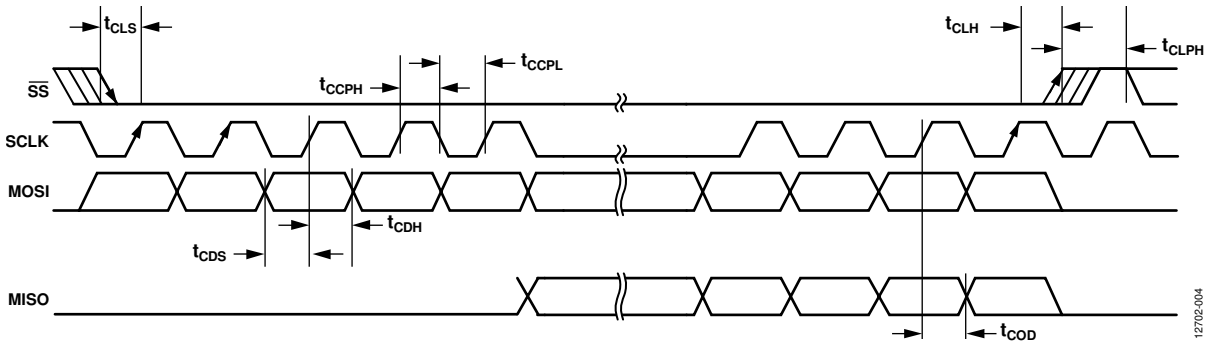

Figure 4. SPI Port Timing

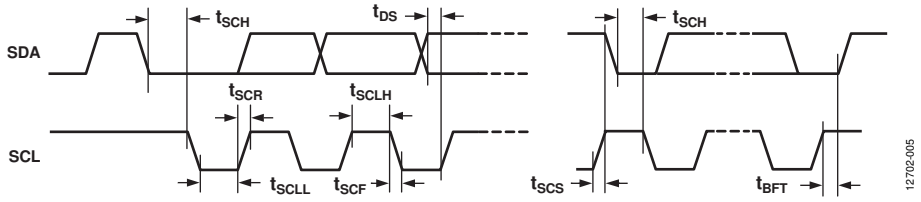

Figure 5. I²C Port Timing

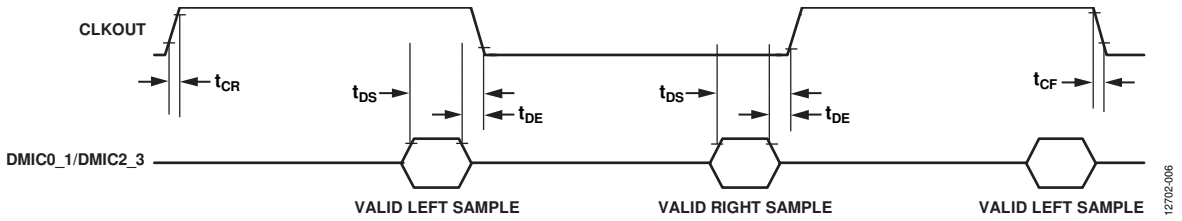

Figure 6. Digital Microphone Timing

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Power Supplies (AVDD, IOVDD)	−0.3 V to +3.63 V
Digital Supply (DVDD)	−0.3 V to +1.98 V
Input Current (Except Supply Pins)	±20 mA
Analog Input Voltage (Signal Pins)	−0.3 V to AVDD + 0.3 V
Digital Input Voltage (Signal Pins)	−0.3 to IOVDD + 0.3 V
Operating Temperature Range (Case)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} represents the junction-to-ambient thermal resistance; θ_{JC} represents the junction-to-case thermal resistance. Thermal numbers are simulated on a 4-layer JEDEC printed circuit board (PCB) with the exposed pad soldered to the PCB. θ_{JC} is simulated at the exposed pad on the bottom of the package.

Table 9. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead LFCSP	29	1.8	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

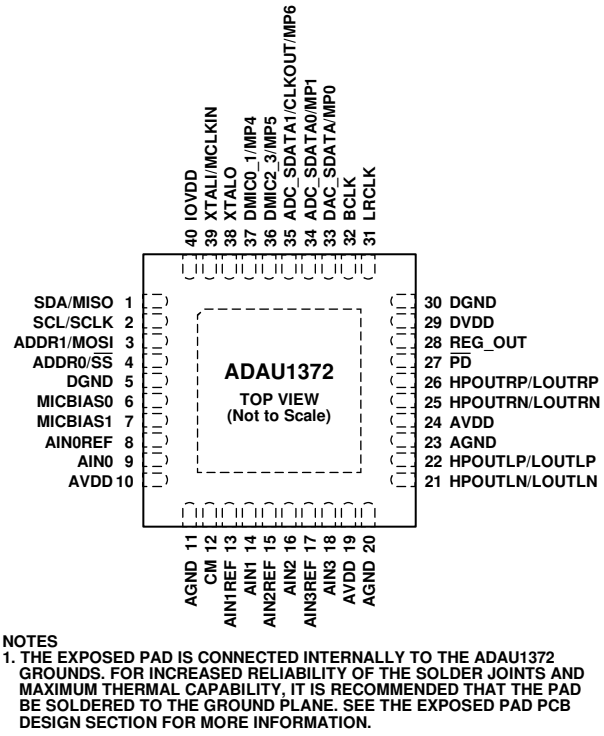

Figure 7. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	SDA/MISO	D_IO	I²C Data (SDA). This pin is a bidirectional open-collector. The line connected to this pin must have a 2.0 kΩ pull-up resistor.
			SPI Data Output (MISO). This SPI data output reads back registers. It is tristated when an SPI read is not active.
2	SCL/SCLK	D_IN	I²C Clock (SCL). This pin is always an open-collector input when the device is in I²C control mode. The line connected to this pin must have a 2.0 kΩ pull-up resistor in I²C mode.
			SPI Clock (SCLK). This pin can either run continuously or be gated off between SPI transactions.
3	ADDR1/MOSI	D_IN	I²C Address 1 (ADDR1).
			SPI Data Input (MOSI).
4	ADDR0/$\overline{SS}$	D_IN	I²C Address 0 (ADDR0).
			SPI Latch Signal ($\overline{SS}$). This pin must go low at the beginning of an SPI transaction and high at the end of a transaction. Each SPI transaction can take a different number of SCLK cycles to complete, depending on the address and the read/write bit sent at the beginning of the SPI transaction.
5	DGND	PWR	Digital Ground. Tie the AGND and DGND pins directly together in a common ground plane.
6	MICBIAS0	A_OUT	Bias Voltage for Electret Microphone. Decouple with a 1 µF capacitor.
7	MICBIAS1	A_OUT	Bias Voltage for Electret Microphone. Decouple with a 1 µF capacitor.
8	AIN0REF	A_IN	ADC0 Input Reference. AC couple this reference pin to ground with a 10 µF capacitor.
9	AIN0	A_IN	ADC0 Input.
10	AVDD	PWR	1.8 V to 3.3 V Analog Supply. Decouple this pin to AGND with a 0.1 µF capacitor.
11	AGND	PWR	Analog Ground. Tie the AGND and DGND pins directly together in a common ground plane. Decouple AGND to AVDD with a 0.1 µF capacitor.

Pin No.	Mnemonic	Type[1]	Description
12	CM	A_OUT	AVDD/2 V Common-Mode Reference. Connect a 10 µF to 47 µF decoupling capacitor between this pin and ground to reduce crosstalk between the ADCs and DACs. The material of the capacitors is not critical. This pin can be used to bias external analog circuits, as long as they are not drawing current from CM (for example, the noninverting input of an operational amplifier).
13	AIN1REF	A_IN	ADC1 Input Reference. AC couple this reference pin to ground with a 10 µF capacitor.
14	AIN1	A_IN	ADC1 Input.
15	AIN2REF	A_IN	ADC2 Input Reference. AC couple this reference pin to ground with a 10 µF capacitor.
16	AIN2	A_IN	ADC2 Input.
17	AIN3REF	A_IN	ADC3 Input Reference. AC couple this reference pin to ground with a 10 µF capacitor.
18	AIN3	A_IN	ADC3 Input.
19	AVDD	PWR	1.8 V to 3.3 V Analog Supply. Decouple this pin to AGND with a 0.1 µF capacitor.
20	AGND	PWR	Analog Ground. See the Grounding section.
21	HPOUTLN/LOUTLN	A_OUT	Left Headphone Inverted (HPOUTLN). Line Output Inverted (LOUTLN).
22	HPOUTLP/LOUTLP	A_OUT	Left Headphone Noninverted (HPOUTLP). Line Output Noninverted, Single-Ended Line Output (LOUTLP).
23	AGND	PWR	Headphone Amplifier Ground. See the Grounding section.
24	AVDD	PWR	Headphone Amplifier Power, 1.8 V to 3.3 V Analog Supply. Decouple this pin to AGND with a 0.1 µF capacitor. The PCB trace to this pin must be able to supply the higher current necessary for driving the headphone outputs.
25	HPOUTRN/LOUTRN	A_OUT	Right Headphone Inverted (HPOUTRN). Line Output Inverted (LOUTRN).
26	HPOUTRP/LOUTRP	A_OUT	Right Headphone Noninverted (HPOUTRP). Line Output Noninverted, Single-Ended Line Output (LOUTRP).
27	$\overline{PD}$	D_IN	Active Low Power-Down. All digital and analog circuits are powered down. There is an internal pull-down resistor on this pin; therefore, the ADAU1372 is held in power-down mode if its input signal is floating while power is applied to the supply pins.
28	REG_OUT	A_OUT	Regulator Output Voltage. Connect this pin to DVDD if the internal voltage regulator is generating the DVDD voltage.
29	DVDD	PWR	Digital Core Supply. The digital supply can be generated from an on-board regulator or supplied directly from an external supply. In each case, decouple DVDD to DGND with a 0.1 µF capacitor.
30	DGND	PWR	Digital Ground. See the Grounding section.
31	LRCLK	D_IO	Serial Data Port Frame Clock.
32	BCLK	D_IO	Serial Data Port Bit Clock.
33	DAC_SDATA/MP0	D_IO	DAC Serial Input Data (DAC_SDATA). General-Purpose Input (MP0).
34	ADC_SDATA0/MP1	D_IO	ADC Serial Data Output 0 (ADC_SDATA0). General-Purpose Input (MP1).
35	ADC_SDATA1/CLKOUT/MP6	D_IO	Serial Data Output 1 (ADC_SDATA1). Master Clock Output/Clock for the Digital Microphone Input (CLKOUT). General-Purpose Input (MP6).
36	DMIC2_3/MP5	D_IN	Digital Microphone Stereo Input 2 and Digital Microphone Stereo Input 3 (DMIC2_3). General-Purpose Input (MP5).
37	DMIC0_1/MP4	D_IN	Digital Microphone Stereo Input 0 and Digital Microphone Stereo Input 1 (DMIC0_1). General-Purpose Input (MP4).
38	XTALO	A_OUT	Crystal Clock Output. This pin is the output of the crystal amplifier and must not be used to provide a clock to other ICs in the system. If a master clock output is needed, use CLKOUT (Pin 35).
39	XTALI/MCLKIN	D_IN	Crystal Clock Input (XTALI). Master Clock Input (MCLKIN).

Pin No.	Mnemonic	Type[1]	Description
40	IOVDD	PWR	Supply for Digital Input and Output Pins. The digital output pins are supplied from IOVDD, and IOVDD sets the highest input voltage that can be present on the digital input pins. The current draw of this pin is variable because it is dependent on the loads of the digital outputs. Decouple IOVDD to DGND with a 0.1 µF capacitor.
	EP		Exposed Pad. The exposed pad is connected internally to the ADAU1372 grounds. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the ground plane. See the Exposed Pad PCB Design section for more information.

[1] D_IO is digital input/output, D_IN is digital input, A_OUT is analog output, PWR is power, and A_IN is analog input.

TYPICAL PERFORMANCE CHARACTERISTICS

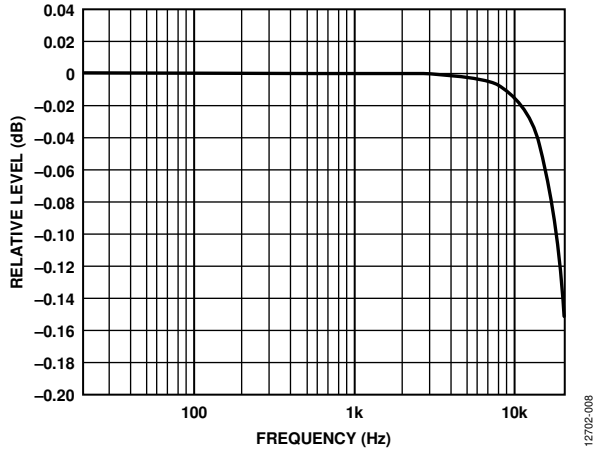

Figure 8. Relative Level vs. Frequency, f_S = 48 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

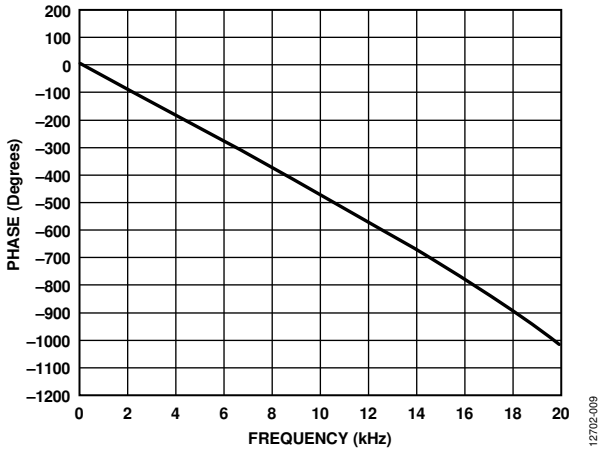

Figure 9. Phase vs. Frequency, 20 kHz Bandwidth, f_S = 48 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

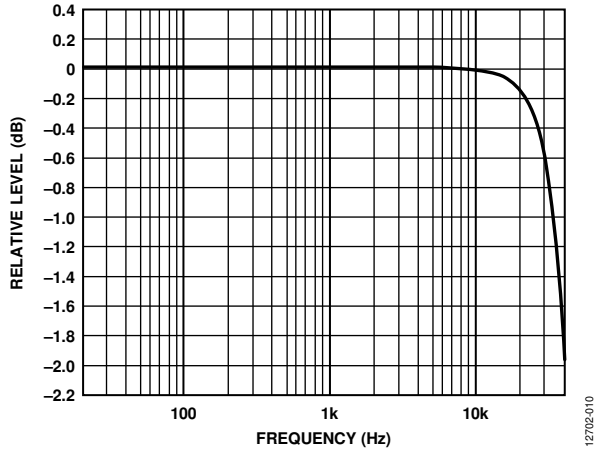

Figure 10. Relative Level vs. Frequency, f_S = 96 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

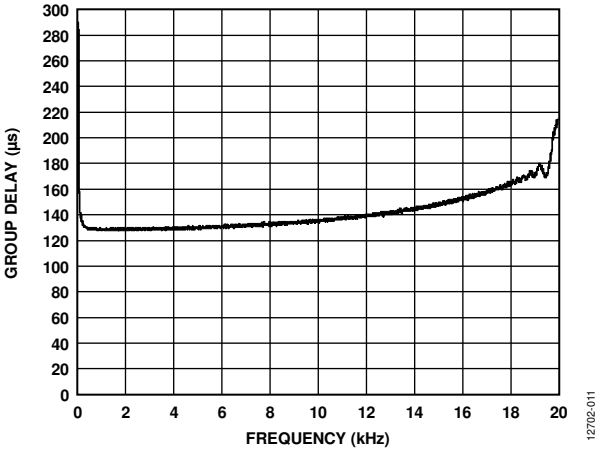

Figure 11. Group Delay vs. Frequency, f_S = 48 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

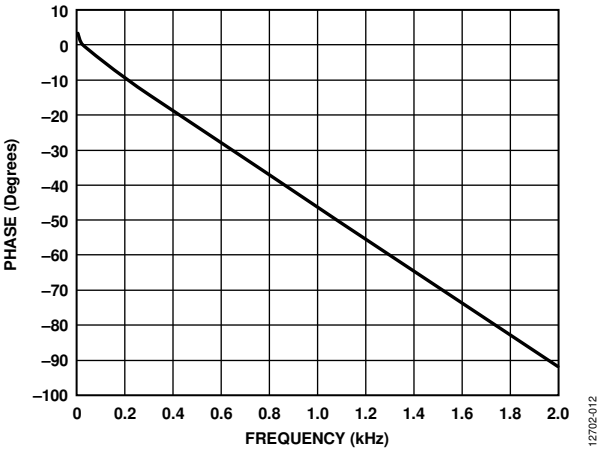

Figure 12. Phase vs. Frequency, 2 kHz Bandwidth, f_S = 48 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

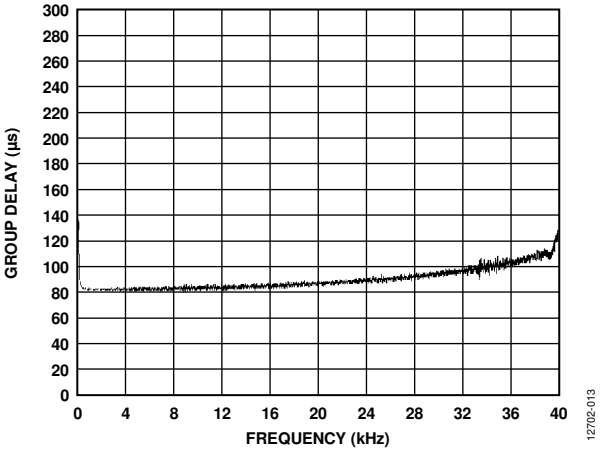

Figure 13. Group Delay vs. Frequency, f_S = 96 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

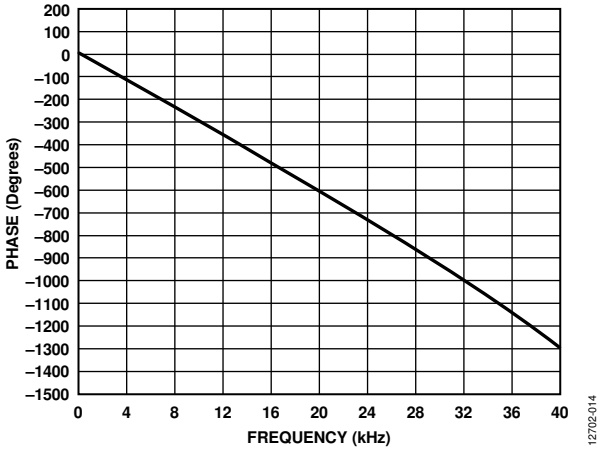

Figure 14. Phase vs. Frequency, 40 kHz Bandwidth, f_S = 96 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

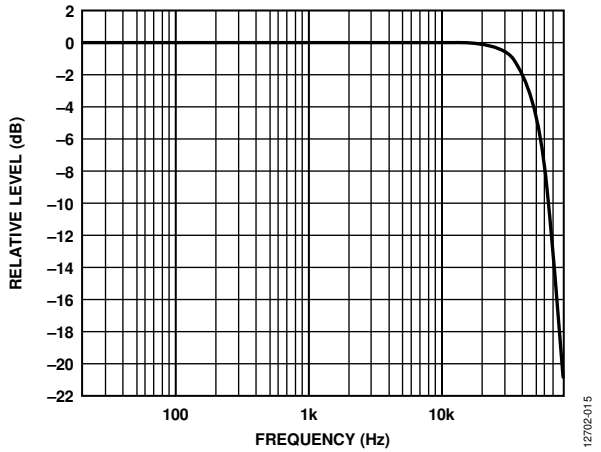

Figure 15. Relative Level vs. Frequency, f_S = 192 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

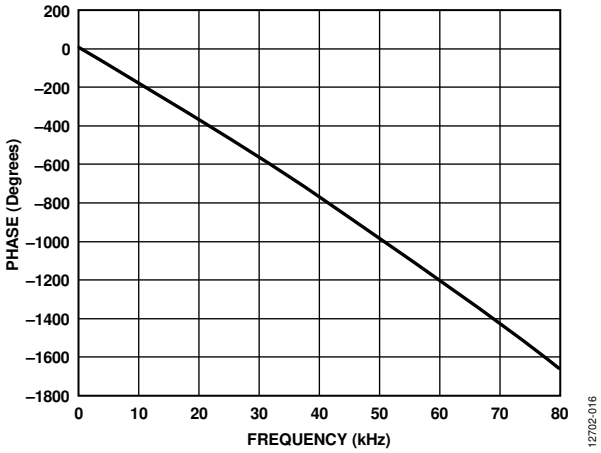

Figure 16. Phase vs. Frequency, 80 kHz Bandwidth, f_S = 192 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

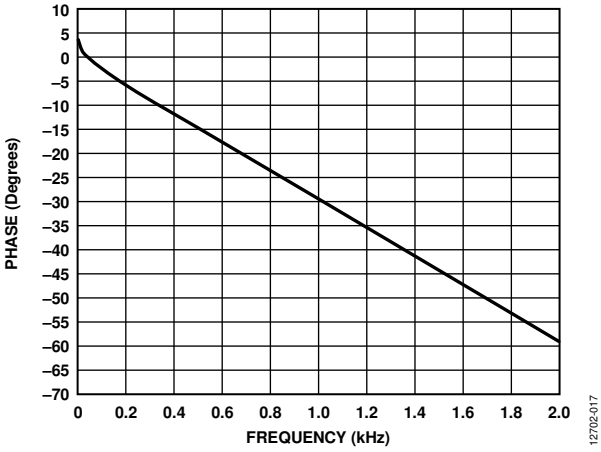

Figure 17. Phase vs. Frequency, 2 kHz Bandwidth, f_S = 96 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

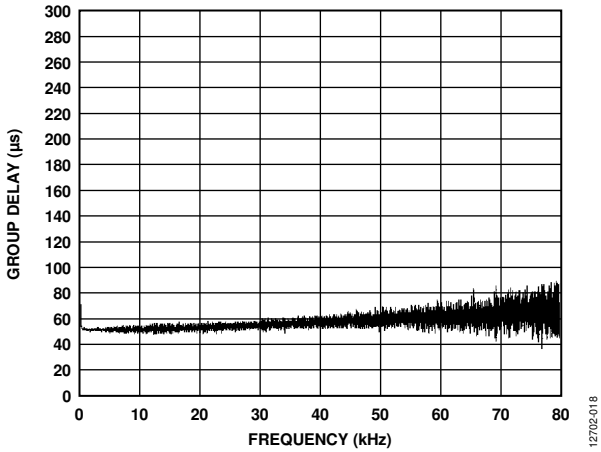

Figure 18. Group Delay vs. Frequency, f_S = 192 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

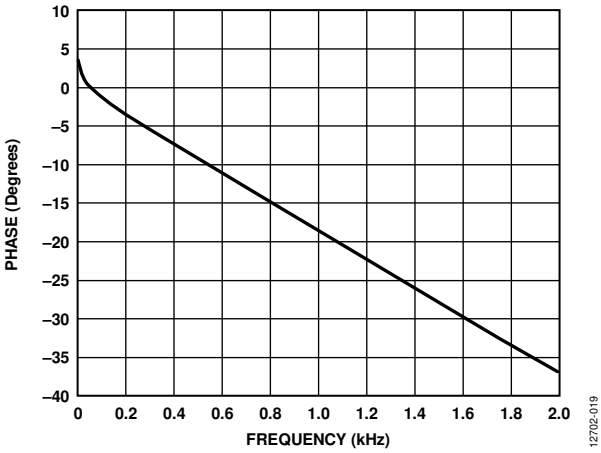

Figure 19. Phase vs. Frequency, 2 kHz Bandwidth, f_S = 192 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

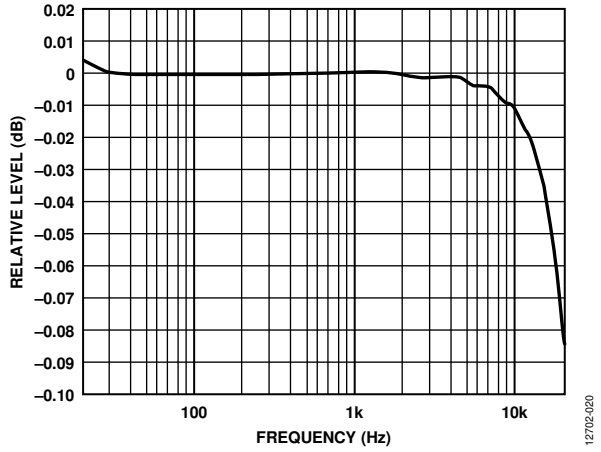

Figure 20. Relative Level vs. Frequency,
f_S = 48 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

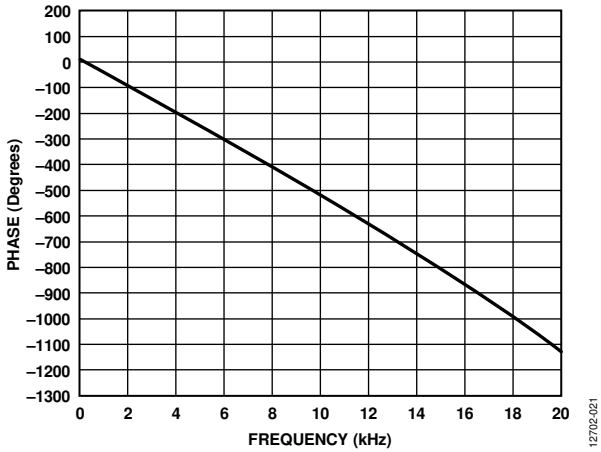

Figure 21. Phase vs. Frequency, 20 kHz Bandwidth,
f_S = 48 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

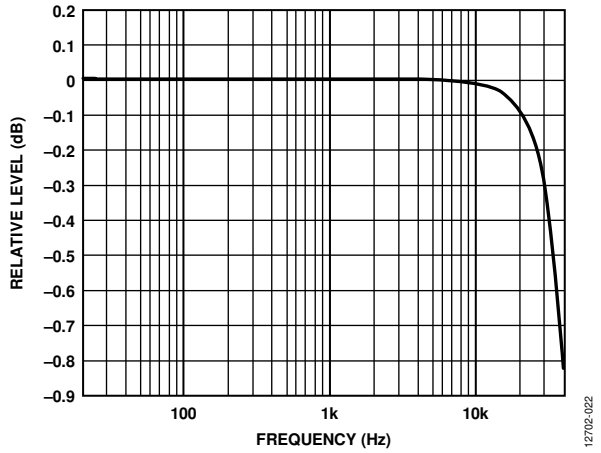

Figure 22. Relative Level vs. Frequency,
f_S = 96 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

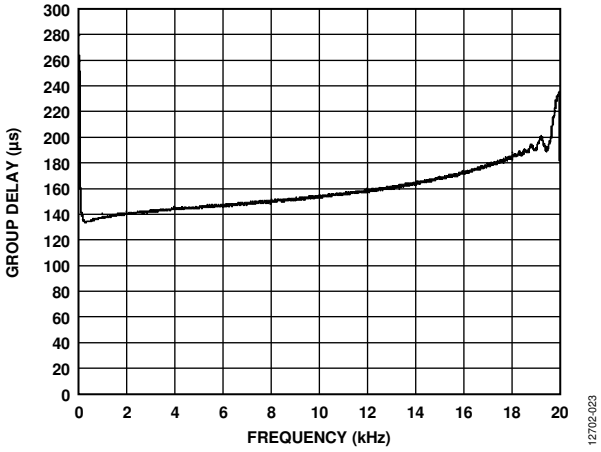

Figure 23. Group Delay vs. Frequency,
f_S = 48 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

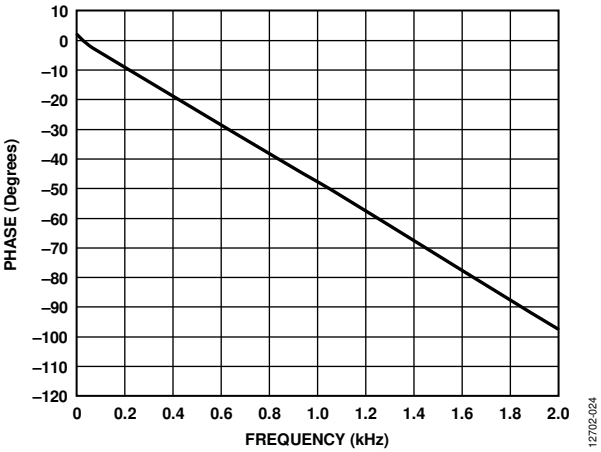

Figure 24. Phase vs. Frequency, 2 kHz Bandwidth,
f_S = 48 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

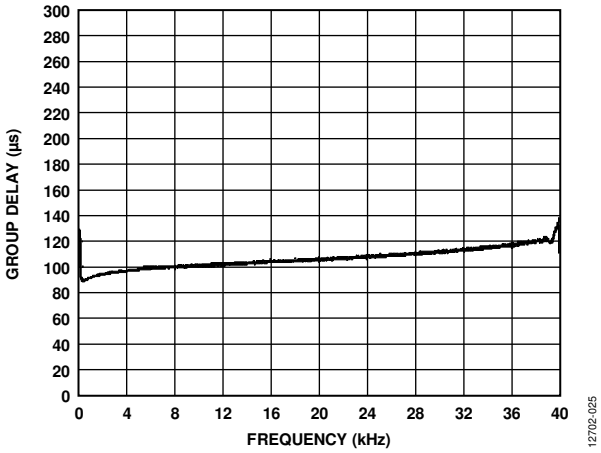

Figure 25. Group Delay vs. Frequency,
f_S = 96 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

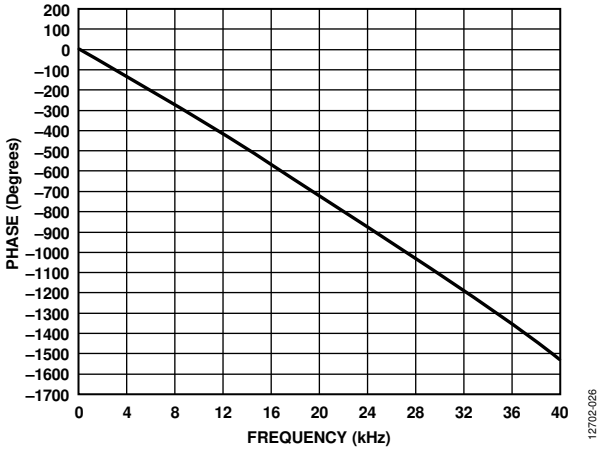

Figure 26. Phase vs. Frequency, 40 kHz Bandwidth, f_S = 96 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

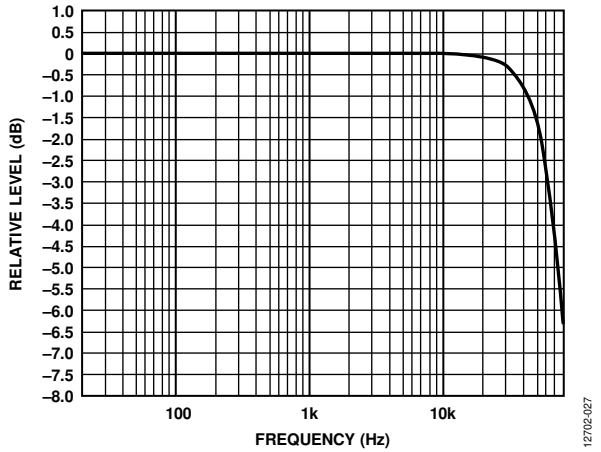

Figure 27. Relative Level vs. Frequency, f_S = 192 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

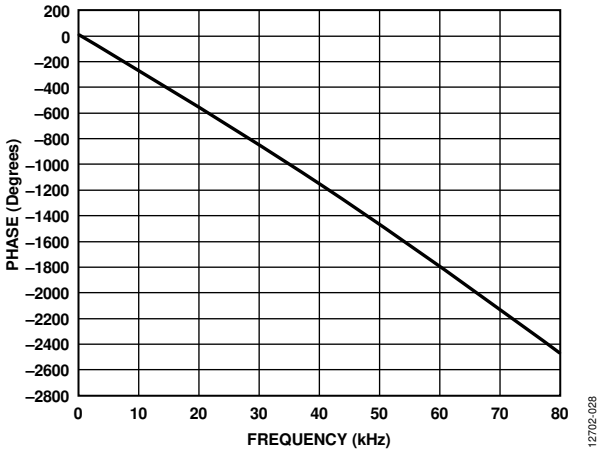

Figure 28. Phase vs. Frequency, 80 kHz Bandwidth, f_S = 192 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

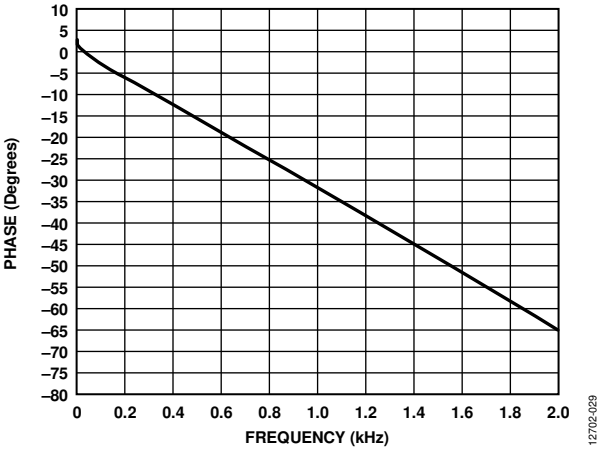

Figure 29. Phase vs. Frequency, 2 kHz Bandwidth, f_S = 96 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

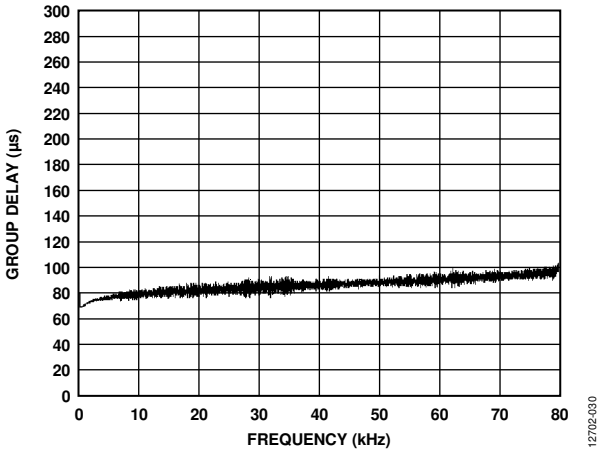

Figure 30. Group Delay vs. Frequency, f_S = 192 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

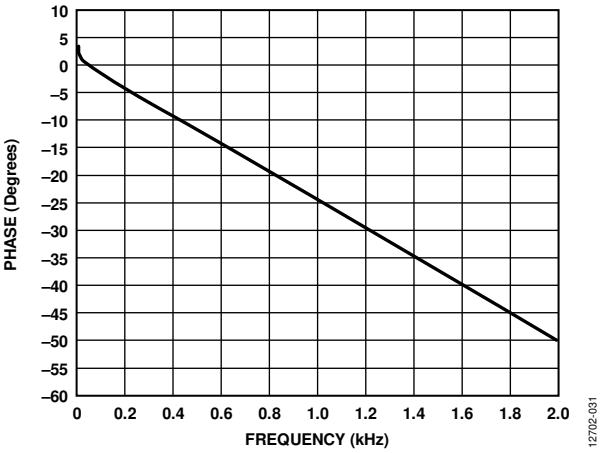

Figure 31. Phase vs. Frequency, 2 kHz Bandwidth, f_S = 192 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

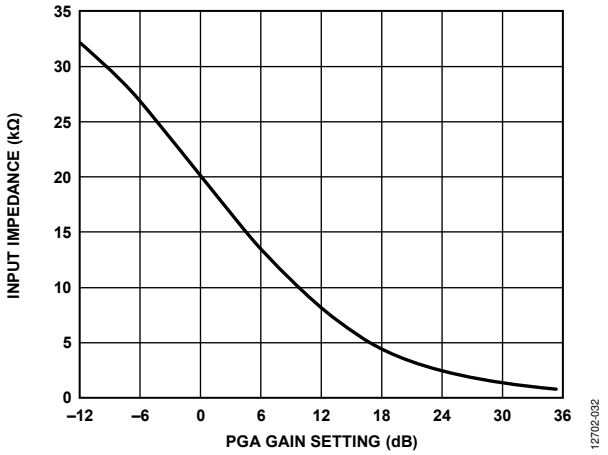

Figure 32. Input Impedance vs. PGA Gain Setting (See the Input Impedance Section)

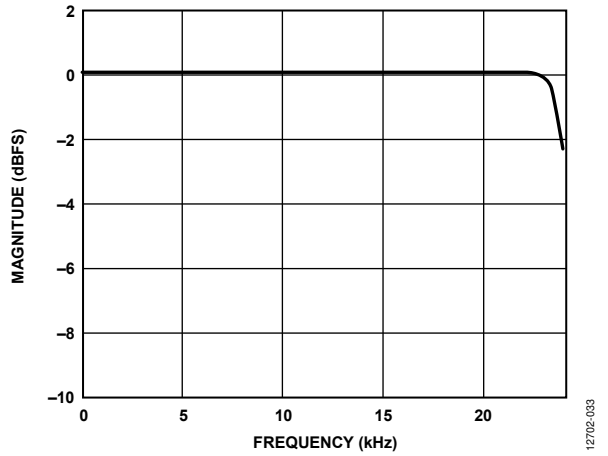

Figure 33. Decimation Pass Band Response, f_S = 96 kHz

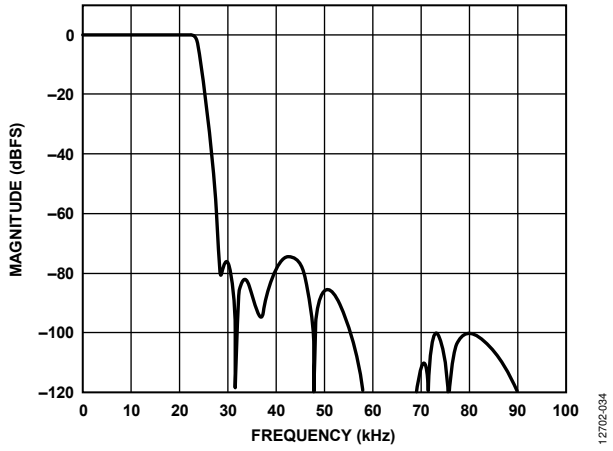

Figure 34. Total Decimation Response, f_S = 96 kHz, Serial Port f_S = 48 kHz

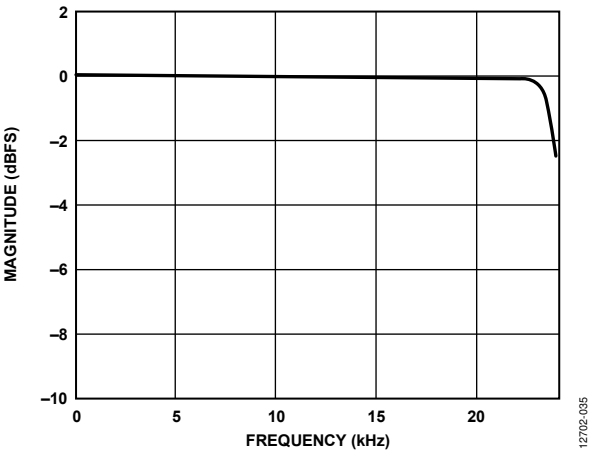

Figure 35. Decimation Pass Band Response, f_S = 192 kHz

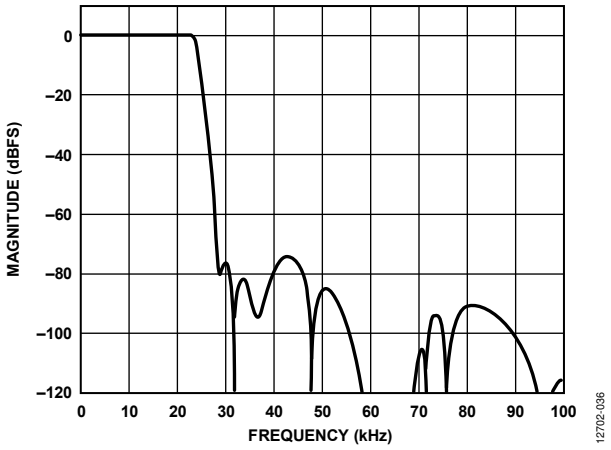

Figure 36. Total Decimation Response, fs = 192 kHz, Serial Port f_S = 48 kHz

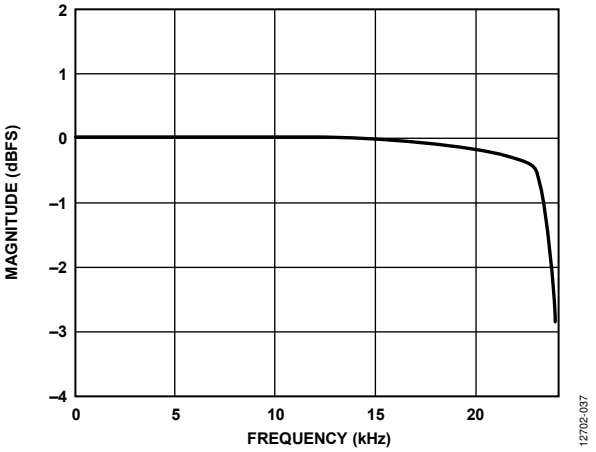

Figure 37. Interpolation Pass Band Response, f_S = 96 kHz

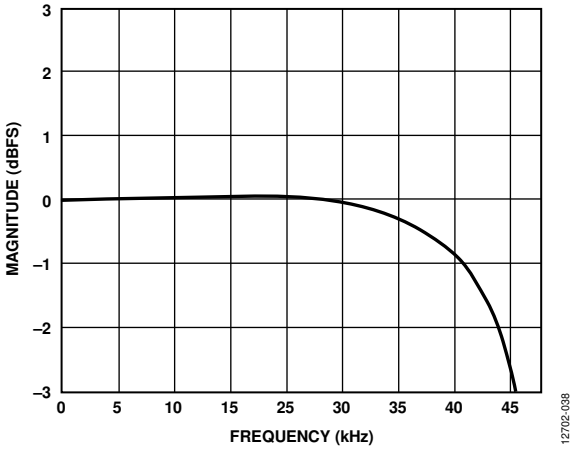

Figure 38. Decimation Pass Band Response, f_S = 96 kHz, Serial Port f_S = 96 kHz

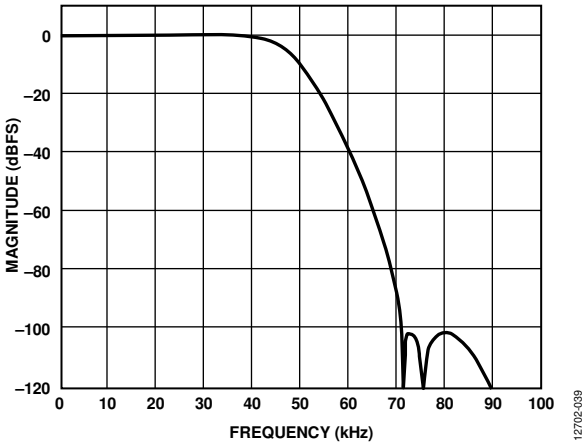

Figure 39. Total Decimation Response, f_S = 96 kHz, Serial Port f_S = 96 kHz

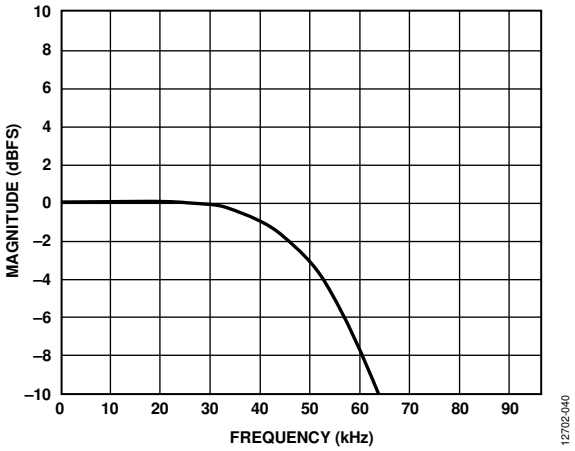

Figure 40. Decimation Pass Band Response, f_S = 96 kHz, Serial Port f_S = 192 kHz

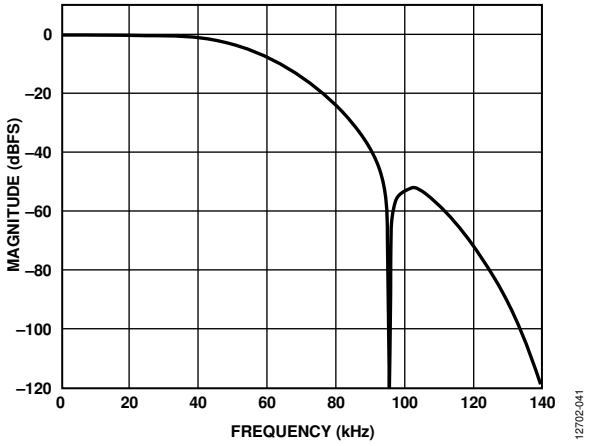

Figure 41. Total Decimation Response, f_S = 96 kHz, Serial Port f_S = 192 kHz

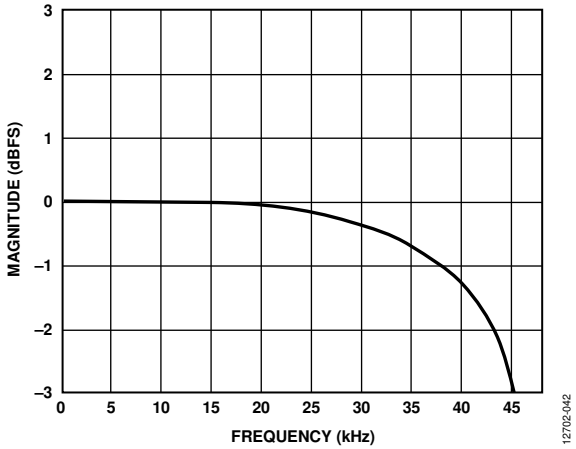

Figure 42. Decimation Pass Band Response, f_S = 192 kHz, Serial Port f_S = 96 kHz

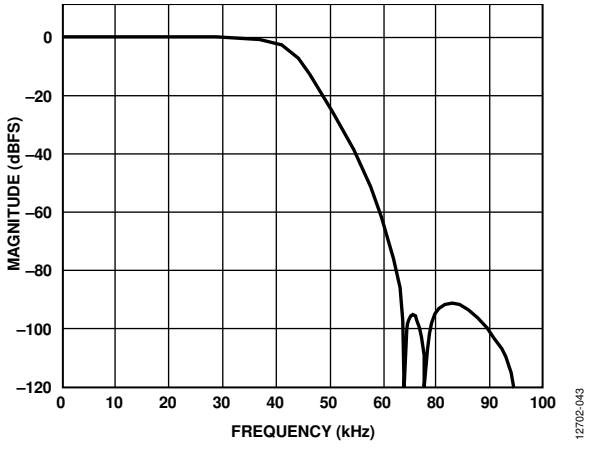

Figure 43. Total Decimation Response, f_S = 192 kHz, Serial Port f_S = 96 kHz

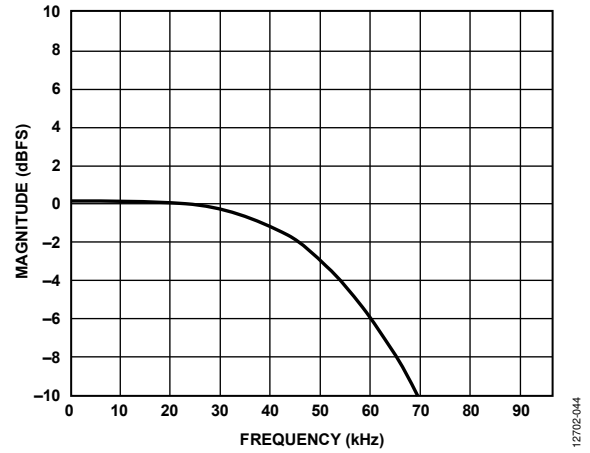

Figure 44. Decimation Pass Band Response, f_S = 192 kHz, Serial Port f_S = 192 kHz

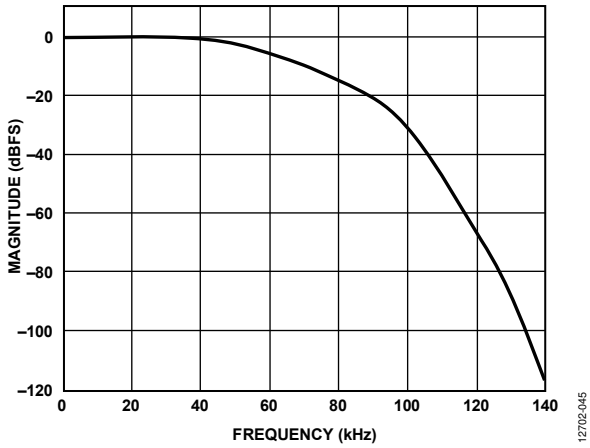

Figure 45. Total Decimation Response, f_S = 192 kHz, Serial Port f_S = 192 kHz

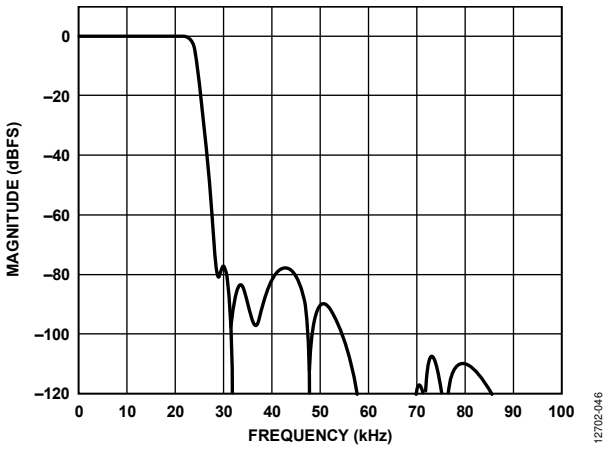

Figure 46. Total Interpolation Response, f_S = 96 kHz

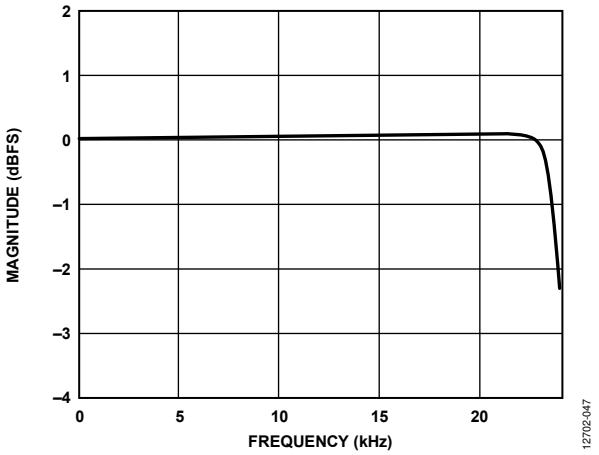

Figure 47. Interpolation Pass Band Response, f_S = 192 kHz

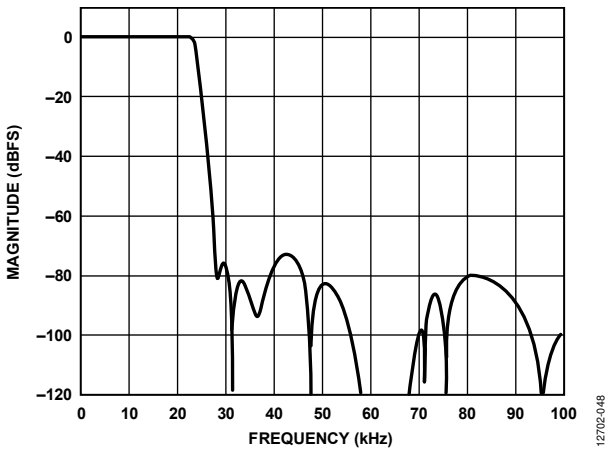

Figure 48. Total Interpolation Response, f_S = 192 kHz

THEORY OF OPERATION

The ADAU1372 is a low power audio codec that is ideal for portable applications that require high quality audio, low power, small size, and low latency. The four ADC and two DAC channels each have an SNR of at least 94 dB and a THD + N of at least −88 dB. The serial data port is compatible with I²S, left justified, right justified, and TDM modes, with tristating for interfacing to digital audio data. The operating voltage range is 1.8 V to 3.3 V, with an on-board regulator generating the internal digital supply voltage. If desired, the regulator can be powered down and the voltage can be supplied externally.

The input signal path includes flexible configurations that can accept single-ended analog microphone inputs as well as up to four channels of digital microphone inputs. Two microphone bias pins provide seamless interfacing to electret microphones. Each input signal has its own PGA for volume adjustment.

The ADCs and DACs are high quality, 24-bit Σ-Δ converters that operate at a selectable 192 kHz or 96 kHz sampling rate. The ADCs have an optional high-pass filter with a cutoff frequency of 1 Hz, 4 Hz, or 8 Hz. The ADCs and DACs also include very fine step digital volume controls.

The stereo DAC output can differentially drive a headphone earpiece speaker with 16 Ω impedance or higher. One side of the differential output can be powered down if single-ended operation is required. There is also the option to change to line output mode when the output is lightly loaded.

The SigmaStudio™ software can be used to control the registers through the control port. SigmaStudio allows an easy graphical interface to control the signal flow; the tool can be used to configure all of the ADAU1372 registers.

The ADAU1372 can generate its internal clocks from a wide range of input clocks by using the on-board fractional PLL. The PLL accepts inputs from 8 MHz to 27 MHz. For standalone operation, the clock can be generated using the on-board crystal oscillator.

The ADAU1372 is provided in a small, 40-lead, 6 mm × 6 mm LFCSP with an exposed bottom pad.