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Low Power Codec with Speaker and Headphone Amplifier

ADAU1373

FEATURES

1 stereo ADC and 2 stereo DACs with sampling rates from 8 kHz to 48 kHz
Low power: 7 mW record, 6 mW playback, 48 kHz at 1.8 V
8 single-ended or 4 differential inputs with PGA
2 microphone bias reference voltages with current sense
2 stereo digital microphone inputs
Flexible analog input/output mixers
1 stereo differential or 2 stereo single-ended line outputs
True ground-centered stereo Class-G headphone amplifier, capable of 2 × 50 mW into 16 Ω at 1.8 V, 10% THD
Filterless stereo Class-D speaker amplifier, capable of 2 × 880 mW into 8 Ω at 3.6 V, 10% THD
Differential earpiece amplifier capable of driving 32 Ω
2 PLLs, supporting input clocks from 8 kHz to 27 MHz
I²C control interface
Digital audio processing
3 digital audio input and output ports with ASRC
I²S, PCM, right-justified, left-justified modes
4.05 mm × 3.82 mm, 81-ball, 0.4 mm pitch WLCSP package
−40°C to +85°C operating temperature range

APPLICATIONS

Mobile phones, tablet PCs, e-books, portable media players

GENERAL DESCRIPTION

The ADAU1373 is a low power, stereo audio codec with integrated digital audio processing that supports stereo 48 kHz record and playback. The stereo audio ADCs and DACs support sampling rates from 8 kHz to 48 kHz, as well as a digital volume control.

Eight single-ended or four differential analog inputs with PGAs are provided for adjusting the gain from −12 dB to +18 dB. They can be configured for microphones or line level signals.

Two stereo digital microphone inputs are supported; four digital microphones can be connected in total. In addition, three serial digital audio input/output ports are provided with asynchronous sample rate converters (ASRCs) to support various sampling rates, allowing for flexible system design in mobile phone applications. The inputs can be mixed and selected before the ADC or configured to bypass the ADC. Two stereo DACs are included, with a flexible mixing option for routing the signals internally.

The analog output side consists of line outputs, headphone output, speaker output, and receiver output. Two stereo single-ended line level outputs, which can be configured as two differential outputs, are included. The headphone output is stereo true ground centered (eliminating the need for coupling capacitors), with efficient Class-G (rail switching) architecture. The efficient stereo filterless Class-D switching amplifier provides ~1 W of stereo power for speakers. The differential receiver amplifier can be used to connect the separate receiver speaker. Two PLL blocks, which can lock to the inputs from 8 kHz to 27 MHz, are included.

The DSP allows system designers to compensate for the real-world limitations of microphones, speakers, amplifiers, and listening environments, resulting in a dramatic improvement in perceived audio quality through equalization, multiband compression, and limiting algorithms. The SigmaStudio™ graphical development tool, which includes audio processing blocks such as filters, mixers, dynamics processors, and amplifiers for fast development of custom signal flows, is used to program the ADAU1373.

FUNCTIONAL BLOCK DIAGRAM

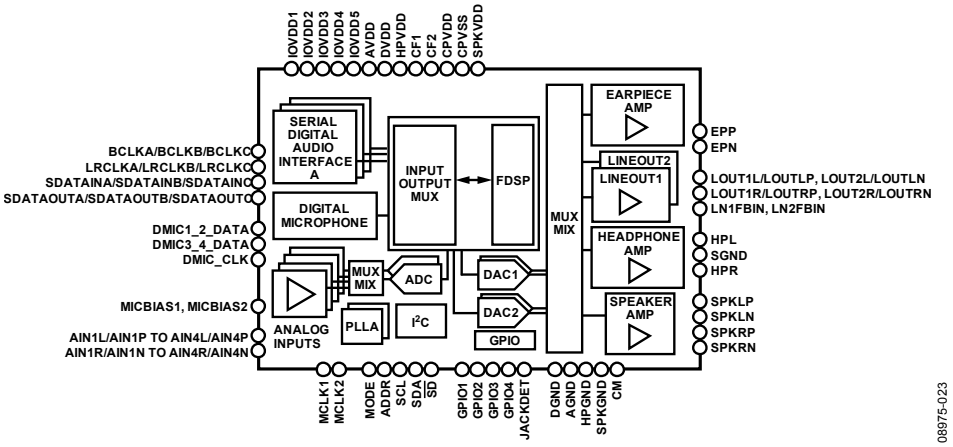

Figure 1.

Rev. 0

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Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

ADAU1373* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADAU1373 Evaluation Board

DOCUMENTATION

Data Sheet

- ADAU1373: Low Power Codec with Speaker and Headphone Amplifier

User Guides

- UG-284: ADAU1373 Evaluation Board User Guide

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADAU1373 Sound CODEC Linux Driver

DESIGN RESOURCES

- ADAU1373 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADAU1373 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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REVISION HISTORY

5/11—Revision 0: Initial Version

SPECIFICATIONS

POWER SUPPLIES

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE RANGES					
Analog	AVDD	1.62	1.8	1.98	V
Digital	DVDD[1]	1.08	1.2	1.98	V
Input/Output	IOVDD	1.62	1.8	3.6	V
Charge Pump	HPVDD	1.62	1.8	1.98	V
Speaker Amplifier	SPKVDD	2.5		5.5	V

[1] For applications using DVDD = 1.8 V, IOVDDx ≥ DVDD.

AUDIO PERFORMANCE

f_S = 48 kHz/24 bits, I²S format, AVDD = HPVDD = IOVDDx = 1.8 V, DVDD = 1.2 V, SPKVDD = 3.6 V, 1 kHz sine wave signal, 20 Hz to 20 kHz measurement bandwidth, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT PROGRAMMABLE GAIN AMPLIFIERS					
Input Resistance					
Single-Ended PGA Mode	+18 dB gain		6.8		kΩ
	0 dB gain		30		kΩ
	−12 dB gain		48		kΩ
Single-Ended Boost Mode	+29 dB gain		20		kΩ
	+9 dB gain		20		kΩ
	0 dB gain		20		kΩ
Differential PGA Mode	+18 dB gain		6.8		kΩ
	0 dB gain		30		kΩ
	−12 dB gain		48		kΩ
Differential Boost Mode	+20 dB gain		20		kΩ
	+9 dB gain		20		kΩ
	0 dB gain		20		kΩ
Gain Range					
PGA Mode	Minimum position		−12		dB
	Maximum position		+18		dB
Boost Mode	0 dB position		0		dB
	+9 dB position		+9		dB
	+20 dB position		+20		dB
Gain Step Size	PGA mode		+1		dB
Maximum Input Level					
Single-Ended PGA Mode	0 dB gain		0.545		V rms
Single-Ended Boost Mode	0 dB gain		0.545		V rms
Differential PGA Mode	0 dB gain		1.09		V rms
Differential Boost Mode	0 dB gain		1.09		V rms
Equivalent Input Noise					
Single-Ended PGA Mode	0 dB gain, unweighted 20 Hz to 20 kHz		7		μV rms
	+18 dB gain, unweighted 20 Hz to 20 kHz		28		μV rms
Single-Ended Boost Mode	0 dB gain, unweighted 20 Hz to 20 kHz		7		μV rms
	+20 dB gain, unweighted 20 Hz to 20 kHz		35		μV rms
Common-Mode Rejection Ratio					
Differential PGA Mode	0 dB gain at 217 Hz		50		dB
Mute Attenuation	Measured at line output reference to full scale (0 dB gain at 1 kHz)		80		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
MICROPHONE BIAS					
Output Voltage	Register 0x21, Bits[5:4] (MICB2GAIN); Bits[3:2] (MICB1GAIN)				
	Setting 00 = 2.9 V	1.71	1.8		V
	Setting 01 = 2.2 V	2.09	2.2		V
	Setting 10 = 2.6 V	2.47	2.6		V
	Setting 11 = 1.8 V	2.75	2.9		V
Output Current		6			mA
Output Noise	Unweighted 20 Hz to 20 kHz		7		μV rms
PSRR	AVDD at 217 Hz = 100 mV p-p		100		dB
	DVDD at 217 Hz = 100 mV p-p		100		dB
	HPVDD at 217 Hz = 100 mV p-p		100		dB
	SPKVDD at 217 Hz = 400 mV p-p		85		dB
Bias Current Detect Threshold	Register 0x22 and Register 0x23, Bits[1:0] (MICBxCURD)				
	Setting 00 = 150 μA		150		μA
	Setting 01 = 330 μA		330		μA
	Setting 10 = 510 μA		510		μA
	Setting 11 = 700 μA		700		μA
Bias Short-Circuit Detect Threshold	Register 0x22 and Register 0x23, Bits[3:2] (MICBxSHT)				
	Setting 00 = 330 μA		330		μA
	Setting 01 = 700 μA		700		μA
	Setting 10 = 1000 μA		1000		μA
	Setting 11 = 1400 μA		1400		μA
MIXER BLOCK					
Mixer ADC					
Mute Attenuation			90		dB
Mixer Line Output					
Mute Attenuation			90		dB
Mixer Headphone Output					
Mute Attenuation			90		dB
Mixer Speaker Output					
Mute Attenuation			90		dB
Mixer Earpiece Output					
Mute Attenuation			90		dB
LINE OUTPUT AMPLIFIER					
Gain			0		dB
Volume Control Step Size	Variable from mute to 0 dB in 32 steps	Mute		0	dB
Mute Attenuation			90		dB
Maximum Output Level					
Single-Ended Mode	Load = 10 kΩ		0.545		V rms
Differential Mode	Load = 10 kΩ		1.09		V rms
Output Resistance	At each output pin: LOUT1L, LOUT1R, LOUT2L, and LOUT2R		0.3		Ω
Common-Mode Voltage	V_{CM} at LOUT1L, LOUT1R, LOUT2L, and LOUT2R		AVDD/2		V
DC Offset	Differential mode between LOUTLP and LOUTLN, LOUTRP and LOUTRN		1		mV
Ground-Loop Rejection Ratio	Measured by injecting 1000 Hz sine wave,100 mV rms at LNxFBIN; referenced to full-scale output voltage		56		dB
Input Resistance into LNxFBIN Pin			120		kΩ

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
HEADPHONE AMPLIFIER					
Gain		−69	0	+6	dB
Volume Control Step Size	Variable from −69 dB to +6 dB in 32 steps	−69		+6	dB
Mute Attenuation			85		dB
Output Level at 1% THD + N	Load = 16 Ω		27		mW
	Load = 32 Ω		24		mW
	Load = 10 kΩ		1.2		V rms
Output Level at 10% THD + N	Load = 16 Ω		50		mW
	Load = 32 Ω		43		mW
	Load = 10 kΩ		1.2		V rms
Efficiency	P_{OUT} = 3 mW, HPVDD = 1.8 V, R_L = 16 Ω		25		%
	P_{OUT} = 3.5 mW, HPVDD = 1.8 V, R_L = 32 Ω		38		%
DC Offset	HPVDD = 1.8 V, R_L = 16 Ω		±3		mV
Output Limiter Threshold	Peak output at HPL, HPR; setting V_{OUT} = 1.1 V peak		1.1		V pk
	Peak output at HPL, HPR; setting V_{OUT} = 0.968 V peak		0.97		V pk
	Peak output at HPL, HPR; setting V_{OUT} = 0.815 V peak		0.82		V pk
	Peak output at HPL, HPR; setting V_{OUT} = 0.56 V peak		0.56		V pk
	Peak output at HPL, HPR; setting V_{OUT} = 0.408 V peak		0.41		V pk
	Peak output at HPL, HPR; setting V_{OUT} = 0.28 V peak		0.28		V pk
	Peak output at HPL, HPR; setting V_{OUT} = 0.23 V peak		0.23		V pk
Load Resistance		12	16		Ω
Load Capacitance				150	pF
Turn On Time			17.1		ms
Turn Off Time			1.9		ms
SPEAKER AMPLIFIER					
Gain	Setting = 12 dB		12		dB
	Setting = 18 dB		18		dB
Volume Control Step Size	Variable from mute to 0 dB in 32 steps	Mute		0	dB
Mute Attenuation			90		dB
Output Power at 1% THD + N	SPKVDD = 2.5 V, 4 Ω + 15 µH (stereo)		0.554		W
	SPKVDD = 3.6 V, 4 Ω + 15 µH (stereo)		1.212		W
	SPKVDD = 4.2 V, 4 Ω + 15 µH (stereo)		1.679		W
	SPKVDD = 5 V, 4 Ω + 15 µH (stereo)		2.4		W
	SPKVDD = 2.5 V, 8 Ω + 33 µH (stereo)		0.33		W
	SPKVDD = 3.6 V, 8 Ω + 33 µH (stereo)		0.71		W
	SPKVDD = 4.2 V, 8 Ω + 33 µH (stereo)		0.98		W
	SPKVDD = 5 V, 8 Ω + 33 µH (stereo)		1.40		W
Output Power at 10% THD + N	SPKVDD = 2.5 V, 4 Ω + 15 µH (stereo)		0.691		W
	SPKVDD = 3.6 V, 4 Ω + 15 µH (stereo)		1.511		W
	SPKVDD = 4.2 V, 4 Ω + 15 µH (stereo)		2.091		W
	SPKVDD = 5 V, 4 Ω + 15 µH (stereo)		2.99		W
	SPKVDD = 2.5 V, 8 Ω + 33 µH (stereo)		0.41		W
	SPKVDD = 3.6 V, 8 Ω + 33 µH (stereo)		0.88		W
	SPKVDD = 4.2 V, 8 Ω + 33 µH (stereo)		1.22		W
	SPKVDD = 5 V, 8 Ω + 33 µH (stereo)		1.73		W
Output Power at 1% THD + N	SPKVDD = 2.5 V, 4 Ω + 15 µH (mono)		0.588		W
	SPKVDD = 3.6 V, 4 Ω + 15 µH (mono)		1.285		W
	SPKVDD = 4.2 V, 4 Ω + 15 µH (mono)		1.78		W
	SPKVDD = 5 V, 4 Ω + 15 µH (mono)		2.55		W
	SPKVDD = 2.5 V, 8 Ω + 33 µH (mono)		0.34		W
	SPKVDD = 3.6 V, 8 Ω + 33 µH (mono)		0.73		W
	SPKVDD = 4.2 V, 8 Ω + 33 µH (mono)		1.00		W
	SPKVDD = 5 V, 8 Ω + 33 µH (mono)		1.43		W

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Output Power at 10% THD + N	SPKVDD = 2.5 V, 4 Ω + 15 µH (mono)		0.733		W
	SPKVDD = 3.6 V, 4 Ω + 15 µH (mono)		1.611		W
	SPKVDD = 4.2 V, 4 Ω + 15 µH (mono)		2.22		W
	SPKVDD = 5 V, 4 Ω + 15 µH (mono)		3.18		W
	SPKVDD = 2.5 V, 8 Ω + 33 µH (mono)		0.43		W
	SPKVDD = 3.6 V, 8 Ω + 33 µH (mono)		0.905		W
	SPKVDD = 4.2 V, 8 Ω + 33 µH (mono)		1.25		W
	SPKVDD = 5 V, 8 Ω + 33 µH (mono)		1.78		W
Efficiency	P_{OUT} = 2.4 W, SPKVDD = 5 V, R_L = 4 Ω + 15 µH (stereo)		89		%
	P_{OUT} = 1.2 W, SPKVDD = 3.6 V, R_L = 4 Ω + 15 µH (stereo)		87		%
	P_{OUT} = 1.4 W, SPKVDD = 5 V, R_L = 8 Ω + 33 µH (stereo)		93		%
	P_{OUT} = 0.71 W, SPKVDD = 3.6 V, R_L = 8 Ω + 33 µH (stereo)		92		%
Average Switching Frequency			350		kHz
R_{DS} On	NMOS at 100 mA		180		mΩ
	PMOS at 100 mA		210		mΩ
DC Offset	Gain = 12 dB, SPKVDD = 3.6 V		±3		mV
Load Resistance	Mono mode	3			Ω
	Stereo mode	4			Ω
Recovery Time from Protect Mode		256		512	ms
Turn On Time	From high-Z (mute) to outputs switching state		3.5		ms
Turn Off Time	From output switching to high-Z (mute) state		1.8		ms
EARPIECE AMPLIFIER					
Gain		0	6	12	dB
Gain Step Size			6		dB
Mute Attenuation			85		dB
Output Level at 1% THD + N	SPKVDD = 2.5 V, load = 8 Ω		53		mW
	SPKVDD = 2.5 V, load = 16 Ω		66		mW
	SPKVDD = 2.5 V, load = 32 Ω		58		mW
	SPKVDD = 3.6 V, load = 8 Ω		123		mW
	SPKVDD = 3.6 V, load = 16 Ω		103		mW
	SPKVDD = 3.6 V, load = 32 Ω		69		mW
	SPKVDD = 5 V, load = 8 Ω		140		mW
	SPKVDD = 5 V, load = 16 Ω		110		mW
	SPKVDD = 5 V, load = 32 Ω		72		mW
Output Power at 10% THD + N	SPKVDD = 2.5 V, load = 8 Ω		74		mW
	SPKVDD = 2.5 V, load = 16 Ω		91		mW
	SPKVDD = 2.5 V, load = 32 Ω		73		mW
	SPKVDD = 3.6 V, load = 8 Ω		162		mW
	SPKVDD = 3.6 V, load = 16 Ω		134		mW
	SPKVDD = 3.6 V, load = 32 Ω		89		mW
	SPKVDD = 5 V, load = 8 Ω		178		mW
	SPKVDD = 5 V, load = 16 Ω		142		mW
	SPKVDD = 5 V, load = 32 Ω		92		mW
DC Offset	SPKVDD = 3.6 V, load = 32 Ω, gain = 0 dB		±1		mV
	SPKVDD = 3.6 V, load = 32 Ω, gain = 6 dB		±2		mV
	SPKVDD = 3.6 V, load = 32 Ω, gain = 12 dB		±3		mV
Load Resistance		8			Ω
Turn On Time			9.6		ms
Turn Off Time			4.1		ms

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG INPUT → ADC → DIGITAL OUTPUT					
ADC Resolution	All ADCs		24		Bits
Dynamic Range	−60 dBFS input at 1 kHz				
Unweighted (RMS)			93		dB
A-weighted (RMS)			96		dB
Signal-to-Noise Ratio	A-weighted (rms), referred to full-scale output		96		dB
THD + N	−1 dBFS input at 1 kHz		0.01		%
Offset Error			±1		mV
Gain Drift			100		ppm/°C
Interchannel Isolation			85		dB
PSRR	AVDD ripple = 100 mV p-p at 217 Hz, input referred for PGA gain = 0 dB		85		dB
	All other supplies (HPVDD, SPKVDD, DVDD, IOVDDx) = 100 mV p-p at 217 Hz, input referred for PGA gain = 0 dB		85		dB
DIGITAL MICROPHONE INPUT → ADC→ DIGITAL OUTPUT					
Dynamic Range	−60 dBFS input at 1 kHz				dB
Unweighted (rms)			93		dB
A-weighted (rms)			96		
Signal-to-Noise Ratio	A-weighted (rms)		96		dB
THD + N	−1 dBFS at 1 kHz		0.01		%
Offset Error			±1		mV
Gain Drift			100		ppm/°C
Interchannel Isolation			85		dB
PSRR	AVDD ripple = 100 mV p-p at 217 Hz, input referred for PGA gain = 0 dB		85		dB
	All other supplies (HPVDD, SPKVDD, DVDD, IOVDDx) = 100 mV p-p at 217 Hz, input referred for PGA gain = 0 dB		85		dB
ANALOG INPUT → LINE OUTPUT					
Dynamic Range	−60 dBFS input at 1 kHz				
Unweighted (RMS)			91		dB
A-weighted (RMS)			94		dB
Signal-to-Noise Ratio	Differential line output, A-weighted (rms), referred to full-scale output		94		dB
THD + N	V_{OUT} = 1 V, 1 kHz, R_L=10 kΩ		0.013		%
	V_{OUT} = 0.5 V, 1 kHz, R_L=10 kΩ		0.017		%
Interchannel Isolation			85		dB
PSRR	AVDD ripple = 100 mV p-p at 217 Hz, input referred for PGA gain = 0 dB		85		dB
	All other supplies (HPVDD, SPKVDD, DVDD, IOVDDx) = 100 mV p-p at 217 Hz, input referred for PGA gain = 0 dB		85		dB
ANALOG INPUT → HEADPHONE OUTPUT					
Dynamic Range	−60 dBFS input at 1 kHz				
	Unweighted (rms)		96		dB
	A-weighted (rms)		99		dB
Signal-to-Noise Ratio	A-weighted (rms), referred to full-scale output		99		dB
THD + N	P_{OUT} = 27 mW, 1 kHz, R_L = 16 Ω		0.01		%
Interchannel Isolation			85		dB
PSRR	HPVDD ripple = 100 mV p-p at 217 Hz, input referred for PGA gain = 0 dB		85		dB
	All other supplies (AVDD, SPKVDD, DVDD, IOVDDx) = 100 mV p-p at 217 Hz, input referred for PGA gain = 0 dB		85		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG INPUT → SPEAKER OUTPUT					
Dynamic Range	−60 dBFS input at 1 kHz				
	Unweighted (rms)		98		dB
	A-weighted (rms)		101		dB
Signal-to-Noise Ratio	A-weighted (rms), referred to 0.7 W at 3.6 V, R_L = 8 Ω		101		dB
THD + N	SPKVDD = 5 V, P_{OUT} = 1 W, 1 kHz, R_L = 8 Ω		0.013		%
	SPKVDD = 3.6 V, P_{OUT} = 0.5 W, 1kHz, R_L = 8 Ω		0.017		%
Interchannel Isolation			85		dB
PSRR	SPKVDD ripple = 100 mV p-p at 217 Hz, input referred for PGA gain = 12 dB		85		dB
	All other supplies (AVDD, HPVDD, DVDD, IOVDDx) = 100 mV p-p at 217 Hz, input referred for PGA gain = 12 dB		85		dB
ANALOG INPUT → EARPIECE OUTPUT					
Dynamic Range	−60 dBFS input at 1 kHz				
	Unweighted (rms)		95		dB
	A-weighted (rms)		98		dB
Signal-to-Noise Ratio	A-weighted (rms), referred to 40 mW at 3.6 V, R_L = 32 Ω		98		dB
THD + N	P_{OUT} = 60 mW, 1 kHz, R_L = 8 Ω		0.1		%
	P_{OUT} = 30 mW, 1 kHz, R_L = 8 Ω		0.2		%
PSRR	AVDD ripple = 100 mV p-p at 217 Hz, input referred for PGA gain = 12 dB		85		dB
	All other supplies (HPVDD, DVDD, SPKVDD, IOVDDx) = 100 mV p-p at 217 Hz, input referred for PGA gain = 12 dB		85		dB
DIGITAL INPUT → DAC → MIXER → LINE OUTPUT					
Dynamic Range	20 Hz to 20 kHz, −60 dBFS input, unweighted (rms)		93		dB
	20 Hz to 20 kHz, −60 dBFS input, A-weighted (rms)		96		dB
Signal-to-Noise Ratio	20 Hz to 20 kHz, A-weighted, relative to full scale		96		dB
THD + N	At −1 dBFS, 1 kHz		0.01		%
Full-Scale Output Voltage	Scales linearly with AVDD		1.0		V rms
Interchannel Isolation			100		dB
Interchannel Phase Deviation			0.1		Degrees
Digital Volume Control					
Step			0.375		dB
Range			95		dB
PSRR	AVDD ripple = 100 mV p-p at 217 Hz, input referred for PGA gain = 12 dB		85		dB
	All other supplies (HPVDD, DVDD, SPKVDD, IOVDDx) = 100 mV p-p at 217 Hz, input referred for PGA gain = 12 dB		85		dB
DIGITAL INPUT → DAC → MIXER → HEADPHONE OUTPUT					
Dynamic Range	20 Hz to 20 kHz, −60 dBFS input, unweighted (rms)		96		dB
	20 Hz to 20 kHz, −60 dBFS input, A-weighted (rms)		99		dB
Signal-to-Noise Ratio	20 Hz to 20 kHz, A-weighted, relative to full scale		99		dB
THD + N	At −1 dBFS, 1 kHz		0.01		%
Full-Scale Output Voltage					V rms
Interchannel Isolation			100		dB
Interchannel Phase Deviation			0.1		Degrees
Digital Volume Control					
Step			0.375		dB
Range			95		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUT → DAC → MIXER → SPEAKER OUTPUT					
Dynamic Range	20 Hz to 20 kHz, −60 dBFS input, unweighted (rms)		93		dB
	20 Hz to 20 kHz, −60 dBFS input, A-weighted (rms)		96		dB
Signal-to-Noise Ratio	20 Hz to 20 kHz, A-weighted, relative to full scale		97		dB
THD + N	At −1 dBFS, 1 kHz		0.01		%
Interchannel Isolation			100		dB
Interchannel Phase Deviation			0.1		Degrees
Digital Volume Control					
Step			0.375		dB
Range			95		dB
DIGITAL INPUT→ DAC → MIXER → EARPIECE OUTPUT					
Dynamic Range	20 Hz to 20 kHz, −60 dBFS input, unweighted (rms)		93		dB
	20 Hz to 20 kHz, −60 dBFS input, A-weighted (rms)		96		dB
Signal-to-Noise Ratio	20 Hz to 20 kHz, A-weighted, relative to full scale		97		dB
THD + N	At −1 dBFS, 1 kHz		0.1		%
Full-Scale Output Voltage	Scales linearly with SPKVDD; SPKVDD = 3.6 V		1.53		V rms
Digital Volume Control					
Step			0.375		dB
Range			95		dB
REFERENCE					
Common-Mode Reference Output	CM pin		AVDD/2		V
CHARGE PUMP					
Supply Voltage		1.62	1.8	1.98	V
Outputs					
CPVDD					
Below Supply Switching Threshold			0.9		V
Above Supply Switching Threshold			1.8		V
CPVSS					
Below Supply Switching Threshold			−0.9		V
Above Supply Switching Threshold			−1.8		V
Switching Frequency			500		kHz
Flying Capacitor Value		0.47	1	10	µF
Supply Switching Threshold			0.4		V
Start-Up Time			0.5		ms
PLLx					
Input Frequency		0.008		27	MHz
Lock Time (Analog PLL)			3		ms
Jitter (Cycle-to-Cycle) rms	Measured at GPIOx with master clock output set at 256 × f_S (12.288 MHz, where f_S = 48 kHz)				
Analog PLL Only (DPLL Bypassed)					
8 MHz Input (Fractional Mode)			470		ps
27 MHz Input (Fractional Mode)			280		ps
12.288 MHz Input (Integer Mode)			200		ps
Digital PLL + Analog PLL					
8 kHz LRCLKx Input			310		ps
96 kHz LRCLKx Input			260		ps
512 kHz (8 kHz × 64) BCLKx Input			310		ps
2.048 MHz (8 kHz × 256) MCLKx Input			210		ps
MCLKx Clock Output Frequency				49.152	MHz
GPIOx					
Drive Capability	IOVDDx = 1.8 V		4		mA
	IOVDDx = 3.3 V		20		mA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
IRQ RESPONSE TIME					
ASRCx_IRQ_STATUS	One clock cycle = 1/256 × f_S = 81.4 ns at f_S = 48 kHz		4		Clock cycles
DRC_IRQ_STATUS, PLL_UNLOCK_STATUS			3		Clock cycles
HP_CFG_STATUS, HP_DECT_STATUS, AFAULT_STATUS			256 ms + 3		Clock cycles
JACK DETECT					
Debounce Time			128		ms
DIGITAL MICROPHONE INPUT					
Clock Output Frequency	Depends on internal sample rate = 64 × f_S		3.072		MHz
Decimator Operating Frequency	Depends on internal sample rate = 128 × f_S		6.144		MHz

POWER CONSUMPTION

Table 3 lists some commonly used paths, as well as the typical current that is consumed by the part under quiescent conditions. The total power consumed includes the power in the loads, as specified. T_A = 25°C, line output load = 10 kΩ, headphone stereo = 16 Ω, speaker load = 8 Ω + 33 μH, and earpiece = 32 Ω, audio port configured as the slave, f_S = 48 kHz, MCLK = 12.288 MHz, unless otherwise specified.

Table 3.

Mode	AVDD (V)	DVDD (V)	HPVDD (V)	SPKVDD (V)	IOVDD (V)	I_{AVDD} (mA)	I_{DVDD} (mA)	I_{HPVDD} (mA)	I_{SPKVDD} (mA)	I_{IOVDD} (mA)	Total Power (mW)
POWER-DOWN											
No Clocks	1.62	1.08	1.62	2.5	1.62	0.008	0.01	0.001	0.0014	0.008	0.04184
	1.8	1.2	1.8	3.6	1.8	0.012	0.011	0.0014	0.0035	0.008	0.06432
	1.8	1.2	1.8	4.2	1.8	0.0124	0.011	0.0015	0.0055	0.008	0.07572
	1.98	1.98	1.98	5.5	3.63	0.0178	0.0149	0.002	0.0147	0.008	0.178596
MCLKx = 12.288 MHz	1.62	1.08	1.62	2.5	1.62	0.032	0.19	0.001	0.0014	0.017	0.2897
	1.8	1.2	1.8	3.6	1.8	0.0378	0.22	0.0014	0.0035	0.017	0.37776
	1.8	1.2	1.8	4.2	1.8	0.0378	0.22	0.0015	0.0055	0.017	0.38844
	1.98	1.98	1.98	5.5	3.63	0.045	0.4	0.002	0.0147	0.017	1.02762
POWER-UP											
No Clocks (Default State)	1.62	1.08	1.62	2.5	1.62	0.31	0.046	0.0012	0.041	0.008	0.669284
	1.8	1.2	1.8	3.6	1.8	0.32	0.0495	0.0018	0.065	0.008	0.88704
	1.8	1.2	1.8	4.2	1.8	0.32	0.0495	0.0018	0.079	0.008	0.98484
	1.98	1.98	1.98	5.5	3.63	0.34	0.083	0.0023	0.118	0.008	1.520134
MCLKx = 12.288 MHz, PLL Bypassed	1.62	1.08	1.62	2.5	1.62	0.34	0.23	0.0013	0.041	0.017	0.931346
	1.8	1.2	1.8	3.6	1.8	0.35	0.256	0.0018	0.065	0.017	1.20504
	1.8	1.2	1.8	4.2	1.8	0.35	0.256	0.0018	0.079	0.017	1.30284
	1.98	1.98	1.98	5.5	3.63	0.37	0.47	0.0023	0.118	0.017	2.378464
With Clocks (PLL Enabled, LRCLKA = 48 kHz, DPLL + APLL Enabled, Master Mode)	1.62	1.08	1.62	2.5	1.62	1.77	1.06	0.0013	0.041	1.72	6.903206
	1.8	1.2	1.8	3.6	1.8	1.83	1.26	0.0018	0.065	1.72	8.13924
	1.8	1.2	1.8	4.2	1.8	1.83	1.26	0.0018	0.079	1.72	8.23704
	1.98	1.98	1.98	5.5	3.63	1.91	2.34	0.0023	0.118	1.72	15.31215
ANALOG BYPASS (NO CLOCKS)											
Analog Input → Line Output	1.62	1.08	1.62	2.5	1.62	1.62	0.045	0.0012	0.041	0.008	2.790404
	1.8	1.2	1.8	3.6	1.8	1.66	0.049	0.0018	0.068	0.008	3.30924
	1.8	1.2	1.8	4.2	1.8	1.66	0.049	0.0018	0.086	0.008	3.42564
	1.98	1.98	1.98	5.5	3.63	1.72	0.083	0.0023	0.128	0.008	4.307534
Analog Input → Headphone Output	1.62	1.08	1.62	2.5	1.62	1.33	0.045	1.35	0.041	0.008	4.50566
	1.8	1.2	1.8	3.6	1.8	1.35	0.05	1.37	0.065	0.008	5.2044
	1.8	1.2	1.8	4.2	1.8	1.35	0.05	1.37	0.079	0.008	5.3022
	1.98	1.98	1.98	5.5	3.63	1.37	0.083	1.39	0.118	0.008	6.30718
Analog Input → Speaker Output (Mono)	1.62	1.08	1.62	2.5	1.62	1.44	0.045	0.0012	3.58	0.008	11.3463
	1.8	1.2	1.8	3.6	1.8	1.46	0.05	0.0018	4.47	0.008	18.79764
	1.8	1.2	1.8	4.2	1.8	1.47	0.05	0.0018	4.92	0.008	23.38764
	1.98	1.98	1.98	5.5	3.63	1.49	0.083	0.0023	5.94	0.008	35.81813
Analog Input → Speaker Output (Stereo)	1.62	1.08	1.62	2.5	1.62	1.98	0.045	0.0012	5.67	0.008	17.4461
	1.8	1.2	1.8	3.6	1.8	2.02	0.05	0.0018	7.17	0.008	29.52564
	1.8	1.2	1.8	4.2	1.8	2.01	0.05	0.0018	7.99	0.008	37.25364
	1.98	1.98	1.98	5.5	3.63	2.04	0.083	0.0023	9.77	0.008	57.97213
Analog Input → Earpiece Output	1.62	1.08	1.62	2.5	1.62	0.89	0.045	0.0012	0.82	0.008	3.555304
	1.8	1.2	1.8	3.6	1.8	0.91	0.049	0.0018	0.9	0.008	4.95444
	1.8	1.2	1.8	4.2	1.8	0.91	0.049	0.0018	0.94	0.008	5.66244
	1.98	1.98	1.98	5.5	3.63	0.92	0.083	0.0023	1.07	0.008	7.904534

Mode	AVDD (V)	DVDD (V)	HPVDD (V)	SPKVDD (V)	IOVDD (V)	I_{AVDD} (mA)	I_{DVDD} (mA)	I_{HPVDD} (mA)	I_{SPKVDD} (mA)	I_{IOVDD} (mA)	Total Power (mW)
RECORD PATH (MCLK = 12.288 MHz)											
Analog Input → ADC → Digital Audio Interface A	1.62	1.08	1.62	2.5	1.62	2.73	0.73	0.0014	0.041	0.017	5.343308
	1.8	1.2	1.8	3.6	1.8	3.42	0.64	0.0018	0.065	0.017	7.19184
	1.8	1.2	1.8	4.2	1.8	3.4	0.64	0.0018	0.079	0.017	7.25364
	1.98	1.98	1.98	5.5	3.63	3.78	1.15	0.0023	0.0118	0.017	9.892564
Digital Microphone Input → Decimator → Digital Audio Interface A	1.62	1.08	1.62	2.5	1.62	0.038	0.59	0.0012	0.041	0.017	0.830744
	1.8	1.2	1.8	3.6	1.8	0.044	0.655	0.0018	0.065	0.017	1.13304
	1.8	1.2	1.8	4.2	1.8	0.044	0.655	0.0018	0.079	0.017	1.23084
	1.98	1.98	1.98	5.5	3.63	0.05	1.18	0.0023	0.0118	0.017	2.566564
PLAYBACK PATH											
Digital Input → DAC → Line Output	1.62	1.08	1.62	2.5	1.62	2.62	0.045	0.0012	0.041	0.017	4.424984
	1.8	1.2	1.8	3.6	1.8	2.82	0.82	0.0018	0.068	0.017	6.33864
	1.8	1.2	1.8	4.2	1.8	2.82	0.82	0.0018	0.086	0.017	6.45504
	1.98	1.98	1.98	5.5	3.63	2.92	1.486	0.0023	0.128	0.017	9.494144
Digital Input → DAC → Headphone Output	1.62	1.08	1.62	2.5	1.62	2.44	0.73	1.35	0.041	0.017	7.05824
	1.8	1.2	1.8	3.6	1.8	2.51	0.82	1.37	0.068	0.017	8.2434
	1.8	1.2	1.8	4.2	1.8	2.51	0.82	1.37	0.086	0.017	8.3598
	1.98	1.98	1.98	5.5	3.63	2.59	1.49	1.39	0.128	0.017	11.59631
Digital Input → DAC → Speaker Output	1.62	1.08	1.62	2.5	1.62	3.09	0.732	0.0013	5.68	0.017	20.02601
	1.8	1.2	1.8	3.6	1.8	3.18	0.82	0.0018	7.17	0.017	32.55384
	1.8	1.2	1.8	4.2	1.8	3.18	0.82	0.0018	7.97	0.017	40.21584
	1.98	1.98	1.98	5.5	3.63	3.27	1.49	0.0023	9.73	0.017	63.00606
Digital Input → DAC → Earpiece Output	1.62	1.08	1.62	2.5	1.62	1.97	0.66	0.0012	0.82	0.017	5.983684
	1.8	1.2	1.8	3.6	1.8	2.06	0.74	0.0018	0.897	0.017	7.85904
	1.8	1.2	1.8	4.2	1.8	2.06	0.74	0.0018	0.94	0.017	8.57784

DIGITAL FILTER/SRC CHARACTERISTICS

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC DECIMATION FILTER					
Pass Band	±0.04 dB	0		0.423 f_S	Hz
	−6 dB		0.5 f_S		Hz
Pass-Band Ripple				±0.04	dB
Stop Band		0.577 f_S			Hz
Stop-Band Attenuation	f > 0.577 f_S	−60			dB
Group Delay [1950/(128 × f_S)]	f_S = 48 kHz		0.317		ms
DAC INTERPOLATION FILTER					
Pass Band	±0.03 dB	0		0.423 f_S	Hz
	−6 dB		0.5 f_S		Hz
Pass-Band Ripple				±0.03	dB
Stop Band		0.577 f_S			Hz
Stop-Band Attenuation	f > 0.577 f_S	−60			dB
Group Delay [1791/(128 × f_S)]	f_S = 48 kHz		0.292		ms
SAMPLE RATE CONVERTER					
Pass Band	0.04 dB	0		0.418 f_S	Hz
	−6 dB		0.5 f_S		Hz
Pass-Band Ripple				0.02	dB
Stop Band		0.582 f_S			Hz
Stop-Band Attenuation	f > 0.582 f_S	−100			dB
Output/Input Sample Rate Ratio		1:8		8:1	
Signal-to-Noise Ratio, A-weighted				100	dB
Dynamic Range, A-weighted		100		120	dB
THD + N		90			dB
Maximum Group Delay	48 kHz in, 8 kHz out		3.7		ms
Maximum Start-Up Time	48 kHz in, 8 kHz out		15		ms

DIGITAL INPUT/OUTPUT SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT SPECIFICATIONS					
Input Voltage High (V_{IH})		0.6 × IOVDD			V
Input Voltage Low (V_{IL})				0.25 × IOVDD	V
Input Leakage	I_{IH} at V_{IH} = 2.4 V			10	µA
	I_{IL} at V_{IL} = 0.8 V			10	µA
OUTPUT SPECIFICATIONS					
High Output Voltage High (V_{OH})	I_{OH} = 1 mA	IOVDD − 0.6			V
Output Voltage Low (V_{OL})	I_{OL} = 1 mA			0.4	V
INPUT CAPACITANCE				5	pF

DIGITAL TIMING SPECIFICATIONS

−40°C < T_A < +85°C, IOVDDx = 1.8 V ± 10%.

Table 6.

Parameter	Limit		Unit	Description
	t_{MIN}	t_{MAX}		
MASTER CLOCK				
Duty Cycle	45	55	%	
SERIAL PORT				
t_{BIL}	5		ns	BCLKx pulse width low
t_{BIH}	5		ns	BCLKx pulse width high
t_{LIS}	5		ns	LRCLKx setup; time to BCLK rising
t_{LIH}	5		ns	LRCLKx hold; time from BCLK rising
t_{SIS}	5		ns	DAC_SDATA setup; time to BCLK rising
t_{SIH}	5		ns	DAC_SDATA hold; time from BCLK rising
t_{SODM}		50	ns	ADC_SDATA delay; time from BCLK falling in master mode
I²C PORT				
f_{SCL}		400	kHz	SCL frequency
t_{SCLH}	0.6		µs	SCL high
t_{SCLL}	1.3		µs	SCL low
t_{SCS}	0.6		µs	Setup time; relevant for repeated start condition
t_{SCH}	0.6		µs	Hold time; after this period of time, the first clock is generated
t_{DS}	100		ns	Data setup time
t_{DH}	5		ns	Data hold time
t_{SCR}		300	ns	SCL rise time
t_{SCF}		300	ns	SCL fall time
t_{SDR}		300	ns	SDA rise time
t_{SDF}		300	ns	SDA fall time
t_{BFT}	0.6		µs	Bus-free time; time between stop and start
DIGITAL MICROPHONE				R_L = 1 MΩ, C_L = 14 pF
t_{DCF}		10	ns	Digital microphone clock fall time
t_{DCR}		10	ns	Digital microphone clock rise time
t_{DDV}	22	30	ns	Digital microphone delay time for valid data
t_{DDH}	0	12	ns	Digital microphone delay time for data, three-stated

Digital Timing Diagrams

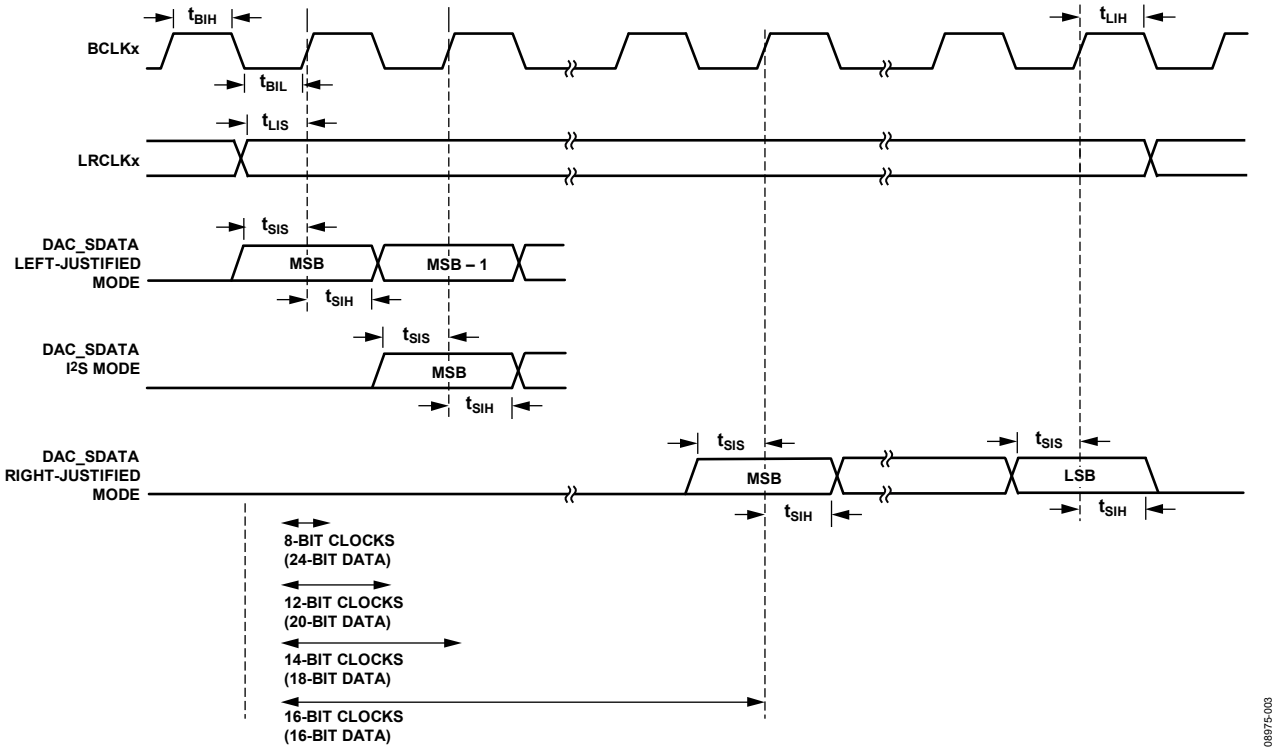

Figure 2. Serial Input Port Timing

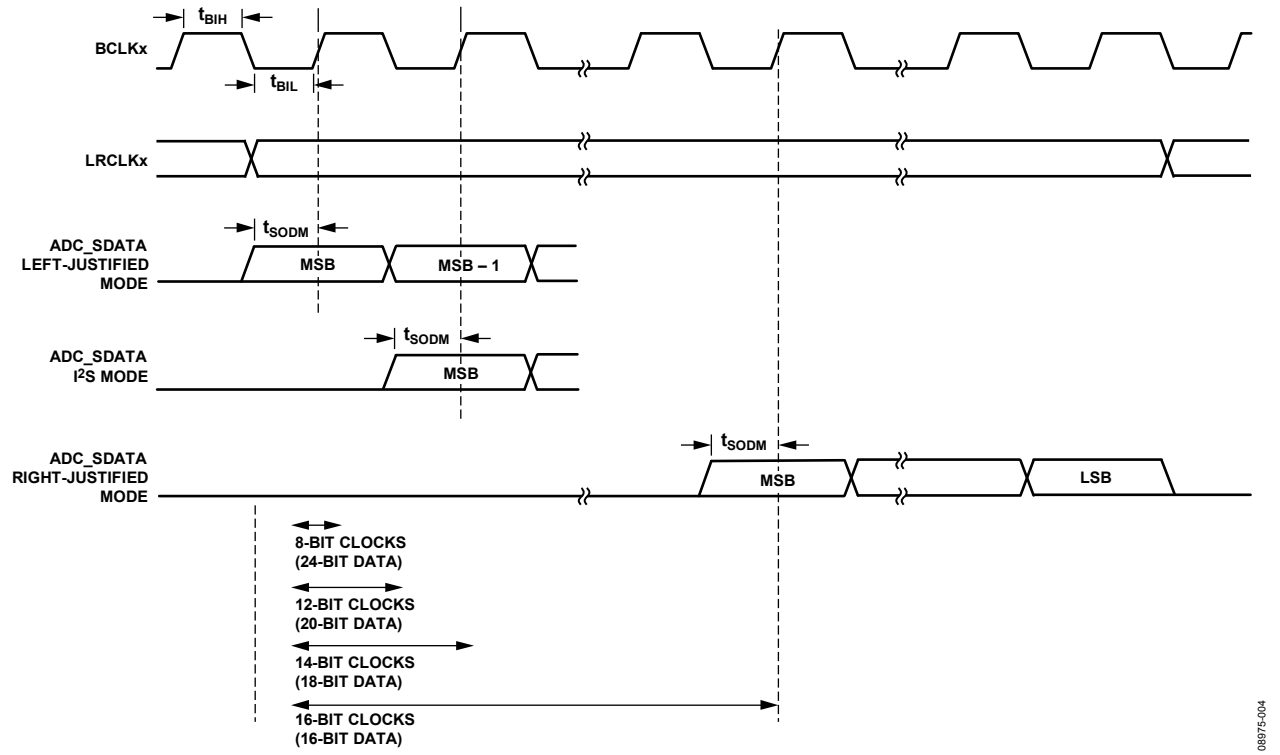

Figure 3. Serial Output Port Timing

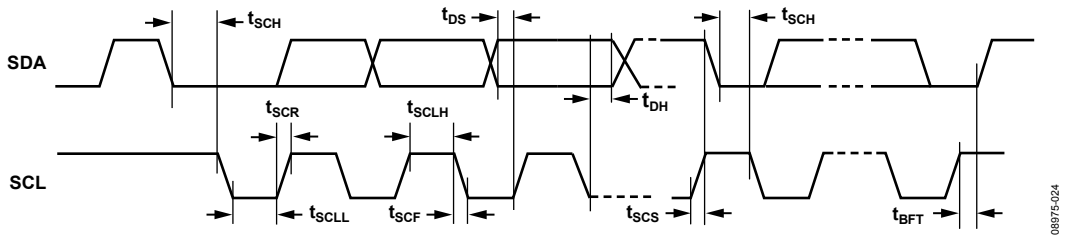

Figure 4. I²C Port Timing

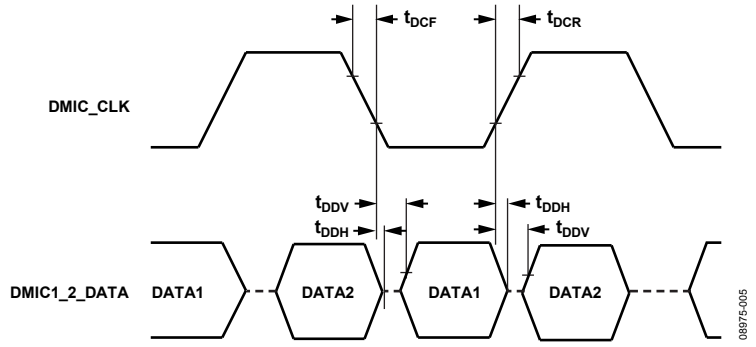

Figure 5. Digital Microphone Timing

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Power Supply	
SPKVDD, IOVDDx	−0.3 V to +5.5 V
DVDD, AVDD	−0.3 V to +1.98 V
HPVDD	−0.3 V to +1.98 V
Analog Input Voltage (Signal Pins)	
AIN4R/AIN4N, AIN3R/AIN3N, AIN2R/AIN2N, AIN1R/AIN1N, AIN4L/AIN4P, AIN3L/AIN3P, AIN2L/AIN4P, AIN1L/AIN1P	−0.3 V to AVDD + 0.3 V
Digital Input Voltage (Signal Pins)	
MCLK1, BCLKA, LRCLKA, SDATAINA, GPIO1	−0.3 V to IOVDD1 + 0.3 V
MCLK2, BCLKB, LRCLKB, SDATAINB, GPIO2	−0.3 V to IOVDD2 + 0.3 V
BCLKC, LRCLKC, SDATAINC, GPIO3	−0.3 V to IOVDD3 + 0.3 V
DMIC1_2_DATA, DMIC3_4_DATA, DMIC_CLK	−0.3 V to IOVDD4 + 0.3 V
SDA, SCL, GPIO4, MODE, ADDR, $\overline{SD}$	−0.3 V to IOVDD5 + 0.3 V
Temperature	
Operating Range	−40°C to +85°C
Storage Range	−65°C to +150°C
Junction Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 8. Thermal Resistance

Package Type	θ_{JA}	Unit
81-Lead, 4.0 mm × 3.8 mm WLCSP[1]	30	°C/W

[1] Applicable for a 4-layer board. For more information on the WLCSP, see the AN-617 Application Note, *MicroCSP Wafer Level Chip Scale Package*.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

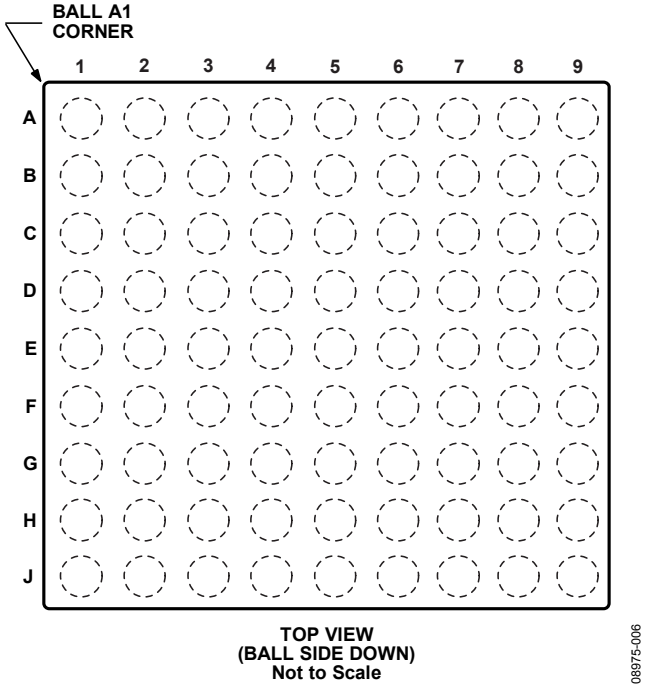

Figure 6. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
A1	DGND	PWR	Digital Ground. The AGND and DGND pins must be tied directly together in a common ground plane.
A2	MODE	D_IN	Mode Select I²C Operation. Must be pulled low for I²C mode.
A3	IOVDD4	PWR	Supply for Digital Microphone Input Port. Set IOVDD4 between 1.8 V and 3.3 V and decouple to DGND using a 100 nF capacitor.
A4	DMIC_CLK	D_OUT	Clock Output for Digital Microphone.
A5	AIN4R/AIN4N	A_IN	Right Channel Input 4 (AIN4R)/Inverting Input 4 (AIN4N).
A6	AIN3R/AIN3N	A_IN	Right Channel Input 3 (AIN3R)/Inverting Input 3 (AIN3N).
A7	AIN2R/AIN2N	A_IN	Right Channel Input 2 (AIN2R)/Inverting Input 2 (AIN2N).
A8	AIN1R/AIN1N	A_IN	Right Channel Input 1 (AIN1R)/Inverting Input 1 (AIN1N).
A9	AVDD	PWR	1.5 V to 1.8 V Analog Supply for DAC and Microphone Bias. Decouple this pin to AGND using a 100 nF capacitor.
B1	DVDD	PWR	Digital Core Supply. Decouple this pin to DGND with a 100 nF capacitor.
B2	ADDR	D_IN	Address Setting Pin for I²C Port. Pull high/low to IOVDD4, using a resistor for the desired chip address.
B3	IOVDD5	PWR	Supply for I²C Port. Set IOVDD5 between 1.8 V and 3.3 V and decouple to DGND using a 100 nF capacitor.
B4	DMIC1_2_DATA	D_IN	Serial Data Input Digital Microphone 1 and Serial Data Input Digital Microphone 2.
B5	AIN4L/AIN4P	A_IN	Left Channel Input 4 (AIN4L)/Noninverting Input 4 (AIN4P).
B6	AIN3L/AIN3P	A_IN	Left Channel Input 3 (AIN3L)/Noninverting Input 3 (AIN3P).
B7	AIN2L/AIN2P	A_IN	Left Channel Input 2 (AIN2L)/Noninverting Input 2 (AIN2P).
B8	AIN1L/AIN1P	A_IN	Left Channel Input 1 (AIN1L)/Noninverting Input 1 (AIN1P).
B9	CM	A_OUT	AVDD/2 V Common-Mode Reference. Connect a 1 µF ceramic decoupling capacitor between this pin and ground to reduce crosstalk between the ADCs and DACs. This pin can be used to bias external analog circuits, as long as they are not drawing current from CM (for example, the noninverting input of an op amp).

Pin No.	Mnemonic	Type	Description
C1	IOVDD1	PWR	Supply for Digital Audio Input/Output Interface A. Set IOVDD1 between 1.8 V and 3.3 V. Decouple this pin to DGND with a 100 nF capacitor.
C2	MCLK1	D_IN	External Master Clock Input 1 (8 kHz to 27 MHz).
C3	SDA	D_I/O	Serial Data for I²C. This pin is a bidirectional open drain and must be pulled up to IOVDD5 with a resistor.
C4	GPIO4	D_I/O	General-Purpose Input/Output 4.
C5	SCL	D_IN	Serial Clock for I²C Port. This pin is input only and must be pulled up to IOVDD5 with a resistor.
C6	DMIC3_4_DATA	D_IN	Serial Data Input Digital Microphone 3 and Serial Data Input Digital Microphone 4.
C7	LOUT1L/LOUTLP	A_OUT	Left Channel Line Output 1, Single-Ended Mode (LOUT1L)/Noninverting Left Channel Line Output, Differential Mode (LOUTLP).
C8	MICBIAS1	A_OUT	Bias Voltage for Electret Microphone 1.
C9	MICBIAS2	A_OUT	Bias Voltage for Electret Microphone 2.
D1	MCLK2	D_IN	External Master Clock Input 2 (8 kHz to 27 MHz).
D2	BCLKA	D_I/O	Serial Bit Clock, Digital Audio Interface A.
D3	LRCLKA	D_I/O	Frame Clock, Digital Audio Interface A.
D4	SDATAOUTA	D_OUT	Serial Data Output, Digital Audio Interface A.
D5	SDATAINA	D_IN	Serial Data Input, Digital Audio Interface A.
D6	GPIO1	D_I/O	General-Purpose Input/Output 1.
D7	LOUT1R/LOUTRP	A_OUT	Right Channel Line Output 1, Single-Ended Mode (LOUT1R)/Noninverting Right Channel Line Output, Differential Mode (LOUTRP).
D8	LOUT2L/LOUTLN	A_OUT	Left Channel Line Output 2, Single-Ended Mode (LOUT2L)/Inverting Left Channel Line Output, Differential Mode (LOUTLN).
D9	LOUT2R/LOUTRN	A_OUT	Right Channel Line Output 2, Single-Ended Mode (LOUT2R)/Inverting Right Channel Line Output, Differential Mode (LOUTRN).
E1	IOVDD3	PWR	Supply for Digital Audio Input/Output Interface C. Set IOVDD3 between 1.8 V and 3.3 V and decouple to DGND with a 100 nF capacitor.
E2	LRCLKB	D_I/O	Frame Clock, Digital Audio Interface B.
E3	SDATAOUTB	D_OUT	Serial Data Output, Digital Audio Interface B.
E4	BCLKB	D_I/O	Serial Bit Clock, Digital Audio Interface B.
E5	DGND	PWR	Digital Ground. The AGND and DGND pins must be tied directly together in a common ground plane.
E6	GPIO2	D_I/O	General-Purpose Input/Output 2.
E7	LN1FBIN	A_IN	Line Output Amplifier 1 Feedback. This pin can be used to sense the ground noise at the line output jack; use a 2.2 µF capacitor to connect this pin to AGND at the line output jack.
E8	LN2FBIN	A_IN	Line Output Amplifier 2 Feedback. This pin can be used to sense the ground noise at the line output jack; use a 2.2 µF capacitor to connect this pin to AGND at the line output jack.
E9	AVDD	PWR	1.5 V to 1.8 V Analog Supply for DAC and Microphone Bias. Decouple this pin to AGND with a 100 nF capacitor in parallel with a 10 µF capacitor.
F1	LRCLKC	D_I/O	Frame Clock, Digital Audio Interface C.
F2	BCLKC	D_I/O	Serial Bit Clock, Digital Audio Interface C.
F3	SDATAINC	D_IN	Serial Data Input, Digital Audio Interface C.
F4	IOVDD2	PWR	Supply for Digital Audio Input/Output Interface B. Set IOVDD2 between 1.8 V and 3.3 V and decouple to DGND with a 100 nF capacitor.
F5	GPIO3	D_I/O	General-Purpose Input/Output 3.
F6	SDATAINB	D_IN	Serial Data Input, Digital Audio Interface B.
F7, F8	AGND	PWR	Analog Ground.
F9	RESERVED	A_IN	Reserved for Internal Use. Do not connect.
G1, G2	SPKVDD	PWR	Supply for Speaker Class-D Amplifier.
G3	SDATAOUTC	D_OUT	Serial Data Output, Digital Audio Interface C.
G4	RESERVED	D_IN	Reserved. Connect to DGND.
G5	JACKDET	D_IN	TLL-Compatible Logic Input. Detects insertion/removal of headphone plug.
G6	$\overline{SD}$	D_IN	Shutdown Control. Set high for normal operation; set low for full chip power-down.
G7	SGND	A_IN	Headphone Signal Return Sense. Connect directly to headphone socket ground for lowest dc offset.
G8	HPL	A_OUT	Left Headphone Output.
G9	HPR	A_OUT	Right Headphone Output.

Pin No.	Mnemonic	Type	Description
H1	SPKRN	A_OUT	Right Channel Speaker Output, Negative.
H2, H3	SPKVDD	PWR	Supply for Speaker Amplifier.
H4, H5	SPKGND	PWR	Ground for Speaker Amplifier.
H6	EPP	A_OUT	Earpiece Amplifier Output, Positive.
H7	CPVSS	PWR	Headphone Amplifier Charge Pump, Negative Supply Output. Decouple this pin to HPGND with a 1 µF MLCC X7R capacitor.
H8	HPVDD	PWR	1.62 V to 2 V Supply for Headphone Amplifier Charge Pump. Decouple this pin to AGND with a 1 µF capacitor.
H9	CPVDD	PWR	Headphone Amplifier Charge Pump, Positive Supply Output. Decouple this pin to HPGND with a 1 µF MLCC X7R capacitor.
J1	SPKGND	PWR	Ground for Speaker Amplifier.
J2	SPKRP	A_OUT	Right Channel Speaker Output, Positive.
J3	SPKLN	A_OUT	Left Channel Speaker Output, Negative.
J4	SPKLP	A_OUT	Left Channel Speaker Output, Positive.
J5	SPKGND	PWR	Ground for Speaker Amplifier.
J6	EPN	A_OUT	Earpiece Amplifier Output, Negative.
J7	CF2	PWR	Charge Pump Flying Capacitor Connection 2.
J8	HPGND	PWR	Charge Pump Ground.
J9	CF1	PWR	Charge Pump Flying Capacitor Connection 1.