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SigmaDSP Digital Audio Processor with Flexible Audio Routing Matrix

Data Sheet

ADAU1442/ADAU1445/ADAU1446

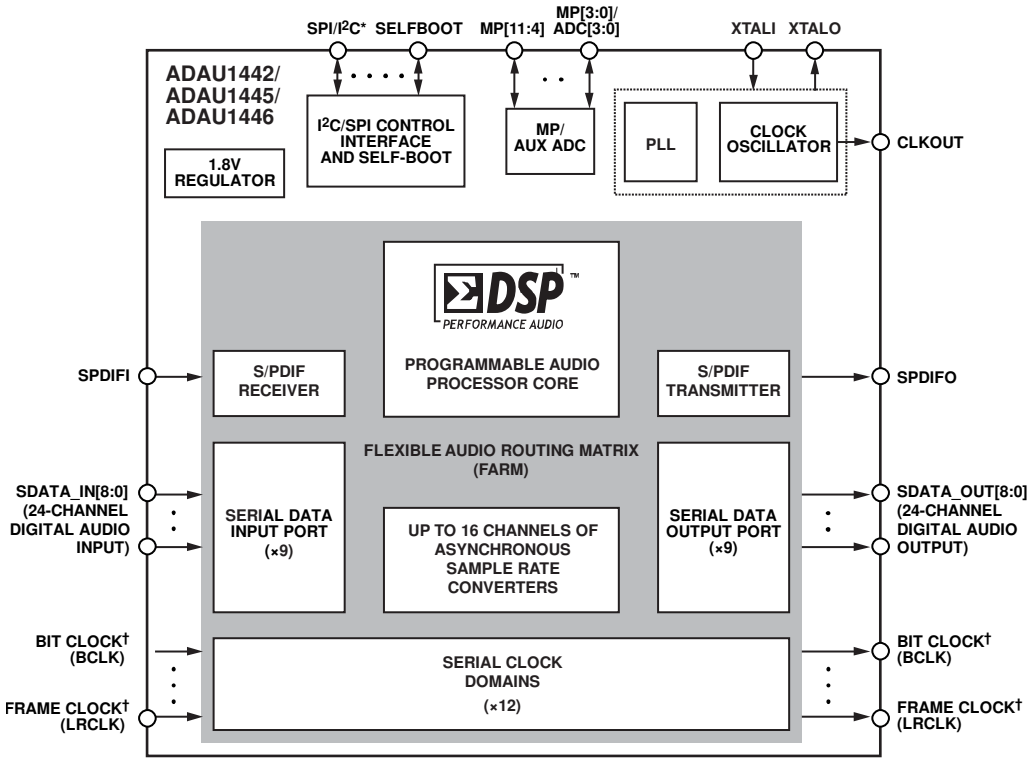
FEATURES

- Fully programmable audio digital signal processor (DSP) for enhanced sound processing
- Features SigmaStudio, a proprietary graphical programming tool for the development of custom signal flows
- 172 MHz SigmaDSP core; 3584 instructions per sample at 48 kHz
- 4k parameter RAM, 8k data RAM
- Flexible audio routing matrix (FARM)
  - 24-channel digital input and output
  - Up to 8 stereo asynchronous sample rate converters (from 1:8 up to 7.75:1 ratio and 139 dB DNR)
  - Stereo S/PDIF input and output
- Supports serial and TDM I/O, up to f_S = 192 kHz
- Multichannel byte-addressable TDM serial port
- Pool of 170 ms digital audio delay (at 48 kHz)
- Clock oscillator for generating master clock from crystal
- PLL for generating core clock from common audio clocks
- I²C and SPI control interfaces
- Standalone operation
  - Self-boot from serial EEPROM
  - 4-channel, 10-bit auxiliary control ADC
  - Multipurpose pins for digital controls and outputs
- Easy implementation of available third-party algorithms
- On-chip regulator for generating 1.8 V from 3.3 V supply
- 100-lead TQFP and LQFP packages
- Temperature range: −40°C to +105°C

APPLICATIONS

- Automotive audio processing
  - Head units
  - Navigation systems
  - Rear-seat entertainment systems
  - DSP amplifiers (sound system amplifiers)
- Commercial audio processing

FUNCTIONAL BLOCK DIAGRAM



*SPI/I²C = THE ADDR0, CLATCH, SCL/CCLK, SDA/COUT, AND ADDR1/CDATA PINS.
†THERE ARE 12 BIT CLOCKS (BCLK[11:0]) AND 12 FRAME CLOCKS (LRCLK[11:0]) IN TOTAL. OF THE 12 CLOCKS, SIX ARE ASSIGNABLE, THREE MUST BE OUTPUTS, AND THREE MUST BE INPUTS.

Figure 1.

Rev. D
Document Feedback

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GENERAL DESCRIPTION

The ADAU1442/ADAU1445/ADAU1446 are enhanced audio processors that allow full flexibility in routing all input and output signals. The SigmaDSP® core features full 28-bit processing (56-bit in double-precision mode), synchronous parameter loading for ensuring filter stability, and 100% code efficiency with the SigmaStudio™ tools. This DSP allows system designers to compensate for the real-world limitations of speakers, amplifiers, and listening environments, resulting in a dramatic improvement of the perceived audio quality through speaker equalization, multiband compression, limiting, and third-party branded algorithms.

The flexible audio routing matrix (FARM) allows the user to multiplex inputs from multiple sources running at various sample rates to or from the SigmaDSP core. This drastically reduces the complexity of signal routing and clocking issues in the audio system. FARM includes up to eight stereo asynchronous sample rate converters (depending on the device model), Sony/Philips Digital Interconnect Format (S/PDIF) input and output, and serial (I^2S) and time division multiplexing (TDM) I/Os. Any of these inputs can be routed to the SigmaDSP core or to any of the asynchronous sample rate converters (ASRCs). Similarly, any one of the output signals can be taken from the SigmaDSP core or from any of the ASRC outputs. This routing scheme, which can be modified at any time via control registers, allows for maximum system flexibility.

The ADAU1442, ADAU1445, and ADAU1446 differ only in ASRC functionality and packaging. The ADAU1442/ADAU1445 contain 16 channels of ASRCs and are packaged in TQFP packages, whereas the ADAU1446 contains no ASRCs and is packaged in an LQFP. The ADAU1442 can handle nine clock domains, the ADAU1445 can handle three clock domains, and the ADAU1446 can handle one clock domain.

The ADAU1442/ADAU1445/ADAU1446 can be controlled in one of two operational modes: the settings of the chip can be loaded and dynamically updated through the SPI/I^2C® port, or the DSP can self-boot from an external EEPROM in a system with no microcontroller. There is also a bank of multipurpose (MP) pins that can be used as general-purpose digital I/Os or as inputs to the 4-channel auxiliary control ADC.

The ADAU1442/ADAU1445/ADAU1446 are supported by the SigmaStudio graphical development environment. This software includes audio processing blocks such as FIR and IIR filters, dynamics processors, mixers, low level DSP functions, and third-party algorithms for fast development of custom signal flows.

Table 1.

Device	ASRC Channels	ASRC Clock Domains	Package
ADAU1442	16	8	TQFP
ADAU1445	16	2	TQFP
ADAU1446	0	N/A	LQFP

SPECIFICATIONS

AVDD = 3.3 V, DVDD = 1.8 V, PVDD = 3.3 V, IOVDD = 3.3 V, T_A = 25°C, master clock input = 12.288 MHz, core clock f_{CORE} = 172.032 MHz, I/O pins set to 2 mA drive setting, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG PERFORMANCE					AVDD = 3.3 V ± 10%.
Auxiliary Analog Inputs					
Resolution		10		Bits	
Full-Scale Analog Input		AVDD		V	
Integral Nonlinearity (INL)	−2.3		+2.3	LSB	
Differential Nonlinearity (DNL)	−2.0		+2.0	LSB	
Gain Error	−2.0		+2.0	LSB	
Input Impedance		200		kΩ	
Sample Rate		f_{CORE}/896		kHz	4:1 multiplexed input, each channel at f_{CORE}/3584. For f_{CORE} = 172.032 MHz, each channel is sampled at 48 kHz.
POWER					
Supply Voltage					
Analog Voltage (AVDD)	2.97	3.3	3.63	V	
Digital Voltage (DVDD)	1.62	1.8	1.98	V	
PLL Voltage (PVDD)	2.97	3.3	3.63	V	
IOVDD Voltage (IOVDD)	2.97	3.3	3.63	V	
Supply Current					
Analog Current (AVDD)		2		mA	
PLL Current (PVDD)		10		mA	
I/O Current (IOVDD)		10		mA	Depends greatly on the number of active serial ports, clock pins, and characteristics of external loads.
Digital Current (DVDD)					
ADAU1442					
Typical Program		335		mA	Test program includes 16 channels I/O, 10-band EQ per channel, all ASRCs active.
Minimal Program		115		mA	Test program includes 2 channels I/O, 10-band EQ per channel.
ADAU1445					
Typical Program		270		mA	Test program includes 16 channels I/O, 10-band EQ per channel, all ASRCs active.
Minimal Program		115		mA	Test program includes 2 channels I/O, 10-band EQ per channel.
ADAU1446					
Typical Program		135		mA	Test program includes 16 channels I/O, 10-band EQ per channel, all ASRCs active.
Minimal Program		110			Test program includes 2 channels I/O, 10-band EQ per channel.
ASYNCHRONOUS SAMPLE RATE CONVERTERS[1]					
Dynamic Range		139		dB	A-weighted, 20 Hz to 20 kHz.
I/O Sample Rate	6		192	kHz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
I/O Sample Rate Ratio	1:8		7.75:1		
THD + N		−133	−120	dB	
CRYSTAL OSCILLATOR					
Transconductance		40		mS	
REGULATOR[2]					
DVDD Voltage	1.65	1.75	1.85	V	Maximum 500 mA load.

[1] To calculate the group delay, refer to the SRC Group Delay section.
[2] Regulator specifications are calculated using an NJT4030P transistor from On Semiconductor in the circuit.

AVDD = 3.3 V ± 10%, DVDD = 1.8 V ± 10%, PVDD = 3.3 V, IOVDD = 3.3 V ± 10%, T_A = −40°C to +105°C, master clock input = 12.288 MHz, core clock f_{CORE} = 172.032 MHz, I/O pins set to 2 mA drive setting, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG PERFORMANCE					AVDD = 3.3 V ± 10%.
Auxiliary Analog Inputs					
Resolution		10		Bits	
Full-Scale Analog Input		AVDD		V	
Integral Nonlinearity (INL)	−2.3		+2.3	LSB	
Differential Nonlinearity (DNL)	−2.0		+2.0	LSB	
Gain Error	−2.0		+2.0	LSB	
Input Impedance		200		kΩ	
Sample Rate		f_{CORE}/896		kHz	4:1 multiplexed input, each channel at f_{CORE}/3584. For f_{CORE} = 172.032 MHz, each channel is sampled at 48 kHz.
DIGITAL I/O					
Input Voltage, High (V_{IH})	0.7 × IOVDD			V	Digital input pins except SPDIFI.[1]
Input Voltage, Low (V_{IL})			0.3 × IOVDD	V	Digital input pins except SPDIFI.[1]
Input Leakage, High (I_{IH}) at 3.3 V	−2		+2	µA	Digital input pins except MCLK and SPDIFI.
	−2		+8	µA	MCLK.
	60		140	µA	SPDIFI.
Input Leakage, Low (I_{IL}) at 0 V	−85		−10	µA	All other pins.
	−2		+2	µA	CLKMODEx, RSVD, PLLx, RESET.
	−8		+2	µA	MCLK.
	−140		−60	µA	SPDIFI.
High Level Output Voltage (V_{OH})	0.85 × IOVDD			V	I_{OH} = 1 mA.
Low Level Output Voltage (V_{OL})			0.1 × IOVDD	V	I_{OL} = 1 mA.
Input Capacitance (C_I)		5		pF	Guaranteed by design.
Multipurpose Pins Output Drive		2		mA	These pins are not designed for static current draw and should not drive LEDs directly.
POWER					
Supply Voltage					
Analog Voltage (AVDD)	2.97	3.3	3.63	V	
Digital Voltage (DVDD)	1.62	1.8	1.98	V	
PLL Voltage (PVDD)	2.97	3.3	3.63	V	
IOVDD Voltage (IOVDD)	2.97	3.3	3.63	V	
Supply Current					
Analog Current (AVDD)		2		mA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PLL Current (PVDD)		10		mA	
I/O Current (IOVDD)		10		mA	Depends greatly on the number of active serial ports, clock pins, and characteristics of external loads.
Maximum Digital Current (DVDD)					
ADAU1442			460	mA	Test program includes 24 channels I/O, fully utilized program RAM.
ADAU1445			365	mA	Test program includes 24 channels I/O, fully utilized program RAM.
ADAU1446			315	mA	Test program includes 24 channels I/O, fully utilized program RAM.
Power Dissipation					
AVDD, DVDD, PVDD During Operation of ADAU1442			960	mW	All supplies at nominal +10%, IOVDD is not included in measurement.
AVDD, DVDD, PVDD During Operation of ADAU1445			780	mW	All supplies at nominal +10%, IOVDD is not included in measurement.
AVDD, DVDD, PVDD During Operation of ADAU1446			675	mW	All supplies at nominal +10%, IOVDD is not included in measurement.
Reset, All Supplies		94		mW	
ASYNCHRONOUS SAMPLE RATE CONVERTERS[2]					
Dynamic Range		139		dB	A-weighted, 20 Hz to 20 kHz.
I/O Sample Rate	6		192	kHz	
I/O Sample Rate Ratio	1:8		7.75:1		
THD + N		−133	−120	dB	
CRYSTAL OSCILLATOR					
Transconductance		40		mS	
REGULATOR[3]					
DVDD Voltage	1.65	1.75	1.85	V	Maximum 500 mA load.

[1] SPDIFI input voltage range exceeds the requirements of the S/PDIF specification.
[2] To calculate the group delay, refer to the SRC Group Delay section.
[3] Regulator specifications are calculated using an NJT4030P transistor from On Semiconductor in the circuit.

DIGITAL TIMING SPECIFICATIONS

T_A = −40°C to +105°C, DVDD = 1.8 V, IOVDD = 3.3 V.

Table 4.

Parameter[1]	Min	Max	Unit	Description
MASTER CLOCK				
f_{MP}	2.822	24.576	MHz	Master clock (MCLK) frequency. See the Master Clock and PLL section.
t_{MP}	40.69	354.36	ns	Master clock (MCLK) period. See the Master Clock and PLL section.
t_{MD}	25	75	%	Master clock (MCLK) duty cycle.
CLKOUT Jitter		250	ps	Cycle-to-cycle rms average.
CORE CLOCK				
f_{CORE}		172.032	MHz	DSP core clock frequency.
SERIAL PORT				
f_{BCLK}		24.576	MHz	BCLK frequency.
t_{BCLK}	40.69		ns	BCLK period.
t_{BIL}	30		ns	BCLKx low pulse width, slave mode.
t_{BIH}	30		ns	BCLKx high pulse width, slave mode.
t_{LIS}	20		ns	LRCLKx setup to BCLKx input rising edge, slave mode.
t_{LIH}	20		ns	LRCLKx hold from BCLKx input rising edge, slave mode.
t_{SIS}	10		ns	SDATA_INx setup to BCLKx input rising edge.
t_{SIH}	10		ns	SDATA_INx hold from BCLKx input rising edge.
t_{TS}		5	ns	BCLKx output falling edge to LRCLKx output timing skew.
t_{SODS}		30	ns	SDATA_OUTx delay in slave mode from BCLKx output falling edge.
t_{SODM}		30	ns	SDATA_OUTx delay in master mode from BCLKx output falling edge.
SPI PORT				
$f_{CCLK\ write}$		32	MHz	CCLK frequency.[2]
$f_{CCLK\ read}$		16	MHz	CCLK frequency.[2]
t_{CCPL}	20		ns	CCLK pulse width low.
t_{CCPH}	20		ns	CCLK pulse width high.
t_{CLS}	0		ns	CLATCH setup to CCLK rising edge.
t_{CLH}	35		ns	CLATCH hold from CCLK rising edge.
t_{CLPH}	20		ns	CLATCH pulse width high.
t_{CLDLY}	20		ns	Minimum delay between CLATCH low pulses.
t_{CDS}	0		ns	CDATA setup to CCLK rising edge.
t_{CDH}	35		ns	CDATA hold from CCLK rising edge.
t_{COV}		40	ns	COUT valid output delay from CCLK falling edge.
I²C PORT				
f_{SCL}		400	kHz	SCL clock frequency.
t_{SCLH}	0.6		µs	SCL pulse width high.
t_{SCLL}	1.3		µs	SCL pulse width low.
t_{SCS}	0.6		µs	Start and repeated start condition setup time.
t_{SCH}	0.6		µs	Start condition hold time.
t_{DS}	100		ns	Data setup time.
t_{DH}	0.9		µs	Data hold time.
t_{SCLR}		300	ns	SCL rise time.
t_{SCLF}		300	ns	SCL fall time.
t_{SDR}		300	ns	SDA rise time.
t_{SDF}		300	ns	SDA fall time.
t_{BFT}	1.3		µs	Bus-free time between stop and start.
MULTIPURPOSE PINS AND RESET				
f_{MP}		$f_S/2$	Hz	MPx maximum switching rate.
t_{MPIL}		$1.5 \times 1/f_{S,NORMAL}$	µs	MPx pin input latency until high/low value is read by core. Guaranteed by design.
t_{RLPW}	10		ns	$\overline{\text{RESET}}$ low pulse width.

[1] All timing specifications are given for the default (I²S) states of the serial audio input ports and the serial audio output ports (see Table 26 and Table 30).
[2] Maximum SPI CCLK clock frequency is dependent on current drive strength and capacitive loads on the circuit board.

Digital Timing Diagrams

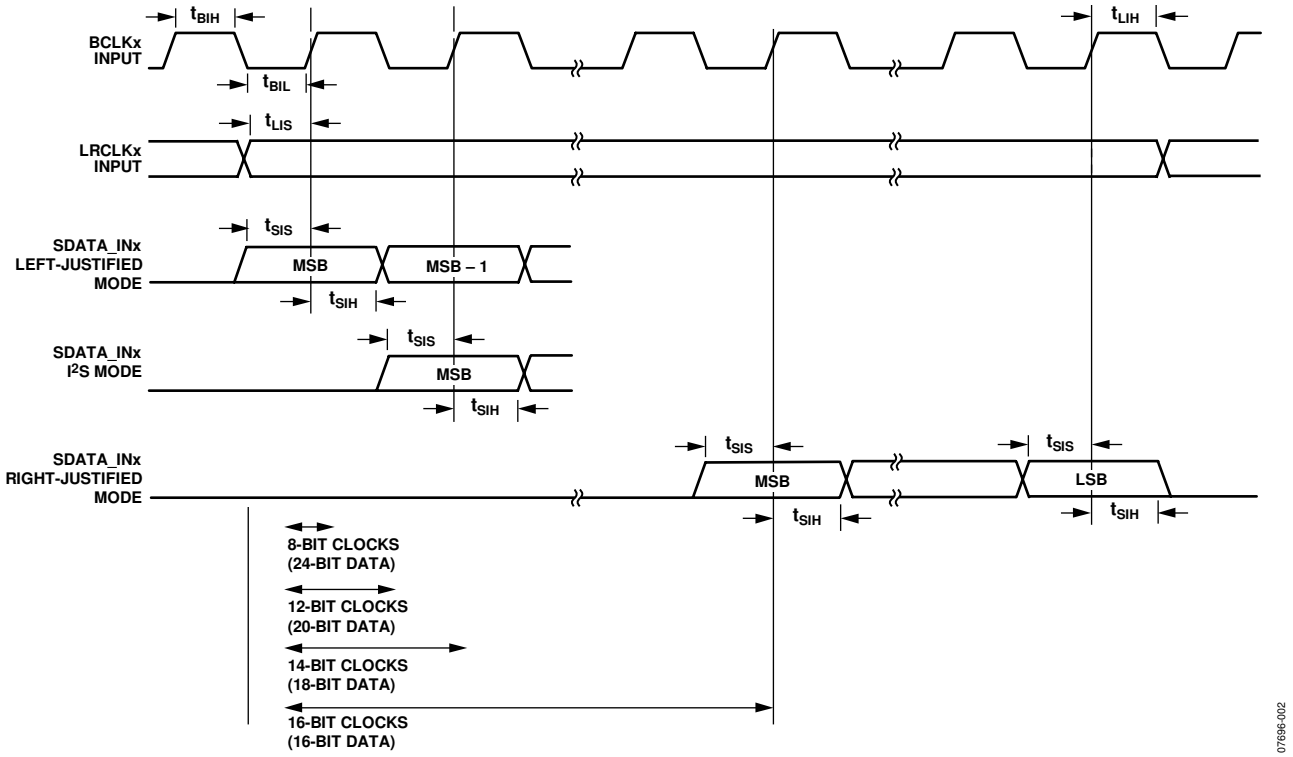


Figure 2. Serial Input Port Timing

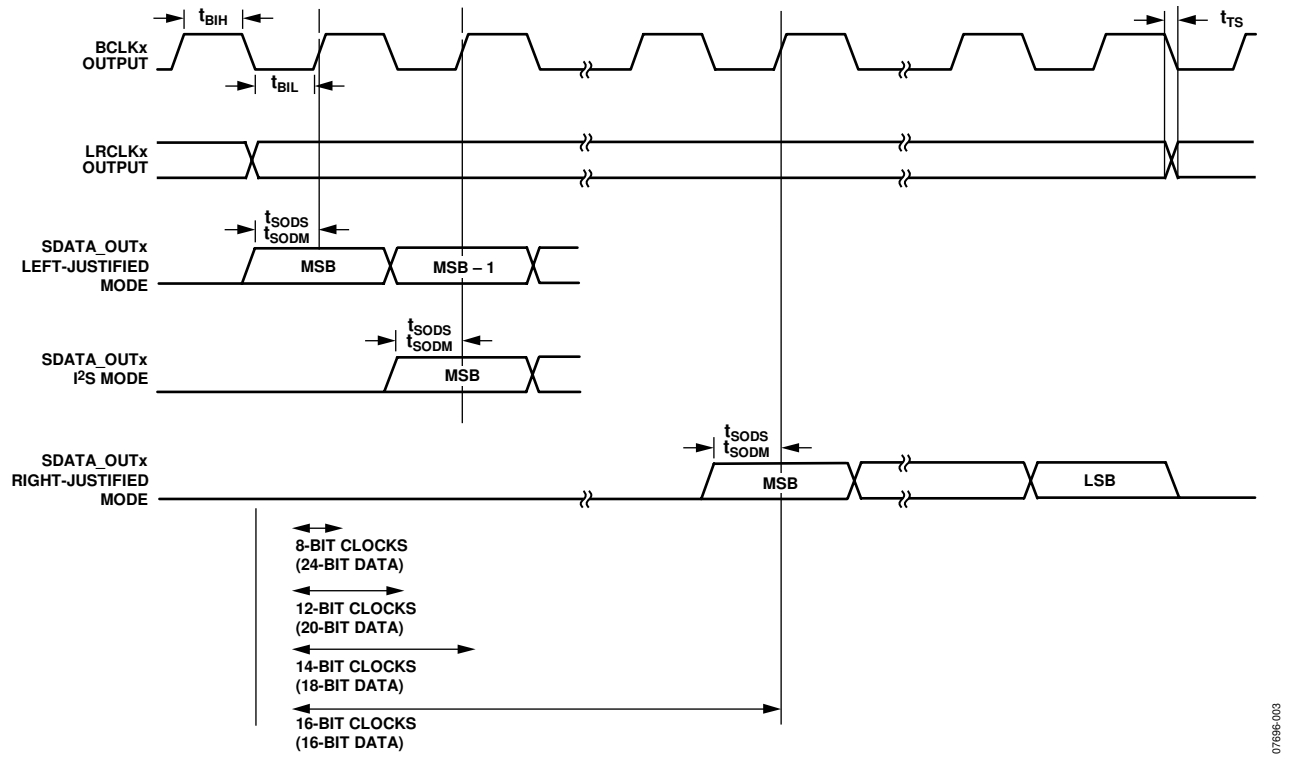


Figure 3. Serial Output Port Timing

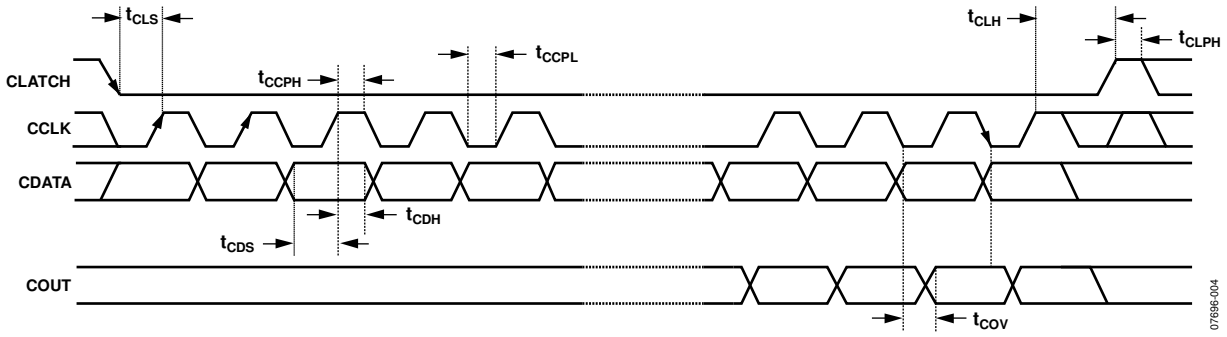


Figure 4. SPI Port Timing

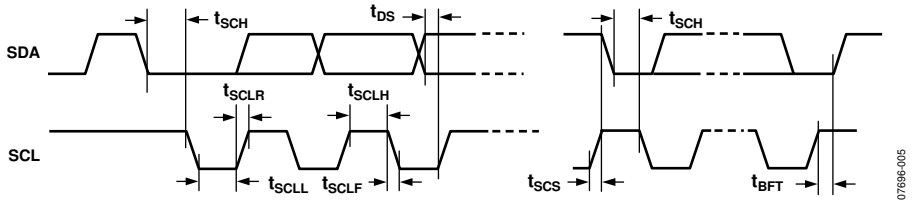


Figure 5. I²C Port Timing

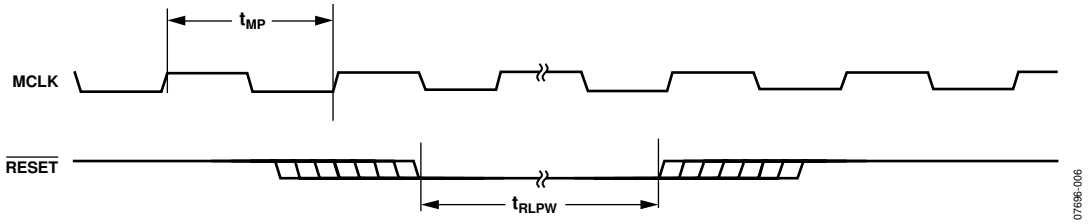


Figure 6. Master Clock and Reset Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
DVDD to Ground	0 V to 2.2 V
AVDD to Ground	0 V to 4.0 V
IOVDD to Ground	0 V to 4.0 V
Digital Inputs	DGND – 0.3 V to IOVDD + 0.3 V
Maximum Ambient Temperature	−40°C to +105°C
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Soldering (10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

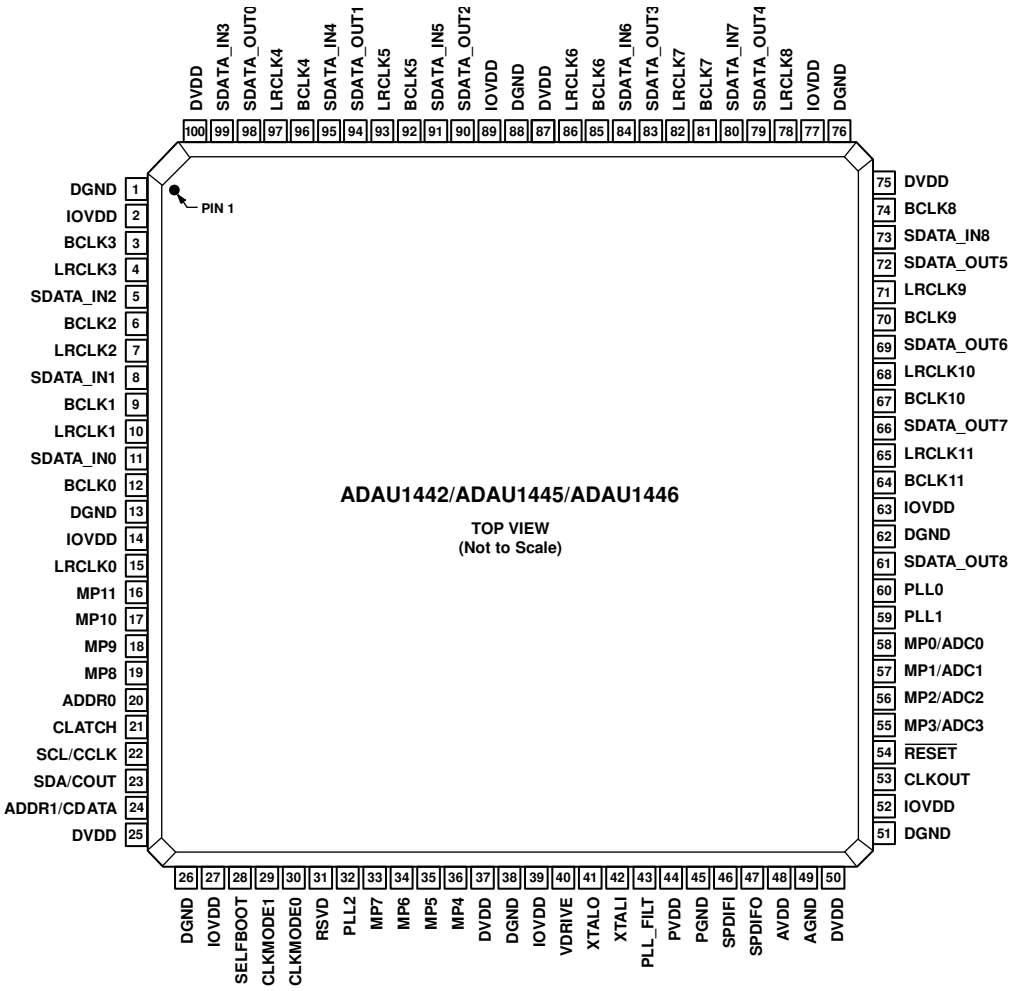
Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
100-Lead TQFP	26.3	9.4	°C/W
100-Lead LQFP	41.4	9.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD DOES NOT HAVE AN INTERNAL ELECTRICAL CONNECTION TO THE INTEGRATED CIRCUIT, BUT SHOULD BE CONNECTED TO THE GROUND PLANE OF THE PCB FOR PROPER HEAT DISSIPATION.

Figure 7. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 13, 26, 38, 51, 62, 76, 88	DGND	PWR	Digital Ground. The AGND, DGND, and PGND pins should be tied directly together in a common ground plane. DGND pins should be decoupled to a DVDD pin with a 100 nF capacitor.
2, 14, 27, 39, 52, 63, 77, 89	IOVDD	PWR	Input and Output Supply. The voltage on this pin sets the highest input voltage that should be present on the digital input pins. This pin is also the supply for the digital output signals on the clock, data, control port, and MP pins. IOVDD should always be set to 3.3 V. The current draw of this pin is variable because it is dependent on the loads of the digital outputs.
3	BCLK3	D_IO	Bit Clock, Input/Output Clock Domain 3. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 3 is set up as a master or slave. When not used, this pin can be left disconnected.
4	LRCLK3	D_IO	Frame Clock, Input/Output Clock Domain 3. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 3 is set up as a master or slave. When not used, this pin can be left disconnected.
5	SDATA_IN2	D_IN	Serial Data Port 2 Input. When not used, this pin can be left disconnected.

Pin No.	Mnemonic	Type[1]	Description
6	BCLK2	D_IO	Bit Clock, Input Clock Domain 2. This pin is bidirectional, with the direction depending on whether the Input Clock Domain 2 is set up as a master or slave. When not used, this pin can be left disconnected.
7	LRCLK2	D_IO	Frame Clock, Input Clock Domain 2. This pin is bidirectional, with the direction depending on whether the Input Clock Domain 2 is set up as a master or slave. When not used, this pin can be left disconnected.
8	SDATA_IN1	D_IN	Serial Data Port 1 Input. When not used, this pin can be left disconnected.
9	BCLK1	D_IO	Bit Clock, Input Clock Domain 1. This pin is bidirectional, with the direction depending on whether the Input Clock Domain 1 is set up as a master or slave. When not used, this pin can be left disconnected.
10	LRCLK1	D_IO	Frame Clock, Input Clock Domain 1. This pin is bidirectional, with the direction depending on whether the Input Clock Domain 1 is set up as a master or slave. When not used, this pin can be left disconnected.
11	SDATA_IN0	D_IN	Serial Data Port 0 Input. When not used, this pin can be left disconnected.
12	BCLK0	D_IO	Bit Clock, Input Clock Domain 0. This pin is bidirectional, with the direction depending on whether the Input Clock Domain 0 is set up as a master or slave. When not used, this pin can be left disconnected.
15	LRCLK0	D_IO	Frame Clock, Input Clock Domain 0. This pin is bidirectional, with the direction depending on whether the Input Clock Domain 0 is set up as a master or slave. When not used, this pin can be left disconnected.
16	MP11	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
17	MP10	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
18	MP9	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
19	MP8	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
20	ADDR0	D_IN	Address 0 for I²C and SPI. In I²C mode, this pin, in combination with ADDR1, allows up to four ADAU1442/ADAU1445/ADAU1446 devices to be used on the same I²C bus. In SPI mode, setting ADDR0 either low or high allows up to two ICs to be used with a common SPI latch signal.
21	CLATCH	D_IN	SPI Latch Signal. Must go low at the beginning of an SPI transaction and high at the end of a transaction. Each SPI transaction may take a different number of CCLK cycles to complete, depending on the address and read/write bits that are sent at the beginning of the SPI transaction. When not used, this pin should be tied to ground, preferably with a 10 kΩ pull-down resistor.
22	SCL/CCLK	D_IN	Serial Clock/Continuous Clock. In I²C mode, this pin functions as SCL and is always an open collector input, except when in self-boot mode, where it is an open collector output (I²C master). The line connected to this pin should have a 2.0 kΩ pull-up resistor. In SPI mode, this pin functions as CCLK and is an input pin that can be either run continuously or gated off between SPI transactions.
23	SDA/COUT	D_IO	Serial Data/Continuous Output. In I²C mode, this pin functions as SDA and is a bidirectional open collector. The line connected to the SDA pin should have a 2.0 kΩ pull-up resistor. In SPI mode, this pin functions as COUT and is used for reading back registers and memory locations. The COUT pin is three-stated when an SPI read is not active.
24	ADDR1/CDATA	D_IN	Address 1/Continuous Data. In I²C mode, this pin functions as ADDR1 and, in combination with ADDR0, sets the I²C address of the IC. This allows up to four ADAU1442/ADAU1445/ADAU1446 devices to be used on the same I²C bus. In SPI mode, this pin functions as CDATA and is the SPI data input.
25, 37, 50, 75, 87, 100	DVDD	PWR	1.8 V Digital Supply. This can be supplied externally or generated from a 3.3 V supply with the on-board 1.8 V regulator. Each DVDD pin should be decoupled to DGND with a 100 nF capacitor.
28	SELFBOOT	D_IN	Self-Boot Select. Allows the ADAU1442/ADAU1445/ADAU1446 to be controlled by the control port or to perform a self-boot. Setting this pin high (that is, to 1) initiates a self-boot operation when the ADAU1442/ADAU1445/ADAU1446 are brought out of a reset. This pin can be tied directly to a voltage source or ground or pulled up/down with a resistor.
29	CLKMODE1	D_IN	Output Clock Mode 1. With CLKMODE0, this pin sets the frequency of the CLKOUT signal.
30	CLKMODE0	D_IN	Output Clock Mode 0. With CLKMODE1, this pin sets the frequency of the CLKOUT signal.
31	RSVD	D_IN	Reserved. Tie this pin to ground, preferably with a 10 kΩ pull-down resistor.
32	PLL2	D_IN	PLL Mode Select Pin 2.
33	MP7	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.

Pin No.	Mnemonic	Type[1]	Description
34	MP6	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
35	MP5	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
36	MP4	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
40	VDRIVE	A_OUT	Regulator Drive. Supplies the drive current for the 1.8 V regulator. The base of the voltage regulator's external PNP transistor is driven from VDRIVE.
41	XTALO	A_OUT	Crystal Oscillator Output. A 100 Ω damping resistor should be connected between this pin and the crystal. This output should not be used to directly drive a clock to another IC; the CLKOUT pin exists for this purpose. If the crystal oscillator is not used, the XTALO pin can be left unconnected.
42	XTALI	A_IN	Crystal Oscillator Input. This pin provides the master clock for the ADAU1442/ADAU1445/ADAU1446. If the ADAU1442/ADAU1445/ADAU1446 generate the master clock in the system, this pin should be connected to the crystal oscillator circuit. If the ADAU1442/ADAU1445/ADAU1446 are slaves to an external master clock, this pin should be connected to the master clock signal generated by another IC.
43	PLL_FILT	A_OUT	Phase-Locked Loop Filter. Two capacitors and a resistor must be connected to this pin as shown in Figure 11.
44	PVDD	PWR	Phase-Locked Loop Supply. Provides the 3.3 V power supply for the PLL. This should be decoupled to PGND with a100 nF capacitor.
45	PGND	PWR	Phase-Locked Loop Ground. Ground for the PLL supply. The AGND, DGND, and PGND pins can be tied directly together in a common ground plane. PGND should be decoupled to PVDD with a 100 nF capacitor.
46	SPDIFI	D_IN	S/PDIF Input. Accepts digital audio data in the S/PDIF format. When not used, this pin can be left disconnected.
47	SPDIFO	D_OUT	S/PDIF Output. Outputs digital audio data in the S/PDIF format. When not used, this pin can be left disconnected.
48	AVDD	PWR	Analog Supply. 3.3 V analog supply for the auxiliary ADC. This pin should be decoupled to AGND with a 100 nF capacitor.
49	AGND	PWR	Analog Ground. Ground for the analog supply. This pin should be decoupled to AVDD with a 100 nF capacitor.
53	CLKOUT	D_OUT	Master Clock Output. Used to output a master clock to other ICs in the system. Set using the CLKMODEx pins. When not used, this pin can be left disconnected.
54	$\overline{\text{RESET}}$	D_IN	Reset. Active-low reset input. Reset is triggered on a high-to-low edge and exited on a low-to-high edge. For detailed information about initialization, see the Power-Up Sequence section. A reset event sets all RAMs and registers to their default values.
55	MP3/ADC3	D_IO, A_IN	Multipurpose, General-Purpose Input or Output/Auxiliary ADC Input 3. When not used, this pin can be left disconnected.
56	MP2/ADC2	D_IO, A_IN	Multipurpose, General-Purpose Input or Output/Auxiliary ADC Input 2. When not used, this pin can be left disconnected.
57	MP1/ADC1	D_IO, A_IN	Multipurpose, General-Purpose Input or Output/Auxiliary ADC Input 1. When not used, this pin can be left disconnected.
58	MP0/ADC0	D_IO, A_IN	Multipurpose, General-Purpose IO/Auxiliary ADC Input 0. When not used, this pin can be left disconnected.
59	PLL1	D_IN	Phase-Locked Loop Mode Select Pin 1.
60	PLL0	D_IN	Phase-Locked Loop Mode Select Pin 0.
61	SDATA_OUT8	D_OUT	Serial Data Port 0 Output. When not used, this pin can be left disconnected.
64	BCLK11	D_IO	Bit Clock, Output Clock Domain 11. This pin is bidirectional, with the direction depending on whether the Output Clock Domain 11 is set up as a master or slave. When not used, this pin can be left disconnected.
65	LRCLK11	D_IO	Frame Clock, Output Clock Domain 11. This pin is bidirectional, with the direction depending on whether the Output Clock Domain 11 is set up as a master or slave. When not used, this pin can be left disconnected.

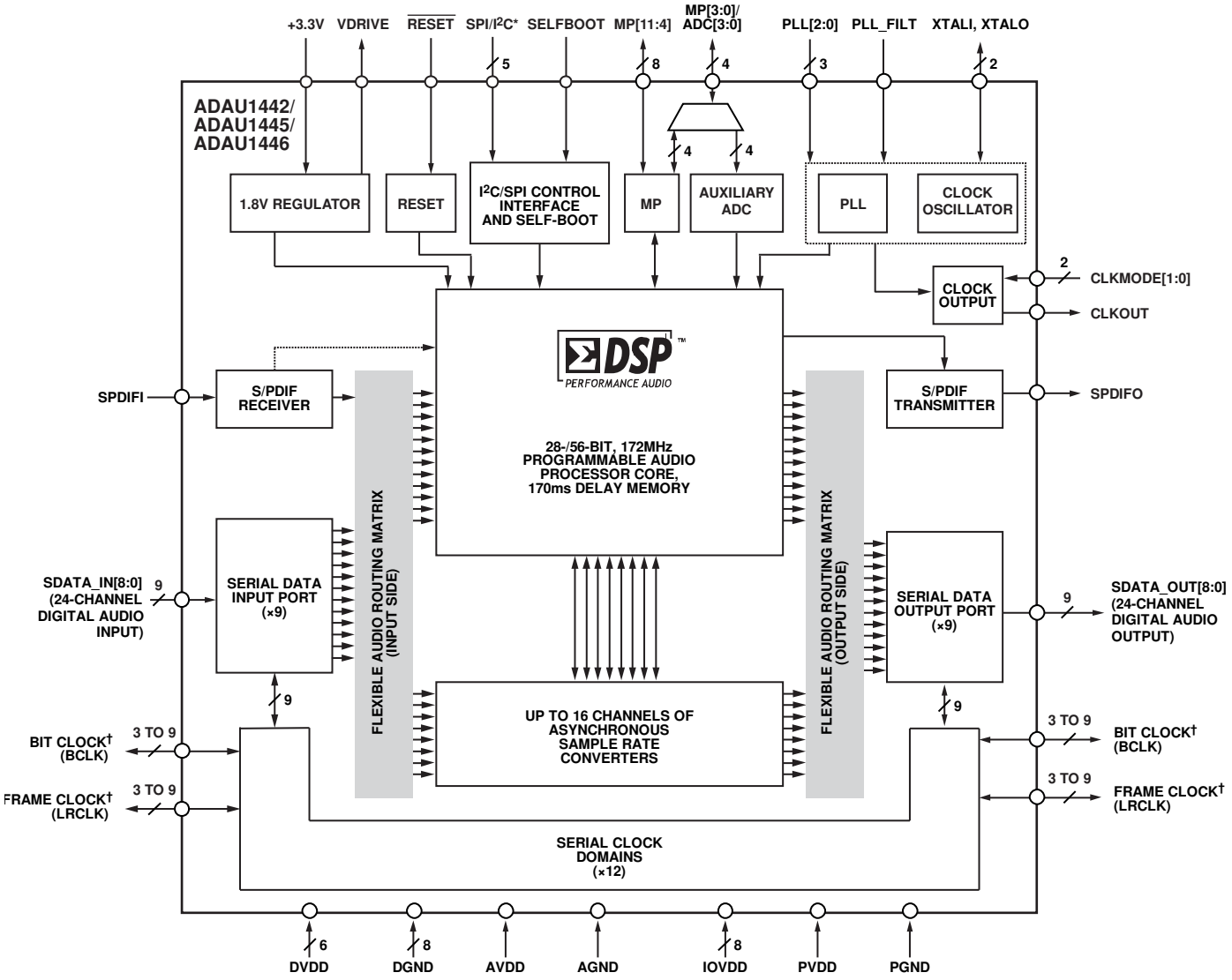
Pin No.	Mnemonic	Type[1]	Description
66	SDATA_OUT7	D_OUT	Serial Data Port 7 Output. When not used, this pin can be left disconnected.
67	BCLK10	D_IO	Bit Clock, Output Clock Domain 10. This pin is bidirectional, with the direction depending on whether the Output Clock Domain 10 is set up as a master or slave. When not used, this pin can be left disconnected.
68	LRCLK10	D_IO	Frame Clock, Output Clock Domain 10. This pin is bidirectional, with the direction depending on whether the Output Clock Domain 10 is set up as a master or slave. When not used, this pin can be left disconnected.
69	SDATA_OUT6	D_OUT	Serial Data Port 6 Output. When not used, this pin can be left disconnected.
70	BCLK9	D_IO	Bit Clock, Output Clock Domain 9. This pin is bidirectional, with the direction depending on whether the Output Clock Domain 9 is set up as a master or slave. When not used, this pin can be left disconnected.
71	LRCLK9	D_IO	Frame Clock, Output Clock Domain 9. This pin is bidirectional, with the direction depending on whether the Output Clock Domain 9 is set up as a master or slave. When not used, this pin can be left disconnected.
72	SDATA_OUT5	D_OUT	Serial Data Port 5 Output. When not used, this pin can be left disconnected.
73	SDATA_IN8	D_IN	Serial Data Port 8 Input. When not used, this pin can be left disconnected.
74	BCLK8	D_IO	Bit Clock, Input/Output Clock Domain 8. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 8 is set up as a master or slave. When not used, this pin can be left disconnected.
78	LRCLK8	D_IO	Frame Clock, Input/Output Clock Domain 8. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 8 is set up as a master or slave. When not used, this pin can be left disconnected.
79	SDATA_OUT4	D_OUT	Serial Data Port 4 Output. When not used, this pin can be left disconnected.
80	SDATA_IN7	D_IN	Serial Data Port 7 Input. When not used, this pin can be left disconnected.
81	BCLK7	D_IO	Bit Clock, Input/Output Clock Domain 7. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 7 is set up as a master or slave. When not used, this pin can be left disconnected.
82	LRCLK7	D_IO	Frame Clock, Input/Output Clock Domain 7. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 7 is set up as a master or slave. When not used, this pin can be left disconnected.
83	SDATA_OUT3	D_OUT	Serial Data Port 3 Output. When not used, this pin can be left disconnected.
84	SDATA_IN6	D_IN	Serial Data Port 6 Input. When not used, this pin can be left disconnected.
85	BCLK6	D_IO	Bit Clock, Input/Output Clock Domain 6. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 6 is set up as a master or slave. When not used, this pin can be left disconnected.
86	LRCLK6	D_IO	Frame Clock, Input/Output Clock Domain 6. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 6 is set up as a master or slave. When not used, this pin can be left disconnected.
90	SDATA_OUT2	D_OUT	Serial Data Port 2 Output. When not used, this pin can be left disconnected.
91	SDATA_IN5	D_IN	Serial Data Port 5 Input. When not used, this pin can be left disconnected.
92	BCLK5	D_IO	Bit Clock, Input/Output Clock Domain 5. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 5 is set up as a master or slave. When not used, this pin can be left disconnected.
93	LRCLK5	D_IO	Frame Clock, Input/Output Clock Domain 5. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 5 is set up as a master or slave. When not used, this pin can be left disconnected.
94	SDATA_OUT1	D_OUT	Serial Data Port 1 Output. When not used, this pin can be left disconnected.
95	SDATA_IN4	D_IN	Serial Data Port 4 Input. When not used, this pin can be left disconnected.

Pin No.	Mnemonic	Type[1]	Description
96	BCLK4	D_IO	Bit Clock, Input/Output Clock Domain 4. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 4 is set up as a master or slave. When not used, this pin can be left disconnected.
97	LRCLK4	D_IO	Frame Clock, Input/Output Clock Domain 4. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 4 is set up as a master or slave. When not used, this pin can be left disconnected.
98	SDATA_OUT0	D_OUT	Serial Data Port 0 Output. When not used, this pin can be left disconnected.
99	SDATA_IN3	D_IN	Serial Data Port 3 Output. When not used, this pin can be left disconnected.

[1] PWR = power/ground, A_IN = analog input, D_IN = digital input, A_OUT = analog output, D_OUT = digital output, D_IO = digital input/output.

THEORY OF OPERATION

SYSTEM BLOCK DIAGRAM



*SPI/I2C = THE ADDR0, CLATCH, SCL/CCLK, SDA/COUT, AND ADDR1/CDATA PINS.
†THERE ARE 12 BIT CLOCKS (BCLK[11:0]) AND 12 FRAME CLOCKS (LRCLK[11:0]) IN TOTAL. OF THE 12 CLOCKS, SIX ARE ASSIGNABLE, THREE MUST BE OUTPUTS, AND THREE MUST BE INPUTS.

Figure 8. System Block Diagram

OVERVIEW

The ADAU1442/ADAU1445/ADAU1446 are each a 24-channel audio DSP with an integrated S/PDIF receiver and transmitter, flexible serial audio ports, up to 16 channels of asynchronous sample rate converters (ASRCs), flexible audio routing, and user interface capabilities. Signal processing capabilities include equalization, crossover, bass enhancement, multiband dynamics processing, delay compensation, speaker compensation, and stereo image widening. These algorithms can be used to compensate for the real-world limitations of speakers, amplifiers, and listening environments, resulting in an improvement in the perceived audio quality.

An on-board oscillator can be connected to an external crystal to generate the master clock. A phase-locked loop (PLL) allows the ADAU1442/ADAU1445/ADAU1446 to be clocked from a variety of clock frequencies. The PLL can accept inputs of 64 × f_S, 128 × f_S, 256 × f_S, 384 × f_S, or 512 × f_S to generate the internal master clock of the core, where f_S is the sampling rate of audio in normal-rate processing mode. In dual- or quad-rate mode, these multipliers are halved or quartered, respectively. System sample rates include, but are not limited to, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, and 192 kHz.

Each ADAU1442/ADAU1445/ADAU1446 operates from a 1.8 V digital power supply and a 3.3 V analog supply. An on-board voltage regulator can be used to operate the chip from a single 3.3 V supply.

The ADAU1442/ADAU1445/ADAU1446 have a sophisticated control port that supports complete read and write capability of all memory locations, excluding read-only addresses. Control registers are provided to offer complete control of the chip's configuration and serial modes. Handshaking is included for ease of memory uploads and downloads. The ADAU1442/ADAU1445/ADAU1446 can be configured for either SPI or I²C control. Program RAM, parameter RAM, and register contents can be saved in an external EEPROM, from which the ADAU1442/ADAU1445/ADAU1446 can self-boot on startup.

The ADAU1442/ADAU1445/ADAU1446 serial ports operate with digital audio I/Os in the I²S, left-justified, right-justified, or TDM-compatible mode. The flexible serial data ports allow for direct interconnection to a variety of ADCs, DACs, and general-purpose DSPs. The combination of an on-board S/PDIF transmitter and receiver and 16 channels of ASRCs allows for easy compatibility with an extensive number of external devices, and a system with up to nine sampling rates.

The flexible audio routing matrix (FARM) is a system of multiplexers used to distribute the audio signals in the ADAU1442/ADAU1445/ADAU1446 among the serial inputs and outputs, audio core, and ASRCs. FARM can easily be configured by setting the appropriate registers.

The ADAU1442, ADAU1445, and ADAU1446 are distinguished by the number of on-board ASRCs and maximum sample rates. The ADAU1442 contains eight 2-channel ASRCs, the ADAU1445 contains two 8-channel ASRCs, and the ADAU1446 has no ASRCs.

Two sets of serial ports at the input and output can operate in a special flexible TDM mode, which allows the user to independently assign byte-specific locations to audio streams at varying bit depths. This mode ensures compatibility with codecs using similar flexible TDM streams.

The core of the ADAU1442/ADAU1445/ADAU1446 is a 28-bit DSP (or a 56-bit DSP when using double-precision mode) optimized for audio processing, and it can process audio at sample rates of up to 192 kHz. The program and parameter RAMs can be loaded with a custom audio processing signal flow built with the SigmaStudio graphical programming software from Analog Devices, Inc. The values stored in the parameter RAM control individual signal processing blocks, such as IIR and FIR equalization filters, dynamics processors, audio delays, and mixer levels. A software safeload feature allows for transparent parameter updates and prevents clicks on the output signals.

Reliability features such as a CRC and program counter watchdog help ensure that the system can detect and recover from any errors related to memory corruption.

S/PDIF signals can be routed through an ASRC for processing in the DSP or can be sent directly to output on MP pins for recovery of the embedded audio signal. Other components of the embedded signal, including status and user bits, are not lost and can be output on the MP pins as well.

Multipurpose (MP) pins are available for providing a simple user interface without the need for an external microcontroller. Twelve pins are available to input external control signals and output flags or controls to other devices in the system. Four of these can alternatively be assigned to an auxiliary ADC for use with analog controls such as potentiometers or system voltages. As inputs, MP pins can be connected to push buttons, switches, rotary encoders, potentiometers, or other external control circuitry to control the internal signal processing program. When configured as outputs, these pins can be used to drive LEDs (with a buffer), to output flags to a microcontroller, to control other ICs, or to connect to other external circuitry in an application.

The SigmaStudio software is used to program and control the ADAU1442/ADAU1445/ADAU1446 through the control port. Along with designing and tuning a signal flow, the software can configure all of the DSP registers in real time and download a new program and parameter into the external self-boot EEPROM. SigmaStudio's easy-to-use graphical interface allows anyone with audio processing knowledge to easily design a DSP signal flow and port it to a target application without the need for writing line-level code. At the same time, the software provides enough flexibility and programmability for an experienced DSP programmer to have in-depth control of the design. In SigmaStudio, the user can add signal processing cells from the library by dragging and dropping cells, connect them together in a flow, compile the design, and load the program and parameter files into the ADAU1442/ADAU1445/ADAU1446 memory through the control port. The complicated tasks of linking, compiling, and downloading the project are all handled automatically by the software.

Signal processing algorithms available in the provided libraries include

- Single- and double-precision biquad filter
- Mono and multichannel dynamics processors with peak or rms detection
- Mixer and splitter
- Tone and noise generator
- Fixed and variable gain
- Loudness
- Delay
- Stereo enhancement
- Dynamic bass boost
- Noise and tone source
- Level detector
- MP pin control and conditioning

New processing algorithms are always being developed. Analog Devices also provides proprietary and third-party algorithms for applications such as matrix decoding, bass enhancement, and surround virtualizers. Contact Analog Devices for information about licensing these algorithms.

Several power-saving mechanisms have been designed into the ADAU1442/ADAU1445/ADAU1446, including programmable pad strength for digital I/O pins and the ability to block the master clock from reaching unused subsystems.

The ADAU1442/ADAU1445/ADAU1446 are fabricated on a single monolithic integrated circuit for operation over the −40°C to +105°C temperature range. The ADAU1442 and ADAU1445 are housed in a 100-lead TQFP package, with an exposed pad to assist in heat dissipation, and the ADAU1446, due to its lower power consumption, is housed in a 100-lead LQFP package.

INITIALIZATION

Power-Up Sequence

The ADAU1442/ADAU1445/ADAU1446 have a built-in initialization period, which allows sufficient time for the PLL to lock and the registers to initialize their values. On a positive edge of $\overline{\text{RESET}}$, the PLL settings are immediately set by the PLL0, PLL1, and PLL2 pins, and the master clock signal is blocked from the chip subsystems. The initialization time, which is measured from the rising edge of $\overline{\text{RESET}}$, is dependent on the frequency of the signal input to the XTALI pin, or f_{XTALI}. The total initialization time is

$$1/(f_{XTALI}/D) \times 2^{15} \text{ sec}$$

where D is the PLL divider, as set by the PLL0, PLL1, and PLL2 pins. The PLL divider settings are described in Table 9.

For example, if the signal input to XTALI has a frequency of 12.288 MHz and the PLL divider is set to 4 (PLL = 0, PLL1 = 1, and PLL2 = 0), the initialization time lasts

$$1/(12288000/4) \times 2^{15} \text{ sec} = 0.010667 \text{ sec (or 10.667 ms)}$$

New values should not be written via the control port until the initialization is complete.

Table 8 shows some typical times to boot the ADAU1442/ADAU1445/ADAU1446 into the operational state necessary for an application, assuming that a 400 kHz I²C clock or a 5 MHz SPI clock is used and a full program, parameter set, and all registers (9 kB) are loaded. In reality, most applications use less than this full amount, and unused program and parameter RAM need not be initialized; therefore, the total boot time may be shorter.

Recommended Program/Parameter Loading Procedure

When writing large amounts of data to the program or parameter RAM in direct write mode, such as when downloading the initial contents of the RAMs from an external memory, the processor core should be disabled to prevent unpleasant noises from appearing at the audio output. When small amounts of data are transmitted during real-time operation of the DSP, such as when updating individual parameters, the software safeload mechanism can be used. More information is available in the Software Safeload section.

Power-Reduction Modes

Sections of the ADAU1442/ADAU1445/ADAU1446 chips can be turned on and off as needed to reduce power consumption. These include the ASRCs, S/PDIF receiver and transmitter, auxiliary ADCs, and DSP core. More information is available in the Master Clock and PLL Modes and Settings section.

System Initialization Sequence

Before the IC can process audio in the DSP, the following initialization sequence must be completed. (Step 5 through Step 11 can be performed in any order, as needed.)

1. Power on the IC and bring it out of reset. The order of the power supplies (DVDD, IOVDD, and AVDD) does not matter.
2. Wait at least 10.667 ms for the initialization to complete if the XTALI input is 12.288 MHz and the PLL divider is set to 4 (see the Power-Up Sequence section for information about calculating the initialization time if another f_{XTALI} is used).
3. Enable the master clocks of all modules to be used (see the Master Clock and PLL Modes and Settings section).
4. Set the DSP core rate select register (0xE220) to 0x001C. This disables the start pulse to the core.
5. Deassert the core run bit (see the DSP Core Modes and Settings section).
6. Set the serial input modes (see the Serial Input Port Modes Registers (Address 0xE000 to Address 0xE008) section).
7. Set the serial output modes (see the Serial Output Port Modes Registers (Address 0xE040 to Address 0xE049) section).
8. Set the routing matrix modes (see details of Address 0xE080 to Address 0xE09B in the Flexible Audio Routing Matrix Modes section).
9. Write the parameter RAM (Address 0x0000 to Address 0x0FFF).
10. Write the program RAM (Address 0x2000 to Address 0x2FFF).
11. Write the nonmodulo data RAM (Addresses vary based on the SigmaStudio project file).
12. Write all other necessary control registers, such as ASRCs and S/PDIF (Address 0xE221 to Address 0xE24C).
13. Set the DSP core rate select register (0xE220) to the desired value. This enables the start pulse to the core. Table 12 contains a list of valid settings.
14. Assert the core run bit (see the DSP Core Modes and Settings section).

Table 8. Power-Up Time

PLL Lock Time (ms) (f_{XTALI} = 12.288 MHz, PLL Divider = 4)	Approximate Boot Time; Loading Maximum Program/Parameter/Registers (ms)			
	I²C (at 400 kHz SCL)	SPI (at 5 MHz CCLK)	SPI (at 25 MHz CCLK)	Total (ms)
10.667	25	2	0.4	11.067 to 35.667

MASTER CLOCK AND PLL

Using the Oscillator

The ADAU1442/ADAU1445/ADAU1446 can use an on-board oscillator to generate its master clock. However, an external crystal must be attached to complete the oscillator circuit. The on-board oscillator is designed to work with a 256 × $f_{S,NORMAL}$ master clock, which is 12.288 MHz when $f_{S,NORMAL}$ is 48 kHz and 11.2896 MHz when $f_{S,NORMAL}$ is 44.1 kHz. The resonant frequency of this crystal should be in this range even when the core is processing dual- or quad-rate signals. When the core is processing dual-rate signals (for example, $f_{S,DUAL}$ = 88.2 kHz or 96 kHz), resonant frequency of the crystal should be 128 × $f_{S,DUAL}$. When the core is processing quad-rate signals (for example, $f_{S,QUAD}$ = 192 kHz), the resonant frequency of the crystal should be 64 × $f_{S,QUAD}$.

The external crystal in the circuit should be an AT-cut parallel resonance device operating at its fundamental frequency. Ceramic resonators should not be used. Figure 9 shows the crystal oscillator circuit recommended for proper operation.

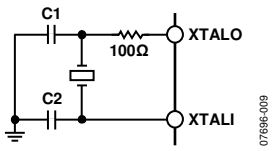


Figure 9. Crystal Oscillator Circuit

The 100 Ω damping resistor on XTALO provides the oscillator with a voltage swing of approximately 2.2 V at the XTALI pin. The crystal shunt capacitance should be 7 pF. Its optimal load capacitance, specified by the manufacturer, should be about 18 pF, although the circuit supports values up to 25 pF. The equivalent series resistance should also be as small as possible. The necessary values of Load Capacitor C1 and Load Capacitor C2 can be calculated from the crystal load capacitance with the following equation:

$$C_L = \frac{C_1 \times C_2}{C_1 + C_2} + C_{STRAY}$$

where C_{STRAY} is the stray capacitance in the circuit and is usually assumed to be approximately 2 pF to 5 pF.

Short trace lengths in the oscillator circuit decrease stray capacitance, thereby increasing the loop gain of the circuit and helping to avoid crystal start-up problems.

On the ADAU1442/ADAU1445/ADAU1446 evaluation boards, the capacitance value for C1 and C2 is 22 pF.

XTALO should not be used to directly drive the crystal signal to another IC. This signal is an analog sine wave and is not appropriate to drive a digital input. A separate pin, CLKOUT, is provided for this purpose. CLKOUT can output 256 × $f_{S,NORMAL}$, 512 × $f_{S,NORMAL}$, or a buffered, digital copy of the crystal oscillator signal to other ICs in the system. CLKOUT is set up using the CLKMODEx pins. For a more detailed explanation of CLKOUT, refer to the Using the ADAU1442/ADAU1445/ADAU1446 as Clock Master section.

Setting Master Clock and PLL Mode

The ADAU1442/ADAU1445/ADAU1446 master clock input feeds a PLL, which generates the 3584 × $f_{S,NORMAL}$ clock (172.032 MHz when $f_{S,NORMAL}$ is 48 kHz) to run the DSP core. This rate is referred to as f_{CORE}. In normal operation, the input to the master clock must be one of the following: 64 × $f_{S,NORMAL}$, 128 × $f_{S,NORMAL}$, 256 × $f_{S,NORMAL}$, 384 × $f_{S,NORMAL}$, or 512 × $f_{S,NORMAL}$, where $f_{S,NORMAL}$ is the audio sampling rate with the core in normal-rate processing mode. The PLL divider mode is set by PLL0, PLL1, and PLL2 as detailed in Table 9.

If the ADAU1442/ADAU1445/ADAU1446 cores are set to receive dual-rate signals (by reducing the number of program steps per sample by a factor of 2 using the DSP core rate select register), then the master clock frequency must be 32 × $f_{S,DUAL}$, 64 × $f_{S,DUAL}$, 128 × $f_{S,DUAL}$, 192 × $f_{S,DUAL}$, or 256 × $f_{S,DUAL}$.

If the ADAU1442/ADAU1445/ADAU1446 cores are set to receive quad-rate signals (by reducing the number of program steps per sample by a factor of 4 using the DSP core rate select register), then the master clock frequency must be 16 × $f_{S,QUAD}$, 32 × $f_{S,QUAD}$, 64 × $f_{S,QUAD}$, 96 × $f_{S,QUAD}$, or 128 × $f_{S,QUAD}$. On power-up, a clock signal must be present on XTALI so that the ADAU1442/ADAU1445/ADAU1446 can complete its initialization routine.

If at any point during operation the clock signal is removed from XTALI, the DSP should be reset to avoid unpredictable behavior on output pins. The clock mode should not be changed without also resetting the ADAU1442/ADAU1445/ADAU1446. If the mode is changed during operation, a click or pop can result on the outputs. The state of the PLLx pins should be changed while $\overline{\text{RESET}}$ is held low.

The phase-locked loop uses the PLL mode select pins (PLL0, PLL1, and PLL2) to derive a 64 × $f_{S,NORMAL}$ clock from whatever signal is present at the XTALI pin. This clock signal is multiplied by 56 to produce the core clock. Therefore, f_{CORE} is 3584 × $f_{S,NORMAL}$. In a system with a $f_{S,NORMAL}$ of 48 kHz, the PLL derives a 3.072 MHz clock and then multiplies it by 56 to produce a 172.032 MHz core clock.

The core clock (f_{CORE}) should never exceed 172.032 MHz, though it may be lower in some applications.

Table 9. PLL Modes

DSP Core Rate[1]	Input to MCLK (XTALI Pin)	PLL2	PLL1	PLL0	PLL Divider[2]	Core Clock Multiplier	Core Clock (f_{CORE})	Instructions per Sample
Normal	64 × $f_{S,NORMAL}$	0	0	0	1	56	3584 × $f_{S,NORMAL}$	3584
	128 × $f_{S,NORMAL}$	0	0	1	2	56	3584 × $f_{S,NORMAL}$	3584
	256 × $f_{S,NORMAL}$	0	1	0	4	56	3584 × $f_{S,NORMAL}$	3584
	384 × $f_{S,NORMAL}$	0	1	1	6	56	3584 × $f_{S,NORMAL}$	3584
	512 × $f_{S,NORMAL}$	1	0	0	8	56	3584 × $f_{S,NORMAL}$	3584
Dual	32 × $f_{S,DUAL}$	0	0	0	1	56	1792 × $f_{S,DUAL}$	1792
	64 × $f_{S,DUAL}$	0	0	1	2	56	1792 × $f_{S,DUAL}$	1792
	128 × $f_{S,DUAL}$	0	1	0	4	56	1792 × $f_{S,DUAL}$	1792
	192 × $f_{S,DUAL}$	0	1	1	6	56	1792 × $f_{S,DUAL}$	1792
	256 × $f_{S,DUAL}$	1	0	0	8	56	1792 × $f_{S,DUAL}$	1792
Quad	16 × $f_{S,QUAD}$	0	0	0	1	56	896 × $f_{S,QUAD}$	896
	32 × $f_{S,QUAD}$	0	0	1	2	56	896 × $f_{S,QUAD}$	896
	64 × $f_{S,QUAD}$	0	1	0	4	56	896 × $f_{S,QUAD}$	896
	96 × $f_{S,QUAD}$	0	1	1	6	56	896 × $f_{S,QUAD}$	896
	128 × $f_{S,QUAD}$	1	0	0	8	56	896 × $f_{S,QUAD}$	896

[1] If the normal DSP core rate ($f_{S,NORMAL}$) is 44.1 kHz, the dual DSP core rate ($f_{S,DUAL}$) is 88.2 kHz, and the quad DSP core rate ($f_{S,QUAD}$) is 176.4 kHz. Likewise, if $f_{S,NORMAL}$ is 48 kHz, then $f_{S,DUAL}$ is 96 kHz and $f_{S,QUAD}$ is 192 kHz.
[2] The PLL divider is set by the PLLx pins.

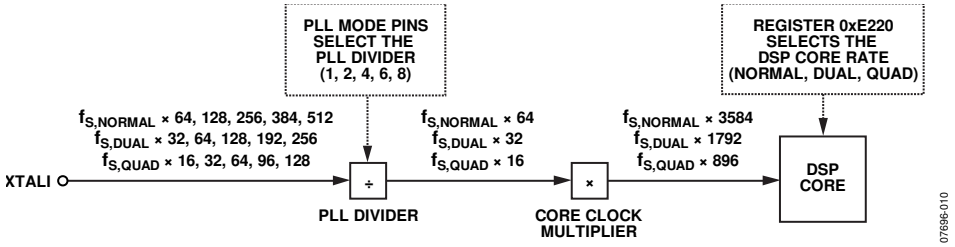


Figure 10. Master Clock Signal Flow

PLL Loop Filter

The PLL loop filter should be connected to the PLL_FILT pin. This filter, shown in Figure 11, includes three passive components—two capacitors and a resistor. The values of these components do not need to be exact; the tolerance can be up to 10% for the resistor and up to 20% for each capacitor. The 3.3 V signal shown in the schematic can be connected to the PVDD supply of the chip.

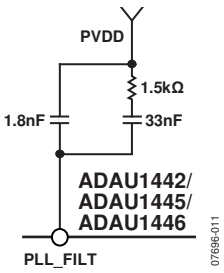


Figure 11. PLL Loop Filter

Using the ADAU1442/ADAU1445/ADAU1446 as Clock Masters

To output a master clock from the ADAU1442/ADAU1445/ADAU1446 to other chips in the system, the CLKOUT pin is used. To set the frequency of this clock signal, the CLKMODEx pins must be set (see Table 10).

Table 10. CLKOUT Modes

CLKOUT Signal	CLKMODE1	CLKMODE0
Disabled	0	0
Buffered Oscillator	0	1
256 × $f_{S,NORMAL}$	1	0
512 × $f_{S,NORMAL}$	1	1

Master Clock and PLL Modes and Settings

DSP Core Rate Select Register (Address 0xE220)

The core's start pulse initiates the operation of the core and determines the sample rate of signals processed inside the core. This pulse can originate from one of three internally generated f_S signals ($f_{S,NORMAL}$, $f_{S,DUAL}$, or $f_{S,QUAD}$), one of the 12 serial input f_S signals (an LRCLK signal associated with a serial input port), one of the 12 serial output f_S signals (an LRCLK signal associated with a serial output port), or LRCLK recovered from the S/PDIF receiver input.

Setting the value of the DSP core rate select register sets the speed of the DSP core (see Table 12). By default, the signals processed in the core are at the normal DSP core rate; therefore, the core clock is 3584 × $f_{S,NORMAL}$. For a system processing signals in the core at the dual rate, the start pulse should be set to the internally generated dual rate, and the core clock is 1792 × $f_{S,DUAL}$. For a system processing signals in the core at the quad rate, the start pulse should be set to the internally generated quad rate, and the core clock is 896 × $f_{S,QUAD}$.

Master Clock Enable Switch Register (Address 0xE280)

For power-saving purposes, various parts of the chip can be switched on and off. Setting the appropriate bit to 0 disables the corresponding subsystem, and setting the bit to 1 enables the subsystem. This is the first register that should be set after the device is powered on and completes its initialization. Failure to set this register may compromise future register writes.

Table 11. Bit Descriptions of Register 0xE280

Bit Position	Description[1]	Default
[15:9]	Reserved	
8	Enable MCLK to auxiliary ADCs	0
7	Enable MCLK to S/PDIF transmitter	0
6	Enable MCLK to S/PDIF receiver	0
5	Enable MCLK to DSP core	0
4	Enable MCLK to Stereo ASRC[7:4][2]	0
3	Enable MCLK to Stereo ASRC[3:0][2]	0
2	Enable MCLK to serial outputs	0
1	Enable MCLK to serial inputs	0
0	Enable MCLK to flexible audio routing matrix (FARM)	0

[1] 0 = disable, 1 = enable.
[2] See the Flexible Audio Routing Matrix—Input Side section for more information.

Table 12. Bit Descriptions of Register 0xE220

Bit Position	Description	Default
[15:5]	Reserved	
[4:0]	Start pulse select 00000 = internally generated normal rate ($f_{S,NORMAL}$) 00001 = internally generated dual rate ($f_{S,DUAL}$) 00010 = internally generated quad rate ($f_{S,QUAD}$) 00011 = f_S from serial input Stereo Pair 0[1] 00100 = f_S from serial input Stereo Pair 1[1] 00101 = f_S from serial input Stereo Pair 2[1] 00110 = f_S from serial input Stereo Pair 3[1] 00111 = f_S from serial input Stereo Pair 4[1] 01000 = f_S from serial input Stereo Pair 5[1] 01001 = f_S from serial input Stereo Pair 6[1] 01010 = f_S from serial input Stereo Pair 7[1] 01011 = f_S from serial input Stereo Pair 8[1] 01100 = f_S from serial input Stereo Pair 9[1] 01101 = f_S from serial input Stereo Pair 10[1] 01110 = f_S from serial input Stereo Pair 11[1] 01111 = f_S from serial output Stereo Pair 0[1] 10000 = f_S from serial output Stereo Pair 1[1] 10001 = f_S from serial output Stereo Pair 2[1] 10010 = f_S from serial output Stereo Pair 3[1] 10011 = f_S from serial output Stereo Pair 4[1] 10100 = f_S from serial output Stereo Pair 5[1] 10101 = f_S from serial output Stereo Pair 6[1] 10110 = f_S from serial output Stereo Pair 7[1] 10111 = f_S from serial output Stereo Pair 8[1] 11000 = f_S from serial output Stereo Pair 9[1] 11001 = f_S from serial output Stereo Pair 10[1] 11010 = f_S from serial output Stereo Pair 11[1] 11011 = f_S from S/PDIF receiver[1] 11100 = no start pulse; core is disabled 11101 = no start pulse; core is disabled 11110 = no start pulse; core is disabled 11111 = no start pulse; core is disabled	00000

[1] f_S is the LRCLK of the associated stereo audio pair in the flexible audio routing matrix whose frequency is dependent on the settings of its associated serial port and the clock pad multiplexer. The intended function of the DSP core rate select register is to allow the DSP core to be synchronized to an external LRCLK signal that is being used by any of the serial ports or S/PDIF receiver.

VOLTAGE REGULATOR

The digital supply voltage of the ADAU1442/ADAU1445/ADAU1446 must be set to 1.8 V. The chip includes an on-board voltage regulator that allows the device to be used in systems where a 1.8 V supply is not available but a 3.3 V supply is. The only external components needed for this are a PNP transistor and one resistor. Only one pin, VDRIVE, is necessary to support the regulator.

The recommended design for the voltage regulator is shown in Figure 12. The 10 µF and 100 nF capacitors shown in this schematic are recommended for bypassing but are not necessary for operation. Each DVDD pin should have its own 100 nF bypass capacitor, but only one bulk capacitor (10 µF) is needed for all pins. In this design, 3.3 V is the main system voltage; 1.8 V is generated at the collector of the transistor, which is connected to the DVDD pins. VDRIVE is connected to the base of the PNP transistor. If the regulator is not used in the design, VDRIVE can be tied to ground.

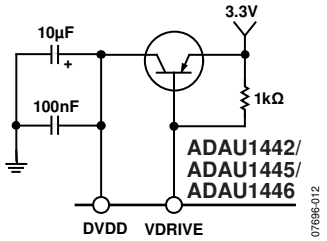


Figure 12. Voltage Regulator Design

Two specifications must be considered when choosing a regulator transistor: the current amplification factor (h_{FE} or beta) should be at least 200, and the collector must be able to dissipate the heat generated when regulating from 3.3 V to 1.8 V. The maximum digital current draw of the ADAU1442 and ADAU1445, which use ASRCs, is 310 mA. The equation to determine the minimum power dissipation specifications of the transistor is as follows:

$$(3.3\ \text{V} - 1.8\ \text{V}) \times 310\ \text{mA} = 465\ \text{mW}$$

Many transistors fit these specifications. Analog Devices recommends the NJT4030P from On Semiconductor. For projects with stringent size constraints, an FMMT734 from Zetex can be used.

The ADAU1446, which does not contain ASRCs, has a lower maximum digital current draw of approximately 235 mA. The maximum power dissipation of the transistor in this case should be around 355 mW.

SRC GROUP DELAY

The group delay of the sample rate converter is dependent on the input and output sampling frequencies as described in the following equations.

For $f_{S\_OUT} > f_{S\_IN}$,

$$GDS = \frac{16}{f_{S\_IN}} + \frac{32}{f_{S\_IN}}$$

For $f_{S\_OUT} < f_{S\_IN}$,

$$GDS = \frac{16}{f_{S\_IN}} + \left(\frac{32}{f_{S\_IN}}\right) \times \left(\frac{f_{S\_IN}}{f_{S\_OUT}}\right)$$

where *GDS* is the group delay in seconds.