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# SigmaDSP Digital Audio Processor

ADAU1462/ADAU1466

FEATURES

Qualified for automotive applications
Fully programmable audio DSP for enhanced sound processing
Features SigmaStudio, a proprietary graphical programming
  tool for the development of custom signal flows
Up to 294.912 MHz, 32-bit SigmaDSP core at 1.2 V
  Up to 24 kWords of program memory
  Up to 80 kWords of parameter/data RAM
  Up to 6144 SIMD instructions per sample at 48 kHz
  Up to 1600 ms digital audio delay pool at 48 kHz
Audio I/O and routing
  4 serial input ports, 4 serial output ports
  48-channel, 32-bit digital I/O up to a sample rate of 192 kHz
  Flexible configuration for TDM, I²S, left and right justified
    formats, and PCM
  Up to 8 stereo ASRCs from 1:8 up to 7.75:1 ratio and
    139 dB dynamic range
  Stereo S/PDIF input and output at 192 kHz
  Four PDM microphone input channels
  Multichannel, byte addressable TDM serial ports

Clock oscillator for generating master clock from crystal
Integer PLL and flexible clock generators
Integrated die temperature sensor
I²C and SPI control interfaces (both slave and master)
Standalone operation
  Self-boot from serial EEPROM
  6-channel, 10-bit SAR auxiliary control ADC
  14 multipurpose pins for digital controls and outputs
On-chip regulator for generating 1.2 V from 3.3 V supply
72-lead, 10 mm × 10 mm LFCSP package with 5.3 mm
  exposed pad
Temperature range: −40°C to +105°C

APPLICATIONS

Automotive audio processing
  Head units
  Distributed amplifiers
  Rear seat entertainment systems
  Trunk amplifiers
Commercial and professional audio processing

FUNCTIONAL BLOCK DIAGRAM
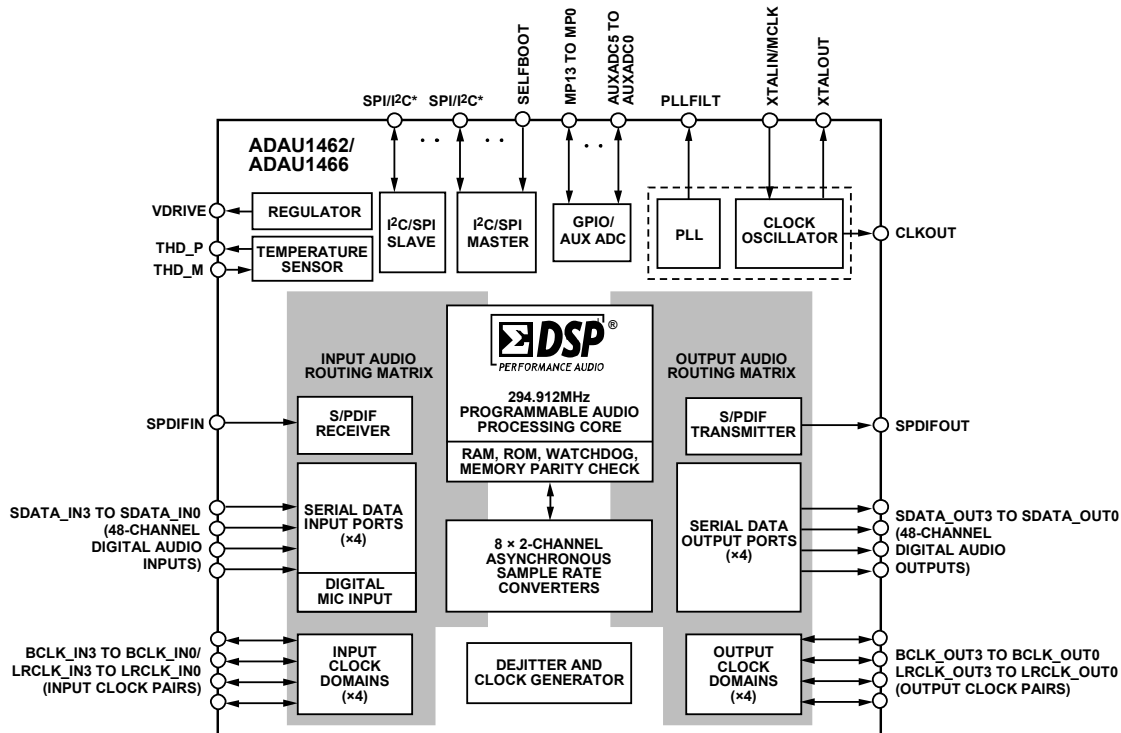
*SPI/I²C INCLUDES THE FOLLOWING PIN FUNCTIONS: SS_M, MOSI_M, SCL_M, SCLK_M, SDA_M, MISO_M, MISO, SDA, SCLK, SCL, MOSI, ADDR1, SS, AND ADDR0 PINS.

Figure 1.

Document Feedback

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Tel: 781.329.4700   ©2017–2018 Analog Devices, Inc. All rights reserved.
Technical Support   **www.analog.com**

TABLE OF CONTENTS

REVISION HISTORY

GENERAL DESCRIPTION

The ADAU1462/ADAU1466 are automotive qualified audio processors that far exceed the digital signal processing capabilities of earlier SigmaDSP® devices. They are pin and register compatible with each other, as well as with the ADAU1450/ADAU1451/ADAU1452 SigmaDSP processors. The restructured hardware architecture is optimized for efficient audio processing. The audio processing algorithms support a seamless combination of stream processing (sample by sample), multirate processing, and block processing paradigms. The SigmaStudio™ graphical programming tool enables the creation of signal processing flows that are interactive, intuitive, and powerful. The enhanced digital signal processor (DSP) core architecture enables some types of audio processing algorithms to be executed using significantly fewer instructions than were required on previous SigmaDSP generations, leading to vastly improved code efficiency.

The 1.2 V, 32-bit DSP core can run at frequencies of up to 294.912 MHz and execute up to 6144 SIMD instructions per sample at the standard sample rate of 48 kHz. Powerful clock generator hardware, including a flexible phase-locked loop (PLL) with multiple fractional integer outputs, supports all industry standard audio sample rates. Nonstandard rates over a wide range can generate up to 15 sample rates simultaneously. These clock generators, along with the on board asynchronous sample rate converters (ASRCs) and a flexible hardware audio routing matrix, make the ADAU1462/ADAU1466 ideal audio hubs that greatly simplify the design of complex multirate audio systems.

The ADAU1462/ADAU1466 interface with a wide range of analog-to-digital converters (ADCs), digital-to-analog converters (DACs), digital audio devices, amplifiers, and control circuitry with highly configurable serial ports, I²C, serial peripheral interface (SPI), Sony/Philips Digital Interconnect Format (S/PDIF) interfaces, and multipurpose input/output (I/O) pins.

Dedicated decimation filters can decode the pulse code modulation (PDM) output of up to four MEMS microphones.

Independent slave and master I²C/SPI control ports allow the ADAU1462/ADAU1466 to be programmed and controlled by an external master device such as a microcontroller, and to program and control slave peripherals directly. Self boot functionality and the master control port enable complex standalone systems.

The power efficient DSP core can execute at high computational loads while consuming only a few hundred milliwatts (mW) in typical conditions. This relatively low power consumption and small footprint make the ADAU1462/ADAU1466 ideal replacements for large, general-purpose DSPs that consume more power at the same processing load.

Note that throughout this data sheet, multifunction pins, such as SS_M/MP0, are referred to either by the entire pin name or by a single function of the pin, for example, MP0, when only that function is relevant.

DIFFERENCES BETWEEN THE ADAU1466 AND ADAU1462

The three variants of this device are differentiated by memory and DSP core frequency. A detailed summary of the differences is listed in Table 1.

Table 1. Product Selection Table

Device	Data Memory (kWords)	Program Memory (kWords)	DSP Core Frequency (MHz)
ADAU1462WBCPZ300	48	16	294.912
ADAU1462WBCPZ150	48	16	147.456
ADAU1466 WBCPZ300	80	24	294.912

SPECIFICATIONS

AVDD = 3.3 V ± 10%, DVDD = 1.2 V ± 5%, PVDD = 3.3 V ± 10%, IOVDD = 1.8 V − 5% to 3.3 V + 10%, T_A = 25°C, master clock input = 12.288 MHz, core clock (f_{CORE}) = 294.912 MHz, I/O pins set to low drive setting, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER					
Supply Voltage					
Analog Voltage (AVDD)	2.97	3.3	3.63	V	Supply for analog circuitry, including auxiliary ADC
Digital Voltage (DVDD)	1.14	1.2	1.26	V	Supply for digital circuitry, including the DSP core, ASRCs, and signal routing
PLL Voltage (PVDD)	2.97	3.3	3.63	V	Supply for PLL circuitry
I/O Supply Voltage (IOVDD)	1.71	3.3	3.63	V	Supply for input/output circuitry, including pads and level shifters
Supply Current					
Analog Current (AVDD)	1.36	1.66	2	mA	
Idle State	1.00	1.10	40	µA	Power applied, chip not programmed
Reset State	1.00	1.10	40	µA	Power applied, $\overline{RESET}$ held low
PLL Current (PVDD)	8.3	10.1	12.9	mA	12.288 MHz MCLK with default PLL settings
Idle State	18.3	18.7	40	µA	Power applied, PLL not configured
Reset State	18.3	18.7	40	µA	Power applied, $\overline{RESET}$ held low
I/O Current (IOVDD)					Dependent on the number of active serial ports, clock pins, and characteristics of external loads
Operation State		53		mA	IOVDD = 3.3 V; all serial ports are clock masters
		22		mA	IOVDD = 1.8 V; all serial ports are clock masters
Power-Down State		4.1	4.2	mA	IOVDD = 1.8 V − 5% to 3.3 V + 10%
Digital Current (DVDD)					
ADAU1466 Operation State					
Maximum Program		233	495	mA	
Typical Program		220		mA	Test program includes 16-channel I/O, 10-band equalizer (EQ) per channel, all ASRCs active
Minimal Program		213		mA	Test program includes 2-channel I/O, 10-band EQ per channel
ADAU1462 Operation State					
f_{CORE} = 294.912 MHz					
Maximum Program		233	495	mA	
Typical Program		220		mA	Test program includes 16-channel I/O, 10-band EQ per channel, all ASRCs active
Minimal Program		213		mA	Test program includes 2-channel I/O, 10-band EQ per channel
f_{CORE} = 147.456 MHz					
Maximum Program		170	455	mA	
Typical Program		135		mA	Test program includes 16-channel I/O, 10-band EQ per channel
Minimal Program		110		mA	Test program includes 2-channel I/O, 10-band EQ per channel
Idle State	18.3	18.7	19.9	mA	Power applied, DSP not enabled
Reset State	18.3	18.7	19.9	mA	Power applied, $\overline{RESET}$ held low
ASYNCHRONOUS SAMPLE RATE CONVERTERS					
Dynamic Range		139		dB	A-weighted, 20 Hz to 20 kHz
I/O Sample Rate	6		192	kHz	
I/O Sample Rate Ratio	1:8		7.75:1		
Total Harmonic Distortion + Noise (THD + N)			−120	dB	
CRYSTAL OSCILLATOR					
Transconductance	8.3	10.6	13.4	mS	
REGULATOR					
DVDD Voltage	1.14	1.2		V	Regulator maintains typical output voltage up to a maximum 800 mA load; IOVDD = 1.8 V − 5% to 3.3 V + 10%

AVDD = 3.3 V ± 10%, DVDD = 1.2 V ± 5%, PVDD = 3.3 V ± 10%, IOVDD = 1.8 V − 5% to 3.3 V + 10%, T_A = −40°C to +105°C, master clock input = 12.288 MHz, f_{CORE} = 294.912 MHz, I/O pins set to low drive setting, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER					
Supply Voltage					
Analog Voltage (AVDD)	2.97	3.3	3.63	V	Supply for analog circuitry, including auxiliary ADC
Digital Voltage (DVDD)	1.14	1.2	1.26	V	Supply for digital circuitry, including the DSP core, ASRCs, and signal routing
PLL Voltage (PVDD)	2.97	3.3	3.63	V	Supply for PLL circuitry
IOVDD Voltage (IOVDD)	1.71	3.3	3.63	V	Supply for input/output circuitry, including pads and level shifters
Supply Current					
Analog Current (AVDD)	1.36	1.66	2	mA	
Idle State	1.0	1.1	40	µA	
Reset State	1.0	1.1	40	µA	
PLL Current (PVDD)	8.3	10.2	15	mA	12.288 MHz master clock; default PLL settings
Idle State	18.4	18.7	40	µA	Power applied, PLL not configured
Reset State	18.4	18.7	40	µA	Power applied, $\overline{RESET}$ held low
I/O Current (IOVDD)					Dependent on the number of active serial ports, clock pins, and characteristics of external loads
Operation State		53		mA	IOVDD = 3.3 V; all serial ports are clock masters
		22		mA	IOVDD = 1.8 V; all serial ports are clock masters
Power-Down State		4.1	4.3	mA	IOVDD = 1.8 V − 5% to 3.3 V + 10%
Digital Current (DVDD)					
ADAU1466 Operation State					
Maximum Program		485	920	mA	
Typical Program		330		mA	Test program includes 16-channel I/O, 10-band EQ per channel, all ASRCs active
Minimal Program		213		mA	Test program includes 2-channel I/O, 10-band EQ per channel
ADAU1462 Operation State					
f_{CORE} = 294.912 MHz					
Maximum Program		485	920	mA	
Typical Program		330		mA	Test program includes 16-channel I/O, 10-band EQ per channel, all ASRCs active
Minimal Program		213		mA	Test program includes 2-channel I/O, 10-band EQ per channel
f_{CORE} = 147.456 MHz					
Maximum Program		270	490	mA	
Typical Program		220		mA	Test program includes 16-channel I/O, 10-band EQ per channel, all ASRCs active
Minimal Program		210		mA	Test program includes 2-channel I/O, 10-band EQ per channel
Idle State	5.9	15.7	559	mA	Power applied, DSP not enabled
Reset State	5.9	15.7	559	mA	Power applied, $\overline{RESET}$ held low
ASYNCHRONOUS SAMPLE RATE CONVERTERS					
Dynamic Range		139		dB	A-weighted, 20 Hz to 20 kHz
I/O Sample Rate	6		192	kHz	
I/O Sample Rate Ratio	1:8		7.75:1		
THD + N			−120	dB	
CRYSTAL OSCILLATOR					
Transconductance	8.1	10.6	14.6	mS	
REGULATOR					
DVDD Voltage	1.14	1.2		V	Regulator maintains typical output voltage up to a maximum 800 mA load; IOVDD = 1.8 V − 5% to 3.3 V + 10%

ELECTRICAL CHARACTERISTICS

Digital Input/Output

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUT					
Input Voltage					Excluding SPDIFIN, which is not a standard digital input
IOVDD = 3.3 V					
High Level (V_{IH})	1.71		3.3	V	
Low Level (V_{IL})	0		1.71	V	
IOVDD = 1.8 V					
High Level (V_{IH})	0.92		1.8	V	
Low Level (V_{IL})	0		0.89	V	
Input Leakage					
High Level (I_{IH})			2	µA	Digital input pins with pull-up resistor
			14	µA	Digital input pins with pull-down resistor
			2	µA	Digital input pins with no pull resistor
			8	µA	MCLK
			120	µA	SPDIFIN
Low Level (I_{IL}) at 0 V	−14			µA	Digital input pins with pull-up resistor
	−2			µA	Digital input pins with pull-down resistor
	−2			µA	Digital input pins with no pull resistor
	−8			µA	MCLK
	−120			µA	SPDIFIN
Input Capacitance (C_I)		2		pF	Guaranteed by design
DIGITAL OUTPUT					
Output Voltage					
IOVDD = 3.3 V					
High Level (V_{OH})	3.09		3.3	V	I_{OH} = 1 mA
Low Level (V_{OL})	0		0.26	V	I_{OL} = 1 mA
IOVDD = 1.8 V					
High Level (V_{OH})	1.45		1.8		
Low Level (V_{OL})	0		0.33		
Digital Output Pins, Output Drive					The digital output pins are driving low impedance PCB traces to a high impedance digital input buffer
IOVDD = 1.8 V					
Drive Strength Setting					
Lowest			1	mA	The digital output pins are not designed for static current draw; do not use these pins to drive LEDs directly
Low			2	mA	The digital output pins are not designed for static current draw; do not use these pins to drive LEDs directly
High			3	mA	The digital output pins are not designed for static current draw; do not use these pins to drive LEDs directly
Highest			5	mA	The digital output pins are not designed for static current draw; do not use these pins to drive LEDs directly
IOVDD = 3.3 V					
Drive Strength Setting					
Lowest			2	mA	The digital output pins are not designed for static current draw; do not use these pins to drive LEDs directly
Low			5	mA	The digital output pins are not designed for static current draw; do not use these pins to drive LEDs directly
High			10	mA	The digital output pins are not designed for static current draw; do not use these pins to drive LEDs directly
Highest			15	mA	The digital output pins are not designed for static current draw; do not use these pins to drive LEDs directly

Auxiliary ADC

T_A = −40°C to +105°C, DVDD = 1.2 V ± 5%, AVDD = 3.3 V ± 10%, IOVDD = 1.8 V − 5% to 3.3 V + 10%, unless otherwise noted.

Table 5.

Parameter	Min	Typ	Max	Unit
RESOLUTION		10		Bits
FULL-SCALE ANALOG INPUT		AVDD		V
NONLINEARITY				
Integrated Nonlinearity (INL)	−2.5		+2.5	LSB
Differential Nonlinearity (DNL)	−2.5		+2.5	LSB
GAIN ERROR	−2.5		+2.5	LSB
INPUT IMPEDANCE		200		kΩ
SAMPLE RATE		f_{CORE}/6144		Hz

TIMING SPECIFICATIONS

Master Clock Input

$T_A = -40°C$ to $+105°C$, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 5% to 3.3 V + 10%, unless otherwise noted.

Table 6.

Parameter	Min	Max	Unit	Description
MASTER CLOCK INPUT (MCLK)				
f_{MCLK}	2.375	36	MHz	MCLK frequency
t_{MCLK}	27.8	421	ns	MCLK period
t_{MCLKD}	25	75	%	MCLK duty cycle
t_{MCLKH}	$0.25 \times t_{MCLK}$	$0.75 \times t_{MCLK}$	ns	MCLK width high
t_{MCLKL}	$0.25 \times t_{MCLK}$	$0.75 \times t_{MCLK}$	ns	MCLK width low
CLKOUT Jitter	12	106	ps	Cycle to cycle rms average
CORE CLOCK				
f_{CORE}				
ADAU1462 and ADAU1466	152	294.912	MHz	System (DSP core) clock frequency; PLL feedback divider ranges from 64 to 108
t_{CORE}[1]				
ADAU1462 and ADAU1466	3.39		ns	System (DSP core) clock period

[1] Not shown in Figure 2.
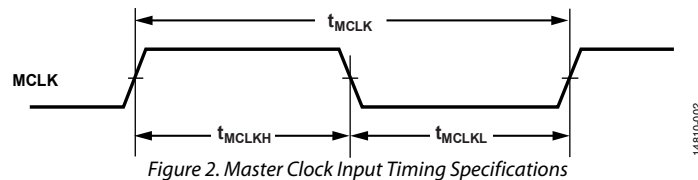
Figure 2. Master Clock Input Timing Specifications

RESET

$T_A = -40°C$ to $+105°C$, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 5% to 3.3 V + 10%.

Table 7.

Parameter	Min	Max	Unit	Description
t_{WRST}	10		ns	Reset pulse width low
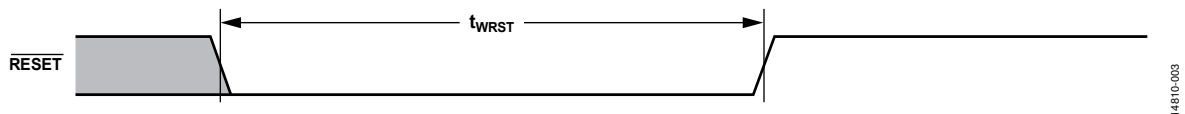
Figure 3. Reset Timing Specification

Serial Ports

$T_A = -40°C$ to $+105°C$, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 5% to 3.3 V + 10%, unless otherwise noted. BCLK in Table 8 refers to BCLK_OUT3 to BCLK_OUT0 and BCLK_IN3 to BCLK_IN0. LRCLK refers to LRCLK_OUT3 to LRCLK_OUT0 and LRCLK_IN3 to LRCKL_IN0.

Table 8.

Parameter	Min	Max	Unit	Description
f_{LRCLK}		192	kHz	LRCLK frequency
t_{LRCLK}	5.21		µs	LRCLK period
f_{BCLK}		24.576	MHz	BCLK frequency, sample rate ranging from 6 kHz to 192 kHz
t_{BCLK}	40.7		ns	BCLK period
t_{BIL}	10		ns	BCLK low pulse width, slave mode; BCLK frequency = 24.576 MHz; BCLK period = 40.6 ns
t_{BIH}	14.5		ns	BCLK high pulse width, slave mode; BCLK frequency = 24.576 MHz; BCLK period = 40.6 ns
t_{LIS}	20		ns	LRCLK setup to BCLK_INx input rising edge, slave mode; LRCLK frequency = 192 kHz
t_{LIH}	5		ns	LRCLK hold from BCLK_INx input rising edge, slave mode; LRCLK frequency = 192 kHz
t_{SIS}	5		ns	SDATA_INx setup to BCLK_INx input rising edge
t_{SIH}	5		ns	SDATA_INx hold from BCLK_INx input rising edge
t_{TS}		10	ns	BCLK_OUTx output falling edge to LRCLK_OUTx output timing skew, slave
t_{SODS}		35	ns	SDATA_OUTx delay in slave mode from BCLK_OUTx output falling edge; serial outputs function in slave mode at all valid sample rates, provided that the external circuit design provides sufficient electrical signal integrity
t_{SODM}		10	ns	SDATA_OUTx delay in master mode from BCLK_OUTx output falling edge
t_{TM}		5	ns	BCLK falling edge to LRCLK timing skew, master
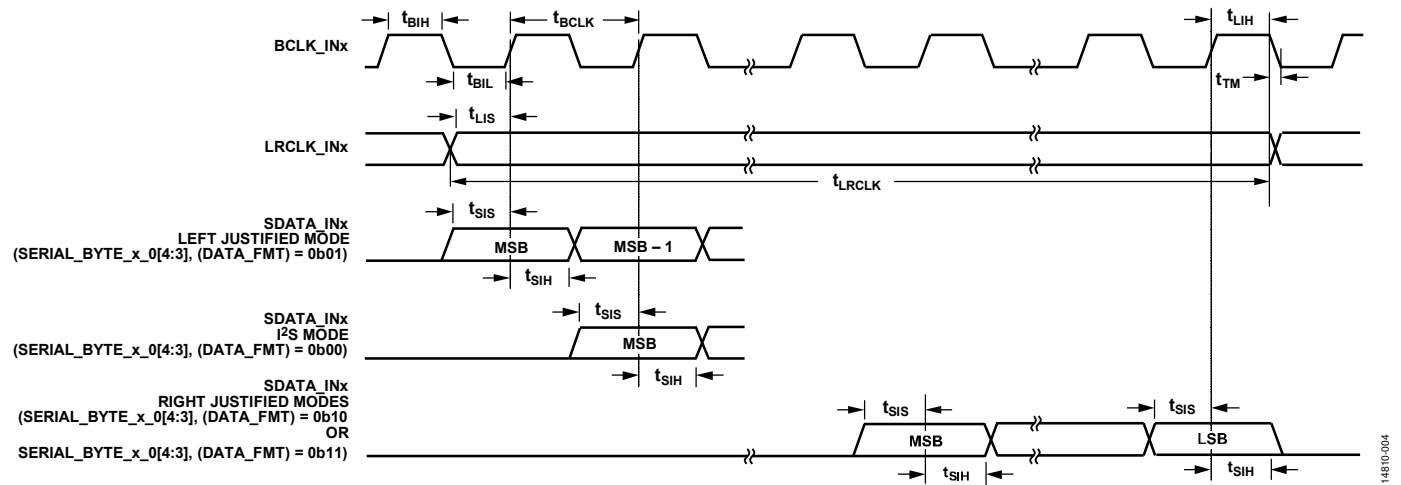
Figure 4. Serial Input Port Timing Specifications
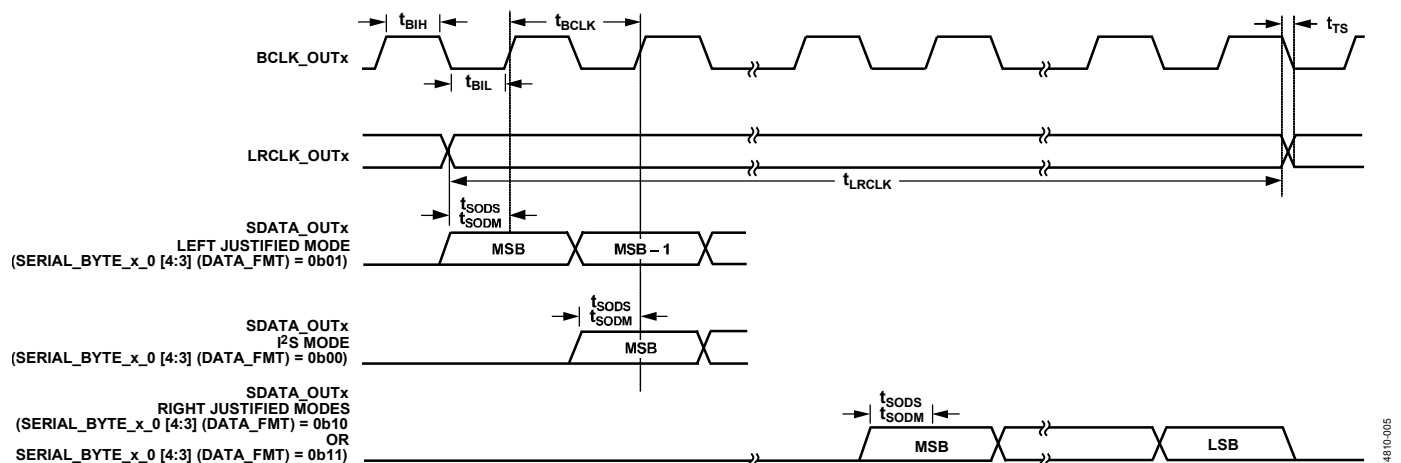
Figure 5. Serial Output Port Timing Specifications

Multipurpose Pins (MPx)

$T_A = -40°C$ to $+105°C$, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 5% to 3.3 V + 10%.

Table 9.

Parameter	Min	Max	Unit	Description
f_{MP}		24.576	MHz	MPx maximum switching rate when pin is configured as a general-purpose input or general-purpose output
t_{MPIL}	$10 \times t_{CORE}$	$6144 \times t_{CORE}$	sec	MPx pin input latency until high/low value is read by core; the duration in the Max column is equal to the period of one audio sample when the DSP is processing 6144 instructions per sample

S/PDIF Transmitter and Receiver

$T_A = -40°C$ to $+105°C$, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 10% to 3.3 V + 10%.

Table 10.

Parameter	Min	Max	Unit	Description
AUDIO SAMPLE RATE				
Transmitter	18	192	kHz	Audio sample rate of data output from S/PDIF transmitter
Receiver	18	192	kHz	Audio sample rate of data input to S/PDIF receiver

I²C Interface—Slave

T_A = −40°C to +105°C, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 5% to 3.3 V + 10%, default drive strength (f_{SCL}) = 400 kHz.

Table 11.

Parameter	Min	Max	Unit	Description
f_{SCL}		1000	kHz	SCL clock frequency
t_{SCLH}	0.26		µs	SCL pulse width high
t_{SCLL}	0.5		µs	SCL pulse width low
t_{SCS}	0.26		µs	Start and repeated start condition setup time
t_{SCH}	0.26		µs	Start condition hold time
t_{DS}	50		ns	Data setup time
t_{DH}		0.45	µs	Data hold time
t_{SCLR}		120	ns	SCL rise time
t_{SCLF}		120	ns	SCL fall time
t_{SDR}		120	ns	SDA rise time
t_{SDF}		120	ns	SDA fall time
t_{BFT}	0.5		µs	Bus free time between stop and start
t_{SUSTO}	0.26		µs	Stop condition setup time

Figure 6. I²C Slave Port Timing Specifications

I²C Interface—Master

T_A = −40°C to +105°C, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 5% to 3.3 V + 10%.

Table 12.

Parameter	Min	Max	Unit	Description
f_{SCL}		1000	kHz	SCL clock frequency
t_{SCLH}	0.26		µs	SCL pulse width high
t_{SCLL}	0.5		µs	SCL pulse width low
t_{SCS}	0.26		µs	Start and repeated start condition setup time
t_{SCH}	0.26		µs	Start condition hold time
t_{DS}	50		ns	Data setup time
t_{DH}		0.45	µs	Data hold time
t_{SCLR}		120	ns	SCL rise time
t_{SCLF}		120	ns	SCL fall time
t_{SDR}		120	ns	SDA rise time
t_{SDF}		120	ns	SDA fall time
t_{BFT}	0.5		µs	Bus free time between stop and start
t_{SUSTO}	0.26		µs	Stop condition setup time

Figure 7. I²C Master Port Timing Specifications

SPI Interface—Slave

$T_A = -40°C$ to $+105°C$, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 5% to 3.3 V + 10%.

Table 13.

Parameter	Min	Max	Unit	Description
$f_{SCLK_{WRITE}}$		20	MHz	SCLK write frequency
$f_{SCLK_{READ}}$		20	MHz	SCLK read frequency
$t_{SCLKPWL}$	6		ns	SCLK pulse width low, SCLK = 20 MHz
$t_{SCLKPWH}$	21		ns	SCLK pulse width high, SCLK = 20 MHz
t_{SSS}	1		ns	SS setup to SCLK rising edge
t_{SSH}	2		ns	SS hold from SCLK rising edge
t_{SSPWH}	10		ns	SS pulse width high
t_{MOSIS}	1		ns	MOSI setup to SCLK rising edge
t_{MOSIH}	2		ns	MOSI hold from SCLK rising edge
t_{MISOD}		39	ns	MISO valid output delay from SCLK falling edge
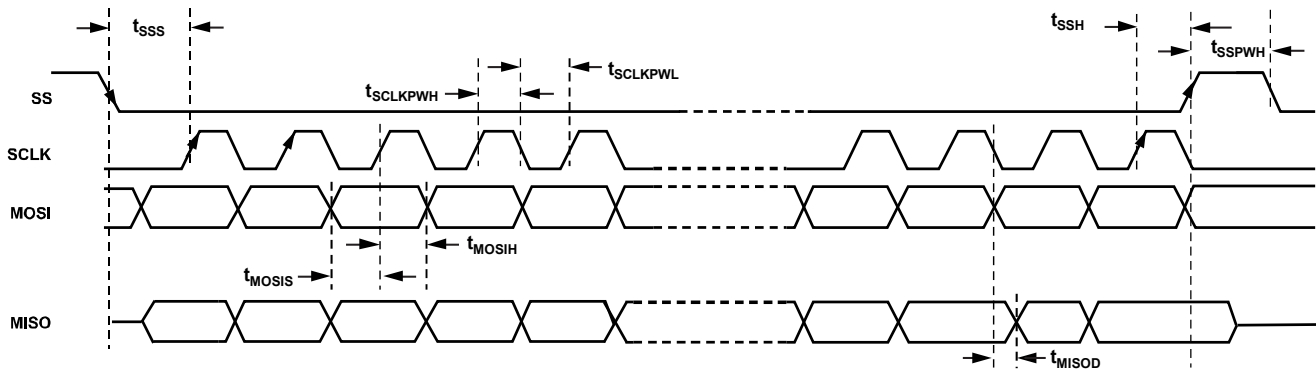
Figure 8. SPI Slave Port Timing Specifications

SPI Interface—Master

$T_A = -40°C$ to $+105°C$, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 5% to 3.3 V + 10%.

Table 14.

Parameter	Min	Max	Unit	Description
Timing Requirements				
t_{SSPIDM}	15		ns	MISO_M data input valid to SCLK_M edge (data input setup time)
t_{HSPIDM}	5		ns	SCLK_M last sampling edge to data input not valid (data input hold time)
Switching Characteristics				
$t_{SPICLKM}$	41.7		ns	SPI master clock cycle period
f_{SCLK_M}		24	MHz	SPI master clock frequency
t_{SPICHM}	17		ns	SCLK_M high period (f_{SCLK_M} = 24 MHz)
t_{SPICLM}	17		ns	SCLK_M low period (f_{SCLK_M} = 24 MHz)
$t_{DDSPIDM}$		16.9	ns	SCLK_M edge to data out valid (data out delay time) (f_{SCLK_M} = 24 MHz)
$t_{HDSPIDM}$	21		ns	SCLK_M edge to data out not valid (data out hold time) (f_{SCLK_M} = 24 MHz)
t_{SDSCIM}	36		ns	SS_M (SPI device select) low to first SCLK_M edge (f_{SCLK_M} = 24 MHz)
t_{HDSM}	95		ns	Last SCLK_M edge to SS_M high (f_{SCLK_M} = 24 MHz)
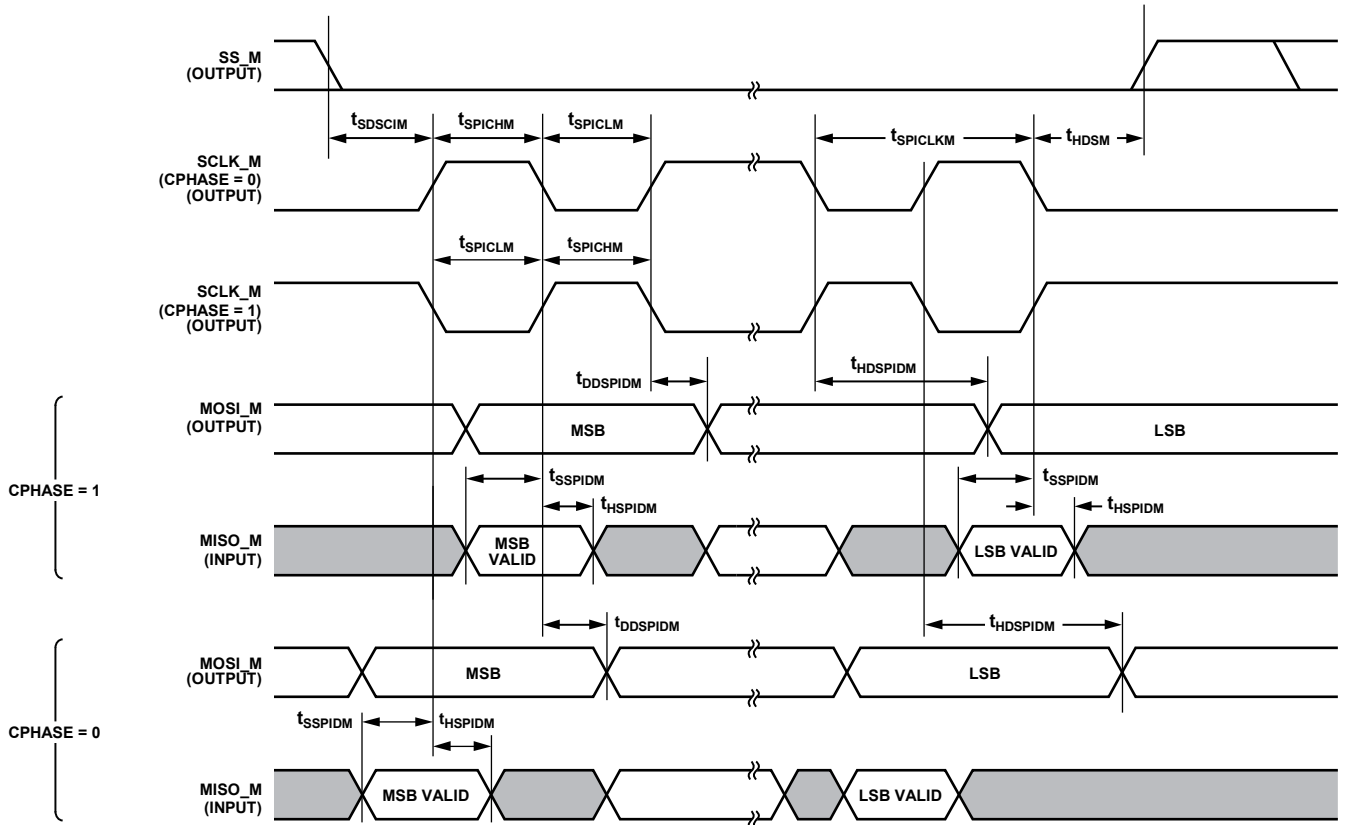
Figure 9. SPI Master Port Timing Specifications

PDM Inputs

T_A = −40°C to +105°C, DVDD = 1.2 V ± 5%, IOVDD = 1.8 V − 5% to 3.3 V + 10%. Pulse density modulation (PDM) data is latched on both edges of the clock (see Figure 10).

Table 15.

Parameter	t_{MIN}	t_{MAX}	Unit	Description
t_{SETUP}	10		ns	Data setup time
t_{HOLD}	5		ns	Data hold time
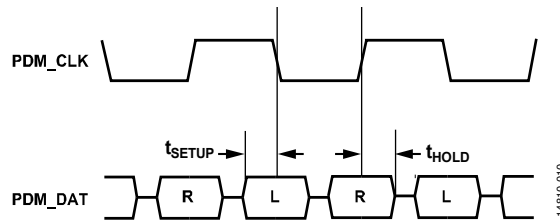
Figure 10. PDM Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 16.

Parameter	Rating
DVDD to Ground	0 V to 1.4 V
AVDD to Ground	0 V to 4.0 V
IOVDD to Ground	0 V to 4.0 V
PVDD to Ground	0 V to 4.0 V
Digital Inputs	DGND − 0.3 V to IOVDD + 0.3 V
Maximum Ambient Temperature Range	−40°C to +105°C
Maximum Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C
Soldering (10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CONSIDERATIONS

The capabilities of the ADAU1462/ADAU1466 are such that it is possible to configure the device in a mode where its power dissipation can risk exceeding the absolute maximum junction temperature. The junction temperature reached in a device is influenced by several factors, for example, the power dissipated in the device; the thermal efficiency of the printed circuit board (PCB) design; the maximum ambient temperature supported in the application.

To ensure that the ADAU1462/ADAU1466 does not exceed its absolute maximum junction temperature in an application, thermal considerations must be taken from the start of the design (for example: likely modes of operation, thermal considerations in the PCB design (see the AN-772 Application Note), and thermal simulations) to its finish (qualification at the maximum ambient temperature supported in the application).

While all of the following thermal coefficients can be used to analyze the thermal performance of ADAU1462/ADAU1466, ψ_{JT} is the most reflective of real-world applications and is recommended as the primary approach for thermal qualification.

Table 17. Thermal Coefficients for ADAU1462/ADAU1466

Thermal Coefficient	Value	Unit
ψ_{JT}[1]	0.15	°C/W
θ_{JA}[1]	29.15	°C/W
θ_{JB}[2]	10.59	°C/W
θ_{JCT}[3]	0.04	°C/W
θ_{JCB}[4]	3.39	°C/W

[1] Based on simulation using a JEDEC 2s2p thermal test PCB with 25 thermal vias in a JEDEC natural convection environment, as per JESD51.
[2] Based on simulation using a JEDEC 2s2p thermal test PCB with 25 thermal vias in a JEDEC Junction to Board environment, as per JESD51.
[3] Based on simulation using a cold plate attached directly to exposed paddle.

To employ the ψ_{JT}-based approach to thermal analysis,

1. Configure the ADAU1462/ADAU1466 in the highest power mode of operation to be used in the application and record the power dissipated in the device.
2. Compute the maximum allowable surface temperature, T_{S_MAX}:

   $$T_{S\_MAX} = T_{J\_MAX} - (Power \times \psi_{JT})$$

3. Measure the case temperature at the center of the ADAU1462/ADAU1466 package (T_S) at the maximum ambient temperature supported in the application and compare to T_{S_MAX}.
4. For safe operation, use $T_S < T_{S\_MAX}$ in the highest power mode of operation in the application.

For more information, see the PCB Design Considerations section and the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Figure 11. Pin Configuration
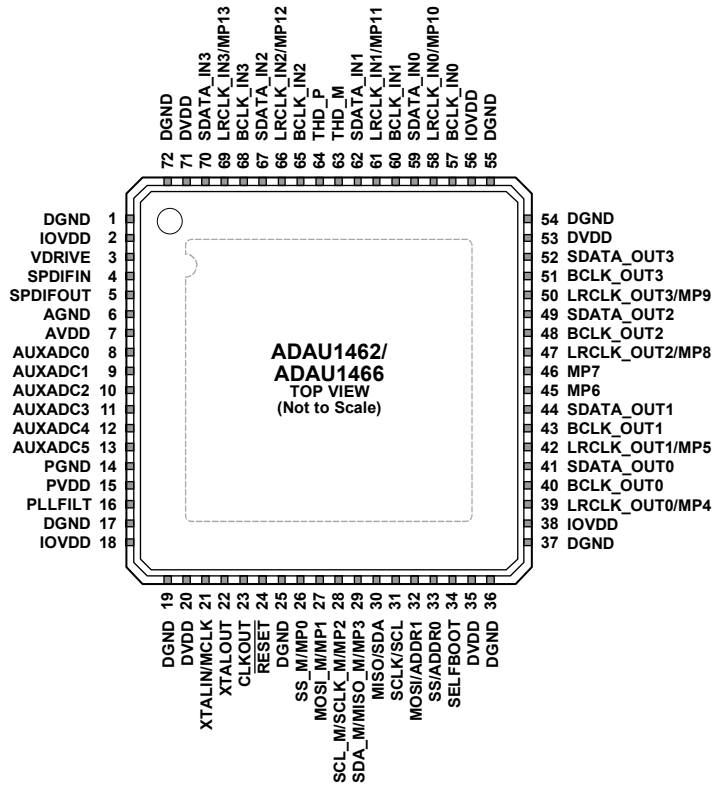
NOTES
1. THE EXPOSED PAD MUST BE GROUNDED BY SOLDERING IT TO A COPPER SQUARE OF EQUIVALENT SIZE ON THE PCB. IDENTICAL COPPER SQUARES MUST EXIST ON ALL LAYERS OF THE BOARD, CONNECTED BY VIAS, AND THEY MUST BE CONNECTED TO A DEDICATED COPPER GROUND LAYER WITHIN THE PCB.

Table 18. Pin Function Descriptions

Pin No.	Mnemonic	Internal Pull Resistor	Description
1	DGND	None	Digital and I/O Ground Reference. Tie all DGND, AGND, and PGND pins directly together in a common ground plane. See the Power Supply Bypass Capacitors and Grounding sections.
2	IOVDD	None	Input/Output Supply, 1.8 V – 5% to 3.3 V + 10%. Bypass this pin with decoupling capacitors to Pin 1 (DGND). See the Power Supply Bypass Capacitors and Grounding sections.
3	VDRIVE	None	PNP Bipolar Junction Transistor-Base Drive Bias Pin for the Digital Supply Regulator. Connect VDRIVE to the base of an external PNP pass transistor (ON Semi NSS1C300ET4G is recommended). If an external supply is provided directly to DVDD, connect the VDRIVE pin to ground.
4	SPDIFIN	None	Input to the Integrated Sony/Philips Digital Interconnect Format Receiver. Disconnect this pin when not in use. This pin is internally biased to IOVDD/2.
5	SPDIFOUT	Configurable	Output from the Integrated Sony/Philips Digital Interface Format Transmitter. Disconnect this pin when not in use. This pin is internally biased to IOVDD/2.
6	AGND	None	Analog Ground Reference. Tie all DGND, AGND, and PGND pins directly together in a common ground plane. See the Power Supply Bypass Capacitors and Grounding sections.
7	AVDD	None	Analog (Auxiliary ADC) Supply. Must be 3.3 V ± 10%. Bypass this pin with decoupling capacitors to Pin 6 (AGND). See the Power Supply Bypass Capacitors and Grounding sections.
8	AUXADC0	None	Auxiliary ADC Input Channel 0. This pin reads an analog input signal and uses its value in the DSP program. Disconnect this pin when not in use.
9	AUXADC1	None	Auxiliary ADC Input Channel 1. This pin reads an analog input signal and uses its value in the DSP program. Disconnect this pin when not in use.
10	AUXADC2	None	Auxiliary ADC Input Channel 2. This pin reads an analog input signal and uses its value in the DSP program. Disconnect this pin when not in use.

Pin No.	Mnemonic	Internal Pull Resistor	Description
11	AUXADC3	None	Auxiliary ADC Input Channel 3. This pin reads an analog input signal and uses its value in the DSP program. Disconnect this pin when not in use.
12	AUXADC4	None	Auxiliary ADC Input Channel 4. This pin reads an analog input signal and uses its value in the DSP program. Disconnect this pin when not in use.
13	AUXADC5	None	Auxiliary ADC Input Channel 5. This pin reads an analog input signal and uses its value in the DSP program. Disconnect this pin when not in use.
14	PGND	None	PLL Ground Reference. Tie all DGND, AGND, and PGND pins directly together in a common ground plane. See the Power Supply Bypass Capacitors and Grounding sections.
15	PVDD	None	PLL Supply. Must be 3.3 V ± 10%. Bypass this pin with decoupling capacitors to Pin 14 (PGND). See the Power Supply Bypass Capacitors and Grounding sections.
16	PLLFILT	None	PLL Filter. The voltage on the PLLFILT pin, which is internally generated, is typically between 1.65 V and 2.10 V.
17	DGND	None	Digital and I/O Ground Reference. Tie all DGND, AGND, and PGND pins directly together in a common ground plane. See the Power Supply Bypass Capacitors and Grounding sections.
18	IOVDD	None	Input/Output Supply, 1.8 V − 5% to 3.3 V + 10%. Bypass this pin to Pin 17 (DGND) with decoupling capacitors. See the Power Supply Bypass Capacitors and Grounding sections.
19	DGND	None	Digital and I/O Ground Reference. Tie all DGND, AGND, and PGND pins directly together in a common ground plane. See the Power Supply Bypass Capacitors and Grounding sections.
20	DVDD	None	Digital Supply. Must be 1.2 V ± 5%. This pin can be supplied externally or by using the internal regulator and external pass transistor. Bypass this pin to Pin 19 (DGND) with decoupling capacitors. See the Power Supply Bypass Capacitors and Grounding sections.
21	XTALIN/MCLK	None	Crystal Oscillator Input (XTALIN)/Master Clock Input to the PLL (MCLK). This pin can be supplied directly or generated by driving a crystal with the internal crystal oscillator via Pin 22 (XTALOUT). If a crystal is used, refer to the circuit shown in Figure 14.
22	XTALOUT	None	Crystal Oscillator Output for Driving an External Crystal. If a crystal is used, refer to the circuit shown in Figure 14. Disconnect this pin when not in use.
23	CLKOUT	Configurable	Master Clock Output. This pin drives a master clock signal to other ICs in the system. CLKOUT can be configured to output a clock signal with a frequency of 1×, 2×, 4×, or 8× the frequency of the divided clock signal being input to the PLL. Disconnect this pin when not in use.
24	$\overline{\text{RESET}}$	Pull-down	Active Low Reset Input. A reset is triggered on a high to low edge and exited on a low to high edge. A reset event sets all RAMs and registers to their default values.
25	DGND	None	Digital and I/O Ground Reference. Tie all DGND, AGND, and PGND pins directly together in a common ground plane. See the Power Supply Bypass Capacitors and Grounding sections.
26	SS_M/MP0	Pull-up; nominally 250 kΩ; can be disabled by a write to control register	SPI Master/Slave Select Port (SS_M)/Multipurpose, General-Purpose Input/Output (MP0). When in SPI master mode, this pin acts as the slave select signal to slave devices on the SPI bus. The pin must go low at the beginning of a master SPI transaction and high at the end of a transaction. This pin has an internal pull-up resistor that is nominally 250 kΩ. When the SELFBOOT pin is held high and the $\overline{\text{RESET}}$ pin has a transition from low to high, Pin 26 sets the communications protocol for self boot operation. If this pin is left floating, the SPI communications protocol is used for self boot operation. If this pin has a 10 kΩ pull-down resistor to DGND, the I²C communications protocol is used for self boot operation. When self boot operation is not used and this pin is not needed as a general-purpose input or output, leave it disconnected.
27	MOSI_M/MP1	Pull-up; can be disabled by a write to control register	SPI Master Data Output Port (MOSI_M)/Multipurpose, General-Purpose Input/Output (MP1). When in SPI master mode, this pin sends data from the SPI master port to slave devices on the SPI bus. Disconnect this pin when not in use.
28	SCL_M/ SCLK_M/MP2	Pull-up; can be disabled by a write to control register	I²C Master Serial Clock Port (SCL_M)/SPI Master Mode Serial Clock (SCLK_M)/Multipurpose, General-Purpose Input/Output (MP2). When in I²C master mode, this pin functions as an open collector output and drives a serial clock to slave devices on the I²C bus; use a 2.0 kΩ pull-up resistor to IOVDD on the line connected to this pin. When in SPI master mode, this pin drives the clock signal to slave devices on the SPI bus. Disconnect this pin when not in use.
29	SDA_M/ MISO_M/MP3	Pull-up; can be disabled by a write to control register	I²C Master Port Serial Data (SDA_M)/SPI Master Mode Data Input (MISO_M)/Multipurpose, General-Purpose Input/Output (MP3). When in I²C master mode, this pin functions as a bi-directional open collector data line between the I²C master port and slave devices on the I²C bus; use a 2.0 kΩ pull-up resistor to IOVDD on the line connected to this pin. When in SPI master mode, this pin receives data from slave devices on the SPI bus. Disconnect this pin when not in use.

Pin No.	Mnemonic	Internal Pull Resistor	Description
30	MISO/SDA	Pull-up; can be disabled by a write to control register	SPI Slave Data Output Port (MISO)/I²C Slave Serial Data Port (SDA). In SPI slave mode, this pin outputs data to the master device on the SPI bus. In I²C slave mode, this pin functions as a bidirectional open collector data line between the I²C slave port and the master device on the I²C bus; use a 2.0 kΩ pull-up resistor to IOVDD on the line connected to this pin. When this pin is not in use, connect it to IOVDD with a 10.0 kΩ pull-up resistor.
31	SCLK/SCL	Pull-up; can be disabled by a write to control register	SPI Slave Port Serial Clock (SCLK)/I²C Slave Port Serial Clock (SCL). In SPI slave mode, this pin receives the serial clock signal from the master device on the SPI bus. In I²C slave mode, this pin receives the serial clock signal from the master device on the I²C bus; use a 2.0 kΩ pull-up resistor to IOVDD on the line connected to this pin. When this pin is not in use, connect it to IOVDD with a 10.0 kΩ pull-up resistor.
32	MOSI/ADDR1	Pull-up; can be disabled by a write to control register	SPI Slave Port Data Input (MOSI)/I²C Slave Port Address MSB (ADDR1). In SPI slave mode, this pin receives a data signal from the master device on the SPI bus. In I²C slave mode, this pin acts as an input and sets the chip address of the I²C slave port, in conjunction with Pin 33 (SS/ADDR0).
33	SS/ADDR0	Pull-up, nominally 250 kΩ; can be disabled by a write to control register	SPI Slave Port Slave Select (SS)/I²C Slave Port Address LSB (ADDR0). In SPI slave mode, this pin receives the slave select signal from the master device on the SPI bus. In I²C slave mode, this pin acts as an input and sets the chip address of the I²C slave port in conjunction with Pin 32 (MOSI/ADDR1).
34	SELFBOOT	Pull-up	Self Boot Select. This pin allows the device to perform a self boot, in which it loads its random access memory (RAM) and register settings from an external EEPROM. Connecting Pin 34 to logic high (IOVDD) initiates a self boot operation the next time there is a rising edge on Pin 24 (RESET). When this pin is connected to ground, no self boot operation is initiated. This pin can be connected to IOVDD or to ground either directly or pulled up or down with a 1.0 kΩ or larger resistor.
35	DVDD	None	Digital Supply. Must be 1.2 V ± 5%. This pin can be supplied externally or by using the internal regulator and external pass transistor. Bypass this pin to Pin 36 (DGND) with decoupling capacitors. See the Power Supply Bypass Capacitors and Grounding sections.
36	DGND	None	Digital and I/O Ground Reference. Tie all DGND, AGND, and PGND pins directly together in a common ground plane. See the Power Supply Bypass Capacitors and Grounding sections.
37	DGND	None	Digital and I/O Ground Reference. Tie all DGND, AGND, and PGND pins directly together in a common ground plane. See the Power Supply Bypass Capacitors and Grounding sections.
38	IOVDD	None	Input/Output Supply, 1.8 V – 5% to 3.3 V + 10%. Bypass this pin with decoupling capacitors to Pin 37 (DGND). See the Power Supply Bypass Capacitors and Grounding sections.
39	LRCLK_OUT0/MP4	Configurable	Frame Clock, Serial Output Port 0 (LRCLK_OUT0)/Multipurpose, General-Purpose Input/Output (MP4). This pin is bidirectional, with the direction depending on whether Serial Output Port 0 is a master or slave. Disconnect this pin when not in use.
40	BCLK_OUT0	Configurable	Bit Clock, Serial Output Port 0. This pin is bidirectional, with the direction depending on whether the Serial Output Port 0 is a master or slave. Disconnect this pin when not in use.
41	SDATA_OUT0	Configurable	Serial Data Output Port 0 (Channel 0 to Channel 15). Capable of 2-channel, 4-channel, 8-channel, and 16-channel modes. Disconnect this pin when not in use.
42	LRCLK_OUT1/MP5	Configurable	Frame Clock, Serial Output Port 1 (LRCLK_OUT1)/Multipurpose, General-Purpose Input/Output (MP5). This pin is bidirectional, with the direction depending on whether Serial Output Port 1 is a master or slave. Disconnect this pin when not in use.
43	BCLK_OUT1	Configurable	Bit Clock, Serial Output Port 1. This pin is bidirectional, with the direction depending on whether Output Serial Port 1 is a master or slave. Disconnect this pin when not in use.
44	SDATA_OUT1	Configurable	Serial Data Output Port 1 (Channel 16 to Channel 31). Capable of 2-channel, 4-channel, 8-channel, and 16-channel modes. Disconnect this pin when not in use.
45	MP6	Configurable	Multipurpose, General-Purpose Input/Output 6. Disconnect this pin when not in use.
46	MP7	Configurable	Multipurpose, General-Purpose Input/Output 7. Disconnect this pin when not in use.
47	LRCLK_OUT2/MP8	Configurable	Frame Clock, Serial Output Port 2 (LRCLK_OUT2)/Multipurpose, General-Purpose Input/Output (MP8). This pin is bidirectional, with the direction depending on whether Serial Output Port 2 is a master or slave. Disconnect this pin when not in use.
48	BCLK_OUT2	Configurable	Bit Clock, Serial Output Port 2. This pin is bidirectional, with the direction depending on whether Serial Output Port 2 is a master or slave. Disconnect this pin when not in use.
49	SDATA_OUT2	Configurable	Serial Data Output Port 2 (Channel 32 to Channel 39). Capable of 2-channel, 4-channel, 8-channel, or flexible TDM mode. Disconnect this pin when not in use.
50	LRCLK_OUT3/MP9	Configurable	Frame Clock, Serial Output Port 3 (LRCLK_OUT3)/Multipurpose, General-Purpose Input/Output (MP9). This pin is bidirectional, with the direction depending on whether Serial Output Port 3 is a master or slave. Disconnect this pin when not in use.

Pin No.	Mnemonic	Internal Pull Resistor	Description
51	BCLK_OUT3	Configurable	Bit Clock, Serial Output Port 3. This pin is bidirectional, with the direction depending on whether Serial Output Port 3 is a master or slave. Disconnect this pin when not in use.
52	SDATA_OUT3	Configurable	Serial Data Output Port 3 (Channel 40 to Channel 47). Capable of 2-channel, 4-channel, 8-channel, and flexible TDM modes. Disconnect this pin when not in use.
53	DVDD	None	Digital Supply. Must be 1.2 V ± 5%. This pin can be supplied externally or by using the internal regulator and external pass transistor. Bypass Pin 53 with decoupling capacitors to Pin 54 (DGND). See the Power Supply Bypass Capacitors and Grounding sections.
54	DGND	None	Digital and I/O Ground Reference. Tie all DGND, AGND, and PGND pins directly together in a common ground plane. See the Power Supply Bypass Capacitors and Grounding sections.
55	DGND	None	Digital and I/O Ground Reference. Tie all DGND, AGND, and PGND pins directly together in a common ground plane. See the Power Supply Bypass Capacitors and Grounding sections.
56	IOVDD	None	Input/Output Supply, 1.8 V − 5% to 3.3 V + 10%. Bypass this pin with decoupling capacitors to Pin 55 (DGND). See the Power Supply Bypass Capacitors and Grounding sections.
57	BCLK_IN0	Configurable	Bit Clock, Serial Input Port 0. This pin is bidirectional, with the direction depending on whether Serial Input Port 0 is a master or slave. Disconnect this pin when not in use.
58	LRCLK_IN0/ MP10	Configurable	Frame Clock, Serial Input Port 0 (LRCLK_IN0)/Multipurpose, General-Purpose Input/Output (MP10). This pin is bidirectional, with the direction depending on whether Serial Input Port 0 is a master or slave. Disconnect this pin when not in use.
59	SDATA_IN0	Configurable	Serial Data Input Port 0 (Channel 0 to Channel 15). Capable of 2-channel, 4-channel, 8-channel, or 16-channel mode. Disconnect this pin when not in use.
60	BCLK_IN1	Configurable	Bit Clock, Serial Input Port 1. This pin is bidirectional, with the direction depending on whether the Serial Input Port 1 is a master or slave. Disconnect this pin when not in use.
61	LRCLK_IN1/ MP11	Configurable	Frame Clock, Serial Input Port 1 (LRCLK_IN1)/Multipurpose, General-Purpose Input/Output (MP11). This pin is bidirectional, with the direction depending on whether the Serial Input Port 1 is a master or slave. Disconnect this pin when not in use.
62	SDATA_IN1	Configurable	Serial Data Input Port 1 (Channels 16 to Channel 31). Capable of 2-channel, 4-channel, 8-channel, or 16-channel mode. Disconnect this pin when not in use.
63	THD_M	None	Thermal Diode Negative (−) Input. Connect this pin to the D− pin of an external temperature sensor IC. Disconnect this pin when not in use.
64	THD_P	None	Thermal Diode Positive (+) Input. Connect this pin to the D+ pin of an external temperature sensor IC. Disconnect this pin when not in use.
65	BCLK_IN2	Configurable	Bit Clock, Serial Input Port 2. This pin is bidirectional, with the direction depending on whether the Serial Input Port 2 is a master or slave. Disconnect this pin when not in use.
66	LRCLK_IN2/ MP12	Configurable	Frame Clock, Input Serial Port 2 (LRCLK_IN2)/Multipurpose, General-Purpose Input/Output (MP12). This pin is bidirectional, with the direction depending on whether Serial Input Port 2 is a master or slave. Disconnect this pin when not in use.
67	SDATA_IN2	Configurable	Serial Data Input Port 2 (Channel 32 to Channel 39). Capable of 2-channel, 4-channel, 8-channel, or flexible TDM mode. Disconnect this pin when not in use.
68	BCLK_IN3	Configurable	Bit Clock, Input Serial Port 3. This pin is bidirectional, with the direction depending on whether Input Serial Port 3 is a master or slave. Disconnect this pin when not in use.
69	LRCLK_IN3/ MP13	Configurable	Frame Clock, Serial Input Port 3 (LRCLK_IN3)/Multipurpose, General-Purpose Input/Output (MP13). This pin is bidirectional, with the direction depending on whether Serial Input Port 3 is a master or slave. Disconnect this pin when not in use.
70	SDATA_IN3	Configurable	Serial Data Input Port 3 (Channel 40 to Channel 47). Capable of 2-channel, 4-channel, 8-channel, or flexible TDM mode. Disconnect this pin when not in use.
71	DVDD	None	Digital Supply. Must be 1.2 V ± 5%. This pin can be supplied externally or by using the internal regulator and external pass transistor. Bypass with decoupling capacitors to Pin 72 (DGND).
72	DGND	None	Digital and I/O Ground Reference. Tie all DGND, AGND, and PGND pins directly together in a common ground plane. See the Power Supply Bypass Capacitors and Grounding sections.
EP	Exposed Pad	None	The exposed pad must be grounded by soldering it to a copper square of equivalent size on the PCB. Identical copper squares must exist on all layers of the board, connected by vias, and they must be connected to a dedicated copper ground layer within the PCB. See Exposed Pad PCB Design, Figure 87, and Figure 88.

THEORY OF OPERATION
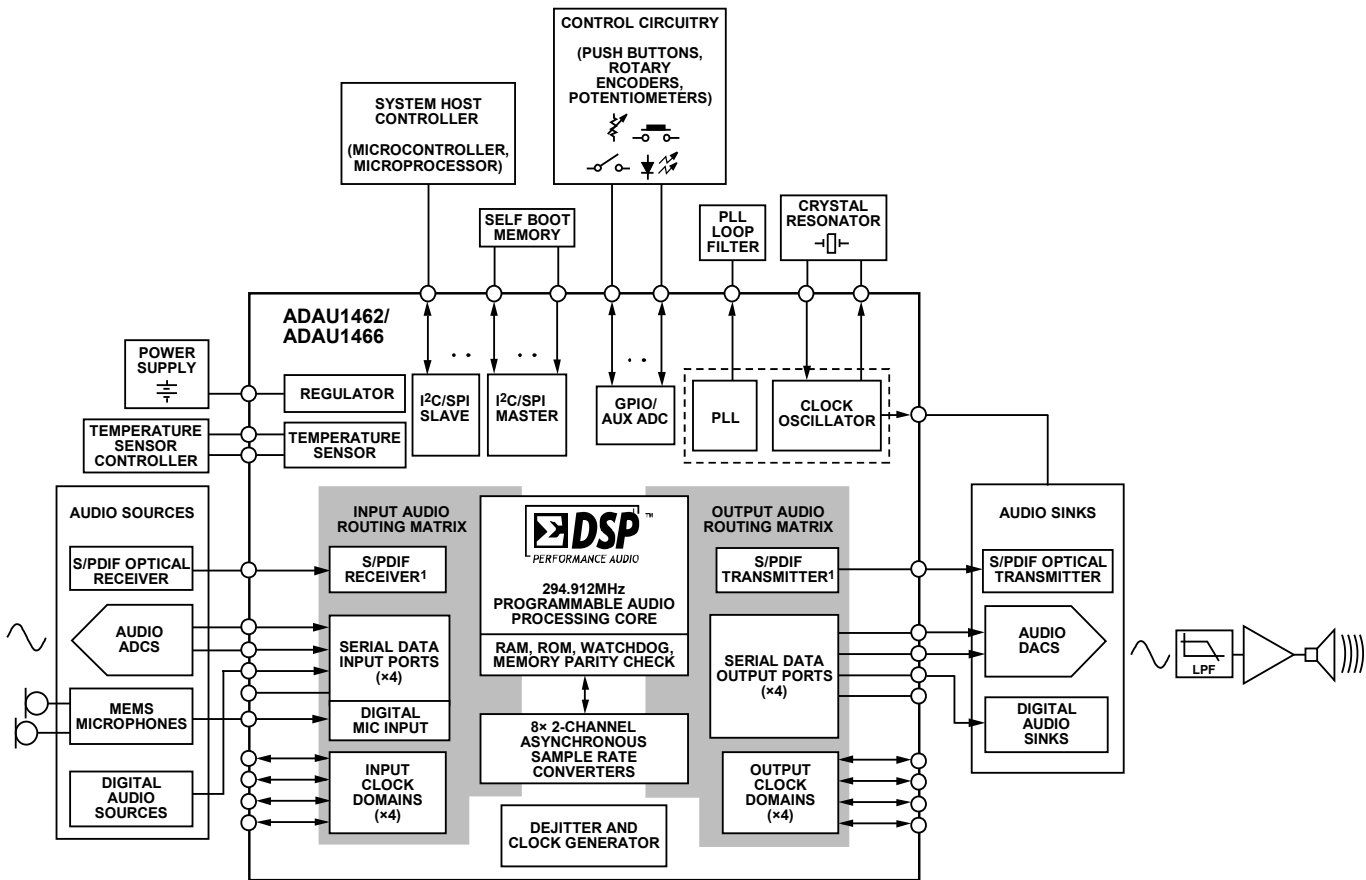## SYSTEM BLOCK DIAGRAM

Figure 12. System Block Diagram with Example Connections to External Components

OVERVIEW

The ADAU1462/ADAU1466 are enhanced audio processors with 48 channels of input and output. They include options for the hardware routing of audio signals between the various inputs, outputs, SigmaDSP core, and integrated sample rate converters. The SigmaDSP core features full 32-bit processing (that is, 64-bit processing in double precision mode) with an 80-bit arithmetic logic unit (ALU). By using a quadruple multiply accumulator (MAC) data path, the ADAU1462/ADAU1466 can execute more than 1.2 billion MAC operations per second, which allows processing power that far exceeds predecessors in the SigmaDSP family of products. The powerful DSP core can process over 3,000 double precision biquad filters or 24,000 FIR filter taps per sample at the standard 48 kHz audio sampling rate. Other features, including synchronous parameter loading for ensuring filter stability and 100% code efficiency with the [SigmaStudio](#) tools, reduce complexity in audio system development. The [SigmaStudio](#) library of audio processing algorithms allows system designers to compensate for real-world limitations of speakers, amplifiers, and listening environments, through speaker equalization, multiband compression, limiting, and third party branded algorithms.

The input audio routing matrix and output audio routing matrix allow the user to multiplex inputs from multiple sources that are running at various sample rates to or from the SigmaDSP core, and then to pass them on to the desired hardware outputs. This multiplexing drastically reduces the complexity of signal routing and clocking issues in the audio system. The audio subsystem includes eight stereo ASRCs, S/PDIF input and output, and serial audio data ports supporting 2 to 16 channels in formats such as I²S and time division multiplexing (TDM). Any of the inputs can be routed to the SigmaDSP core or to any of the ASRCs. Similarly, the output signals can be taken from the SigmaDSP core, any of the ASRC outputs, the serial inputs, the PDM microphones, or the S/PDIF receiver. This routing scheme, which can be modified at any time using control registers, allows maximum system flexibility without requiring hardware design changes.

Two serial input ports and two serial output ports can operate as pairs in a special flexible TDM mode, allowing the user to assign byte specific locations independently to audio streams at varying bit depths. This mode ensures compatibility with codecs that use similar flexible TDM streams.

The DSP core is optimized for audio processing, and it can process audio at sample rates of up to 192 kHz. The program and parameter/data RAMs can be loaded with a custom audio processing signal flow built with the SigmaStudio graphical programming software from Analog Devices, Inc., which is available for download at www.analog.com. The values that are stored in the parameter RAM can control individual signal processing blocks, such as infinite impulse response (IIR) and finite impulse response (FIR) equalization filters, dynamics processors, audio delays, and mixer levels. A software safeload feature allows transparent parameter updates and prevents clicks on the output signals.

Reliability features, such as memory parity checking and a program counter watchdog, help ensure that the system can detect and recover from any errors related to memory corruption.

On the ADAU1462/ADAU1466, the audio data in an S/PDIF stream can be routed through an ASRC for processing in the DSP or can be sent directly to a serial audio output. Other components of the stream, including status and user bits, are not lost and can be used in algorithm or output on the MPx pins. The user can also independently program the nonaudio data that is embedded in the output signal of the S/PDIF transmitter.

The 14 MPx pins are available to provide a simple user interface without the need for an external microcontroller. These multi-purpose pins are available to input external control signals and output flags or controls to other devices in the system. As inputs, the MPx pins can be connected to push buttons, switches, rotary encoders, or other external control circuitry to control the internal signal processing program. When configured as outputs, these pins can drive LEDs (with a buffer), output flags to a microcontroller, control other ICs, or connect to other external circuitry in an application. In addition to the multipurpose pins, six dedicated input pins (AUXADC5 to AUXADC0) are connected to an auxiliary ADC for use with analog controls such as potentiometers or system voltages.

The SigmaStudio software programs and controls the device through the control port. In addition to designing and tuning a signal flow, the software can configure all of the DSP registers in real time and download a new program and parameters into the external self boot EEPROM. The SigmaStudio graphical interface allows anyone with audio processing knowledge to design a DSP signal flow and export production quality code without the need for writing text code. The software provides enough flexibility and programmability to allow an experienced DSP programmer to have in-depth control of the design.

Algorithms are created in SigmaStudio by dragging and dropping signal processing cells from the library, connecting them together in a flow, compiling the design, and downloading the executable program and parameters to the SigmaDSP memory through the control port. The tasks of linking, compiling, and downloading the project are all handled automatically by the software.

The signal processing cells included in the library range from primitive operations, such as addition and gain, to large and highly optimized building blocks. For example, the libraries include the following:

- Single and double precision biquad filter
- Monochannel and multichannel dynamics processors with peak or rms detection
- Mixer and splitter
- Tone and noise generator
- Fixed and variable gain
- Loudness
- Delay
- Stereo enhancement
- Dynamic bass boost
- Noise and tone source
- Level detector
- MPx pin control and conditioning
- FFT and frequency domain processing algorithms

Analog Devices continuously develops new processing algorithms and provides proprietary and third party algorithms for applications such as matrix decoding, bass enhancement, and surround virtualizers.

Several power saving mechanisms are available, including programmable pad strength for digital I/O pins and the ability to power down unused subsystems.

Fabricated on a single monolithic integrated circuit for operation over the −40°C to +105°C temperature range, the device is housed in a 72-lead LFCSP package with an exposed pad to assist in heat dissipation.

The device can be controlled in one of two operational modes, as follows:

- The settings of the chip can be loaded and dynamically updated through the SPI/I²C port via SigmaStudio or a processor in the system.
- The DSP can self boot from an external EEPROM in a system with no microcontroller.

INITIALIZATION

Power-Up Sequence

The first step in the initialization sequence is to power up the device. First, apply voltage to the power pins. All the power pins can be supplied simultaneously. If the power pins are not supplied simultaneously, supply IOVDD first because the internal ESD protection diodes are referenced to the IOVDD voltage. AVDD, DVDD, and PVDD can be supplied at the same time as IOVDD or after, but they must not be supplied prior to IOVDD. The order in which AVDD, DVDD, and PVDD are supplied does not matter.

DVDD, the power supply for the internal digital logic, can be regulated and supplied directly or it can by generated from IOVDD using an internal voltage regulator. When the internal regulator is not used and DVDD is directly supplied, no special sequence is required when providing the proper voltages to AVDD, DVDD, and PVDD.

When the internal regulator is used, DVDD is derived from IOVDD in combination with an external pass transistor, after AVDD, IOVDD, and PVDD are supplied. See the Power Supplies section for more information.

Each power supply domain has its own internal power-on reset (POR) circuits (also known as power OK circuits) to ensure that the level shifters attached to each power domain can be initialized properly. AVDD and PVDD must reach their nominal level before the auxiliary ADC and PLL can be used, respectively.

However, the AVDD and PVDD supplies have no role in the rest of the power-up sequence. After the AVDD power reaches its nominal threshold, the regulator becomes active and begins to charge up the DVDD supply. The DVDD supply also has a POR circuit to ensure that the level shifters initialize during power-up.

The POR signals are combined into three global level shifter resets that properly initialize the signal crossings between each separate power domain and DVDD.

The digital circuits remain in reset until the IOVDD to DVDD level shifter reset is released. At that point, the digital circuits exit reset.

When a crystal is in use, the crystal oscillator circuit must provide a stable master clock to the XTALIN/MCLK pin by the time the PVDD supply reaches its nominal level. The XTALIN/MCLK pin is restricted from passing into the PLL circuitry until the DVDD POR signal becomes active and the PVDD to DVDD level shifter is initialized.

When all four POR circuits signal that the power-on conditions are met, a reset synchronizer circuit releases the internal digital circuitry from reset, provided that the following conditions are met:

- A valid MCLK signal is provided to the digital circuitry and the PLL.
- The $\overline{\text{RESET}}$ pin is high.

When the internal digital circuitry becomes active, the DSP core runs eight lines of initialization code stored in read-only memory (ROM), requiring eight cycles of the MCLK signal. For a 12.288 MHz MCLK input, this process takes 650 ns.
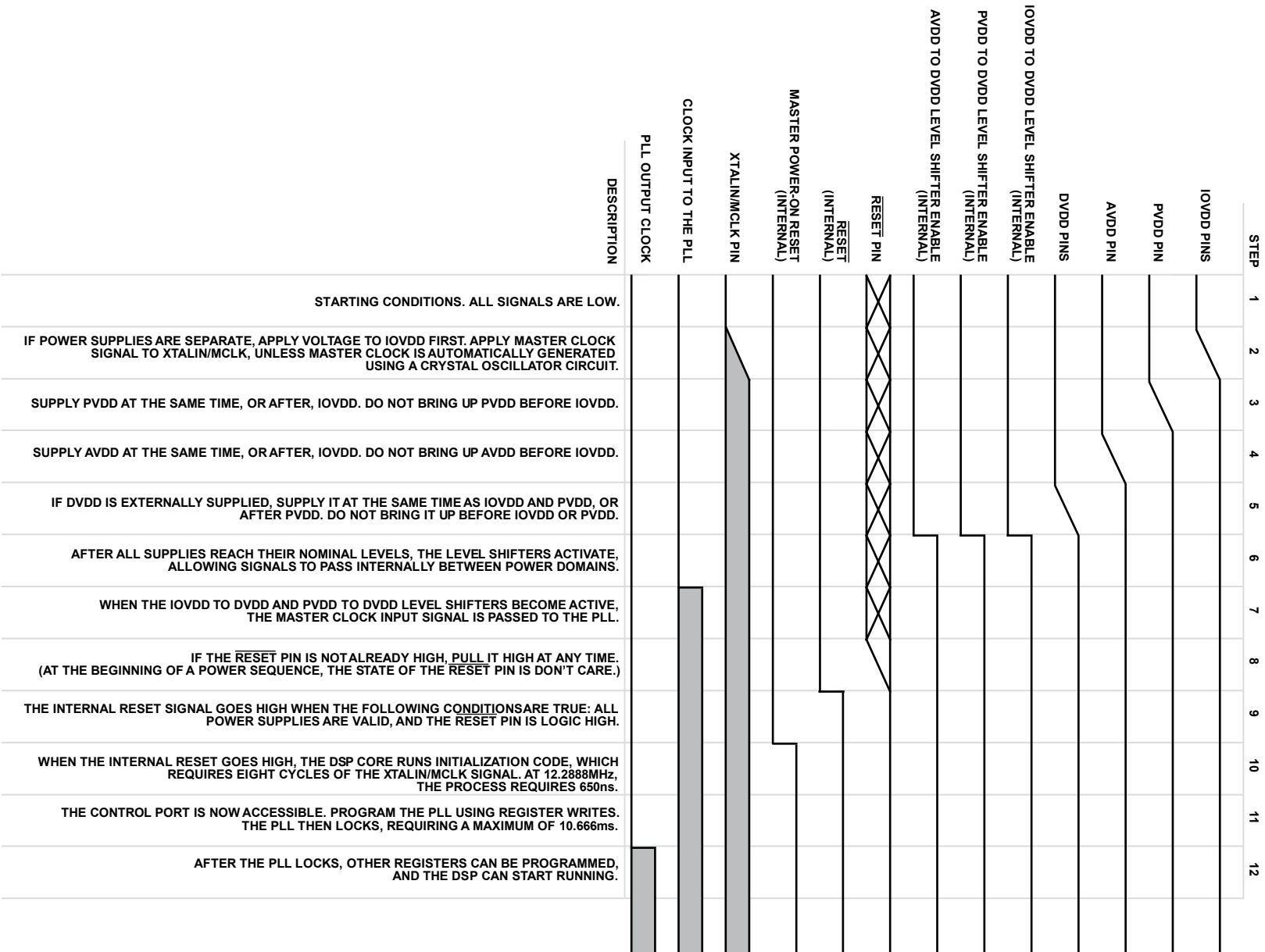
After the ROM program completes its execution, the PLL is ready to be configured using register writes to Register 0xF000 (PLL_CTRL0), Register 0xF001 (PLL_CTRL1), Register 0xF002 (PLL_CLK_SRC), and Register 0xF003 (PLL_ENABLE).

When the PLL is configured and enabled, the PLL starts to lock to the incoming master clock signal. The absolute maximum PLL lock time is $32 \times 1024 = 32{,}768$ clock cycles on the clock signal (after the input prescaler), which is fed to the input of the PLL. In a standard 48 kHz use case, the PLL input clock frequency after the prescaler is 3.072 MHz; therefore, the maximum PLL lock time is 10.666 ms.

Typically, the PLL locks much faster than 10.666 ms. In most systems, the PLL locks within about 3.5 ms. The PLL_LOCK register (Address 0xF004) can be polled via the control port until Bit 0 (PLL_LOCK) goes high, signifying that the PLL lock is complete.

While the PLL is attempting to lock to the input clock, the I²C slave and SPI slave control ports are inactive; therefore, no other registers are accessible over the control port. While the PLL is attempting to lock, all attempts to write to the control port fail.

Figure 13 shows an example power-up sequence with all relevant signals labeled. If possible, apply the required voltage to all four power supply domains (IOVDD, AVDD, PVDD, and DVDD) simultaneously. If the power supplies are separate, IOVDD, which is the reference for the ESD protection diodes that are situated inside the input and output pins, must be applied first to avoid stressing these diodes. PVDD, AVDD, and DVDD can then be supplied in any order (see the System Initialization Sequence section for more information). Note that the gray areas in Figure 13 represent clock signals.

STEP	DESCRIPTION
1	STARTING CONDITIONS. ALL SIGNALS ARE LOW.
2	IF POWER SUPPLIES ARE SEPARATE, APPLY VOLTAGE TO IOVDD FIRST. APPLY MASTER CLOCK SIGNAL TO XTALIN/MCLK, UNLESS MASTER CLOCK IS AUTOMATICALLY GENERATED USING A CRYSTAL OSCILLATOR CIRCUIT.
3	SUPPLY PVDD AT THE SAME TIME, OR AFTER, IOVDD. DO NOT BRING UP PVDD BEFORE IOVDD.
4	SUPPLY AVDD AT THE SAME TIME, OR AFTER, IOVDD. DO NOT BRING UP AVDD BEFORE IOVDD.
5	IF DVDD IS EXTERNALLY SUPPLIED, SUPPLY IT AT THE SAME TIME AS IOVDD AND PVDD, OR AFTER PVDD. DO NOT BRING IT UP BEFORE IOVDD OR PVDD.
6	AFTER ALL SUPPLIES REACH THEIR NOMINAL LEVELS, THE LEVEL SHIFTERS ACTIVATE, ALLOWING SIGNALS TO PASS INTERNALLY BETWEEN POWER DOMAINS.
7	WHEN THE IOVDD TO DVDD AND PVDD TO DVDD LEVEL SHIFTERS BECOME ACTIVE, THE MASTER CLOCK INPUT SIGNAL IS PASSED TO THE PLL.
8	IF THE RESET PIN IS NOT ALREADY HIGH, PULL IT HIGH AT ANY TIME. (AT THE BEGINNING OF A POWER SEQUENCE, THE STATE OF THE RESET PIN IS DON'T CARE.)
9	THE INTERNAL RESET SIGNAL GOES HIGH WHEN THE FOLLOWING CONDITIONS ARE TRUE: ALL POWER SUPPLIES ARE VALID, AND THE RESET PIN IS LOGIC HIGH.
10	WHEN THE INTERNAL RESET GOES HIGH, THE DSP CORE RUNS INITIALIZATION CODE, WHICH REQUIRES EIGHT CYCLES OF THE XTALIN/MCLK SIGNAL. AT 12.2888MHz, THE PROCESS REQUIRES 650ns.
11	THE CONTROL PORT IS NOW ACCESSIBLE. PROGRAM THE PLL USING REGISTER WRITES. THE PLL THEN LOCKS, REQUIRING A MAXIMUM OF 10.666ms.
12	AFTER THE PLL LOCKS, OTHER REGISTERS CAN BE PROGRAMMED, AND THE DSP CAN START RUNNING.

Figure 13. Power Sequencing and POR Timing Diagram for a System with Separate Power Supplies

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