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FEATURES

- 28-/56-bit, 50 MIPS digital audio processor
- 2 ADCs: SNR of 100 dB, THD + N of -83 dB
- 4 DACs: SNR of 104 dB, THD + N of -90 dB
- Complete standalone operation
- Self-boot from serial EEPROM
- Auxiliary ADC with 4-input mux for analog control
- GPIOs for digital controls and outputs
- Fully programmable with SigmaStudio graphical tool
- 28-bit × 28-bit multiplier with 56-bit accumulator for full double-precision processing
- Clock oscillator for generating a master clock from crystal
- PLL for generating master clock from $64 \times f_s$, $256 \times f_s$, $384 \times f_s$, or $512 \times f_s$ clocks
- Flexible serial data input/output ports with I²S-compatible, left-justified, right-justified, and TDM modes
- Sampling rates of up to 192 kHz are supported
- On-chip voltage regulator for compatibility with 3.3 V systems
- 48-lead, plastic LQFP

APPLICATIONS

- Multimedia speaker systems
- MP3 player speaker docks
- Automotive head units
- Minicomponent stereos
- Digital televisions
- Studio monitors
- Speaker crossovers
- Musical instrument effects processors
- In-seat sound systems (aircraft/motor coaches)

GENERAL DESCRIPTION

The ADAU1701 is a complete single-chip audio system with a 28-/56-bit audio DSP, ADCs, DACs, and microcontroller-like control interfaces. Signal processing includes equalization, cross-over, bass enhancement, multiband dynamics processing, delay compensation, speaker compensation, and stereo image widening. This processing can be used to compensate for real-world limitations of speakers, amplifiers, and listening environments, providing dramatic improvements in perceived audio quality.

Its signal processing is comparable to that found in high end studio equipment. Most processing is done in full 56-bit, double precision mode, resulting in very good low level signal performance. The ADAU1701 is a fully programmable DSP. The easy to use SigmaStudio™ software allows the user to graphically configure a custom signal processing flow using blocks such as biquad filters, dynamics processors, level controls, and GPIO interface controls.

ADAU1701 programs can be loaded on power-up either from a serial EEPROM through its own self-boot mechanism or from an external microcontroller. On power-down, the current state of the parameters can be written back to the EEPROM from the ADAU1701 to be recalled the next time the program is run.

Two Σ - Δ ADCs and four Σ - Δ DACs provide a 98.5 dB analog input to analog output dynamic. Each ADC has a THD + N of -83 dB, and each DAC has a THD + N of -90 dB. Digital input and output ports allow a glueless connection to additional ADCs and DACs. The ADAU1701 communicates through an I²C® bus or a 4-wire SPI port.

ADAU1701* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADAU1701 Evaluation Board
- ADUSB2EBZ Evaluation Board

DOCUMENTATION

Application Notes

- AN-1006: Using the EVAL-ADUSB2EBZ
- AN-923: Designing a System Using the ADAU1701/ADAU1702 in Self-Boot Mode
- AN-951: Using Hardware Controls with SigmaDSP GPIO Pins

Data Sheet

- ADAU1701: SigmaDSP 28-/56-Bit Audio Processor with Two ADCs and Four DACs Data Sheet

User Guides

- UG-072: Evaluation Board User Guide for ADAU1401

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADAU1701 Sound Audio System Linux Driver
- Firmware Loader for SigmaDSPs

TOOLS AND SIMULATIONS

- SigmaDSP Processors: Software and Tools

REFERENCE DESIGNS

- CN0162

DESIGN RESOURCES

- ADAU1701 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADAU1701 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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REVISION HISTORY

5/16—Rev. B to Rev. C

Changes to Audio DACs Section and Figure 1921

6/11—Rev. A to Rev. B

Deleted Table 2; Renumbered Sequentially6

Changes to Table 46

2/11—Rev. 0 to Rev. A

Moved Figure 14

Changes to Specifications Section.....5

Changes to Table 8, Test Conditions/Comments Column8

Reordered Figures in Digital Timing Diagrams Section9

Changes to Figure 2.....9

Changes to Figure 5 and Figure 6 10

Changes to Table 11 12

Replaced Figure 8 to Figure 11 15

Renamed Theory of Operation Section 17

Changes to Initialization Section 18

Change to Setting the Master Clock/PLL Mode Section 19

Changes to Table 15 23

Replaced Figure 22 through Figure 25 26

Changes to EEPROM Format Section..... 28

Deleted Table 20, Renumbered Sequentially 29

Inserted Figure 28, Renumbered Sequentially 29

Changes to Control Register Details Section 35

Changes to Ordering Guide..... 53

7/07—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

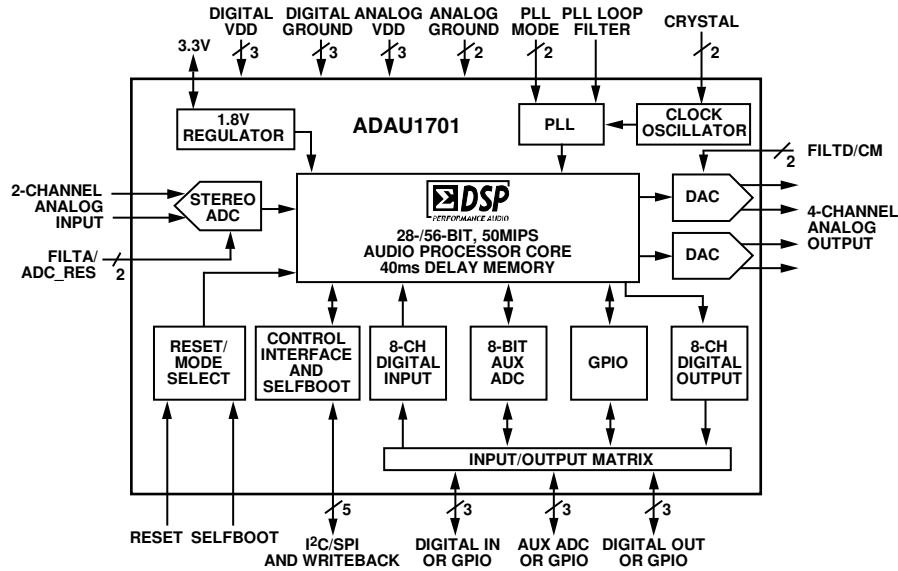


Figure 1.

06412-001

SPECIFICATIONS

AVDD = 3.3 V, DVDD = 1.8 V, PVDD = 3.3 V, IOVDD = 3.3 V, master clock input = 12.288 MHz, unless otherwise noted.

ANALOG PERFORMANCE

Specifications are guaranteed at 25°C (ambient).

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC INPUTS					
Number of Channels		2			Stereo input
Resolution		24		Bits	
Full-Scale Input		100 (283)		μA rms (μA p-p)	2 V rms input with 20 kΩ (18 kΩ external + 2 kΩ internal) series resistor
Signal-to-Noise Ratio					
A-Weighted		100		dB	
Dynamic Range					–60 dB with respect to full-scale analog input
A-Weighted	95	100		dB	
Total Harmonic Distortion + Noise		–83		dB	–3 dB with respect to full-scale analog input
Interchannel Gain Mismatch		25	250	mdB	
Crosstalk		–82		dB	Analog channel-to-channel crosstalk
DC Bias	1.4	1.5	1.6	V	
Gain Error	–11		+11	%	
DAC OUTPUTS					
Number of Channels		4			Two stereo output channels
Resolution		24		Bits	
Full-Scale Analog Output		0.9 (2.5)		V rms (V p-p)	
Signal-to-Noise Ratio					
A-Weighted		104		dB	
Dynamic Range					–60 dB with respect to full-scale analog output
A-Weighted	99	104		dB	
Total Harmonic Distortion + Noise		–90		dB	–1 dB with respect to full-scale analog output
Crosstalk		–100		dB	Analog channel-to-channel crosstalk
Interchannel Gain Mismatch		25	250	mdB	
Gain Error	–10		+10	%	
DC Bias	1.4	1.5	1.6	V	
VOLTAGE REFERENCE					
Absolute Voltage (CM)	1.4	1.5	1.6	V	
AUXILIARY ADC					
Full-Scale Analog Input	2.8	3.0	3.1	V	
INL		0.5		LSB	
DNL		1.0		LSB	
Offset		15		mV	
Input Impedance	17.8	30	42	kΩ	

DIGITAL INPUT/OUTPUT

Table 2.

Parameter	Symbol	Min	Typ	Max ¹	Unit	Test Conditions/Comments
Input Voltage, High	V _{IH}	2.0		IOVDD	V	
Input Voltage, Low	V _{IL}			0.8	V	
Input Leakage, High	I _{IH}			1	μA	Excluding MCLKI
Input Leakage, Low	I _{IL}			1	μA	Excluding MCLKI and bidirectional pins
Bidirectional Pin Pull-Up Current, Low				150	μA	
MCLKI Input Leakage, High	I _{IH}			3	μA	
MCLKI Input Leakage, Low	I _{IL}			3	μA	
High Level Output Voltage	V _{OH}	2.0			V	I _{OH} = 2 mA
Low Level Output Voltage	V _{OL}			0.8	V	I _{OL} = 2 mA
Input Capacitance				5	pF	
GPIO Output Drive			2		mA	

¹ Maximum specifications are measured across a temperature range of -40°C to +130°C (case), a DVDD range of 1.62 V to 1.98 V, and an AVDD range of 2.97 V to 3.63 V.

POWER

Table 3.

Parameter	Min	Typ	Max ¹	Unit
SUPPLY VOLTAGE				
Analog Voltage		3.3		V
Digital Voltage		1.8		V
PLL Voltage		3.3		V
IOVDD Voltage		3.3		V
SUPPLY CURRENT				
Analog Current (AVDD and PVDD)		50	85	mA
Digital Current (DVDD)		40	60	mA
Analog Current, Reset		35	55	mA
Digital Current, Reset		1.5	4.5	mA
DISSIPATION				
Operation (AVDD, DVDD, PVDD) ²		286.5		mW
Reset, All Supplies		118		mW
POWER SUPPLY REJECTION RATIO (PSRR)				
1 kHz, 200 mV p-p Signal at AVDD		50		dB

¹ Maximum specifications are measured across a temperature range of -40°C to +130°C (case), a DVDD range of 1.62 V to 1.98 V, and an AVDD range of 2.97 V to 3.63 V.

² Power dissipation does not include IOVDD power because the current drawn from this supply is dependent on the loads at the digital output pins.

TEMPERATURE RANGE

Table 4.

Parameter	Min	Typ	Max	Unit
Functionality Guaranteed	0		70	°C ambient

PLL AND OSCILLATOR

Table 5. PLL and Oscillator¹

Parameter	Min	Typ	Max	Unit
PLL Operating Range	MCLK_Nom - 20%		MCLK_Nom + 20%	MHz
PLL Lock Time			20	ms
Crystal Oscillator Transconductance (g _m)		78		mmho

¹ Maximum specifications are measured across a temperature range of -40°C to +130°C (case), a DVDD range of 1.62 V to 1.98 V, and an AVDD range of 2.97 V to 3.63 V.

REGULATOR**Table 6. Regulator¹**

Parameter	Min	Typ	Max	Unit
DVDD Voltage	1.7	1.8	1.84	V

¹ Regulator specifications are calculated using a Zetex Semiconductors FZT953 transistor in the circuit.

DIGITAL TIMING SPECIFICATIONS**Table 7. Digital Timing¹**

Parameter	Limit		Unit	Test Conditions/Comments
	t _{MIN}	t _{MAX}		
MASTER CLOCK				
t _{MP}	36	244	ns	MCLKI period, 512 × f _s mode
	48	366	ns	MCLKI period, 384 × f _s mode
	73	488	ns	MCLKI period, 256 × f _s mode
	291	1953	ns	MCLKI period, 64 × f _s mode
SERIAL PORT				
t _{BIL}	40		ns	INPUT_BCLK (Pin 9) low pulse width
t _{BIH}	40		ns	INPUT_BCLK (Pin 9) high pulse width
t _{LIS}	10		ns	INPUT_LRCLK (Pin 8) setup; time to INPUT_BCLK rising
t _{LIH}	10		ns	INPUT_LRCLK (Pin 8) hold; time from INPUT_BCLK rising
t _{SIS}	10		ns	SDATA_INx (Pin 10, Pin 11, Pin 28, or Pin 29) setup; time to INPUT_BCLK (Pin 9) rising
t _{SIH}	10		ns	SDATA_INx (Pin 10, Pin 11, Pin 28, or Pin 29) hold; time from INPUT_BCLK (Pin 9) rising
t _{LOS}	10		ns	OUTPUT_LRCLK (Pin 16) setup in slave mode
t _{LOH}	10		ns	OUTPUT_LRCLK (Pin 16) hold in slave mode
t _{TS}		5	ns	OUTPUT_BCLK (Pin 11) falling to OUTPUT_LRCLK (Pin 16) timing skew
t _{SODS}		40	ns	SDATA_OUTx (Pin 14, Pin 15, Pin 26, or Pin 27) delay in slave mode; time from OUTPUT_BCLK (Pin 11) falling
t _{SODM}		40	ns	SDATA_OUTx (Pin 14, Pin 15, Pin 26, or Pin 27) delay in master mode; time from OUTPUT_BCLK (Pin 11) falling
SPI PORT				
f _{CCLK}		6.25	MHz	CCLK (Pin 23) frequency
t _{CCPL}	80		ns	CCLK (Pin 23) pulse width low
t _{CCPH}	80		ns	CCLK (Pin 23) pulse width high
t _{CLS}	0		ns	CLATCH (Pin 21) setup; time to CCLK (Pin 23) rising
t _{CLH}	100		ns	CLATCH (Pin 21) hold; time from CCLK (Pin 23) rising
t _{CLPH}	80		ns	CLATCH (Pin 21) pulse width high
t _{CDS}	0		ns	CDATA (Pin 20) setup; time to CCLK (Pin 23) rising
t _{CDH}	80		ns	CDATA (Pin 20) hold; time from CCLK (Pin 23) rising
t _{COD}		101	ns	COUT (Pin 22) delay; time from CCLK (Pin 23) falling
I ² C PORT				
f _{SCL}		400	kHz	SCL (Pin 23) frequency
t _{SCLH}	0.6		μs	SCL (Pin 23) high
t _{SCLL}	1.3		μs	SCL (Pin 23) low
t _{SCS}	0.6		μs	Setup time, relevant for repeated start condition
t _{SCH}	0.6		μs	Hold time; after this period, the first clock is generated
t _{DS}	100		ns	Data setup time
t _{SCR}		300	ns	SCL (Pin 23) rise time
t _{SCF}		300	ns	SCL (Pin 23) fall time
t _{SDR}		300	ns	SDA (Pin 22) rise time
t _{SDF}		300	ns	SDA (Pin 22) fall time
t _{BFT}	0.6			Bus-free time; time between stop and start

Parameter	Limit		Unit	Test Conditions/Comments
	t _{MIN}	t _{MAX}		
MULTIPURPOSE PINS AND RESET				
t _{GRT}		50	ns	GPIO (MPx pins) rise time
t _{GFT}		50	ns	GPIO (MPx pins) fall time
t _{GIL}		1.5 × 1/f _s	μs	GPIO (MPx pins) input latency; time until high/low value is read by core
t _{RLPW}	20		ns	RESET low pulse width

¹ All timing specifications are given for the default (I²S) states of the serial input port and the serial output port (see Table 65).

Digital Timing Diagrams

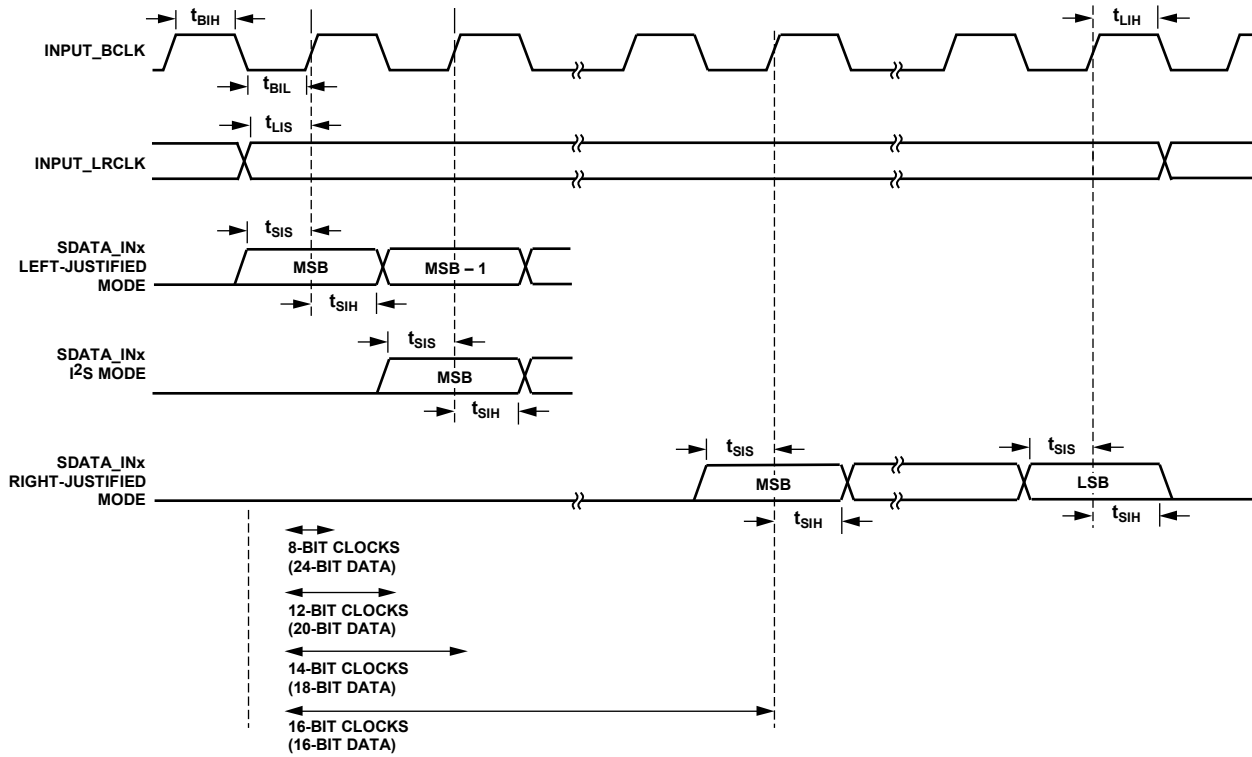


Figure 2. Serial Input Port Timing

06412-002

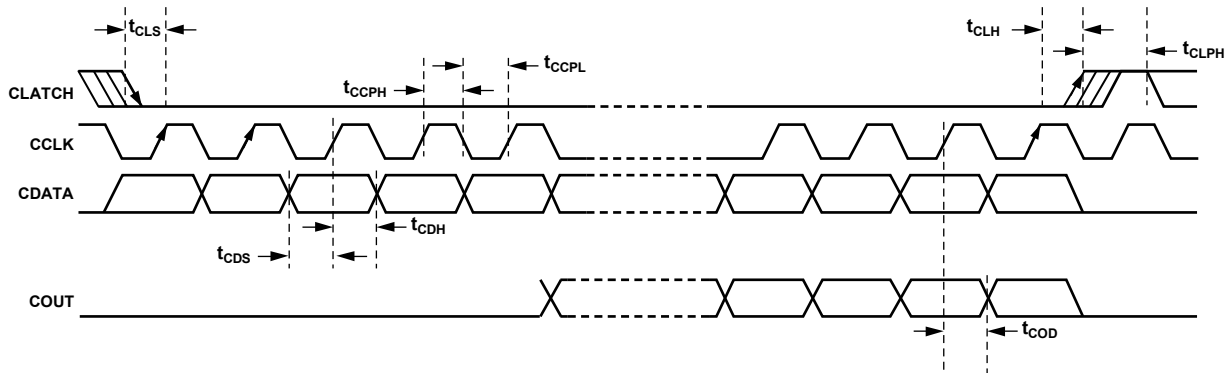


Figure 3. SPI Port Timing

06412-004

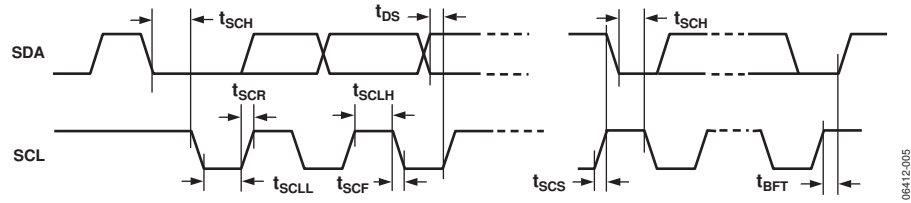


Figure 4. I²C Port Timing

06412-005

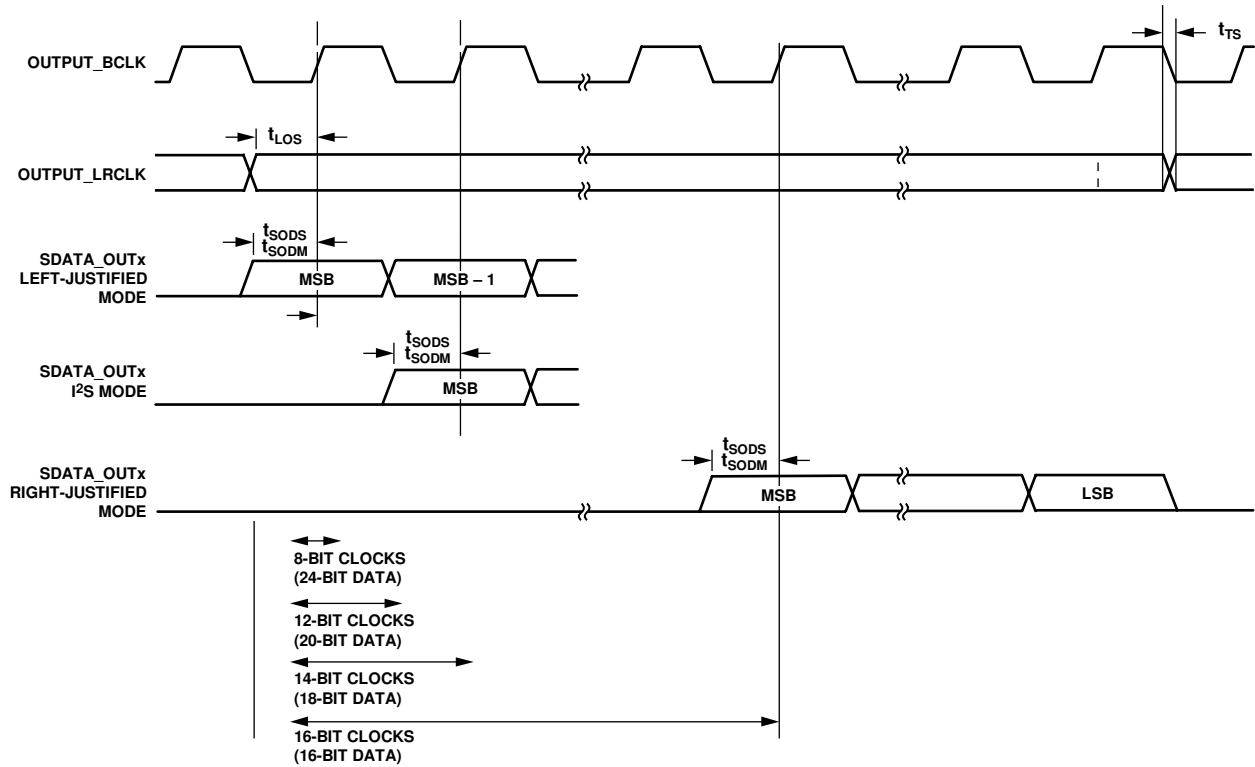


Figure 5. Serial Output Port Timing

06412-003

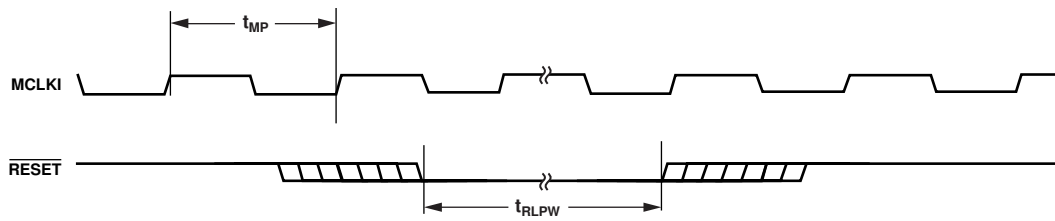


Figure 6. Master Clock and RESET Timing

06412-005

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
DVDD to GND	0 V to 2.2 V
AVDD to GND	0 V to 4.0 V
IOVDD to GND	0 V to 4.0 V
Digital Inputs	DGND – 0.3 V, IOVDD + 0.3 V
Maximum Junction Temperature	135°C
Temperature Range	
Storage	–65°C to +150°C
Operating	0°C to +70°C
Soldering (10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 9. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
48-Lead LQFP	72	19.5	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

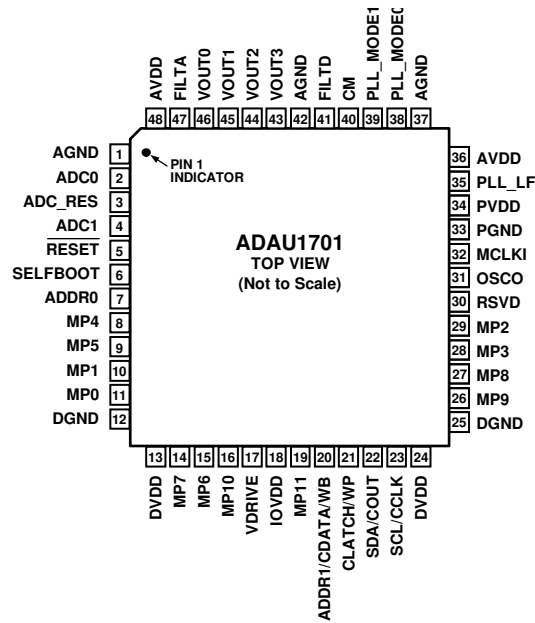


Figure 7. 48-Lead LQFP Pin Configuration

06412.007

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Type ¹	Description
1, 37, 42	AGND	PWR	Analog Ground Pin. The AGND, DGND, and PGND pins can be tied directly together in a common ground plane. Decouple AGND to an AVDD pin with a 100 nF capacitor.
2	ADC0	A_IN	Analog Audio Input 0. Full-scale 100 μ A rms input. Current input allows input voltage level to be scaled with an external resistor. An 18 k Ω resistor gives a 2 V rms full-scale input. See the Audio ADCs section for details.
3	ADC_RES	A_IN	ADC Reference Current. Set the full-scale current of the ADCs with an external 18 k Ω resistor connected between this pin and ground. See the Audio ADCs section for details.
4	ADC1	A_IN	Analog Audio Input 1. Full-scale 100 μ A rms input. Current input allows the input voltage level to be scaled with an external resistor. An 18 k Ω resistor gives a 2 V rms full-scale input.
5	RESET	D_IN	Active Low Reset Input. Reset is triggered on a high-to-low edge, and the ADAU1701 exits reset on a low-to-high edge. For more information about initialization, see the Power-Up Sequence section for details.
6	SELFBOOT	D_IN	Enable/Disable Self-Boot. SELFBOOT selects control port (low) or self-boot (high). Setting this pin high initiates a self-boot operation when the ADAU1701 is brought out of a reset. This pin can be tied directly to the control voltage or pulled up/down with a resistor. See the Self-Boot section for details.
7	ADDR0	D_IN	I ² C and SPI Address 0. In combination with ADDR1 function on Pin 20, this pin allows up to four ADAU1701 devices to be used on the same I ² C bus and up to two ICs to be used with a common SPI CLATCH signal. See the I ² C Port section for details.
8	MP4	D_IO	Multipurpose GPIO or Serial Input Port LRCLK (INPUT_LRCLK). See the Multipurpose Pins section for more details.
9	MP5	D_IO	Multipurpose GPIO or Serial Input Port BCLK (INPUT_BCLK). See the Multipurpose Pins section for more details.
10	MP1	D_IO	Multipurpose GPIO or Serial Input Port Data 1 (SDATA_IN0). See the Multipurpose Pins section for more details.
11	MP0	D_IO	Multipurpose GPIO or Serial Input Port Data 0 (SDATA_IN1). See the Multipurpose Pins section for more details.
12, 25	DGND	PWR	Digital Ground Pin. The AGND, DGND, and PGND pins can be tied directly together in a common ground plane. Decouple DGND to a DVDD pin with a 100 nF capacitor.
13, 24	DVDD	PWR	1.8 V Digital Supply. This can be supplied either externally or generated from a 3.3 V supply with the on-board 1.8 V regulator. Decouple DVDD to DGND with a 100 nF capacitor.

Pin No.	Mnemonic	Type ¹	Description
14	MP7	D_IO	Multipurpose GPIO or Serial Output Port Data 1 (SDATA_OUT1). See the Multipurpose Pins section for more details.
15	MP6	D_IO	Multipurpose GPIO, Serial Output Port Data 0, or TDM Data Output (SDATA_OUT0). See the Multipurpose Pins section for more details.
16	MP10	D_IO	Multipurpose GPIO or Serial Output Port LRCLK (OUTPUT_LRCLK). See the Multipurpose Pins section for more details.
17	VDRIVE	A_OUT	Drive for 1.8 V Regulator. The base of the voltage regulator external PNP transistor is driven from VDRIVE. See the Voltage Regulator section for details.
18	IOVDD	PWR	Supply for Input and Output Pins. The voltage on this pin sets the highest input voltage that should be seen on the digital input pins. This pin is also the supply for the digital output signals on the control port and MP pins. Always set IOVDD to 3.3 V. The current draw of this pin is variable because it is dependent on the loads of the digital outputs.
19	MP11	D_IO	Multipurpose GPIO or Serial Output Port BCLK (OUTPUT_BCLK). See the Multipurpose Pins section for more details.
20	ADDR1/CDATA/WB	D_IN	I ² C Address 1/SPI Data Input/EEPROM Write Back Trigger. This is a multifunction pin as follows: ADDR1: I ² C Address 1. In combination with ADDR0, this sets the I ² C address of the IC so that four ADAU1701 devices can be used on the same I ² C bus. See the I ² C Port section for details. CDATA: SPI Data Input. See the SPI Port section for details. WB: EEPROM Writeback Trigger. A rising (default) or falling (if set in the EEPROM messages) edge on this pin triggers a writeback of the interface registers to the external EEPROM. This function can be used to save parameter data on power-down. See the Self-Boot section for details.
21	CLATCH/WP	D_IO	SPI Latch Signal/Self-Boot EEPROM Write Protect. This is a multifunction pin as follows: CLATCH: SPI Latch Signal. Must go low at the beginning of an SPI transaction and high at the end of a transaction. Each SPI transaction can take a different number of cycles on the CCLK pin to complete, depending on the address and read/write bit that are sent at the beginning of the SPI transaction. See the SPI Port section for details. WP: Self-Boot EEPROM Write Protect. This pin is an open-collector output when in self-boot mode. The ADAU1701 pulls this low to enable writes to an external EEPROM. This pin should be pulled high to 3.3 V. See the Self-Boot section for details.
22	SDA/COUT	D_IO	I ² C Data/SPI Data Output. This is a multifunction pin, as follows: SDA: I ² C Data. This pin is a bidirectional open-collector. The line connected to this pin should have a 2.2 k Ω pull-up resistor. See the I ² C Port section for details. COUT: This SPI data output is used for reading back registers and memory locations. It is three-stated when an SPI read is not active. See the SPI Port section for details.
23	SCL/CCLK	D_IO	I ² C Clock/SPI Clock. This is a dual function pin, as follows: SCL: I ² C Clock. This pin is always an open-collector input when in I ² C control mode. In self-boot mode, this pin is an open-collector output (I ² C master). The line connected to this pin should have a 2.2 k Ω pull-up resistor. See the I ² C Port section for details. CCLK: SPI Clock. This pin can either run continuously or be gated off between SPI transactions. See the SPI Port section for details.
26	MP9	D_IO/A_IO	Multipurpose GPIO, Serial Output Port Data 3 (SDATA_OUT3), or Auxiliary ADC Input 0. See the Multipurpose Pins section for more details.
27	MP8	D_IO/A_IO	Multipurpose GPIO, Serial Output Port Data 2 (SDATA_OUT2), or Auxiliary ADC Input 3. See the Multipurpose Pins section for more details.
28	MP3	D_IO/A_IO	Multipurpose GPIO, Serial Input Port Data 3 (SDATA_IN3), or Auxiliary ADC Input 2. See the Multipurpose Pins section for more details.
29	MP2	D_IO/A_IO	Multipurpose GPIO, Serial Input Port Data 2 (SDATA_IN2), or Auxiliary ADC Input 1. See the Multipurpose Pins section for more details.
30	RSVD		Reserved. Tie to ground, either directly or through a pull-down resistor.
31	OSCO	D_OUT	Crystal Oscillator Circuit Output. Connect a 100 Ω damping resistor between this pin and the crystal. Do not use this output to directly drive a clock to another IC. If the crystal oscillator is not used, this pin can be left disconnected. See the Using the Oscillator section for details.
32	MCLKI	D_IN	Master Clock Input. MCLKI can either be connected to a 3.3 V clock signal or be the input from the crystal oscillator circuit. See the Setting Master Clock/PLL Mode section for details.

Pin No.	Mnemonic	Type ¹	Description
33	PGND	PWR	PLL Ground Pin. The AGND, DGND, and PGND pins can be tied directly together in a common ground plane. Decouple PGND to PVDD by using a 100 nF capacitor.
34	PVDD	PWR	3.3 V Power Supply for the PLL and the Auxiliary ADC Analog Section. Decouple this pin to PGND by using a 100 nF capacitor.
35	PLL_LF	A_OUT	PLL Loop Filter Connection. Two capacitors and a resistor need to be connected to this pin, as shown in Figure 15. See the Setting Master Clock/PLL Mode section for more details.
36, 48	AVDD	PWR	3.3V Analog Supply. Decouple this pin to AGND by using a 100 nF capacitor.
38, 39	PLL_MODE0, PLL_MODE1	D_IN	PLL Mode Setting. PLL_MODE0 and PLL_MODE1 set the output frequency of the master clock PLL. See the Setting Master Clock/PLL Mode section for more details.
40	CM	A_OUT	1.5 V Common-Mode Reference. Connect a 47 μ F decoupling capacitor between this pin and ground to reduce crosstalk between the ADCs and DACs. The material of the capacitors is not critical. This pin can be used to bias external analog circuits, as long as those circuits are not drawing current from the pin (such as when CM is connected to the noninverting input of an op amp).
41	FILTD	A_OUT	DAC Filter Decoupling Pin. Connect a 10 μ F capacitor between this pin and ground. The capacitor material is not critical. The voltage on this pin is 1.5 V.
43 to 46	VOUT3	A_OUT	VOUT DAC Output. The full-scale output voltage is 0.9 V rms. This output can be used with either an active or passive output reconstruction filter. See the Audio DACs section for details.
44	VOUT2	A_OUT	VOUT2 DAC Output. The full-scale output voltage is 0.9 V rms. This output can be used with either an active or passive output reconstruction filter. See the Audio DACs section for details.
45	VOUT1	A_OUT	VOUT1 DAC Output. The full-scale output voltage is 0.9 V rms. This output can be used with either an active or passive output reconstruction filter. See the Audio DACs section for details.
46	VOUT0	A_OUT	VOUT0 DAC Output. The full-scale output voltage is 0.9 V rms. This output can be used with either an active or passive output reconstruction filter. See the Audio DACs section for details.
47	FILTA	A_OUT	ADC Filter Decoupling Pin. A 10 μ F capacitor should be connected between this pin and ground. The capacitor material is not critical. The voltage on this pin is 1.5 V.

¹ PWR = power/ground, A_IN = analog input, D_IN = digital input, A_OUT = analog output, D_IO = digital input/output, D_IO/A_IO = digital input/output or analog input/output.

TYPICAL PERFORMANCE CHARACTERISTICS

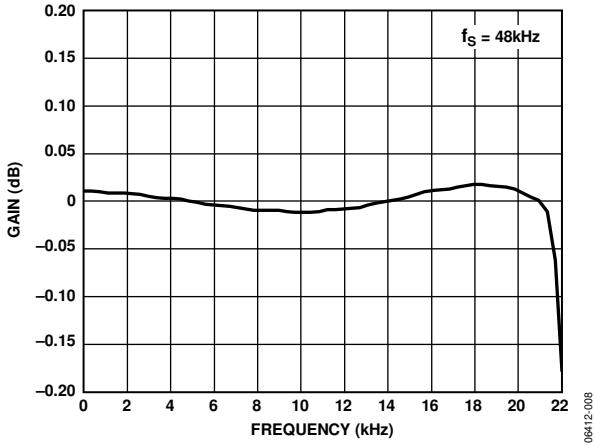


Figure 8. ADC Pass-Band Filter Response

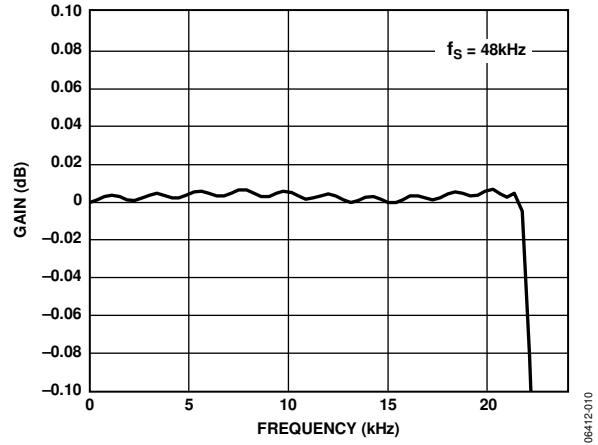


Figure 10. DAC Pass-Band Filter Response

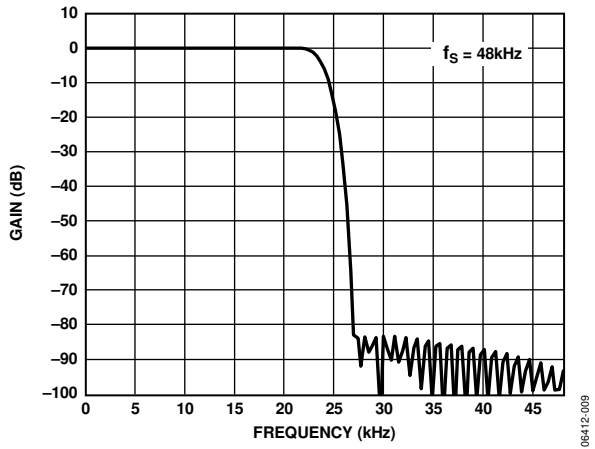


Figure 9. ADC Stop-Band Filter Response

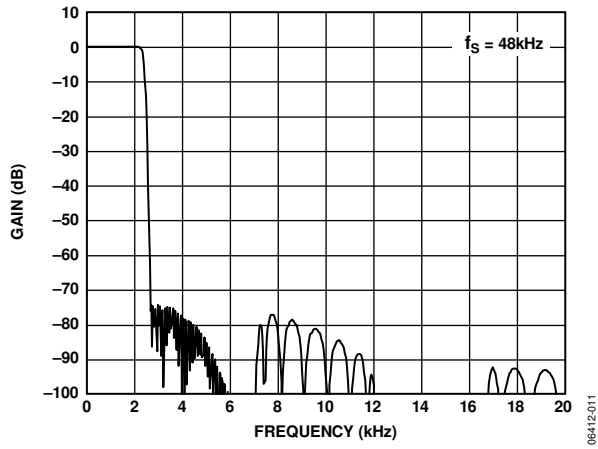


Figure 11. DAC Stop-Band Filter Response

SYSTEM BLOCK DIAGRAM

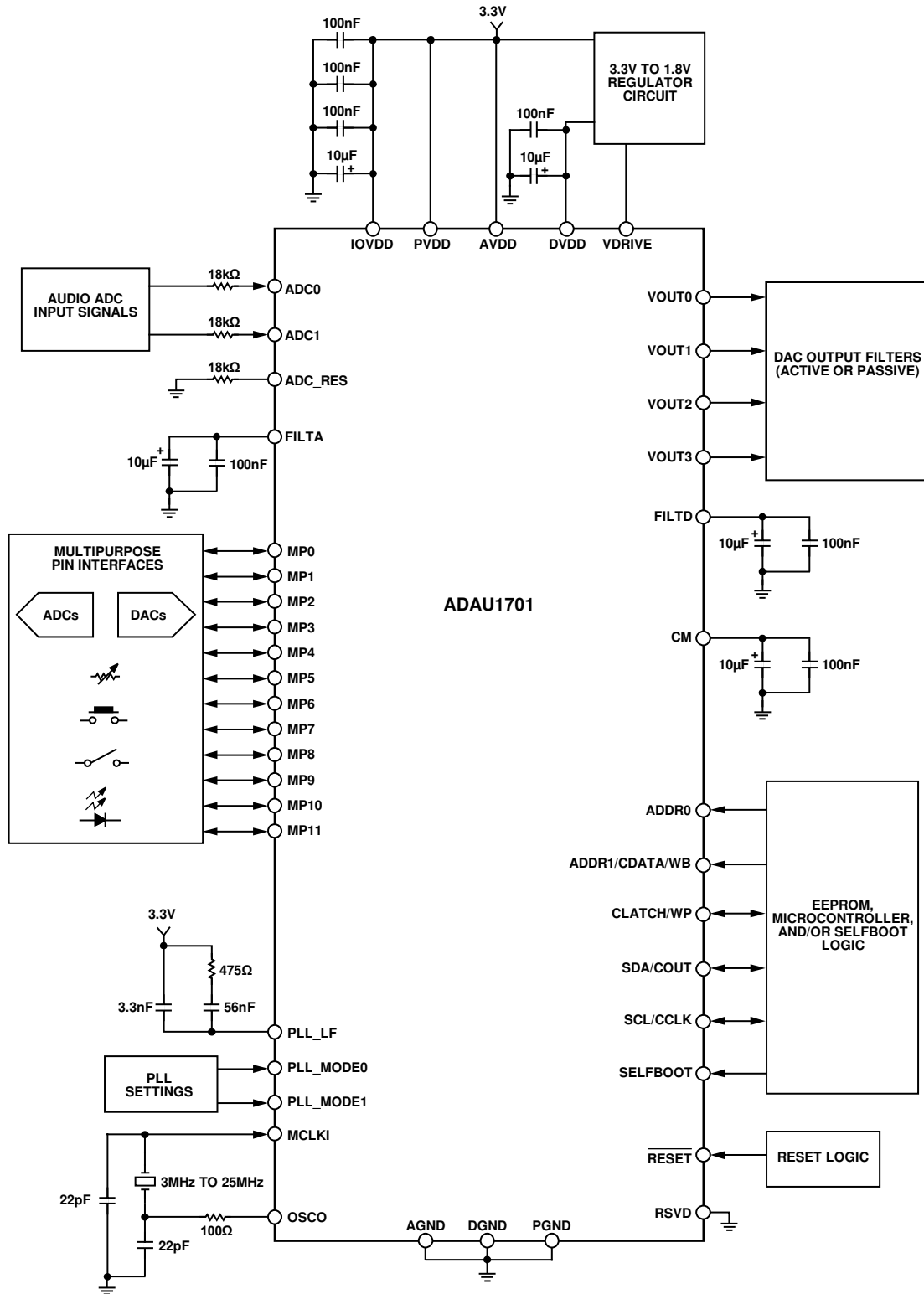


Figure 12. System Block Diagram

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THEORY OF OPERATION

The core of the [ADAU1701](#) is a 28-bit DSP (56-bit with double-precision processing) optimized for audio processing. The program and parameter RAMs can be loaded with a custom audio processing signal flow built by using SigmaStudio graphical programming software from Analog Devices, Inc. The values stored in the parameter RAM control individual signal processing blocks, such as equalization filters, dynamics processors, audio delays, and mixer levels. A safeload feature allows for transparent parameter updates and prevents clicks in the output signals.

The program RAM, parameter RAM, and register contents can be saved in an external EEPROM, from which the [ADAU1701](#) can self-boot on startup. In this standalone mode, parameters can be controlled through the on-board multipurpose pins. The [ADAU1701](#) can accept controls from switches, potentiometers, rotary encoders, and IR receivers. Parameters such as volume and tone settings can be saved to the EEPROM on power-down and recalled again on power-up.

The [ADAU1701](#) can operate with digital or analog inputs and outputs, or a mix of both. The stereo ADC and four DACs each have an SNR of at least +100 dB and a THD + N of at least -83 dB. The 8-channel, flexible serial data input/output ports allow glueless interconnection to a variety of ADCs, DACs, general-purpose DSPs, S/PDIF receivers and transmitters, and sample rate converters. The serial ports of the [ADAU1701](#) can be configured in I²S, left-justified, right-justified, or TDM serial port-compatible modes.

Twelve multipurpose (MP) pins allow the [ADAU1701](#) to receive external control signals as input and to output flags or controls to other devices in the system. The MP pins can be configured as digital I/Os, inputs to the 4-channel auxiliary ADC, or serial data I/O ports. As inputs, they can be connected to buttons, switches, rotary encoders, potentiometers, IR receivers, or other external circuitry to control the internal signal processing program. When configured as outputs, these pins can be used to drive LEDs, control other ICs, or connect to other external circuitry in an application.

The [ADAU1701](#) has a sophisticated control port that supports complete read/write capability of all memory locations. Control registers are provided to offer complete control of the configuration and serial modes of the chip. The [ADAU1701](#) can be configured for either SPI or I²C control, or can self-boot from an external EEPROM.

An on-board oscillator can be connected to an external crystal to generate the master clock. In addition, a master clock phase-

locked loop (PLL) allows the [ADAU1701](#) to be clocked from a variety of different clock speeds. The PLL can accept inputs of $64 \times f_s$, $256 \times f_s$, $384 \times f_s$, or $512 \times f_s$ to generate the internal master clock of the core.

The SigmaStudio software is used to program and control the SigmaDSP® through the control port. Along with designing and tuning a signal flow, the tools can be used to configure all of the DSP registers and burn a new program into the external EEPROM. The SigmaStudio graphical interface allows anyone with digital or analog audio processing knowledge to easily design a DSP signal flow and port it to a target application. At the same time, it provides enough flexibility and programmability for an experienced DSP programmer to have in-depth control of the design. In SigmaStudio, the user can connect graphical blocks (such as biquad filters, dynamics processors, mixers, and delays), compile the design, and load the program and parameter files into the [ADAU1701](#) memory through the control port. Signal processing blocks available in the provided libraries include

- Single- and double-precision biquad filters
- Processors with peak or rms detection for monochannel and multichannel dynamics
- Mixers and splitters
- Tone and noise generators
- Fixed and variable gain
- Loudness
- Delay
- Stereo enhancement
- Dynamic bass boost
- Noise and tone sources
- FIR filters
- Level detectors
- GPIO control and conditioning

Additional processing blocks are always being developed. Analog Devices also provides proprietary and third-party algorithms for applications such as matrix decoding, bass enhancement, and surround virtualizers. Contact Analog Devices for information about licensing these algorithms.

The [ADAU1701](#) operates from a 1.8 V digital power supply and a 3.3 V analog supply. An on-board voltage regulator can be used to operate the chip from a single 3.3 V supply. It is fabricated on a single monolithic, integrated circuit and is packaged in a 48-lead LQFP for operation over the 0°C to +70°C temperature range.

INITIALIZATION

This section details the procedure for properly setting up the ADAU1701. The following five-step sequence provides an overview of how to initialize the IC:

1. Apply power to ADAU1701.
2. Wait for PLL to lock.
3. Load SigmaDSP program and parameters.
4. Set up registers (including multipurpose pins and digital interfaces).
5. Turn off the default muting of the converters, clear the data registers, and initialize the DAC setup register (see the Control Registers Setup section for specific settings).

To only test analog audio pass-through (ADCs to DACs), skip Step 3 and Step 4 and use the default internal program.

POWER-UP SEQUENCE

The ADAU1701 has a built-in power-up sequence that initializes the contents of all internal RAMs on power-up or when the device is brought out of a reset. On the positive edge of $\overline{\text{RESET}}$, the contents of the internal program boot ROM are copied to the internal program RAM memory, the parameter RAM is filled with values (all 0s) from its associated boot ROM, and all registers are initialized to 0s. The default boot ROM program copies audio from the inputs to the outputs without processing it (see Figure 13). In this program, serial digital Input 0 and Input 1 are output on DAC0 and DAC1 and serial digital Output 0 and Output 1. ADC0 and ADC1 are output on DAC2 and DAC3. The data memories are also zeroed at power-up. New values should not be written to the control port until the initialization is complete.

Table 11. Power-Up Time

MCLKI Input	Init. Time	Max Program/Parameter/Register Boot Time (I ² C)	Total
3.072 MHz ($64 \times f_s$)	85 ms	175 ms	260 ms
11.289 MHz ($256 \times f_s$)	23 ms	175 ms	198 ms
12.288 MHz ($256 \times f_s$)	21 ms	175 ms	196 ms
18.432 MHz ($384 \times f_s$)	16 ms	175 ms	191 ms
24.576 MHz ($512 \times f_s$)	11 ms	175 ms	186 ms

The PLL start-up time lasts for 2^{18} cycles of the clock on the MCLKI pin. This time ranges from 10.7 ms for a 24.576 MHz ($512 \times f_s$) input clock to 85.3 ms for a 3.072 MHz ($64 \times f_s$) input clock and is measured from the rising edge of $\overline{\text{RESET}}$. Following the PLL startup, the duration of the ADAU1701 boot cycle is about 42 μs for a f_s of 48 kHz. The user should avoid writing to or reading from the ADAU1701 during this start-up time. For an MCLK input of 12.288 MHz, the full initialization sequence (PLL startup plus boot cycle) is approximately 21 ms. As the device comes out of a reset, the clock mode is immediately set by the PLL_MODE0 and PLL_MODE1 pins. The reset is synchronized to the falling edge of the internal clock.

Table 11 lists typical times to boot the ADAU1701 into an operational state of an application, assuming a 400 kHz I²C clock loading a full program, parameter set, and all registers (about 8.5 kB). In reality, most applications do not fill the RAMs and therefore boot time (Column 3 of Table 11) is less.

CONTROL REGISTERS SETUP

The following registers must be set as described in this section to initialize the ADAU1701. These settings are the basic minimum settings needed to operate the IC with an analog input/output of 48 kHz. More registers may need to be set, depending on the application. See the RAMs and Registers section for additional settings.

DSP Core Control Register (Address 2076)

Set Bits[4:2] (ADM, DAM, and CR) each to 1.

DAC Setup Register (Address 2087)

Set Bits[0:1] (DS[1:0]) to 01.

RECOMMENDED PROGRAM/PARAMETER LOADING PROCEDURE

When writing large amounts of data to the program or parameter RAM in direct write mode, the processor core should be disabled to prevent unpleasant noises from appearing in the audio output.

1. Set Bit 3 and Bit 4 (active low) of the core control register to 1 to mute the ADCs and DACs. This begins a volume ramp-down.
2. Set Bit 2 (active low) of the core control register to 1. This zeroes the SigmaDSP accumulators, the data output registers, and the data input registers.
3. Fill the program RAM using burst mode writes.
4. Fill the parameter RAM using burst mode writes.
5. Deassert Bit 2 to Bit 4 of the core control register.

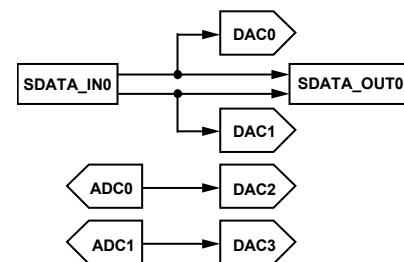


Figure 13. Default Program Signal Flow

POWER REDUCTION MODES

Sections of the ADAU1701 chip can be turned on and off as needed to reduce power consumption. These include the ADCs, DACs, and voltage reference.

The individual analog sections can be turned off by writing to the auxiliary ADC and power control register. By default, the ADCs, DACs, and reference are enabled (all bits set to 0). Each of these can be turned off by writing a 1 to the appropriate bits

in this register. The ADC power-down mode powers down both ADCs, and each DAC can be powered down individually. The current savings is about 15 mA when the ADCs are powered down and about 4 mA for each DAC that is powered down. The voltage reference, which is supplied to both the ADCs and DACs, should only be powered down if all ADCs and DACs are powered down. The reference is powered down by setting both Bit 6 and Bit 7 of the control register.

USING THE OSCILLATOR

The ADAU1701 can use an on-board oscillator to generate its master clock. The oscillator is designed to work with a $256 \times f_s$ master clock, which is 12.288 MHz for a f_s of 48 kHz and 11.2896 MHz for a f_s of 44.1 kHz. The crystal in the oscillator circuit should be an AT-cut, parallel resonator operating at its fundamental frequency. Figure 14 shows the external circuit recommended for proper operation.

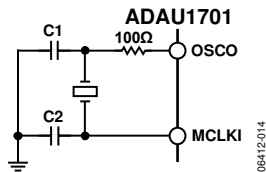


Figure 14. Crystal Oscillator Circuit

The 100 Ω damping resistor on OSCO gives the oscillator a voltage swing of approximately 2.2 V. The crystal shunt capacitance should be 7 pF. Its load capacitance should be about 18 pF, although the circuit supports values of up to 25 pF. The necessary values of the C1 and C2 load capacitors can be calculated from the crystal load capacitance as follows:

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_{stray}$$

where C_{stray} is the stray capacitance in the circuit and is usually assumed to be approximately 2 pF to 5 pF.

OSCO should not be used to directly drive the crystal signal to another IC. This signal is an analog sine wave, and it is not appropriate to use it to drive a digital input. There are two options for using the ADAU1701 to provide a master clock to other ICs in the system. The first, and less recommended, method is to use a high impedance input digital buffer on the OSCO signal. If this is done, minimize the trace length to the buffer input. The second method is to use a clock from the serial output port. Pin MP11 can be set as an output (master) clock divided down from the internal core clock. If this pin is set to serial output port (OUTPUT_BCLK) mode in the multipurpose pin configuration register (2081) and the port is set to master in the serial output control register (2078), the desired output frequency can also be set in the serial output control register with Bits[OBF<1:0>] (see Table 48).

If the oscillator is not utilized in the design, it can be powered down to save power. This can be done if a system master clock is already available in the system. By default, the oscillator is powered on. The oscillator powers down when a 1 is written to the OPD bit of the oscillator power-down register (see Table 59).

SETTING MASTER CLOCK/PLL MODE

The MCLKI input of the ADAU1701 feeds a PLL, which generates the 50 MIPS SigmaDSP core clock. In normal operation, the input to MCLKI must be one of the following: $64 \times f_s$, $256 \times f_s$, $384 \times f_s$, or $512 \times f_s$, where f_s is the input sampling rate. The mode is set on PLL_MODE0 and PLL_MODE1 as described in Table 12. If the ADAU1701 is set to receive double-rate signals (by reducing the number of program steps per sample by a factor of 2 using the core control register), the master clock frequency must be $32 \times f_s$, $128 \times f_s$, $192 \times f_s$, or $256 \times f_s$. If the ADAU1701 is set to receive quad-rate signals (by reducing the number of program steps per sample by a factor of 4 using the core control register), the master clock frequency must be $16 \times f_s$, $64 \times f_s$, $96 \times f_s$, or $128 \times f_s$. On power-up, a clock signal must be present on the MCLKI pin so that the ADAU1701 can complete its initialization routine.

Table 12. PLL Modes

MCLKI Input	PLL_MODE0	PLL_MODE1
$64 \times f_s$	0	0
$256 \times f_s$	0	1
$384 \times f_s$	1	0
$512 \times f_s$	1	1

The clock mode should not be changed without also resetting the ADAU1701. If the mode is changed during operation, a click or pop can result in the output signals. The state of the PLL_MODEx pins should be changed while RESET is held low.

The PLL loop filter should be connected to the PLL_LF pin. This filter, shown in Figure 15, includes three passive components—two capacitors and a resistor. The values of these components do not need to be exact; the tolerance can be up to 10% for the resistor and up to 20% for the capacitors. The 3.3 V signal shown in Figure 15 can be connected to the AVDD supply of the chip.

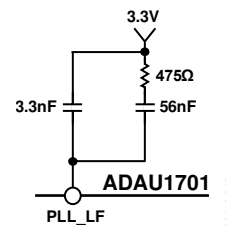


Figure 15. PLL Loop Filter

VOLTAGE REGULATOR

The digital voltage of the ADAU1701 must be set to 1.8 V. The chip includes an on-board voltage regulator that allows the device to be used in systems without an available 1.8 V supply but with an available 3.3 V supply. The only external components needed in such instances are a PNP transistor, a resistor, and a few bypass capacitors. Only one pin, VDRIVE, is necessary to support the regulator.

The recommended design for the voltage regulator is shown in Figure 16. The 10 μ F and 100 nF capacitors shown in this configuration are recommended for bypassing, but are not necessary for operation. Each DVDD pin should have its own 100 nF bypass capacitor, but only one bulk capacitor (10 μ F to 47 μ F) is needed for both DVDD pins. With this configuration, 3.3 V is the main system voltage; 1.8 V is generated at the transistor's collector, which is connected to the DVDD pins. VDRIVE is connected to the base of the PNP transistor. If the regulator is not used in the design, VDRIVE can be tied to ground.

Two specifications must be considered when choosing a regulator transistor: The transistor's current amplification factor (h_{FE} or beta) should be at least 100, and the transistor's collector must be able to dissipate the heat generated when regulating from 3.3 V to 1.8 V. The maximum digital current drawn from the ADAU1701 is 60 mA. The equation to determine the minimum power dissipation of the transistor is as follows:

$$(3.3 \text{ V} - 1.8 \text{ V}) \times 60 \text{ mA} = 90 \text{ mW}$$

There are many transistors, such as the FZT953 from Zetex Semiconductors, with these specifications available in small SOT-23 or SOT-223 packages.

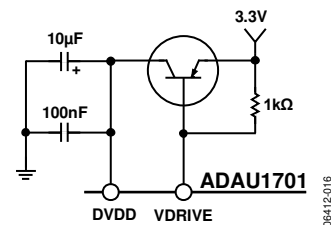


Figure 16. Voltage Regulator Configuration

AUDIO ADCs

The ADAU1701 has two Σ - Δ ADCs. The signal-to-noise ratio (SNR) of the ADCs is 100 dB, and the THD + N is -83 dB.

The stereo audio ADCs are current input; therefore, a voltage-to-current resistor is required on the inputs. This means that the voltage level of the input signals to the system can be set to any level; only the input resistors need to be scaled to provide the proper full-scale current input. The ADC0 and ADC1 input pins, as well as ADC_RES, have an internal 2 k Ω resistor for ESD protection. The voltage seen directly on the ADC input pins is the 1.5 V common mode.

The external resistor connected to ADC_RES sets the full-scale current input of the ADCs. The full range of the ADC inputs is 100 μ A rms with an external 18 k Ω resistor on ADC_RES (20 k Ω total, because it is in series with the internal 2 k Ω). The only reason to change the ADC_RES resistor is if a sampling rate other than 48 kHz is used.

The voltage-to-current resistors connected to ADC0/ADC1 set the full-scale voltage input of the ADCs. With a full-scale current input of 100 μ A rms, a 2.0 V rms signal with an external 18 k Ω resistor (in series with the 2 k Ω internal resistor) results in an input using the full range of the ADC. The matching of these resistors to the ADC_RES resistor is important to the operation of the ADCs. For these three resistors, a 1% tolerance is recommended.

Either the ADC0 and/or ADC1 input pins can be left unconnected if that channel of the ADC is unused.

These calculations of resistor values assume a 48 kHz sample rate. The recommended input and current setting resistors scale linearly with the sample rate because the ADCs have a switched-capacitor input. The total value (2 k Ω internal plus external resistor) of the ADC_RES resistor with sample rate f_{S_NEW} can be calculated as follows:

$$R_{total} = 20 \text{ k}\Omega \times \frac{48,000}{f_{S_NEW}}$$

The values of the resistors (internal plus external) in series with the ADC0 and ADC1 pins can be calculated as follows:

$$R_{Input\ Total} = (rms\ Input\ Voltage) \times 10 \text{ k}\Omega \times \frac{48,000}{f_{S_NEW}}$$

Table 13 lists the external and total resistor values for common signal input levels at a 48 kHz sampling rate. A full-scale rms input voltage of 0.9 V is shown in the table because a full-scale signal at this input level is equal to a full-scale output on the DACs.

Table 13. ADC Input Resistor Values

Full-Scale RMS Input Voltage (V)	ADC_RES Value (k Ω)	ADC0/ADC1 Resistor Value (k Ω)	Total ADC0/ADC1 Input Resistance (External + Internal) (k Ω)
0.9	18	7	9
1.0	18	8	10
2.0	18	18	20

Figure 17 shows a typical configuration of the ADC inputs for a 2.0 V rms input signal for a f_s of 48 kHz. The 47 μ F capacitors are used to ac-couple the signals so that the inputs are biased at 1.5 V.

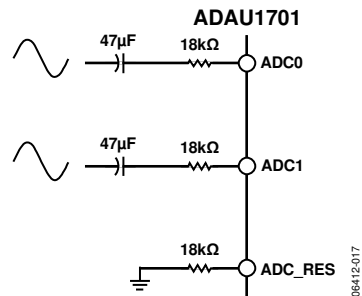


Figure 17. Audio ADC Input Configuration

AUDIO DACs

The ADAU1701 includes four Σ - Δ DACs. The SNR of the DAC is 104 dB, and the THD + N is -90 dB. A full-scale output on the DACs is 0.9 V rms (2.5 V p-p).

The DACs are in an inverting configuration. If a signal inversion from input to output is undesirable, it can be reversed either by using an inverting configuration for the output filter or by simply inverting the signal in the SigmaDSP program flow.

The DAC outputs can be filtered with either an active or a passive reconstruction filter. A single-pole, passive, low-pass filter with a 50 kHz corner frequency, as shown in Figure 18, is sufficient to filter the DAC out-of-band noise, although an active filter may provide better audio performance. Figure 19

shows a triple-pole, active, low-pass filter that provides a steeper roll-off and better stop band attenuation than the passive filter. In this configuration, the V+ and V- pins of the AD8606 op amp are set to AVDD and ground, respectively.

To properly initialize the DACs, the DS[1:0] bits in the DAC setup register (Address 2087) should be set to 01.

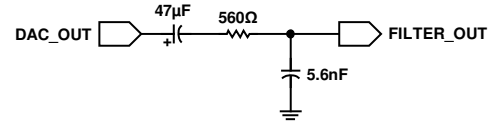


Figure 18. Passive DAC Output Filter

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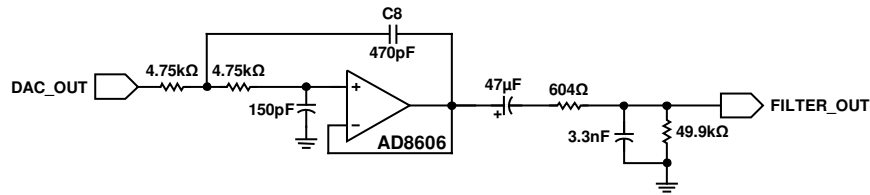


Figure 19. Active DAC Output Filter

08412-019

CONTROL PORTS

The ADAU1701 can operate in one of three control modes:

- I²C control
- SPI control
- Self-boot (no external controller)

The ADAU1701 has both a 4-wire SPI control port and a 2-wire I²C bus control port. Each can be used to set the RAMs and registers. When the SELFBOT pin is low at power-up, the part defaults to I²C mode but can be put into SPI control mode by pulling the CLATCH/WP pin low three times. When the SELFBOT pin is set high at power-up, the ADAU1701 loads its program, parameters, and register settings from an external EEPROM on startup.

The control port is capable of full read/write operation for all addressable memory and registers. Most signal processing parameters are controlled by writing new values to the parameter RAM using the control port. Other functions, such as mute and input/output mode control, are programmed by writing to the registers.

All addresses can be accessed in a single-address mode or a burst mode. The first byte (Byte 0) of a control port write contains the 7-bit chip address plus the R/W bit. The next two bytes (Byte 1 and Byte 2) together form the subaddress of the memory or register location within the ADAU1701. This subaddress must be two bytes because the memory locations within the ADAU1701 are directly addressable and their sizes

exceed the range of single-byte addressing. All subsequent bytes (starting with Byte 3) contain the data, such as control port data, program data, or parameter data. The number of bytes per word depends on the type of data that is being written. The exact formats for specific types of writes are shown in Table 21 to Table 30.

The ADAU1701 has several mechanisms for updating signal processing parameters in real time without causing pops or clicks. If large blocks of data need to be downloaded, the output of the DSP core can be halted (using the CR bit in the DSP core control register (Address 2076)), new data can be loaded, and then the device can be restarted. This is typically done during the booting sequence at startup or when loading a new program into RAM. In cases where only a few parameters need to be changed, they can be loaded without halting the program. To avoid unwanted side effects while loading parameters on the fly, the SigmaDSP provides the safeload registers. The safeload registers can be used to buffer a full set of parameters (for example, the five coefficients of a biquad) and then transfer these parameters into the active program within one audio frame. The safeload mode uses internal logic to prevent contention between the DSP core and the control port.

The control port pins are multifunctional, depending on the mode in which the part is operating. Table 14 details these multiple functions.

Table 14. Control Port Pins and SELFBOT Pin Functions

Pin	I ² C Mode	SPI Mode	Self-Boot
SCL/CCLK	SCL—input	CCLK—input	SCL—output
SDA/COUT	SDA—open-collector output	COUT—output	SDA—open-collector output
ADDR1/CDATA/WB	ADDR1—input	CDATA—input	WB—writeback trigger
CLATCH/WP	Unused input—tie to ground or IOVDD	CLATCH—input	WP—EEPROM write protect, open-collector output
ADDR0	ADDR0—input	ADDR0—input	Unused input—tie to ground or IOVDD

I²C PORT

The ADAU1701 supports a 2-wire serial (I²C-compatible) microprocessor bus driving multiple peripherals. Two pins, serial data (SDA) and serial clock (SCL), carry information between the ADAU1701 and the system I²C master controller. In I²C mode, the ADAU1701 is always a slave on the bus, meaning it cannot initiate a data transfer. Each slave device is recognized by a unique address. The address byte format is shown in Table 15. The ADAU1701 slave addresses are set with the ADDR0 and ADDR1 pins. The address resides in the first seven bits of the I²C write. The LSB of this byte sets either a read or write operation. Logic Level 1 corresponds to a read operation, and Logic Level 0 corresponds to a write operation. Bit 5 and Bit 6 of the address are set by tying the ADDR_x pins of the ADAU1701 to Logic Level 0 or Logic Level 1. The full byte addresses, including the pin settings and read/write (R/W) bit, are shown in Table 16.

Burst mode addressing, where the subaddresses are automatically incremented at word boundaries, can be used for writing large amounts of data to contiguous memory locations. This increment happens automatically after a single-word write unless a stop condition is encountered. The registers and RAMs in the ADAU1701 range in width from one to five bytes, so the auto-increment feature knows the mapping between subaddresses and the word length of the destination register (or memory location). A data transfer is always terminated by a stop condition.

Both SDA and SCL should have 2.2 kΩ pull-up resistors on the lines connected to them. The voltage on these signal lines should not be more than IOVDD (3.3 V).

Table 15. ADAU1701 I²C Address Byte Format

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	1	1	0	1	ADDR1	ADDR0	R/W

Table 16. ADAU1701 I²C Addresses

ADDR1	ADDR0	R/W	Slave Address
0	0	0	0x68
0	0	1	0x69
0	1	0	0x6A
0	1	1	0x6B
1	0	0	0x6C
1	0	1	0x6D
1	1	0	0x6E
1	1	1	0x6F

Addressing

Initially, each device on the I²C bus is in an idle state monitoring the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream follows. All devices on the bus respond to the start condition and shift the next eight bits (the 7-bit address plus the R/W bit) MSB first. The device that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This ninth bit is known as an acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition. The R/W bit determines the direction of the data. A Logic 0 on the LSB of the first byte means the master writes information to the peripheral, whereas a Logic 1 means the master reads information from the peripheral after writing the subaddress and repeating the start address. A data transfer takes place until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high. Figure 20 shows the timing of an I²C write, and Figure 21 shows an I²C read.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, the ADAU1701 immediately jumps to the idle condition. During a given SCL high period, the user should only issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADAU1701 does not issue an acknowledge and returns to the idle condition. If the user exceeds the highest subaddress while in auto-increment mode, one of two actions is taken. In read mode, the ADAU1701 outputs the highest subaddress register contents until the master device issues a no acknowledge, indicating the end of a read. A no-acknowledge condition is where the SDA line is not pulled low on the ninth clock pulse on SCL. On the other hand, if the highest subaddress location is reached while in write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the ADAU1701, and the part returns to the idle condition.

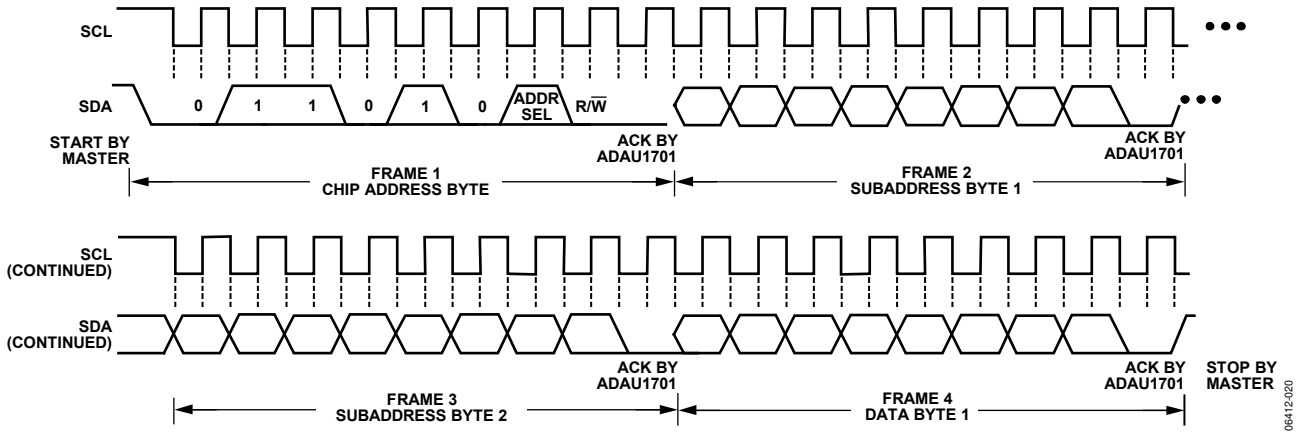


Figure 20. I²C Write to ADAU1701 Clcking

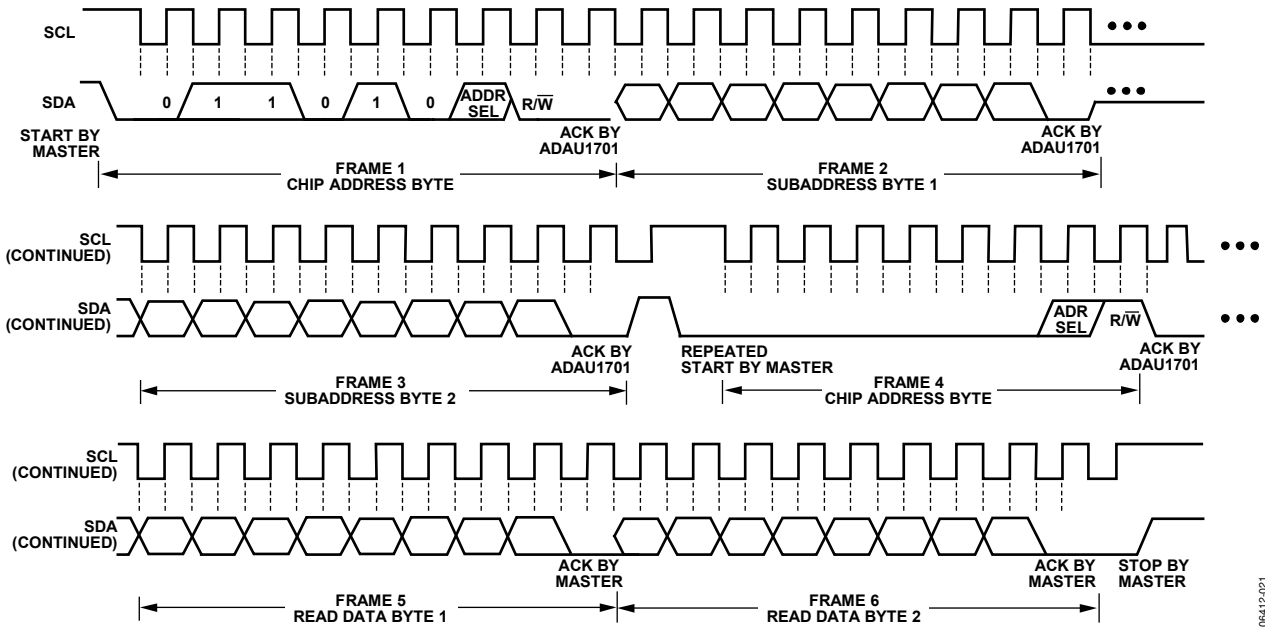


Figure 21. I²C Read from ADAU1701 Clcking