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Four-ADC, Two-DAC, Low Power Codec with Audio Processor

Data Sheet

ADAU1777

FEATURES

- Programmable audio processing engine
  - Fast (up to 768 kHz) and slow processing paths
  - Biquad filters, limiters, volume controls, and mixing
- Low latency, 24-bit ADCs and DACs
  - 102 dB SNR (through PGA and ADC with A weighted filter)
  - 108 dB combined SNR (through DAC and headphone with A weighted filter)
- Serial port sampling rate from 8 kHz to 192 kHz
- 5 µs analog-to-analog latency
- 4 single-ended analog inputs, configurable as microphone or line inputs
- Dual stereo digital microphone inputs
- Stereo analog audio output, single-ended or differential, configurable as either line output or headphone driver
- PLL supporting any input clock rate from 8 MHz to 27 MHz
- Full duplex, asynchronous sample rate converters (ASRCs)
- Power supplies
  - Analog and digital input/output of 1.8 V to 3.3 V
  - Digital signal processing (DSP) core of 1.1 V to 1.8 V
- Low power
- I²C and SPI control interfaces, self boot from I²C EEPROM
- 7 multipurpose (MPx) pins for digital controls and outputs

APPLICATIONS

- Noise canceling handsets, headsets, and headphones
- Bluetooth® active noise canceling (ANC) handsets, headsets, and headphones
- Personal navigation devices
- Digital still and video cameras

GENERAL DESCRIPTION

The ADAU1777 is a codec with four inputs and two outputs that incorporates a digital processing engine to perform filtering, level control, signal level monitoring, and mixing. The path from the analog input to the DSP core to the analog output is optimized for low latency and is ideal for noise canceling headsets. With the addition of just a few passive components, a crystal, and an EEPROM for booting, the ADAU1777 provides a complete headset solution.

Note that throughout this data sheet, multifunction pins, such as SCL/SCLK, are referred to either by the entire pin name or by a single function of the pin, for example, SCLK, when only that function is relevant.

FUNCTIONAL BLOCK DIAGRAM

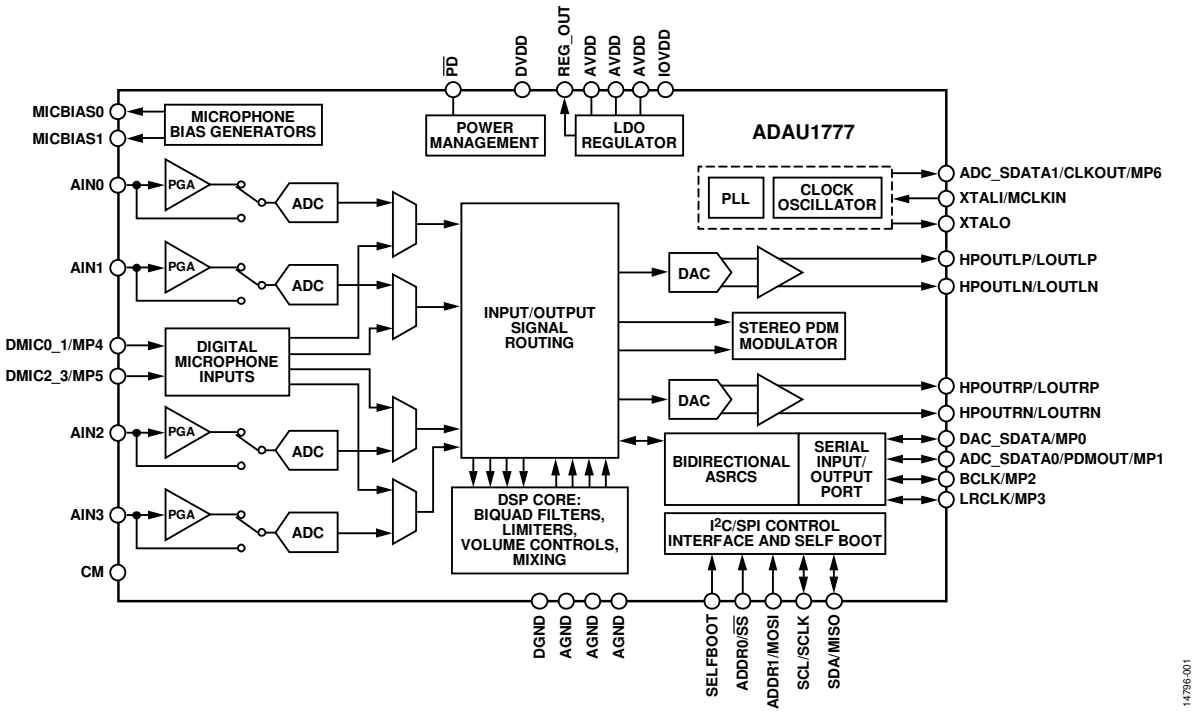

Figure 1.

Rev. 0 Document Feedback

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COMPARABLE PARTS

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EVALUATION KITS

- ADAU1777 Evaluation Board

DOCUMENTATION

Data Sheet

- ADAU1777: Four-ADC, Two-DAC, Low Power Codec with Audio Processor Data Sheet

User Guides

- UG-1055: Evaluating the ADAU1777 Four ADC, Two DAC, Low Power Codec with Audio Processor

DESIGN RESOURCES

- ADAU1777 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADAU1777 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

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REVISION HISTORY

12/2016—Revision 0: Initial Version

SPECIFICATIONS

Master clock = 12.288 MHz, serial input sample rate = 48 kHz, measurement bandwidth = 20 Hz to 20 kHz, word width = 24 bits, T_A = 25°C, outputs line loaded with 10 kΩ.

ANALOG PERFORMANCE SPECIFICATIONS

AVDD = IOVDD = 1.8 V, DVDD = 1.1 V, unless otherwise noted. Phase-locked loop (PLL) disabled, direct master clock.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTERS (ADCs)					
ADC Resolution	All ADCs		24		Bits
Digital Attenuation Step			0.375		dB
Digital Attenuation Range			95		dB
INPUT RESISTANCE	Gain settings do not include 10 dB gain from PGA_x_BOOST settings; this additional gain does not affect input impedance; PGA_POP_DISx = 1				
Single-Ended Line Input	0 dB gain		14.3		kΩ
Programmable Gain Amplifier (PGA) Inputs	−12 dB gain		32.0		kΩ
	0 dB gain		20		kΩ
	+35.25 dB gain		0.68		kΩ
LINE INPUT	PGA_ENx = 0, PGA_x_BOOST = 0, PGA_POP_DISx = 1				
Full-Scale Input Voltage	Scales linearly with AVDD		AVDD/3.3		V rms
	AVDD = 1.8 V		0.55		V rms
	AVDD = 1.8 V		1.54		V p-p
	AVDD = 3.3 V		1.00		V rms
	AVDD = 3.3 V		2.83		V p-p
Dynamic Range[1]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V	95	97		dB
	AVDD = 3.3 V	99	102		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V	92	94		dB
	AVDD = 3.3 V	96	99		dB
Signal-to-Noise Ratio (SNR)[2]					
With A-Weighted Filter (RMS)	AVDD = 1.8 V	96	98		dB
	AVDD = 3.3 V	100	103		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V	92	96		dB
	AVDD = 3.3 V	96	100		dB
Interchannel Gain Mismatch		0	40	200	mdB
Total Harmonic Distortion + Noise (THD + N)	20 Hz to 20 kHz, −1 dB from full-scale input				
	AVDD = 1.8 V		−90	−83	dB
	AVDD = 3.3 V		−94	−87	dB
Offset Error		−0.11		+0.12	mV
Gain Error		−0.4		+0.2	dB
Interchannel Isolation	CM capacitor = 22 µF		95		dB
Power Supply Rejection Ratio (PSRR)	CM capacitor = 22 µF, 100 mV p-p at 1 kHz		55		dB
PGA INPUT	PGA_ENx = 1, PGA_x_BOOST = 0				
Full-Scale Input Voltage	Scales linearly with AVDD		AVDD/3.3		V rms
	AVDD = 1.8 V		0.55		V rms
	AVDD = 1.8 V		1.54		V p-p
	AVDD = 3.3 V		1.00		V rms
	AVDD = 3.3 V		2.83		V p-p
Dynamic Range[1]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		94		dB
	AVDD = 3.3 V		102		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V		92		dB
	AVDD = 3.3 V		98		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
THD + N	20 Hz to 20 kHz, −1 dB from full-scale input				
	AVDD = 1.8 V		−88		dB
	AVDD = 3.3 V		−90		dB
SNR[2]					
With A-Weighted Filter (RMS)	AVDD = 1.8 V		94		dB
	AVDD = 3.3 V		102		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V		93		dB
	AVDD = 3.3 V		98		dB
PGA Gain Variation	Standard deviation				
With −12 dB Setting			0.05		dB
With +35.25 dB Setting			0.15		dB
PGA Boost	PGA_x_BOOST		10		dB
PGA Mute Attenuation	PGA_MUTEx		−63		dB
Interchannel Gain Mismatch			0.04		dB
Offset Error		−0.12		+0.12	mV
Gain Error			−0.05		dB
Interchannel Isolation			100		dB
PSRR	CM capacitor = 20 µF, 100 mV p-p at 1 kHz		63		dB
MICROPHONE BIAS	MIC_ENx = 1				
Bias Voltage					
0.65 × AVDD	AVDD = 1.8 V, MIC_GAINx = 1	1.14	1.16	1.17	V
	AVDD = 3.3 V, MIC_GAINx = 1	2.10	2.12	2.14	V
0.90 × AVDD	AVDD = 1.8 V, MIC_GAINx = 0	1.61	1.63	1.65	V
	AVDD = 3.3 V, MIC_GAINx = 0	2.95	2.97	2.99	V
Bias Current Source				3	mA
Output Impedance			1		Ω
MICBIASx Isolation	MIC_GAINx = 0		95		dB
	MIC_GAINx = 1		99		dB
Noise in the Signal Bandwidth	20 Hz to 20 kHz, 4.7 µF decoupling capacitor, 5.0 kΩ load on the MICBIASx pins				
AVDD = 1.8 V	MIC_GAINx = 0		27		nV/√Hz
	MIC_GAINx = 1		16		nV/√Hz
AVDD = 3.3 V	MIC_GAINx = 0		35		nV/√Hz
	MIC_GAINx = 1		19		nV/√Hz
DIGITAL-TO-ANALOG CONVERTERS (DACs)					
Resolution	All DACs		24		Bits
Digital Attenuation Step			0.375		dB
Digital Attenuation Range			95		dB
DAC SINGLE-ENDED OUTPUT	Single-ended operation, HPOUTLP/LOUTLP and HPOUTRP/LOUTRP pins				
Full-Scale Output Voltage	Scales linearly with AVDD		AVDD/3.4		V rms
	AVDD = 1.8 V		0.53		V rms
	AVDD = 1.8 V		1.5		V p-p
	AVDD = 3.3 V		0.97		V rms
	AVDD = 3.3 V		2.74		V p-p
Mute Attenuation			−72		dB
Line Output Mode					
Dynamic Range[1]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V	97	100		dB
	AVDD = 3.3 V	102	104		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V	95	97		dB
	AVDD = 3.3 V	99	101		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SNR[2]	20 Hz to 20 kHz				
With A-Weighted Filter (RMS)	AVDD = 1.8 V	98	100		dB
	AVDD = 3.3 V	102	104		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V	96	98		dB
	AVDD = 3.3 V	99	102		dB
Interchannel Gain Mismatch		0	50	200	mdB
THD + N	20 Hz to 20 kHz, −1 dBFS input				dB
	AVDD = 1.8 V		−93	−89	dB
	AVDD = 3.3 V		−94	−90	dB
Gain Error		−0.13		+0.13	dB
Headphone Mode					
Dynamic Range[1]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V	97	100		dB
	AVDD = 3.3 V	102	104		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V	95	97		dB
	AVDD = 3.3 V	99	101		dB
SNR[2]	20 Hz to 20 kHz				
With A-Weighted Filter (RMS)	AVDD = 1.8 V	98	100		dB
	AVDD = 3.3 V	102	104		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V	96	98		dB
	AVDD = 3.3 V	100	102		dB
Interchannel Gain Mismatch		0	50	230	mdB
THD + N	20 Hz to 20 kHz, −1 dBFS input				
32 Ω Load	AVDD = 1.8 V, output power = 6.3 mW		−79	−67	dB
	AVDD = 3.3 V, output power = 20.5 mW		−84	−67	dB
24 Ω Load	AVDD = 1.8 V, output power = 8.4 mW		−79	−65	dB
	AVDD = 3.3 V, output power = 27 mW		−80	−64	dB
16 Ω Load	AVDD = 1.8 V, output power = 13 mW		−74	−61	dB
	AVDD = 3.3 V, output power = 30 mW		−77	−67	dB
Gain Error		−0.13		+0.13	dB
Headphone Output Power					
32 Ω Load	AVDD = 1.8 V, <0.1% THD + N		8.0		mW
	AVDD = 3.3 V, <0.1% THD + N		28.1		mW
24 Ω Load	AVDD = 1.8 V, <0.1% THD + N		11.1		mW
	AVDD = 3.3 V, <0.1% THD + N		30.5		mW
16 Ω Load	AVDD = 1.8 V, <0.1% THD + N		16.5		mW
	AVDD = 3.3 V, <0.1% THD + N		32.7		mW
Offset Error		−0.11		+0.09	mV
Interchannel Isolation	1 kHz, 0 dBFS input signal		100		dB
PSRR	CM capacitor = 22 µF, 100 mV p-p at 1 kHz		70		dB
DAC DIFFERENTIAL OUTPUT	Differential operation				
Full-Scale Output Voltage	Scales linearly with AVDD		AVDD/1.7		V rms
	AVDD = 1.8 V		1.06		V rms
	AVDD = 1.8 V		3.00		V p-p
	AVDD = 3.3 V		1.94		V rms
	AVDD = 3.3 V		5.49		V p-p
Mute Attenuation			−72		dB
Line Output Mode					
Dynamic Range[1]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V	102	105		dB
	AVDD = 3.3 V	105	107		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V	100	102		dB
	AVDD = 3.3 V	102	105		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SNR[2]	20 Hz to 20 kHz				
With A-Weighted Filter (RMS)	AVDD = 1.8 V	103	105		dB
	AVDD = 3.3 V	106	108		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V	100	102		dB
	AVDD = 3.3 V	103	105		dB
Interchannel Gain Mismatch		0	50	200	mdB
THD + N	20 Hz to 20 kHz, −1 dBFS input				dB
	AVDD = 1.8 V		−96	−90	dB
	AVDD = 3.3 V		−96	−90	dB
Gain Error		−0.1		+0.16	dB
Headphone Mode					
Dynamic Range[1]	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V	102	105		dB
	AVDD = 3.3 V	105	107		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V	100	102		dB
	AVDD = 3.3 V	102	104		dB
SNR[2]	20 Hz to 20 kHz				
With A-Weighted Filter (RMS)	AVDD = 1.8 V	103	106		dB
	AVDD = 3.3 V	106	108		dB
With Flat 20 Hz to 20 kHz Filter	AVDD = 1.8 V	101	103		dB
	AVDD = 3.3 V	104	106		dB
Interchannel Gain Mismatch		0	75	370	mdB
THD + N					
32 Ω Load	−1 dBFS, AVDD = 1.8 V, output power = 26 mW		−75	−64	dB
	−1 dBFS, AVDD = 3.3 V, output power = 87 mW		−83	−75	dB
24 Ω Load	−2 dBFS, AVDD = 1.8 V, output power = 27 mW		−75	−64	dB
	−1 dBFS, AVDD = 3.3 V, output power = 115 mW		−82	−75	dB
16 Ω Load	−3 dBFS, AVDD = 1.8 V, output power = 32 mW		−75	−65	dB
	−1 dBFS, AVDD = 3.3 V, output power = 168 mW		−77	−68	dB
Gain Error	Headphone mode	−0.25		+0.25	dB
Headphone Output Power					
32 Ω Load	AVDD = 1.8 V, <0.1% THD + N		29.1		mW
	AVDD = 3.3 V, <0.1% THD + N		111.8		mW
24 Ω Load	AVDD = 1.8 V, <0.1% THD + N		31.8		mW
	AVDD = 3.3 V, <0.1% THD + N		148.3		mW
16 Ω Load	AVDD = 1.8 V, <0.1% THD + N		32.3		mW
	AVDD = 3.3 V, <0.1% THD + N		193.0		mW
Offset Error		−0.12	0	+0.08	mV
Interchannel Isolation	1 kHz, 0 dBFS input signal		100		dB
PSRR	CM capacitor = 22 µF, 100 mV p-p at 1 kHz		73		dB
ANALOG-TO-ANALOG LATENCY	f_S = 768 kHz		5		µs
	f_S = 192 kHz		38		µs
CM REFERENCE	CM pin				
Common-Mode Reference Output			AVDD/2		V
Common-Mode Source Impedance			5		kΩ
REGULATOR					
Line Regulation			1		mV/V
Load Regulation			6		mV/mA

[1] Dynamic range is the ratio of the sum of the noise and harmonic power in the band of interest with a −60 dBFS signal present vs. the full-scale power level in decibels.
[2] SNR is the ratio of the sum of all noise power in the band of interest with no signal present vs. the full-scale power level in decibels.

CRYSTAL AMPLIFIER SPECIFICATIONS

AVDD = IOVDD = 1.8 V, DVDD = 1.1 V, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
CRYSTAL AMPLIFIER				
Jitter		270	500	ps rms
Frequency Range	8		27	MHz
Load Capacitance			20	pF

DIGITAL INPUT/OUTPUT SPECIFICATIONS

−40°C < T_A < +85°C, IOVDD = 3.3 V ± 10% and 1.8 V − 5% to 1.8 V + 10%, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT/OUTPUT					
Input Voltage					
High (V_{IH})	IOVDD = 3.3 V	2.0			V
	IOVDD = 1.8 V	1.1			V
Low (V_{IL})	IOVDD = 3.3 V			0.8	V
	IOVDD = 1.8 V			0.45	V
Input Leakage	IOVDD = 3.3 V, I_{IH}[1] at V_{IH} = 2.0 V			10	µA
	I_{IL}[1] at V_{IL} = 0.8 V			10	µA
	IOVDD = 1.8 V, I_{IH}[1] at V_{IH} = 1.1 V			10	µA
	I_{IL}[1] at V_{IL} = 0.45 V			10	µA
Output Voltage High (V_{OH})					
Low Drive Strength	I_{OH}[1] = 1 mA	IOVDD − 0.6			V
High Drive Strength	I_{OH}[1] = 3 mA	IOVDD − 0.6			V
Output Voltage Low (V_{OL})					
Low Drive Strength	I_{OL}[1] = 1 mA			0.4	V
High Drive Strength	I_{OL}[1] = 3 mA			0.4	V
Input Capacitance				5	pF

[1] I_{IH} is the current when the input is high; I_{IL} is the current when the input is low; I_{OH} is the current when the output is high; and I_{OL} is the current when the output is low.

POWER SUPPLY SPECIFICATIONS

AVDD = IOVDD = 1.8 V, DVDD = 1.1 V, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLIES					
AVDD Voltage		1.71	1.8	3.63	V
DVDD Voltage		1.045	1.1	1.98	V
IOVDD Voltage		1.71	1.8	3.63	V
Analog Current (I_{AVDD})					
Normal Operation	See Table 5				
Power-Down			1.6		µA
Digital Input/Output Current (I_{IOVDD})					
Normal Operation	See Table 5				
Power-Down			1.3		µA
POWER CONSUMPTION					
All Supplies	See Table 5				
Power-Down, All Supplies			1		µW

TYPICAL POWER MANAGEMENT SETTINGS

Typical ANC settings, master clock = 12.288 MHz, PLL disabled, crystal oscillator enabled, core f_S = DAC = ADC = 768 kHz. On-board regulator enabled. Two ADCs with PGA enabled and two ADCs configured for line input, no input signal. Two DACs are configured for differential headphone (HP) operation; DAC outputs are unloaded. Both MICBIAS0 and MICBIAS1 enabled at 0.9 × AVDD. ASRCs and pulse density modulation (PDM) modulator disabled. Core running 26 out of 32 possible instructions. Serial port set to slave. See Register 0x46 and Register 0x47 for settings.

Table 5.

Operating Voltage	Power Management Setting	Typical AVDD Current Consumption (mA)	Typical IOVDD Current Consumption (mA)	Typical ADC THD + N (dB)	Typical HP Output THD + N (dB)	Total Power Consumption (mW)
AVDD = IOVDD = 3.3 V	Normal	9.71	2.58	−91	−97	40.56
	Extreme power saving	7.55	2.57	−86	−96	33.40
	Power saving	7.99	2.57	−87	−96	34.85
	Enhanced performance	10.97	2.58	−91	−98	44.72
AVDD = IOVDD = 1.8 V	Normal	7.29	0.37	−87	−95	13.79
	Extreme power saving	5.38	0.37	−81	−89	10.35
	Power saving	5.73	0.37	−81	−90	10.98
	Enhanced Performance	8.62	0.37	−87	−95	16.18

DIGITAL FILTERS SPECIFICATIONS

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC INPUT TO DAC OUTPUT PATH					
Pass-Band Ripple	DC to 20 kHz, f_S = 768 kHz	−0.03		+0.01	dB
	DC to 20 kHz, f_S = 192 kHz			±0.02	dB
SAMPLE RATE CONVERTER					
Pass Band	LRCLK < 63 kHz	0		0.475 × f_S	kHz
	63 kHz < LRCLK <130 kHz	0		0.4286 × f_S	kHz
	LRCLK > 130 kHz	0		0.4286 × f_S	kHz
Pass-Band Ripple	Upsampling, 96 kHz	−0.27		+0.05	dB
	Upsampling, 192 kHz	−0.06		+0.05	dB
	Downsampling, 96 kHz	0		0.07	dB
	Downsampling, 192 kHz	0		0.07	dB
Input/Output Frequency Range		8		192	kHz
Dynamic Range			100		dB
THD + N			−90		dB
Start-Up Time				15	ms
PDM MODULATOR					
Dynamic Range (A-Weighted)			112		dB
THD + N			−92		dB

DIGITAL TIMING SPECIFICATIONS

−40°C < T_A < +85°C, IOVDD = 1.71 V to 3.63 V, DVDD = 1.045 V to 1.98 V.

Table 7. Digital Timing

	Limit			
Parameter	**t_{MIN}**	**t_{MAX}**	**Unit**	**Description**
MASTER CLOCK (MCLK)				
t_{MP}	37	125	ns	MCLKIN period; 8 MHz to 27 MHz input clock using PLL
t_{MCLK}	77	82	ns	Internal MCLK period; direct MCLK and PLL output divided by 2
SERIAL PORT				
t_{BL}	40		ns	BCLK low pulse width (master and slave modes)
t_{BH}	40		ns	BCLK high pulse width (master and slave modes)
t_{LS}	10		ns	LRCLK setup; time to BCLK rising (slave mode)
t_{LH}	10		ns	LRCLK hold; time from BCLK rising (slave mode)
t_{SS}	5		ns	DAC_SDATA setup; time to BCLK rising (master and slave modes)
t_{SH}	5		ns	DAC_SDATA hold; time from BCLK rising (master and slave modes)
t_{TS}		10	ns	BCLK falling to LRCLK timing skew (master mode)
t_{SOD}	0	34	ns	ADC_SDATAx delay; time from BCLK falling (master and slave modes)
t_{SOTD}		30	ns	BCLK falling to ADC_SDATAx driven in time-division multiplexing (TDM) tristate mode
t_{SOTX}		30	ns	BCLK falling to ADC_SDATAx tristate in TDM tristate mode
SERIRAL PERIPHERAL INTERFACE (SPI) PORT				
f_{SCLK}		6.25	MHz	SCLK frequency
t_{CCPL}	80		ns	SCLK pulse width low
t_{CCPH}	80		ns	SCLK pulse width high
t_{CLS}	5		ns	$\overline{SS}$ setup; time to SCLK rising
t_{CLH}	100		ns	$\overline{SS}$ hold; time from SCLK rising
t_{CLPH}	80		ns	$\overline{SS}$ pulse width high
t_{CDS}	10		ns	MOSI setup; time to SCLK rising
t_{CDH}	10		ns	MOSI hold; time from SCLK rising
t_{COD}		101	ns	MISO delay; time from SCLK falling
I²C PORT				
f_{SCL}		400	kHz	SCL frequency
t_{SCLH}	0.6		µs	SCL high
t_{SCLL}	1.3		µs	SCL low
t_{SCS}	0.6		µs	SCL rise setup time (to SDA falling), relevant for repeated start condition
t_{SCR}		250	ns	SCL and SDA rise time, C_{LOAD} = 400 pF
t_{SCH}	0.6		µs	SCL fall hold time (from SDA falling), relevant for start condition
t_{DS}	100		ns	SDA setup time (to SCL rising)
t_{SCF}		250	ns	SCL and SDA fall time; C_{LOAD} = 400 pF
t_{BFT}	0.6		µs	SCL rise setup time (to SDA rising), relevant for stop condition
I²C EEPROM SELF BOOT				
t_{SCHE}	$26 \times t_{MP} - 70$		ns	SCL fall hold time (from SDA falling), relevant for start condition; t_{MP} is the input clock on the MCLKIN pin
t_{SCSE}	$38 \times t_{MP} - 70$		ns	SCL rise setup time (to SDA falling), relevant for repeated start condition
t_{BFTE}	$70 \times t_{MP} - 70$		ns	SCL rise setup time (to SDA rising), relevant for stop condition
t_{DSE}	$6 \times t_{MP} - 70$		ns	Delay from SCL falling to SDA changing
t_{BHTE}	$32 \times t_{MP}$		ns	SDA rising in self boot stop condition to SDA falling edge for external master start condition

Parameter	Limit t_{MIN}	Limit t_{MAX}	Unit	Description
MULTIPURPOSE AND POWER-DOWN PINS				
t_{GIL}		1.5 × 1/f_S	µs	MPx input latency; time until high or low value is read by core
t_{RLPW}	20		ns	$\overline{PD}$ low pulse width
DIGITAL MICROPHONE				
t_{CF}		20	ns	Digital microphone clock fall time
t_{CR}		20	ns	Digital microphone clock rise time
t_{DS}	40			Digital microphone valid data start time
t_{DE}		0	ns	Digital microphone valid data end time
PDM OUTPUT				
t_{DCF}		20	ns	PDM clock fall time
t_{DCR}		20	ns	PDM clock rise time
t_{DDV}	0	30	ns	PDM delay time for valid data

Digital Timing Diagrams

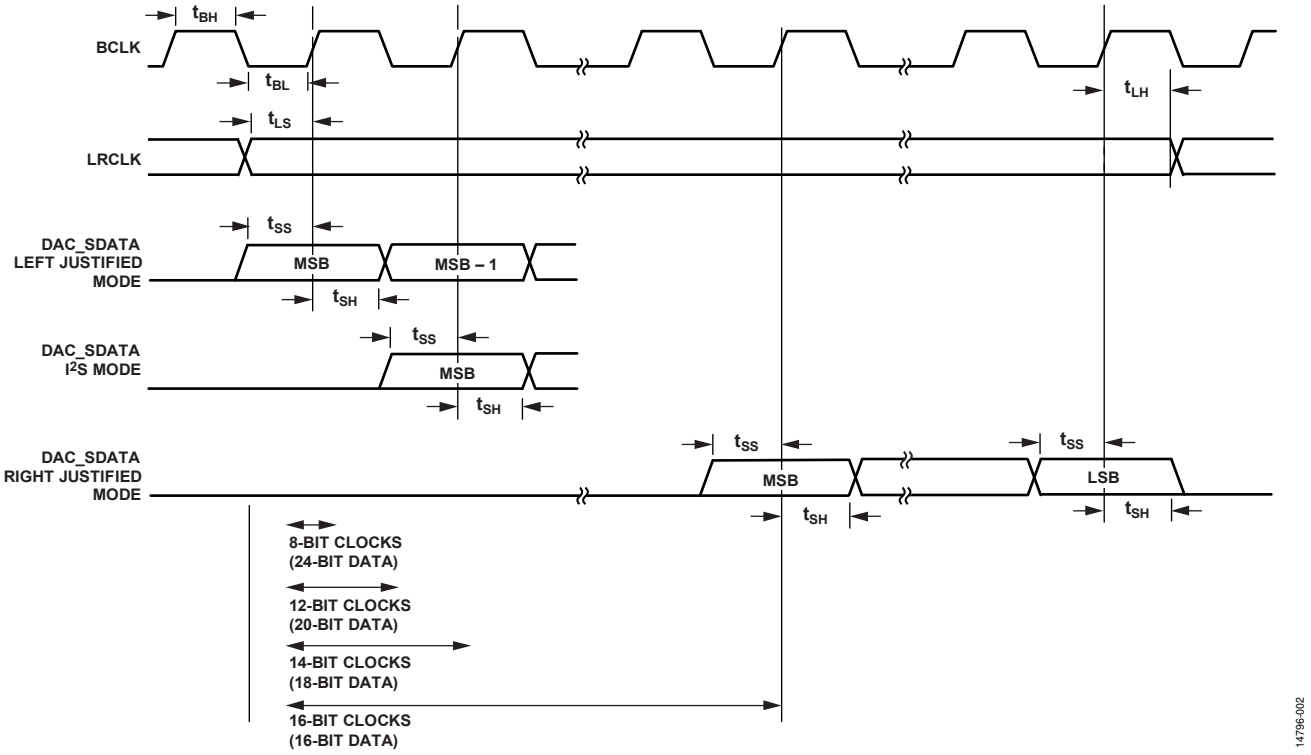

Figure 2. Serial Input Port Timing

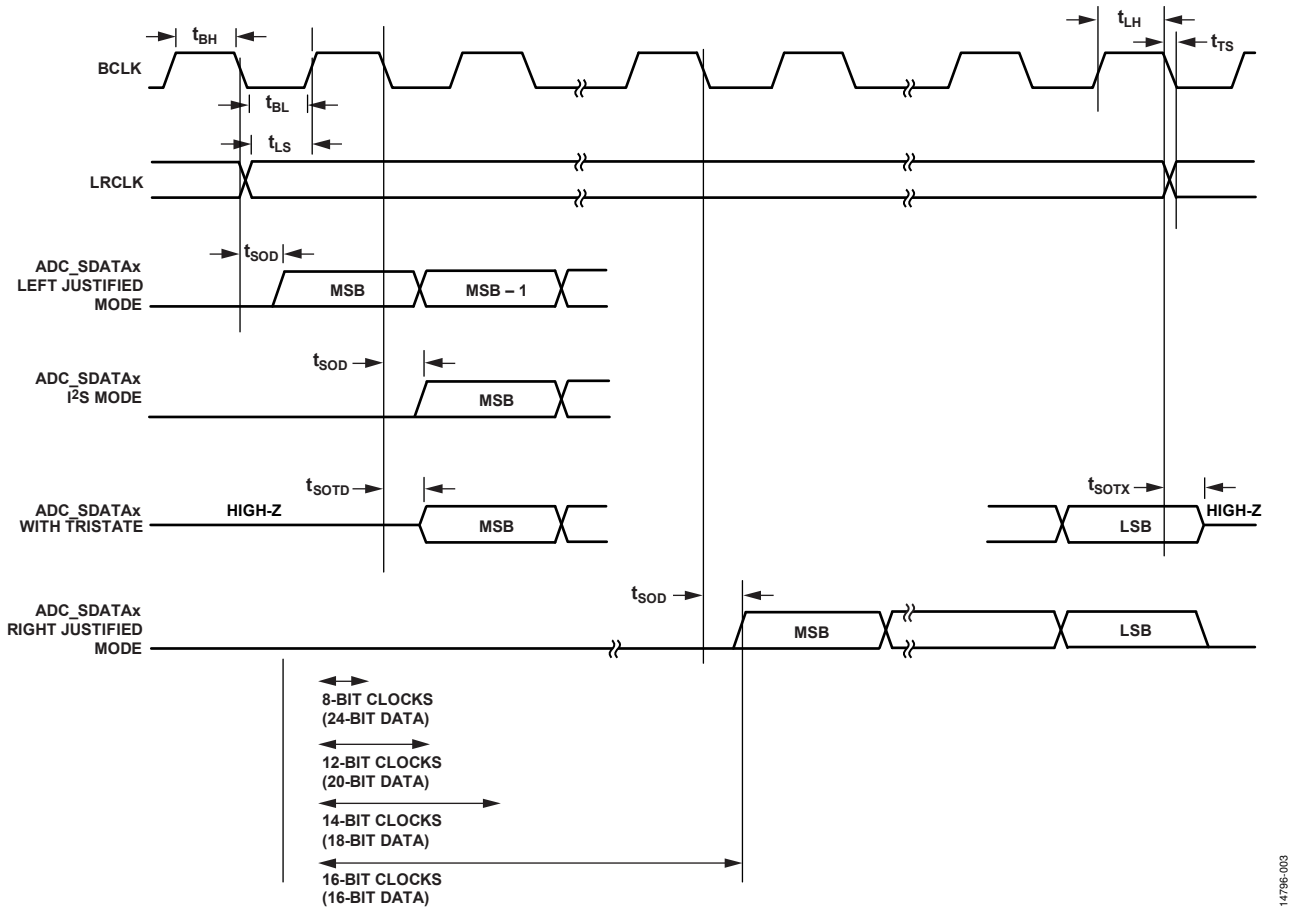

Figure 3. Serial Output Port Timing

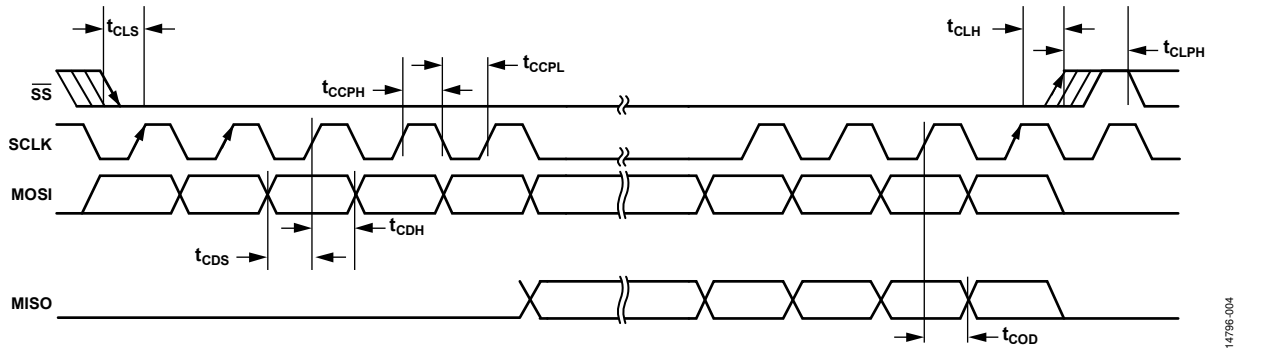

Figure 4. SPI Port Timing

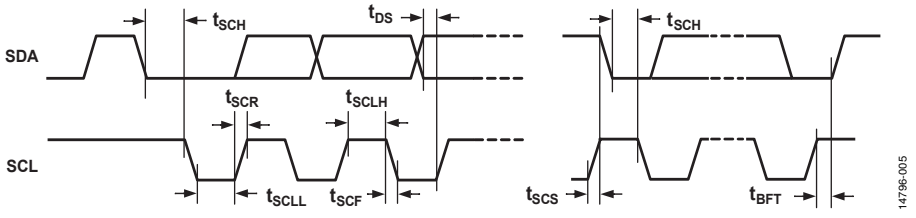

Figure 5. I²C Port Timing

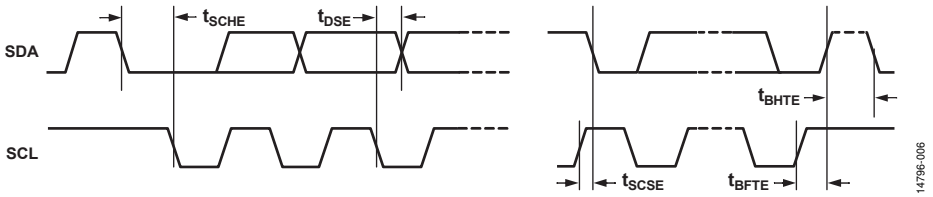

Figure 6. I²C EEPROM Self Boot Timing

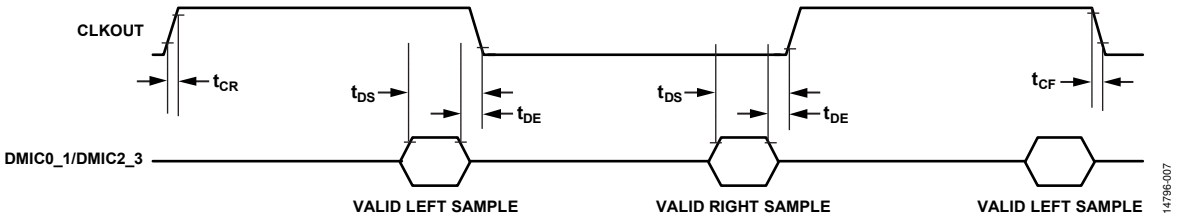

Figure 7. Digital Microphone Timing

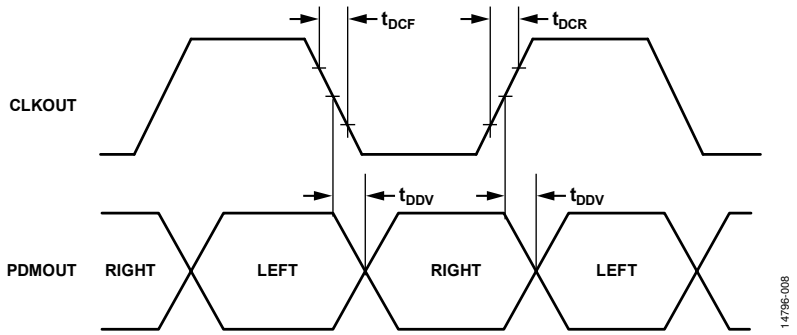

Figure 8. PDM Output Timing

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Power Supplies (AVDD, IOVDD)	−0.3 V to +3.63 V
Digital Supply (DVDD)	−0.3 V to +1.98 V
Input Current (Except Supply Pins)	±20 mA
Analog Input Voltage (Signal Pins)	−0.3 V to AVDD + 0.3 V
Digital Input Voltage (Signal Pins)	−0.3 to IOVDD + 0.3 V
Operating Temperature Range (Case)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure

For more information, see the AN-617 Application Note, *Wafer Level Chip Scale Package*.

Table 9. Thermal Resistance

Package Type	θ_{JA}	Unit
CB-36-4[1]	36	°C/W

[1] Thermal impedance simulated values are based on a 4-layer PCB with two signal layers and two power planes using natural convection cooling. See JEDEC JESD51-9.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

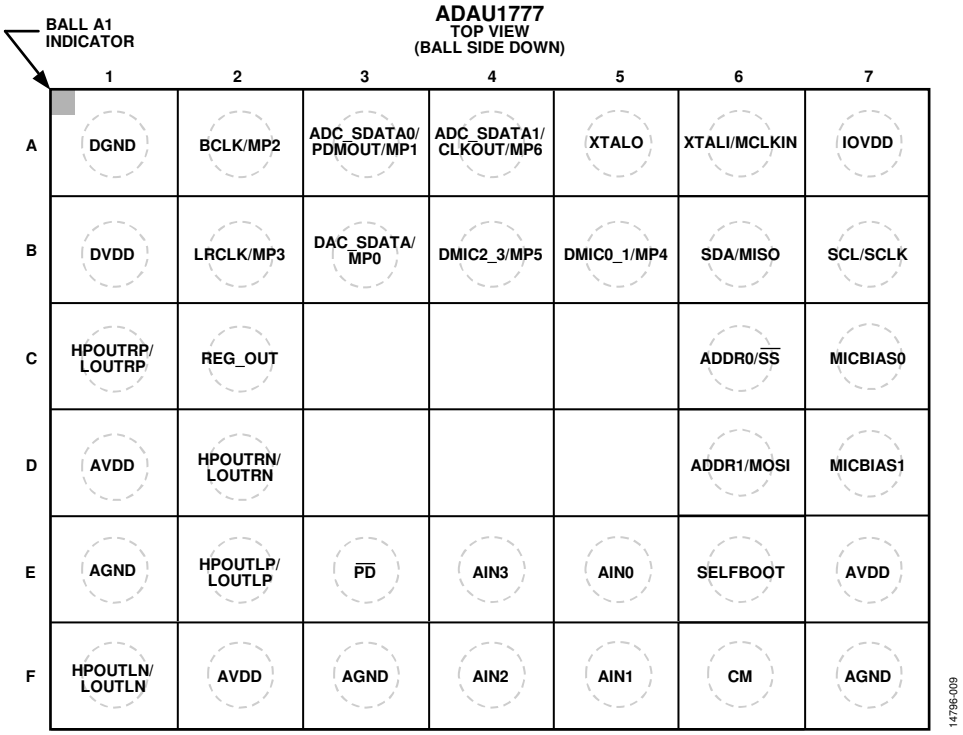

Figure 9. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1	DGND	PWR	Digital Ground. Tie the AGND and DGND pins directly together in a common ground plane.
A2	BCLK/MP2	D_IO	Serial Data Port Bit Clock (BCLK). Multipurpose Pin (MP2).
A3	ADC_SDATA0/PDMOUT/MP1	D_IO	ADC Serial Data Output 0 (ADC_SDATA0). Stereo PDM Output to Drive a High Efficiency Class-D Amplifier (PDMOUT). Multipurpose Pin (MP1).
A4	ADC_SDATA1/CLKOUT/MP6	D_IO	Serial Data Output 1 (ADC_SDATA1). Master Clock Output/Clock for the Digital Microphone Input and PDM Output (CLKOUT). Multipurpose Pin (MP6).
A5	XTALO	A_OUT	Crystal Clock Output. This pin is the output of the crystal amplifier; do not use this pin to provide a clock to other ICs in the system. If a master clock output is needed, use CLKOUT (Pin A4).
A6	XTALI/MCLKIN	D_IN	Crystal Clock Input (XTALI). Master Clock Input (MCLKIN).
A7	IOVDD	PWR	Supply for Digital Input and Output Pins. The digital output pins are supplied from IOVDD; thus, the IOVDD voltage level is the highest input voltage that can be present on the digital input pins. The current draw of this pin is variable because it is dependent on the loads of the digital outputs. Decouple IOVDD to DGND with a 0.1 µF capacitor.
B1	DVDD	PWR	Digital Core Supply. The digital supply can be generated from an on-board regulator or supplied directly from an external supply. In each case, decouple DVDD to DGND with a 0.1 µF capacitor.
B2	LRCLK/MP3	D_IO	Serial Data Port Frame Clock (LRCLK). Multipurpose Pin (MP3).
B3	DAC_SDATA/MP0	D_IO	DAC Serial Input Data (DAC_SDATA). Multipurpose Pin (MP0).
B4	DMIC2_3/MP5	D_IN	Digital Microphone Stereo Input 2 and Digital Microphone Stereo Input 3 (DMIC2_3). Multipurpose Pin (MP5).

Pin No.	Mnemonic	Type[1]	Description
B5	DMIC0_1/MP4	D_IN	Digital Microphone Stereo Input 0 and Digital Microphone Stereo Input 1 (DMIC0_1).
			Multipurpose Pin (MP4).
B6	SDA/MISO	D_IO	I²C Data (SDA). This pin is a bidirectional open-collector. The line connected to this pin must have a 2.0 kΩ pull-up resistor.
			SPI Data Output (MISO). This SPI data output reads back registers and memory locations. It is tristated when an SPI read is not active.
B7	SCL/SCLK	D_IN	I²C Clock (SCL). This pin is always an open-collector input when the device is in I²C control mode. When the device is in self boot mode, this pin is an open-collector output (I²C master). The line connected to this pin must have a 2.0 kΩ pull-up resistor.
			SPI Clock (SCLK). This pin either can run continuously or be gated off between SPI transactions.
C1	HPOUTRP/LOUTRP	A_OUT	Right Headphone Output Noninverted (HPOUTRP).
			Line Output Noninverted, Single-Ended Line Output (LOUTRP).
C2	REG_OUT	A_OUT	Regulator Output Voltage. Connect this pin to DVDD if the internal voltage regulator is being used to generate the DVDD voltage.
C6	ADDR0/$\overline{SS}$	D_IN	I²C Address 0 (ADDR0).
			SPI Latch Signal ($\overline{SS}$). This pin must go low at the beginning of an SPI transaction and high at the end of a transaction. Each SPI transaction can take a different number of SCLK cycles to complete, depending on the address and read/write bit that are sent at the beginning of the SPI transaction.
C7	MICBIAS0	A_OUT	Bias Voltage for Electret Microphone. Decouple this pin with a 1 µF capacitor.
D1	AVDD	PWR	Headphone Amplifier Power, 1.8 V to 3.3 V Analog Supply. Decouple this pin to AGND with a 0.1 µF capacitor. The PCB trace to this pin must have the capacity to supply the higher current necessary for driving the headphone outputs.
D2	HPOUTRN/LOUTRN	A_OUT	Right Headphone Output Inverted (HPOUTRN).
			Line Output Inverted (LOUTRN).
D6	ADDR1/MOSI	D_IN	I²C Address 1 (ADDR1).
			SPI Data Input (MOSI).
D7	MICBIAS1	A_OUT	Bias Voltage for Electret Microphone. Decouple this pin with a 1 µF capacitor.
E1	AGND	PWR	Headphone Amplifier Ground.
E2	HPOUTLP/LOUTLP	A_OUT	Left Headphone Output Noninverted (HPOUTLP).
			Line Output Noninverted, Single-Ended Line Output (LOUTLP).
E3	$\overline{PD}$	D_IN	Active Low Power-Down. All digital and analog circuits are powered down. An internal pull-down resistor is on this pin; therefore, the ADAU1777 is held in power-down mode if its input signal is floating while power is applied to the supply pins.
E4	AIN3	A_IN	ADC3 Input.
E5	AIN0	A_IN	ADC0 Input.
E6	SELFBOOT	D_IN	Self Boot Enable. Pull this pin up to IOVDD at power-up to enable the self boot mode.
E7	AVDD	PWR	1.8 V to 3.3 V Analog Supply. Decouple this pin to AGND with a 0.1 µF capacitor.
F1	HPOUTLN/LOUTLN	A_OUT	Left Headphone Output Inverted (HPOUTLN).
			Line Output Inverted (LOUTLN).
F2	AVDD	PWR	1.8 V to 3.3 V Analog Supply. Decouple this pin to AGND with a 0.1 µF capacitor.
F3	AGND	PWR	Analog Ground.
F4	AIN2	A_IN	ADC2 Input.
F5	AIN1	A_IN	ADC1 Input.
F6	CM	A_OUT	AVDD/2 V Common-Mode Reference. Connect a 10 µF to 47 µF decoupling capacitor between this pin and ground to reduce crosstalk between the ADCs and DACs. The material of the capacitors is not critical. This pin can bias external analog circuits, as long as they are not drawing current from CM (for example, the noninverting input of an op amp).
F7	AGND	PWR	Analog Ground. The AGND and DGND pins can be tied directly together in a common ground plane. Decouple AGND to AVDD with a 0.1 µF capacitor.

[1] PWR is power; D_IO is digital input/output; A_OUT is analog output; D_IN is digital input; and A_IN is analog input.

TYPICAL PERFORMANCE CHARACTERISTICS

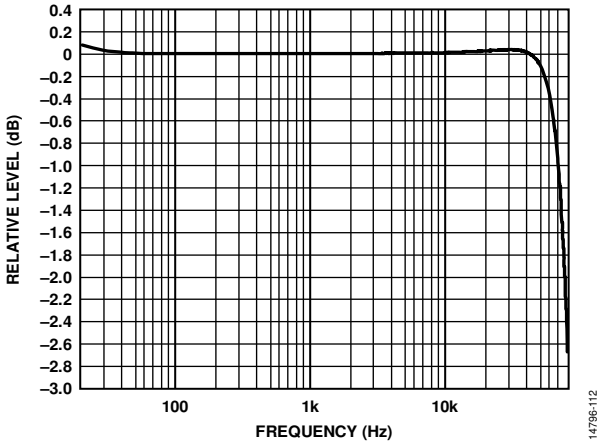

Figure 10. Relative Level vs. Frequency, f_S = 96 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx

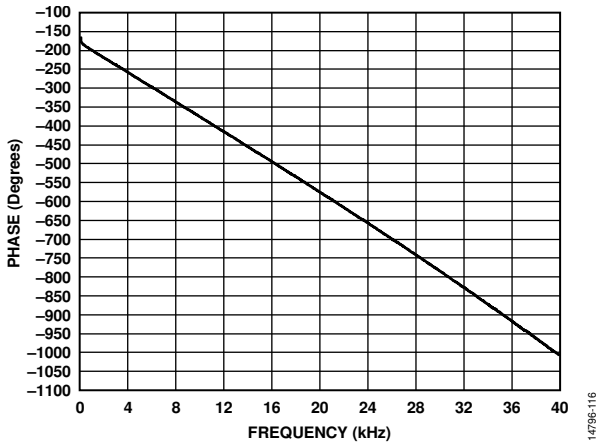

Figure 11. Phase vs. Frequency, 40 kHz Bandwidth, f_S = 96 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx

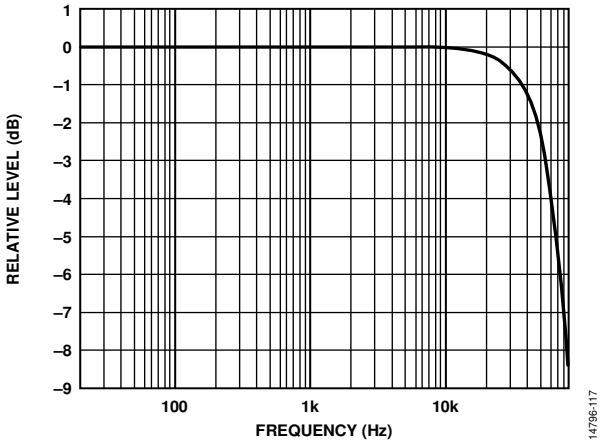

Figure 12. Relative Level vs. Frequency, f_S = 192 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx

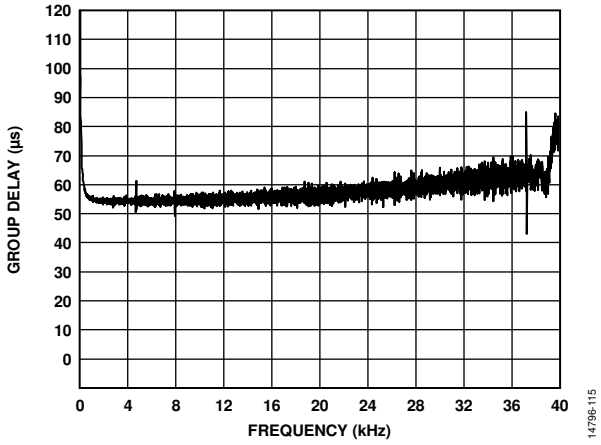

Figure 13. Group Delay vs. Frequency, f_S = 96 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx

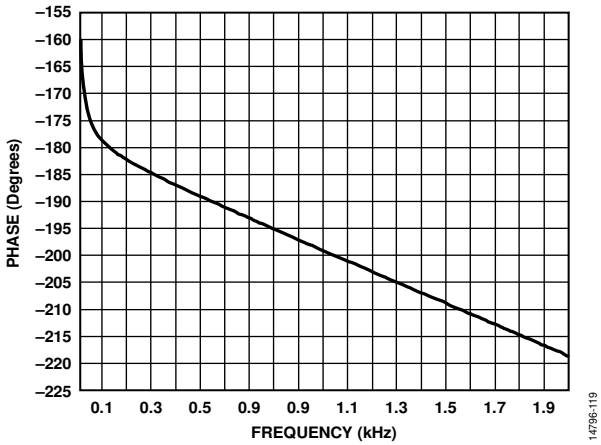

Figure 14. Phase vs. Frequency, 2 kHz Bandwidth, f_S = 96 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx

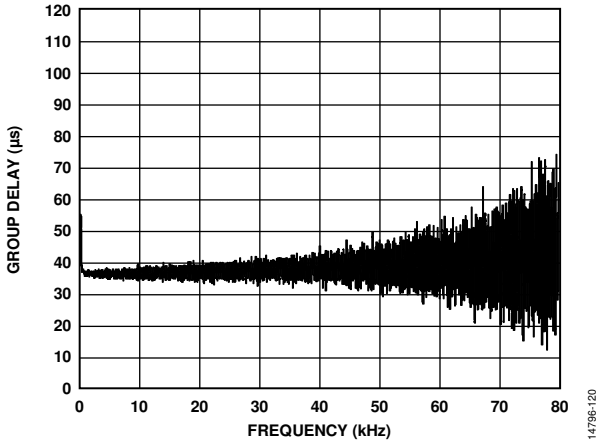

Figure 15. Group Delay vs. Frequency, f_S = 192 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx

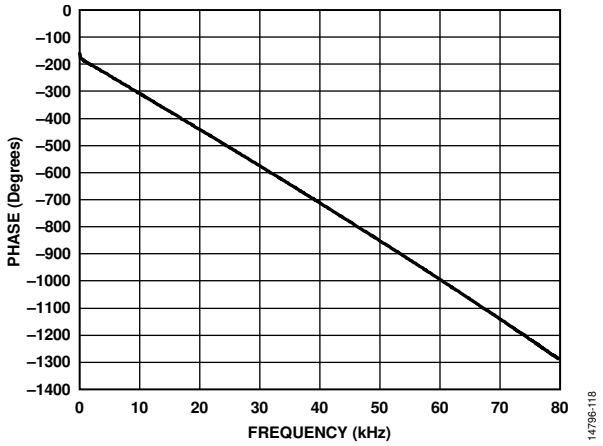

Figure 16. Phase vs. Frequency, 80 kHz Bandwidth, f_S = 192 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx

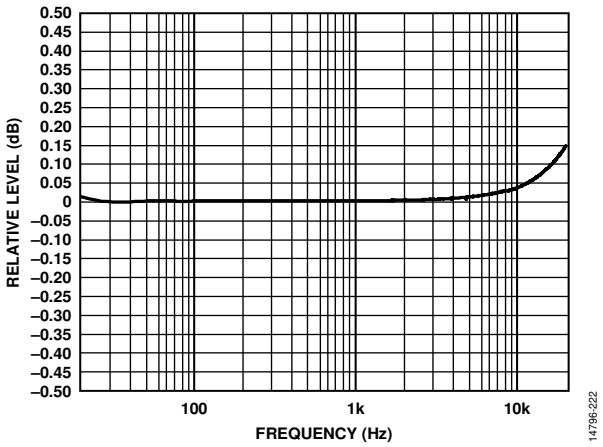

Figure 17. Relative Level vs. Frequency, f_S =768 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx

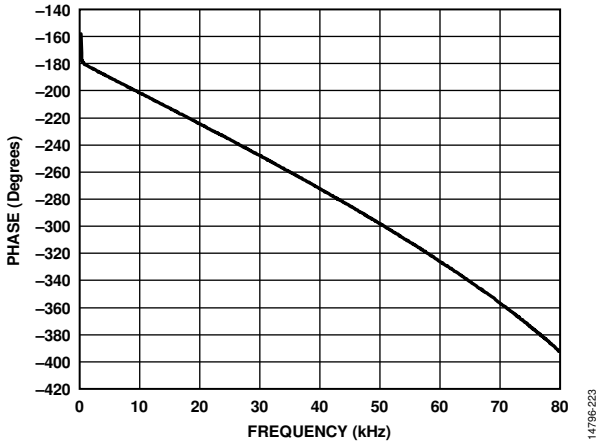

Figure 18. Phase vs. Frequency, 80 kHz Bandwidth, f_S =768 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx

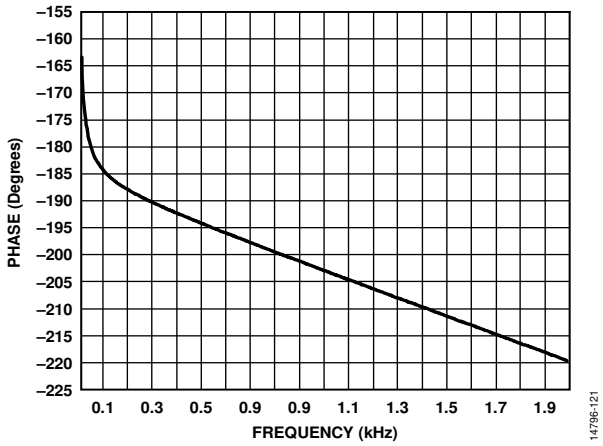

Figure 19. Phase vs. Frequency, 2 kHz Bandwidth, f_S = 192 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx

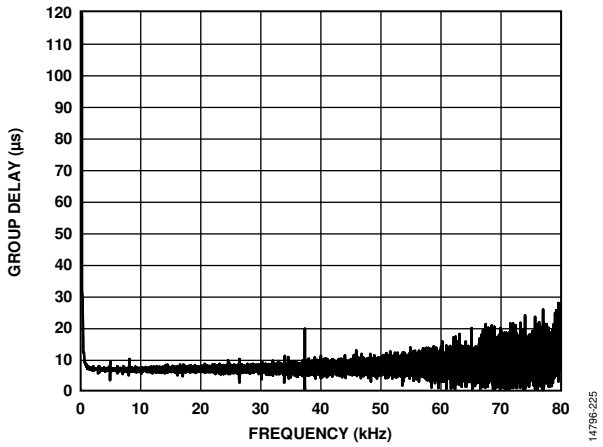

Figure 20. Group Delay vs. Frequency, f_S =768 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx

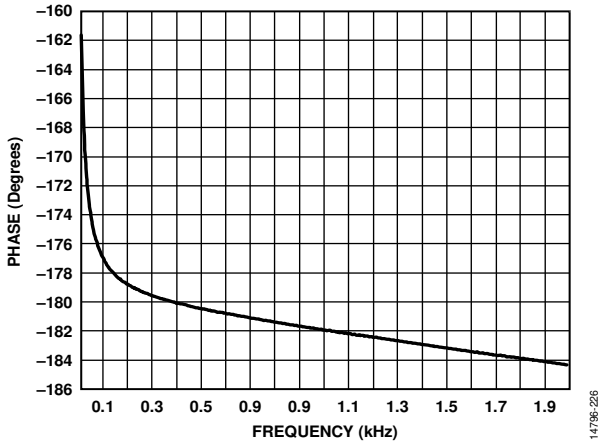

Figure 21. Phase vs. Frequency, 2 kHz Bandwidth, f_S =768 kHz, Signal Path = AIN0 to DSP (Without Processing) to LOUTLx

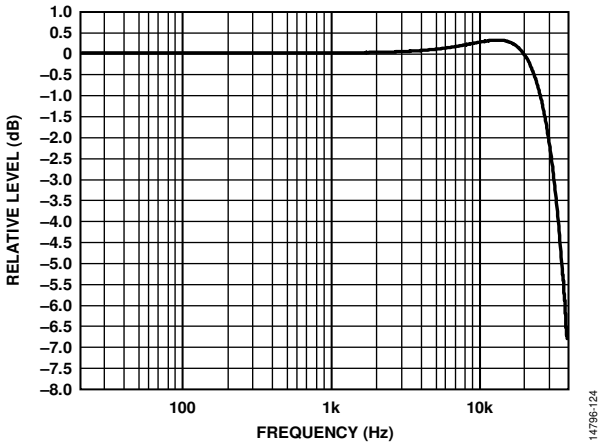

Figure 22. Relative Level vs. Frequency, f_S = 96 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

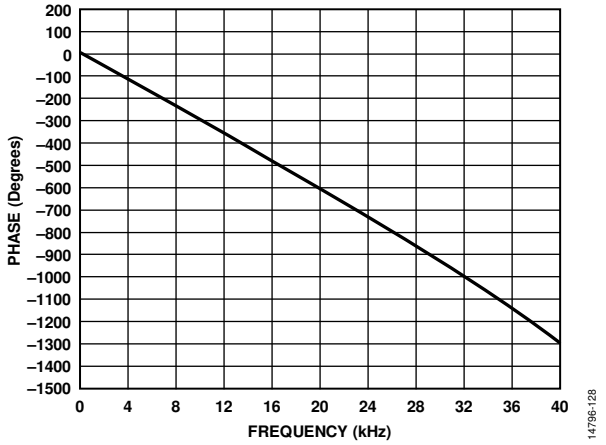

Figure 23. Phase vs. Frequency, 40 kHz Bandwidth, f_S = 96 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

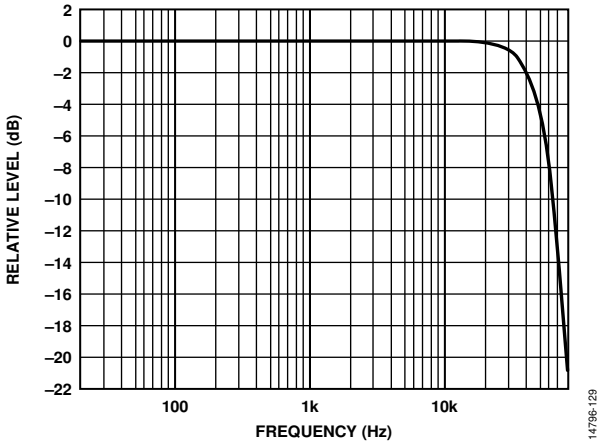

Figure 24. Relative Level vs. Frequency, f_S = 192 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

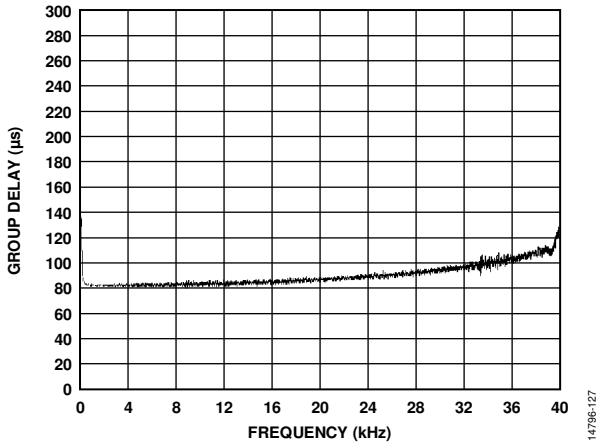

Figure 25. Group Delay vs. Frequency, f_S = 96 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

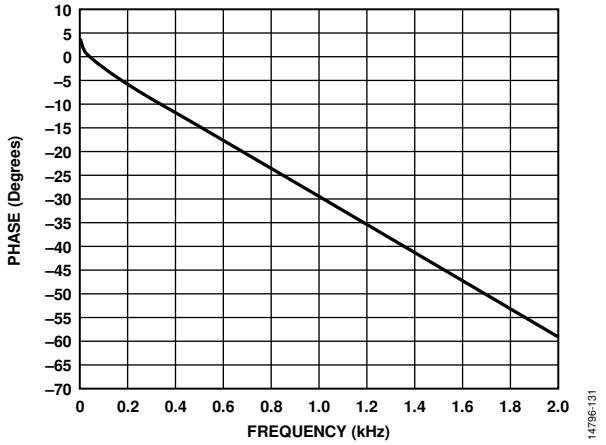

Figure 26. Phase vs. Frequency, 2 kHz Bandwidth, f_S = 96 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

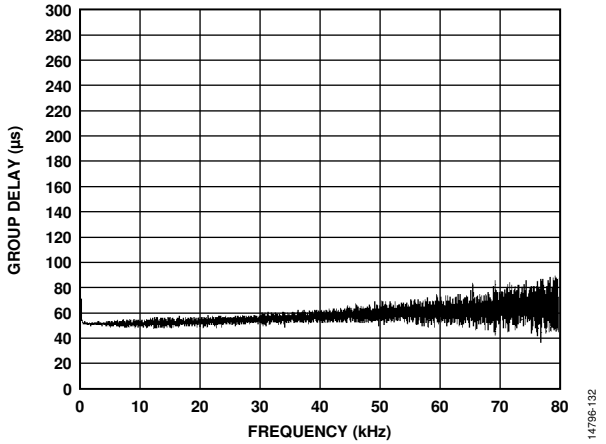

Figure 27. Group Delay vs. Frequency, f_S = 192 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

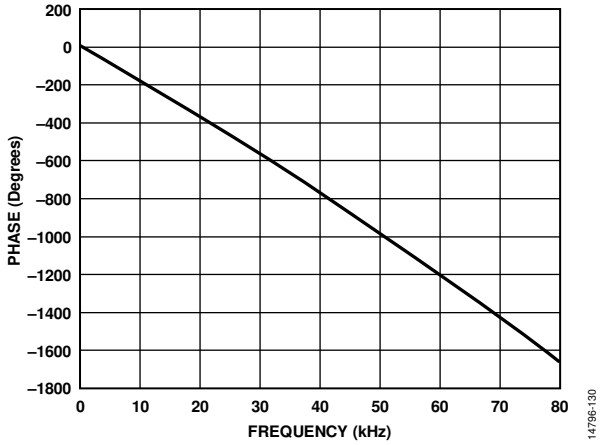

Figure 28. Phase vs. Frequency, 80 kHz Bandwidth, f_S = 192 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

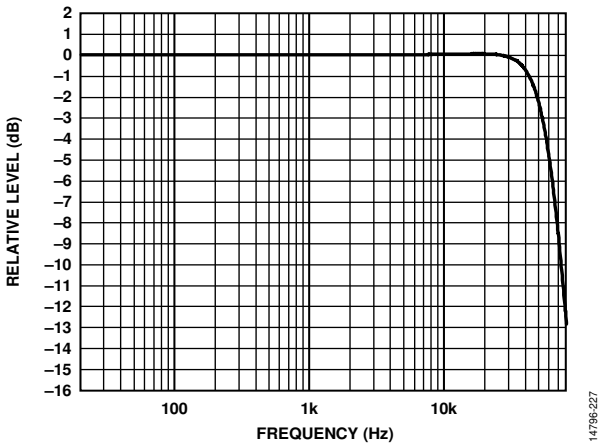

Figure 29. Relative Level vs. Frequency, f_S = 786 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

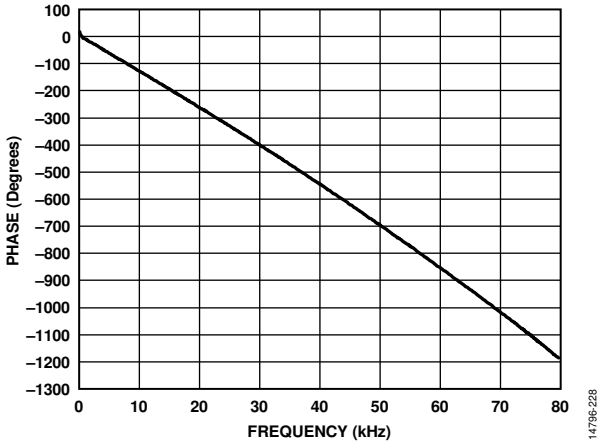

Figure 30. Phase vs. Frequency, 80 kHz Bandwidth, f_S = 786 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

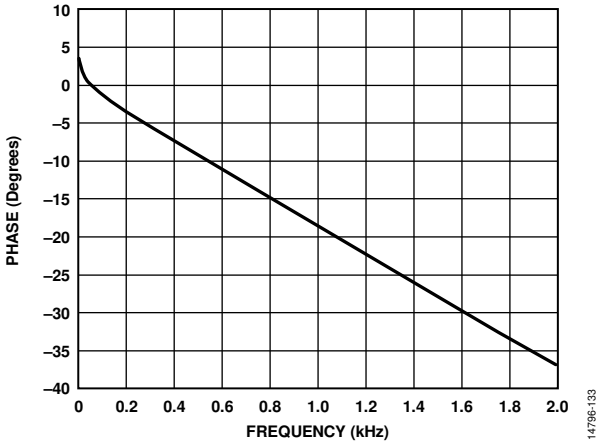

Figure 31. Phase vs. Frequency, 2 kHz Bandwidth, f_S = 192 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

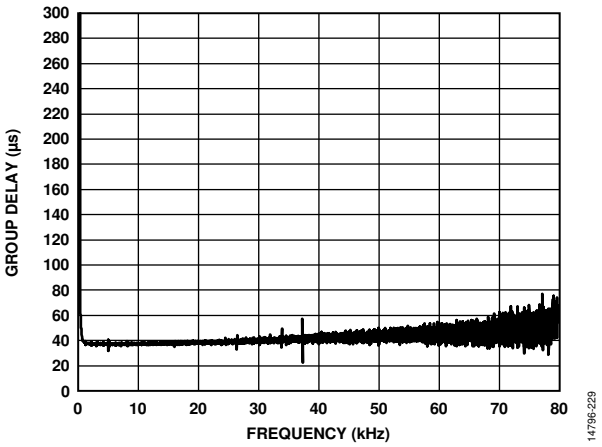

Figure 32. Group Delay vs. Frequency, f_S = 786 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

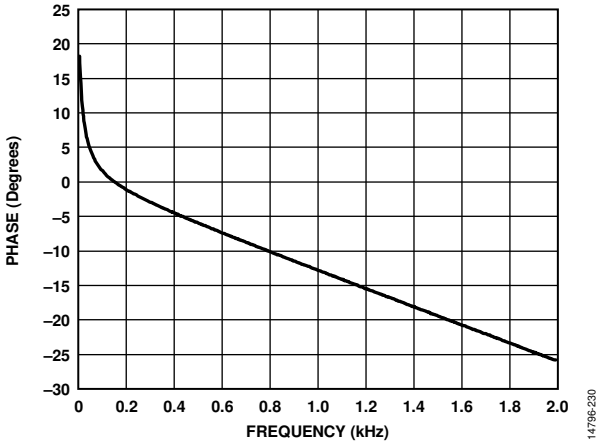

Figure 33. Phase vs. Frequency, 2 kHz Bandwidth, f_S = 786 kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

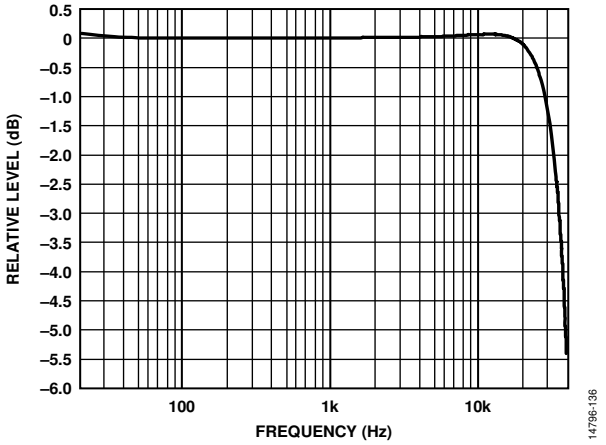

Figure 34. Relative Level vs. Frequency, f_S = 96 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

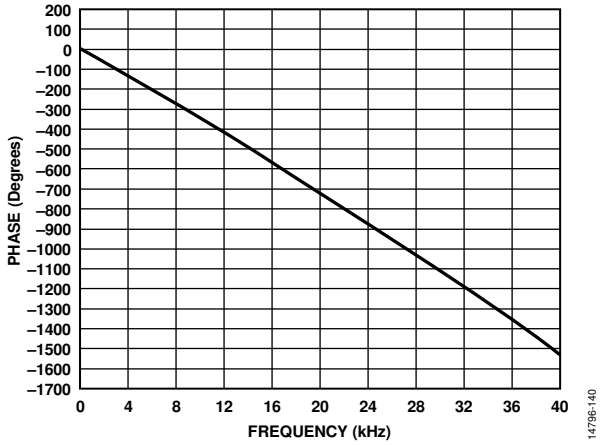

Figure 35. Phase vs. Frequency, 40 kHz Bandwidth, f_S = 96 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

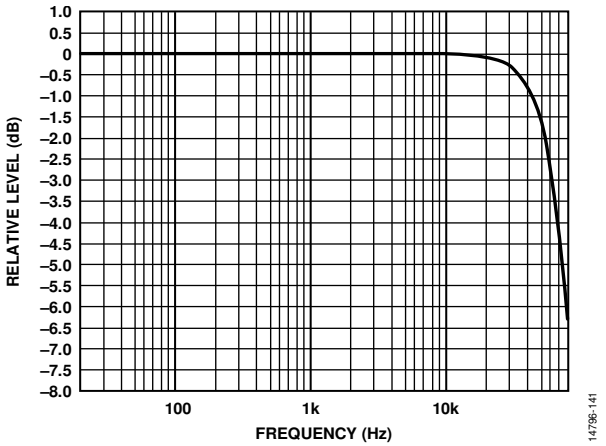

Figure 36. Relative Level vs. Frequency, f_S = 192 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

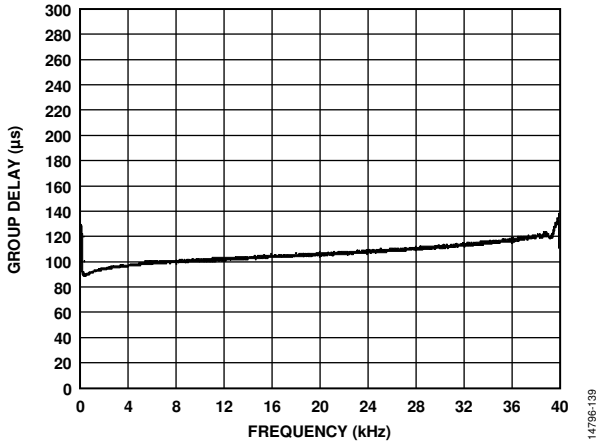

Figure 37. Group Delay vs. Frequency, f_S = 96 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

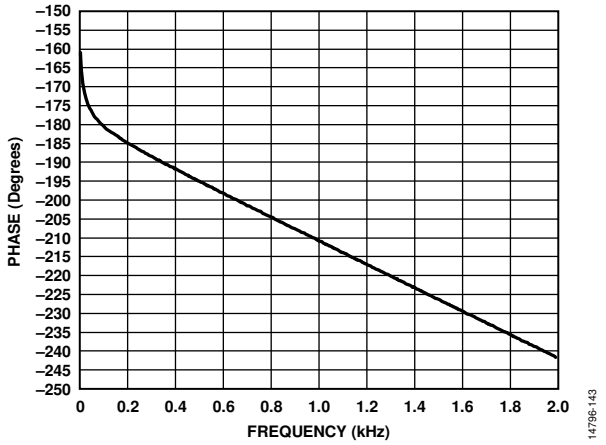

Figure 38. Phase vs. Frequency, 2 kHz Bandwidth, f_S = 96 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

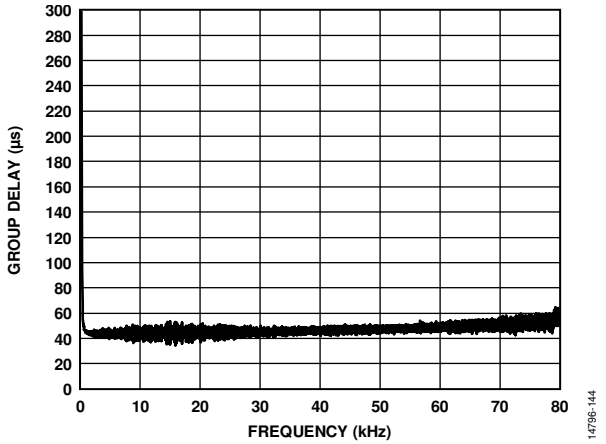

Figure 39. Group Delay vs. Frequency, f_S = 192 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

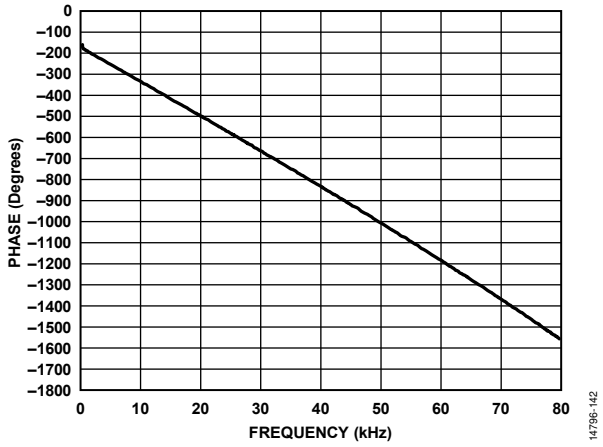

Figure 40. Phase vs. Frequency, 80 kHz Bandwidth, f_S = 192 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

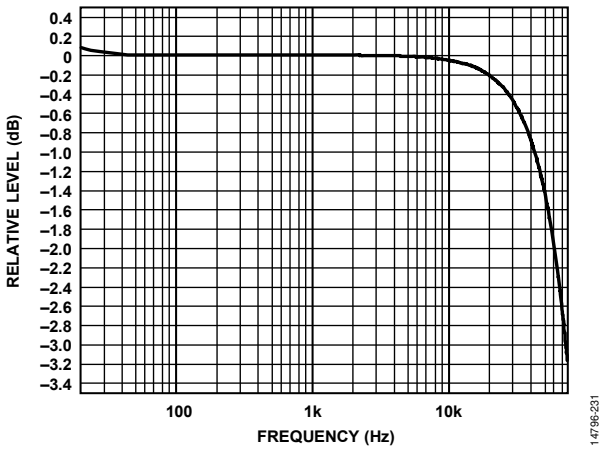

Figure 41. Relative Level vs. Frequency, f_S = 786 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

Figure 42. Phase vs. Frequency, 20 kHz Bandwidth, f_S = 786 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

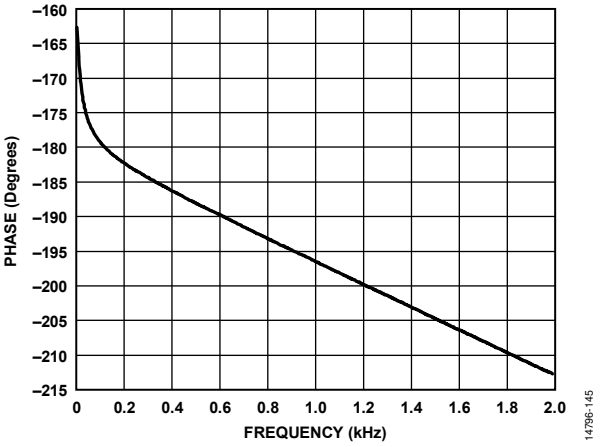

Figure 43. Phase vs. Frequency, 2 kHz Bandwidth, f_S = 192 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

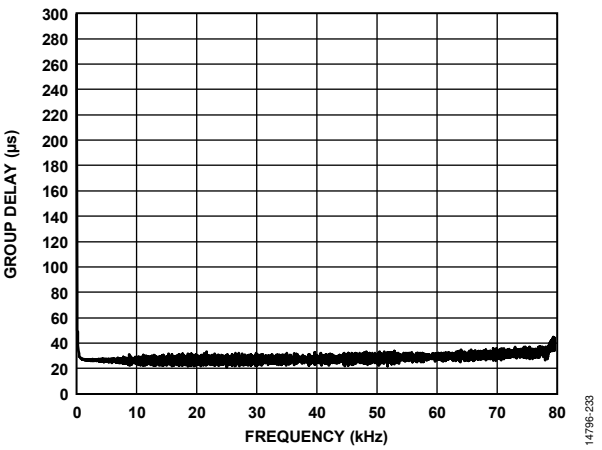

Figure 44. Group Delay vs. Frequency, f_S = 786 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

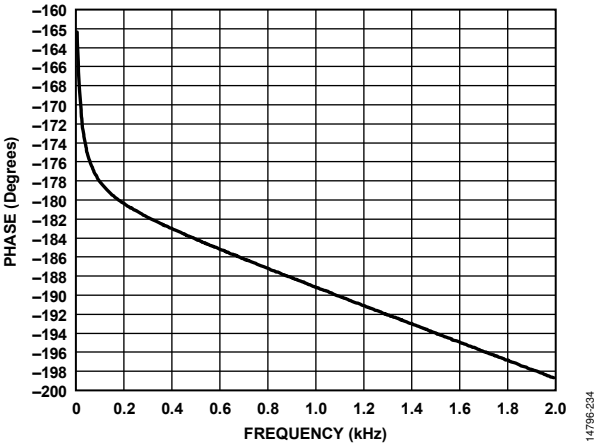

Figure 45. Phase vs. Frequency, 2 kHz Bandwidth f_S = 786 kHz, Signal Path = DAC_SDATA to ASRC to LOUTLx

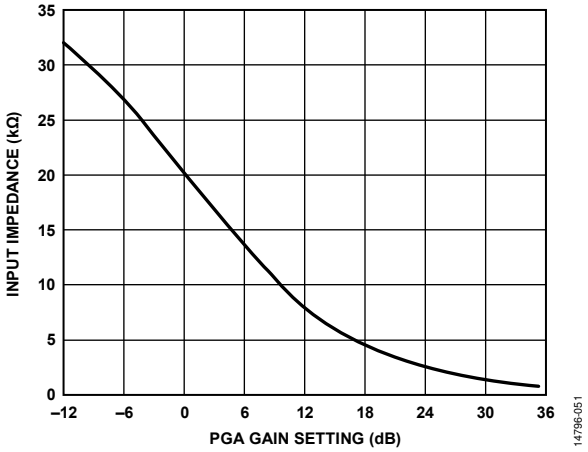

Figure 46. Input Impedance vs. PGA Gain Setting (See the Input Impedance Section)

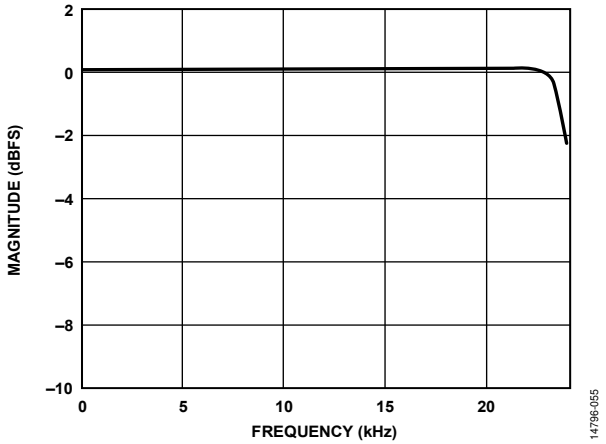

Figure 47. Decimation Pass Band Response, f_S = 768 kHz

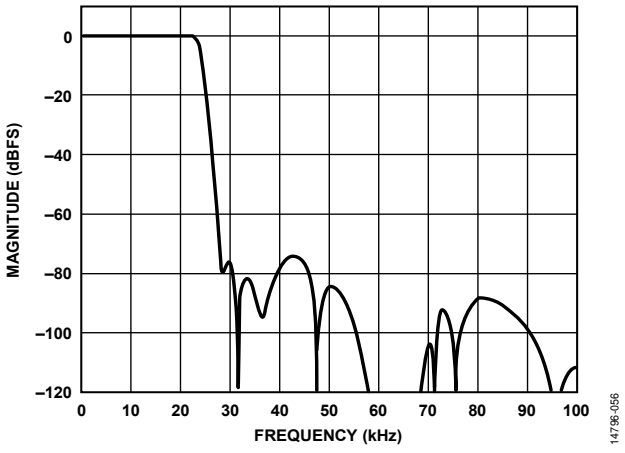

Figure 48. Total Decimation Response, f_S = 768 kHz

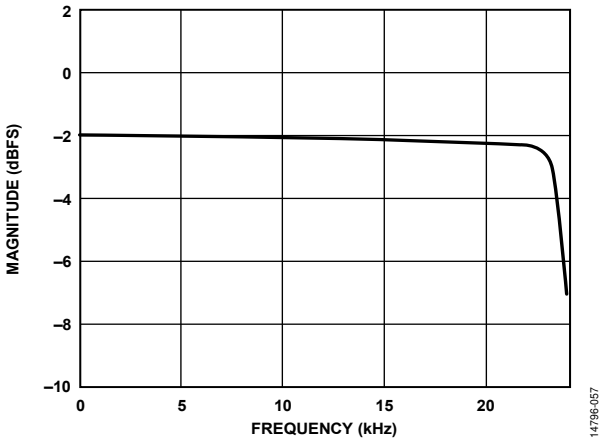

Figure 49. Interpolation Pass Band Response, f_S = 768 kHz

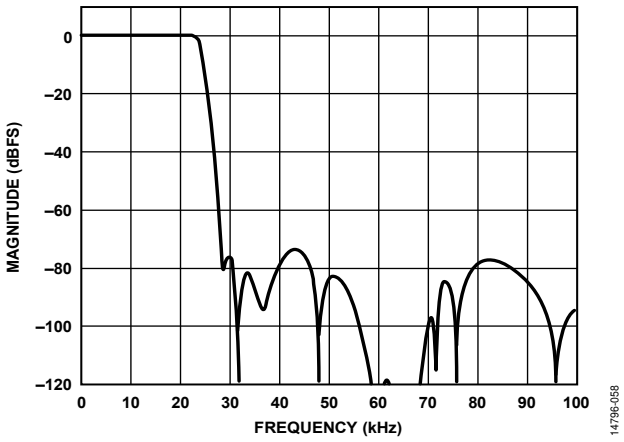

Figure 50. Total Interpolation Response, f_S = 768 kHz

THEORY OF OPERATION

The ADAU1777 is a low power audio codec with a streamlined audio processing core, making it ideal for noise canceling applications that require high quality audio, low power, small size, and low latency. The operating voltage range is 1.71 V to 3.63 V, with an on-board regulator optionally generating the internal digital supply voltage. By enabling low latency settings, the ADAU1777 can reach latencies as low as 5 µs.

The ADCs and DACs are high quality, 24-bit, Σ-Δ converters that operate at a selectable 768 kHz, 192 kHz, or 96 kHz sampling rate. The ADCs have an optional high-pass filter with a cutoff frequency of 1 Hz, 4 Hz, or 8 Hz. The ADCs and DACs also include fine step digital volume controls.

The stereo DAC output can differentially drive a headphone earpiece speaker with 16 Ω or higher impedance. One side of the differential output can be powered down if single-ended operation is required. There is also the option to change to line output mode when the output has a low load.

The input signal path is flexible and can accept single-ended analog microphone inputs, serial audio inputs, and digital microphone inputs. Two microphone bias pins provide seamless interfacing to electret microphones. Each analog input has an independent PGA that can be used for volume adjustment. The serial data port is compatible with I²S, left justified, right justified, and TDM modes, with tristating for interfacing to digital audio data streams.

The core has a reduced instruction set that is optimized for active noise cancellation. The program and parameter RAMs can be loaded with custom audio processing signal flows built using the SigmaStudio™ graphical programming software from Analog Devices, Inc. The values stored in the parameter RAM control individual signal processing blocks. The ADAU1777 also has a self boot function that can load the program RAM, parameter RAM, and register settings on power-up using an external EEPROM.

The SigmaStudio software programs and controls the core through the I²C or SPI control port. Along with aiding in the design and tuning of a signal flow, SigmaStudio can configure all of the ADAU1777 registers. The SigmaStudio graphical interface allows anyone with digital or analog audio processing knowledge to easily design the DSP signal flow and port it to a target application. The interface also provides enough flexibility and programmability for an experienced DSP programmer to have in-depth control of the design. In SigmaStudio, the user can connect graphical blocks (such as biquad filters, volume controls, and arithmetic operations), compile the design, and load the program and parameter files into the ADAU1777 memory through the control port. SigmaStudio also allows the user to download the design to an external EEPROM for self boot operation. Signal processing blocks available in the provided libraries include the following:

- Single-precision biquad filters
- Second-order filters
- Absolute value and two-input adder
- Volume controls
- Limiter

The ADAU1777 can generate its internal clocks from a wide range of input clocks by using the on-board fractional PLL. The PLL accepts inputs from 8 MHz to 27 MHz. For standalone operation, the clock can be generated using the on-board crystal oscillator.