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Low Noise Stereo Codec with SigmaDSP Processing Core

ADAU1781

FEATURES

- 24-bit stereo audio ADC and DAC
- 400 mW speaker amplifier (into 8 Ω load)
- Programmable SigmaDSP audio processing core
  - Wind noise detection and filtering
  - Enhanced stereo capture (ESC)
  - Dynamics processing
  - Equalization and filtering
  - Volume control and mute
- Sampling rates from 8 kHz to 96 kHz
- Stereo pseudo differential microphone input
- Optional stereo digital microphone input pulse-density modulation (PDM)
- Stereo line output
- PLL supporting a range of input clock rates
- Analog and digital I/O 1.8 V to 3.3 V
- Software control via SigmaStudio graphical user interface
- Software-controllable, clickless mute
- Software register and hardware pin standby mode
- 32-lead, 5 mm × 5 mm LFCSP

APPLICATIONS

- Digital still cameras
- Digital video cameras

GENERAL DESCRIPTION

The ADAU1781 is a low power, 24-bit stereo audio codec. The low noise DAC and ADC support sample rates from 8 kHz to 96 kHz. Low current draw and power saving modes make the ADAU1781 ideal for battery-powered audio applications.

A programmable SigmaDSP® core provides enhanced record and playback processing to improve overall audio quality.

The record path includes two digital stereo microphone inputs and an analog stereo input path. The analog inputs can be configured for either a pseudo differential or a single-ended stereo source. A dedicated analog beep input signal can be mixed into any output path. The ADAU1781 includes a stereo line output and speaker driver, which makes the device capable of supporting dynamic speakers.

The serial control bus supports the I²C® or SPI protocols, and the serial audio bus is programmable for I²S, left-justified, right-justified, or TDM mode. A programmable PLL supports flexible clock generation for all standard rates and available master clocks from 11 MHz to 20 MHz.

FUNCTIONAL BLOCK DIAGRAM

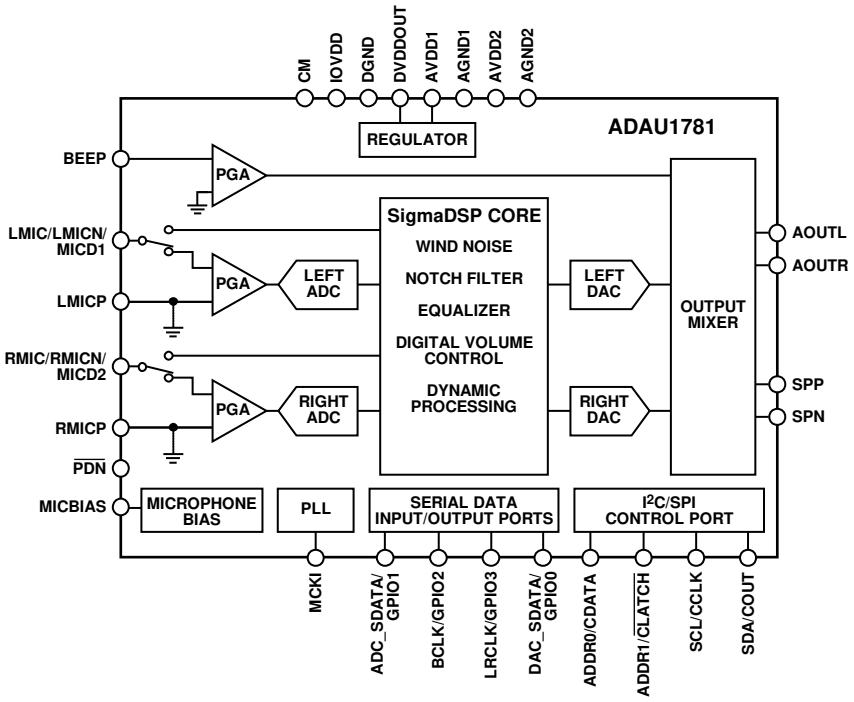

Figure 1.

Rev. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

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Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADAU1781 Evaluation Board
- ADUSB2EBZ Evaluation Board

DOCUMENTATION

Application Notes

- AN-1006: Using the EVAL-ADUSB2EBZ
- AN-951: Using Hardware Controls with SigmaDSP GPIO Pins

Data Sheet

- ADAU1781: Low Noise Stereo Codec with SigmaDSP Processing Core

User Guides

- UG-177: Evaluating the ADAU1781 SigmaDSP using the EVAL-ADAU1781Z

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADAU1781 Sound CODEC Linux Driver
- Firmware Loader for SigmaDSPs

TOOLS AND SIMULATIONS

- SigmaDSP Processors: Software and Tools

DESIGN RESOURCES

- ADAU1781 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADAU1781 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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12/09—Revision 0: Initial Version

SPECIFICATIONS

Performance of all channels is identical, exclusive of the interchannel gain mismatch and interchannel phase deviation specifications. Supply voltages AVDD = AVDD1 = AVDD2 = I/O supply = 3.3 V, digital supply = 1.5 V, unless otherwise noted; temperature = 25°C; master clock (MCLK) = 12.288 MHz (f_S = 48 kHz, 256 × f_S mode); input sample rate = 48 kHz; measurement bandwidth = 20 Hz to 20 kHz; word width = 24 bits; load capacitance (digital output) = 20 pF; load current (digital output) = 2 mA; high level input voltage = 0.7 × IOVDD; and low level input voltage = 0.3 × IOVDD. All power management registers are set to their default states.

RECORD SIDE PERFORMANCE SPECIFICATIONS

Specifications guaranteed at 25°C (ambient).

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTERS					
ADC Resolution	All ADCs		24		Bits
Digital Attenuation Step			0.375		dB
Digital Attenuation Range			95		dB
INPUT RESISTANCE					
Noninverting Inputs PGA (LMICP, RMICP)	All gain settings		500		kΩ
Inverting Inputs PGA (LMICN, RMICN)	0 dB gain		62		kΩ
	6 dB gain		32		kΩ
	10 dB gain		22		kΩ
	14 dB gain		14		kΩ
	17 dB gain		10		kΩ
	20 dB gain		8		kΩ
	26 dB gain		5		kΩ
	32 dB gain		4		kΩ
Beep Input PGA	0 dB		20		kΩ
	6 dB		9		kΩ
	10 dB		6		kΩ
	14 dB		3.5		kΩ
	−23 dB		50		kΩ
	20 dB		2		kΩ
	26 dB		2		kΩ
	32 dB		2		kΩ
SINGLE-ENDED MICROPHONE INPUT TO ADC PATH					
Full-Scale Input Voltage (0 dB)	Scales linearly with AVDD		AVDD/3.3		V rms
	AVDD = 1.8 V		0.55 (1.56)		V rms (V p-p)
	AVDD = 3.3 V		1.0 (2.83)		V rms (V p-p)
Dynamic Range	−60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		96		dB
	AVDD = 3.3 V	94	99.2		dB
No Filter (RMS)	AVDD = 1.8 V		92		dB
	AVDD = 3.3 V	92	96.5		dB
Total Harmonic Distortion + Noise	−3 dBFS				
	AVDD = 1.8 V		−88		dB
	AVDD = 3.3 V		−90		dB
Signal-to-Noise Ratio					
With A-Weighted Filter (RMS)	AVDD = 1.8 V		96		dB
	AVDD = 3.3 V		100		dB
No Filter (RMS)	AVDD = 1.8 V		92		dB
	AVDD = 3.3 V		97		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Left/Right Microphone PGA Gain Range	AVDD = 3.3 V	0		32	dB
Left/Right Microphone PGA Mute Attenuation	AVDD = 3.3 V; mute set by Register 0x400E, Bit 1, and Register 0x400F, Bit 1		−98		dB
Interchannel Gain Mismatch	AVDD = 3.3 V		50		mdB
Offset Error	AVDD = 3.3 V		0.25		mV
Gain Error	AVDD = 3.3 V		−1		%
Interchannel Isolation	AVDD = 3.3 V		−98		dB
Power Supply Rejection Ratio	CM capacitor = 10 µF				
	AVDD = 3.3 V, 100 mV p-p at 217 Hz		−55		dB
	AVDD = 3.3 V, 100 mV p-p at 1 kHz		−55		dB
DIFFERENTIAL MICROPHONE INPUT TO ADC PATH					
Full-Scale Input Voltage (0 dB)	Scales linearly with AVDD		AVDD/3.3		V rms
	AVDD = 1.8 V		0.55 (1.56)		V rms (V p-p)
	AVDD = 3.3 V		1.0 (2.83)		V rms (V p-p)
Dynamic Range	−60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		96		dB
	AVDD = 3.3 V	94	99.2		dB
No Filter (RMS)	AVDD = 1.8 V		92		dB
	AVDD = 3.3 V	92	96.5		dB
Total Harmonic Distortion + Noise	−3 dBFS				
	AVDD = 1.8 V		−84		dB
	AVDD = 3.3 V		−85		dB
Signal-to-Noise Ratio					
With A-Weighted Filter (RMS)	AVDD = 1.8 V		96		dB
	AVDD = 3.3 V		100		dB
No Filter (RMS)	AVDD = 1.8 V		92		dB
	AVDD = 3.3 V		97		dB
Left/Right Microphone PGA Mute Attenuation	AVDD = 3.3 V; mute set by Register 0x400E, Bit 1, and Register 0x400F, Bit 1		−98		dB
Interchannel Gain Mismatch	AVDD = 3.3 V		50		mdB
Offset Error	AVDD = 3.3 V		0.25		mV
Gain Error	AVDD = 3.3 V		−1		%
Interchannel Isolation	AVDD = 3.3 V		−85		dB
Common-Mode Rejection Ratio	AVDD = 3.3 V, 100 mV rms, 1 kHz		−60		dB
	AVDD = 3.3 V, 100 mV rms, 20 kHz		−45		dB
BEEP TO LINE OUTPUT PATH					
Full-Scale Input Voltage (0 dB)	Scales linearly with AVDD		AVDD/3.3		V rms
	AVDD = 1.8 V		0.55 (1.56)		V rms (V p-p)
	AVDD = 3.3 V		1.0 (2.83)		V rms (V p-p)
Total Harmonic Distortion + Noise	−3 dBFS input, measured at AOUTL pin, beep gain set to 0 dB				
	AVDD = 1.8 V		−88		dB
	AVDD = 3.3 V		−88		dB
Signal-to-Noise Ratio					
With A-Weighted Filter (RMS)	AVDD = 1.8 V		99		dB
	AVDD = 3.3 V		105		dB
No Filter (RMS)	AVDD = 1.8 V		96		dB
	AVDD = 3.3 V		102		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Dynamic Range	−60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		99		dB
	AVDD = 3.3 V		105		dB
No Filter (RMS)	AVDD = 1.8 V		96		dB
	AVDD = 3.3 V		102		dB
Beep Input Mute Attenuation	AVDD = 3.3 V; mute set by Register 0x4008, Bit 3		−90		dB
Offset Error	AVDD = 3.3 V		10		mV
Gain Error	AVDD = 3.3 V		−0.3		dB
Interchannel Gain Mismatch			30		mdB
Beep Input PGA Gain Range	AVDD = 3.3 V	−23		+32	dB
Beep Playback Mixer Gain Range	AVDD = 3.3 V	−15		+6	dB
Power Supply Rejection Ratio	CM capacitor = 10 µF				
	AVDD = 3.3 V, 100 mV p-p at 217 Hz		−58		dB
	AVDD = 3.3 V, 100 mV p-p at 1 kHz		−72		dB
MICROPHONE BIAS	Microphone bias enabled				
Bias Voltage					
0.65 × AVDD	AVDD = 1.8 V, low bias		1.17		V
	AVDD = 3.3 V, low bias		2.145		V
0.90 × AVDD	AVDD = 1.8 V, high bias		1.62		V
	AVDD = 3.3 V, high bias		2.97		V
Bias Current Source	AVDD = 3.3 V, high bias, high performance			5	mA
Noise in the Signal Bandwidth	AVDD = 3.3 V, 20 Hz to 20 kHz				
	High bias, high performance		39		nV√Hz
	High bias, low performance		78		nV√Hz
	Low bias, high performance		25		nV√Hz
	Low bias, low performance		35		nV√Hz
	AVDD = 1.8 V, 20 Hz to 20 kHz				
	High bias, high performance		35		nV√Hz
	High bias, low performance		45		nV√Hz
	Low bias, high performance		23		nV√Hz
	Low bias, low performance		23		nV√Hz

OUTPUT SIDE PERFORMANCE SPECIFICATIONS

Specifications guaranteed at 25°C (ambient). The output load for the speaker output path is an 8 Ω, 400 mW speaker.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL-TO-ANALOG CONVERTERS					
DAC Resolution	All DACs		24		Bits
Digital Attenuation Step			0.375		dB
Digital Attenuation Range			95		dB
DAC TO LINE OUTPUT PATH					
Full-Scale Output Voltage (0 dB)	Scales linearly with AVDD		AVDD/3.3		V rms
	AVDD = 1.8 V		0.55 (1.56)		V rms (V p-p)
	AVDD = 3.3 V		1.0 (2.83)		V rms (V p-p)
Line Output Mute Attenuation, DAC to Mixer Path Muted	AVDD = 3.3 V; mute set by Register 0x401C, Bit 5, and Register 0x401E, Bit 6		−85		dB
Line Output Mute Attenuation, Line Output Muted	AVDD = 3.3 V; mute set by Register 0x4025, Bit 1, and Register 0x4026, Bit 1		−85		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Dynamic Range	−60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		99		dB
	AVDD = 3.3 V	94	103		dB
No Filter (RMS)	AVDD = 1.8 V		97		dB
	AVDD = 3.3 V	92	100		dB
Total Harmonic Distortion + Noise	−3 dBFS				dB
	AVDD = 1.8 V		−88		dB
	AVDD = 3.3 V		−88		dB
Signal-to-Noise Ratio					
With A-Weighted Filter (RMS)	AVDD = 1.8 V		99		dB
	AVDD = 3.3 V		103		dB
No Filter (RMS)	AVDD = 1.8 V		97		dB
	AVDD = 3.3 V		100		dB
Power Supply Rejection Ratio	CM capacitor = 10 µF				
	AVDD = 3.3 V, 100 mV p-p at 217 Hz		−55		dB
	AVDD = 3.3 V, 100 mV p-p at 1 kHz		−63		dB
Gain Error	AVDD = 3.3 V		−1		dB
Interchannel Gain Mismatch	AVDD = 3.3 V		50		mdB
Offset Error	AVDD = 3.3 V		10		mV
DAC TO SPEAKER OUTPUT PATH	P_O = output power				
Differential Full-Scale Output Voltage (0 dB)	Scales linearly with AVDD		AVDD/1.65		V rms
	AVDD = 1.8 V		1.1 (3.12)		V rms (V p-p)
	AVDD = 3.3 V		2.0 (5.66)		V rms (V p-p)
Total Harmonic Distortion + Noise					
4 Ω Load	AVDD = 1.8 V, P_O = 50 mW		−60		dB
	AVDD = 3.3 V, P_O = 175 mW		−60		dB
8 Ω Load	AVDD = 1.8 V, P_O = 50 mW		−60		dB
	AVDD = 3.3 V, P_O = 175 mW		−60		dB
	AVDD = 3.3 V, P_O = 330 mW		−60		dB
	AVDD = 3.3 V, P_O = 440 mW		−16		dB
Dynamic Range	−60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		100		dB
	AVDD = 3.3 V	94	105		dB
No Filter (RMS)	AVDD = 1.8 V		98		dB
	AVDD = 3.3 V	92	103		dB
Signal-to-Noise Ratio					
With A-Weighted Filter (RMS)	AVDD = 1.8 V		100		dB
	AVDD = 3.3 V		105		dB
No Filter (RMS)	AVDD = 1.8 V		98		dB
	AVDD = 3.3 V		103		dB
Power Supply Rejection Ratio	CM capacitor = 10 µF				
	AVDD = 3.3 V,100 mV p-p at 217 Hz		−55		dB
	AVDD = 3.3 V, 100 mV p-p at 1 kHz		−55		dB
Differential Offset Error	AVDD = 3.3 V		2		mV
Mono Mixer Mute Attenuation, DAC to Mixer Path Muted	Mute set by Register 0x401F, Bit 0		−90		dB
BEEP TO SPEAKER OUTPUT PATH	P_O = output power				
Differential Full-Scale Output Voltage (0 dB)	Scales linearly with AVDD		AVDD/1.65		V rms
	AVDD = 1.8 V		1.1 (3.12)		V rms (V p-p)
	AVDD = 3.3 V		2.0 (5.66)		V rms (V p-p)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Total Harmonic Distortion + Noise					
	8 Ω, 1 nF load, AVDD = 1.8 V, P_O = 50 mW		−60		dB
	AVDD = 3.3 V, P_O = 175 mW		−60		dB
Dynamic Range	−60 dB input				
With A-Weighted Filter (RMS)	AVDD = 1.8 V		97		dB
	AVDD = 3.3 V		103		dB
No Filter (RMS)	AVDD = 1.8 V		94		dB
	AVDD = 3.3 V		100		dB
Signal-to-Noise Ratio					
With A-Weighted Filter (RMS)	AVDD = 1.8 V		98		dB
	AVDD = 3.3 V		103		dB
No Filter (RMS)	AVDD = 1.8 V		96		dB
	AVDD = 3.3 V		101		dB
Power Supply Rejection Ratio	CM capacitor = 10 µF				
	100 mV p-p at 217 Hz		−57		dB
	100 mV p-p at 1 kHz		−60		dB
Differential Offset Error			2		mV
Mono Mixer Mute Attenuation, Beep to Mixer Path Muted	Mute set by Register 0x401F, Bit 0		−90		dB
REFERENCE (CM PIN)					
Common-Mode Reference Output			AVDD/2		V

POWER SUPPLY SPECIFICATIONS

AVDD1 and AVDD2 must always be equal. Power supply measurements are taken with the SigmaDSP processing core enabled.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
AVDD1, AVDD2		1.8[1]	3.3	3.65	V
IOVDD		1.63	3.3	3.65	V
Digital I/O Current (IOVDD = 3.3 V)	20 pF capacitive load on all digital pins				
Slave Mode, Analog I/O, 12.288 MHz External MCLK Input	f_S = 48 kHz		0.20		mA
	f_S = 96 kHz		0.35		mA
	f_S = 8 kHz		0.04		mA
Master Mode, MCKO Disabled	f_S = 48 kHz		1.25		mA
	f_S = 96 kHz		2.50		mA
	f_S = 8 kHz		0.22		mA
Digital I/O Current (IOVDD = 1.8 V)	20 pF capacitive load on all digital pins				
Slave Mode, Analog I/O, 12.288 MHz External MCLK Input	f_S = 48 kHz		0.10		mA
	f_S = 96 kHz		0.18		mA
	f_S = 8 kHz		0.02		mA
Master Mode, MCKO Disabled	f_S = 48 kHz		0.68		mA
	f_S = 96 kHz		1.33		mA
	f_S = 8 kHz		0.12		mA
Analog Current (AVDD)	See Table 4				

[1] The zero-cross detection of the beep path is not supported at AVDD1, AVDD2 < 2.2 V.

TYPICAL POWER MANAGEMENT MEASUREMENTS

Master clock = 12.288 MHz, PLL is active in integer mode at a 256 × f_S input rate for f_S = 48 kHz, analog and digital input tones are −1 dBFS with a frequency of 1 kHz. Analog input and output are simultaneously active. Pseudo differential stereo input is routed to ADCs, and DACs are routed to stereo line output with a 16 kΩ load. ADC input at −1 dBFS, DAC input at 0 dBFS. The speaker output is disabled. The serial port is configured in slave mode. The beep path is disabled. SigmaDSP processing is enabled. Current measurements are given in units of mA rms.

Table 4. Mixer Boost and Power Management Conditions

Operating Voltage	Power Management Mode[1]	Mixer Boost Mode[2]	Typical AVDD Current Consumption (mA)	Typical ADC THD + N (dB)	Typical Line Output THD + N (dB)
AVDD = IOVDD = 3.3 V	Normal (default)	Normal operation	16.84	88.5	93.0
		Boost Level 1	16.88	88.5	93.0
		Boost Level 2	16.92	88.5	93.0
		Boost Level 3	17.00	88.5	93.0
	Extreme power saving	Normal operation	15.66	88.0	87.5
		Boost Level 1	15.68	88.0	87.5
		Boost Level 2	15.70	88.0	87.5
		Boost Level 3	15.75	88.0	87.5
	Enhanced performance	Normal operation	17.43	88.5	94.5
		Boost Level 1	17.50	88.5	94.5
		Boost Level 2	17.53	88.5	94.5
		Boost Level 3	17.63	88.5	94.5
	Power saving	Normal operation	16.25	89.0	90.5
		Boost Level 1	16.28	89.0	90.5
		Boost Level 2	16.31	89.0	90.5
		Boost Level 3	16.38	89.0	90.5
AVDD = IOVDD = 1.8 V	Normal (default)	Normal operation	15.15	88.5	89.5
		Boost Level 1	15.19	88.5	89.5
		Boost Level 2	15.23	88.5	89.5
		Boost Level 3	15.30	88.5	89.5
	Extreme power saving	Normal operation	14.03	86.5	85.5
		Boost Level 1	14.05	86.5	85.5
		Boost Level 2	14.07	86.5	85.5
		Boost Level 3	14.12	86.5	85.5
	Enhanced performance	Normal operation	15.71	88.5	90.5
		Boost Level 1	15.76	88.5	90.5
		Boost Level 2	15.81	88.5	90.5
		Boost Level 3	15.89	88.5	90.5
	Power saving	Normal operation	14.59	88.0	88.0
		Boost Level 1	14.62	88.0	88.0
		Boost Level 2	14.65	88.0	88.0
		Boost Level 3	14.71	88.0	88.0

[1] Set by Register 0x4009, Bits[4:1], and Register 0x4029, Bits[5:2].
[2] Set by Register 0x4009, Bits[6:5].

DIGITAL FILTERS

Table 5.

Parameter	Mode	Factor	Min	Typ	Max	Unit
ADC DECIMATION FILTER	All modes, typ value is for 48 kHz					
Pass Band		0.4375 × f_S		21		kHz
Pass-Band Ripple				±0.015		dB
Transition Band		0.5 × f_S		24		kHz
Stop Band		0.5625 × f_S		27		kHz
Stop-Band Attenuation			70			dB
Group Delay		22.9844/f_S		479		µs

Parameter	Mode	Factor	Min	Typ	Max	Unit
DAC INTERPOLATION FILTER						
Pass Band	48 kHz mode, typ value is for 48 kHz	$0.4535 \times f_S$		22		kHz
	96 kHz mode, typ value is for 96 kHz	$0.3646 \times f_S$	35	69		kHz
Pass-Band Ripple	48 kHz mode, typ value is for 48 kHz				±0.01	dB
	96 kHz mode, typ value is for 96 kHz				±0.05	dB
Transition Band	48 kHz mode, typ value is for 48 kHz	$0.5 \times f_S$		24		kHz
	96 kHz mode, typ value is for 96 kHz	$0.5 \times f_S$		48		kHz
Stop Band	48 kHz mode, typ value is for 48 kHz	$0.5465 \times f_S$		26		kHz
	96 kHz mode, typ value is for 96 kHz	$0.6354 \times f_S$		61		kHz
Stop-Band Attenuation	48 kHz mode, typ value is for 48 kHz		70			dB
	96 kHz mode, typ value is for 96 kHz		70			dB
Group Delay	48 kHz mode, typ value is for 48 kHz	$25/f_S$		521		µs
	96 kHz mode, typ value is for 96 kHz	$11/f_S$		115		µs

DIGITAL INPUT/OUTPUT SPECIFICATIONS

$-25°C < T_A < +85°C$, IOVDD = 1.62 V to 3.63 V, unless otherwise specified.

Table 6.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
HIGH LEVEL INPUT VOLTAGE (V_{IH})		0.7 × IOVDD			V
LOW LEVEL INPUT VOLTAGE (V_{IL})	IOVDD ≥ 2.97 V			0.3 × IOVDD	V
	1.8 V ≤ IOVDD ≤ 2.97 V			0.2 × IOVDD	V
	IOVDD < 1.8 V			0.1 × IOVDD	V
INPUT LEAKAGE	I_{IH} at V_{IH} = 2.4 V		±0.17		µA
	I_{IL} at V_{IL} = 0.8 V		±0.17		µA
	I_{IL} of MCKI		−7		µA
	I_{IH} with internal pull-up		±0.7		µA
	I_{IL} with internal pull-down		−7		µA
	I_{IH} with internal pull-up		5		µA
	I_{IL} with internal pull-down		±0.18		µA
HIGH LEVEL OUTPUT VOLTAGE (V_{OH})	For low drive strength, I_{OH} = 2 mA and I_{OL} = 2 mA at IOVDD = 3.3 V, I_{OH} = 0.6 mA and I_{OL} = 0.6 mA at IOVDD = 1.8 V; for high drive strength, I_{OH} = 3 mA and I_{OL} = 3 mA at IOVDD = 3.3 V, I_{OH} = 0.9 mA and I_{OL} = 0.9 mA at IOVDD = 1.8 V	IOVDD − 0.4			V
LOW LEVEL OUTPUT VOLTAGE (V_{OL})	For low drive strength, I_{OH} = 2 mA and I_{OL} = 2 mA at IOVDD = 3.3 V, I_{OH} = 0.6 mA and I_{OL} = 0.6 mA at IOVDD = 1.8 V; for high drive strength, I_{OH} = 3 mA and I_{OL} = 3 mA at IOVDD = 3.3 V, I_{OH} = 0.9 mA and I_{OL} = 0.9 mA at IOVDD = 1.8 V			0.4	V
INPUT CAPACITANCE				5	pF

DIGITAL TIMING SPECIFICATIONS

−25°C < T_A < +85°C, IOVDD = 1.62 V to 3.63 V, unless otherwise specified.

Table 7. Digital Timing

Parameter	Limit t_{MIN}	Limit t_{MAX}	Unit	Description
MASTER CLOCK				
t_{MP}	50	90.9	ns	Master clock (MCLK) period (that is, period of the signal input to MCKI).
Duty Cycle	30	70	%	
SERIAL PORT				
t_{BIL}	10		ns	BCLK pulse width low.
t_{BIH}	10		ns	BCLK pulse width high.
t_{LIS}	5		ns	LRCLK setup. Time to BCLK rising.
t_{LIH}	5		ns	LRCLK hold. Time from BCLK rising.
t_{SIS}	5		ns	DAC_SDATA setup. Time to BCLK rising.
t_{SIH}	5		ns	DAC_SDATA hold. Time from BCLK rising.
t_{SODM}		70	ns	ADC_SDATA delay. Time from BCLK falling in master mode.
SPI PORT				
$f_{CCLK,R}$		5	MHz	CCLK frequency, read operation, IOVDD = 1.8 V ± 10%.
$f_{CCLK,R}$		10	MHz	CCLK frequency, read operation, IOVDD = 3.3 V ± 10%.
$f_{CCLK,W}$		25	MHz	CCLK frequency, write operation, IOVDD = 1.8 V ± 10%.
$f_{CCLK,W}$		25	MHz	CCLK frequency, write operation, IOVDD = 3.3 V ± 10%.
t_{CCPL}	10		ns	CCLK pulse width low.
t_{CCPH}	10		ns	CCLK pulse width high.
t_{CLS}	10		ns	$\overline{\text{CLATCH}}$ setup. Time to CCLK rising.
t_{CLH}	5		ns	$\overline{\text{CLATCH}}$ hold. Time from CCLK rising.
t_{CLPH}	10		ns	$\overline{\text{CLATCH}}$ pulse width high.
t_{CDS}	5		ns	CDATA setup. Time to CCLK rising.
t_{CDH}	5		ns	CDATA hold. Time from CCLK rising.
t_{COD}		70		COUT delay from CCLK edge to valid data, IOVDD = 1.8 V ± 10%.
		40	ns	COUT delay from CCLK edge to valid data, IOVDD = 3.3 V ± 10%.
I^2C PORT				
f_{SCL}		400	kHz	SCL frequency.
t_{SCLH}	0.6		µs	SCL high.
t_{SCLL}	1.3		µs	SCL low.
t_{SCS}	0.6		µs	Setup time; relevant for repeated start condition.
t_{SCH}	0.6		µs	Hold time. After this period, the first clock is generated.
t_{DS}	100		ns	Data setup time.
t_{SCR}		300	ns	SCL rise time.
t_{SCF}		300	ns	SCL fall time.
t_{SDR}		300	ns	SDA rise time.
t_{SDF}		300	ns	SDA fall time.
t_{BFT}	0.6		µs	Bus-free time. Time between stop and start.
DIGITAL MICROPHONE				R_L = 1 MΩ, C_L = 14 pF.
t_{DCF}		10	ns	Digital microphone clock fall time.
t_{DCR}		10	ns	Digital microphone clock rise time.
t_{DDV}	22	30	ns	Digital microphone delay time for valid data.
t_{DDH}	0	12	ns	Digital microphone delay time for data three-stated.

Digital Timing Diagrams

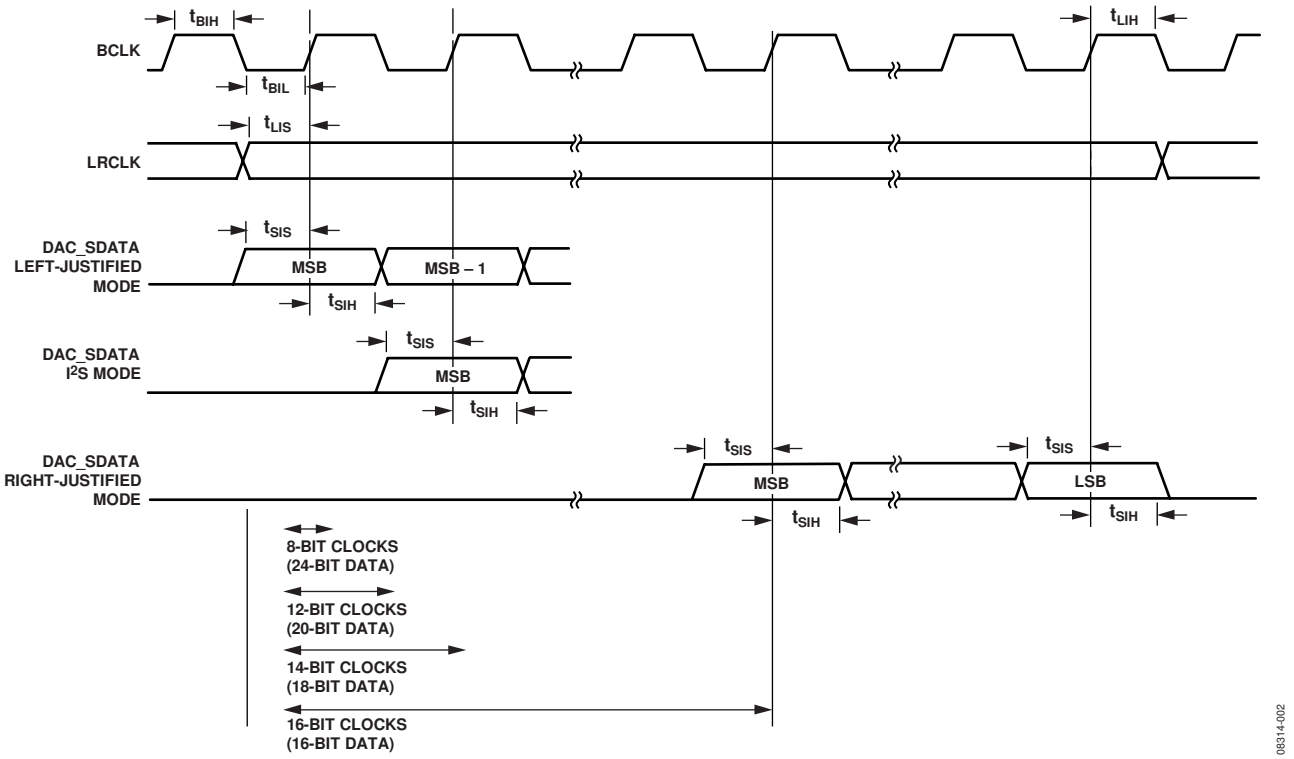

Figure 2. Serial Input Port Timing

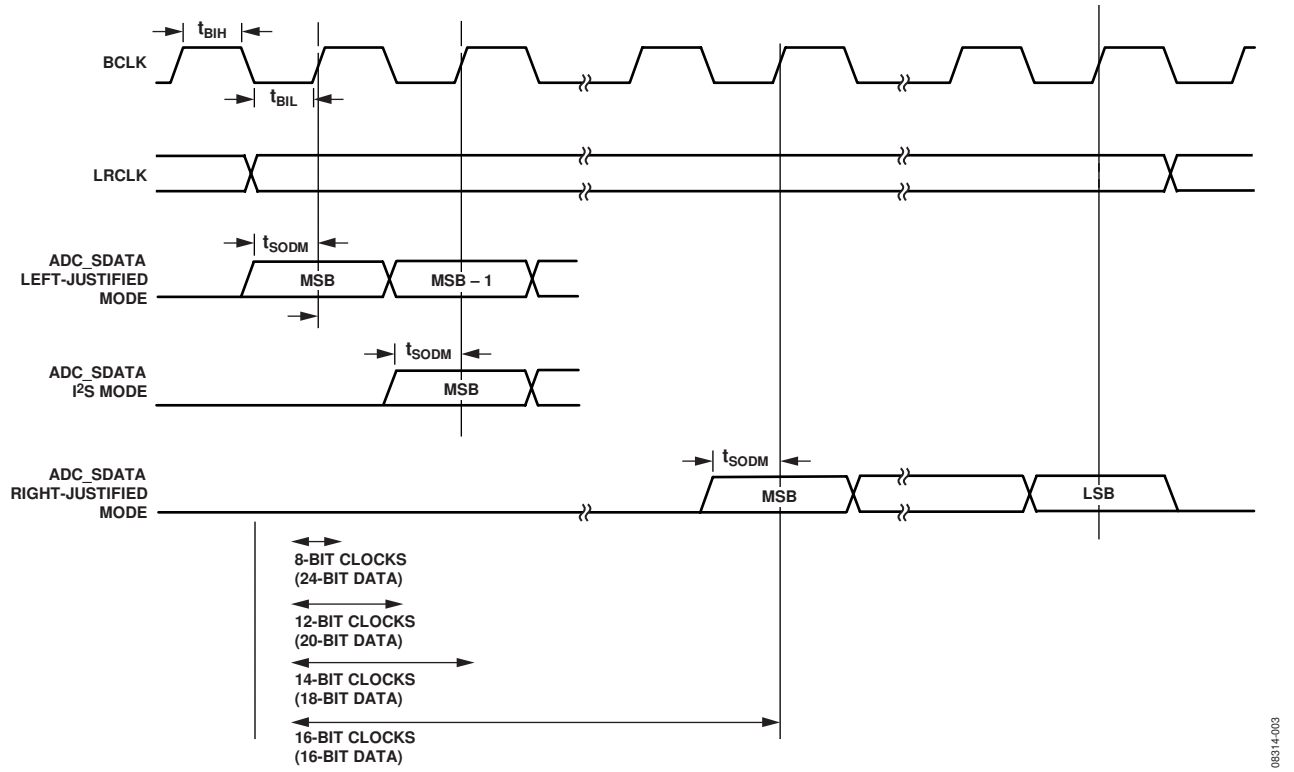

Figure 3. Serial Output Port Timing

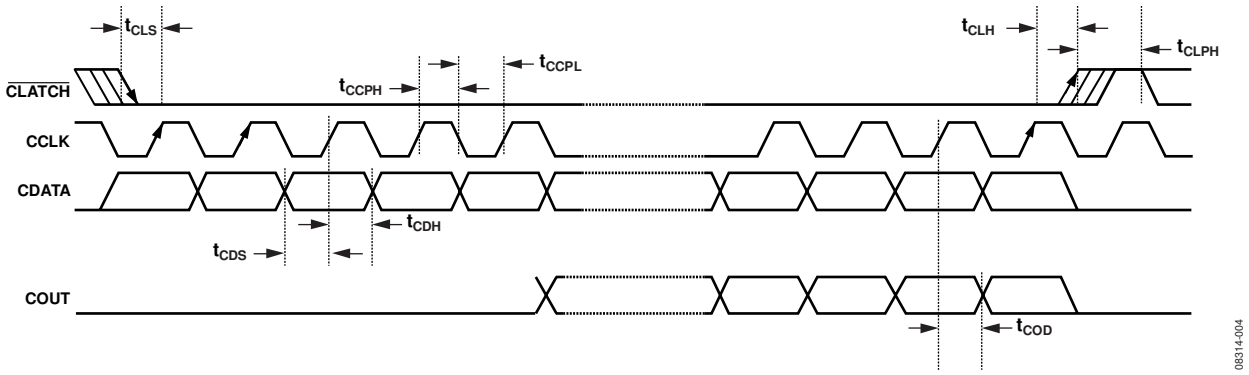

Figure 4. SPI Port Timing

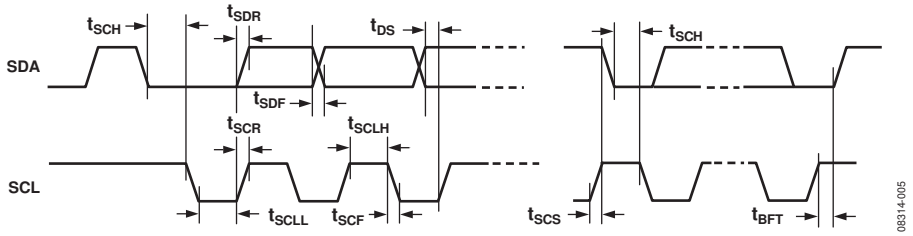

Figure 5. I²C Port Timing

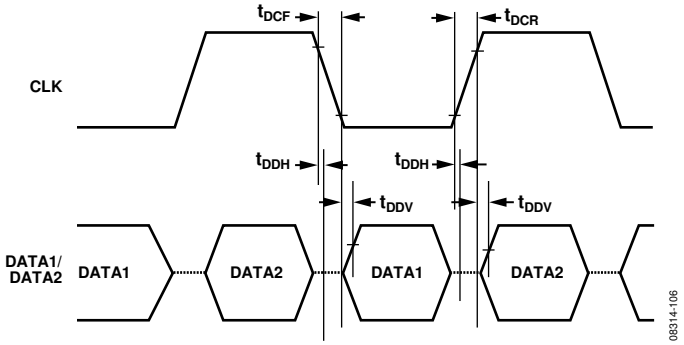

Figure 6. Digital Microphone Timing

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Power Supply (AVDD1 = AVDD2)	−0.3 V to +3.9 V
Input Current (Except Supply Pins)	±20 mA
Analog Input Voltage (Signal Pins)	−0.3 V to VDD + 0.3 V
Digital Input Voltage (Signal Pins)	−0.3 V to VDD + 0.3 V
Operating Temperature Range (Case)	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

In Table 9, θ_{JA} is the junction-to-ambient thermal resistance, θ_{JB} is the junction-to-board thermal resistance, θ_{JC} is the junction-to-case thermal resistance, ψ_{JB} is the in-use junction-to-top of package thermal resistance, and ψ_{JT} is the in-use junction-to-board thermal resistance. All characteristics are for a 4-layer board.

Table 9. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	ψ_{JB}	ψ_{JT}	Unit
32-Lead LFCSP	35	19	2.5	18	0.3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

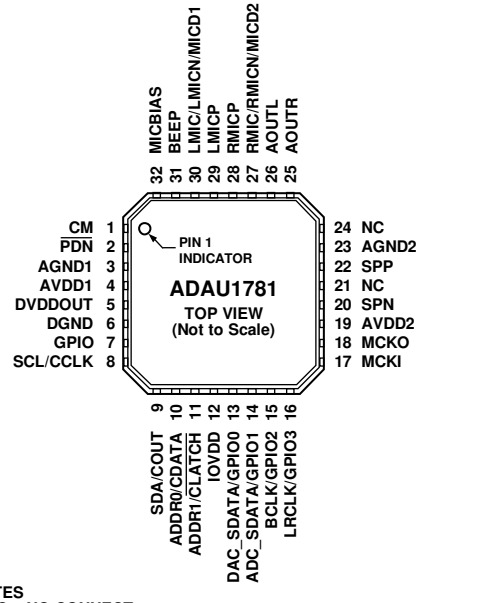

Figure 7. 32-Lead LFCSP Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	CM	A_OUT	VDD/2 V Common-Mode Reference. A 10 µF to 47 µF decoupling capacitor should be connected between this pin and ground to reduce crosstalk between the ADCs and DACs. The material of the capacitors is not critical. This pin can be used to bias external analog circuits, as long as they are not drawing current from CM (for example, the noninverting input of an op amp).
2	$\overline{\text{PDN}}$	A_IN	Power-Down. Connecting this pin to GND powers down the chip. Resides in AVDD1 domain.
3	AGND1	PWR	Analog Ground.
4	AVDD1	PWR	Analog Power Supply. Should be equivalent to AVDD2.
5	DVDDOUT	PWR	Digital Core Supply Decoupling Point. The digital supply is generated from an on-board regulator and does not require an external supply. DVDDOUT should be decoupled to DGND with a 100 nF capacitor.
6	DGND	PWR	Digital Ground.
7	GPIO	D_IO	Dedicated General-Purpose Input/Output.
8	SCL/CCLK	D_IN	I^2C Clock/SPI Clock.
9	SDA/COUT	D_IO	I^2C Data/SPI Data Output.
10	ADDR0/CDATA	D_IN	I^2C Address 0/SPI Data Input.
11	ADDR1/$\overline{\text{CLATCH}}$	D_IN	I^2C Address 1/SPI Latch Signal.
12	IOVDD	PWR	Supply for Digital Input and Output Pins. The digital output pins are supplied from IOVDD, which sets the highest allowed input voltage for the digital input pins. The current draw of this pin is variable because it is dependent on the loads of the digital outputs. IOVDD should be decoupled to DGND with a 100 nF capacitor.
13	DAC_SDATA/GPIO0	D_IO	DAC Serial Input Data/General-Purpose Input and Output.
14	ADC_SDATA/GPIO1	D_IO	ADC Serial Output Data/General-Purpose Input and Output.
15	BCLK/GPIO2	D_IO	Serial Data Port Bit Clock/General-Purpose Input and Output.
16	LRCLK/GPIO3	D_IO	Serial Data Port Frame Clock/General-Purpose Input and Output.
17	MCKI	D_IN	Master Clock Input.

Pin No.	Mnemonic	Type[1]	Description
18	MCKO	D_OUT	Master Clock Output.
19	AVDD2	PWR	Analog Power Supply. Should be equivalent to AVDD1.
20	SPN	A_OUT	Speaker Amplifier Negative Signal Output.
21	NC		No Connect.
22	SPP	A_OUT	Speaker Amplifier Positive Signal Output.
23	AGND2	PWR	Speaker Amplifier Ground.
24	NC		No Connect.
25	AOUTR	A_OUT	Line Output Amplifier, Right Channel.
26	AOUTL	A_OUT	Line Output Amplifier, Left Channel.
27	RMIC/RMICN/MICD2	A_IN	Right Channel Input from Single-Ended Source/Right Channel Input from Negative Pseudo Differential Source/Digital Microphone Input 2.
28	RMICP	A_IN	Right Channel Input from Positive Pseudo Differential Source.
29	LMICP	A_IN	Left Channel Input from Positive Pseudo Differential Source.
30	LMIC/LMICN/MICD1	A_IN	Left Channel Input from Single-Ended Source/Left Channel Input from Negative Pseudo Differential Source/Digital Microphone Input 1.
31	BEEP	A_IN	Beep Signal Input.
32	MICBIAS	PWR	Microphone Bias.
	THERM_PAD (Exposed Pad)		Exposed Pad. The exposed pad is connected internally to the ADAU1781 grounds. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the ground plane.

[1] A_OUT = analog output, A_IN = analog input, PWR = power, D_IO = digital input/output, D_OUT = digital output, and D_IN = digital input.

TYPICAL PERFORMANCE CHARACTERISTICS

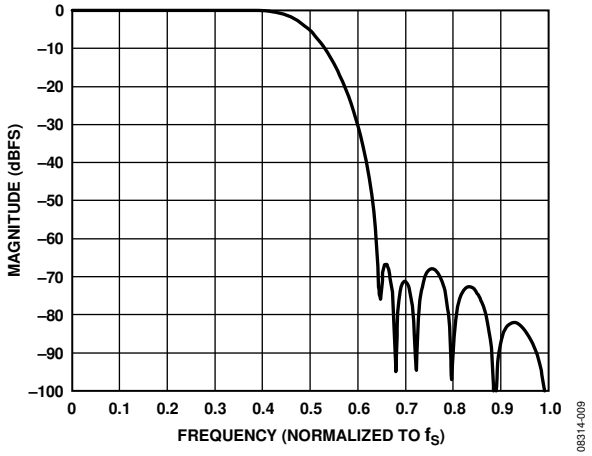

Figure 8. ADC Decimation Filter, 64× Oversampling, Normalized to f_S

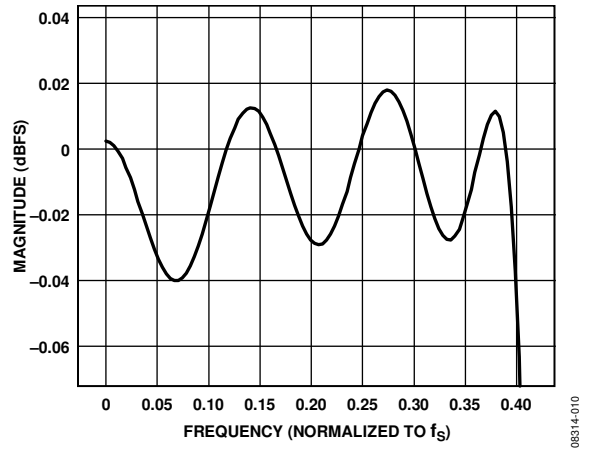

Figure 9. ADC Decimation Filter Pass-Band Ripple, 64× Oversampling, Normalized to f_S

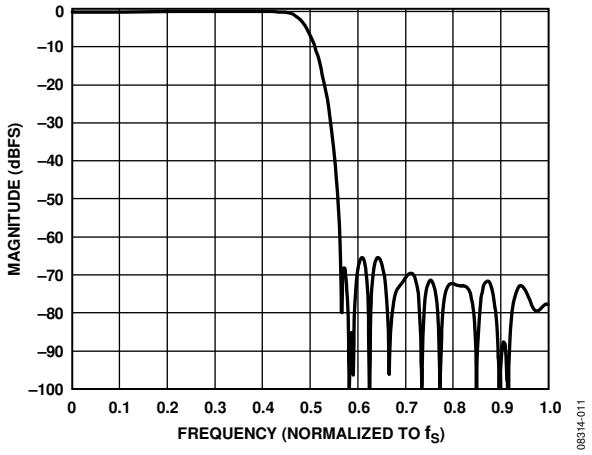

Figure 10. ADC Decimation Filter, 128× Oversampling, Normalized to f_S

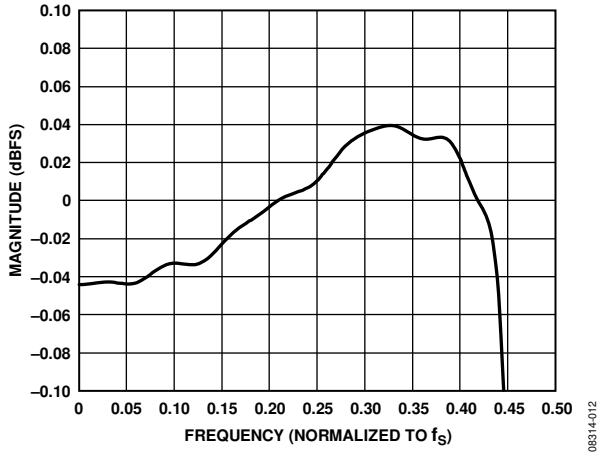

Figure 11. ADC Decimation Filter Pass-Band Ripple, 128× Oversampling, Normalized to f_S

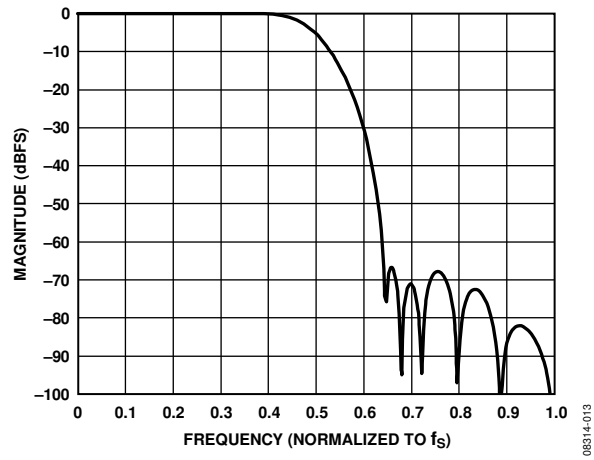

Figure 12. ADC Decimation Filter, Double-Rate Mode, Normalized to f_S

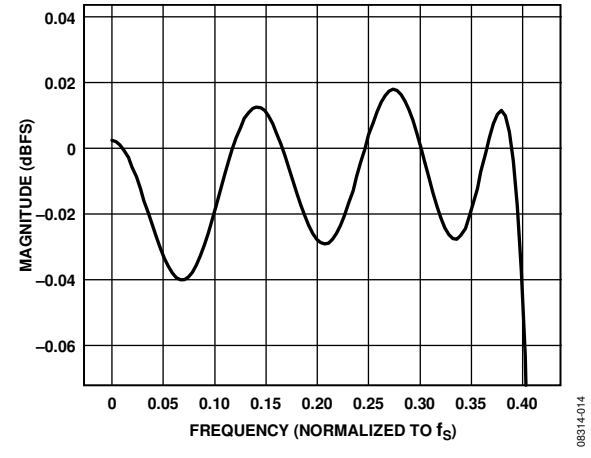

Figure 13. ADC Decimation Filter Pass-Band Ripple, Double-Rate Mode, Normalized to f_S

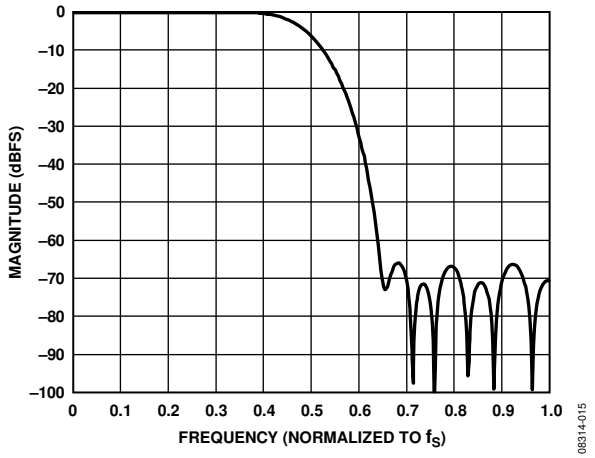

Figure 14. DAC Interpolation Filter, 64× Oversampling, Normalized to f_S

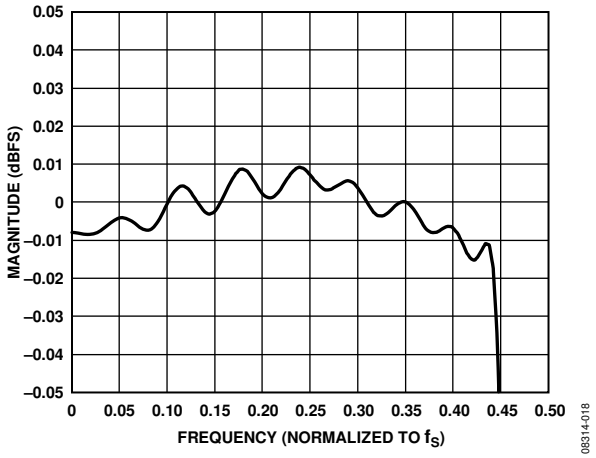

Figure 17. DAC Interpolation Filter Pass-Band Ripple, 128× Oversampling, Normalized to f_S

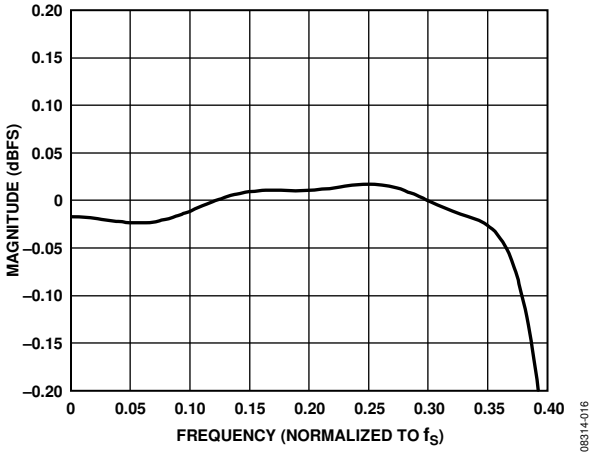

Figure 15. DAC Interpolation Filter Pass-Band Ripple, 64× Oversampling, Normalized to f_S

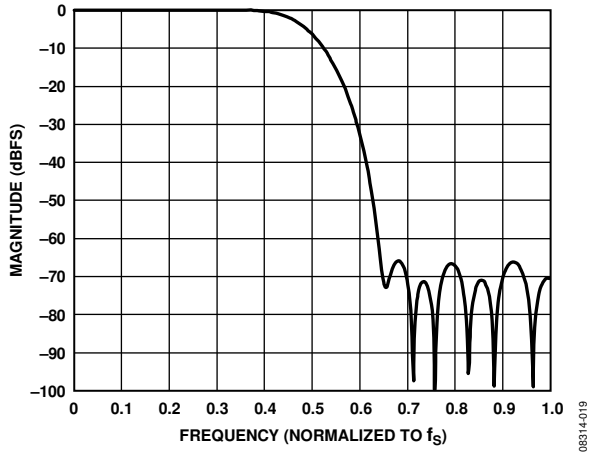

Figure 18. DAC Interpolation Filter, Double-Rate Mode, Normalized to f_S

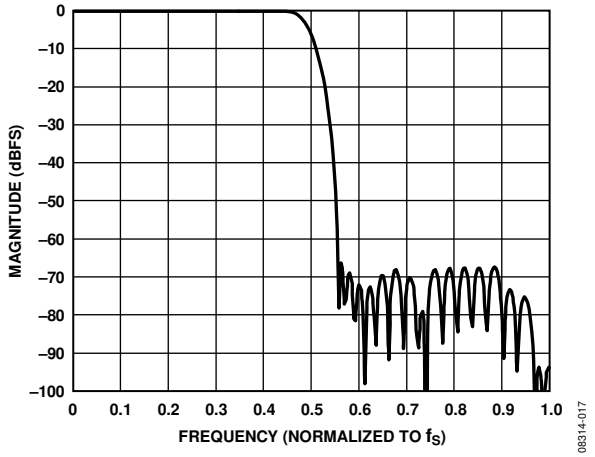

Figure 16. DAC Interpolation Filter, 128× Oversampling, Normalized to f_S

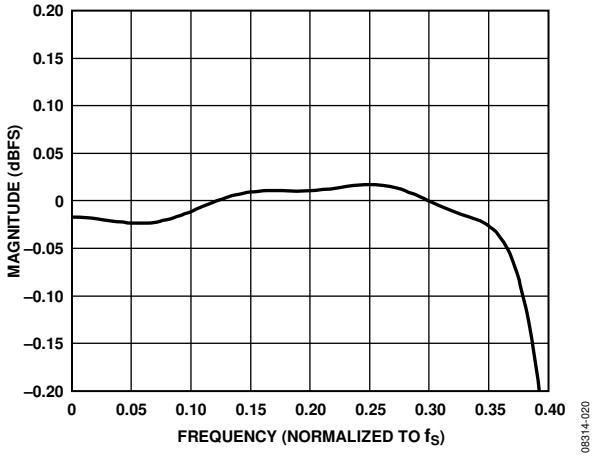

Figure 19. DAC Interpolation Filter Pass-Band Ripple, Double-Rate Mode, Normalized to f_S

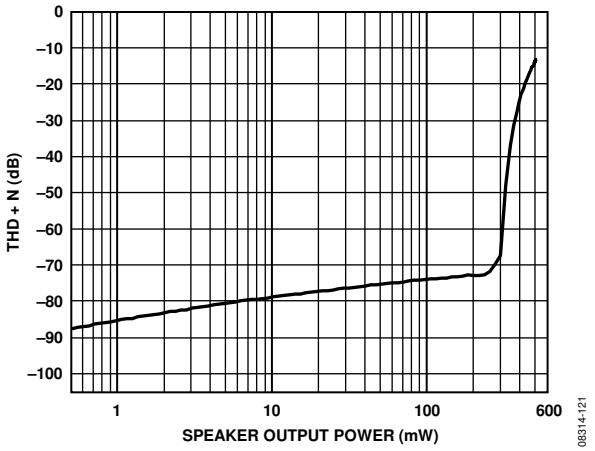

Figure 20. THD + N vs. Speaker Output Power, 8 Ω Load, 3.3 V Supply

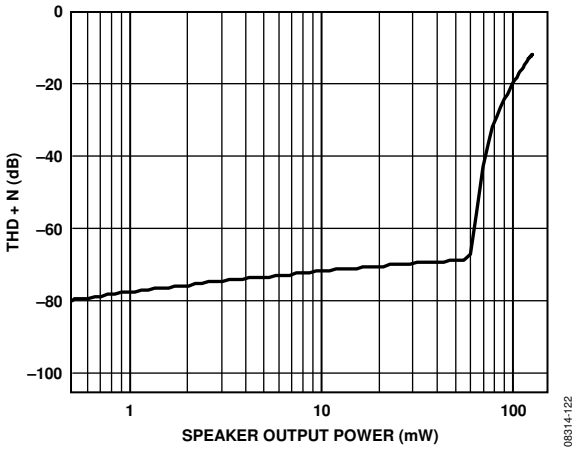

Figure 21. THD + N vs. Speaker Output Power, 8 Ω Load, 1.8 V Supply

SYSTEM BLOCK DIAGRAMS

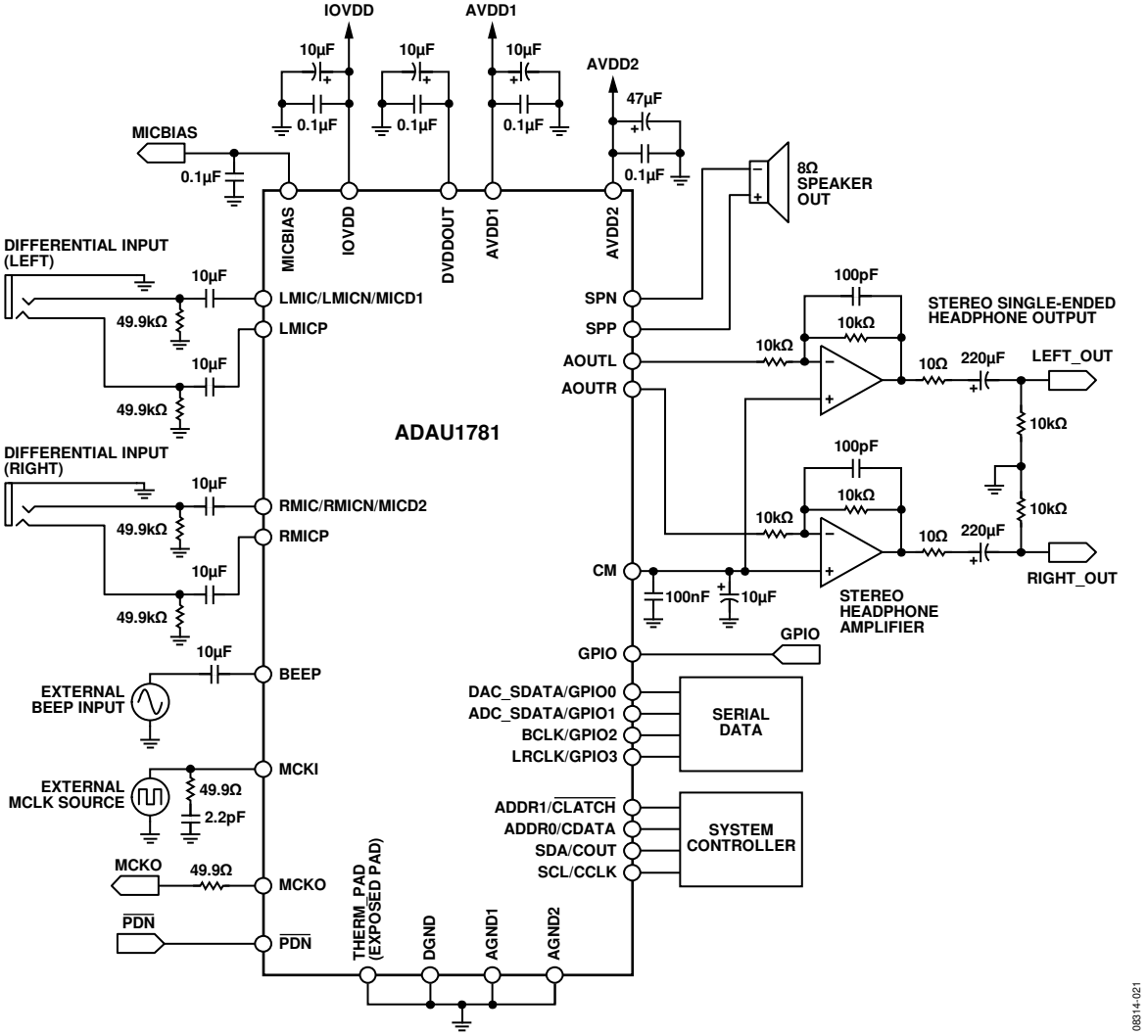

Figure 22. System Block Diagram with Differential Inputs

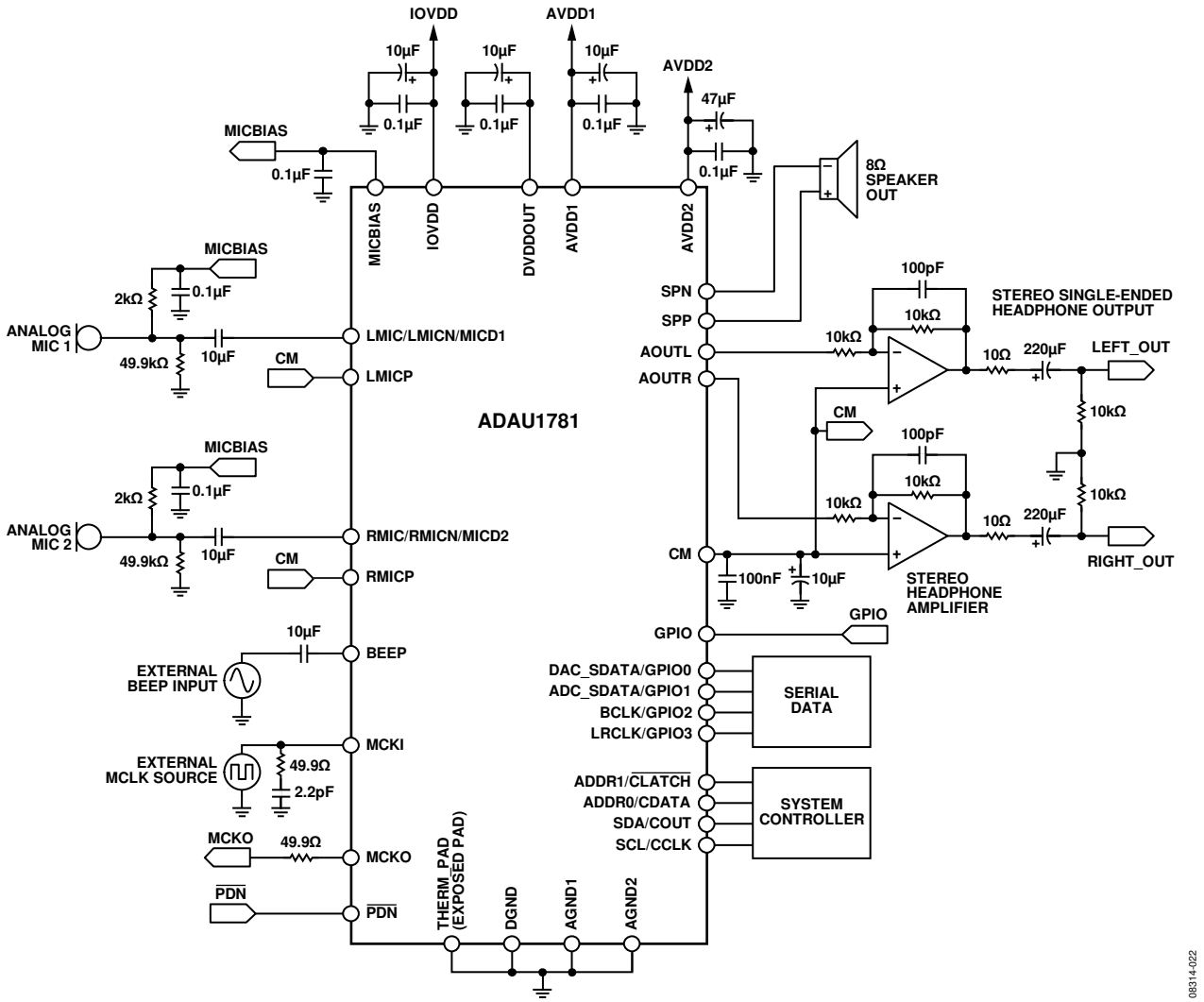

Figure 23. System Block Diagram with Analog Microphone Inputs

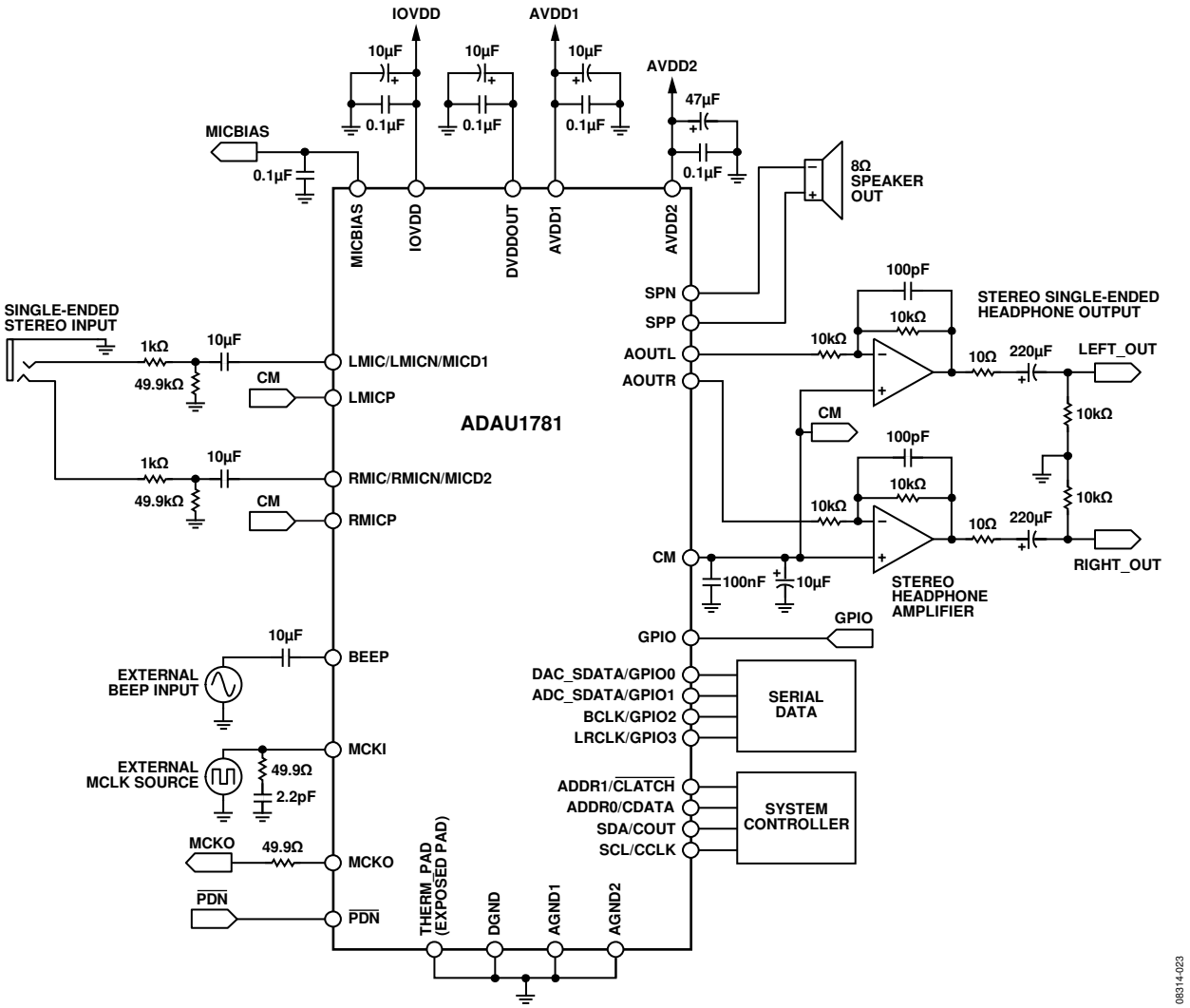

Figure 24. System Block Diagram with Single-Ended Stereo Line Inputs

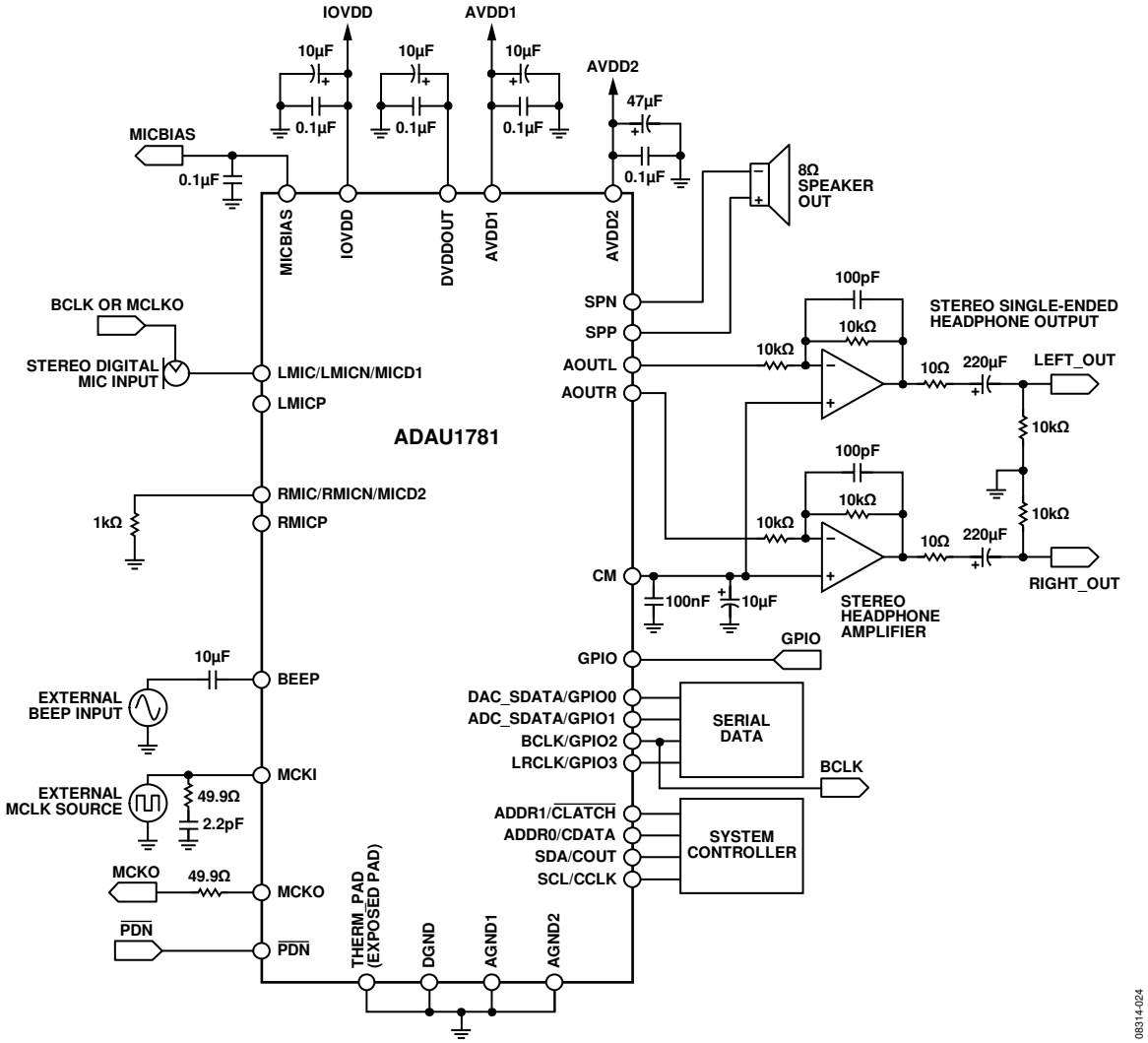

Figure 25. System Block Diagram with Stereo Digital Microphone Inputs

THEORY OF OPERATION

The ADAU1781 is a low power audio codec with an integrated, programmable SigmaDSP audio processing core. It is an all-in-one package that offers high quality audio, low power, small size, and many advanced features. The stereo ADC and stereo DAC each have a dynamic range (DNR) performance of at least 96.5 dB and a total harmonic distortion plus noise (THD + N) performance of at least −90 dB. The serial data port is compatible with I²S, left-justified, right-justified, and TDM modes for interfacing to digital audio data. The operating voltage range is 1.8 V to 3.65 V, with an on-board regulator generating the internal digital supply voltage.

The record path includes very flexible input configurations that can accept differential or single-ended analog microphone inputs as well as two stereo digital microphone inputs. There is also a beep input pin (BEEP) dedicated to analog beep signals that are common in digital still camera applications. A microphone bias pin that can power electrets-type microphones is also available. Each input signal has its own programmable gain amplifier (PGA) for input volume adjustment. An automatic level control (ALC) can be implemented in the SigmaDSP audio processing core to maintain a constant input recording volume.

The ADCs and DACs are high quality, 24-bit Σ-Δ converters that operate at selectable 64× or 128× oversampling rates. The base sampling rate of the converters is set by the input clock rate and can be further scaled with the converter control register settings. The converters can operate at sampling frequencies from 8 kHz to 96 kHz. The ADCs and DACs also include very fine-step digital volume controls.

The playback path allows input signals and DAC outputs to be mixed into speaker and/or line outputs. The speaker driver is capable of driving 400 mW into an 8 Ω load.

The SigmaDSP audio processing core can be programmed to enhance the audio quality and improve the end-user experience. The flexibility offered by the SigmaDSP core allows this codec to be used for a wide variety of low power applications. Signal processing blocks available for use in the SigmaDSP core include the following:

- Dynamics processing, including compressors, expanders, gates, and limiters
- Chime, tone, and noise generators
- Enhanced stereo capture (ESC)
- Wind noise detection and filtering
- Stereo spatialization
- Dynamic bass
- Loudness
- Filtering, including crossover, equalization, and notch
- GPIO controls
- Mixers and multiplexers
- Volume controls and mute

The ADAU1781 can generate its internal clocks from a wide range of input clocks by using the on-board fractional PLL. The PLL accepts inputs from 11 MHz to 20 MHz.

The ADAU1781 is provided in a small, 32-lead, 5 mm × 5 mm lead frame chip scale package (LFCSP) with an exposed bottom pad.