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FEATURES

- Differential or single-ended voltage DAC output
- 114 dB DAC dynamic range, A-weighted, differential
- 97 dB total harmonic distortion plus noise (THD + N), differential
- 110 dB DAC dynamic range, A-weighted, single-ended
- 95 dB THD + N, single-ended
- 2.5 V digital and 3.3 V analog and input/output (I/O) supplies
- 299 mW total quiescent power
- Phase-locked loop (PLL) generated or direct master clock
- Low electromagnetic interference (EMI) design
- Linear regulator driver to generate digital supply
- Supports 24-bit and 32 kHz to 192 kHz sample rates
- Low propagation 192 kHz sample rate mode
- Log volume control with autoramp function
- Temperature sensor with digital readout $\pm 3^{\circ}\text{C}$ accuracy
- SPI and I²C controllable for flexibility
- Software-controllable clickless mute
- Software power-down
- Right justified, left justified, I²S, and TDM modes
- Master and slave modes with up to 16-channel input/output
- 80-lead LQFP package
- Qualified for automotive applications

APPLICATIONS

- Automotive audio systems
- Home theater systems
- Digital audio effects processors

GENERAL DESCRIPTION

The ADAU1966A is a high performance, single-chip digital-to-analog converter (DAC) that provides 16 DACs with differential or single-ended outputs using the Analog Devices, Inc., patented multibit sigma-delta (Σ - Δ) architecture. A serial peripheral interface (SPI)/I²C port is included, allowing a microcontroller to adjust volume and many other parameters. The ADAU1966A operates from 2.5 V digital and 3.3 V analog supplies. A linear regulator is included to generate the digital supply voltage from the analog supply voltage. The ADAU1966A is available in an 80-lead LQFP.

The ADAU1966A is designed for low EMI. This consideration is apparent in both the system and circuit design architectures. By using the on-board PLL to derive the internal master clock from an external left-right frame clock (LRCLK), the ADAU1966A can eliminate the need for a separate high frequency master clock and can be used with or without a bit clock. The DACs are designed using the latest Analog Devices continuous time architectures to further minimize EMI. By using 2.5 V digital supplies, power consumption is minimized, and the digital waveforms are a smaller amplitude, further reducing emissions.

Note that throughout this data sheet, multifunction pins, such as SCLK/SCL, are referred to by the entire pin name or by a single function of the pin, for example, SCLK, when only that function is relevant.

FUNCTIONAL BLOCK DIAGRAM

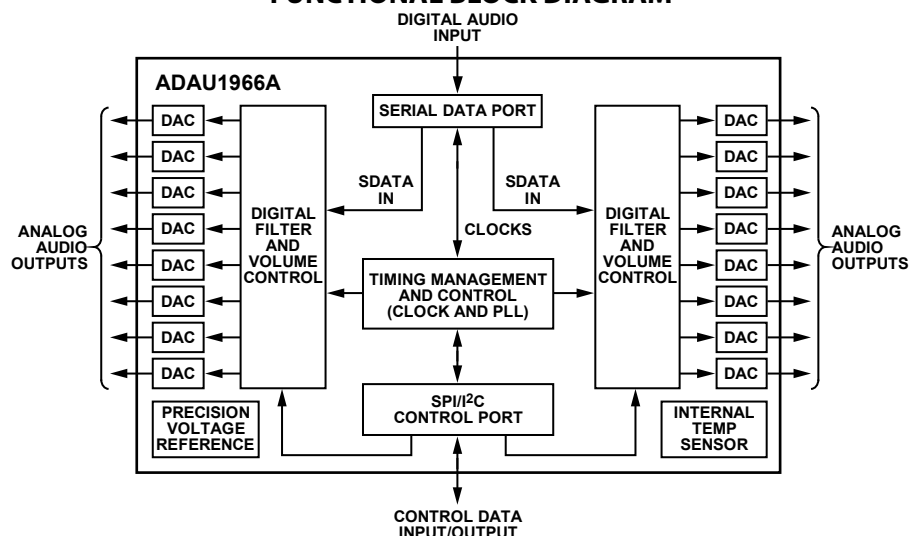


Figure 1.

Rev. A

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COMPARABLE PARTS

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EVALUATION KITS

- ADAU1962A/ADAU1966A Evaluation Board

DOCUMENTATION

Data Sheet

- ADAU1966A: 16-Channel, High Performance, 192 kHz, 24-Bit DAC Data Sheet

User Guides

- UG-564: Evaluating the ADAU1962A/ADAU1966A High Performance, Low Power Multibit Sigma-Delta DAC

TOOLS AND SIMULATIONS

- ADAU1966A IBIS Model

DESIGN RESOURCES

- ADAU1966A Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADAU1966A EngineerZone Discussions.

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REVISION HISTORY

3/16—Rev. 0 to Rev. A	
Changes to Table 4	5

8/13—Revision 0: Initial Version

SPECIFICATIONS

Performance of all channels is identical, exclusive of the interchannel gain mismatch and interchannel phase deviation specifications. Master clock = 12.288 MHz (48 kHz f_s , $256 \times f_s$ mode), input sample rate = 48 kHz, measurement bandwidth = 20 Hz to 20 kHz, word width = 24 bits, load capacitance (digital output) = 20 pF, load current (digital output) = ± 1 mA or $1.5 \text{ k}\Omega$ to $\frac{1}{2}$ DVDD supply, input voltage high = 2.0 V, input voltage low = 0.8 V, analog audio output resistive load = 3100Ω per pin, unless otherwise noted.

ANALOG PERFORMANCE SPECIFICATIONS: $T_A = 25^\circ\text{C}$

Specifications guaranteed at supply voltages of AVDDx = 3.3 V, DVDD = 2.5 V, ambient temperature¹ (T_A) = 25°C , unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL-TO-ANALOG CONVERTERS					
Dynamic Range (DNR)	20 Hz to 20 kHz, -60 dB input				
No Filter (RMS)	Differential output	105.5	111		dB
With A-Weighted Filter (RMS)	Differential output	108.5	114		dB
No Filter (RMS)	Single-ended output	102.5	107		dB
With A-Weighted Filter (RMS)	Single-ended output	105.5	110		dB
Total Harmonic Distortion + Noise					
Differential Output	Two channels running -1 dBFS		-97	-85	dB
	All channels running -1 dBFS		-97	-85	dB
Single-Ended Output	Two channels running -1 dBFS		-95	-80	dB
	All channels running -1 dBFS		-95	-80	dB
Full-Scale Differential Output Voltage			2.00 (2.83)		V rms (V p-p)
Full-Scale Single-Ended Output Voltage			1.00 (1.41)		V rms (V p-p)
Gain Error		-10		+10	%
Offset Error		-25	-6	+25	mV
Gain Drift		-30		+30	ppm/ $^\circ\text{C}$
Interchannel Isolation			100		dB
Interchannel Phase Deviation			0		Degrees
Volume Control Step			0.375		dB
Volume Control Range			95.25		dB
De-Emphasis Gain Error				± 0.6	dB
Output Resistance at Each Pin			33		Ω
REFERENCE					
Temperature Sensor Reference Voltage	TS_REF pin		1.50		V
Common-Mode Reference Output	CM pin	1.40	1.50	1.56	V
External Reference Voltage Source	CM pin	1.40	1.50	1.56	V
REGULATOR					
Input Supply Voltage	VSUPPLY pin	3.14	3.3	3.46	V
Regulated Output Voltage	VSENSE pin	2.25	2.50	2.59	V
TEMPERATURE SENSOR					
Temperature Accuracy		-3		+3	$^\circ\text{C}$
Temperature Readout Range		-60		+140	$^\circ\text{C}$
Temperature Readout Step Size			1		$^\circ\text{C}$
Temperature Sample Rate		0.25		6	Hz

¹ Functionally guaranteed at -40°C to $+125^\circ\text{C}$, case temperature.

ANALOG PERFORMANCE SPECIFICATIONS: T_A = 105°C

Specifications guaranteed at supply voltages of AVDDx = 3.3 V, DVDD = 2.5 V, ambient temperature¹ (T_A) = 105°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL-TO-ANALOG CONVERTERS					
Dynamic Range (DNR)	20 Hz to 20 kHz, –60 dB input				
No Filter (RMS)	Differential output	106.5	110		dB
With A-Weighted Filter (RMS)	Differential output	109.5	113		dB
No Filter (RMS)	Single-ended output	101.5	108		dB
With A-Weighted Filter (RMS)	Single-ended output	104.5	110		dB
Total Harmonic Distortion + Noise					
Differential Output	Two channels running –1 dBFS		–92	–83	dB
	All channels running –1 dBFS		–92	–83	dB
Single-Ended Output	Two channels running –1 dBFS		–90	–80	dB
	All channels running –1 dBFS		–90	–80	dB
Full-Scale Differential Output Voltage			2.00 (2.83)		V rms (V p-p)
Full-Scale Single-Ended Output Voltage			1.00 (1.41)		V rms (V p-p)
Gain Error		–10		+10	%
Offset Error		–25	–6	+25	mV
Gain Drift		–30		+30	ppm/°C
Interchannel Isolation			100		dB
Interchannel Phase Deviation			0		Degrees
Volume Control Step			0.375		dB
Volume Control Range			95.25		dB
De-Emphasis Gain Error				±0.6	dB
Output Resistance at Each Pin			33		Ω
REFERENCE					
Temperature Sensor Reference Voltage	TS_REF pin		1.50		V
Common-Mode Reference Output	CM pin	1.40	1.50	1.56	V
External Reference Voltage Source	CM pin	1.40	1.50	1.56	V
REGULATOR					
Input Supply Voltage	VSUPPLY pin	3.14	3.3	3.46	V
Regulated Output Voltage	VSENSE pin	2.25	2.50	2.55	V
TEMPERATURE SENSOR					
Temperature Accuracy		–3		+3	°C
Temperature Readout Range		–60		+140	°C
Temperature Readout Step Size			1		°C
Temperature Sample Rate		0.25		6	Hz

¹ Functionally guaranteed at –40°C to +125°C, case temperature.

CRYSTAL OSCILLATOR SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit
TRANSCONDUCTANCE				
T _A = 25°C	6.4	7 to 10	14	mmhos
T _A = 105°C	5.2	7.5 to 8.5	12	mmhos

DIGITAL INPUT/OUTPUT SPECIFICATIONS

–40°C < T_A < +105°C, IOVDD = 3.3 V ± 5%, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUT					
High Level Input Voltage (V _{IH})		0.7 × IOVDD			V
Low Level Input Voltage (V _{IL})				0.3 × IOVDD	V
Input Leakage	I _{IH} at V _{IH} = 3.3 V I _{IL} at V _{IL} = 0 V			10	μA
				10	μA
INPUT CAPACITANCE				5	pF
DIGITAL OUTPUT					
High Level Output Voltage (V _{OH})	I _{OH} = 1 mA	0.8 × IOVDD			V
Low Level Output Voltage (V _{OL})	I _{OL} = 1 mA			0.1 × IOVDD	V

POWER SUPPLY SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLIES					
Voltage	AVDDx DVDD PLLVDD IOVDD VSUPPLY	3.14 2.25 2.25 3.14 3.14	3.3 2.5 2.5 3.3 3.3	3.46 3.46 3.46 3.46 3.46	V V V V V
Analog Current	AVDDx = 3.3 V				
Normal Operation			60		mA
Power-Down			1		μA
Digital Current	DVDD = 2.5 V				
Normal Operation	f _s = 48 kHz to 192 kHz		30		mA
Power-Down	No MCLK or I ² S		4		μA
PLL Current	PLLVDD = 2.5 V				
Normal Operation	f _s = 48 kHz to 192 kHz		5		mA
Power-Down			1		μA
Input/Output Current	IOVDD = 3.3 V				
Normal Operation			4		mA
Power-Down			1		μA
QUIESCENT DISSIPATION—DITHER INPUT					
Operation	MCLK = 256 × f _s , 48 kHz				
All Supplies	AVDDx = 3.3 V, DVDD/PLLVDD = 2.5 V, IOVDD = 3.3 V		299		mW
Analog Supply	AVDDx = 3.3 V, 12.4 mW per channel		198		mW
Digital Supply	DVDD = 2.5 V		75		mW
PLL Supply	PLLVDD = 2.5 V		13		mW
I/O Supply	IOVDD = 3.3 V		13		mW
Power-Down, All Supplies			0		mW
POWER SUPPLY REJECTION RATIO					
Signal at Analog Supply Pins	1 kHz, 200 mV p-p, differential 20 kHz, 200 mV p-p, differential 1 kHz, 200 mV p-p, single-ended 20 kHz, 200 mV p-p, single-ended		88 85 85 75		dB dB dB dB

DIGITAL FILTERS

Table 6.

Parameter	Mode	Factor	Min	Typ	Max	Unit
DAC INTERPOLATION FILTER						
Pass Band	48 kHz mode, typical at 48 kHz	$0.4535 \times f_s$		22		kHz
	96 kHz mode, typical at 96 kHz	$0.3646 \times f_s$	35			kHz
	192 kHz mode, typical at 192 kHz	$0.3646 \times f_s$		70		kHz
Pass-Band Ripple	48 kHz mode, typical at 48 kHz				± 0.01	dB
	96 kHz mode, typical at 96 kHz				± 0.05	dB
	192 kHz mode, typical at 192 kHz				± 0.1	dB
Transition Band	48 kHz mode, typical at 48 kHz	$0.5 \times f_s$		24		kHz
	96 kHz mode, typical at 96 kHz	$0.5 \times f_s$		48		kHz
	192 kHz mode, typical at 192 kHz	$0.5 \times f_s$		96		kHz
Stop Band	48 kHz mode, typical at 48 kHz	$0.5465 \times f_s$		26		kHz
	96 kHz mode, typical at 96 kHz	$0.6354 \times f_s$		61		kHz
	192 kHz mode, typical at 192 kHz	$0.6354 \times f_s$		122		kHz
Stop-Band Attenuation	48 kHz mode, typical at 48 kHz		68			dB
	96 kHz mode, typical at 96 kHz		68			dB
	192 kHz mode, typical at 192 kHz		68			dB
Propagation Delay	48 kHz mode, typical at 48 kHz	$25/f_s$		521		μs
	96 kHz mode, typical at 96 kHz	$11/f_s$		115		μs
	192 kHz mode, typical at 192 kHz	$8/f_s$		42		μs
	192 kHz low propagation delay mode, typical at 192 kHz	$2/f_s$		10		μs

TIMING SPECIFICATIONS

$-40^\circ C < T_A < +105^\circ C$, DVDD = 2.5 V \pm 10%, unless otherwise noted.

Table 7.

Parameter ¹	Description	Min	Typ	Max	Unit
INPUT MASTER CLOCK (MCLKI) AND RESET					
t_{MH}	Master clock duty cycle, DAC clock source = PLL clock at $256 \times f_s$, $384 \times f_s$, $512 \times f_s$, and $768 \times f_s$	40		60	%
	DAC clock source = direct MCLKI at $512 \times f_s$ (bypass on-chip PLL)	40		60	%
f_{MCLK}	MCLKI frequency of the MCLKI/XTALI pin, PLL mode	6.9		40.5	MHz
	Direct MCLKI $512 \times f_s$ mode			27.1	MHz
f_{BCLK}	DBCLK pin frequency, PLL mode			27.0	MHz
t_{PDR}	Low	15			ns
t_{PDRR}	Recovery, reset to active output	300			ms
PLL					
Lock Time	MCLKI input of the MCLKI/XTALI pin			10	ms
	DLRCLK pin input			50	ms
Output Duty Cycle, MCLKO Pin	$256 \times f_s$ VCO clock	40		60	%

Parameter ¹	Description	Min	Typ	Max	Unit
SPI PORT					
f _{SCLK}	See Figure 19 SCLK frequency, not shown in Figure 19			10	MHz
t _{SCH}	SCLK high	35			ns
t _{SCL}	SCLK low	35			ns
t _{MOS}	MOSI setup, time to SCLK rising	10			ns
t _{MOH}	MOSI hold, time from SCLK rising	10			ns
t _{SSS}	\overline{SS} setup, time to SCLK rising	10			ns
t _{SSH}	\overline{SS} hold, time from SCLK falling	10			ns
t _{SSHIGH}	\overline{SS} high	10			ns
t _{MIE}	MISO enable from \overline{SS} falling			30	ns
t _{MID}	MISO delay from SCLK falling			30	ns
t _{MIH}	MISO hold from SCLK falling, not shown in Figure 19	30			ns
t _{MITS}	MISO tristate from \overline{SS} rising			30	ns
I²C					
f _{SCL}	See Figure 2 and Figure 15 SCL clock frequency			400	kHz
t _{SCLL}	SCL low	1.3			μs
t _{SCLH}	SCL high	0.6			μs
t _{SCS}	Setup time (start condition), relevant for repeated start condition	0.6			μs
t _{SCH}	Hold time (start condition), first clock generated after this period	0.6			μs
t _{SSH}	Setup time (stop condition)	0.6			μs
t _{DS}	Data setup time	100			ns
t _{SR}	SDA and SCL rise time			300	ns
t _{SF}	SDA and SCL fall time			300	ns
t _{BFT}	Bus-free time between stop and start	1.3			μs
DAC SERIAL PORT					
t _{DBH}	See Figure 21 DBCLK high, slave mode	10			ns
t _{DBL}	DBCLK low, slave mode	10			ns
t _{DLS}	DLRCLK setup, time to DBCLK rising, slave mode	10			ns
t _{DLH}	DLRCLK hold from DBCLK rising, slave mode	5			ns
t _{DLSK}	DLRCLK skew from DBCLK falling, master mode, not shown in Figure 21	-8		+8	ns
t _{DDS}	DSDATAx setup to DBCLK rising	10			ns
t _{DDH}	DSDATAx hold from DBCLK rising	5			ns

¹ The timing specifications may refer to single functions of multifunction pins, such as the SCL function of the SCLK/SCL pin.

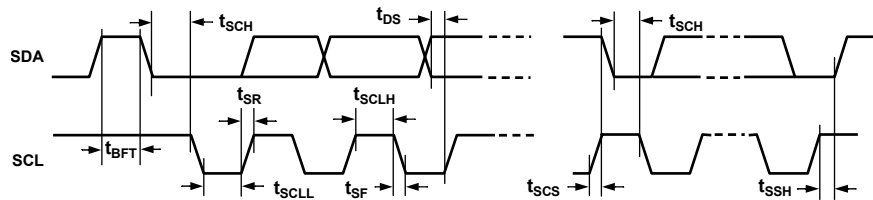


Figure 2. I²C Timing Diagram

11238-002

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Analog (AVDDx)	-0.3 V to +3.6 V
Input/Output (IOVDD)	-0.3 V to +3.6 V
Digital (DVDD)	-0.3 V to +3.6 V
PLL (PLLVD)	-0.3 V to +3.6 V
VSUPPLY	-0.3 V to +3.6 V
Input Current (Except Supply Pins)	±20 mA
Analog Input Voltage (Signal Pins)	-0.3 V to AVDDx + 0.3 V
Digital Input Voltage (Signal Pins)	-0.3 V to DVDD + 0.3 V
Operating Temperature Range (Case)	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} represents junction-to-ambient thermal resistance, and θ_{JC} represents the junction-to-case thermal resistance. All characteristics are for a 4-layer board with a solid ground plane.

Table 9. Thermal Resistance

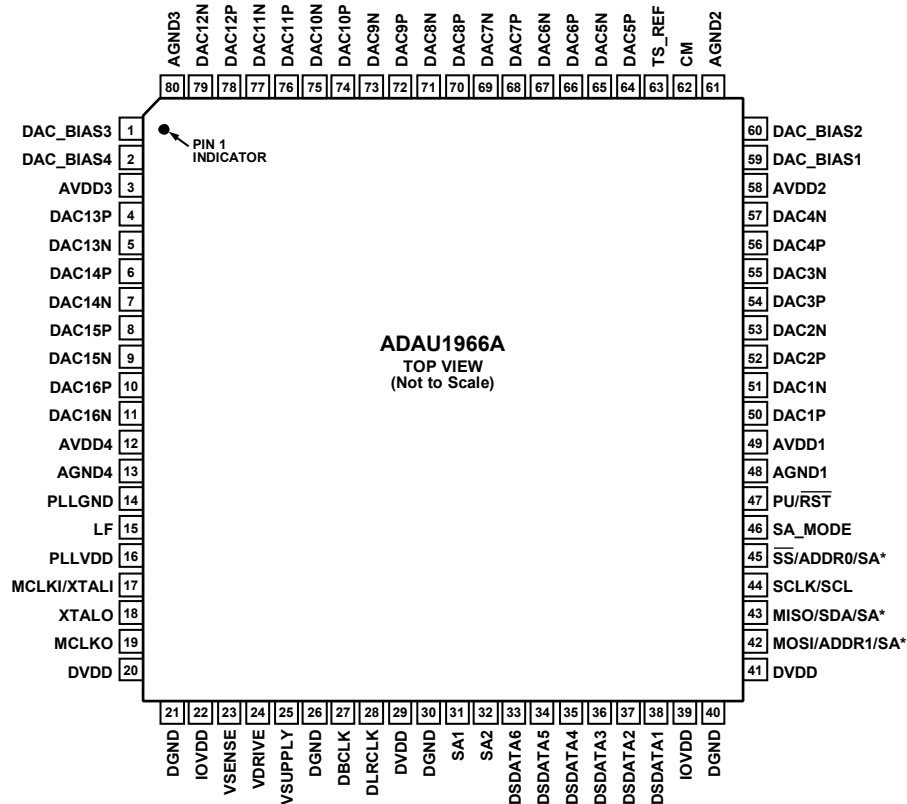
Package Type	θ_{JA}	θ_{JC}	Unit
80-Lead LQFP	42.3	10.0	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



*SEE TABLE 13 FOR SA_MODE SETTINGS.

Figure 3. Pin Configuration

11298-003

Table 10. Pin Function Descriptions

Pin No.	Mnemonic ^{1,2}	Type ³	Description
1	DAC_BIAS3	I	DAC Bias 3. AC couple with a 470 nF to AGND3.
2	DAC_BIAS4	I	DAC Bias 4. AC couple with a 470 nF to AVDD3.
3	AVDD3	PWR	Analog Power.
4	DAC13P	O	DAC13 Positive Output.
5	DAC13N	O	DAC13 Negative Output.
6	DAC14P	O	DAC14 Positive Output.
7	DAC14N	O	DAC14 Negative Output.
8	DAC15P	O	DAC15 Positive Output.
9	DAC15N	O	DAC15 Negative Output.
10	DAC16P	O	DAC16 Positive Output.
11	DAC16N	O	DAC16 Negative Output.
12	AVDD4	PWR	Analog Power.
13	AGND4	GND	Analog Ground.
14	PLLGND	GND	PLL Ground.
15	LF	O	PLL Loop Filter. Reference the LF pin to PLLVDD.
16	PLLVDD	PWR	PLL Power. Apply 2.5 V to power the PLL.
17	MCLKI/XTALI	I	Master Clock Input/Input to Crystal Inverter. This is a multifunction pin.
18	XTALO	O	Output from Crystal Inverter.
19	MCLKO	O	Master Clock Output.

Pin No.	Mnemonic ^{1,2}	Type ³	Description
20, 29, 41	DVDD	PWR	Digital Power, 2.5 V.
21, 26, 30, 40	DGND	GND	Digital Ground.
22, 39	IOVDD	PWR	Power for Digital Input and Output Pins, 3.3 V.
23	VSENSE	I	2.5 V Regulator Output, Pass Transistor Collector. Bypass VSENSE with a 10 μ F capacitor in parallel with a 100 nF capacitor.
24	VDRIVE	O	Pass Transistor Base Driver.
25	VSUPPLY	I	3.3 V Voltage Regulator Input , Pass Transistor Emitter . Bypass VSUPPLY with a 10 μ F capacitor in parallel with a 100 nF capacitor.
27	DBCLK	I/O	Bit Clock for DACs.
28	DLRCLK	I/O	Frame Clock for DACs.
31	SA1	I	Standalone Mode, Time Domain Multiplexed (SA_MODE TDM) State. See the Standalone Mode section, Table 13, and Table 14, for more information.
32	SA2	I	Standalone Mode, Time Domain Multiplexed (SA_MODE TDM) State. See the Standalone Mode section, Table 13, and Table 14, for more information.
33	DSDATA6	I	DAC11 and DAC 12 Serial Data Input.
34	DSDATA5	I	DAC9 and DAC 10 Serial Data Input.
35	DSDATA4	I	DAC7 and DAC 8 Serial Data Input.
36	DSDATA3	I	DAC5 and DAC 6 Serial Data Input.
37	DSDATA2	I	DAC3 and DAC 4 Serial Data Input.
38	DSDATA1	I	DAC1 and DAC 2 Serial Data Input.
42	MOSI/ADDR1/SA	I	Master Output Slave Input (SPI)/Address 1 (I ² C)/SA_MODE State (see the Standalone Mode section and Table 13).
43	MISO/SDA/SA	I/O	Master Output Slave Input (SPI)/Control Data Input (I ² C)/SA_MODE State (see the Standalone Mode section and Table 13).
44	SCLK/SCL	I	Serial Clock Input (SPI)/Control Clock Input (I ² C).
45	\overline{SS} /ADDR0/SA	I	Slave Select (SPI) (Active Low)/Address 0 (I ² C)/SA_MODE State (see the Standalone Mode section and Table 13).
46	SA_MODE	I	Standalone Mode. This pin allows mode control of ADAU1966A using Pin 42, Pin 43, Pin 45, Pin 31, and Pin 32 (high active). See Table 13 and Table 14 for more information).
47	PU/ \overline{RST}	I	Power-Up/Reset (Active Low). See Power-Up and Reset section for more information.
48	AGND1	GND	Analog Ground.
49	AVDD1	PWR	Analog Power.
50	DAC1P	O	DAC1 Positive Output.
51	DAC1N	O	DAC1 Negative Output.
52	DAC2P	O	DAC2 Positive Output.
53	DAC2N	O	DAC2 Negative Output.
54	DAC3P	O	DAC3 Positive Output.
55	DAC3N	O	DAC3 Negative Output.
56	DAC4P	O	DAC4 Positive Output.
57	DAC4N	O	DAC4 Negative Output.
58	AVDD2	PWR	Analog Power.
59	DAC_BIAS1	I	DAC Bias 1. AC couple Pin 59 with a 470 nF capacitor to AVDD2.
60	DAC_BIAS2	I	DAC Bias 2. AC couple Pin 60 with a 470 nF capacitor to AGND2.
61	AGND2	GND	Analog Ground.
62	CM	O	Common-Mode Reference Filter Capacitor Connection. Bypass the CM pin with a 10 μ F capacitor in parallel with a 100 nF capacitor to AGND2. This reference can be shut off in the PLL_CLK_CTRL1 register (Register 0x01) and the pin can be driven with an outside voltage source.
63	TS_REF	O	Voltage Reference Filter Capacitor Connection. Bypass Pin 63 with a 10 μ F capacitor in parallel with a 100 nF capacitor to AGND2.
64	DAC5P	O	DAC5 Positive Output.
65	DAC5N	O	DAC5 Negative Output.
66	DAC6P	O	DAC6 Positive Output.
67	DAC6N	O	DAC6 Negative Output.
68	DAC7P	O	DAC7 Positive Output.

Pin No.	Mnemonic ^{1,2}	Type ³	Description
69	DAC7N	O	DAC7 Negative Output.
70	DAC8P	O	DAC8 Positive Output.
71	DAC8N	O	DAC8 Negative Output.
72	DAC9P	O	DAC9 Positive Output.
73	DAC9N	O	DAC9 Negative Output.
74	DAC10P	O	DAC10 Positive Output.
75	DAC10N	O	DAC10 Negative Output.
76	DAC11P	O	DAC11 Positive Output.
77	DAC11N	O	DAC11 Negative Output.
78	DAC12P	O	DAC12 Positive Output.
79	DAC12N	O	DAC12 Negative Output.
80	AGND3	GND	Analog Ground.

¹ AVDD1, AVDD2, AVDD3, and AVDD4 are referred to elsewhere in this document as AVDDx when AVDDx means any or all of the AVDD pins.

² DAC Channel 1 to DAC Channel 12 pins are referred to elsewhere in this document as DACx, DACxP, or DACxN when it means any or all of the DAC channel pins.

³ I = input, O = output, I/O = input/output, PWR = power, and GND = ground.

TYPICAL PERFORMANCE CHARACTERISTICS

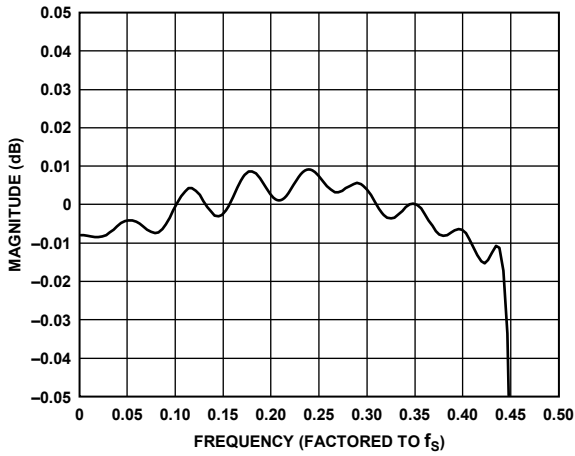


Figure 4. DAC Pass-Band Filter Response, 48 kHz

11298-004

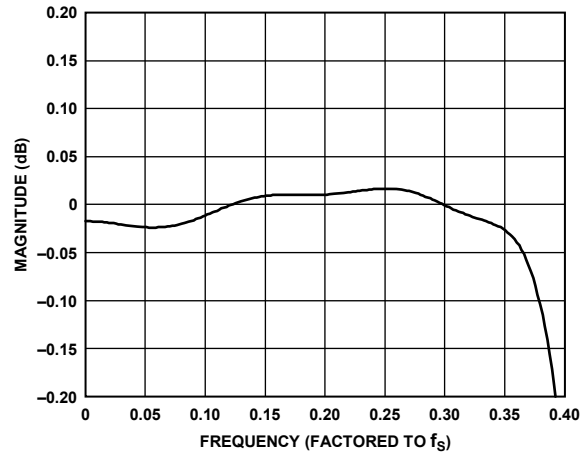


Figure 6. DAC Pass-Band Filter Response, 96 kHz

11298-006

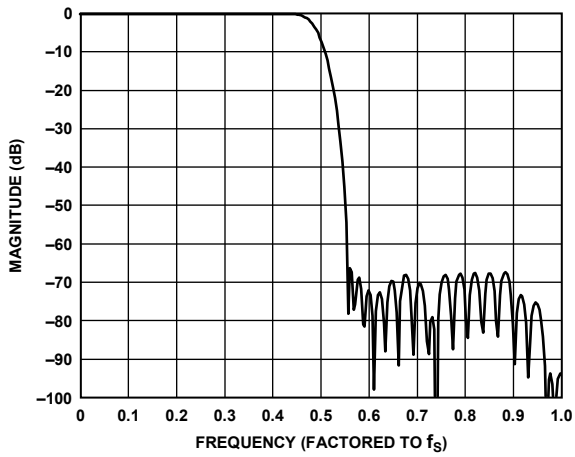


Figure 5. DAC Stop-Band Filter Response, 48 kHz

11298-005

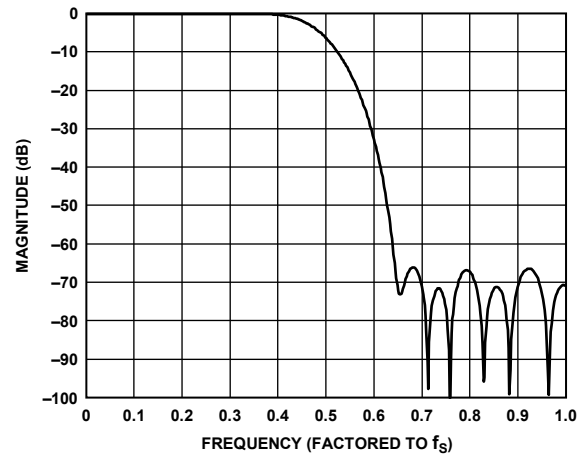


Figure 7. DAC Stop-Band Filter Response, 96 kHz

11298-007

TYPICAL APPLICATION CIRCUITS

Typical application circuits are shown in Figure 8 to Figure 13. Recommended loop filters for DLRCLK and MCLKI/XTALI modes of the PLL reference are shown in Figure 8. Output filters for the DAC outputs are shown in Figure 10 to Figure 13, and an external regulator circuit is shown in Figure 9. When pins for multiple outputs are referred to generically in this datasheet, there is an x in place of the number. For example, DACxP refers to DAC1P through DAC16P.

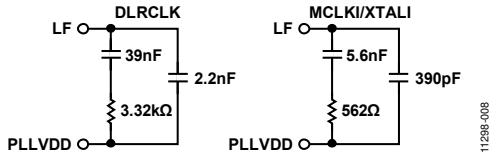


Figure 8. Recommended Loop Filters for DLRCLK and MCLKI/XTALI PLL Reference Modes

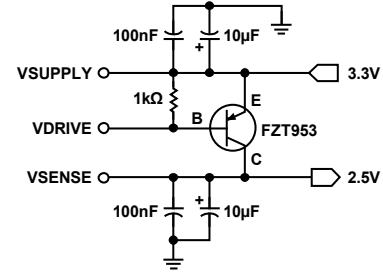


Figure 9. Recommended 2.5 V Regulator Circuit

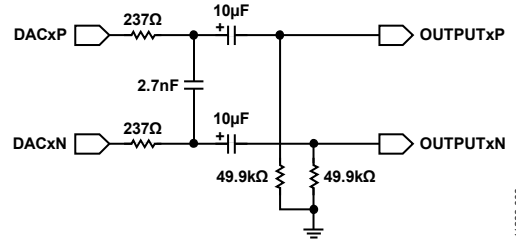


Figure 10. Typical DAC Output Passive Filter Circuit (Differential)

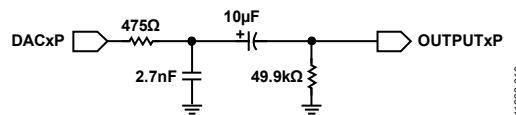


Figure 11. Typical DAC Output Passive Filter Circuit (Single-Ended)

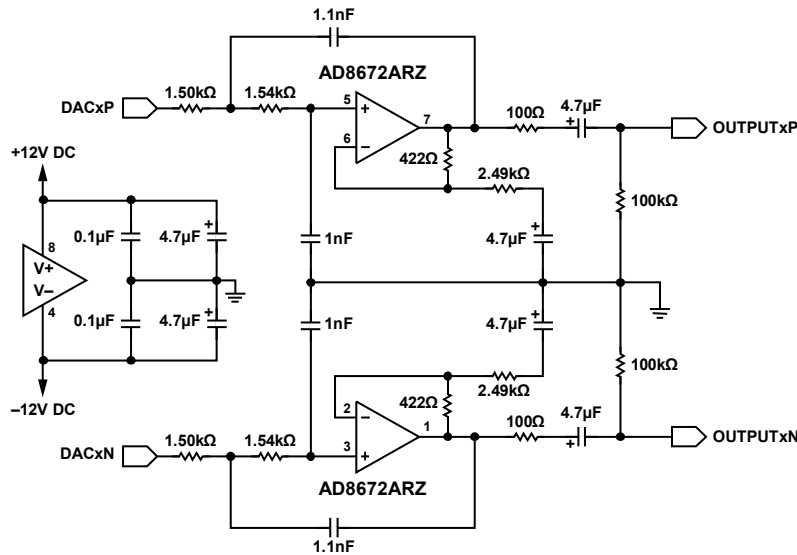


Figure 12. Typical DAC Output Active Filter Circuit (Differential)

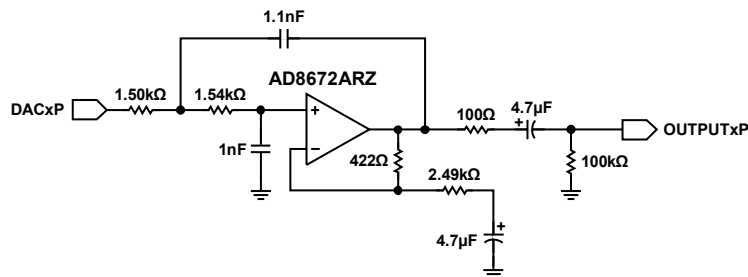


Figure 13. Typical DAC Output Active Filter Circuit (Single-Ended)

THEORY OF OPERATION

DACs

The 16 ADAU1966A DAC channels are differential for improved noise and distortion performance and are voltage output for simplified connection. The DACs include on-chip digital interpolation filters with 68 dB stop-band attenuation and linear phase response, operating at an oversampling ratio of 256× (48 kHz range), 128× (96 kHz range), or 64× (192 kHz range). Each channel has its own independently programmable attenuator, adjustable in 255 steps in increments of 0.375 dB. Digital inputs are supplied through six serial data input pins (two channels on each pin), a common frame clock (DLRCLK), and a bit clock (DBCLK). Alternatively, any one of the time domain multiplexed (TDM) modes can be used to access up to 16 channels on a single TDM data line.

The ADAU1966A has a low propagation delay mode; this mode is an option for an f_s of 192 kHz and is enabled in Register DAC_CTRL0[2:1]. By setting these bits to 0b11, the propagation delay is reduced by the amount listed in Table 6. The shorter delay is achieved by reducing the amount of digital filtering; the negative impact of selecting this mode is reduced audio frequency response and increased out-of-band energy.

Because AVDDx is supplied with 3.3 V, each analog output pin has a nominal common-mode (CM) dc level of 1.5 V. With a 0 dB full-scale digital input signal, each pin swings approximately ±1.42 V peak (2.83 V p-p and 2 V rms). Therefore, the voltage swing differentially across the two pins is 5.66 V p-p (4 V rms). The differential analog outputs require a single-order passive differential resistor-capacitor (RC) filter only to provide the specified DNR performance; see Figure 10 or Figure 11 for an example filter. The outputs can easily drive differential inputs on a separate printed circuit board (PCB) through cabling as well as differential inputs on the same PCB.

If more signal level is required, or if a more robust filter is needed, a single op amp gain stage designed as a second-order, low-pass Bessel filter can be used to remove the high frequency out-of-band noise present on each pin of the differential outputs. The choice of components and design of this circuit is critical to yield the full DNR of the DACs (see the recommended passive and active circuits in Figure 10, Figure 11, Figure 12, and Figure 13). The differential filter can be built into an active difference amplifier to provide a single-ended output with gain, if necessary. Note that the use of op amps with low slew rate or low bandwidth can cause high frequency noise and tones to fold down into the audio band; exercise care when selecting these components.

The ADAU1966A offers control over the analog performance of the DACs; it is possible to program the registers to reduce the

power consumption with the trade-off of lower SNR and THD + N. The reduced power consumption is the result of changing the internal bias current to the analog output amplifiers.

Register DAC_POWER1 to Register DAC_POWER4 present four basic settings for the DAC power vs. performance in each of the 16 channels: best performance, good performance, low power, and lowest power. Alternatively, in Register PLL_CLK_CTRL1[7:6], the LOPWR_MODE bits offer global control over the power and performance for all 16 channels. To select the low power or lowest power settings, set Bit 7 and Bit 6 of the DAC_POWERx registers to 0b10 or 0b11, respectively. The default setting is 0b00. This setting allows the channels to be controlled individually using the DAC_POWERx registers. The data presented in Table 11 shows the result of setting all 16 channels to each of the four settings. The SNR and THD + N specifications are shown in relation to the measured performance of a device at the best performance setting.

The voltage at CM, the common-mode reference pin, can be used to bias the external op amps that buffer the output signals (see the Power Supply and Voltage Reference section).

CLOCK SIGNALS

Upon powering the ADAU1966A and asserting the PU/RST pin high, the part starts in either standalone mode (SA_MODE) or program mode, depending on the state of SA_MODE (Pin 46). The clock functionality of SA_MODE is described in the Standalone Mode section.

In program mode, the default for the ADAU1966A is for the MCLKO pin to feed a buffered output of the MCLKI signal on the MCLKI/XTALI pin. The default for the DLRCLK and DBCLK ports is slave mode; the DAC must be driven with a coherent set of master clock, frame clock, and bit clock signals to function.

The MCLKO pin can be programmed to provide different clock signals using Register PLL_CLK_CTRL1[5:4]. The default, 0b10, provides a buffered copy of the clock signal that is driving the MCLKI pin. Two modes, 0b00 and 0b01, provide low jitter clock signals.

The b00 setting yields a clock rate between 4 MHz and 6 MHz, and the b01 setting yields a clock rate between 8 MHz and 12 MHz. Both of these clock frequencies are scaled as ratios of the master clock automatically inside the ADAU1966A. As an example, an input to MCLKI of 8.192 MHz and a setting of 0b00 yield an MCLKO of $(8.192/2) = 4.096$ MHz. Alternatively, an input to MCLKI of 36.864 MHz and a setting of 0b01 yield an MCLKO frequency of $(36.864/3) = 12.288$ MHz. The 0b11 setting disables the MCLKO pin.

Table 11. DAC Power vs. Performance

Register Setting	Best Performance	Good Performance	Low Power	Lowest Power
Total AVDDx Current	60 mA	53 mA	47 mA	40 mA
SNR	Reference	-0.2 dB	-1.5 dB	-14.2 dB
THD + N (-1 dBFS Signal)	Reference	-1.8 dB	-3.0 dB	-5.8 dB

After the $\overline{\text{PU/RST}}$ pin is asserted high, the PLL_CLK_CTRLx registers (Register 0x00 and Register 0x01) can be programmed. The on-chip PLL can be selected to use the clock appearing at the MCLKI/XTALI pin at a frequency of 256, 384, 512, or 768 times the sample rate (f_s), referenced to the 48 kHz mode from the master clock select (MCS) setting, as described in Table 12.

In 96 kHz mode, the master clock frequency stays at the same absolute frequency; therefore, the actual multiplication rate is divided by 2. In 192 kHz mode, the actual multiplication rate is divided by 4.

For example, if the ADAU1966A is programmed in $256 \times f_s$ mode, the frequency of the master clock input is $256 \times 48 \text{ kHz} = 12.288 \text{ MHz}$. If the ADAU1966A is then switched to 96 kHz operation (by writing to DAC_CTRL0[2:1]), the frequency of the master clock remains at 12.288 MHz, which is an MCS ratio of $128 \times f_s$ in this example. Therefore, in 192 kHz mode, MCS becomes $64 \times f_s$. The internal clock for the digital core varies by mode: $512 \times f_s$ (48 kHz mode), $256 \times f_s$ (96 kHz mode), or $128 \times f_s$ (192 kHz mode). By default, the on-board PLL generates this internal master clock from an external clock.

The PLL must be powered and stable before using the ADAU1966A as a source for quality audio. The PLL is enabled by reset and does not require writing to the I²C or SPI port for normal operation.

With the PLL enabled, the performance of the ADAU1966A is not affected by jitter as high as a 300 ps rms time interval error

(TIE). When the internal PLL is disabled, use an independent crystal oscillator to generate the master clock.

When using the ADAU1966A in direct master clock mode, power down the PLL in the PDN_THRMSSENS_CTRL_1 register. For direct master clock mode, a frequency of $512 \times f_s$ (referenced to 48 kHz mode) must be fed into the MCLKI pin, and the CLK_SEL bit in the PLL_CLK_CTRL1 register must be set to 1. However, for the device to function, 2.5 V power must be connected to the PLLVDD pin.

The PLL of the ADAU1966A can also be programmed to run from an external LRCLK without an external master clock. Setting the PLLIN bits in the PLL_CLK_CTRL0 register to 0b01 and connecting the appropriate loop filter to the LF pin (see Figure 8), the ADAU1966A PLL generates all of the necessary internal clocks for operation with no external master clock. This mode reduces the number of high frequency signals in the design, reducing EMI emissions.

It is possible to further reduce EMI emissions of the circuit by using the internal bit clock generation setting of the BCLK_GEN bit in the DAC_CTRL1 register. Setting the BCLK_GEN bit to 1 (internal) and the SAI_MS bit to 0 (slave), the ADAU1966A generates its own bit clock; this configuration works with the PLL input register (PLL_CLK_CTRL0[7:6]) set to either MCLKI/XTALI or DLCLK. The clock on the DLCLK pin is the only required clock in DLCLK PLL mode.

Table 12. MCS and f_s Modes

Frequency Sample Select DAC_CTRL0[2:1]		Master Clock Select (MCS), PLL_CLK_CTRL0[2:1]							
		Setting 0, 0b00		Setting 1, 0b01		Setting 2, 0b10		Setting 3, 0b11	
f_s (kHz)	Bit Setting	Ratio	Master Clock (MHz)	Ratio	Master Clock (MHz)	Ratio	Master Clock (MHz)	Ratio	Master Clock (MHz)
32 kHz,	0b00	$256 \times f_s$	8.192	$384 \times f_s$	12.288	$512 \times f_s$	16.384	$768 \times f_s$	24.576
44.1 kHz	0b00	$256 \times f_s$	11.2896	$384 \times f_s$	16.9344	$512 \times f_s$	22.5792	$768 \times f_s$	33.8688
48 kHz	0b00	$256 \times f_s$	12.288	$384 \times f_s$	18.432	$512 \times f_s$	24.576	$768 \times f_s$	36.864
64 kHz	0b01	$128 \times f_s$	8.192	$192 \times f_s$	12.288	$256 \times f_s$	16.384	$384 \times f_s$	24.576
88.2 kHz	0b01	$128 \times f_s$	11.2896	$192 \times f_s$	16.9344	$256 \times f_s$	22.5792	$384 \times f_s$	33.8688
96 kHz	0b01	$128 \times f_s$	12.288	$192 \times f_s$	18.432	$256 \times f_s$	24.576	$384 \times f_s$	36.864
128 kHz	0b10 or 0b11	$64 \times f_s$	8.192	$96 \times f_s$	12.288	$128 \times f_s$	16.384	$192 \times f_s$	24.576
176.4 kHz	0b10 or 0b11	$64 \times f_s$	11.2896	$96 \times f_s$	16.9344	$128 \times f_s$	22.5792	$192 \times f_s$	33.8688
192 kHz	0b10 or 0b11	$64 \times f_s$	12.288	$96 \times f_s$	18.432	$128 \times f_s$	24.576	$192 \times f_s$	36.864

POWER-UP AND RESET

The power sequencing for the ADAU1966A begins with AVDDx and IOVDD, followed by DVDD. It is very important that AVDDx be settled at a regulated voltage and that IOVDD be within 10% of regulated voltage before applying DVDD. When using the internal regulator of the ADAU1966A, this timing occurs by default.

To guarantee proper startup, pull the PU/RST pin low by an external resistor and then drive it high after the power supplies have stabilized. The PU/RST can also be pulled high using a simple RC network.

Driving the PU/RST pin low puts the part into a very low power state (<3 µA). All functionality of the ADAU1966A is disabled until the PU/RST pin is asserted high. Once this pin is asserted high, the ADAU1966A requires 300 ms to stabilize. The MMUTE bit in the DAC_CTRL0 register must be toggled for operation.

The PUP (master power-up control) bit in the PLL_CLK_CTRL0 register can be used to power down the ADAU1966A. Setting the PUP bit to 0 puts the ADAU1966A in an idle state while maintaining the settings of all registers. Additionally, the power-down bits in the PDN_THRMSSENS_CTRL_1 register (TS_PDN, PLL_PDN, and VREG_PDN) can be used to power down individual sections of the ADAU1966A.

The SOFT_RST bit in the PLL_CLK_CTRL0 register sets all of the control registers to their default settings while maintaining the internal clocks in default mode. The SOFT_RST bit does not power down the analog outputs; nor does toggling this bit cause audible popping sounds at the differential analog outputs.

For proper startup of the ADAU1966A, follow these steps:

1. Apply power to the ADAU1966A as described previously in this Power-Up and Reset section.
2. Assert the PU/RST pin high after power supplies are stable.
3. Set the PUP bit to 1.
4. Program all necessary registers for the desired settings.
5. Set the MMUTE bit to 0 to unmute all channels.

STANDALONE MODE

The ADAU1966A can operate without a typical I²C or SPI connection to a microcontroller. This standalone mode is available by setting SA_MODE (Pin 46) to IOVDD. All registers are set to default except for the options shown in Table 13.

Table 13. SA_MODE Settings

Pin No.	Setting	Function
42	0	Master mode serial audio interface (SAI)
	1	Slave mode SAI
43	0	MCLK = 256 × f _s , PLL on
	1	MCLK = 384 × f _s , PLL on
45	0	I ² S SAI format
	1	TDM modes, determined by Pin 31 and Pin 32

When both SA_MODE (Pin 46) and SS/ADDR0/SA (Pin 45) are set high, TDM mode is selected. Table 14 shows the available TDM modes; these modes are set by connecting Pin 31 (SA1) and Pin 32 (SA2) to GND or IOVDD.

Table 14. TDM Modes

Pin No.	Setting	Function
31 to 32	00	TDM4, DLRCLK pulse
	01	TDM8, DLRCLK pulse
	10	TDM16, DLRCLK pulse
	11	TDM8, DLRCLK 50% duty cycle

By powering up the ADAU1966A in SA_MODE, and asserting the PU/RST pin high, the MCLKO pin provides a buffered version of the MCLKI/XTALI pin, whether the source is a crystal or an active oscillator.

I²C CONTROL PORT

The ADAU1966A has an I²C-compatible control port that permits programming and readback of the internal control registers for the DACs and clock system. The I²C interface of the ADAU1966A is a 2-wire interface consisting of a clock line, SCL, and a data line, SDA. SDA is bidirectional, and the ADAU1966A drives SDA either to acknowledge the master (ACK) or to send data during a read operation. The SDA pin (MISO/SDA/SA) for the I²C port is an open-drain collector and requires a 2 kΩ pull-up resistor. A write or read access occurs when the SDA line is pulled low while the SCL line (SCLK/SCL) is high, indicated by a start in Figure 14 and Figure 15.

SDA is only allowed to change when SCL is low, except when a start or stop condition occurs, as shown in Figure 14 and Figure 15. The first eight bits of the data-word consist of the device address and the R/W bit. The device address consists of an internal built-in address (0x04) and two address bits, ADDR1 and ADDR0. The two address bits allow four ADAU1966A devices to be used in a system.

Table 15. I²C Addresses

ADDR1 (AD1)	ADDR0 (AD0)	Slave Address
0	0	0x04
0	1	0x24
1	0	0x44
1	1	0x64

I²C Write

Initiating a write operation to the ADAU1966A involves the following steps (see Figure 14):

1. Send a start condition
2. Send the device address with the $\overline{R/W}$ bit set low.
 - a. The ADAU1966A responds by issuing an acknowledge to indicate that it has been addressed.
3. Send a second frame directing the ADAU1966A to which register is required to be written.
 - a. A second acknowledge is issued by the ADAU1966A.
4. Send a third frame with the eight data bits required to be written to the register.
 - a. A third acknowledge is issued by the ADAU1966A.
5. Send a stop condition to complete the data transfer.

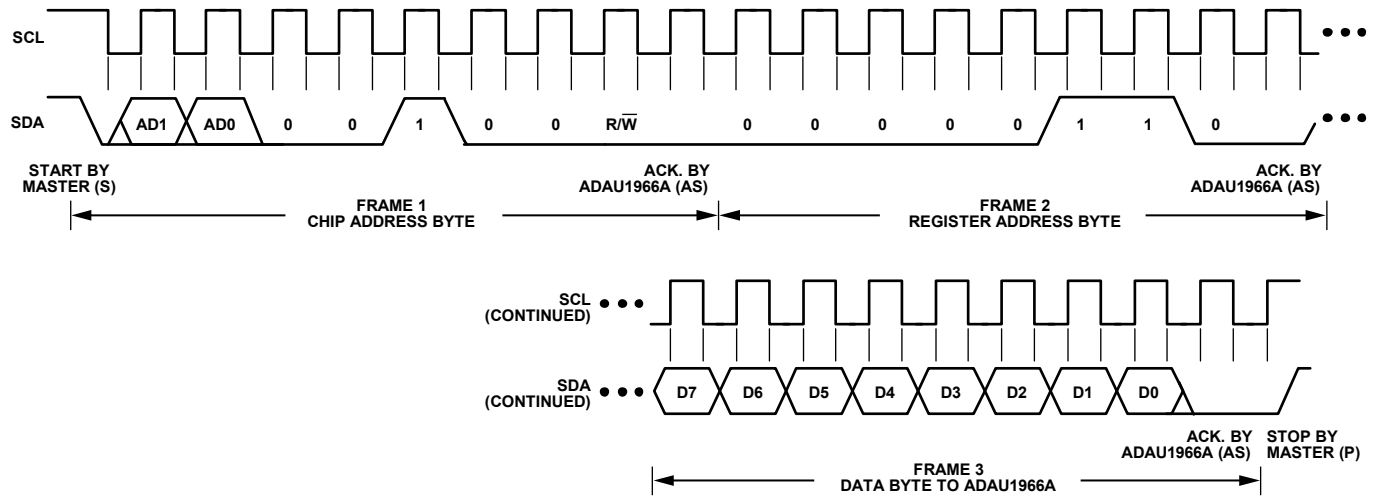


Figure 14. I²C Write Format

Table 16. I²C Abbreviations

Abbreviation	Condition
S	Start bit
P	Stop bit
AM	Acknowledge by master
AS	Acknowledge by slave

Table 17. Single Word I²C Write

S	Chip Address, $\overline{R/W} = 0$	AS	Register Address	AS	Data-Word	AS	P
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Table 18. Burst Mode I²C Write

S	Chip Address, $\overline{R/W} = 0$	AS	Register Address	AS	Data-Word 1	AS	Data-Word 2	AS	Data-Word N	AS	P
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I²C Read

A read operation requires that the user first write to the ADAU1966A to point to the correct register and then read the data. The following steps achieve this (see Figure 15):

1. Send a start condition followed by the device address frame with the R/W bit low and then the register address frame.
 - a. The ADAU1966A responds with an acknowledge.
2. Issue a repeated start condition.
 - a. The next frame is the device address with the R/W bit set high.
 - b. On the next frame, the ADAU1966A outputs the register data on the SDA line.
3. Issue a stop condition to complete the read operation.

Table 19. Single Word I²C Read

S	Chip Address, R/W = 0	AS	Register Address	AS	S	Chip Address, R/W = 1	AS	Data-Word	AM	P
---	-----------------------	----	------------------	----	---	-----------------------	----	-----------	----	---

Table 20. Burst Mode I²C Read

S	Chip Address, R/W = 0	AS	Register Address	AS	S	Chip Address, R/W = 1	AS	Data-Word 1	AM	Data-Word 2	AM	Data-Word N	AM	P
---	-----------------------	----	------------------	----	---	-----------------------	----	-------------	----	-------------	----	-------------	----	---

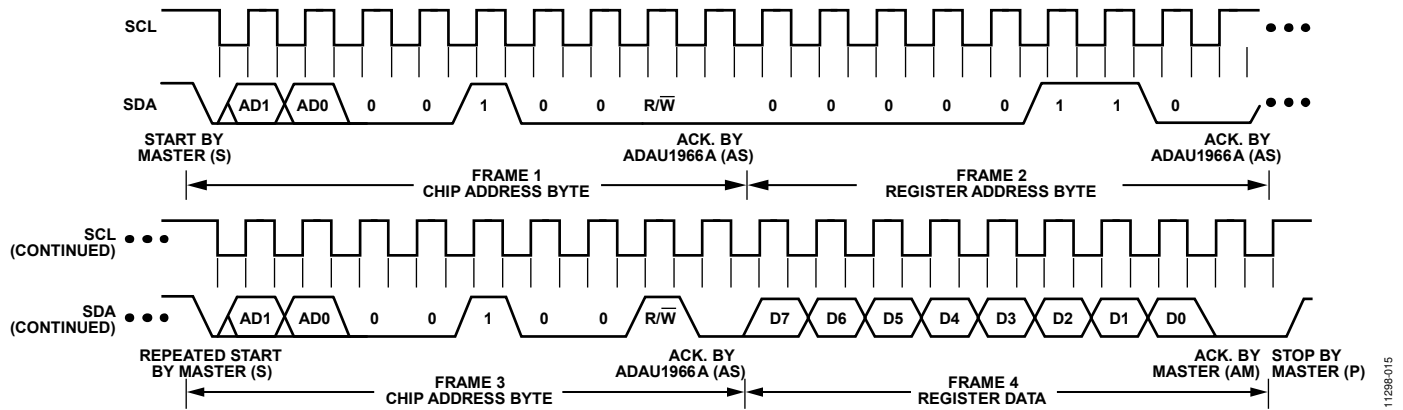


Figure 15. I²C Read Format

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SERIAL CONTROL PORT: SPI CONTROL MODE

The ADAU1966A has a 4-wire SPI control port that permits the programming and reading back of the internal control registers for the DACs and clock system. A standalone mode is also available for operation without serial control; it is configured at reset using the SA_MODE pin. See the Standalone Mode section for details about the SA_MODE pin.

By default, the ADAU1966A is in I²C mode; however, it can be put into SPI control mode by pulling \overline{SS} low three times. This is done by performing three dummy writes to the SPI port (the ADAU1966A does not acknowledge these three writes, see Figure 16). Beginning with the fourth SPI write, data can be written to or read from the IC. The ADAU1966A can only be taken out of SPI control mode by a full reset initiated by power cycling the device.

The format is a 24-bit wide data-word. The serial bit clock and latch can be completely asynchronous to the sample rate of the DACs. The first byte is a global address with a read/write bit. For the ADAU1966A, the address is 0x06, shifted left one bit due to the R/W bit. The second byte is the ADAU1966A register address, and the third byte is the data, as shown in Figure 17 and Figure 18. When reading data from the ADAU1966A, MISO is tristated until the third byte where it drives data out (see Figure 18). MISO is tristated at all other times, allowing it to be bused with other devices. The timing requirements are shown in Figure 19.

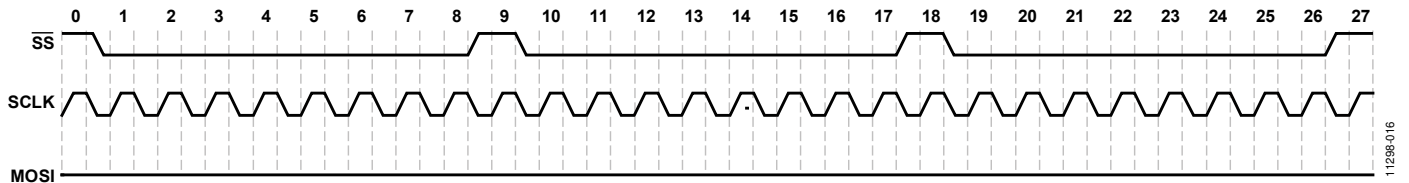


Figure 16. SPI Mode Initial Sequence

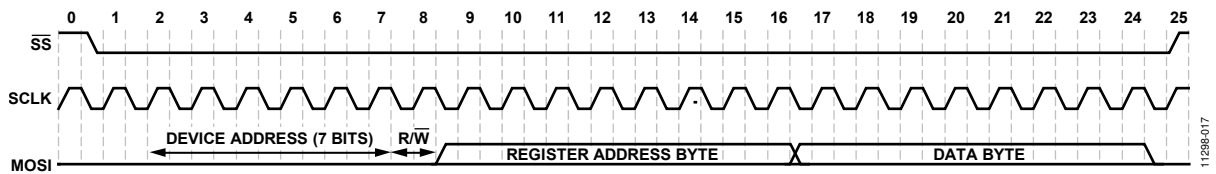


Figure 17. SPI Write to ADAU1966A Clocking

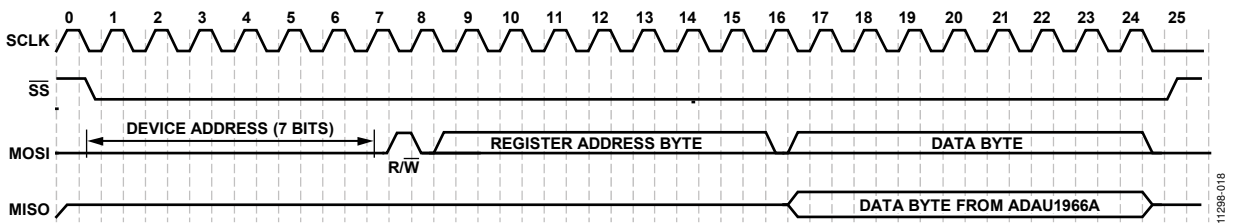


Figure 18. SPI Read from ADAU1966A Clocking

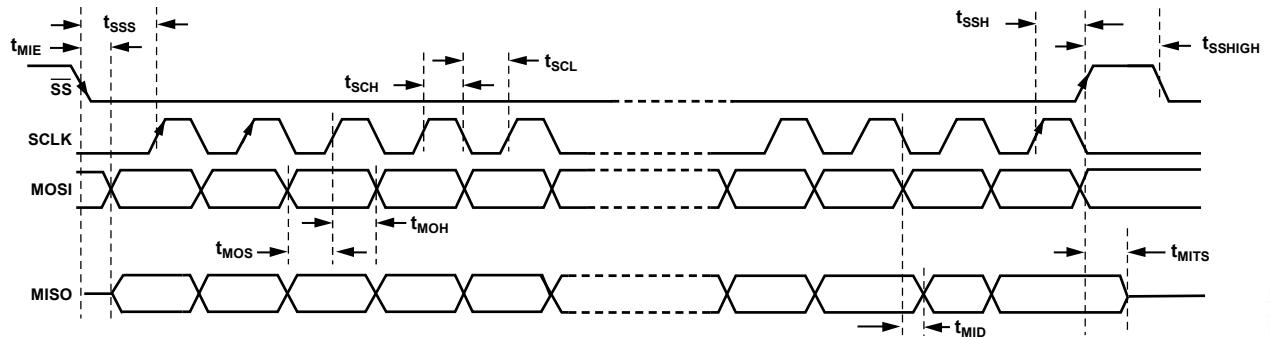


Figure 19. SPI Signal Timing

Chip Address R/\overline{W}

The LSB of the first byte of an SPI transaction is a R/\overline{W} bit. This bit determines whether the communication is a read (Logic Level 1) or a write (Logic Level 0). This format is shown in Table 21.

Table 21. ADAU1966A SPI Address and R/\overline{W} Byte Format

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	0	0	0	1	1	0	R/\overline{W}

SPI Burst Read/Write

The SPI port is capable of performing burst reads or writes by sending the chip address byte with the R/\overline{W} bit followed by the first register address that needs to be read from or written to. Then, as long as the \overline{SS} pin is held low, the user can sequentially read from or write to the registers by continuing to send clock pulses into the SCLK pin. An efficient way to initialize the ADAU1966A is by

- Sending out the address byte with the R/\overline{W} bit low (write)
- Sending out the address of the first register
- Sending out all the register byte values
- Toggling \overline{SS} to end the transfer
- Performing a burst read to verify that the register writes were successful

When referencing back to Analog Devices legacy devices, different pin names (mnemonics) were used for these SPI port functions. See Table 22 for details of the changes.

Table 22. SPI Port Pin Naming Conventions

Pin No.	Legacy Pin Mnemonic	New Pin Mnemonic
42	CDATA	MOSI
43	COU \overline{T}	MISO
44	CCLK	SCLK
45	\overline{CLATCH}	\overline{SS}

POWER SUPPLY AND VOLTAGE REFERENCE

The ADAU1966A is designed for 3.3 V analog and 2.5 V digital supplies. To minimize noise pickup, bypass the power supply pins with 100 nF ceramic chip capacitors placed as close to the pins as possible. Provide a bulk aluminum electrolytic capacitor of at least 22 μ F for each rail on the same PCB as the codec. It is important that the analog supply be as clean as possible.

The ADAU1966A includes a 2.5 V regulator driver that requires only an external pass transistor and bypass capacitors to make a 2.5 V regulator from a 3.3 V supply. Decouple the VSUPPLY and VSENSE pins with no more than 10 μ F of capacitance in parallel with 100 nF high frequency bypassing. If the regulator driver is not used, connect VSUPPLY and VDRIVE to GND and leave VSENSE unconnected.

The temperature sensor internal voltage reference (V_{TS_REF}) is connected to the TS_REF pin and must be bypassed as close as possible to the chip with a parallel combination of 10 μ F and 100 nF capacitors.

The internal band gap reference can be disabled in the PLL_CLK_CTRL1 register by setting VREF_EN to 0; the CM pin can be then be driven from an external source. This can be used to scale the DAC output to the clipping level of a power amplifier based on its power supply voltage.

The CM pin is the internal common-mode reference. Bypass it as close as possible to the chip with a parallel combination of 10 μ F and 100 nF capacitors. This voltage can be used to bias external op amps to the common-mode voltage of the analog input and output signal pins. It is recommended that the CM pin be isolated from the external circuitry by using a high quality buffer to provide a quiet, low impedance source for the external circuitry. Use of a quiet op amp is critical because any noise added to the reference voltage is injected into the signal path.

SERIAL DATA PORTS—DATA FORMAT

The 16 DAC channels use a common serial bit clock (DBCLK) and a common left-right framing clock (DLRCLK) in the serial data port. The clock signals are all synchronous with the sample rate. The normal stereo serial modes are shown in Figure 20.

The DAC serial data mode defaults to I²S (1 BCLK delay) upon power-up and reset. The ports can also be programmed for left justified and right justified (24-bit and 16-bit) operation using DAC_CTRL0[7:6]. Stereo and TDM modes can be selected using DAC_CTRL0[5:3]. The polarity of DBCLK and DLRCLK is programmable according to the DAC_CTRL1[1] and DAC_CTRL1[5] bits. The serial ports are programmable as the clock masters according to the DAC_CTRL1[0] bit. By default, the serial port is in slave mode.

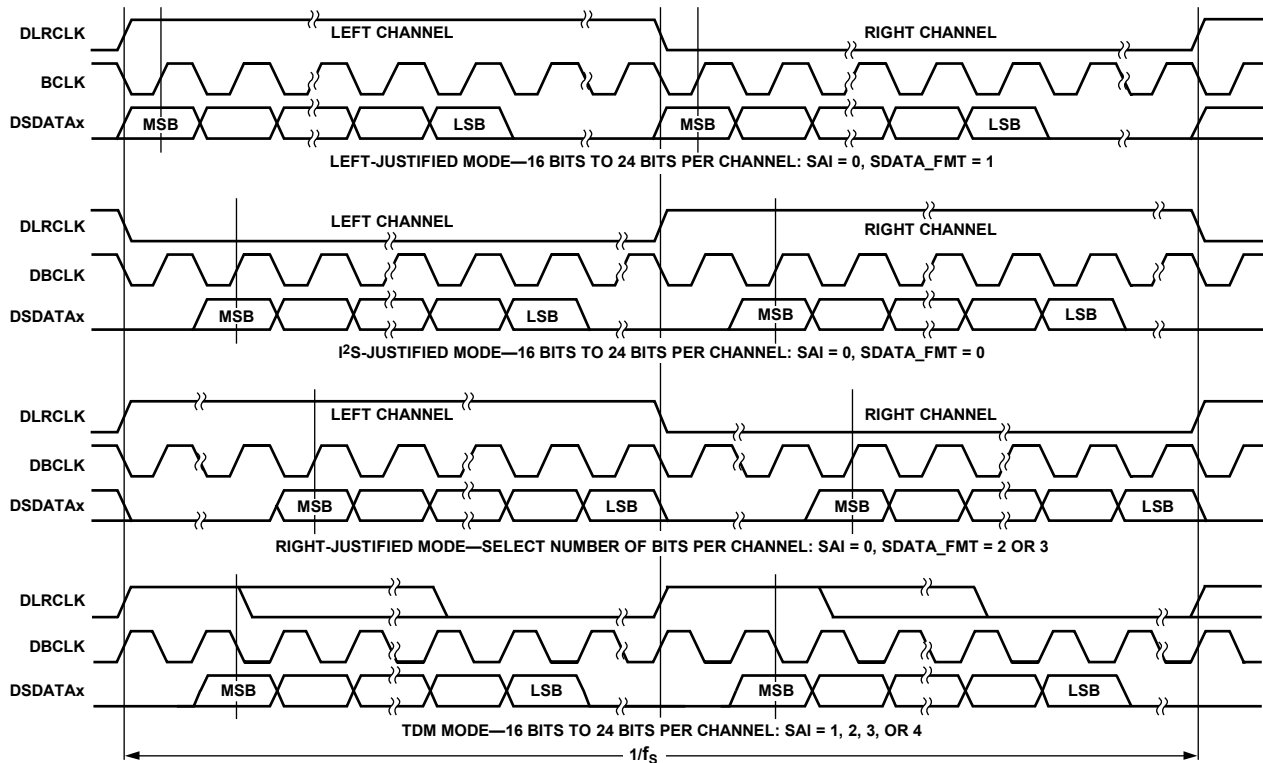


Figure 20. Stereo Serial Audio Modes

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TIME-DIVISION MULTIPLEXED (TDM) MODES

The ADAU1966A serial ports also have several different TDM serial data modes. The ADAU1966A can support a single data line (TDM16), a dual data line (TDM8), a quad data line (TDM4), or eight data lines (TDM2). The DLRCLK/frame clock can operate in both single-cycle pulse mode and a 50% duty cycle mode. Both 16 DBCLKs and 32 DBCLKs per channel are selectable for each mode.

The I/O pins of the serial ports are defined according to the serial mode that is selected. For a detailed description of the function of each pin in TDM and stereo modes, see Table 23.

TEMPERATURE SENSOR

The ADAU1966A has an on-board temperature sensor that allows the user to read the temperature of the silicon inside the device. The temperature sensor readout has a range of -60°C to $+140^{\circ}\text{C}$ in 1°C steps. The PDN_THRMSSENS_CTRL_1 register controls the settings of the sensor. The temperature sensor is powered on by default and can be shut off by setting the TS_PDN[2] bit to 1 in the

PDN_THRMSSENS_CTRL_1 register. The temperature sensor can be run in either continuous operation or one-shot mode. The temperature sensor conversion mode is modified using THRМ_MODE (Bit 5); the default is THRМ_MODE = 1, one-shot mode. In one-shot mode, writing a 0 followed by writing a 1 to THRМ_GO (Bit 4), results in a single reset and temperature conversion, placing the resulting temperature data in the THRМ_TEMP_STAT register.

In continuous operation mode, the data conversion takes place at a rate set by THRМ_RATE[7:6], with a range of 0.5 sec to 4 sec between samples. Faster rates are possible using one-shot mode.

Once a temperature conversion is placed in the THRМ_TEMP_STAT register, the data can be translated into degrees Celsius ($^{\circ}\text{C}$) using the following steps:

1. Convert the binary or hexadecimal data read from THRМ_TEMP_STAT into decimal form.
2. Subtract 60 from the converted THRМ_TEMP_STAT data; this is the temperature of the silicon in $^{\circ}\text{C}$.

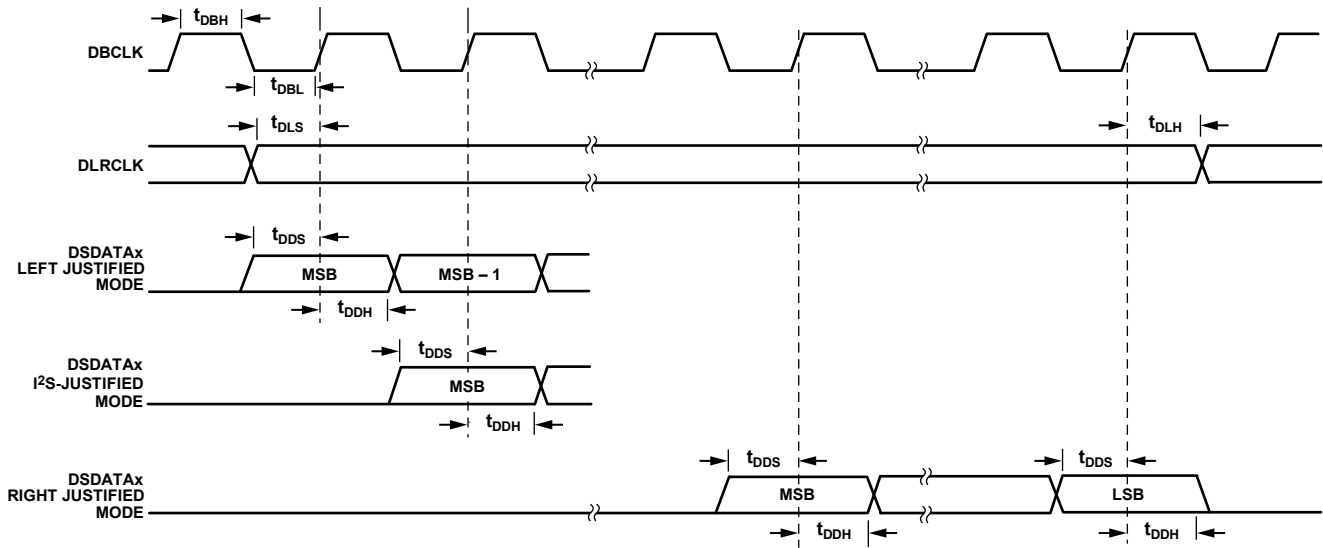


Figure 21. DAC Serial Timing

Table 23. Pin Function Changes in Different Serial Audio Interface Modes

Signal	Stereo Modes (SAI = 0 or SAI = 1)	TDM4 Mode (SAI = 2)	TDM8 Mode (SAI = 3)	TDM16 Mode (SAI = 4)
DSDATA1	Channel 1/Channel 2 data input	Channel 1 to Channel 4 data input	Channel 1 to Channel 8 data input	Channel 1 to Channel 16 data input
DSDATA2	Channel 3/Channel 4 data input	Channel 5 to Channel 8 data input	Channel 9 to Channel 16 data input	Not used
DSDATA3	Channel 5/Channel 6 data input	Channel 9 to Channel 12 data input	Not used	Not used
DSDATA4	Channel 7/Channel 8 data input	Channel 13 to Channel 16 data input	Not used	Not used
DSDATA5	Channel 9/Channel 10 data input	Not used	Not used	Not used
DSDATA6	Channel 11/Channel 12 data input	Not used	Not used	Not used
DSDATA7	Channel 13/Channel 14 data input	Not used	Not used	Not used
DSDATA8	Channel 15/Channel 16 data input	Not used	Not used	Not used
DLRCLK	DLRCLK input/DLRCLK output	TDM frame sync input/ TDM frame sync output	TDM frame sync input/ TDM frame sync output	TDM frame sync input/ TDM frame sync output
DBCLK	DBCLK input/DBCLK output	TDM DBCLK input/ TDM DBCLK output	TDM DBCLK input/ TDM DBCLK output	TDM DBCLK input/ TDM DBCLK output
Maximum Sample Rate	192 kHz	192 kHz	96 kHz	48 kHz

ADDITIONAL MODES

The ADAU1966A offers several additional modes for board level design enhancements. To reduce the EMI in board level design, serial data can be transmitted without an explicit bit clock input on the DBCLK pin. See Figure 22 for an example of a DAC TDM data transmission mode that does not require a high speed bit clock or an external master clock. This configuration is applicable when the ADAU1966A master clock is generated by the PLL with the DLRCLK pin as the PLL reference frequency.

To relax the requirement for the setup time of the ADAU1966A in cases of high speed TDM data transmission, the ADAU1966A can latch in the data using the falling edge of DBCLK pin; see the BCLK_EDGE bit in the DAC_CTRL1 register. This effectively dedicates the entire bit clock period to the setup time. This mode is useful when the source has a large delay time in the serial data driver. Figure 23 shows this inverted bit clock mode of data transmission.

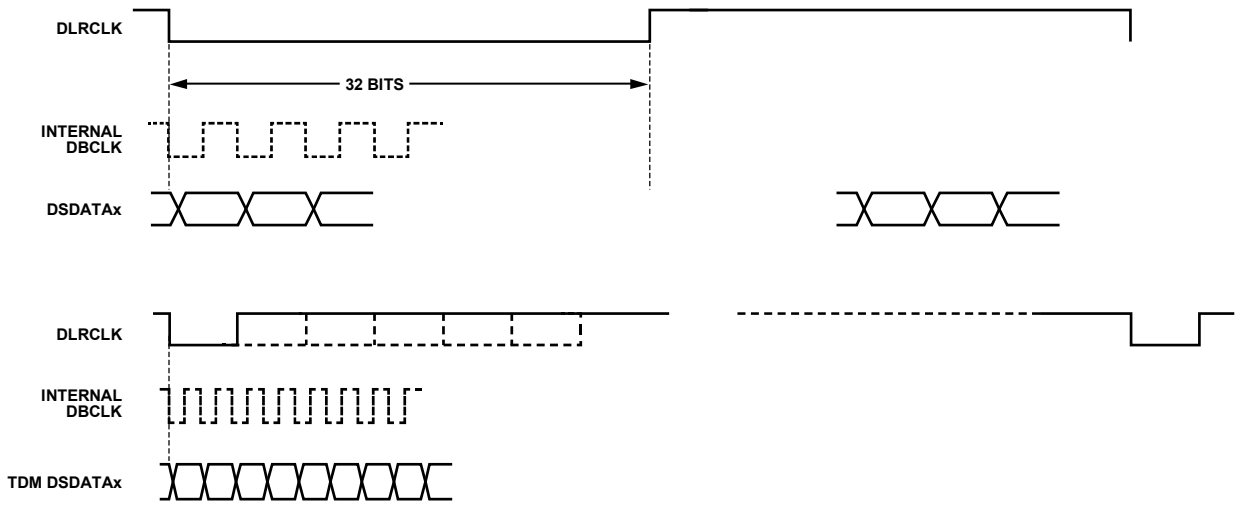


Figure 22. Serial DAC Data Transmission in TDM Format Without DBCLK (Applicable Only If PLL Locks to DLRCLK)

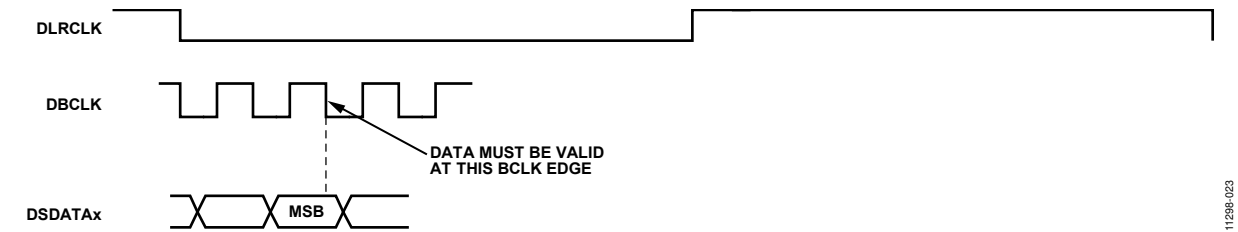


Figure 23. Inverted DBCLK Mode in DAC Serial Data Transmission (Applicable in Stereo and TDM, Useful for High Frequency TDM Transmission)

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REGISTER SUMMARY

Table 24. ADAU1966A Register Summary

Reg. No.	Register Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW	
0x00	PLL_CLK_CTRL0	[7:0]	PLLIN		XTAL_SET		SOFT_RST	MCS		PUP	0x00	RW	
0x01	PLL_CLK_CTRL1	[7:0]	LOPWR_MODE		MCLKO_SEL		PLL_MUTE	PLL_LOCK	VREF_EN	CLK_SEL	0x2A	RW	
0x02	PDN_THRMSSENS_CTRL_1	[7:0]	THRM_RATE		THRM_MODE	THRM_GO	RESERVED	TS_PDN	PLL_PDN	VREG_PDN	0xA0	RW	
0x03	PDN_CTRL2	[7:0]	DAC08_PDN	DAC07_PDN	DAC06_PDN	DAC05_PDN	DAC04_PDN	DAC03_PDN	DAC02_PDN	DAC01_PDN	0x00	RW	
0x04	PDN_CTRL3	[7:0]	DAC16_PDN	DAC15_PDN	DAC14_PDN	DAC13_PDN	DAC12_PDN	DAC11_PDN	DAC10_PDN	DAC09_PDN	0x00	RW	
0x05	THRM_TEMP_STAT	[7:0]	TEMP									0x00	R
0x06	DAC_CTRL0	[7:0]	SDATA_FMT		SAI			FS		MMUTE	0x01	RW	
0x07	DAC_CTRL1	[7:0]	BCLK_GEN	LRCLK_MODE	LRCLK_POL	SAI_MSB	RESERVED	BCLK_RATE	BCLK_EDGE	SAI_MS	0x00	RW	
0x08	DAC_CTRL2	[7:0]	RESERVED			BCLK_TDMC	DAC_POL	AUTO_MUTE_EN	DAC_OSR	DE_EMP_EN	0x06	RW	
0x09	DAC_MUTE1	[7:0]	DAC08_MUTE	DAC07_MUTE	DAC06_MUTE	DAC05_MUTE	DAC04_MUTE	DAC03_MUTE	DAC02_MUTE	DAC01_MUTE	0x00	RW	
0x0A	DAC_MUTE2	[7:0]	DAC16_MUTE	DAC15_MUTE	DAC14_MUTE	DAC13_MUTE	DAC12_MUTE	DAC11_MUTE	DAC10_MUTE	DAC09_MUTE	0x00	RW	
0x0B	DACMSTR_VOL	[7:0]	DACMSTR_VOL									0x00	RW
0x0C	DAC01_VOL	[7:0]	DAC01_VOL									0x00	RW
0x0D	DAC02_VOL	[7:0]	DAC02_VOL									0x00	RW
0x0E	DAC03_VOL	[7:0]	DAC03_VOL									0x00	RW
0x0F	DAC04_VOL	[7:0]	DAC04_VOL									0x00	RW
0x10	DAC05_VOL	[7:0]	DAC05_VOL									0x00	RW
0x11	DAC06_VOL	[7:0]	DAC06_VOL									0x00	RW
0x12	DAC07_VOL	[7:0]	DAC07_VOL									0x00	RW
0x13	DAC08_VOL	[7:0]	DAC08_VOL									0x00	RW
0x14	DAC09_VOL	[7:0]	DAC09_VOL									0x00	RW
0x15	DAC10_VOL	[7:0]	DAC10_VOL									0x00	RW
0x16	DAC11_VOL	[7:0]	DAC11_VOL									0x00	RW
0x17	DAC12_VOL	[7:0]	DAC12_VOL									0x00	RW
0x18	DAC13_VOL	[7:0]	DAC13_VOL									0x00	RW
0x19	DAC14_VOL	[7:0]	DAC14_VOL									0x00	RW
0x1A	DAC15_VOL	[7:0]	DAC15_VOL									0x00	RW
0x1B	DAC16_VOL	[7:0]	DAC16_VOL									0x00	RW
0x1C	PAD_STRGTH	[7:0]	RESERVED		PAD_DRV	RESERVED					0x00	RW	
0x1D	DAC_POWER1	[7:0]	DAC04_POWER		DAC03_POWER		DAC02_POWER		DAC01_POWER		0xAA	RW	
0x1E	DAC_POWER2	[7:0]	DAC08_POWER		DAC07_POWER		DAC06_POWER		DAC05_POWER		0xAA	RW	
0x1F	DAC_POWER3	[7:0]	DAC12_POWER		DAC11_POWER		DAC10_POWER		DAC09_POWER		0xAA	RW	
0x20	DAC_POWER4	[7:0]	DAC16_POWER		DAC15_POWER		DAC14_POWER		DAC13_POWER		0xAA	RW	