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Quad ADC with Diagnostics

Data Sheet

ADAU1977

FEATURES

Programmable microphone bias (5 V to 9 V) with diagnostics
Four 10 V rms capable direct-coupled differential inputs
On-chip PLL for master clock
Low EMI design
109 dB ADC dynamic range
–95 dB THD + N
Selectable digital high-pass filter
24-bit ADC with 8 kHz to 192 kHz sample rates
Digital volume control with autoramp function
I²C/SPI control
Software-controllable clickless mute
Software power-down
Right justified, left justified, I²S justified, and TDM modes
Master and slave operation modes
40-lead LFCSP package
Qualified for automotive applications

APPLICATIONS

Automotive audio systems
Active noise cancellation system

GENERAL DESCRIPTION

The ADAU1977 incorporates four high performance analog-to-digital converters (ADCs) with direct-coupled inputs capable of 10 V rms. The ADC uses multibit sigma-delta (Σ-Δ) architecture with continuous time front end for low EMI. The ADCs can be connected to the electret microphone (ECM) directly and provide the bias for powering the microphone. Built-in diagnostic circuitry detects faults on input lines and includes comprehensive diagnostics for faults on microphone inputs. The faults reported are short to battery, short to microphone bias, short to ground, short between positive and negative input pins, and open input terminals. In addition, each diagnostic fault is available as an IRQ flag for ease in system design. An I²C/SPI control port is also included. The ADAU1977 uses only a single 3.3 V supply. The part internally generates the microphone bias voltage. The microphone bias is programmable in a few steps from 5 V to 9 V. The low power architecture reduces the power consumption. An on-chip PLL can derive the master clock from an external clock input or frame clock (sample rate clock). When fed with a frame clock, the PLL eliminates the need for a separate high frequency master clock in the system. The ADAU1977 is available in a 40-lead LFCSP package.

FUNCTIONAL BLOCK DIAGRAM

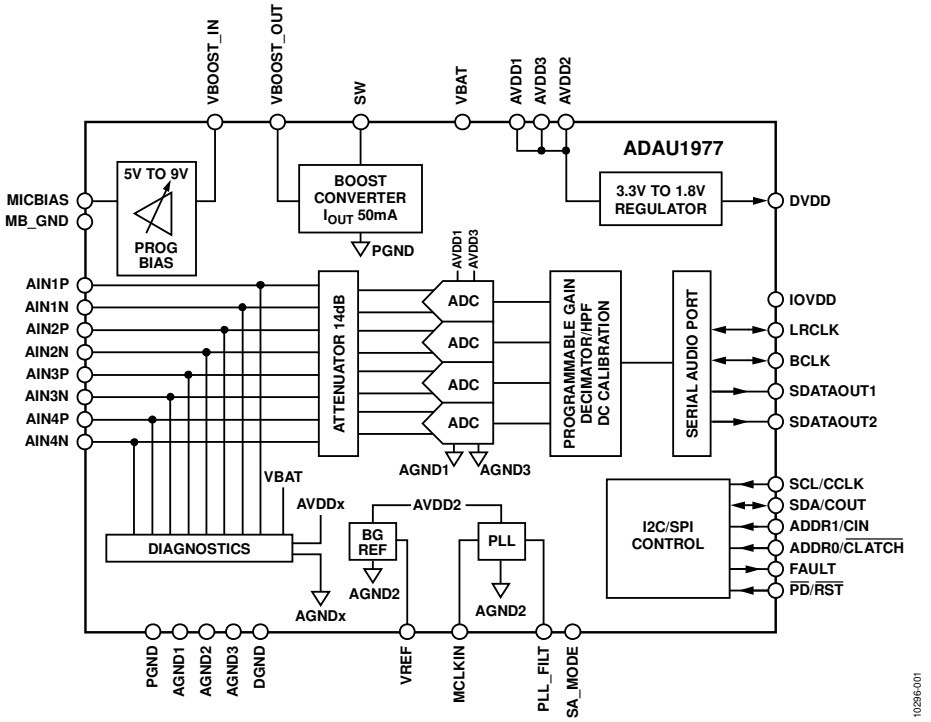

Figure 1.

Rev. C Document Feedback

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Tel: 781.329.4700
Technical Support www.analog.com

ADAU1977* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADAU1977/ADAU1978/ADAU1979 Evaluation Board
- ADSP-SC584 Evaluation Hardware for the ADSP-SC58x/ ADSP-2158x SHARC Family (349-ball CSPBGA)
- ADUSB2EBZ Evaluation Board

DOCUMENTATION

Data Sheet

- ADAU1977: Quad ADC with Diagnostics Data Sheet

User Guides

- UG-600: Evaluating the ADAU1977/ADAU1978/ ADAU1979

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADAU1977 Sound CODEC Linux Driver

TOOLS AND SIMULATIONS

- ADAU1977 IBIS Model

DESIGN RESOURCES

- ADAU1977 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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1/13—Revision 0: Initial Version

SPECIFICATIONS

Performance of all channels is identical, exclusive of the interchannel gain mismatch and interchannel phase deviation specifications. AVDDx/IOVDD = 3.3 V; DVDD (internally generated) = 1.8 V; VBAT = 14.4 V; T_A = −40°C to +105°C, unless otherwise noted; master clock = 12.288 MHz (48 kHz f_S, 256 × f_S mode); input sample rate = 48 kHz; measurement bandwidth = 20 Hz to 20 kHz; word width = 24 bits; load capacitance (digital output) = 20 pF; load current (digital output) = ±1 mA; digital input voltage high = 2.0 V; digital input voltage low = 0.8 V.

ANALOG PERFORMANCE SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LINE INPUT APPLICATION	See Figure 46				
Full-Scale Differential Input Voltage	DC-coupled, V_{CM} at AINxP/AINxN = 7 V		10		V rms
Full-Scale Single-Ended Input Voltage	DC-coupled, V_{CM} at AINxP/AINxN = 7 V		5		V rms
MICROPHONE INPUT APPLICATION	See Figure 46, MICBIAS = 8.5 V				
Differential Input Voltage	DC-coupled, V_{CM} at AINxP = 5.66 V, AINxN = 2.83 V		2		V rms
QUASI DC INPUT					
Single-Ended Input Voltage			5		V peak
Input Common-Mode Voltage	V_{CM} at AINxP/AINxN pins	0		8	V dc
Peak Input Voltage	V_{CM} + V ac peak at AINxP/AINxN pins	0		14	V
MICROPHONE BIAS					
Output Voltage	Programmable from 5 V to 9 V in steps of 0.5 V; the output voltage is within the specified load regulation	5		9	V
Load Regulation	From no load to maximum load of 25 mA at 5 V	−1	+0.2	+1	%
	From no load to maximum load of 45 mA at 9 V	−1	+0.3	+1	%
Output Current	At MICBIAS = 5 V			25	mA
	At MICBIAS = 9 V			45	mA
Output Noise	20 Hz to 20 kHz, MICBIAS = 5 V		22	32	µV rms
	20 Hz to 20 kHz, MICBIAS = 9 V		35	54	µV rms
Power Supply Rejection Ratio (PSRR)	350 mV rms, 1 kHz ripple on VBOOST_IN at 10 V		60		dB
Interchannel Isolation at MICBIAS Pin	Referred to full scale at 1 kHz		60		dB
Start-Up Time	With C_{LOAD} = 1 nF		40		ms
BOOST CONVERTER					
Input Voltage		2.97	3.3	3.63	V
Input Current	L = 4.7 µH, f_{SW} = 1.536 MHz, MICBIAS = 9 V at 45 mA load		195		mA
	L = 2.2 µH, f_{SW} = 3.072 MHz, MICBIAS = 9 V at 45 mA load		220		mA
Output Current	MICBIAS = 5 V		50		mA
	MICBIAS = 9 V		88		mA
Load Regulation	From no load to maximum load of 50 mA at MICBIAS = 5 V	−1		+1	%
	From no load to maximum load of 88 mA at MICBIAS = 9 V	−1		+1	%
Input Overcurrent Threshold			900		mA peak
Switching Frequency	f_S = 48 kHz L = 2.2 µH		3.072		MHz
	f_S = 48 kHz, L = 4.7 µH		1.536		MHz
External Load Capacitor at VBOOST_OUT Pin		4.7	10	22	µF
ANALOG-TO-DIGITAL CONVERTERS					
Input Resistance					
Differential	Between AINxP and AINxN		50		kΩ
Single-Ended (Rin_{1977})	Between AINxP and AINxN		25		kΩ
ADC Resolution			24		Bits
Dynamic Range (A-Weighted)[1]	Input = 1 kHz, −60 dBFS				
Line Input	Referred to full-scale differential input = 10 V rms	103	109		dB
Microphone Input	Referred to full-scale differential input = 2 V rms		95		dB
Total Harmonic Distortion Plus Noise (THD + N)	Input = 1 kHz, −1 dBFS (0 dBFS = 10 V rms input)		−95	−89	dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Digital Gain Post ADC	Gain step size = 0.375 dB	−35.625		+60	dB
Gain Error		−10		+10	%
Interchannel Gain Mismatch		−0.25		+0.25	dB
Gain Drift			0.6		ppm/°C
Common-Mode Rejection Ratio (CMRR)	1 V rms, 1 kHz		60		dB
	1 V rms, 20 kHz		56		dB
Power Supply Rejection Ratio (PSRR)	100 mV rms, 1 kHz on AVDDx = 3.3 V		70		dB
Interchannel Isolation			100		dB
Interchannel Phase Deviation			0		Degrees
REFERENCE					
Internal Reference Voltage	VREF pin	1.47	1.50	1.54	V
Output Impedance			20		kΩ
ADC SERIAL PORT					
Output Sample Rate		8		192	kHz

[1] For f_S ranging from 44.1 kHz to 192 kHz.

DIAGNOSTIC AND FAULT SPECIFICATIONS

Applicable to differential microphone input using MICBIAS on AINxP and AINxN pins.

Table 2.

Parameter	Test Conditions/ Comments	Min	Typ	Max	Unit
INPUT VOLTAGE THRESHOLDS FOR FAULT DETECTION[1]					
Hysteresis AINxP or AINxN Shorted to VBAT	SHT_B_TRIP = 10	0.79 × VBAT	0.85 × VBAT	0.86 × VBAT	V
	SHT_B_TRIP = 01	0.84 × VBAT	0.9 × VBAT	0.91 × VBAT	V
	SHT_B_TRIP = 00	0.89 × VBAT	0.95 × VBAT	0.96 × VBAT	V
	SHT_B_TRIP = 11	0.93 × VBAT	0.975 × VBAT	0.99 × VBAT	V
Hysteresis AINxP and AINxN Shorted Together	SHT_T_TRIP = 00	MICBIAS(0.5 ± 0.015)	MICBIAS(0.5 ± 0.035)	MICBIAS(0.5 ± 0.047)	V
	SHT_T_TRIP = 01	MICBIAS(0.5 ± 0.001)	MICBIAS(0.5 ± 0.017)	MICBIAS(0.5 ± 0.03)	V
	SHT_T_TRIP = 10	MICBIAS(0.5 ± 0.05)	MICBIAS(0.5 ± 0.071)	MICBIAS(0.5 ± 0.08)	V
Hysteresis AINxP or AINxN Shorted to Ground	SHT_G_TRIP = 10	0.04 × VREF	0.1 × VREF	0.13 × VREF	V
	SHT_G_TRIP = 01	0.08 × VREF	0.133 × VREF	0.16 × VREF	V
	SHT_G_TRIP = 00	0.12 × VREF	0.2 × VREF	0.22 × VREF	V
	SHT_G_TRIP = 11	0.19 × VREF	0.266 × VREF	0.28 × VREF	V
Hysteresis AINxP Shorted to MICBIAS	SHT_M_TRIP = 10	0.82 × MICBIAS	0.85 × MICBIAS	0.89 × MICBIAS	V
	SHT_M_TRIP = 01	0.87 × MICBIAS	0.9 × MICBIAS	0.94 × MICBIAS	V
	SHT_M_TRIP = 00	0.92 × MICBIAS	0.95 × MICBIAS	1.0 × MICBIAS	V
	SHT_M_TRIP = 11	0.95 × MICBIAS	0.975 × MICBIAS	1.0 × MICBIAS	V
Hysteresis AINxP or AINxN Open Circuit[2]	Refer to the AINxP shorted to MICBIAS and the AINxN shorted to ground specifications for upper and lower thresholds.				
FAULT DURATION	Programmable	10	100	150	ms

[1] The threshold limits are tested with VREF = 1.5 V, MICBIAS = 5 V to 8.5 V, and VBAT = 11 V to 18 V set using an external source. When VBAT ≤ MICBIAS, a short to VBAT cannot be distinguished from a short to MICBIAS, and reporting a short to VBAT fault takes precedence over a short to MICBIAS fault.

[2] The AINxP open terminal fault cannot be distinguished from the AINxN open terminal fault because the voltage at the AINxP and AINxN pins remain at MICBIAS and ground, respectively, when either of these two terminals becomes open circuit.

DIGITAL INPUT/OUTPUT SPECIFICATIONS

Table 3.

Parameter	Test Conditions/Comments	Min	Max	Unit
INPUT				
High Level Input Voltage (V_{IH})		0.7 × IOVDD		V
Low Level Input Voltage (V_{IL})			0.3 × IOVDD	V
Input Leakage Current			±10	µA
Input Capacitance			5	pF
OUTPUT				
High Level Output Voltage (V_{OH})	I_{OH} = 1 mA	IOVDD – 0.60		V
Low Level Output Voltage (V_{OL})	I_{OL} = 1 mA		0.4	V

POWER SUPPLY SPECIFICATIONS

L = 4.7 µH, AVDDx = 3.3 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_S = 48 kHz (master mode), unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DVDD	On-chip LDO	1.62	1.8	1.98	V
AVDDx		3.0	3.3	3.6	V
IOVDD		1.62	3.3	3.6	V
VBAT[1]			14.4	18	V
IOVDD Current	Master clock = 256 f_S				
Normal Operation	f_S = 48 kHz		450		µA
	f_S = 96 kHz		880		µA
	f_S = 192 kHz		1.75		mA
Power-Down	f_S = 48 kHz to 192 kHz		20		µA
AVDDx Current					
Normal Operation	Boost off, 4-channel ADC, DVDD internal		14		mA
	Boost on, 4-channel ADC, DVDD internal		14.5		mA
	Boost off, 4-channel ADC, DVDD external		9.6		mA
	Boost on, 4-channel ADC, DVDD external		10.1		mA
Power-Down			270		µA
Boost Converter Current					
Normal Operation	Boost on, 4-channel ADC, MICBIAS = 8.5 V, no load		34		mA
	Boost on, 4-channel ADC, MICBIAS = 8.5 V, 42 mA		168		mA
Power-Down			180		µA
DVDD Current					
Normal Operation	DVDD external = 1.8 V		4.5		mA
Power-Down			65		µA
VBAT Current	VBAT = 14.4 V				
Normal Operation			575	625	µA
Power-Down			575	625	µA
POWER DISSIPATION					
Normal Operation	Master clock = 256 f_S, 48 kHz				
AVDDx	DVDD internal, MICBIAS = 8.5 V at 42 mA load		265		mW
Power-Down, All Supplies	$\overline{PD}/\overline{RST}$ pin held low		9		mW

[1] When VBAT ≤ MICBIAS, a short to VBAT cannot be distinguished from a short to MICBIAS, and reporting a short to VBAT fault takes precedence over a short to MICBIAS fault.

DIGITAL FILTERS SPECIFICATIONS

Table 5.

Parameter	Mode	Factor	Min	Typ	Max	Unit
ADC DECIMATION FILTER	All modes, typical at f_S = 48 kHz					
Pass Band		0.4375 × f_S		21		kHz
Pass-Band Ripple				±0.015		dB
Transition Band		0.5 × f_S		24		kHz
Stop Band		0.5625 × f_S		27		kHz
Stop-Band Attenuation			79			dB
Group Delay	f_S = 8 kHz to 96 kHz	22.9844/f_S		479		µs
	f_S = 192 kHz			35		µs
HIGH-PASS FILTER	All modes, typical at 48 kHz					
Cutoff Frequency	At −3 dB point			0.9375		Hz
Phase Deviation	At 20 Hz			10		Degrees
Settling Time						
ADC DIGITAL GAIN	All modes		0		60	dB
Gain Step Size				0.375		dB

TIMING SPECIFICATIONS

Table 6.

Parameter	Limit at Min	Max	Unit	Description
INPUT MASTER CLOCK (MCLK)				
Duty Cycle	40	60	%	MCLKIN duty cycle; MCLKIN at 256 × f_S, 384 × f_S, 512 × f_S, and 768 × f_S
f_{MCLK}	See Table 10		MHz	MCLKIN frequency, PLL in MCLK mode
RESET				
Reset Pulse	15		ns	$\overline{RST}$ low
PLL				
Lock Time		10	ms	
I^2C PORT				
f_{SCL}		400	kHz	SCL frequency
t_{SCLH}	0.6		µs	SCL high
t_{SCLL}	1.3		µs	SCL low
t_{SCS}	0.6		µs	Setup time; relevant for repeated start condition
t_{SCH}	0.6		µs	Hold time; after this period of time, the first clock pulse is generated
t_{DS}	100		ns	Data setup time
t_{DH}	0			Data hold time
t_{SCR}		300	ns	SCL rise time
t_{SCF}		300	ns	SCL fall time
t_{SDR}		300	ns	SDA rise time
t_{SDF}		300	ns	SDA fall time
t_{BFT}	1.3		µs	Bus-free time; time between stop and start
t_{SUSTO}	0.6		µs	Setup time for stop condition
SPI PORT				
t_{CCPH}	35		ns	CCLK high
t_{CCPL}	35		ns	CCLK low
f_{CCLK}		10	MHz	CCLK frequency
t_{CDS}	10		ns	CIN setup to CCLK rising
t_{CDH}	10		ns	CIN hold from CCLK rising
t_{CLS}	10		ns	$\overline{CLATCH}$ setup to CCLK rising
t_{CLH}	40		ns	$\overline{CLATCH}$ hold from CCLK rising
t_{CLPH}	10		ns	$\overline{CLATCH}$ high
t_{COE}		30	ns	COUT enable from $\overline{CLATCH}$ falling
t_{COD}		30	ns	COUT delay from CCLK falling
t_{COTS}		30	ns	COUT tristate from $\overline{CLATCH}$ rising
ADC SERIAL PORT				
t_{ABH}	10		ns	BCLK high, slave mode
t_{ABL}	10		ns	BCLK low, slave mode
t_{ALS}	10		ns	LRCLK setup to BCLK rising, slave mode
t_{ALH}	5		ns	LRCLK hold from BCLK rising, slave mode
t_{ABDD}		18	ns	SDATAOUTx delay from BCLK falling

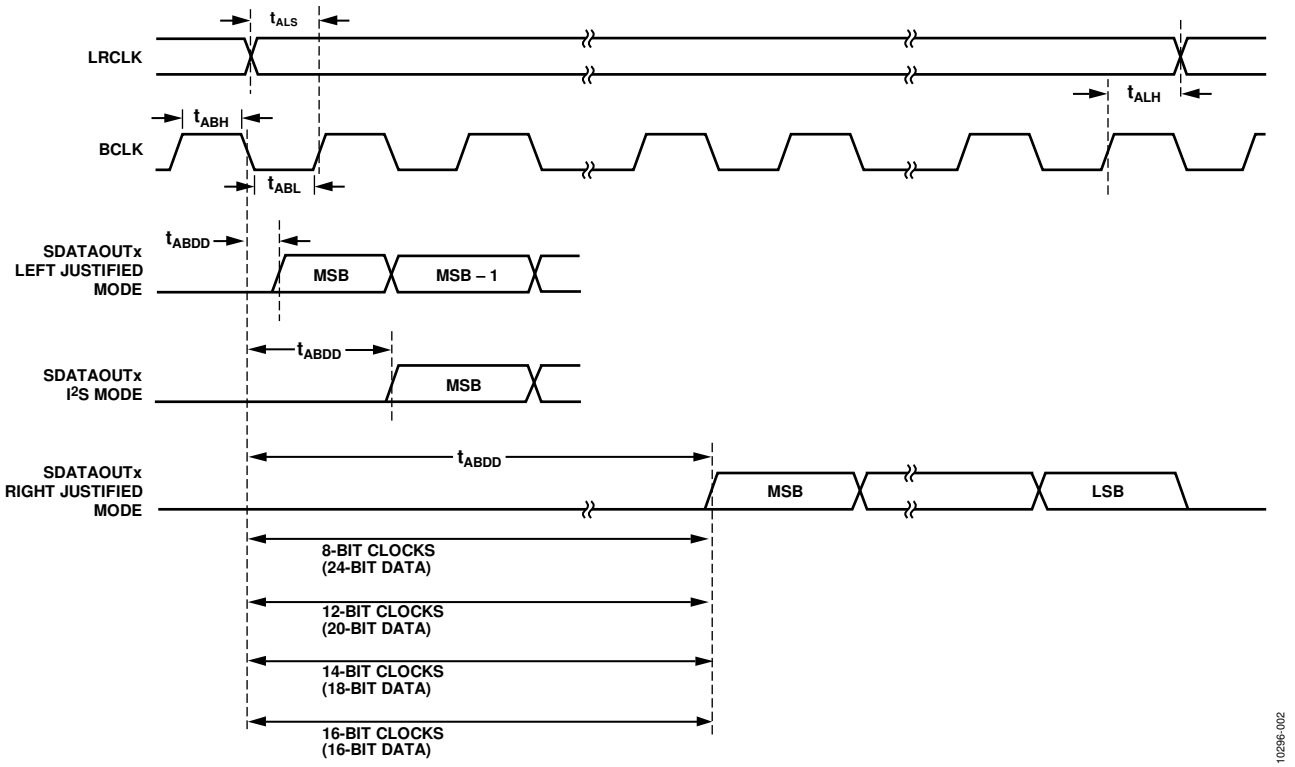


Figure 2. Serial Output Port Timing

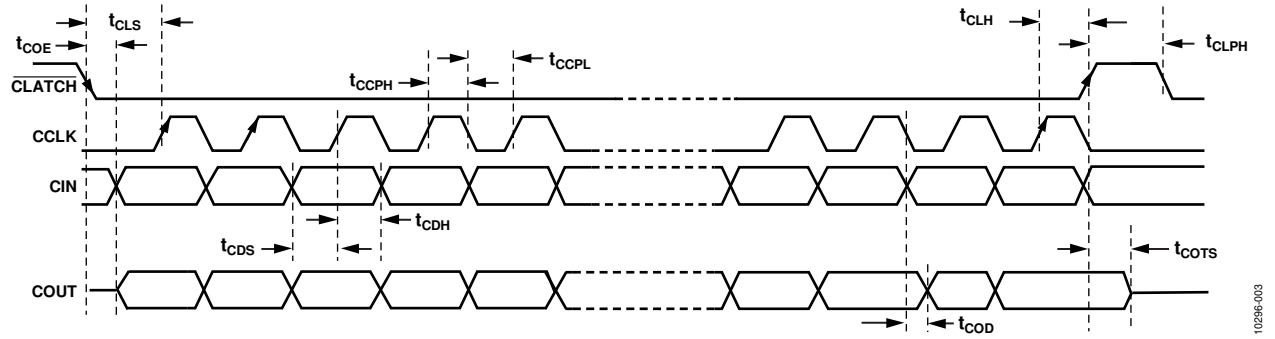


Figure 3. SPI Port Timing

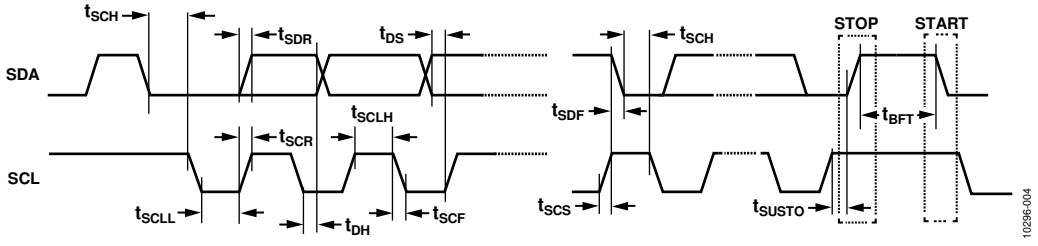


Figure 4. I²C Port Timing

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Analog Supply (AVDDx)	−0.3 V to +3.63 V
Digital Supply	
DVDD	−0.3 V to +1.98 V
IOVDD	−0.3 V to +3.63 V
Input Current (Except Supply Pins)	±20 mA
Analog Input Voltage (AINx, VBAT Pins)	−0.3 V to +18 V
Digital Input Voltage (Signal Pins)	−0.3 V to +3.63 V
Operating Temperature Range (Ambient)	−40°C to +105°C
Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} represents thermal resistance, junction-to-ambient, and θ_{JC} represents the thermal resistance, junction-to-case. All characteristics are for a standard JEDEC board per JESD51.

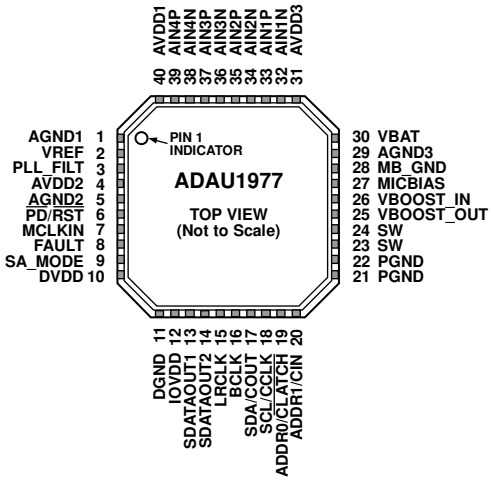
Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead LFCSP	32.8	1.93	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD MUST BE CONNECTED TO THE GROUND PLANE ON THE PCB.

Figure 5. Pin Configuration, 40-Lead LFCSP

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	In/Out[1]	Description
1	AGND1	P	Analog Ground.
2	VREF	O	Voltage Reference. Decouple this pin to AGNDx with 10 µF||100 nF capacitors.
3	PLL_FILT	O	PLL Loop Filter. Return this pin to AVDDx using recommended loop filter components.
4	AVDD2	P	Analog Power Supply. Connect this pin to analog 3.3 V supply.
5	AGND2	P	Analog Ground.
6	$\overline{PD}/\overline{RST}$	I	Power-Down Reset (Active Low).
7	MCLKIN	I	Master Clock Input.
8	FAULT	O	Fault Output. Programmable logic output.
9	SA_MODE	I	Standalone Mode. Connect this pin to IOVDD using a 10 kΩ pull-up resistor for standalone mode.
10	DVDD	O	1.8 V Digital Power Supply Output. Decouple this pin to DGND with a 0.1 µF capacitor.
11	DGND	P	Digital Ground.
12	IOVDD	P	Digital Input and Output Power Supply. Connect this pin to a supply in the range of 1.8 V to 3.3 V.
13	SDATAOUT1	O	ADC Serial Data Output Pair 1.
14	SDATAOUT2	O	ADC Serial Data Output Pair 2.
15	LRCLK	I/O	Frame Clock for the ADC Serial Port.
16	BCLK	I/O	Bit Clock for the ADC Serial Port.
17	SDA/COUT	I/O	Serial Data Output I²C/Control Data Output (SPI).
18	SCL/CCLK	I	Serial Clock Input I²C/Control Clock Input (SPI).
19	ADDR0/$\overline{CLATCH}$	I	Chip Address Bit 0 Setting I²C/Chip Select Input for Control Data (SPI).
20	ADDR1/CIN	I	Chip Address Bit 1 Setting I²C/Control Data Input (SPI).
21	PGND	P	Power Ground Boost Converter.
22	PGND	P	Power Ground Boost Converter.
23	SW	I	Inductor Switching Terminal.
24	SW	I	Inductor Switching Terminal.
25	VBOOST_OUT	O	Boost Converter Output. Decouple this pin to PGND with a 10 µF capacitor.
26	VBOOST_IN	I	MICBIAS Regulator Input. Connect this pin to VBOOST_OUT (Pin 25).
27	MICBIAS	O	Microphone Bias Output. Decouple this pin to AGNDx using a 10 µF capacitor.
28	MB_GND	P	Analog Return Ground for the Microphone Bias Regulator. Connect this pin directly to AGNDx for best noise performance.
29	AGND3	P	Analog Ground.
30	VBAT	I	Voltage Sense for Diagnostics. Connect this pin to a load dump suppressed battery voltage. Decouple this to AGNDx using a 0.1 µF capacitor.

Pin No.	Mnemonic	In/Out[1]	Description
31	AVDD3	P	Analog Power Supply. Connect this pin to an analog 3.3 V supply.
32	AIN1N	I	Analog Input Channel 1 Inverting Input.
33	AIN1P	I	Analog Input Channel 1 Noninverting Input.
34	AIN2N	I	Analog Input Channel 2 Inverting Input.
35	AIN2P	I	Analog Input Channel 2 Noninverting Input.
36	AIN3N	I	Analog Input Channel 3 Inverting Input.
37	AIN3P	I	Analog Input Channel 3 Noninverting Input.
38	AIN4N	I	Analog Input Channel 4 Inverting Input.
39	AIN4P	I	Analog Input Channel 4 Noninverting Input.
40	AVDD1	P	Analog Power Supply. Connect this pin to an analog 3.3 V supply.
	EP		Exposed Pad. The exposed pad must be connected to the ground plane on the printed circuit board (PCB).

[1] I = input, O = output, I/O = input/output, and P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

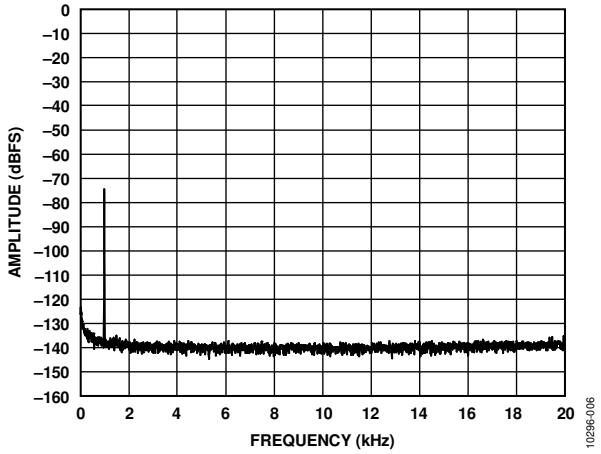


Figure 6. Fast Fourier Transform, 2 mV Differential Input at f_S = 48 kHz

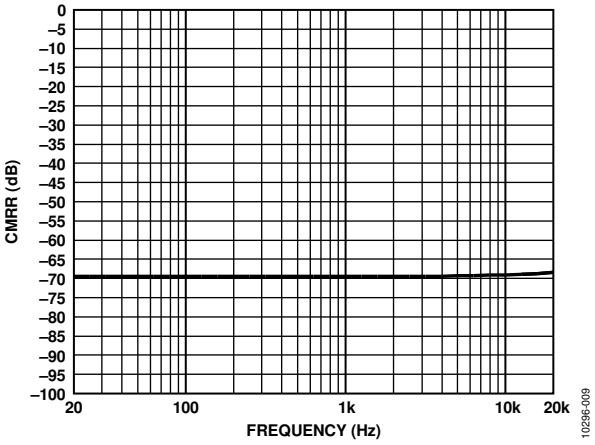


Figure 9. CMRR Differential Input, Referenced to 1 V Differential Input

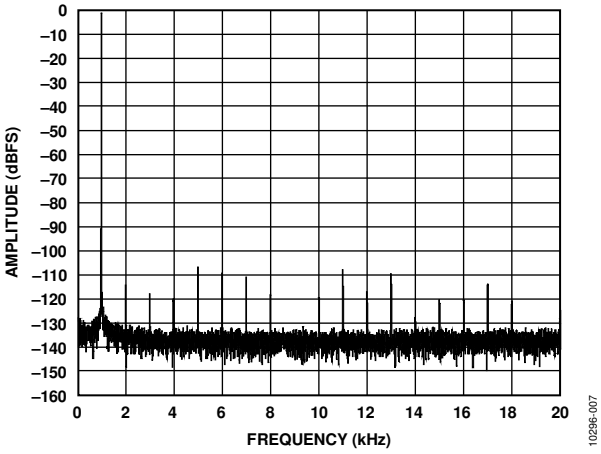


Figure 7. Fast Fourier Transform, −1 dBFS Differential Input

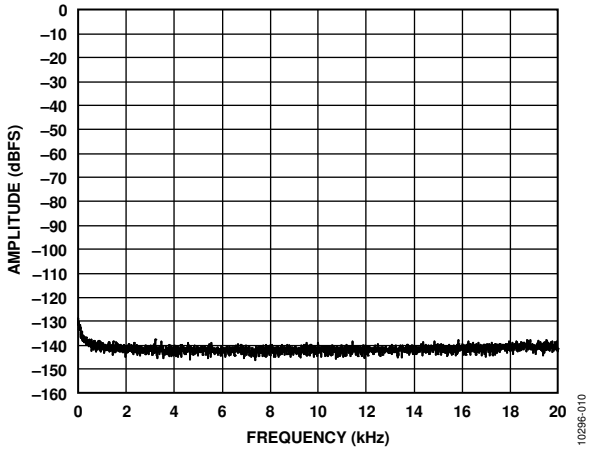


Figure 10. Fast Fourier Transform, No Input

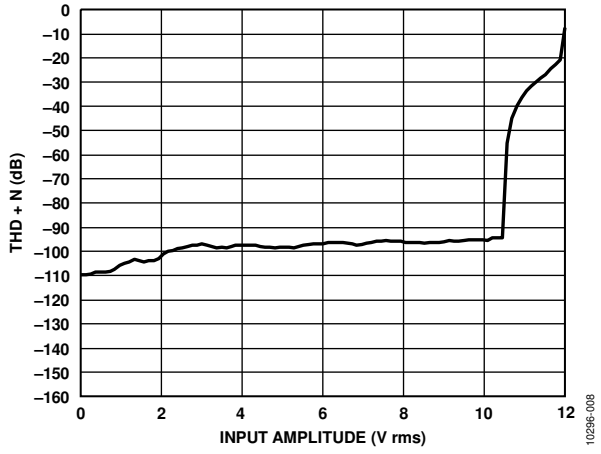


Figure 8. THD + N vs. Input Amplitude

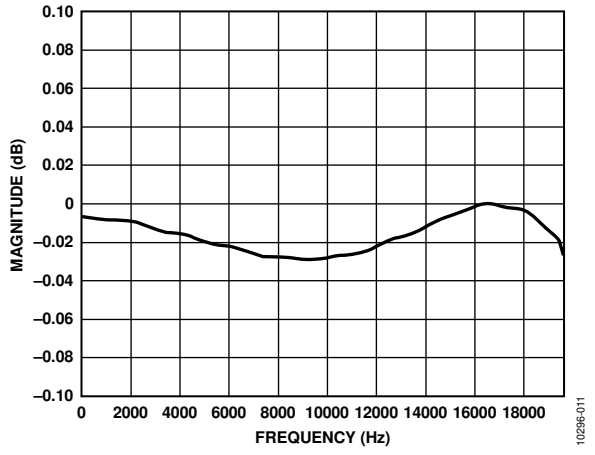


Figure 11. ADC Pass-Band Ripple at f_S = 48 kHz

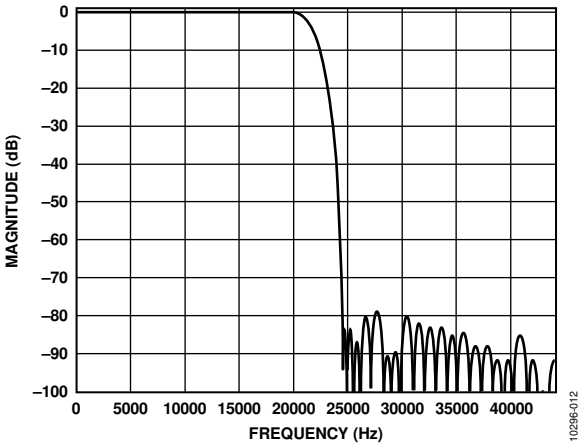


Figure 12. ADC Filter Stop-Band Response at f_S = 48 kHz

THEORY OF OPERATION

OVERVIEW

The ADAU1977 incorporates four high performance ADCs with an integrated boost converter for microphone bias, the associated microphone diagnostics for fault detection, and a phase-locked loop circuit for generating the necessary on-chip clock signals.

POWER SUPPLY AND VOLTAGE REFERENCE

The ADAU1977 requires a single 3.3 V power supply. Separate power supply input pins are provided for the analog and boost converter. These pins should be decoupled to AGND with 100 nF ceramic chip capacitors placed as close as possible to the pins to minimize noise pickup. A bulk aluminum electrolytic capacitor of at least 10 µF must be provided on the same PCB as the ADC. It is important that the analog supply be as clean as possible for best performance.

The supply voltage for the digital core (DVDD) is generated using an internal low dropout regulator. The typical DVDD output is 1.8 V and must be decoupled using a 100 nF ceramic capacitor and a 10 µF capacitor. Place the 100 nF ceramic capacitor as close as possible to the DVDD pin.

The voltage reference for the analog blocks is generated internally and output at the VREF pin (Pin 2). The typical voltage at the pin is 1.5 V with an AVDDx of 3.3 V.

All digital inputs are compatible with TTL and CMOS levels. All outputs are driven from the IOVDD supply. The IOVDD can be in the range of 1.8 V to 3.3 V. The IOVDD pin must be decoupled with a 100 nF capacitor placed as close to the IOVDD pin as possible. It is recommended to connect the AGND, DGND, PGND, and exposed pad to a single GND plane on the PCB for best performance.

The ADC internal voltage reference is output from the VREF pin and should be decoupled using a 100 nF ceramic capacitor in parallel with a 10 µF capacitor. The VREF pin has limited current capability. The voltage reference is used as a reference to the ADC; therefore, it is recommended not to draw current from this pin for external circuits. When using this reference, use a noninverting amplifier buffer to provide a reference to other circuits in the application.

In reset mode, the VREF pin is disabled to save power and is enabled only when the $\overline{\text{RST}}$ pin is pulled high.

POWER-ON RESET SEQUENCE

The ADAU1977 requires that a single 3.3 V power supply be provided externally at the AVDDx pin. The part internally generates DVDD (1.8 V), which is used for the digital core of the ADC. The DVDD supply output pin (Pin 10) is provided to connect the decoupling capacitors to DGND. The typical recommended values for the decoupling capacitors are 100 nF in parallel with 10 µF. During a reset, the DVDD regulator is disabled to reduce power consumption. After the $\overline{\text{PD}}/\overline{\text{RST}}$ pin (Pin 6) is pulled high, the part enables the DVDD regulator. However, the internal ADC and digital core reset is controlled by the internal $\overline{\text{POR}}$ signal (power-on reset) circuit, which monitors the DVDD level. Therefore, the device does not come out of a reset until DVDD reaches 1.2 V and the $\overline{\text{POR}}$ signal is released. The DVDD settling time depends on the charge-up time for the external capacitors and on the AVDDx ramp-up time.

The internal POR circuit is provided with hysteresis to ensure that a reset of the part is not initiated by an instantaneous glitch on DVDD. The typical trip points are 1.2 V with $\overline{\text{RST}}$ high and 0.6 V (±20%) with $\overline{\text{RST}}$ low. This ensures that the core is not reset until the DVDD level falls below the 0.6 V trip point.

As soon as the $\overline{\text{PD}}/\overline{\text{RST}}$ pin is pulled high, the internal regulator starts charging up the C_{EXT} on the DVDD pin. The DVDD charge-up time is based on the output resistance of the regulator and the external decoupling capacitor. The time constant can be calculated as

$$t_C = R_{OUT} \times C_{EXT} \ (R_{OUT} = 20\ \Omega \text{ typical})$$

For example, if C_{EXT} is 10 µF, then t_C is 200 µs and is the time to reach the DVDD voltage, within 63.6%.

The POR circuit releases an internal reset of the core when DVDD reaches 1.2 V (see Figure 13). Therefore, it is recommended to wait for at least the t_C period to elapse before sending I^2C or SPI control signals.

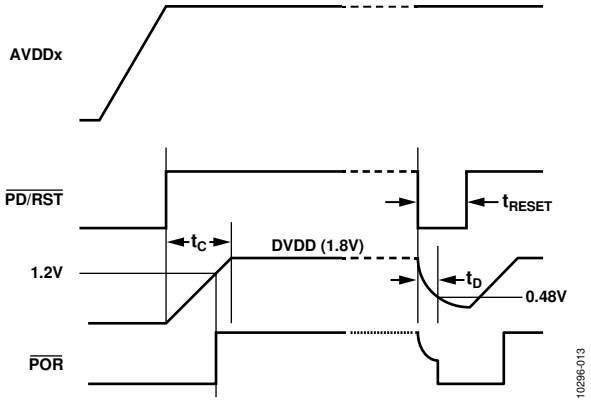


Figure 13. Power-On Reset Timing

When applying a hardware reset to the part by pulling the $\overline{\text{PD}}/\overline{\text{RST}}$ pin (Pin 6) low and then high, there are certain time restrictions. During the $\overline{\text{RST}}$ low pulse period, the DVDD starts discharging. The discharge time constant is decided by the internal resistance of the regulator and C_{EXT}. The time required for DVDD to fall from 1.8 V to 0.48 V (0.6 V − 20%) can be estimated using the following equation:

$$t_D = 1.32 \times R_{INT} \times C_{EXT}$$

where R_{INT} = 64 kΩ typical. (R_{INT} can vary due to process by ±20%.)

For example, if C_{EXT} is 10 µF, then t_D is 0.845 sec.

Depending on C_{EXT}, t_D may vary and in turn decide the minimum hold period for the $\overline{RST}$ pulse. The $\overline{RST}$ pulse must be held low for the t_D time period to initialize the core properly.

The required $\overline{RST}$ low pulse period can be reduced by adding a resistor across C_{EXT}. The new t_D value can then be calculated as

$$t_D = 1.32 \times R_{EQ} \times C_{EXT}$$

where $R_{EQ} = 64\ k\Omega \parallel R_{EXT}$.

The resistor ensures that DVDD not only discharges quickly during a reset or an AVDDx power loss but also resets the internal blocks correctly. Note that some power loss in this resistor is to be expected because the resistor constantly draws current from DVDD. The typical value for C_{EXT} is 10 µF and for R_{EXT} is 3 kΩ. This results in a time constant of

$$t_D = 1.32 \times R_{EQ} \times C_{EXT} = 37.8\ ms$$

where $R_{EQ} = 2.866\ k\Omega$ (64 kΩ || 3 kΩ).

Using this equation at a set C_{EXT} value, the R_{EXT} can be calculated for a desired $\overline{RST}$ pulse period.

There is also a software reset register (S_RST, Bit 7 of Register 0x00) available that can be used to reset the part, but it must be noted that during an AVDDx power loss, the software reset may not ensure proper initialization because DVDD may not be stable.

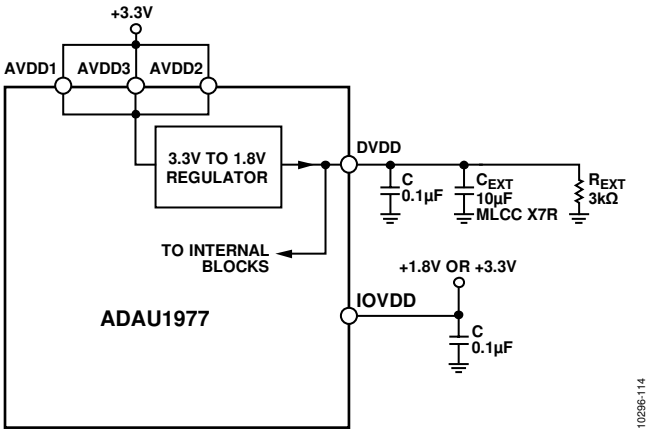


Figure 14. DVDD Regulator Output Connections

PLL AND CLOCK

The ADAU1977 has a built-in analog PLL to provide a jitter-free master clock to the internal ADC. The PLL must be programmed for the appropriate input clock frequency. The PLL Control Register 0x01 is used for setting the PLL.

The CLK_S bit (Bit 4) of Register 0x01 is used for setting the clock source for the PLL. The clock source can be either the MCLKIN pin or the LRCLK pin (slave mode). In LRCLK mode, the PLL can support sample rates between 32 kHz and 192 kHz.

In MCLK input mode, the MCS bits (Bits[2:0] of Register 0x01) must be set to the desired input clock frequency for the MCLKIN pin. Table 10 shows the input MCLK required for the most common sample rates and the MCS bit settings.

The PLL_LOCK bit (Bit 7) of Register 0x01 indicates the lock status of the PLL. It is recommended that after initial power-up the PLL lock status be read to ensure that the PLL outputs the correct frequency before unmuting the audio outputs.

Table 10. Required Input MCLK for Common Sample Rates

MCS (Bits[2:0])	f_S (kHz)	Frequency Multiplication Ratio	MCLKIN Frequency (MHz)
000	32	128 × f_S	4.096
001	32	256 × f_S	8.192
010	32	384 × f_S	12.288
011	32	512 × f_S	16.384
100	32	768 × f_S	24.576
000	44.1	128 × f_S	5.6448
001	44.1	256 × f_S	11.2896
010	44.1	384 × f_S	16.9344
011	44.1	512 × f_S	22.5792
100	44.1	768 × f_S	33.8688
000	48	128 × f_S	6.144
001	48	256 × f_S	12.288
010	48	384 × f_S	18.432
011	48	512 × f_S	24.576
100	48	768 × f_S	36.864
000	96	64 × f_S	6.144
001	96	128 × f_S	12.288
010	96	192 × f_S	18.432
011	96	256 × f_S	24.576
100	96	384 × f_S	36.864
000	192	32 × f_S	6.144
001	192	64 × f_S	12.288
010	192	96 × f_S	18.432
011	192	128 × f_S	24.576
100	192	192 × f_S	36.864

The PLL can accept the audio frame clock (sample rate clock) as input, but the serial port must be configured as a slave and the frame clock must be fed to the part from the master. It is strongly recommended that the PLL be disabled, reprogrammed with the new setting, and then reenabled. A lock bit is provided that can be polled via the I²C to check whether the PLL has acquired lock.

The PLL requires an external filter, which is connected at the PLL_FILT pin (Pin 3). The recommended PLL filter circuit for MCLK or LRCLK mode is shown in Figure 15. Using NPO capacitors is recommended for temperature stability. Place the filter components close to the device for best performance.

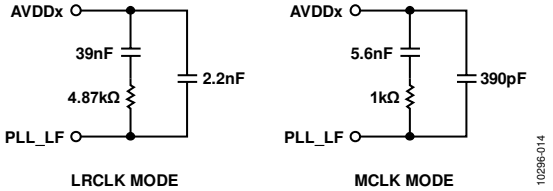


Figure 15. PLL Filter

DC-TO-DC BOOST CONVERTER

The boost converter generates a supply voltage for the microphone bias circuit from a fixed 3.3 V supply. The boost converter output voltage is programmable using Register 0x03. The boost converter output voltage is approximately 1 V above the set microphone bias voltage. The boost converter uses the clock from the PLL, and the switching frequency is dependent on the sample rate of the ADC. The FS_RATE bits (Bits[6:5] of Register 0x02) must be set to the desired sample rate. The boost converter switching frequency can be selected to be 1.5 MHz or 3 MHz using Bit 4 of Register 0x02. For the 1.5 MHz switching frequency, the recommended value for the inductor is 4.7 µH, whereas for the 3 MHz switching frequency, the recommended value for the inductor is 2.2 µH.

Table 11 lists the typical switching frequency based on the sample rates.

Capacitor Selection

The boost converter output is available at the VBOOST_OUT pin (Pin 25) and must be decoupled to PGND using a 10 µF ceramic capacitor to remove the ripple at the switching frequency. The capacitor must have low ESR and good temperature stability. The MLCC X7R/NPO dielectric type with 25 V is recommended. Care must be taken to place this capacitor as close as possible to the VBOOST_OUT pin (Pin 25).

Table 11. Typical Switching Frequency Based on the Sample Rates

		Boost Converter Switching Frequency	
Base Sample Rate (kHz)	**Sample Rates (kHz)**	**Inductor = 2.2 µH**	**Inductor = 4.7 µH**
32	8/16/32/64	(1024/12) × f_S	(1024/22) × f_S
44.1	11.025/22.05/44.1/88.2/176.4	(1024/16) × f_S	(1024/30) × f_S
48	12/24/48/96/192	(1024/16) × f_S	(1024/32) × f_S

MICROPHONE BIAS

The microphone bias is generated by the input voltage at the VBOOST_IN pin (Pin 26) via a linear regulator to ensure low noise performance and to reject the high frequency noise from the boost converter. If the internal boost converter output is used, the VBOOST_OUT pin (Pin 25) must be connected to the VBOOST_IN pin (Pin 26). If an external supply is used for the microphone bias, the supply can be fed at the VBOOST_IN pin (Pin 26); in this case, leave the VBOOST_OUT pin (Pin 25) open. The microphone bias voltage is programmable from 5 V to 9 V by using the MB_VOLTS bits (Bits[7:4] of Register 0x03). The microphone bias output voltage is available at the MICBIAS pin (Pin 27). This pin can be decoupled to AGND using a maximum of up to a 10 µF capacitor with an ESR of at least 1 Ω. For higher value capacitors, especially those above 1 nF, the ESR of the capacitor should be ≥ 1 Ω to ensure the stability of the microphone bias regulator. Register 0x03 can be used to enable the microphone bias. Table 11 lists the switching frequency of the boost converter based on the inductor value and common sample rates.

ANALOG INPUTS

The ADAU1977 has four differential analog inputs. The ADCs can accommodate both dc- and ac-coupled input signals.

The block diagram shown in Figure 16 represents the typical input circuit.

In most audio applications, the dc content of the signal is removed by using a coupling capacitor. However, the ADAU1977 consists of a unique input structure that allows direct coupling of the input signal, eliminating the need for using a large coupling capacitor at the input. Each input has a fixed 14 dB attenuator connected to AGND for accommodating a 10 V rms differential input. The typical input resistance is approximately 26 kΩ from each input to AGND.

In dc-coupled applications, if the V_{CM} at AINxP and AINxN is the same, the dc content in the ADC output is close to 0. If the input pins are presented with different common-mode dc levels, the difference between the two levels appears at the ADC output and can be removed by enabling the high-pass filter.

The high-pass filter has a 1.4 Hz, 6 dB per octave cutoff at a 48 kHz sample rate. The cutoff frequency scales directly with the sample frequency. However, care is required in dc-coupled applications to ensure that the common-mode dc voltage does not exceed the specified limit. The common-mode loop can accommodate a common-mode dc voltage from 0 V to 7 V. The input required for the full-scale ADC output (0 dBFS) is typically 10 V rms differential.

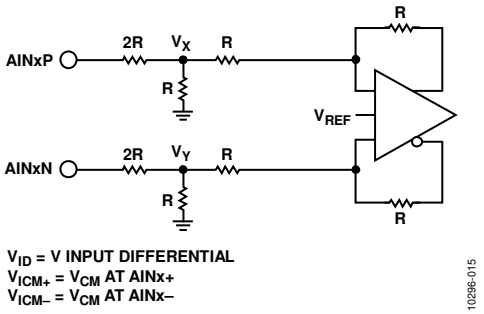


Figure 16. Analog Input Block

Line Inputs

This section describes some of the possible ways to connect the ADAU1977 for line level inputs.

Line Input Balanced or Differential Input DC-Coupled Case

For example, in the case of a typical power amplifier for an automobile, the output can swing around 10 V rms differential with approximately 7.2 V common-mode dc input voltage (assuming a 14.4 V battery and bridge-tied load connection). The signal at each input pin has a 5 V rms or 14.14 V p-p signal swing. With a common-mode dc voltage of 7.2 V, the signal can swing between (7.2 V + 7.07 V) = +14.27 V p-p and (7 V − 7.07 V) = 0.13 V at each input. Therefore, this results in approximately a 28.54 V p-p differential signal swing and measures around −0.16 dBFS (ac only with dc high-pass filter) at the ADC output. See Figure 17.

Line Input Balanced or Differential Input AC-Coupled Case

For an amplifier output case with ac coupling, refer to Figure 18 for information about connecting the line level inputs to the ADAU1977. In this case, the AINxP/AINxN pins must be pulled up to the required common-mode level using the resistors on MICBIAS. The V_{CM} must be such that the input never swings below a ground. In other words, if the input signal is 14 V p-p, the V_{CM} must be around 14 V/2 = 7 V to ensure that the signal never swings below a ground. The microphone bias can provide the required clean reference for generating the V_{CM}.

The R1 value can be calculated as follows:

$$R1 = Rin_{1977}\,(MB - V_{CM})/V_{CM}$$

where:
V_{CM} is the peak-to-peak input swing divided by 2.
MB = 8.5 V.
Rin_{1977} is the single-ended input resistance (see Table 1).

However, in this case the equivalent input resistance of AINxP/AINxN is reduced and can be calculated as R1 || Rin_{1977}.

$$Input\ Resistance = R1 \times Rin_{1977}/(R1 + Rin_{1977})$$

where Rin_{1977} is the single-ended value from Table 1.

The C1 and C2 values can be determined for the required low frequency cutoff using the following equation:

$$C1 \text{ or } C2 = 1/(2 \times \pi \times f_C \times Input\ Resistance)$$

Line Input Unbalanced or Single-Ended Pseudo Differential AC-Coupled Case

For a single-ended application, the signal swing is reduced by half because only one input is used for the signal, and the other input is connected to 0 V. As a result, the input signal capability is reduced to 5 V rms in a single-ended application. With a common-mode dc voltage of 7.2 V, the signal can swing between (7.2 V + 7.07 V) = +14.27 V p-p and (7.2 V − 7 V) = 0.13 V. Therefore, this results in approximately a 14.14 V p-p differential signal swing and measures around −6.16 dBFS (ac only with dc high-pass filter) at the ADC output. See Figure 19.

The values of the resistors (R1/R2) and capacitors (C1/C2) are similar to those for the balanced ac-coupled case described in the Line Input Balanced or Differential Input AC-Coupled Case section.

Line Input Unbalanced or Single-Ended AC-Coupled Case

For a single-ended application, the signal swing is reduced by half because only one input is used for the signal, and the other input is connected to 0 V. As a result, the input signal capability is reduced to 5 V rms in a single-ended application. With a common-mode dc voltage of 7.2 V, the signal can swing between (7.2 V + 7.07 V) = +14.27 V p-p and (7.2 V − 7 V) = 0.13 V. Therefore, this results in approximately a 14.14 V p-p differential signal swing and measures around −6.16 dBFS (ac only with dc high-pass filter) at the ADC output. The difference in the common-mode dc voltage between the positive and negative input (7.2 V) would appear at the ADC output if the signal was not high-pass filtered. See Figure 20.

The values of the resistor (R1) and capacitor (C1) are similar to those for the balanced ac-coupled case described in the Line Input Balanced or Differential Input AC-Coupled Case section.

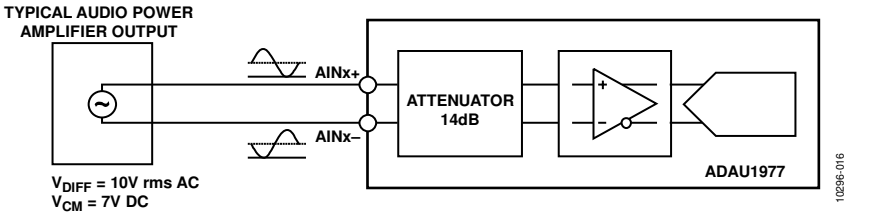


Figure 17. Connecting the Line Level Inputs—Differential DC-Coupled Case

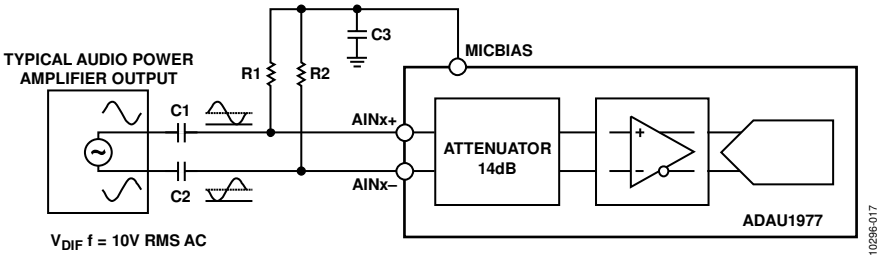


Figure 18. Connecting the Line Level Inputs—Differential AC-Coupled Case

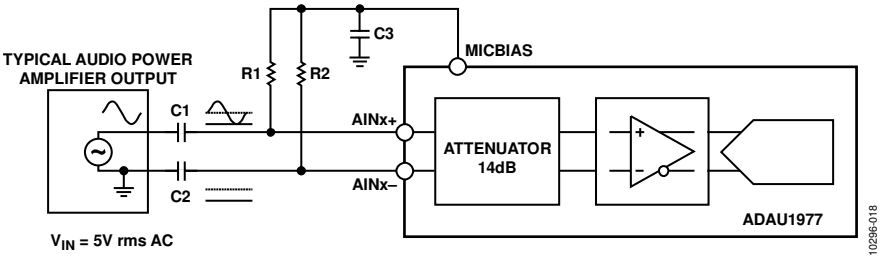


Figure 19. Connecting the Line Level Inputs—Pseudo Differential AC-Coupled Case

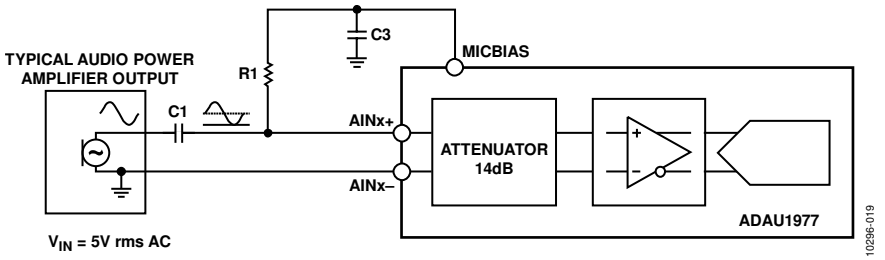


Figure 20. Connecting the Line Level Inputs—Single-Ended AC-Coupled Case

Microphone Inputs

This section describes some ways to connect the ADAU1977 for microphone input applications. The MICBIAS voltage and the bias resistor value depend on the ECM selected. The ADAU1977 can provide the MICBIAS from 5 V up to 9 V in 0.5 V steps. In an application requiring multiple microphones, care must be taken not to exceed the MICBIAS output current rating.

ECM Balanced or Differential Input DC-Coupled Case

For example, in a typical ECM, the output signal swing depends on the MICBIAS voltage. With a typical 8.5 V supply, the ECM can output a 2 V rms differential signal. The signal at each input pin has a 1 V rms or 2.8 V p-p signal swing. With a common-mode dc level of 2/3 × MICBIAS on the AINxP and 1/3 × MICBIAS on the AINxN pins, this results in around −14 dBFS (ac only with dc high-pass filter) at the ADC output because the input is 14 dB below the full-scale input of 10 V rms differential. See Figure 21.

ECM Pseudo Differential Input AC-Coupled Case

For a typical MEMS ECM module, the output signal swing is low. With a typical 3.3 V supply, the ECM module can output a 2 V rms differential signal. The signal at the input pin has a 1 V rms or 2.8 V p-p signal swing. For this application, it is recommended to bias the input pins using resistors to 7 V dc, similar to the case described in the Line Input Unbalanced or Single-Ended Pseudo Differential AC-Coupled Case section. See Figure 22.

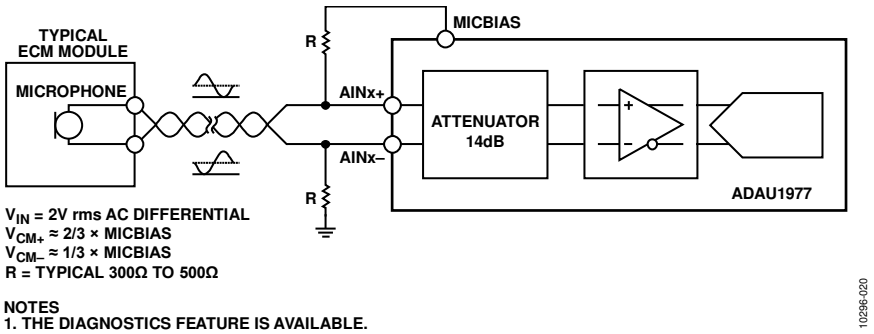


Figure 21. Connecting the Microphone Inputs—Differential Input DC-Coupled Case

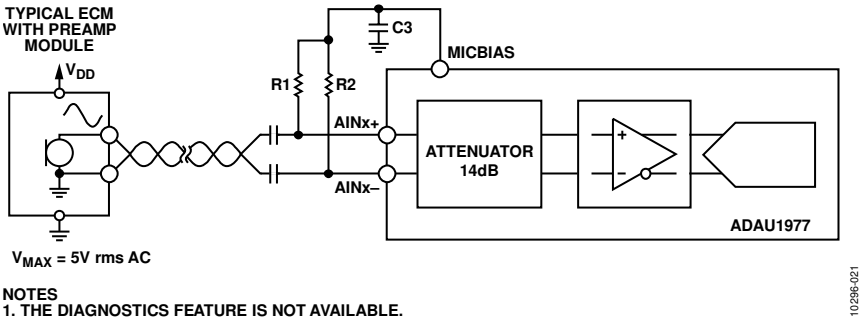


Figure 22. Connecting the Microphone Inputs—Pseudo Differential Input AC-Coupled Case

ADC

The ADAU1977 contains four Δ-Σ ADC channels configured as two stereo pairs with configurable differential/single-ended inputs. The ADC can operate at a nominal sample rate of 32 kHz up to 192 kHz. The ADCs include on-board digital antialiasing filters with 79 dB stop-band attenuation and linear phase response. Digital outputs are supplied through two serial data output pins (one for each stereo pair) and a common frame clock (LRCLK) and bit clock (BCLK). Alternatively, one of the TDM modes can be used to support up to 16 channels on a single TDM data line.

With smaller amplitude input signals, a 10-bit programmable digital gain compensation for an individual channel is provided to scale up the output word to full scale. Care must be taken to avoid overcompensation (large gain compensation), which leads to clipping and THD degradation in the ADC.

The ADCs also have a dc-offset calibration algorithm to null the systematic dc offset of the ADC. This feature is useful for dc measurement applications.

Inductor Selection

For the boost converter to operate efficiently, the inductor selection is critical. The two most important parameters for the inductor are the saturation current rating and the dc resistance. The recommended saturation rating for the inductor must be >1 A. The dc resistance affects the efficiency of the boost converter. Assuming that the board trace resistances are negligible for 80% efficiency, the dc resistance of the inductor should be less than 50 mΩ.

Table 12 lists some of the recommended inductors for the application.

Table 12. Recommended Inductors[1]

Value	Manufacturer	Manufacturer Part Number
2.2 µH	Würth Elektronik	7440430022
4.7 µH	Würth Elektronik	7440530047

[1] Check with the manufacturer for the appropriate temperature ratings for a given application.

The boost converter has a soft start feature that prevents inrush current from the input source.

The boost converter has built-in overcurrent and overtemperature protection. The input current to the boost converter is monitored and if it exceeds the set current threshold for 1.2 ms, the boost converter shuts down. The fault condition is recorded into Register 0x02 and asserts the fault interrupt pin. This condi tion is cleared after reading the BOOST_OV bit (Bit 2) or the BOOST_OC bit (Bit 0) in Register 0x02. The overcurrent protection bit, OC_EN (Bit 1), or the overvoltage protection bit, OV_EN (Bit 3), is on by default, and it is recommended not to disable the bit.

Each protection circuit has two modes for recovery after a fault event: autorecovery and manual recovery. The recovery mode can be selected using Bit 0 of Register 0x03. The autorecovery mode attempts to enable the boost converter after a set recovery time, typically 20 ms. The manual recovery mode enables the boost converter only if the user writes 1 to the MRCV bit (Bit 1). If the fault persists, the boost converter remains in shutdown mode until the fault is cleared.

The boost converter is capable of supplying the 42 mA of total output current at the MICBIAS output. The boost converter has overcurrent protection at the input; the threshold is around 900 mA peak. Ensure that the 3.3 V power supply feeding the boost converter has built-in overcurrent protection because there is no protection internal to ADAU1977 for a short circuit to any of the ground pins (AGND/DGND/PGND) at the VBOOST_OUT or VBOOST_IN pin.

By default, the boost converter is disabled on power-up to allow the flexibility of connecting an external voltage source at the VBOOST_IN pin to power the microphone bias circuit. The boost converter can be enabled by using the BOOST_EN bit (Bit 2 of Register 0x03).

ADC SUMMING MODES

The four ADCs can be grouped into either a single stereo ADC or a single mono ADC to increase the signal-to-noise ratio (SNR) for the application. Two options are available: one option for summing two channels of the ADC and another option for summing all four channels of the ADC. Summing is performed in the digital block.

2-Channel Summing Mode

When the SUM_MODE Bits (Bits[7:6] of Register 0x0E) are set to 01, the Channel 1 and Channel 2 ADC data are combined and output from the SDATAOUT1 pin. Similarly, the Channel 3 and Channel 4 ADC data are combined and output from the SDATAOUT2 pin. As a result, the SNR improves by 3 dB. For this mode, both Channel 1 and Channel 2 must be connected to the same input signal source. Similarly, Channel 3 and Channel 4 must be connected to the same input signal source.

4-Channel Summing Mode

When the SUM_MODE Bits (Bits[7:6] of Register 0x0E) are set to 10, the Channel 1 through Channel 4 ADC data are combined and output from the SDATAOUT1 pin. As a result, the SNR improves by 6 dB. For this mode, all four channels must be connected to the same input signal source.

DIAGNOSTICS

The diagnostics block monitors the input pins in real time and reports a fault as an interrupt signal on the FAULT pin (Pin 8), which triggers sending an interrupt request to an external controller. The diagnostics status registers (Register 0x11 through Register 0x14) for Channel 1 through Channel 4 are also updated. Refer to the register map table (Table 25) and the register details tables (Table 42, Table 43, Table 44, and Table 45) for more information about the diagnostics register content. The diagnostics can be enabled or disabled for each channel using Bits[3:0] of Register 0x10. The diagnostics are provided only when MICBIAS is enabled and the microphone is connected as recommended in the appropriate application circuit (see Figure 21).

Diagnostics Reporting

The diagnostics status is reported individually for each channel in Register 0x11 through Register 0x14. The faults listed in Table 13 are reported on each input pin.

Table 13. Faults Reported

Fault	AINxP	AINxN
Short to Battery	Yes	Yes
Short to MICBIAS	Yes	No
Short to Ground	Yes	Yes
Short Between Positive and Negative Inputs	Yes	Yes
Open Input	Yes	Yes

Diagnostics Adjustments

Short Circuit to Battery Supply

When an input terminal is shorted to the battery, the voltage at the terminal approaches the battery voltage. Any voltage higher than the set threshold is reported as a fault. The threshold can be set using the SHT_B_TRIP bits, Bits[1:0] of Register 0x17 (see Table 14).

Table 14. Setting the Short to Battery Threshold

SHT_B_TRIP (Register 0x17, Bits[1:0])	Short to Battery Threshold
00	0.95 × VBAT
01	0.9 × VBAT
10	0.85 × VBAT
11	0.975 × VBAT

Short Circuit to MICBIAS

This feature is supported only on the AINxP terminal. When an AINxP terminal is shorted to MICBIAS, the voltage at the AINxP terminal approaches the MICBIAS voltage. Any voltage higher than the set threshold is reported as a fault. The threshold can be set using the SHT_M_TRIP bits, Bits[5:4] of Register 0x17 (see Table 15).

Table 15. Setting the Short to MICBIAS Threshold

SHT_M_TRIP (Register 0x17, Bits[5:4])	Short to MICBIAS Threshold
00	0.95 × MICBIAS
01	0.9 × MICBIAS
10	0.85 × MICBIAS
11	0.975 × MICBIAS

Short Circuit to Ground

When an input terminal is shorted to ground, the terminal voltage reaches close to 0 V. Any voltage lower than the set threshold is reported as a fault. The threshold is referenced to VREF and, therefore, scales with the voltage at the VREF pin. The threshold can be set using the SHT_G_TRIP bits, Bits[3:2] of Register 0x17 (see Table 16).

Table 16.

SHT_G_TRIP (Register 0x17, Bits[3:2])	Short to Ground Threshold
00	0.2 × VREF
01	0.133 × VREF
10	0.1 × VREF
11	0.266 × VREF

Microphone Terminal Short Circuited

When both input terminals are shorted, both the AINxP and AINxN input terminals are at the same voltage—around MICBIAS/2. Any voltage between the set thresholds is reported as a fault. The upper and lower threshold voltages can be set using the SHT_T_TRIP bits, Bits[7:6] of Register 0x17 (see Table 17).

The following equations can be used to calculate the upper and lower thresholds:

$$Upper\ Threshold = MICBIAS(0.5 + x)$$

$$Lower\ Threshold = MICBIAS(0.5 - x)$$

where x can be set using the SHT_T_TRIP bits, Bits[7:6] of Register 0x17 (see Table 17).

Table 17.

SHT_T_TRIP (Register 0x17, Bits [7:6])	x
00	0.035
01	0.017
10	0.071
11	Reserved

Microphone Terminals Open

In the event that any of the input terminals becomes open circuited, AINxP is pulled to MICBIAS and AINxN is pulled to a common ground. When the AINxP terminal is at a voltage that is higher than the short to the MICBIAS threshold (set using Bits[5:4] of Register 0x17) and the AINxN terminal voltage is at a voltage that is less than the short to the ground threshold (set using Bits[3:2] of Register 0x17), a fault is reported. The fault cannot indicate which terminal is open circuited because any terminal that is open circuited pulls AINxP to MICBIAS and AINxN to a common ground.

FAULT Pin

The FAULT pin is an output pin that can be programmed to be active high or active low logic using the IRQ_POL bit (Bit 4 of Register 0x15). In addition, the FAULT pin can be set using the IRQ_DRIVE bit (Bit 5 of Register 0x15) to drive always or to drive only during a fault and is otherwise set to high-Z. The fault status is registered in the IRQ_RESET bit (Bit 6 of Register 0x15). The IRQ_RESET bit is a latched bit and is set in the event of a fault and cleared only after the fault status bit is read.

Fault Timeout

To prevent the false triggering of a fault event, the fault timeout adjust bits (Bits[5:4] of Register 0x18) are provided. These bits can be used to set the time that the fault needs to persist before being reported. The timeout can be set to 0 ms, 50 ms, 100 ms, or 150 ms using the FAULT_TO bits (Bits[5:4] of Register 0x18). The default value is 100 ms. A fault is recorded only if the condition persists for more than a set minimum timeout.

Fault Masking

The faults can be masked to prevent triggering an interrupt on the FAULT pin. Fault masking can be set using Bits[6:0] of Register 0x16. The mask can be set for the faults listed in Table 18.

Table 18. Fault Masking

Fault	AINxP	AINxN
Short to Battery	Yes	Yes
Short to MICBIAS	Yes	No
Short to Ground	Yes	Yes
Short Between Positive and Negative Inputs	Yes	Yes
Open Input	Yes	Yes

When a fault mask bit is set, it is applied to all the channels. There is no individual fault mask available per channel using this bit. To mask individual channels, use the DIAG_MASK[4:1] bits (Bits[3:0] of Register 0x15).

Diagnostics Sequence

The sequence shown in Figure 23 is recommended for reading the faults reported by diagnostics.

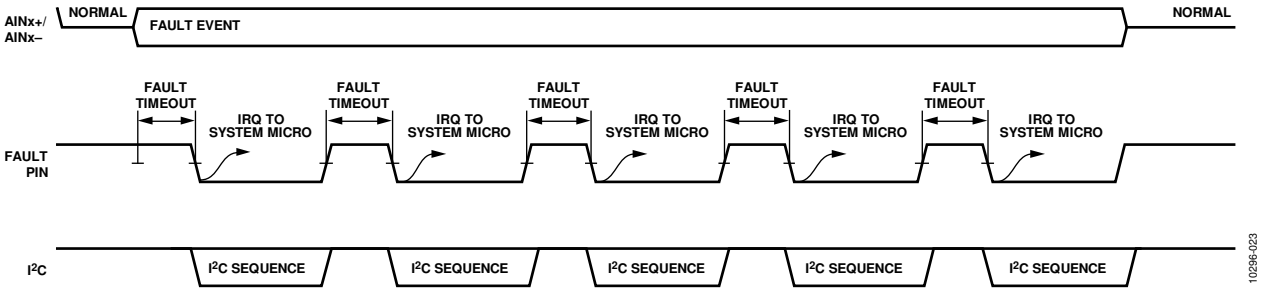


Figure 23. Diagnostics Sequence