Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Audio Processor for Advanced TV

ADAV4601

FEATURES

- Fully programmable 28-bit audio processor for enhanced ATV sound—default audio processing flow loaded on reset
- Implements Analog Devices, Inc. and third-party branded audio algorithms
- Adjustable digital delay line for audio/video Synchronization for up to 200 ms stereo delay
- High performance 24-bit ADC and DAC
  - 94 dB DNR performance on DAC channels
  - 95 dB DNR performance on ADC channels
- Headphone output with integrated amplifiers
- High performance pulse-width modulation (PWM) digital outputs
- Multichannel digital baseband I/O
  - 4 stereo synchronous digital I²S input channels
  - One 6-channel sample rate converter (SRC) and one stereo SRC supporting input sample rates from 5 kHz to 50 kHz
  - One stereo synchronous digital I²S output
  - S/PDIF output with S/PDIF input mux capability
- Fast I²C control
- Operates from 3.3 V (analog), 1.8 V (digital core), and 3.3 V (digital interface)
- Available in 80-lead LQFP

APPLICATIONS

- General-purpose consumer audio post processing
  - Home audio
  - DVD recorders
  - Home theater in a box systems and DVD receivers
- Audio processing subsystems for DTV-ready TVs
- Analog broadcast capability for iDTVs

GENERAL DESCRIPTION

The ADAV4601 is an enhanced audio processor targeting advanced TV applications with full support for digital and analog baseband audio.

The audio processor, by default, loads a dedicated TV audio flow that incorporates full matrix switching (any input to any output), automatic volume control that compensates for volume changes during advertisements or when switching channels, dynamic bass, a multiband equalizer, and up to 200 ms of stereo delay memory for audio-video synchronization.

Alternatively, Analog Devices offers an award-winning graphical programming tool (SigmaStudio™) that allows custom flows to be quickly developed and evaluated. This allows the creation of customer-specific audio flows, including the use of ADI library of third-party algorithms.

The analog I/O integrates Analog Devices proprietary continuous-time, multibit Σ-Δ architecture to bring a higher level of performance to ATV systems, required by third-party algorithm providers to meet system branding certification. The analog input is provided by 95 dB dynamic range (DNR) ADCs, and analog output is provided by 94 dB DNR DACs.

The main speaker outputs can be supplied as a digitally modulated PWM stream to support digital amplifiers.

The ADAV4601 includes multichannel digital inputs and outputs. In addition, digital input channels can be routed through integrated sample rate converters (SRC), which are capable of supporting any arbitrary sample rate from 5 kHz to 50 kHz.

Advantiv
Advanced Television Solutions
by Analog Devices

Rev. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

ADAV4601* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- ADAV4601: Audio Processor for Advanced TV Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- Firmware Loader for SigmaDSPs

DESIGN RESOURCES

- ADAV4601 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADAV4601 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

9/09—Rev. A to Rev. B

Changes to Table 11 24
Changes to Table 15 31
Changes to Table 16 32
Changes to Table 40 45
Changes to Table 50 51
Changes to Table 51 53
Changes to Table 54 54

4/09—Rev. 0 to Rev. A

Added Advantiv Logo 1
Changes to General Description Section 1
Changes to Figure 1 3
Changes to Table 2 6
Changes to FILTA and FILTD Section, AVDD Section, and VDD Section 15
Added Power-Up Sequence Section and Figure 22; Renumbered Sequentially 16
Changes to Master Clock Oscillator Section 16
Added Table 6, Table 7, Table 8, Table 9, and Figure 23; Renumbered Sequentially 17
Added Figure 24 18
Changes to ADC Inputs Section and Figure 25 18
Added Figure 31 21
Changes to DAC Voltage Outputs Section, Figure 30, PWM Outputs Section, Headphone Output Section, and Figure 33 21
Added Figure 36 22
Changes to Hardware Mute Control Section 22
Added SigmaStudio Pin Assignment Section, Table 10, Table 11, and Numeric Formats Section 23
Changes to Application Layer Section 23
Added Figure 38, ROMs and Registers Section, Safe Loading to Parameter RAM and Target/Slew RAM Section, and Read/Write Data Formats Section 24
Added Target/Slew RAM Section, Table 12, Table 13, and Table 14 25
Added Figure 39, Figure 40, Figure 41, Figure 42, and Figure 43 26
Added Figure 44, Figure 45, Figure 46, and Layout Recommendations Section 27
Changes to Figure 47 28
Added Figure 48 29
Added Table 15 to Table 61 30

3/08—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

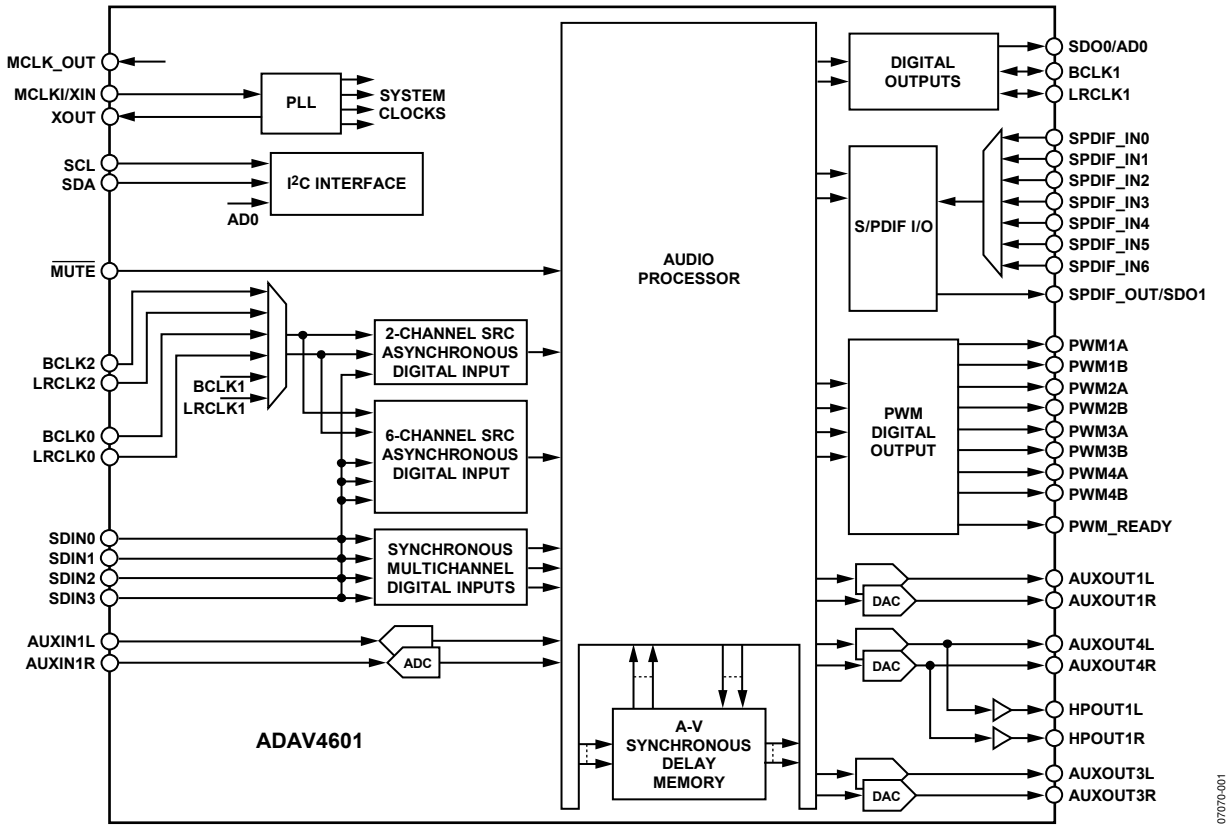

Figure 1. ADAV4601 with PWM-Based Speaker Outputs

SPECIFICATIONS

AVDD = 3.3 V, DVDD = 1.8 V, ODVDD = 3.3 V, operating temperature = −40°C to +85°C, master clock 24.576 MHz, measurement bandwidth = 20 Hz to 20 kHz, ADC input signal = DAC output signal = 1 kHz, unless otherwise noted.

PERFORMANCE PARAMETERS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE SECTION					
Absolute Voltage V_{REF}		1.53		V	
V_{REF} Temperature Coefficient		100		ppm/°C	
ADC SECTION					
Number of Channels		2			One stereo channel
Full-Scale Input Level		100		µA rms	
Resolution		24		Bits	
Dynamic Range (Stereo Channel)					
A-Weighted		95		dB	−60 dBFS with respect to full-scale analog input
Total Harmonic Distortion + Noise (Stereo Channel)		−90		dB	−3 dBFS with respect to full-scale analog input
Gain Mismatch		0.2		dB	Left- and right-channel gain mismatch
Crosstalk (Left-to-Right, Right-to-Left)		−110		dB	
Gain Error		−1		dB	Input signal is 100 µA rms
Current Setting Resistor (R_{ISET})		20		kΩ	External resistor to set current input range of ADC for nominal 2.0 V rms input signal
Power Supply Rejection		−87		dB	1 kHz, 300 mV p-p signal at AVDD
ADC DIGITAL DECIMATOR FILTER CHARACTERISTICS					At 48 kHz, guaranteed by design
Pass Band		22.5		kHz	
Pass-Band Ripple		±0.0002		dB	
Stop Band		26.5		kHz	
Stop-Band Attenuation		100		dB	
Group Delay		1040		µs	
PWM SECTION					
Frequency		384		kHz	Guaranteed by design
Modulation Index		0.976			Guaranteed by design
Dynamic Range					
A-Weighted		98		dB	−60 dBFS with respect to full-scale code input
Total Harmonic Distortion + Noise		−80		dB	−3 dBFS with respect to full-scale code input
DAC SECTION					
Number of Auxiliary Output Channels		6			Three stereo channels
Resolution		24		Bits	
Full-Scale Analog Output		1		V rms	
Dynamic Range					
A-Weighted		94		dB	−60 dBFS with respect to full-scale code input
Total Harmonic Distortion + Noise		−86		dB	−3 dBFS with respect to full-scale code input
Crosstalk (Left-to-Right, Right-to-Left)		−102		dB	
Interchannel Gain Mismatch		0.1		dB	Left- and right-channel gain mismatch
Gain Error		0.525		dB	1 V rms output
DC Bias		1.53		V	
Power Supply Rejection		−90		dB	1 kHz, 300 mV p-p signal at AVDD
Output Impedance		235		Ω	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DAC DIGITAL INTERPOLATION FILTER CHARACTERISTICS					At 48 kHz, guaranteed by design
Pass Band		21.769		kHz	
Pass-Band Ripple		±0.01		dB	
Transition Band		23.95		kHz	
Stop Band		26.122		kHz	
Stop-Band Attenuation		75		dB	
Group Delay		580		µs	
HEADPHONE AMPLIFIER					Measured at headphone output with 32 Ω load
Number of Channels		2			One stereo channel
Full-Scale Output Power		31		mW rms	1 V rms output
Dynamic Range					
A-Weighted		93		dB	−60 dBFS with respect to full-scale code input
Total Harmonic Distortion + Noise		−83		dB	−3 dBFS with respect to full-scale code input
Interchannel Gain Mismatch		0.1		dB	
DC Bias		1.53		V	
Power Supply Rejection		−85		dB	1 kHz, 300 mV p-p signal at AVDD
SRC					
Number of Channels		8			Two channels (SRC1), six channels (SRC2)
Dynamic Range					
A-Weighted		115		dB	−60 dBFS input (worst-case input f_S = 50 kHz)
Total Harmonic Distortion + Noise		−113		dB	−3 dBFS input (worst-case input f_S = 50 kHz)
Sample Rate	5		50	kHz	
SRC DIGITAL INTERPOLATION FILTER CHARACTERISTICS					At 48 kHz, guaranteed by design
Pass Band		21.678		kHz	
Pass-Band Ripple		0.005		dB	
Stop Band		26.232		kHz	
Stop-Band Attenuation		110		dB	
Group Delay		876		µs	
DIGITAL INPUT/OUTPUT					
Input Voltage High (V_{IH})	2.0		ODVDD	V	
Input Voltage Low (V_{IL})			0.8	V	
Input Leakage					
I_{IH} (SDIN0, SDIN1, SDIN2, SDIN3, LRCLK0, LRCLK1, LRCLK2, BCLK0, BCLK1, BCLK2, SPDIF_OUT, SPDIF_IN)		40		µA	V_{IH} = ODVDD, equivalent to a 90 kΩ pull-up resistor
I_{IH} ($\overline{\text{RESET}}$)		13.5		µA	V_{IH} = ODVDD, equivalent to a 266 kΩ pull-up resistor
I_{IL} (SDO0, SCL, SDA)		−40		µA	V_{IL} = 0 V, equivalent to a 90 kΩ pull-down resistor
Output Voltage High (V_{OH})	2.4			V	I_{OH} = 0.4 mA
Output Voltage Low (V_{OL})			0.4	V	I_{OL} = −2 mA
Output Voltage High (V_{OH}) (MCLK_OUT)	1.4			V	I_{OH} = 0.4 mA
Output Voltage Low (V_{OL}) (MCLK_OUT)			0.4	V	I_{OL} = −3.2 mA
Input Capacitance		10		pF	
SUPPLIES					
Analog Supplies (AVDD)	3.0	3.3	3.6	V	
Digital Supplies (DVDD)	1.65	1.8	2.0	V	
Interface Supply (ODVDD)	3.0	3.3	3.6	V	
Supply Currents					MCLK = 24 MHz, ADCs and DACs active, headphone outputs active and driving a 16 Ω load
Analog Current		115		mA	
Digital Current		160		mA	
Interface Current		2		mA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Power Dissipation		0.674		W	
Standby Currents					ADC, DAC, and headphone outputs floating, $\overline{\text{RESET}}$ low, MCLK = 24 MHz
Analog Current		7		mA	
Digital Current		3		mA	
Interface Current		1.6		mA	
TEMPERATURE RANGE					
Operating Temperature	−40		+85	°C	
Storage Temperature	−65		+150	°C	

TIMING SPECIFICATIONS

Table 2.

Parameter	Description	Min	Max	Unit	Comments
MASTER CLOCK AND $\overline{\text{RESET}}$					
f_{MCLKI}	MCLKI frequency	3.072	24.576	MHz	
t_{MP}	MCLKI period	40	325	ns	
t_{MCH}	MCLKI high	10		ns	
t_{MCL}	MCLKI low	10		ns	
$t_{\overline{\text{RESET}}}$	$\overline{\text{RESET}}$ low	200		ns	
MASTER CLOCK OUTPUT					
t_{CK}	MCLK_OUT period	8	162	ns	
t_{JIT}	Period jitter		800	ps	
t_{CH}	MCLK_OUT high	45	55	%	
t_{CL}	MCLK_OUT low	45	55	%	
I^2C PORT					
f_{SCL}	SCL clock frequency		400	kHz	
t_{SCLH}	SCL high	600		ns	
t_{SCLL}	SCL low	1.3		µs	
Start Condition					
t_{SCS}	Setup time	600		ns	Relevant for repeated start condition
t_{SCH}	Hold time	600		ns	After this period, the first clock is generated
t_{DS}	Data setup time	100		ns	
t_{SCR}	SCL rise time		300	ns	
t_{SCF}	SCL fall time		300	ns	
t_{SDR}	SDA rise time		300	ns	
t_{SDF}	SDA fall time		300	ns	
Stop Condition					
t_{SCS}	Setup time	0		ns	
SERIAL PORTS					
Slave Mode					
t_{SBH}	BCLK high	40		ns	
t_{SBL}	BCLK low	40		ns	
f_{SBF}	BCLK frequency	$64 \times f_S$			
t_{SLS}	LRCLK setup	10		ns	To BCLK rising edge
t_{SLH}	LRCLK hold	10		ns	From BCLK rising edge
t_{SDS}	SDIN setup	10		ns	To BCLK rising edge
t_{SDH}	SDIN hold	10		ns	From BCLK rising edge
t_{SDD}	SDO delay		50	ns	From BCLK falling edge
Master Mode					
t_{MLD}	LRCLK delay		25	ns	From BCLK falling edge
t_{MDD}	SDO delay		15	ns	From BCLK falling edge
t_{MDS}	SDIN setup	10		ns	From BCLK rising edge
t_{MDH}	SDIN hold	10		ns	From BCLK rising edge

TIMING DIAGRAMS

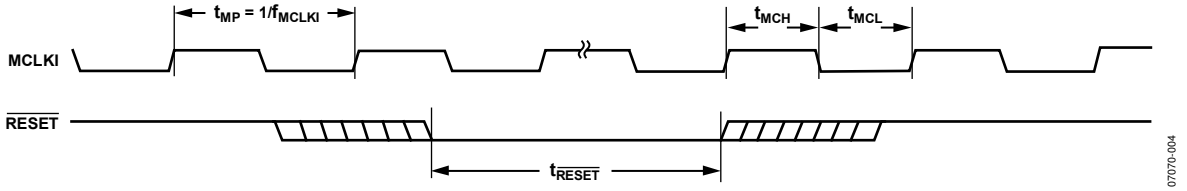

Figure 2. Master Clock and Reset Timing

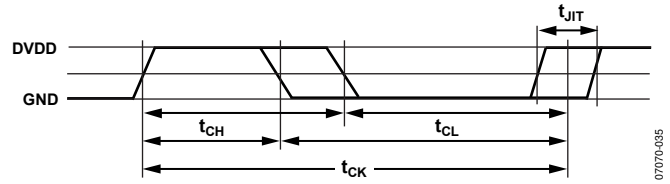

Figure 3. Master Clock Output Timing

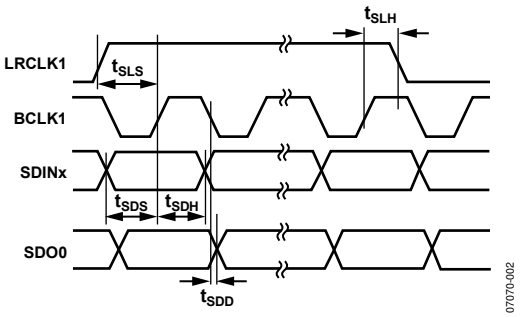

Figure 4. Serial Port Slave Mode Timing

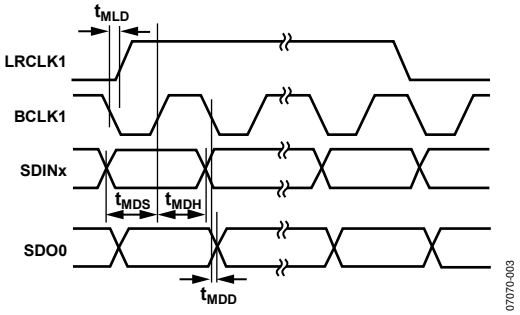

Figure 5. Serial Port Master Mode Timing

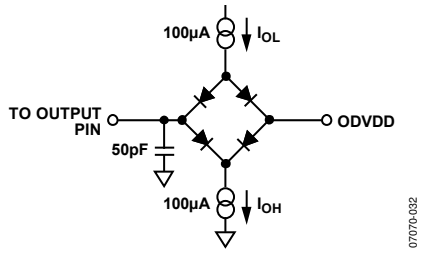

Figure 6. Load Circuit for Digital Output Timing Specifications

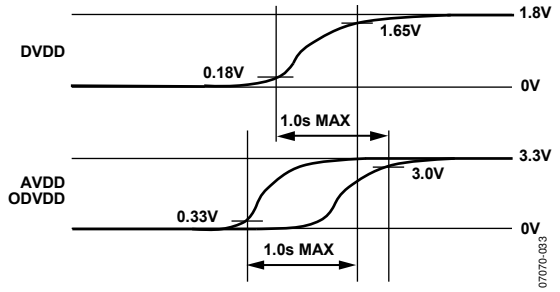

Figure 7. Power-Up Sequence Timing

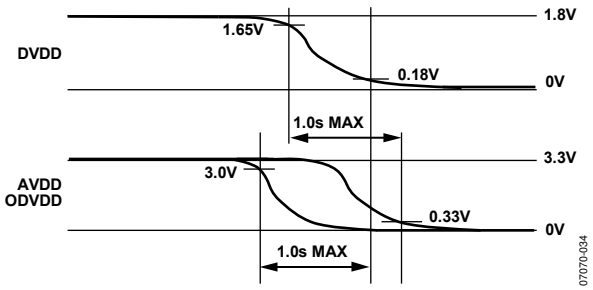

Figure 8. Power-Down Sequence Timing

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
DVDD to DGND	0 V to 2.2 V
ODVDD to DGND	0 V to 4 V
AVDD to AGND	0 V to 4 V
AGND to DGND	−0.3 V to +0.3 V
Digital Inputs	DGND − 0.3 V to ODVDD + 0.3 V
Analog Inputs	AGND − 0.3 V to AVDD + 0.3 V
Reference Voltage	Indefinite short circuit to ground
Soldering (10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. Thermal resistance is based on JEDEC 2S2P PCB.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
80-Lead LQFP	38.1	7.6	°C/W

THERMAL CONDITIONS

To ensure correct operation of the device, the case temperature (T_{CASE}) must be kept below 121°C to keep the junction temperature (T_J) below the maximum allowed, 125°C.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

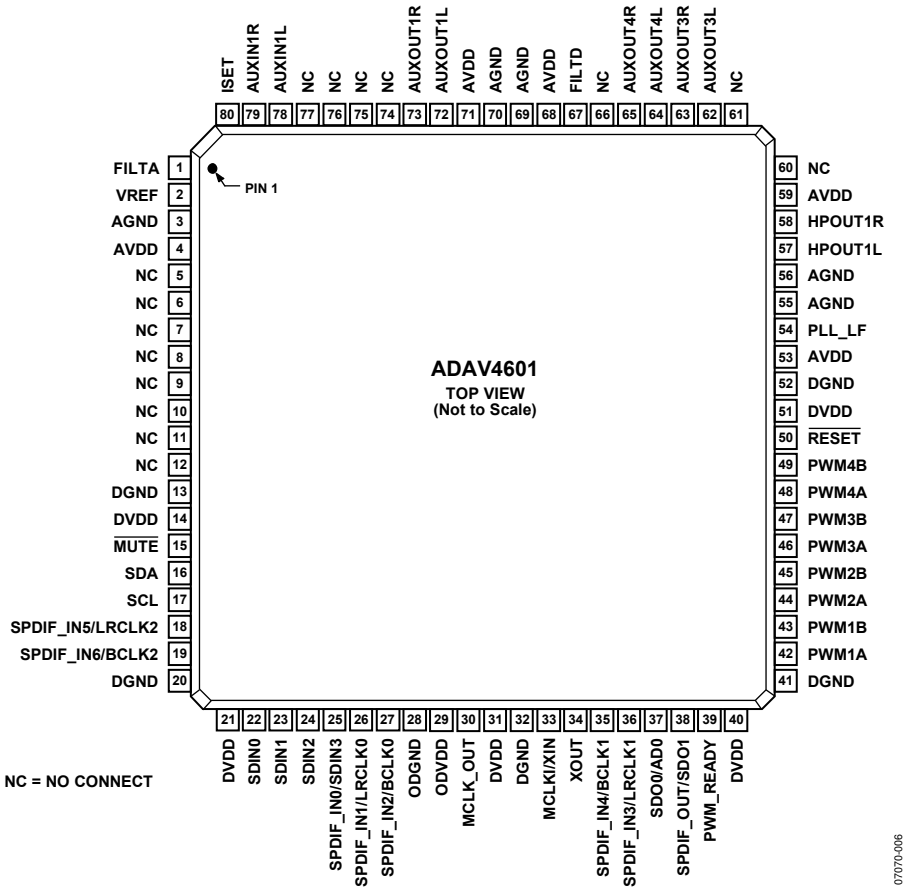

Figure 9. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FILTA	ADC Filter Capacitor.
2	VREF	Reference Capacitor.
3	AGND	ADC Ground.
4	AVDD	ADC Supply (3.3 V).
5 to 12	NC	No Connection to This Pin Allowed.
13	DGND	Digital Ground.
14	DVDD	Digital Supply (1.8 V).
15	$\overline{\text{MUTE}}$	Active-Low Mute Request Input Signal.
16	SDA	I^2C Data.
17	SCL	I^2C Clock.
18	SPDIF_IN5/LRCLK2	External Input to S/PDIF Mux/Left/Right Clock for SRC2 (Default).
19	SPDIF_IN6/BCLK2	External Input to S/PDIF Mux/Bit Clock for SRC2 (Default).
20	DGND	Digital Ground.
21	DVDD	Digital Supply (1.8 V).
22	SDIN0	Serial Data Input 0/SRC Data Input.
23	SDIN1	Serial Data Input 1/SRC Data Input.
24	SDIN2	Serial Data Input 2/SRC Data Input.

Pin No.	Mnemonic	Description
25	SPDIF_IN0/SDIN3	External Input to S/PDIF Mux/SRC Data Input/Serial Data Input 3 (Default).
26	SPDIF_IN1/LRCLK0	External Input to S/PDIF Mux/Left/Right Clock for SRC1 (Default).
27	SPDIF_IN2/BCLK0	External Input to S/PDIF Mux/Bit Clock for SRC1 (Default).
28	ODGND	Digital Ground.
29	ODVDD	Digital Interface Supply (3.3 V).
30	MCLK_OUT	Master Clock Output.
31	DVDD	Digital Supply (1.8 V).
32	DGND	Digital Ground.
33	MCLKI/XIN	Master Clock/Crystal Input.
34	XOUT	Crystal Output.
35	SPDIF_IN4/BCLK1	External Input to S/PDIF Mux/Bit Clock for Serial Data I/O (Default).
36	SPDIF_IN3/LRCLK1	External Input to S/PDIF Mux/Left/Right Clock for Serial Data I/O (Default).
37	SDO0/AD0	Serial Data Output. This pin acts as the I^2C address select on reset. It has an internal pull-down resistor.
38	SPDIF_OUT/SDO1	Output of S/PDIF Mux/Serial Data Output.
39	PWM_READY	PWM Ready Flag.
40	DVDD	Digital Supply (1.8 V).
41	DGND	Digital Ground.
42	PWM1A	Pulse-Width Modulated Output 1A.
43	PWM1B	Pulse-Width Modulated Output 1B.
44	PWM2A	Pulse-Width Modulated Output 2A.
45	PWM2B	Pulse-Width Modulated Output 2B.
46	PWM3A	Pulse-Width Modulated Output 3A.
47	PWM3B	Pulse-Width Modulated Output 3B.
48	PWM4A	Pulse-Width Modulated Output 4A.
49	PWM4B	Pulse-Width Modulated Output 4B.
50	$\overline{\text{RESET}}$	Reset Analog and Digital Cores.
51	DVDD	Digital Supply (1.8 V).
52	DGND	Digital Ground.
53	AVDD	PLL Supply (3.3 V).
54	PLL_LF	PLL Loop Filter.
55	AGND	PLL Ground.
56	AGND	Headphone Driver Ground.
57	HPOUT1L	Left Headphone Output.
58	HPOUT1R	Right Headphone Output.
59	AVDD	Headphone Driver Supply (3.3 V).
60, 61	NC	No Connection to This Pin Allowed.
62	AUXOUT3L	Left Auxiliary Output 3.
63	AUXOUT3R	Right Auxiliary Output 3.
64	AUXOUT4L	Left Auxiliary Output 4.
65	AUXOUT4R	Right Auxiliary Output 4.
66	NC	No Connection to This Pin Allowed.
67	FILTD	DAC Filter Capacitor.
68	AVDD	DAC Supply (3.3 V).
69	AGND	DAC Ground.
70	AGND	DAC Ground.
71	AVDD	DAC Supply (3.3 V).
72	AUXOUT1L	Left Auxiliary Output 1.
73	AUXOUT1R	Right Auxiliary Output 1.
74 to 77	NC	No Connection to This Pin Allowed.
78	AUXIN1L	Left Auxiliary Input 1.
79	AUXIN1R	Right Auxiliary Input 1.
80	ISET	ADC Current Setting.

TYPICAL PERFORMANCE CHARACTERISTICS

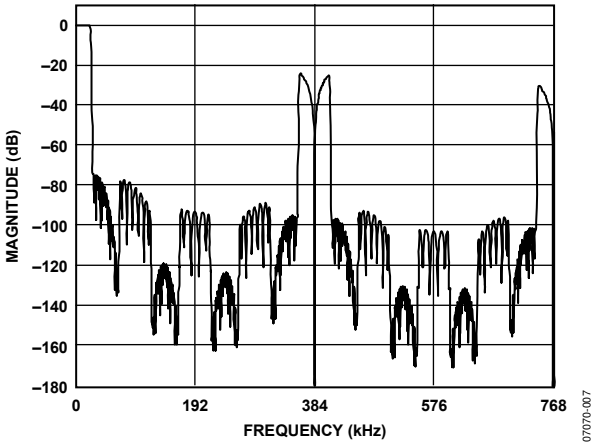

Figure 10. DAC Composite Filter Response (48 kHz)

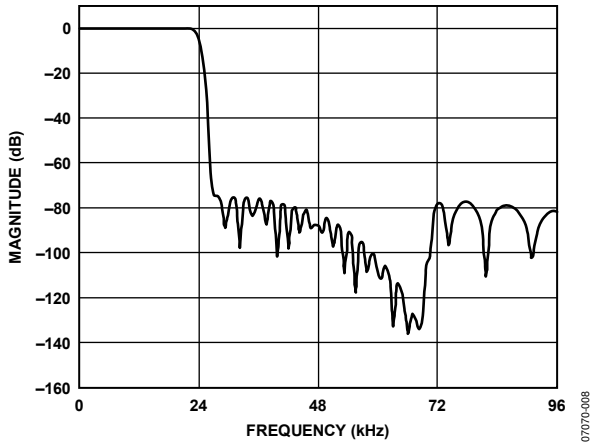

Figure 11. DAC Pass-Band Filter Response (48 kHz)

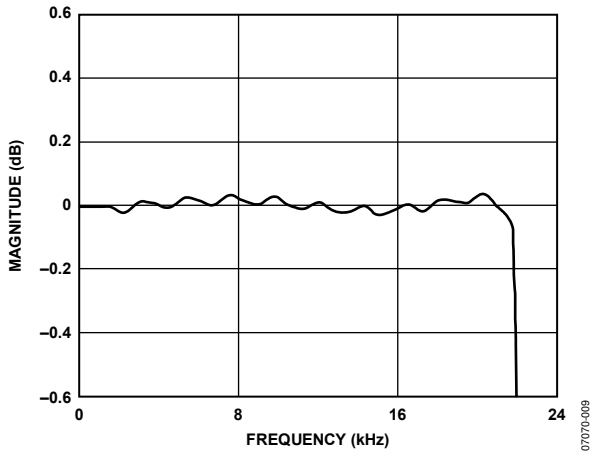

Figure 12. DAC Pass-Band Ripple (48 kHz)

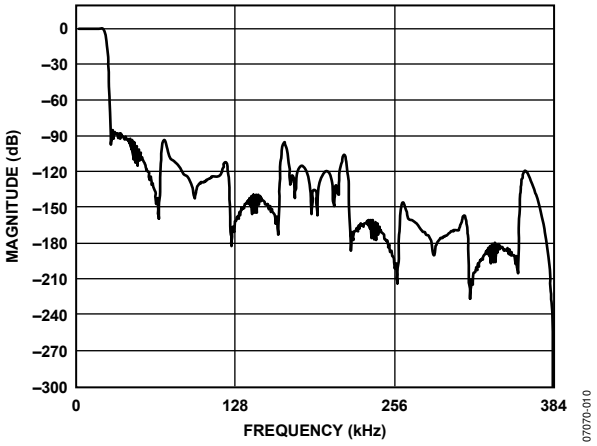

Figure 13. ADC Composite Filter Response (48 kHz)

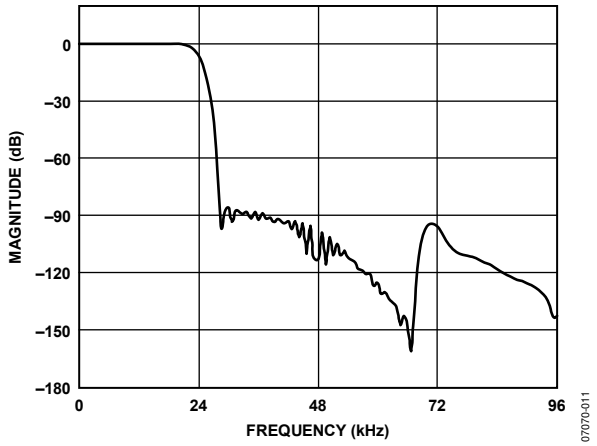

Figure 14. ADC Pass-Band Filter Response (48 kHz)

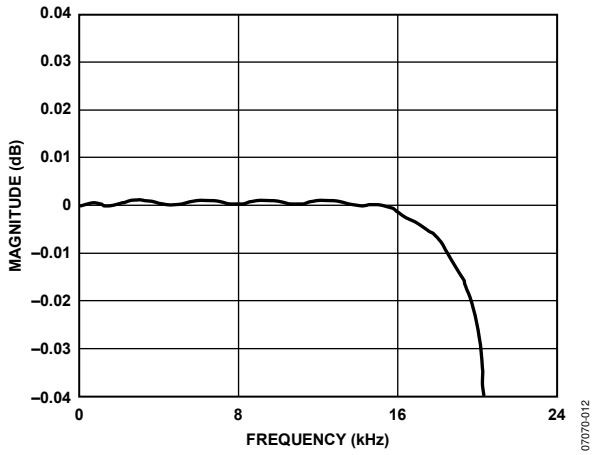

Figure 15. ADC Pass-Band Ripple (48 kHz)

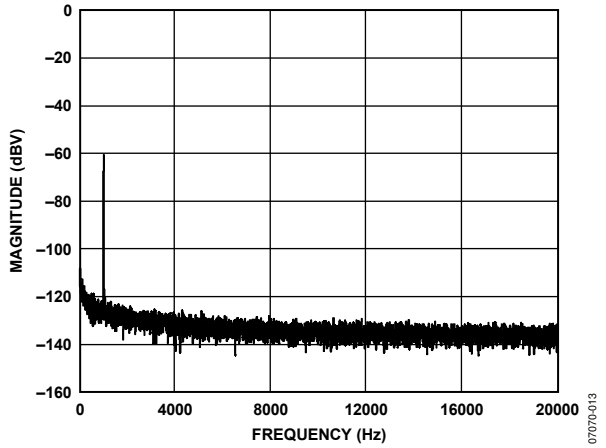

Figure 16. DAC Dynamic Range

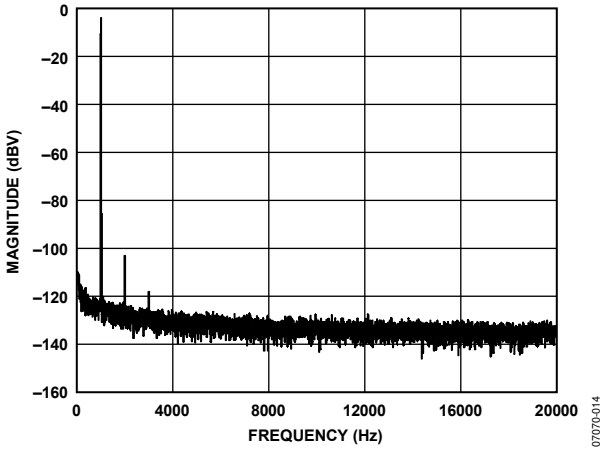

Figure 17. DAC Total Harmonic Distortion + Noise

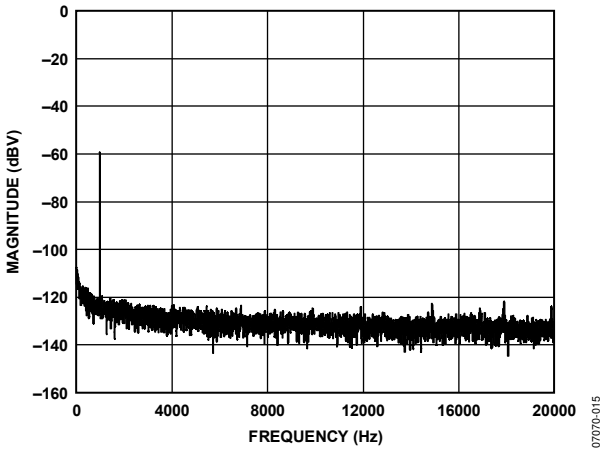

Figure 18. ADC Dynamic Range

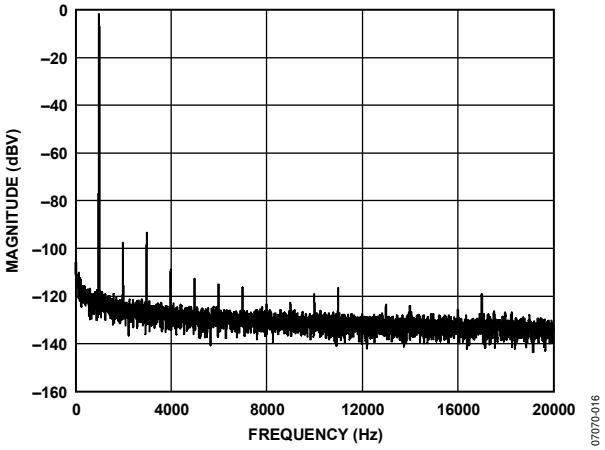

Figure 19. ADC Total Harmonic Distortion + Noise

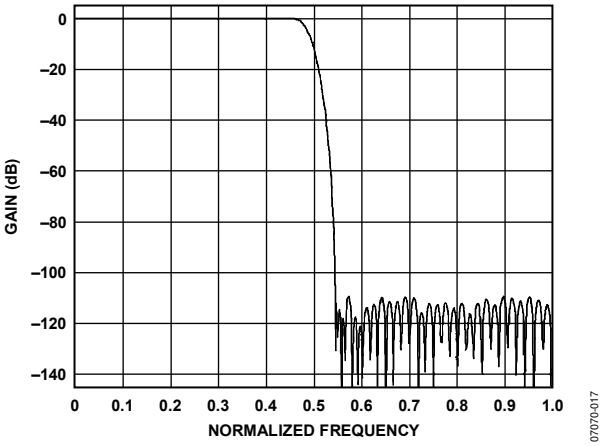

Figure 20. Sample Rate Converter Transfer Function

TERMINOLOGY

Dynamic Range
The ratio of a full-scale input signal to the integrated input noise in the pass band (20 Hz to 20 kHz), expressed in decibels (dB). Dynamic range is measured with a −60 dB input signal and is equal to (S/[THD+N]) + 60 dB. Note that spurious harmonics are below the noise with a −60 dB input; therefore, the noise level establishes the dynamic range. The dynamic range is specified with and without an A-weight filter applied.

Pass Band
The region of the frequency spectrum unaffected by the attenuation of the filter of the digital decimator.

Pass-Band Ripple
The peak-to-peak variation in amplitude response from equal amplitude input signal frequencies within the pass band, expressed in decibels.

Stop Band
The region of the frequency spectrum attenuated by the filter of the digital decimator to the degree specified by stop-band attenuation.

Gain Error
With a near full-scale input, the ratio of the actual output to the expected output, expressed in dB.

Interchannel Gain Mismatch
With identical near full-scale inputs, the ratio of the outputs of the two stereo channels, expressed in decibels.

Crosstalk
Ratio of response on one channel with a grounded input to a full-scale 1 kHz sine wave input on the other channel, expressed in decibels.

Power Supply Rejection
With no analog input, the signal present at the output when a 300 mV p-p signal is applied to power supply pins, expressed in decibels of full scale.

Group Delay
Intuitively, the time interval required for an input pulse to appear at the output of the converter, expressed in milliseconds (ms); more precisely, the derivative of radian phase with respect to radian frequency at a given frequency.

PIN FUNCTIONS

DETAILED PIN DESCRIPTIONS

Table 5 shows the pin numbers, mnemonics, and descriptions for the ADAV4601. The input pins have a logic threshold compatible with 3.3 V input levels.

SDIN0, SDIN1, SDIN2, and SDIN3/SPDIF_IN0

Serial data inputs. These input pins provide the digital audio data to the signal processing core. Any of the inputs can be routed to either of the SRCs for conversion; this input is then not available as a synchronous input to the audio processor but only as an input through the selected SRC. The serial format for the synchronous data is selected by Bits[3:2] of the Serial Port Control Register 1. If the SRCs are required, the serial format is selected by Bits[12:9] of the same register. The synchronous inputs are capable of using any pair of serial clocks, LRCLK0/BCLK0, LRCLK1/BCLK1, or LRCLK2/BCLK2. By default, they use LRCLK1 and BCLK1. See Figure 26 for more details regarding the configuration of the synchronous inputs.

SDIN3 is a shared pin with SPDIF_IN0. If SDIN3 is not in use, this pin can be used to connect an S/PDIF signal from an external source, such as an MPEG decoder, to the ADAV4601 on-chip S/PDIF output multiplexer. If SPDIF_OUT is selected from one of the SPDIF_IN (external) signals, the signal is simply passed through from input to output.

LRCLK0/SPDIF_IN1, BCLK0/SPDIF_IN2, LRCLK1/SPDIF_IN3, BCLK1/SPDIF_IN4, LRCLK2/SPDIF_IN5, and BCLK2/SPDIF_IN6

By default, LRCLK1 and BCLK1 are associated with the synchronous inputs, LRCLK0 and BCLK0 are associated with SRC1, and LRCLK2 and BCLK2 are associated with SRC2. However, the SRCs and synchronous inputs can use any of the serial clocks (see Figure 26). LRCLK0, BCLK0, LRCLK1, BCLK1, LRCLK2, and BCLK2 are shared pins with SPDIF_IN1, SPDIF_IN2, SPDIF_IN3, SPDIF_IN4, SPDIF_IN5, and SPDIF_IN6, respectively. If LRCLK0/LRCLK1/ LRCLK2 or BCLK0/BCLK1/BCLK2 are not in use, these pins can be used to connect an S/PDIF signal from an external source, such as an MPEG decoder, to the ADAV4601 on-chip S/PDIF output multiplexer. If SPDIF_OUT is selected from one of the SPDIF_IN (external) signals, the signal is simply passed through from input to output.

SDO0/AD0

Serial data output. This pin can output two channels of digital audio using a variety of standard 2-channel formats. The clocks for SDO0 are always the same as those used by the synchronous inputs; therefore, LRCLK1 and BCLK1 are used by default, although SDO0 is capable of using any pair of serial clocks, LRCLK0/BCLK0, LRCLK1/BCLK1, or LRCLK2/BCLK2. The Serial Port Control Register 1 selects the serial format for the synchronous output. On reset, the SDO0 pin duplicates as the $I^2C^®$ address select pin. In this mode, the logical state of the pin is polled for four MCLKI cycles following reset. The address select bit is set as the majority poll of the logic level of the pin after the four MCLKI cycles.

SPDIF_OUT/SDO1

The ADAV4601 contains an S/PDIF multiplexer functionality that allows the SPDIF_OUT signal to be chosen from an internally generated S/PDIF signal or from the S/PDIF signal of an external source, which is connected via one of the SPDIF_IN pins. This pin can also be configured as an additional serial output (SDO1) as an alternate function.

MCLKI/XIN

Master clock input. The ADAV4601 uses a PLL to generate the appropriate internal clock for the audio processing core. A clock signal of a suitable frequency can be connected directly to this pin, or a crystal can be connected between MCLKI/XIN and XOUT together with the appropriate capacitors to DGND to generate a suitable clock signal.

XOUT

This pin is used in conjunction with MCLKI/XIN to generate a clock signal for the ADAV4601.

MCLK_OUT

This pin can be used to output MCLKI or one of the internal system clocks. Note that the output level of this pin is referenced to DVDD (1.8 V) and not ODVDD (3.3 V) like all the other digital inputs and outputs.

SDA

Serial data input for the I^2C control port. SDA features a glitch elimination filter that removes spurious pulses that are less than 50 ns wide.

SCL

Serial clock for the I^2C control port. SCL features a glitch elimination filter that removes spurious pulses that are less than 50 ns wide.

$\overline{\text{MUTE}}$

Mute input request. This active-low input pin controls the muting of the output ports (both analog and digital) from the ADAV4601. When low, it asserts mute on the outputs that are enabled in the audio flow.

$\overline{\text{RESET}}$

Active-low reset signal. After $\overline{\text{RESET}}$ goes high, the circuit blocks are powered down. The blocks can be individually powered up with software. When the part is powered up, it takes approximately 3072 internal clocks to initialize the internal circuitry. The internal system clock is equal to MCLKI until the PLL is powered and enabled, after which the internal system clock becomes $2560 \times f_S$ (122.88 MHz). When the PLL is powered up and enabled after reset, it takes approximately 3 ms to lock. When the audio processor is enabled, it takes approximately 32,768 internal system clocks to initialize and load the default flow to the audio processor memory. The audio processor is not available during this time.

AUXIN1L AND AUXIN1R

Analog inputs to the on-chip ADCs.

AUXOUT1L, AUXOUT1R, AUXOUT3L, AUXOUT3R, AUXOUT4L, and AUXOUT4R

Auxiliary DAC analog outputs. These pins can be programmed to supply the outputs of the internal audio processing for line out or record use.

HPOUT1L and HPOUT1R

Analog outputs from the headphone amplifiers.

PLL_LF

PLL loop filter connection. A 100 nF capacitor and a 2 kΩ resistor in parallel with a 1 nF capacitor tied to AVDD are required for the PLL loop filter to operate correctly.

VREF

Voltage reference for DACs and ADCs. This pin is driven by an internal 1.5 V reference voltage.

FILTA and FILTD

Decoupling nodes for the ADC and DAC. Decoupling capacitors should be connected between these nodes and AGND, typically 47 µF in parallel with 0.1 µF and 10 µF in parallel with 0.1 µF, respectively.

PWM1A, PWM1B, PWM2A, PWM2B, PWM3A, PWM3B, PWM4A, and PWM4B

Differential pulse-width modulation outputs are suitable for driving Class-D amplifiers.

PWM_READY

This pin is set high when PWM is enabled and stable.

AVDD

Analog power supply pins. These pins should be connected to 3.3 V. Each AVDD pin should be decoupled with a 0.1 µF capacitor to AGND, as close to the pin as possible. In addition, the ADC supply (Pin 4) and the DAC supplies (Pin 68 and Pin 71) should share a 10 µF capacitor to ground. The PLL supply (Pin 53) should have an additional 1 nF and 10 µF capacitor to ground, and the headphone supply (Pin 59) should have an additional 10 µF capacitor to ground.

DVDD

Digital power supply pins. These pins should be connected to a 1.8 V digital supply. For optimal performance, each DVDD/DGND pair requires a 0.1 µF decoupling capacitor as close to the pin as possible. In addition, these 0.1 µF decoupling capacitors are in parallel with a single 10 µF capacitor.

ODVDD

Digital interface power supply pin. Connect this pin to a 3.3 V digital supply. Decouple this pin with 10 µF and 0.1 µF capacitors to DGND, as close to the pin as possible.

DGND

Digital ground.

AGND

Analog ground.

ODGND

Ground for the digital interface power supply.

ISET

ADC current setting resistor. See the ADC Inputs section for more details.

FUNCTIONAL DESCRIPTIONS

POWER-UP SEQUENCE

The following sequence provides an overview of how to initialize the IC:

1. Apply power to the ADAV4601.
2. Enable PLL via an I²C write and wait 15 ms for PLL to lock.
3. Power up via an I²C write to the global power-up bit in the initialization control register (0x0000).
4. A default flow is automatically loaded on power-up. If a user-defined flow is loaded, see the Loading a Custom Audio Processing Flow section for additional information.
5. Depending on the I/O blocks required, other steps may need to be taken; for example, headphone outputs may need to be tristated. See the ADC Inputs, DAC Voltage Outputs, PWM Outputs, Headphone Output and S/PDIF Input/Output sections that describe the I/O blocks in detail.
6. Unmute.

MASTER CLOCK OSCILLATOR

Internally, the ADAV4601 operates synchronously to the master MCLKI input. All internal system clocks are generated from this single clock input using an internal PLL. This MCLKI input can also be generated by an external crystal oscillator connected to the MCLKI/XIN pin or by using a simple crystal oscillator connected across MCLKI/XIN and XOUT. By default, the master clock frequency is 24.576 MHz; however, by using the internal dividers, an MCLKI of 12.288 MHz, 6.144 MHz, and 3.072 MHz are also supported.

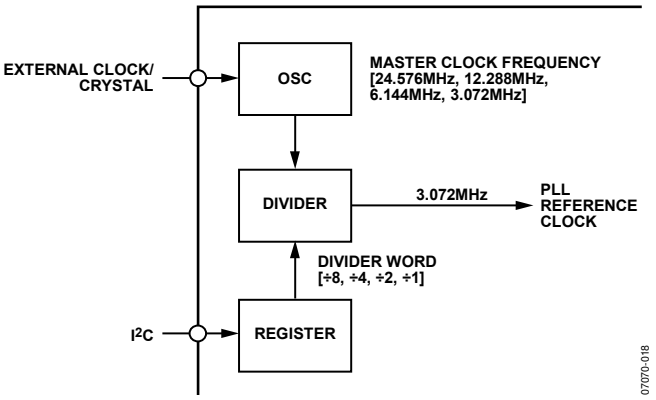

Figure 21. Master Clock

Figure 22 shows the external circuit recommended for proper operation when using a crystal oscillator. Due to the effect of stray capacitance, consideration must be given to the value of C1 and C2 when calculating the desired C_{LOAD} for the crystal.

$$C_{LOAD} = \frac{(C_{pg1} + C1)(C_{pg2} + C2)}{C_{pg1} + C1 + C_{pg2} + C2} + C_S$$

where:
C_{pg1} and C_{pg2} are the pin to ground capacitances.
C_S is the PCB stray capacitance.

A good rule of thumb is to approximate C_{pg1} and C_{pg2} to be between 5 pF and 10 pF and C_S to be between 2 pF and 3 pF.

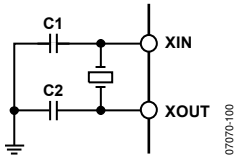

Figure 22. Circuit for Crystal Resonator

I²C INTERFACE

The ADAV4601 supports a 2-wire serial (I²C compatible) microprocessor bus driving multiple peripherals. The ADAV4601 is controlled by an external I²C master device, such as a microcontroller. The ADAV4601 is in slave mode on the I²C bus, except during self-boot. While the ADAV4601 is self-booting, it becomes the master, and the EEPROM, which contains the ROMs to be booted, is the slave. When the self-boot process is complete, the ADAV4601 reverts to slave mode on the I²C bus. No other devices should access the I²C bus while the ADAV4601 is self-booting (refer to the Application Layer section and the Loading a Custom Audio Processing Flow section).

Initially, all devices on the I²C bus are in an idle state, wherein the devices monitor the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream follows. All devices on the bus respond to the start condition and read the next byte (7-bit address plus the R/$\overline{W}$ bit) MSB first. The device that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This ninth bit is known as an acknowledge bit.

All other devices on the bus revert to an idle condition. The R/$\overline{W}$ bit determines the direction of the data. A Logic Level 0 on the LSB of the first byte means the master writes information to the peripheral. A Logic Level 1 on the LSB of the first byte means the master reads information from the peripheral. A data transfer takes place until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high.

The ADAV4601 determines its I²C device address by sampling the SDO0 pin after reset. Internally, the SDO0 pin is sampled by four MCLKI edges to determine the state of the pin (high or low). Because the pin has an internal pull-down resistor default, the address of the ADAV4601 is 0x34 (write) and 0x35 (read). An alternate address, 0x36 (write) and 0x37 (read), is available by tying the SDO0 pin to ODVDD via a 10 kΩ resistor. The I²C interface supports a clock frequency of up to 400 kHz.

Table 6. Single Word I²C Write[1]

S	Chip address, R/$\overline{W}$ = 0	AS	Subaddress high	AS	Subaddress low	AS	Data Byte 1	AS	Data Byte 2	…	AS	Data Byte N	P

[1] S = start bit, P = stop bit, and AS = acknowledge by slave.

Table 7. Burst Mode I²C Write[1]

S	Chip address, R/$\overline{W}$ = 0	AS	Subaddress high	AS	Subaddress low	AS	Data-Word 1, Byte 1	AS	Data-Word 1, Byte 2	AS	Data-Word 2, Byte 1	AS	Data-Word 2, Byte 2	AS	…	P

[1] S = start bit, P = stop bit, and AS = acknowledge by slave.

Table 8. Single Word I²C Read[1]

S	Chip address, R/$\overline{W}$ = 0	AS	Subaddress high	AS	Subaddress low	AS	S	Chip address, R/$\overline{W}$ = 1	AS	Data Byte 1	AM	Data Byte 2	…	AM	Data Byte N	P

[1] S = start bit, P = stop bit, AM = acknowledge by master, and AS = acknowledge by slave.

Table 9. Burst Mode I²C Read[1]

S	Chip address, R/$\overline{W}$ = 0	AS	Subaddress high	AS	Subaddress low	AS	S	Chip address, R/$\overline{W}$ = 1	AS	Data-Word 1 Byte 1	AM	Data-Word 1 Byte 2	AM	…	P	

[1] S = start bit, P = stop bit, AM = acknowledge by master, and AS = acknowledge by slave.

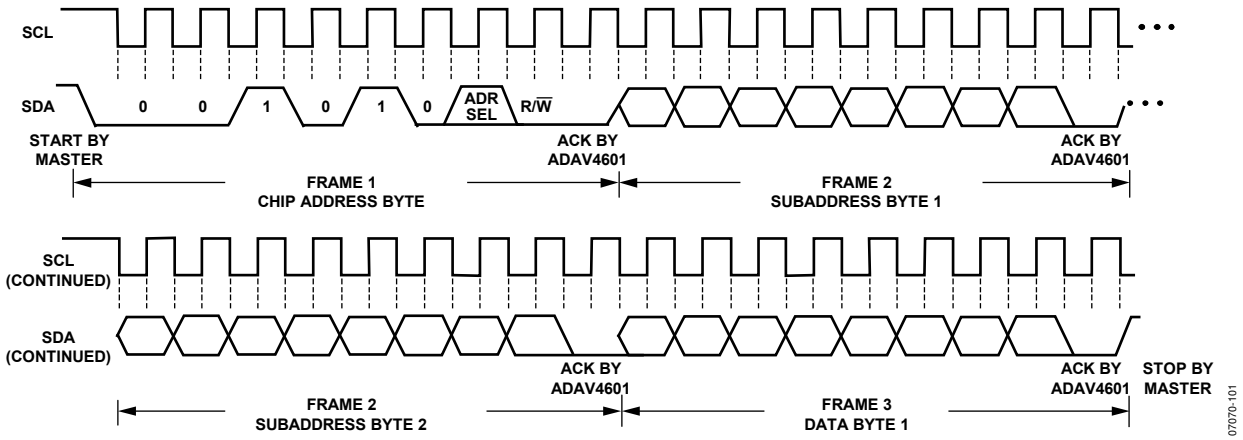

Figure 23. I²C Write Format

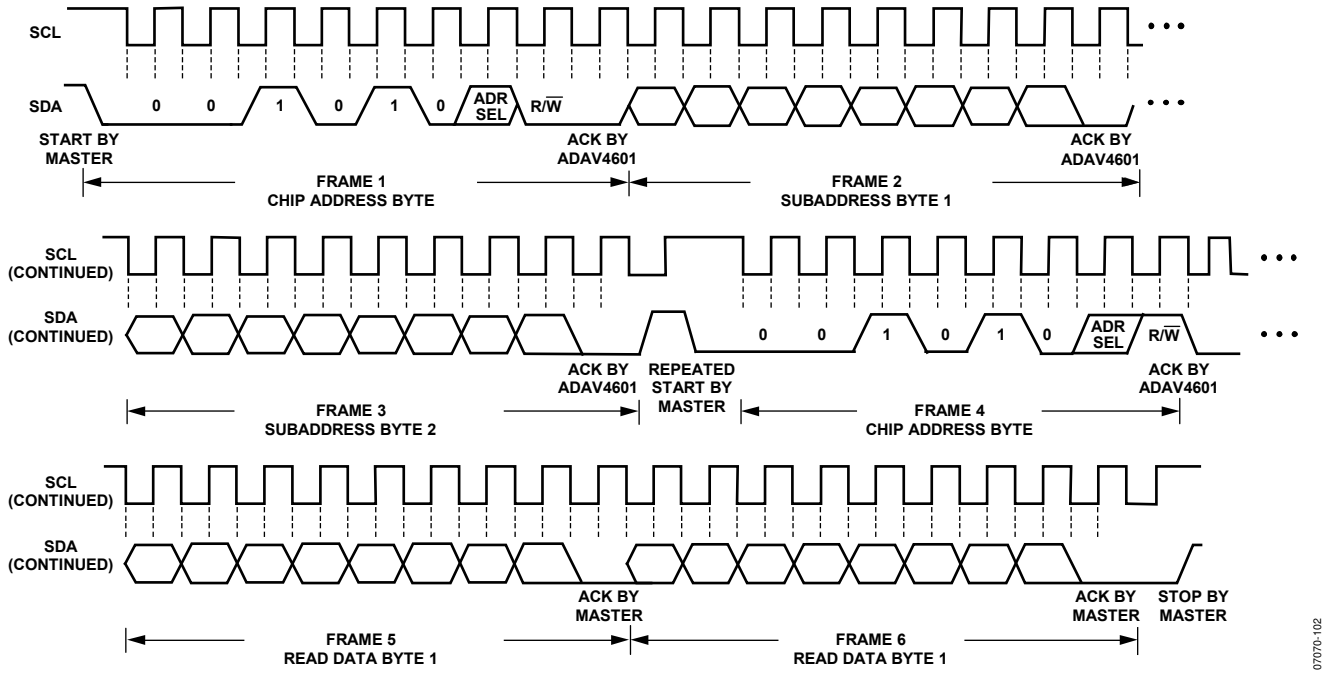

Figure 24. I²C Read Format

I²C READ AND WRITE OPERATIONS

Table 6 shows the timing of a single word write operation. Every ninth clock, the ADAV4601 issues an acknowledge by pulling SDA low.

Table 7 shows the timing of the burst mode write sequence. Table 7 shows an example where the target destination registers are two bytes. The ADAV4601 auto-increments its subaddress register counter every two bytes until a stop condition occurs.

The timing of a single word read operation is shown in Table 8. Note that the first R/$\overline{W}$ bit is still 0, indicating a write operation. This is because the subaddress must be written to set up the internal address. After the ADAV4601 acknowledges the receipt of the subaddress, the master must issue a repeated start command followed by the chip address byte with the R/$\overline{W}$ set to 1 (read). The ADAV4601 responds with the read result on SDA. The master then responds every ninth clock with an acknowledge pulse to the ADAV4601.

Table 9 shows the timing of the burst mode read sequence. Table 9 shows an example where the target read registers are two bytes. The ADAV4601 increments its subaddress register every two bytes because the requested subaddress corresponds to a register or memory area with word lengths of two bytes. Other address ranges may have a variety of word lengths ranging from one to six bytes; the ADAV4601 always decodes the subaddress and sets the auto-increment circuit so that the address increments after the appropriate number of bytes.

ADC INPUTS

The ADAV4601 has two ADC inputs. By default, this is configured as a single stereo input; however, because the audio processor is programmable, these inputs can be reconfigured.

The ADC inputs are shown in Figure 25. The analog inputs are current inputs (100 μA rms FS) with a 1.5 V dc bias voltage. Any input voltage can be accommodated by choosing a suitable combination of input resistor (R_{IN}) and ISET resistor (R_{ISET}) using the formulas

$$R_{IN} = V_{FS\ rms}/100\ \mu A\ rms$$

$$R_{ISET} = 2R_{IN}/V_{IN}$$

Resistor matching (typically 1%) between R_{IN} and R_{ISET} is important to ensure a full-scale signal on the ADC without clipping. A 10 μF dc blocking capacitor is also required at the input.

After reset, the ADCs are in a power-down state. The ADCs can be powered up using the global power-up in the initialization control register (0x0000). In power critical applications, it is possible to use the analog power management register (0x0005) to power-up or power-down individual ADCs.

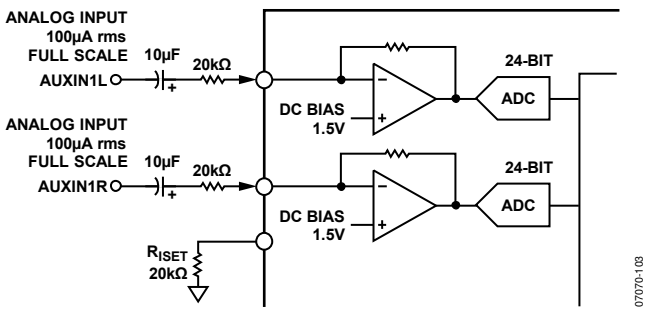

Figure 25. Analog Input Section

I²S DIGITAL AUDIO INPUTS

The ADAV4601 has four I²S digital audio inputs that are, by default, synchronous to the master clock. Also available are two SRCs capable of supporting any nonsynchronous input with a sample rate between 5 kHz and 50 kHz. Any of the serial digital inputs can be redirected through the SRC. Figure 26 shows a block diagram of the input serial port.

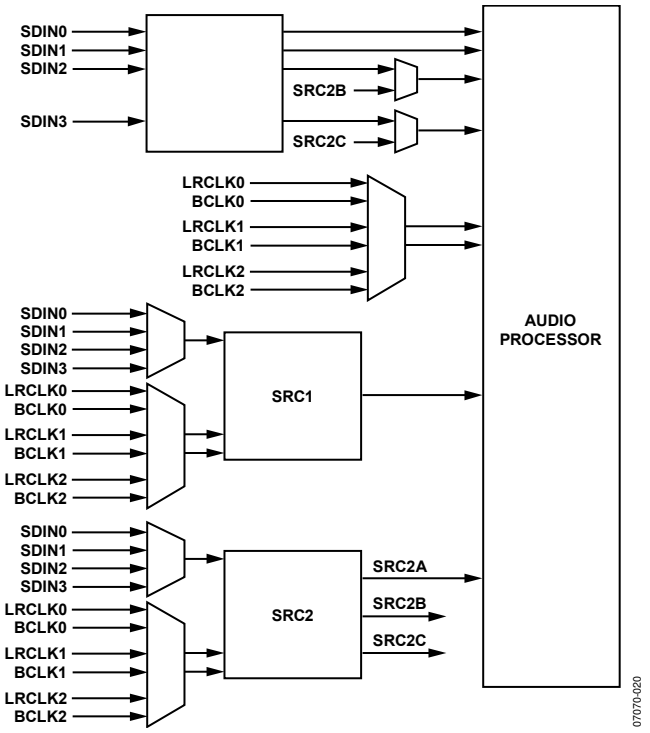

Figure 26. Digital Input Section

Synchronous Inputs and Outputs

The synchronous digital inputs and outputs can use any of the BCLK or LRCLK inputs as a clock and framing signal. By default, BCLK1 and LRCLK1 are the serial clocks used for the synchronous inputs. The synchronous port for the ADAV4601 is in slave mode by default, which means the user must supply the appropriate serial clocks, BCLK and LRCLK. The synchronous port can also be set to master mode, which means that the appropriate serial clocks, BCLK and LRCLK, can be generated internally from the MCLK; therefore, the user does not need to provide them. The serial data inputs are capable of accepting all of the popular audio transmission standards (see the Serial Data Interface section for more details).

Asynchronous Inputs

The ADAV4601 has two SRCs, SRC1 and SRC2, that can be used for converting digital data, which is not synchronous to the master clock. Each SRC can accept input sample rates in the range of 5 kHz to 50 kHz. Data that has been converted by the SRC is input to the part and is then synchronous to the internal audio processor.

The SRC1 is a 2-channel (single-stereo) sample rate converter that is capable of using any of the three serial clocks available. The SRC1 can accept data from any of the serial data inputs (SDIN0, SDIN1, SDIN2, and SDIN3). When selected as an input to the SRC, this SDIN line is assumed to contain asynchronous data and is then masked as an input to the audio processor to ensure that asynchronous data is not processed as synchronous data. By default, SRC1 uses the LRCLK0 and BCLK0 as the clock and framing signals.

The SRC2 is a 6-channel (3-stereo) sample rate converter that is capable of using any of the three serial clocks available. The SRC2 can accept data from any of the serial data inputs (SDIN0, SDIN1, SDIN2, and SDIN3). When selected as an input to the SRC, this SDIN line is assumed to contain asynchronous data and is then masked internally as an input to the audio processor to ensure that asynchronous data is not processed as synchronous data. By default, SRC2 uses the LRCLK2 and BCLK2 as the clock and framing signals.

The first output (SRC2A) from SRC2 is always available to the audio processor. The other two outputs are muxed with two of the serial inputs before being available to the audio processor. SRC2B is muxed with SDIN2, and SRC2C is muxed with SDIN3. By default, these muxes are configured so that the synchronous inputs are available to the audio processor. The SRC2B and SRC2C channels can be made available to the audio processor simply by enabling them by register write.

When using the ADAV4601 in an asynchronous digital-in-to-digital-out configuration, the input digital data is input to the audio processor core from one of the SRCs, using the assigned BCLK/LRCLK as a framing signal. The digital output is synchronous to the BCLK/LRCLK, which is assigned to the synchronous port; the default clock in this case is BCLK1 and LRCLK1.

Serial Data Interface

LRCLK is the framing signal for the left- and right-channel inputs, with a frequency equal to the sampling frequency (f_S).

BCLK is the bit clock for the digital interface, with a frequency of $64 \times f_S$ (32 BCLK periods for each of the left and right channels).

The serial data interface supports all the popular audio interface standards, such as I²S, left-justified (LJ), and right-justified (RJ). The interface mode is software selectable, and its default is I²S. The data sample width is also software selectable from 16 bits, 20 bits, or 24 bits. The default is 24 bits.

I²S Mode

In I²S mode, the data is left-justified, MSB first, with the MSB placed in the second BCLK period following the transition of the LRCLK. A high-to-low transition of the LRCLK signifies the beginning of the left channel data transfer, and a low-to-high transition on the LRCLK signifies the beginning of the right channel data transfer (see Figure 27).

Left-Justified (LJ) Mode

In LJ mode, the data is left-justified, MSB first, with the MSB placed in the first BCLK period following the transition of the LRCLK. A high-to-low transition of the LRCLK signifies the beginning of the right-channel data transfer, and a low-to-high transition on the LRCLK signifies the beginning of the left-channel data transfer (see Figure 28).

Right-Justified (RJ) Mode

In RJ mode, the data is right-justified, LSB last, with the LSB placed in the last BCLK period preceding the transition of LRCLK. A high-to-low transition of the LRCLK signifies the beginning of the right-channel data transfer, and a low-to-high transition on the LRCLK signifies the beginning of the left-channel data transfer (see Figure 29).

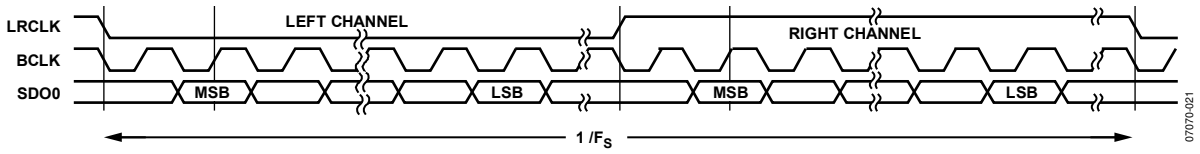

Figure 27. I²S Mode

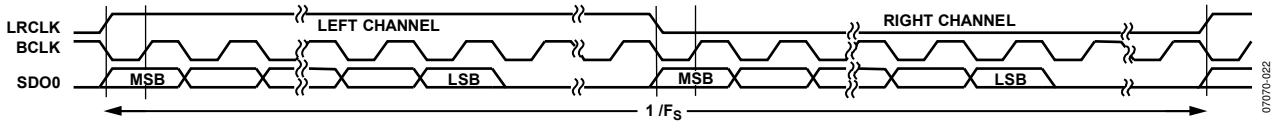

Figure 28. Left-Justified Mode

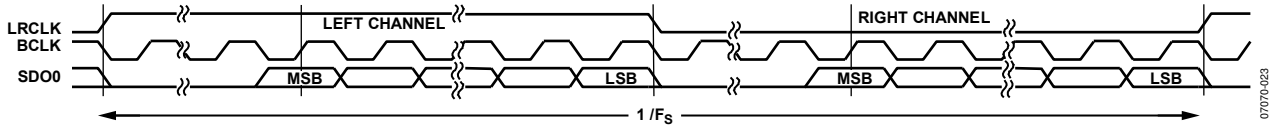

Figure 29. Right-Justified Mode

DAC VOLTAGE OUTPUTS

The ADAV4601 has six DAC outputs, configured as 3-stereo auxiliary DAC outputs. However, because the flow is customizable, it is programmable. The output level is 1 V rms full scale. The DAC outputs should have a 10 nF capacitor to ground for filtering out high frequency noise. Following the filtering capacitor, a 10 µF is required for dc blocking.

After reset, the DACs are in a power-down state. They can power up quickly using the global power-up in the initialization control register (0x0000). A popless and clickless power-up and power-down are also possible.

In power critical applications, it is possible to use the Analog Power Management 1 register (0x0005) to power up or power down individual DACs.

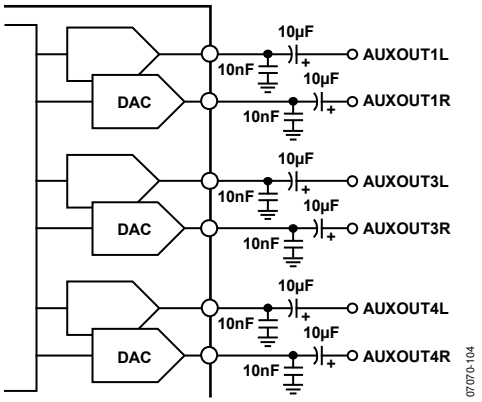

Figure 30. DAC Output Section

PWM OUTPUTS

In the ADAV4601, the main outputs are available as four PWM output channels, which are suitable for driving Class-D amplifiers.

After reset, the PWM channels are in a power-down state. Writing to the miscellaneous control register (0x000A) enables the PWM channels. To help ensure popless and clickless power-up and power-down, there is an enable/disable pattern that is specially constructed to bring the PWM channels from a zero condition to a 50/50 duty-cycle square wave (effectively, a zero signal into the PWM block). This takes 365 ms to complete and can be seen in Figure 33.

Designed for use in conjunction with this ramp-up scheme, the ADAV4601 features a status pin, PWM_READY, that indicates when the PWM outputs are in a state that can cause pops/clicks, such as power-up and power-down. During PWM power-up and power-down, this pin remains low to signify that the outputs are not in a valid state. This functionality helps to eliminate pop/click and other unwanted noise on the outputs.

To accommodate different power stages, the point at which the PWM_READY signal goes high is programmable. It can go high when the PWM outputs begin their ramp-up scheme (PWM_READY early), or it can be programmed to go high when this ramp-up scheme is complete (PWM_READY late). This is shown in Figure 33, and it is configured in the PWM control register (0x001F).

Each set of PWM outputs comprises complementary outputs. The modulation frequency is 384 kHz, and the full-scale duty cycle has a ratio of 97:3.

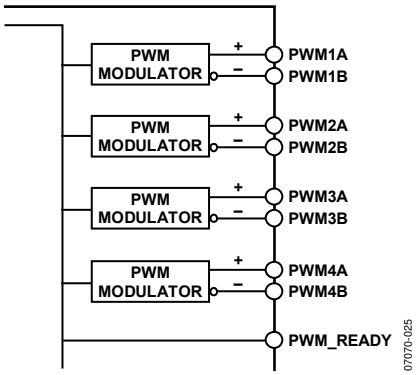

Figure 31. PWM Output Section

HEADPHONE OUTPUT

There is a dedicated stereo headphone amplifier output that is capable of driving 32 Ω loads at 1 V rms.

After reset, the headphone output is tristated. The tristate is disabled using the headphone control register (0x000B). Using the same register, the gain of the headphone amplifier can be set in +1.5 dB steps from +1.5 dB to −45 dB. The headphone output should have a 10 µF capacitor for dc blocking.

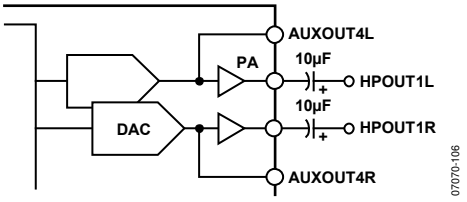

Figure 32. Headphone Output Section

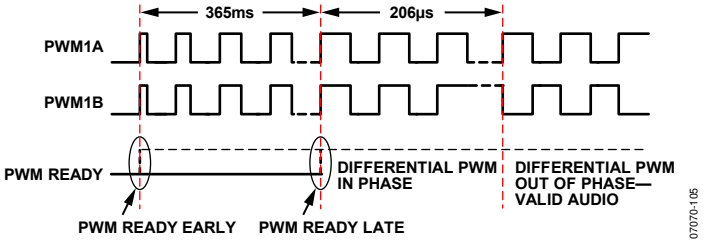

Figure 33. PWM Early

I²S DIGITAL AUDIO OUTPUTS

One I²S output, SDO0, uses the same serial clocks as the serial inputs, which are BCLK1 and LRCLK1 by default. If an additional digital output is required, an additional pin can be reconfigured as a serial digital output, as shown in Figure 34.

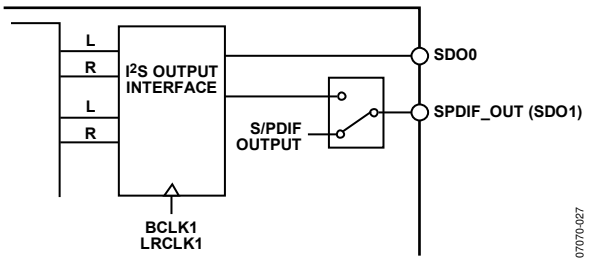

Figure 34. I²S Digital Outputs

S/PDIF INPUT/OUTPUT

The S/PDIF output (SPDIF_OUT/SDO1) uses a multiplexer to select an output from the audio processor or to pass through the unprocessed SPDIF_IN signals, as shown in Figure 35. On the ADAV4601, the S/PDIF inputs, SPDIF_IN0/SPDIF_IN1/SPDIF_IN2/SPDIF_IN3/SPDIF_IN4/SPDIF_IN5/SPDIF_IN6, are available on the SDIN3, LRCLK0, BCLK0, LRCLK1, BCLK1, LRCLK2, and BCLK2 pins, respectively. It is possible to have all seven S/PDIF inputs connected to different S/PDIF signals at one time. A consequence of this setup is that none of the LRCLKs and BCLKs are available for use with the digital inputs SDIN0, SDIN1, SDIN2, and SDIN3. If there is only one S/PDIF input in use, using the SDIN3 pin as the dedicated S/PDIF input is recommended; this enables BCLK0/LRCLK0, BCLK1/LRCLK1, and BCLK2/LRCLK2 to be used as the clock and framing signals for the synchronous and asynchronous port. If SDIN3 is used as an S/PDIF input, it should not be used internally as an input to the audio processor because it contains invalid data. Similarly, if BCLK or LRCLK is used as the S/PDIF input, they can no longer be used as the lock and framing signals for SDIN0, SDIN1, SDIN2, and SDIN3. The S/PDIF encoder supports only consumer formats that conform to IEC-600958.

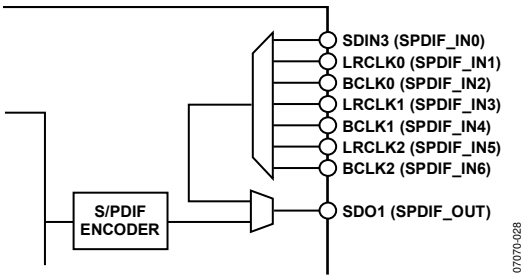

Figure 35. S/PDIF Output

HARDWARE MUTE CONTROL

The ADAV4601 mute input can be used to mute any of the analog or digital outputs. When the $\overline{\text{MUTE}}$ pin goes low, the selected outputs ramp to a muted condition. Unmuting is handled in one of two ways and depends on the register setting. By default, the $\overline{\text{MUTE}}$ pin going high causes the outputs to immediately ramp to an unmuted state. However, it is also possible to have the unmute operation controlled by a control register bit. In this scenario, even if the $\overline{\text{MUTE}}$ pin goes high, the device does not unmute until a bit in the control register is set. This can be used when the user wants to keep the outputs muted, even after the pin has gone high again, for example, in the case of a fault condition. This allows the system controller total control over the unmute operation.

AUDIO PROCESSOR

The internal audio processor runs at 2560 × f_S; at 48 kHz, this is 122.88 MHz. Internally, the word size is 28 bits, which allows 24 dB of headroom for internal processing. Designed specifically with audio processing in mind, it can implement complex audio algorithms efficiently.

By default, the ADAV4601 loads a default audio flow, as shown in Figure 48. However, because the audio processor is fully programmable, a custom audio flow can be quickly developed and loaded to the audio processor.

The audio flow is contained in program RAM and parameter RAM. Program RAM contains the instructions to be processed by the audio processor, and parameter RAM contains the coefficients that control the flow, such as volume control, filter coefficients, and enable bits.

GRAPHICAL PROGRAMMING ENVIRONMENT

Custom flows for the ADAV4601 are created in a powerful drag-and-drop graphical programming application called SigmaStudio. No knowledge of assembly code is required to program the ADAV4601. Featuring a comprehensive library of audio processing blocks (such as filters, delays, dynamics processors, and third-party algorithms), sigma studio allows a quick and simple creation of custom flows. For debugging purposes, run-time control of the audio flow allows the user to fully configure and test the created flow.

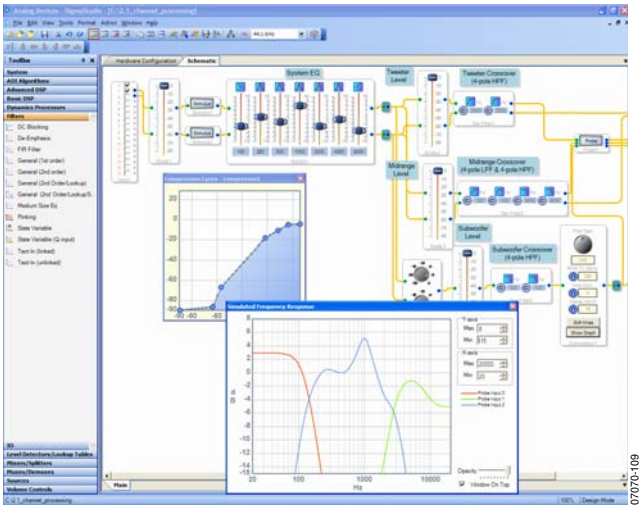

Figure 36. SigmaStudio Window

SIGMASTUDIO PIN ASSIGNMENT

Inputs and outputs are defined as numbers in SigmaStudio. Each number corresponds to a physical input or output on the ADAV4601. Table 10 and Table 11 show these relationships.

Table 10. Input Channels

SigmaStudio Input	Pin Name
0	SDINL0
1	SDINR0
2	SDINL1
3	SDINR1
4	SDINL2/SRC2BL
5	SDINR2/SRC2BR
6	SDINL3/SRC2CL
7	SDINR3/SRC2CR
8	AUXIN1L
9	AUXIN1R
10, 11	No connect
12	SRC1L
13	SRC1R
14	SRC2AL
15	SRC2AR
16, 17	No connect

Table 11. Output Channels

Sigma Studio Output	Pin Name
0	SDOL0
1	SDOR0
2 to 7	No connect
8	PWM1/AUXOUT3L
9	PWM2/AUXOUT3R
10	AUXOUT4L/Headphone 1L
11	AUXOUT4R/Headphone 1R
12	AUXOUT1L
13	AUXOUT1R
14	PWM3
15	PWM4
16 to 19	No connect
20	SPDIF OUTL
21	SPDIF OUTR

APPLICATION LAYER

Unique to the ADAV46xx family is the embedded application layer, which allows the user to define a custom set of registers to control the audio flow, greatly simplifying the interface between the audio processor and the system controller. This allows the ADAV4601 to appear as a simple fixed function register-based device to the system controller.

When a custom flow is created, a user-customized register map can be defined for controlling the flow. Each register is 16 bits, but controls can use only one bit or all 16 bits. Users have full control over which parameters they use and the degree of control they have over those parameters during run time. The combination of the graphical programming environment and the powerful application layer allows the user to quickly develop a custom audio flow and still maintain the usability of a simple register-based device.

LOADING A CUSTOM AUDIO PROCESSING FLOW

The ADAV4601 can load a custom audio flow from an external I²C ROM. The boot process is initiated by a simple control register write. The EEPROM device address and the EEPROM start address for the audio flow ROMs can all be programmed.

For the duration of the boot sequence, the ADAV4601 becomes the master on the I²C bus. Transfer of the ROMs from the EEPROM to the ADAV4601 takes a maximum of 1.06 sec, assuming that the full audio processor memory is required, during which time no other devices should access the I²C bus. When the transfer is complete, the ADAV4601 automatically reverts to slave mode, and the I²C bus master can resume sending commands.

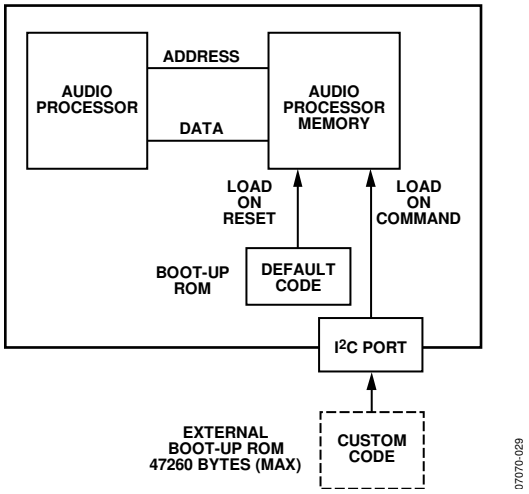

Figure 37. External EEPROM Booting

NUMERIC FORMATS

It is common in DSP systems to use a standardized method of specifying numeric formats. Fractional number systems are specified by an A.B format, where A is the number of bits to the left of the decimal point and B is the number of bits to the right of the decimal point.

The ADAV4601 uses the same numeric format for both the coefficient values (stored in the parameter RAM) and the signal data values.

Numeric Format: 5.23

It ranges from −16.0 to (+16.0 − 1 LSB).