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Audio Codec for Recordable DVD

ADAV801

FEATURES

- **Stereo analog-to-digital converter (ADC)**
  - **Supports 48 kHz/96 kHz sample rates**
  - **102 dB dynamic range**
  - **Single-ended input**
  - **Automatic level control**
- **Stereo digital-to-analog converter (DAC)**
  - **Supports 32 kHz/44.1 kHz/48 kHz/96 kHz/192 kHz sample rates**
  - **101 dB dynamic range**
  - **Single-ended output**
- **Asynchronous operation of ADC and DAC**
- **Stereo sample rate converter (SRC)**
  - **Input/output range: 8 kHz to 192 kHz**
  - **140 dB dynamic range**
- **Digital interfaces**
  - **Record**
  - **Playback**
  - **Auxiliary record**
  - **Auxiliary playback**
- **S/PDIF (IEC 60958) input and output**
  - **Digital interface receiver (DIR)**
  - **Digital interface transmitter (DIT)**
- **PLL-based audio MCLK generators**
- **Generates required DVDR system MCLKs**
- **Device control via SPI-compatible serial port**
- **64-lead LQFP package**

FUNCTIONAL BLOCK DIAGRAM

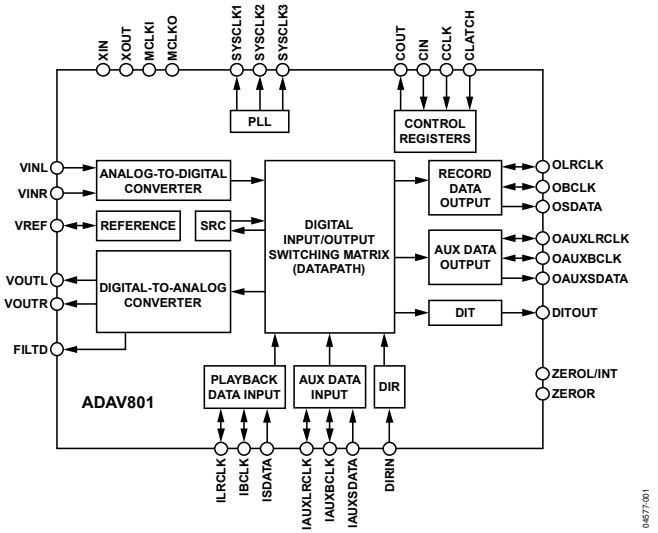

Figure 1.

APPLICATIONS

DVD-recordable
All formats
CD-R/W

GENERAL DESCRIPTION

The ADAV801 is a stereo audio codec intended for applications such as DVD or CD recorders that require high performance and flexible, cost-effective playback and record functionality. The ADAV801 features Analog Devices, Inc. proprietary, high performance converter cores to provide record (ADC), playback (DAC), and format conversion (SRC) on a single chip. The ADAV801 record channel features variable input gain to allow for adjustment of recorded input levels and automatic level control, followed by a high performance stereo ADC whose digital output is sent to the record interface. The record channel also features level detectors that can be used in feedback loops to adjust input levels for optimum recording. The playback channel features a high performance stereo DAC with independent digital volume control.

The sample rate converter (SRC) provides high performance sample rate conversion to allow inputs and outputs that require different sample rates to be matched. The SRC input can be selected from playback, auxiliary, DIR, or ADC (record). The SRC output can be applied to the playback DAC, both main and auxiliary record channels, and a DIT.

Operation of the ADAV801 is controlled via an SPI-compatible serial interface, which allows the programming of individual control register settings. The ADAV801 operates from a single analog 3.3 V power supply and a digital power supply of 3.3 V with an optional digital interface range of 3.0 V to 3.6 V.

The part is housed in a 64-lead LQFP package and is characterized for operation over the commercial temperature range of −40°C to +85°C.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

ADAV801* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADAV801 Evaluation Board

DOCUMENTATION

Application Notes

- AN-910: Recovering the DIR PLL Operation on the ADAV801 and ADAV803

Data Sheet

- ADAV801: Audio Codec for Recordable DVD Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADAV80X Sound CODEC Linux Driver

REFERENCE DESIGNS

- CN0219

REFERENCE MATERIALS

Technical Articles

- Benchmarking Integrated Audio: Why CPU Usage Alone No Longer Predicts User Experience

DESIGN RESOURCES

- ADAV801 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADAV801 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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TABLE OF CONTENTS

REVISION HISTORY

7/07—Rev. 0 to Rev. A

Changes to Table 1 ... 3
Changes to ADC Section ... 15
Changes to Figure 25 ... 15
Changes to Figure 33 ... 21
Changes to SRC Architecture Section ... 21
Changes to Table 7 ... 22
Changes to Figure 36 ... 22
Changes to Figure 39 and Figure 42 ... 23
Changes to Transmitter Operation Section ... 27
Changes to Interrupts Section ... 27
Changes to Figure 50 ... 28
Changes to Table 97 ... 46
Changes to Table 101 ... 47
Changes to Table 136 and Table 137 ... 55
Updated Outline Dimensions ... 59
Changes to Ordering Guide ... 59

7/04—Revision 0: Initial Version

SPECIFICATIONS

TEST CONDITIONS

Test conditions, unless otherwise noted.

Table 1.

Test Parameter	Condition
Supply Voltage	
Analog	3.3 V
Digital	3.3 V
Ambient Temperature	25°C
Master Clock (MCLKI)	12.288 MHz
Measurement Bandwidth	20 Hz to 20 kHz
Word Width (All Converters)	24 bits
Load Capacitance on Digital Outputs	100 pF
ADC Input Frequency	1007.8125 Hz at −1 dBFS
DAC Output Frequency	960.9673 Hz at 0 dBFS
Digital Input	Slave mode, I^2S justified format
Digital Output	Slave mode, I^2S justified format

ADAV801 SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Comments
PGA SECTION					
Input Impedance		4		kΩ	
Minimum Gain		0		dB	
Maximum Gain		24		dB	
Gain Step		0.5		dB	
REFERENCE SECTION					
Absolute Voltage, V_{REF}		1.5		V	
V_{REF} Temperature Coefficient		80		ppm/°C	
ADC SECTION					
Number of Channels		2			
Resolution		24		Bits	
Dynamic Range					−60 dB input
Unweighted		99		dB	f_S = 48 kHz
		98		dB	f_S = 96 kHz
A-Weighted	98	102		dB	f_S = 48 kHz
		101		dB	f_S = 96 kHz
Total Harmonic Distortion + Noise					Input = −1.0 dBFS
		−88		dB	f_S = 48 kHz
		−87		dB	f_S = 96 kHz
Analog Input					
Input Range (± Full Scale)		1.0		V rms	
DC Accuracy					
Gain Error	−1.5	−0.8		dB	
Interchannel Gain Mismatch		0.05		dB	
Gain Drift		1		mdB/°C	
Offset		−10		mV	

Parameter	Min	Typ	Max	Unit	Comments
Crosstalk (EIAJ Method)		−110		dB	
Volume Control Step Size (256 Steps)		0.39		% per step	
Maximum Volume Attenuation		−48		dB	
Mute Attenuation		∞		dB	ADC outputs all zero codes
Group Delay					
f_S = 48 kHz		910		µs	
f_S = 96 kHz		460		µs	
ADC LOW-PASS DIGITAL DECIMATION FILTER CHARACTERISTICS[1]					
Pass-Band Frequency		22		kHz	f_S = 48 kHz
		44		kHz	f_S = 96 kHz
Stop-Band Frequency		26		kHz	f_S = 48 kHz
		52		kHz	f_S = 96 kHz
Stop-Band Attenuation		120		dB	f_S = 48 kHz
		120		dB	f_S = 96 kHz
Pass-Band Ripple		±0.01		dB	f_S = 48 kHz
		±0.01		dB	f_S = 96 kHz
ADC HIGH-PASS DIGITAL FILTER CHARACTERISTICS					
Cutoff Frequency		0.9		Hz	f_S = 48 kHz
SRC SECTION					
Resolution		24		Bits	
Sample Rate	8		192	kHz	XIN = 27 MHz
SRC MCLK	138 × f_{S-MAX}		33	MHz	f_{S-MAX} is the greater of the input or output sample rate
Maximum Sample Rate Ratios					
Upsampling			1:8		
Downsampling			7.75:1		
Dynamic Range		140			20 Hz to f_S/2, 1 kHz, −60 dBFS input, f_{IN} = 44.1 kHz, f_{OUT} = 48 kHz
Total Harmonic Distortion + Noise		120		dB	20 Hz to f_S/2, 1 kHz, 0 dBFS input, f_{IN} = 44.1 kHz, f_{OUT} = 48 kHz
DAC SECTION					
Number of Channels		2			
Resolution		24		Bits	
Dynamic Range					20 Hz to 20 kHz, −60 dB input
Unweighted		99		dB	f_S = 48 kHz
		98		dB	f_S = 96 kHz
A-Weighted	97	101		dB	f_S = 48 kHz
		100		dB	f_S = 96 kHz
Total Harmonic Distortion + Noise					Referenced to 1 V rms
		−91		dB	f_S = 48 kHz
		−90		dB	f_S = 96 kHz
Analog Outputs					
Output Range (± Full Scale)		1.0		V rms	
Output Resistance		60		Ω	
Common-Mode Output Voltage		1.5		V	
DC Accuracy					
Gain Error	−2	−0.8		dB	
Interchannel Gain Mismatch		0.05		dB	
Gain Drift		1		mdB/°C	
DC Offset	−30		+30	mV	

Parameter	Min	Typ	Max	Unit	Comments
Crosstalk (EIAJ Method)		−110		dB	
Phase Deviation		0.05		Degrees	
Mute Attenuation		−95.625		dB	
Volume Control Step Size (256 Steps)		0.375		dB	
Group Delay					
48 kHz		630		µs	
96 kHz		155		µs	
192 kHz		66		µs	
DAC LOW-PASS DIGITAL INTERPOLATION FILTER CHARACTERISTICS					
Pass-Band Frequency		20		kHz	f_S = 44.1 kHz
		22		kHz	f_S = 48 kHz
		42		kHz	f_S = 96 kHz
Stop-Band Frequency		24		kHz	f_S = 44.1 kHz
		26		kHz	f_S = 48 kHz
		60		kHz	f_S = 96 kHz
Stop-Band Attenuation		70		dB	f_S = 44.1 kHz
		70		dB	f_S = 48 kHz
		70		dB	f_S = 96 kHz
Pass-Band Ripple		±0.002		dB	f_S = 44.1 kHz
		±0.002		dB	f_S = 48 kHz
		±0.005		dB	f_S = 96 kHz
PLL SECTION					
Master Clock Input Frequency		27/54		MHz	
Generated System Clocks					
MCLKO		27/54		MHz	
SYSCLK1	256		768	× f_S	256/384/512/768 × 32 kHz/ 44.1 kHz/48 kHz
SYSCLK2	256		768	× f_S	256/384/512/768 × 32 kHz/ 44.1 kHz/48 kHz
SYSCLK3	256	512		× f_S	256/512 × 32 kHz/44.1 kHz/ 48 kHz
Jitter					
SYSCLK1		65		ps rms	
SYSCLK2		75		ps rms	
SYSCLK3		75		ps rms	
DIR SECTION					
Input Sample Frequency	27.2		200	kHz	
Differential Input Voltage	200			mV	
DIT SECTION					
Output Sample Frequency	27.2		200	kHz	
DIGITAL I/O					
Input Voltage High, V_{IH}	2.0		DVDD	V	
Input Voltage Low, V_{IL}			0.8	V	
Input Leakage, I_{IH} @ V_{IH} = 3.3 V			10	µA	
Input Leakage, I_{IL} @ V_{IL} = 0 V			10	µA	
Output Voltage High, V_{OH} @ I_{OH} = 0.4 mA	2.4			V	
Output Voltage Low, V_{OL} @ I_{OL} = −2 mA			0.4	V	
Input Capacitance			15	pF	

Parameter	Min	Typ	Max	Unit	Comments
POWER					
Supplies					
Voltage, AVDD	3.0	3.3	3.6	V	
Voltage, DVDD	3.0	3.3	3.6	V	
Voltage, ODVDD	3.0	3.3	3.6	V	
Operating Current					All supplies at 3.3 V
Analog Current			60	mA	
Digital Current			38	mA	
Digital Interface Current			13	mA	
DIRIN/DIROUT Current		5		mA	
PLL Current			18	mA	
Power-Down Current					$\overline{\text{RESET}}$ low, no MCLK
Analog Current		18		mA	
Digital Current		2.5		mA	
Digital Interface Current		700		µA	
DIRIN/DIROUT Current		3.5		mA	
PLL Current		900		µA	
Power Supply Rejection					
Signal at Analog Supply Pins		−70		dB	1 kHz, 300 mV p-p
		−70		dB	20 kHz, 300 mV p-p

[1] Guaranteed by design.

TIMING SPECIFICATIONS

Timing specifications are guaranteed over the full temperature and supply range.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Comments
MASTER CLOCK AND RESET						
MCLKI Frequency	f_{MCLK}		12.288	54	MHz	
XIN Frequency	f_{XIN}		27.0	54	MHz	
$\overline{\text{RESET}}$ Low	t_{RESET}	20			ns	
SPI PORT						
CCLK High	t_{CCH}	40			ns	
CCLK Low	t_{CCL}	40			ns	
CIN Setup	t_{CIS}	10			ns	To CCLK rising edge
CIN Hold	t_{CIH}	10			ns	From CCLK rising edge
CLATCH Setup	t_{CLS}	10			ns	To CCLK rising edge
CLATCH Hold	t_{CLH}	10			ns	From CCLK rising edge
COUT Enable	t_{COE}			15	ns	From CLATCH falling edge
COUT Delay	t_{COD}			20	ns	From CCLK falling edge
COUT Three-State	t_{COTS}			25	ns	From CLATCH rising edge
SERIAL PORTS[1]						
Slave Mode						
xBCLK High	t_{SBH}	40			ns	
xBCLK Low	t_{SBL}	40			ns	
xBCLK Frequency	f_{SBF}	$64 \times f_S$				
xLRCLK Setup	t_{SLS}	10			ns	To xBCLK rising edge
xLRCLK Hold	t_{SLH}	10			ns	From xBCLK rising edge
xSDATA Setup	t_{SDS}	10			ns	To xBCLK rising edge
xSDATA Hold	t_{SDH}	10			ns	From xBCLK rising edge
xSDATA Delay	t_{SDD}	10			ns	From xBCLK falling edge
Master Mode						
xLRCLK Delay	t_{MLD}			5	ns	From xBCLK falling edge
xSDATA Delay	t_{MDD}			10	ns	From xBCLK falling edge
xSDATA Setup	t_{MDS}	10			ns	From xBCLK rising edge
xSDATA Hold	t_{MDH}	10			ns	From xBCLK rising edge

[1] The prefix x refers to I-, O-, IAUX-, or OAUX- for the full pin name.

TEMPERATURE RANGE

Table 4.

Heading	Min	Typ	Max	Unit
Specifications Guaranteed		25		°C
Functionality Guaranteed	−40		+85	°C
Storage	−65		+150	°C

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
DVDD to DGND and ODVDD to DGND	0 V to 4.6 V
AVDD to AGND	0 V to 4.6 V
Digital Inputs	DGND − 0.3 V to DVDD + 0.3 V
Analog Inputs	AGND − 0.3 V to AVDD + 0.3 V
AGND to DGND	−0.3 V to +0.3 V
Reference Voltage	Indefinite short circuit to ground
Soldering (10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

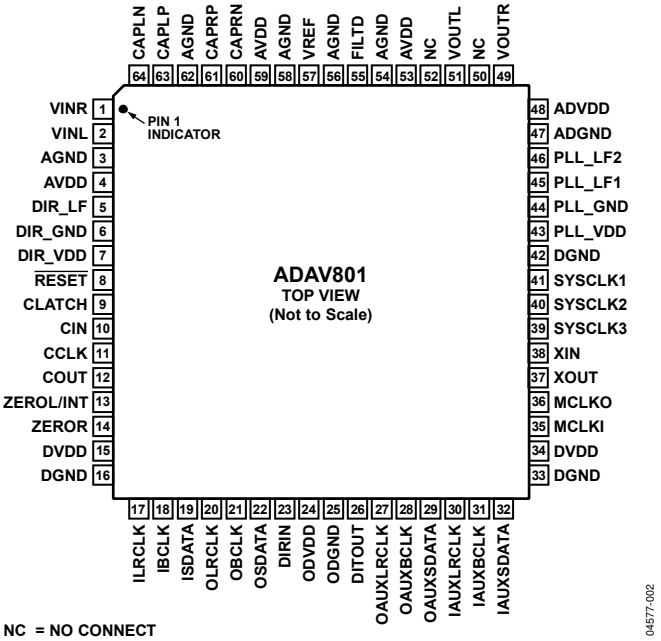

Figure 2. ADAV801 Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	I/O	Description
1	VINR	I	Analog Audio Input, Right Channel.
2	VINL	I	Analog Audio Input, Left Channel.
3	AGND		Analog Ground.
4	AVDD		Analog Voltage Supply.
5	DIR_LF		DIR Phase-Locked Loop (PLL) Filter Pin.
6	DIR_GND		Supply Ground for DIR Analog Section. This pin should be connected to AGND.
7	DIR_VDD		Supply for DIR Analog Section. This pin should be connected to AVDD.
8	$\overline{\text{RESET}}$	I	Asynchronous Reset Input (Active Low).
9	CLATCH	I	Chip Select (Control Latch) Pin of SPI-Compatible Control Interface.
10	CIN	I	Data Input of SPI-Compatible Control Interface.
11	CCLK	I	Clock Input of SPI-Compatible Control Interface.
12	COUT	O	Data Output of SPI-Compatible Control Interface.
13	ZEROL/INT	O	Left Channel (Output) Zero Flag or Interrupt (Output) Flag. The function of this pin is determined by the INTRPT bit in DAC Control Register 4.
14	ZEROR	O	Right Channel (Output) Zero Flag.
15	DVDD		Digital Voltage Supply.
16	DGND		Digital Ground.
17	ILRCLK	I/O	Sampling Clock (LRCLK) of Playback Digital Input Port.
18	IBCLK	I/O	Serial Clock (BCLK) of Playback Digital Input Port.
19	ISDATA	I	Data Input of Playback Digital Input Port.
20	OLRCLK	I/O	Sampling Clock (LRCLK) of Record Digital Output Port.
21	OBCLK	I/O	Serial Clock (BCLK) of Record Digital Output Port.
22	OSDATA	O	Data Output of Record Digital Output Port.
23	DIRIN	I	Input to Digital Input Receiver (S/PDIF).
24	ODVDD		Interface Digital Voltage Supply.
25	ODGND		Interface Digital Ground.
26	DITOUT	O	S/PDIF Output from DIT.

Pin No.	Mnemonic	I/O	Description
27	OAUXLRCLK	I/O	Sampling Clock (LRCLK) of Auxiliary Digital Output Port.
28	OAUXBCLK	I/O	Serial Clock (BCLK) of Auxiliary Digital Output Port.
29	OAUXSDATA	O	Data Output of Auxiliary Digital Output Port.
30	IAUXLRCLK	I/O	Sampling Clock (LRCLK) of Auxiliary Digital Input Port.
31	IAUXBCLK	I/O	Serial Clock (BCLK) of Auxiliary Digital Input Port.
32	IAUXSDATA	I	Data Input of Auxiliary Digital Input Port.
33	DGND		Digital Ground.
34	DVDD		Digital Supply Voltage.
35	MCLKI	I	External MCLK Input.
36	MCLKO	O	Oscillator Output.
37	XOUT	I	Crystal Input.
38	XIN	I	Crystal or External MCLK Input.
39	SYSCLK3	O	System Clock 3 (from PLL2).
40	SYSCLK2	O	System Clock 2 (from PLL2).
41	SYSCLK1	O	System Clock 1 (from PLL1).
42	DGND		Digital Ground.
43	PLL_VDD		Supply for PLL Analog Section. This pin should be connected to AVDD.
44	PLL_GND		Ground for PLL Analog Section. This pin should be connected to AGND.
45	PLL_LF1		Loop Filter for PLL1.
46	PLL_LF2		Loop Filter for PLL2.
47	ADGND		Analog Ground (Mixed Signal). This pin should be connected to AGND.
48	ADVDD		Analog Voltage Supply (Mixed Signal). This pin should be connected to AVDD.
49	VOUTR	O	Right Channel Analog Output.
50	NC		No Connect.
51	VOUTL	O	Left Channel Analog Output.
52	NC		No Connect.
53	AVDD		Analog Voltage Supply.
54	AGND		Analog Ground.
55	FILTD		Output DAC Reference Decoupling.
56	AGND		Analog Ground.
57	VREF		Voltage Reference Voltage.
58	AGND		Analog Ground.
59	AVDD		Analog Voltage Supply.
60	CAPRN		ADC Modulator Input Filter Capacitor (Right Channel, Negative).
61	CAPRP		ADC Modulator Input Filter Capacitor (Right Channel, Positive).
62	AGND		Analog Ground.
63	CAPLP		ADC Modulator Input Filter Capacitor (Left Channel, Positive).
64	CAPLN		ADC Modulator Input Filter Capacitor (Left Channel, Negative).

TYPICAL PERFORMANCE CHARACTERISTICS

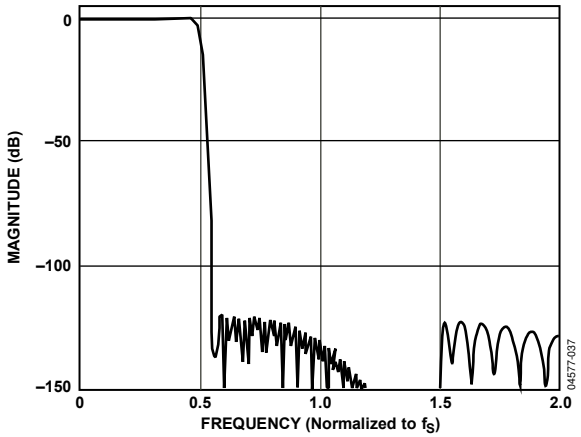

Figure 3. ADC Composite Filter Response

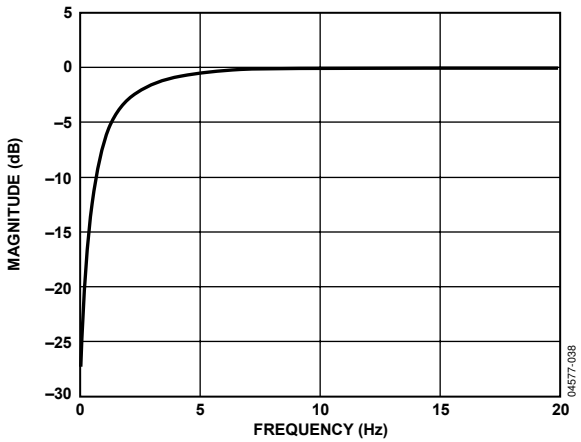

Figure 4. ADC High-Pass Filter Response, f_S = 48 kHz

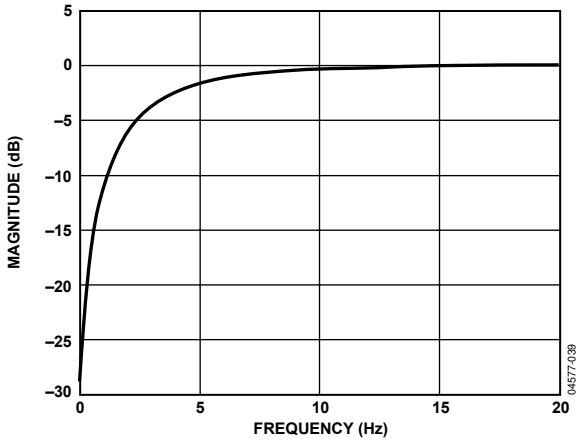

Figure 5. ADC High-Pass Filter Response, f_S = 96 kHz

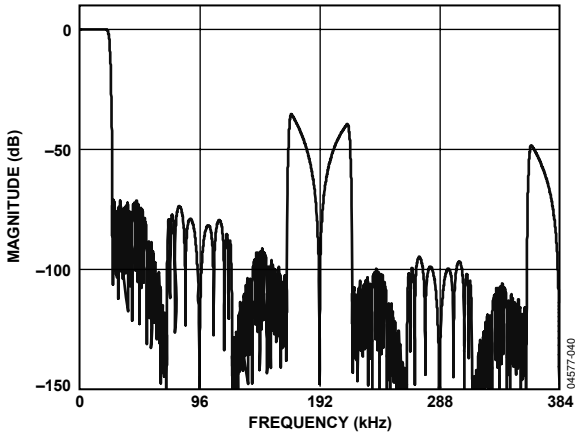

Figure 6. DAC Composite Filter Response, 48 kHz

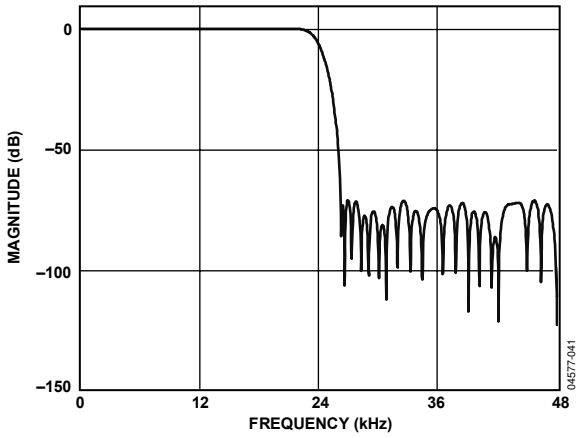

Figure 7. DAC Pass-Band Filter Response, 48 kHz

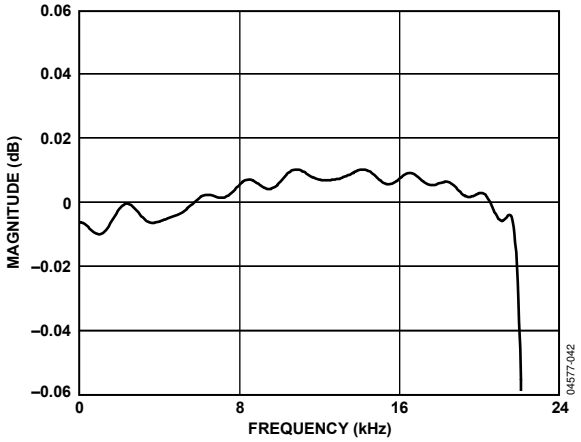

Figure 8. DAC Filter Ripple, 48 kHz

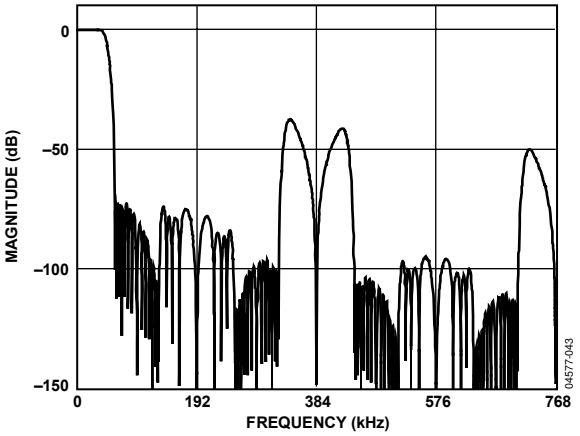

Figure 9. DAC Composite Filter Response, 96 kHz

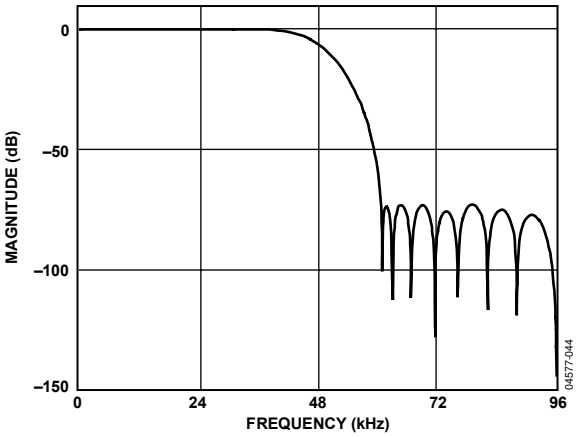

Figure 10. DAC Pass-Band Filter Response, 96 kHz

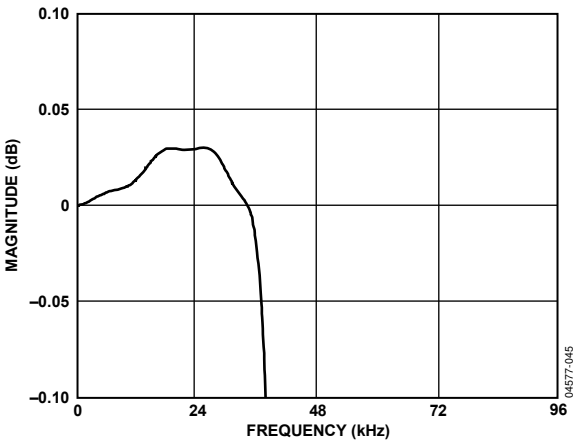

Figure 11. DAC Filter Ripple, 96 kHz

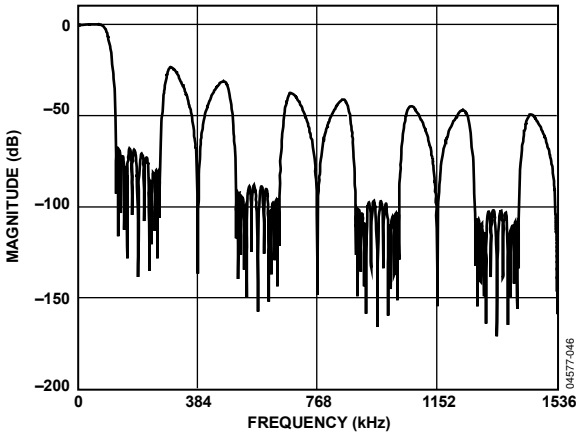

Figure 12. DAC Composite Filter Response, 192 kHz

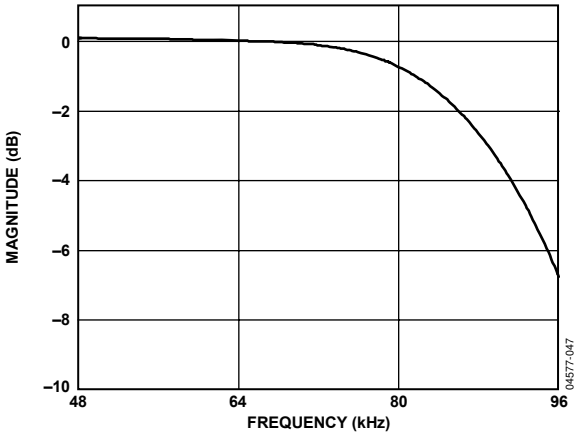

Figure 13. DAC Pass-Band Filter Response, 192 kHz

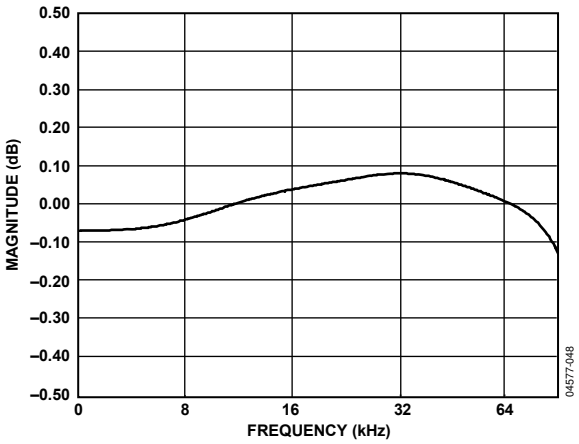

Figure 14. DAC Filter Ripple, 192 kHz

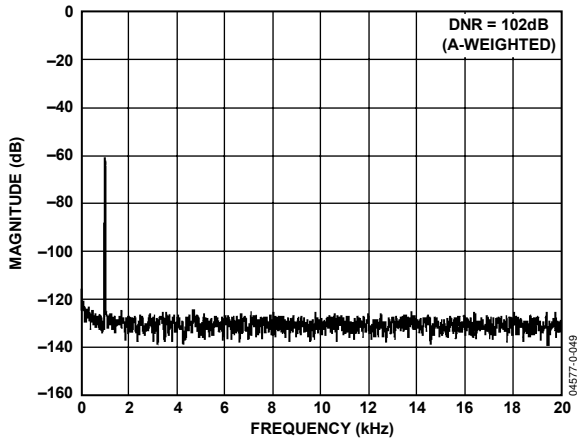

Figure 15. DAC Dynamic Range, f_S = 48 kHz

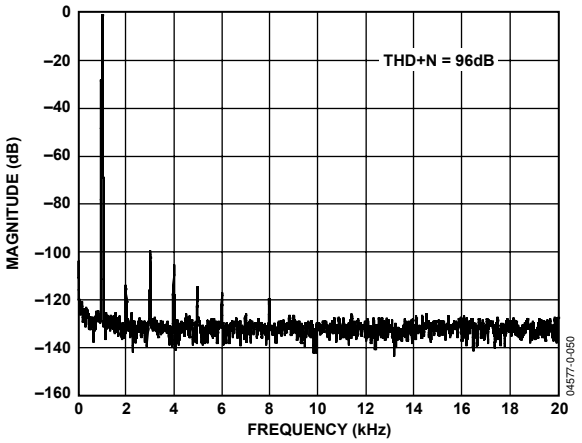

Figure 16. DAC THD + N, f_S = 48 kHz

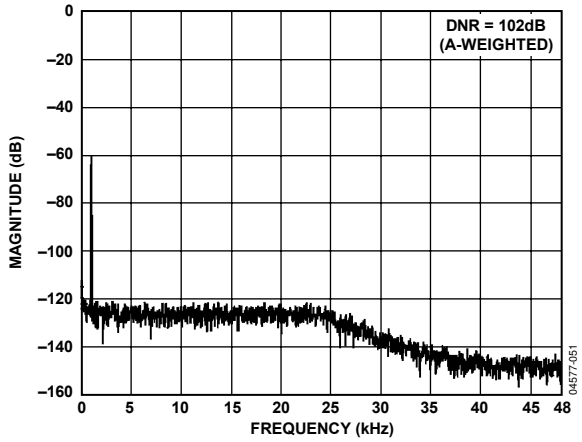

Figure 17. DAC Dynamic Range, f_S = 96 kHz

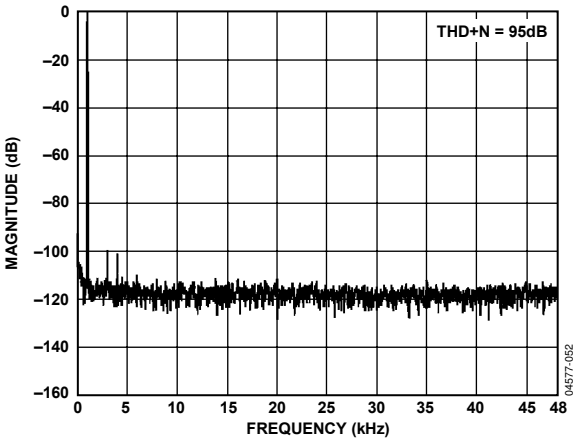

Figure 18. DAC THD + N, f_S = 96 kHz

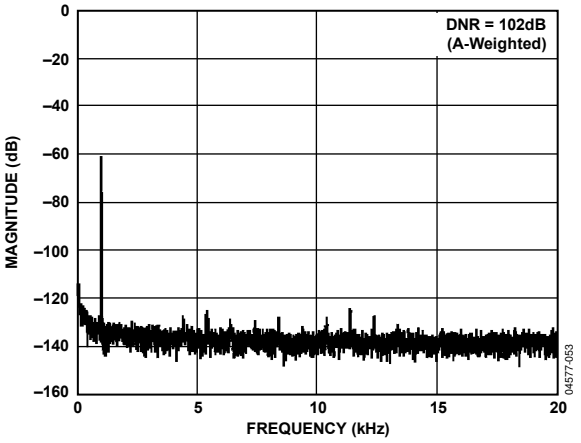

Figure 19. ADC Dynamic Range, f_S = 48 kHz

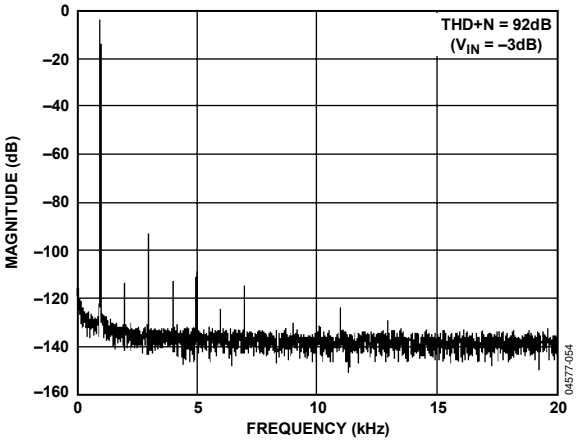

Figure 20. DAC THD + N, f_S = 48 kHz

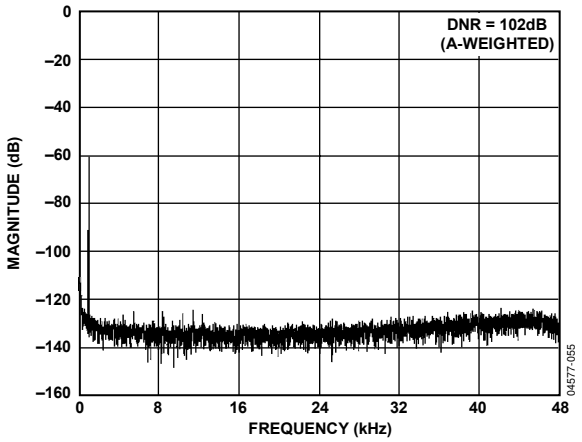

Figure 21. ADC Dynamic Range, f_S = 96 kHz

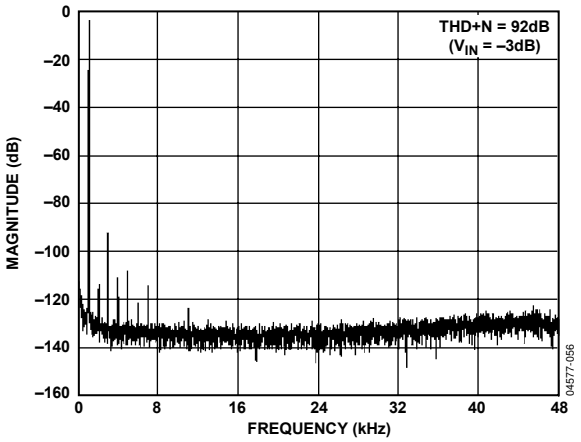

Figure 22. ADC THD + N, f_S = 96 kHz

FUNCTIONAL DESCRIPTION

ADC SECTION

The ADAV801's ADC section is implemented using a second-order multibit (5 bits) Σ-Δ modulator. The modulator is sampled at either half of the ADC MCLK rate (modulator clock = 128 × f_S) or one-quarter of the ADC MCLK rate (modulator clock = 64 × f_S). The digital decimator consists of a Sinc^5 filter followed by a cascade of three half-band FIR filters. The Sinc decimates by a factor of 16 at 48 kHz and by a factor of 8 at 96 kHz. Each of the half-band filters decimates by a factor of 2.

Figure 23 shows the details of the ADC section. By default, the ADC assumes that the MCLK rate is 256 times the sample rate. The ADC can be clocked by a number of different clock sources to control the sample rate. MCLK selection for the ADC is set by Internal Clocking Control Register 1 (Address 0x76). The ADC provides an output word of up to 24 bits in resolution in twos complement format. The output word can be routed to either the output ports, the sample rate converter, or the S/PDIF digital transmitter.

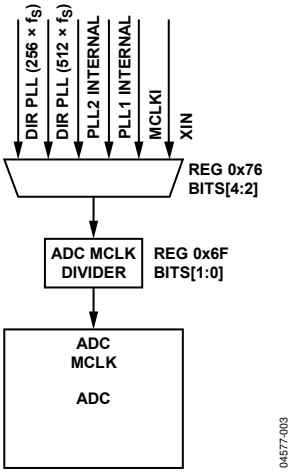

Figure 23. Clock Path Control on the ADC

Programmable Gain Amplifier (PGA)

The input of the record channel features a PGA that converts the single-ended signal to a differential signal, which is applied to the analog Σ-Δ modulator of the ADC. The PGA can be programmed to amplify a signal by up to 24 dB in 0.5 dB increments. Figure 24 shows the structure of the PGA circuit.

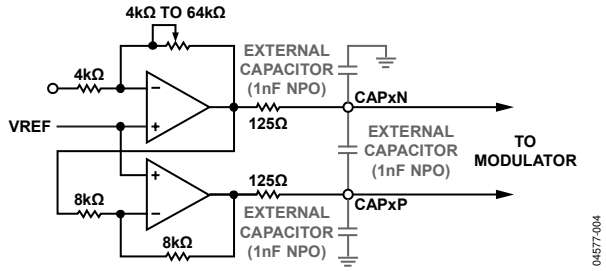

Figure 24. PGA Block Diagram

Analog Σ-Δ Modulator

The ADC features a second-order, multibit, Σ-Δ modulator. The input features two integrators in cascade followed by a flash converter. This multibit output is directed to a scrambler, followed by a DAC for loop feedback. The flash ADC output is also converted from thermometer coding to binary coding for input as a 5-bit word to the decimator. Figure 25 shows the ADC block diagram.

The ADC also features independent digital volume control for the left and right channels. The volume control consists of 256 linear steps, with each step reducing the digital output codes by 0.39%. Each channel also has a peak detector that records the peak level of the input signal. The peak detector register is cleared by reading it.

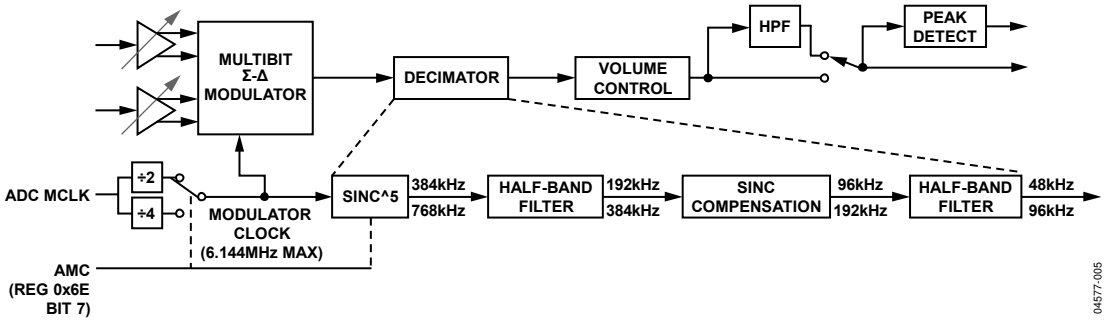

Figure 25. ADC Block Diagram

Automatic Level Control (ALC)

The ADC record channel features a programmable automatic level control block. This block monitors the level of the ADC output signal and automatically reduces the gain, if the signal at the input pins causes the ADC output to exceed a preset limit. This function can be useful to maximize the signal dynamic range when the input level is not well defined. The PGA can be used to amplify the unknown signal, and the ALC reduces the gain until the ADC output is within the preset limits. This results in maximum front end gain.

Because the ALC block monitors the output of the ADC, the volume control function should not be used. The ADC volume control scales the results from the ADC, and any distortion caused by the input signal exceeding the input range of the ADC is still present at the output of the ADC, but scaled by a value determined by the volume control register.

The ALC block has two functions, attack mode and recovery mode. Recovery mode consists of three settings: no recovery, normal recovery, and limited recovery. These modes are discussed in the following sections. Figure 26 is a flow diagram of the ALC block. When the ALC has been enabled, any changes made to the PGA or ALC settings are ignored. To change the functionality of the ALC, it must first be disabled. The settings can then be changed and the ALC re-enabled.

Attack Mode

When the absolute value of the ADC output exceeds the level set by the attack threshold bits in ALC Control Register 2, attack mode is initiated. The PGA gain for both channels is reduced by one step (0.5 dB). The ALC then waits for a time determined by the attack timer bits before sampling the ADC output value again. If the ADC output is still above the threshold, the PGA gain is reduced by a further step. This procedure continues until the ADC output is below the limit set by the attack threshold bits. The initial gains of the PGAs are defined by the ADC left PGA gain register and the ADC right PGA gain register, and they can have different values. The ALC subtracts a common gain offset to these values. The ALC preserves any gain difference in dB as defined by these registers. At no time do the PGA gains exceed their initial values. The initial gain setting, therefore, also serves as a maximum value.

The limit detection mode bit in ALC Control Register 1 determines how the ALC responds to an ADC output that exceeds the set limits. If this bit is a 1, both channels must exceed the threshold before the gain is reduced. This mode can be used to prevent unnecessary gain reduction due to spurious noise on a single channel. If the limit detection mode bit is a 0, the gain is reduced when either channel exceeds the threshold.

No Recovery Mode

By default, there is no gain recovery. Once the gain has been reduced, it is not recovered until the ALC is reset, either by toggling the ALCEN bit in ALC Control Register 1 or by writing any value to ALC Control Register 3. The latter option is more efficient because it requires only one write operation to reset the ALC function. No recovery mode prevents volume modulation of the signal caused by adjusting the gain, which can create undesirable artifacts in the signal. The gain can be reduced but not recovered. Therefore, care should be taken that spurious signals do not interfere with the input signal because these might trigger a gain reduction unnecessarily.

Normal Recovery Mode

Normal recovery mode allows for the PGA gain to be recovered, provided that the input signal meets certain criteria. First, the ALC must not be in attack mode, that is, the PGA gain has been reduced sufficiently such that the input signal is below the level set by the attack threshold bits. Second, the output result from the ADC must be below the level set by the recovery threshold bits in the ALC control register. If both of these criteria are met, the gain is recovered by one step (0.5 dB). The gain is incrementally restored to its original value, assuming that the ADC output level is below the recovery threshold at intervals determined by the recovery time bits.

If the ADC output level exceeds the recovery threshold while the PGA gain is being restored, the PGA gain value is held and does not continue restoration until the ADC output level is again below the recovery threshold. Once the PGA gain is restored to its original value, it is not changed again unless the ADC output value exceeds the attack threshold and the ALC then enters attack mode. Care should be taken when using this mode to choose values for the attack and recovery thresholds that prevent excessive volume modulation caused by continuous gain adjustments.

Limited Recovery Mode

Limited recovery mode offers a compromise between no recovery and normal recovery modes. If the output level of the ADC exceeds the attack threshold, attack mode is initiated. When attack mode has reduced the PGA gain to suitable levels, the ALC attempts to recover the gain to its original level. If the ADC output level exceeds the level set by the recovery threshold bits, a counter is incremented (GAINCNTR). This counter is incremented at intervals equal to the recovery time selection, if the ADC has any excursion above the recovery threshold. If the counter reaches its maximum value, determined by the GAINCNTR bits in ALC Control Register 1, the PGA gain is deemed suitable and no further gain recovery is attempted. Whenever the ADC output level exceeds the attack threshold, attack mode is reinitiated and the counter is reset.

Selecting a Sample Rate

The output sample rate of the ADC is always ADC MCLK/256, as shown in Figure 23. By default, the ADC modulator runs at ADC MCLK/2. When the ADC MCLK exceeds 12.288 MHz, the ADC modulator should be set to run at ADC MCLK/4. This is achieved by setting the AMC (ADC Modulator Clock) bit in the ADC Control Register 1. To compensate for the reduced modulator clock speed, a different set of filters are used in the decimator section, ensuring that the sample rate remains the same.

The AMC bit can also be used to boost the THD + N performance of the ADC at the expense of dynamic range. The improvement is typically 0.5 dB to 1.0 dB and works because selecting the lower modulator rate reduces the amount of digital noise, improving THD + N, but also reduces the oversampling ratio, therefore reducing the dynamic range by a corresponding amount.

For best performance of the ADC, avoid using similar frequency clocks from separate sources in the ADAV801. For example, running the ADC from a 12.288 MHz clock connected to MCLKI and using the PLL to generate a separate 12.288 MHz clock for the DAC can reduce the performance of the ADC. This is due to the interaction of the clocks, which generate beat frequencies that can affect the charge on the switch capacitors of the analog inputs.

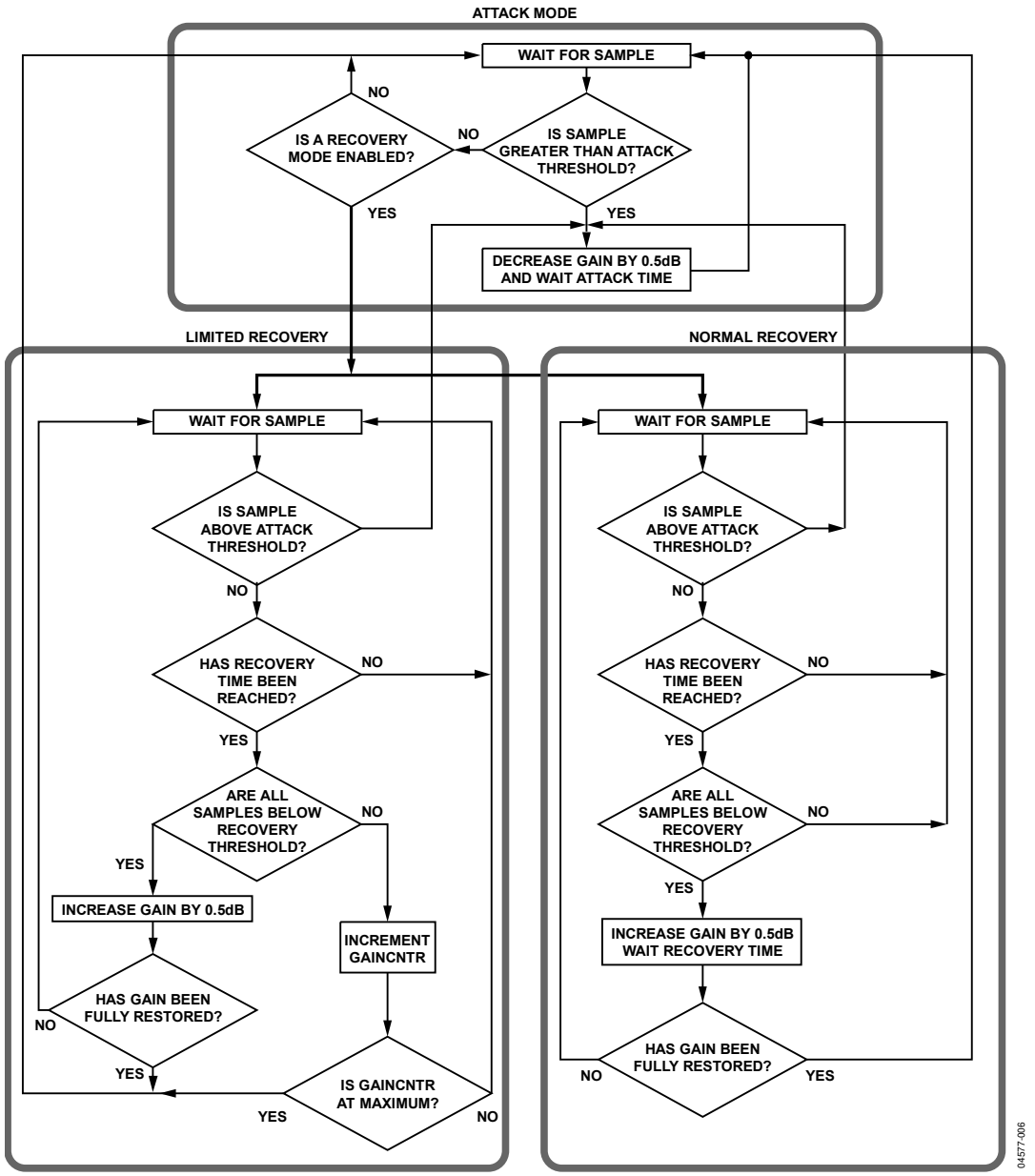

Figure 26. ALC Flow Diagram

DAC SECTION

The ADAV801 has two DAC channels arranged as a stereo pair with single-ended analog outputs. Each channel has its own independently programmable attenuator, adjustable in 128 steps of 0.375 dB per step. The DAC can receive data from the playback or auxiliary input ports, the SRC, the ADC, or the DIR. Each analog output pin sits at a dc level of VREF, and swings 1.0 V rms for a 0 dB digital input signal. A single op amp third-order external low-pass filter is recommended to remove high frequency noise present on the output pins. Note that the use of op amps with low slew rate or low bandwidth can cause high frequency noise and tones to fold down into the audio band. Care should be taken in selecting these components.

The FILTD and VREF pins should be bypassed by external capacitors to AGND. The FILTD pin is used to reduce the noise of the internal DAC bias circuitry, thereby reducing the DAC output noise. The voltage at the VREF pin can be used to bias external op amps used to filter the output signals. For applications in which the VREF is required to drive external op amps, which might draw more than 50 μA or have dynamic load changes, extra buffering should be used to preserve the quality of the ADAV801 reference.

The digital input data source for the DAC can be selected from a number of available sources by programming the appropriate bits in the datapath control register. Figure 27 shows how the digital data source and the MCLK source for the DAC are selected. Each DAC has an independent volume register giving 256 steps of control, with each step giving approximately 0.375 dB of attenuation. Note that the DACs are muted by default to prevent unwanted pops, clicks, and other noises from appearing on the outputs while the ADAV801 is being configured. Each DAC also has a peak-level register that records the peak value of the digital audio data. Reading the register clears the peak.

Selecting a Sample Rate

Correct operation of the DAC is dependent upon the data rate provided to the DAC, the master clock applied to the DAC, and the selected interpolation rate. By default, the DAC assumes that the MCLK rate is 256 times the sample rate, which requires an 8× oversampling rate. This combination is suitable for sample rates of up to 48 kHz.

For a 96 kHz data rate that has a 24.576 MHz MCLK (256 × f_S) associated with it, the DAC MCLK divider should be set to divide the MCLK by 2. This prevents the DAC engine from running too fast. To compensate for the reduced MCLK rate, the interpolator should be selected to operate in 4 × (DAC MCLK = 128 × f_S). Similar combinations can be selected for different sample rates.

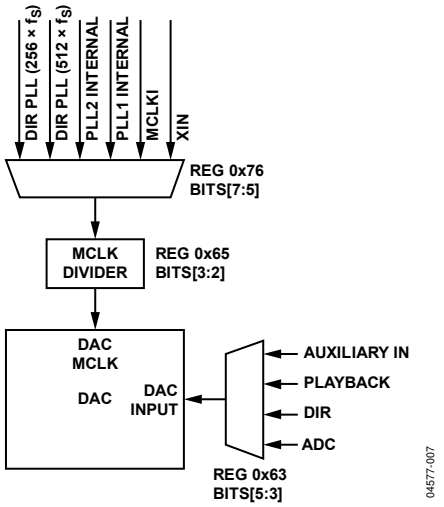

Figure 27. Clock and Datapath Control on the DAC

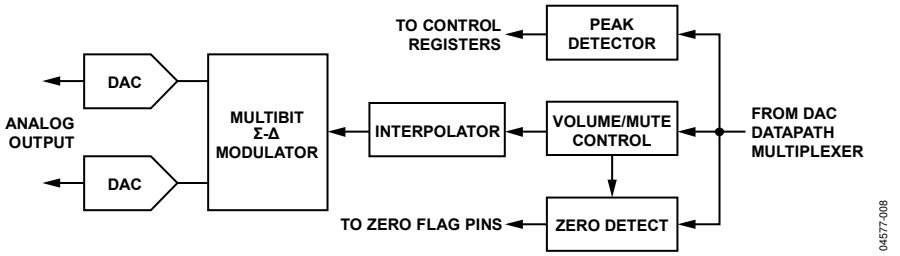

Figure 28. DAC Block Diagram

SAMPLE RATE CONVERTER (SRC) FUNCTIONAL OVERVIEW

During asynchronous sample rate conversion, data can be converted at the same sample rate or at different sample rates. The simplest approach to an asynchronous sample rate conversion is to use a zero-order hold between the two samplers, as shown in Figure 29. In an asynchronous system, T2 is never equal to T1, nor is the ratio between T2 and T1 rational. As a result, samples at f_{S_OUT} are repeated or dropped, producing an error in the resampling process.

The frequency domain shows the wide side lobes that result from this error when the sampling of f_{S_OUT} is convolved with the attenuated images from the sin(x)/x nature of the zero-order hold. The images at f_{S_IN} (dc signal images) of the zero-order hold are infinitely attenuated. Because the ratio of T2 to T1 is an irrational number, the error resulting from the resampling at f_{S_OUT} can never be eliminated. The error can be significantly reduced, however, through interpolation of the input data at f_{S_IN}. Therefore, the sample rate converter in the ADAV801 is conceptually interpolated by a factor of 2^{20}.

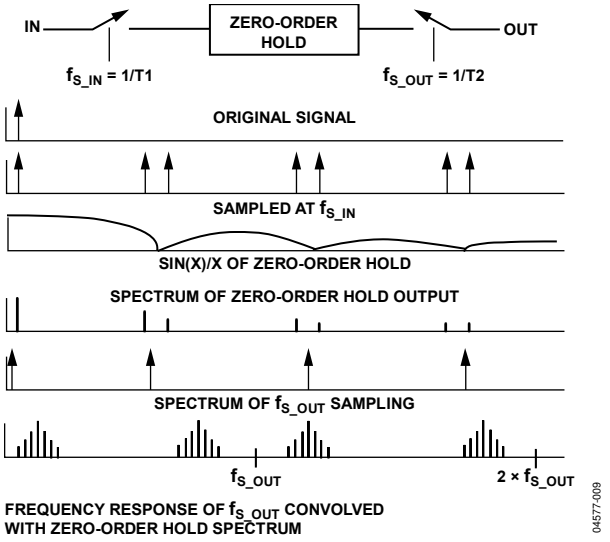

Figure 29. Zero-Order Hold Used by f_{S_OUT} to Resample Data from f_{S_IN}

Conceptual High Interpolation Model

Interpolation of the input data by a factor of 2^{20} involves placing $(2^{20} - 1)$ samples between each f_{S_IN} sample. Figure 30 shows both the time domain and the frequency domain of interpolation by a factor of 2^{20}. Conceptually, interpolation by 2^{20} involves the steps of zero-stuffing $(2^{20} - 1)$ number of samples between each f_{S_IN} sample and convolving this interpolated signal with a digital low-pass filter to suppress the images. In the time domain, it can be seen that f_{S_OUT} selects the closest $f_{S\_IN} \times 2^{20}$ sample from the zero-order hold, as opposed to the nearest f_{S_IN} sample in the case of no interpolation. This significantly reduces the resampling error.

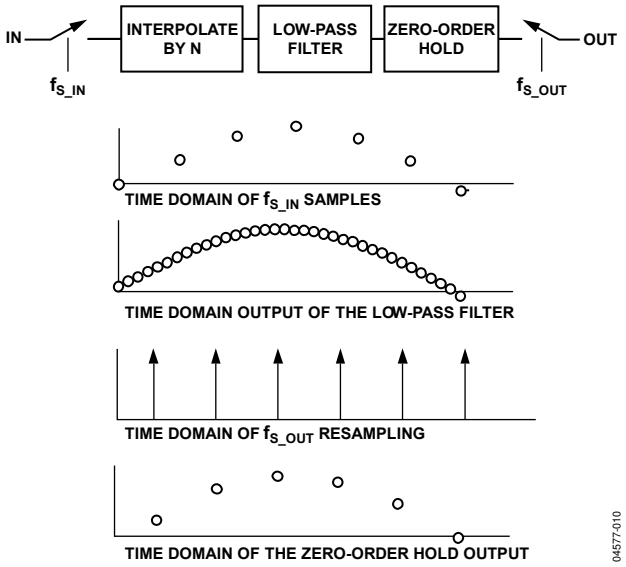

Figure 30. SRC Time Domain

In the frequency domain shown in Figure 31, the interpolation expands the frequency axis of the zero-order hold. The images from the interpolation can be sufficiently attenuated by a good low-pass filter. The images from the zero-order hold are now pushed by a factor of 2^{20} closer to the infinite attenuation point of the zero-order hold, which is $f_{S\_IN} \times 2^{20}$. The images at the zero-order hold are the determining factor for the fidelity of the output at f_{S_OUT}.

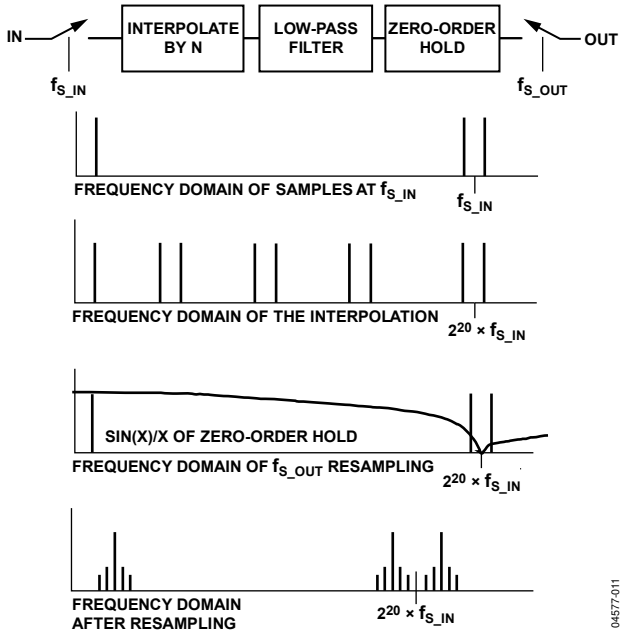

Figure 31. Frequency Domain of the Interpolation and Resampling

The worst-case images can be computed from the zero-order hold frequency response:

$$Maximum\ Image = \sin(\pi \times F/f_{S\_INTERP})/(\pi \times F/f_{S\_INTERP})$$

where:
F is the frequency of the worst-case image that would be $2^{20} \times f_{S\_IN} \pm f_{S\_IN}/2$.
$f_{S\_INTERP} = f_{S\_IN} \times 2^{20}$.

The following worst-case images would appear for f_{S_IN} equal to 192 kHz:

$$Image\ at\ f_{S\_INTERP} - 96\ kHz = -125.1\ dB$$

$$Image\ at\ f_{S\_INTERP} + 96\ kHz = -125.1\ dB$$

Hardware Model

The output rate of the low-pass filter in Figure 30 is the interpolation rate:

$$2^{20} \times 192{,}000\ kHz = 201.3\ GHz$$

Sampling at a rate of 201.3 GHz is clearly impractical, in addition to the number of taps required to calculate each interpolated sample. However, because interpolation by 2^{20} involves zero-stuffing $2^{20} - 1$ samples between each f_{S_IN} sample, most of the multiplies in the low-pass FIR filter are by zero. A further reduction can be realized because only one interpolated sample is taken at the output at the f_{S_OUT} rate, so only one convolution needs to be performed per f_{S_OUT} period instead of 2^{20} convolutions. A 64-tap FIR filter for each f_{S_OUT} sample is sufficient to suppress the images caused by the interpolation.

One difficulty with the preceding approach is that the correct interpolated sample must be selected upon the arrival of f_{S_OUT}. Because there are 2^{20} possible convolutions per f_{S_OUT} period, the arrival of the f_{S_OUT} clock must be measured with an accuracy of 1/201.3 GHz = 4.96 ps. Measuring the f_{S_OUT} period with a clock of 201.3 GHz frequency is clearly impossible; instead, several coarse measurements of the f_{S_OUT} clock period are made and averaged over time.

Another difficulty with the preceding approach is the number of coefficients required. Because there are 2^{20} possible convolutions with a 64-tap FIR filter, there must be 2^{20} polyphase coefficients for each tap, which requires a total of 2^{26} coefficients. To reduce the number of coefficients in ROM, the SRC stores a small subset of coefficients and performs a high order interpolation between the stored coefficients.

The preceding approach works when $f_{S\_OUT} > f_{S\_IN}$. However, when the output sample rate, f_{S_OUT}, is less than the input sample rate, f_{S_IN}, the ROM starting address, input data, and length of the convolution must be scaled. As the input sample rate rises over the output sample rate, the antialiasing filter's cutoff frequency must be lowered because the Nyquist frequency of the output samples is less than the Nyquist frequency of the input samples. To move the cutoff frequency of the antialiasing filter, the coefficients are dynamically altered and the length of the convolution is increased by a factor of (f_{S_IN}/f_{S_OUT}).

This technique is supported by the Fourier transform property that, if f(t) is F(ω), then f(k × t) is F(ω/k). Thus, the range of decimation is limited by the size of the RAM.

SRC Architecture

The architecture of the sample rate converter is shown in Figure 32. The sample rate converter's FIFO block adjusts the left and right input samples and stores them for the FIR filter's convolution cycle. The f_{S_IN} counter provides the write address to the FIFO block and the ramp input to the digital servo loop. The ROM stores the coefficients for the FIR filter convolution and performs a high order interpolation between the stored coefficients. The sample rate ratio block measures the sample rate for dynamically altering the ROM coefficients and scaling of the FIR filter length as well as the input data. The digital servo loop automatically tracks the f_{S_IN} and f_{S_OUT} sample rates and provides the RAM and ROM start addresses for the start of the FIR filter convolution.

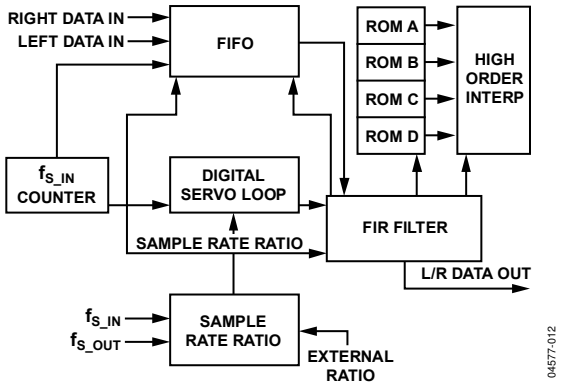

Figure 32. Architecture of the Sample Rate Converter

The FIFO receives the left and right input data and adjusts the amplitude of the data for both the soft muting of the sample rate converter and the scaling of the input data by the sample rate ratio before storing the samples in the RAM. The input data is scaled by the sample rate ratio because, as the FIR filter length of the convolution increases, so does the amplitude of the convolution output. To keep the output of the FIR filter from saturating, the input data is scaled down by multiplying it by (f_{S_OUT}/f_{S_IN}) when $f_{S\_OUT} < f_{S\_IN}$. The FIFO also scales the input data for muting and unmuting of the SRC.

The RAM in the FIFO is 512 words deep for both left and right channels. An offset to the write address provided by the f_{S_IN} counter is added to prevent the RAM read pointer from overlapping the write address. The minimum offset on the SRC is 16 samples. However, the group delay and mute-in register can be used to increase this offset.

The number of input samples added to the write pointer of the FIFO on the SRC is 16 plus Bit 6 to Bit 0 of the group delay register. This feature is useful in varispeed applications to prevent the read pointer to the FIFO from running ahead of the write pointer. When set, Bit 7 of the group delay and mute-in register soft-mutes the sample rate. Increasing the offset of the

write address pointer is useful for applications in which small changes in the sample rate ratio between f_{S_IN} and f_{S_OUT} are expected. The maximum decimation rate can be calculated from the RAM word depth and the group delay as

(512 − 16)/64 taps = 7.75

for short group delay and

(512 − 64)/64 taps = 7

for long group delay.

The digital servo loop is essentially a ramp filter that provides the initial pointer to the address in RAM and ROM for the start of the FIR convolution. The RAM pointer is the integer output of the ramp filter, and the ROM is the fractional part. The digital servo loop must provide excellent rejection of jitter on the f_{S_IN} and f_{S_OUT} clocks, as well as measure the arrival of the f_{S_OUT} clock within 4.97 ps. The digital servo loop also divides the fractional part of the ramp output by the ratio of f_{S_IN}/f_{S_OUT} to dynamically alter the ROM coefficients when $f_{S\_IN} > f_{S\_OUT}$.

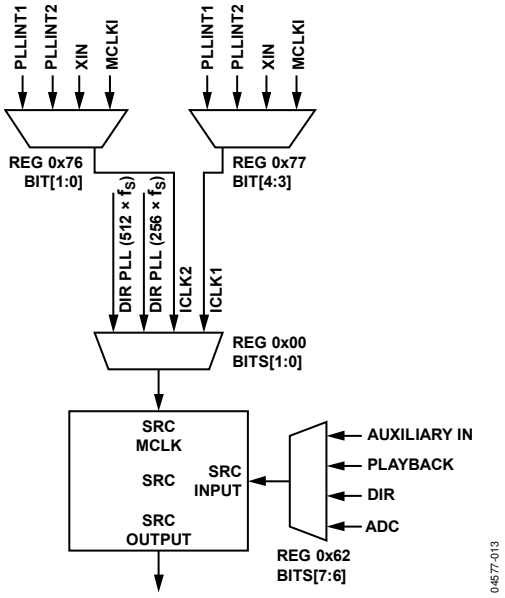

Figure 33. Clock and Datapath Control on the SRC

The digital servo loop is implemented with a multirate filter. To settle the digital servo loop filter more quickly upon startup or a change in the sample rate, a fast mode has been added to the filter. When the digital servo loop starts up or the sample rate is changed, the digital servo loop enters fast mode to adjust and settle on the new sample rate. Upon sensing that the digital servo loop is settling down to a reasonable value, the digital servo loop returns to normal (or slow) mode.

During fast mode, the MUTE_IND bit in the Sample Rate Converter Error register is asserted to let the user know that clicks or pops might be present in the digital audio data. The output of the SRC can be muted by asserting Bit 7 of the Group Delay and Mute register until the SRC has changed to slow mode. The MUTE_IND bit can be set to generate an interrupt when the SRC changes to slow mode, indicating that the data is being sample rate converted accurately.

The frequency responses of the digital servo loop for fast mode and slow mode are shown in Figure 34. The FIR filter is a 64-tap filter when $f_{S\_OUT} \geq f_{S\_IN}$ and is $(f_{S\_IN}/f_{S\_OUT}) \times 64$ taps when $f_{S\_IN} > f_{S\_OUT}$. The FIR filter performs its convolution by loading in the starting address of the RAM address pointer and the ROM address pointer from the digital servo loop at the start of the f_{S_OUT} period. The FIR filter then steps through the RAM by decrementing its address by 1 for each tap, and the ROM pointer increments its address by the $(f_{S\_OUT}/f_{S\_IN}) \times 2^{20}$ ratio for $f_{S\_IN} > f_{S\_OUT}$ or 2^{20} for $f_{S\_OUT} \geq f_{S\_IN}$. Once the ROM address rolls over, the convolution is completed.

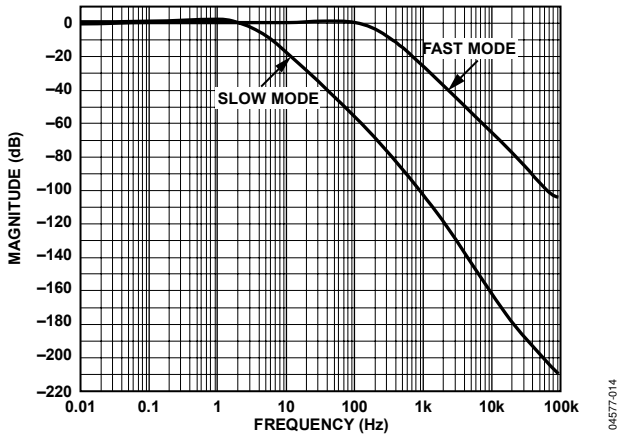

Figure 34. Frequency Response of the Digital Servo Loop; f_{S_IN} is the X-Axis, f_{S_OUT} = 192 kHz, Master Clock is 30 MHz

The convolution is performed for both the left and right channels, and the multiply accumulate circuit used for the convolution is shared between the channels. The f_{S_IN}/f_{S_OUT} sample rate ratio circuit is used to dynamically alter the coefficients in the ROM when $f_{S\_IN} > f_{S\_OUT}$. The ratio is calculated by comparing the output of an f_{S_OUT} counter to the output of an f_{S_IN} counter. If $f_{S\_OUT} > f_{S\_IN}$, the ratio is held at one. If $f_{S\_IN} > f_{S\_OUT}$, the sample rate ratio is updated, if it is different by more than two f_{S_OUT} periods from the previous f_{S_OUT} to f_{S_IN} comparison. This is done to provide some hysteresis to prevent the filter length from oscillating and causing distortion.

Figure 33 shows the detail of the SRC section. The SRC master clock is expected to be equal to 256 times the output sample rate. This master clock can be provided by four different clock sources. The selection is set by the SRC and Clock Control register (Address 0x00), and the selected clock source can be divided using the same register.

PLL SECTION

The ADAV801 features a dual PLL configuration to generate independent system clocks for asynchronous operation. Figure 37 shows the block diagram of the PLL section. The PLL generates the internal and system clocks from a 27 MHz clock. This clock is generated either by a crystal connected between XIN and XOUT, as shown in Figure 35, or from an external clock source connected directly to XIN. A 54 MHz clock can also be used, if the internal clock divider is used.

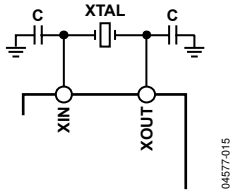

Figure 35. Crystal Connection

Both PLLs (PLL1 and PLL2) can be programmed independently and can accommodate a range of sampling rates (32 kHz/44.1 kHz/48 kHz) with selectable system clock oversampling rates of 256 and 384. Higher oversampling rates can also be selected by enabling the doubling of the sampling rate to give 512 or 768 × f_S ratios. Note that this option also allows oversampling ratios of 256 or 384 at double sample rates of 64 kHz/88.2 kHz/96 kHz.

The PLL outputs can be routed internally to act as clock sources for the other component blocks such as the ADC and DAC. The outputs of the PLLs are also available on the three SYSCLK pins. Figure 38 shows how the PLLs can be configured to provide the sampling clocks.

Table 7. PLL Frequency Selection Options

PLL	Sample Rate, f_S (kHz)	MCLK Selection	
		Normal f_S	Double f_S
1	32/44.1/48	256/384 × f_S	512/768 × f_S
	64/88.2/96		256/384 × f_S
2A	32/44.1/48	256/384 × f_S	512/768 × f_S
	64/88.2/96		256/384 × f_S
2B	Same as f_S selected for PLL2A	256/512 × f_S	

The PLLs require some external components to operate correctly. These components, shown in Figure 36, form a loop filter that integrates the current pulses from a charge pump and produces a voltage that is used to tune the VCO. Good quality capacitors, such as PPS film, are recommended. Figure 37 shows a block diagram of the PLL section, including the master clock selection. Figure 38 shows how the clock frequencies at the clock output pins, SYSCLK1 to SYSCLK3, and the internal PLL clock values, PLL1 and PLL2, are selected.

The clock nodes, PLL1 and PLL2, can be used as master clocks for the other blocks in the ADAV801, such as the DAC or ADC. The PLL has separate supply and ground pins, which should be as clean as possible to prevent electrical noise from being converted into clock jitter by coupling onto the loop filter pins.

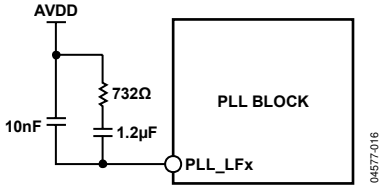

Figure 36. PLL Loop Filter

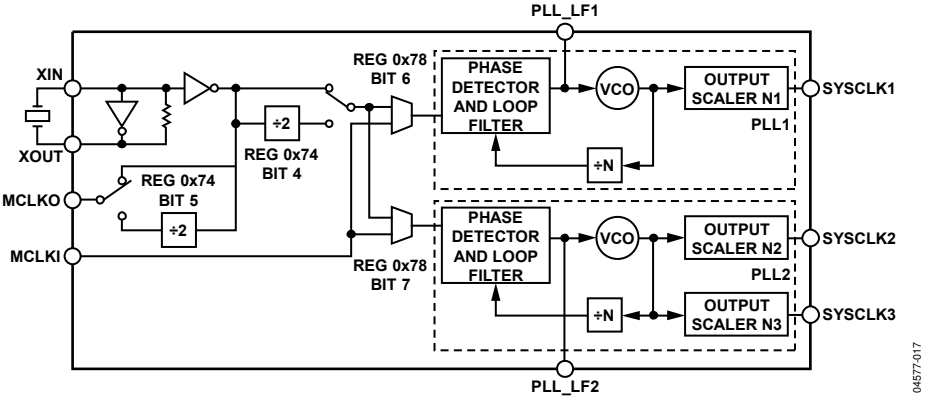

Figure 37. PLL Section Block Diagram

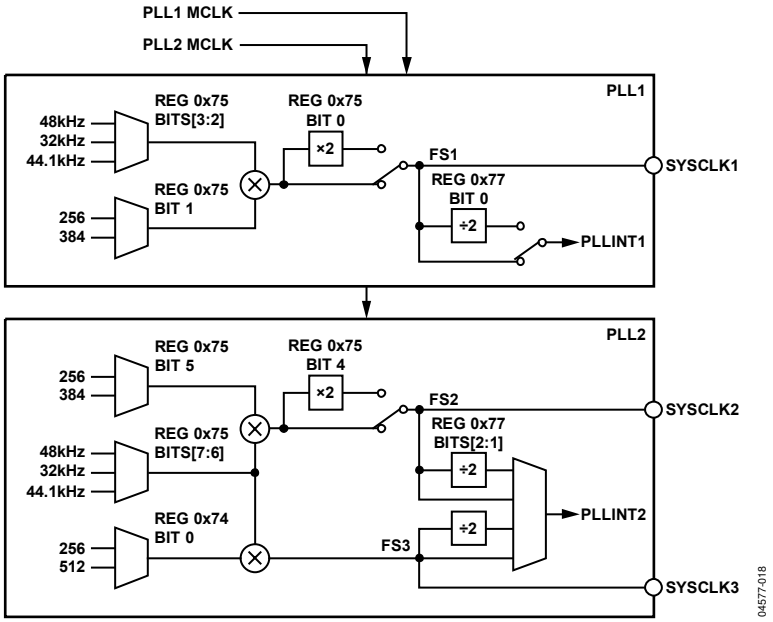

Figure 38. PLL Clocking Scheme

S/PDIF TRANSMITTER AND RECEIVER

The ADAV801 contains an integrated S/PDIF transmitter and receiver. The transmitter consists of a single output pin, DITOUT, on which the biphase encoded data appears. The S/PDIF transmitter source can be selected from the different blocks making up the ADAV801. Additionally, the clock source for the S/PDIF transmitter can be selected from the various clock sources available in the ADAV801.

The receiver uses two pins, DIRIN and DIR_LF. DIRIN accepts the S/PDIF input data stream. The DIRIN pin can be configured to accept a digital input level, as defined in the Specifications section, or an input signal with a peak-to-peak level of 200 mV minimum, as defined by the IEC 60958-3 specification. DIR_LF is a loop filter pin, required by the internal PLL, which is used to recover the clock from the S/PDIF data stream.

The components shown in Figure 42 form a loop filter, which integrates the current pulses from a charge pump and produces a voltage that is used to tune the VCO of the clock recovery PLL. The recovered audio data and audio clock can be routed to the different blocks of the ADAV801, as required. Figure 39 shows a conceptual diagram of the DIRIN block.

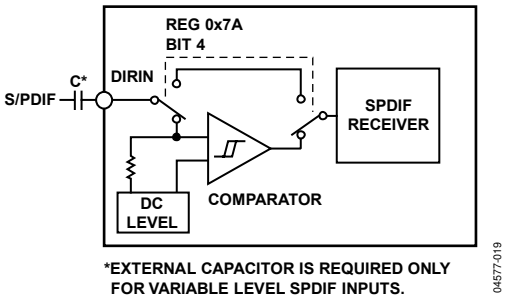

Figure 39. DIRIN Block

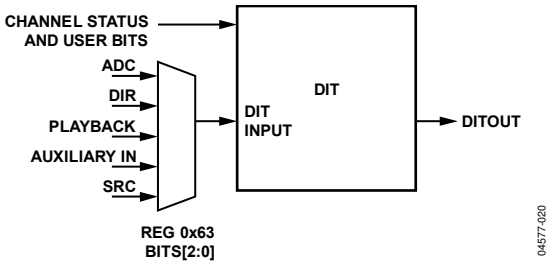

Figure 40. Digital Output Transmitter Block Diagram

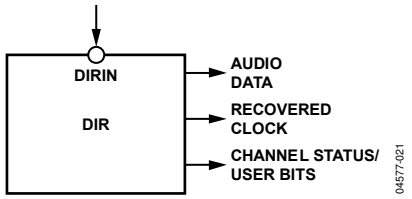

Figure 41. Digital Input Receiver Block Diagram

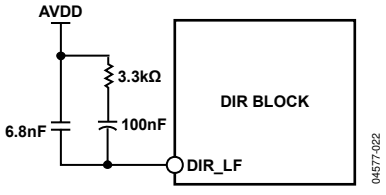

Figure 42. DIR Loop Filter Components

Serial Digital Audio Transmission Standards

The ADAV801 can receive and transmit S/PDIF, AES/EBU, and IEC-958 serial streams. S/PDIF is a consumer audio standard, and AES/EBU is a professional audio standard. IEC-958 has both consumer and professional definitions. This data sheet is not intended to fully define or to provide a tutorial for these standards. Contact the international standards-setting bodies for the full specifications.

All these digital audio communication schemes encode audio data and audio control information using the biphase-mark method. This encoding method minimizes the dc content of the transmitted signal. As can be seen from Figure 43, 1s in the original data end up with midcell transitions in the biphase-mark encoded data, while 0s in the original data do not. Note that the biphase-mark encoded data always has a transition between bit boundaries.

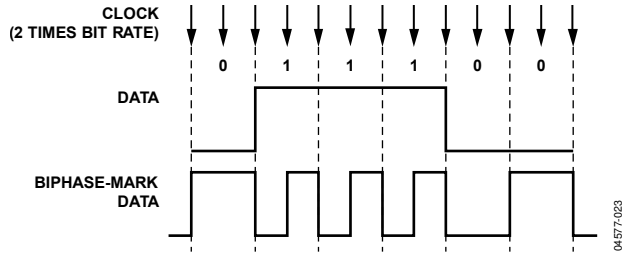

Figure 43. Biphase-Mark Encoding

Digital audio-communication schemes use preambles to distinguish among channels (called subframes) and among longer-term control information blocks (called frames). Preambles are particular biphase-mark patterns, which contain encoding violations that allow the receiver to uniquely recognize them. These patterns and their relationship to frames and subframes are shown in Table 8 and Figure 44.

Table 8. Biphase-Mark Encode Preamble

	Biphase Patterns	Channel
X	11100010 or 00011101	Left
Y	11100100 or 00011011	Right
Z	11101000 or 00010111	Left and CS block start

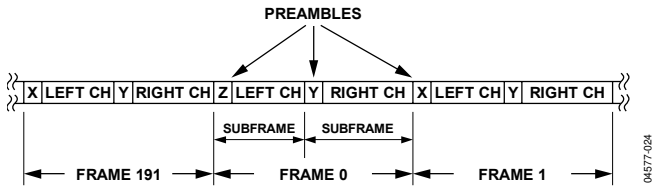

Figure 44. Preambles, Frames, and Subframes

The biphase-mark encoding violations are shown in Figure 45. Note that all three preambles include encoding violations. Ordinarily, the biphase-mark encoding method results in a polarity transition between bit boundaries.

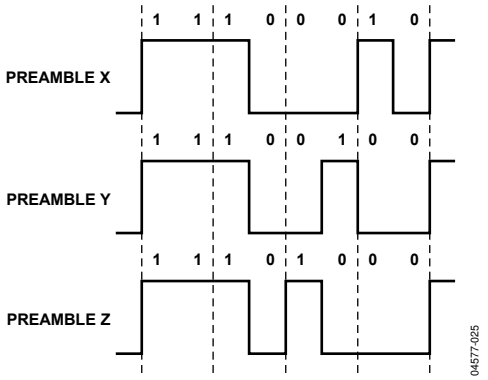

Figure 45. Preambles

The serial digital audio communication scheme is organized using a frame and subframe construction. There are two subframes per frame (ordinarily the left and right channel). Each subframe includes the appropriate 4-bit preamble, up to 24 bits of audio data, a validity (V) bit, a user (U) bit, a channel status (C) bit, and an even parity (P) bit. The channel status bits and the user bits accumulate over many frames to convey control information. The channel status bits accumulate over a 192 frame period (called a channel status block). The user bits accumulate over 1176 frames when the interconnect is implementing the so-called subcode scheme (EIAJ CP-2401). The organization of the channel status block, frames, and subframes is shown in Table 9 and Table 10. Note that the ADAV801 supports the professional audio standard from a software point of view only. The digital interface supports only consumer mode.

Table 9. Consumer Audio Standard

	Data Bits							
Address[1]	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
N	Channel Status		Emphasis			Copy-right	Non-Audio	Pro/Con = 0
N + 1	Category Code							
N + 2	Channel Number					Source Number		
N + 3	Reserved		Clock Accuracy			Sampling Frequency		
N + 4	Reserved					Word Length		
N + 5 to (N + 23)	Reserved							

[1] N = 0x20 for receiver channel status buffer.
N = 0x38 for transmitter channel status buffer.