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ADBM-A350

Optical Finger Navigation

Data Sheet

Description

The ADBM-A350 sensor is a small form factor (SFF) optical finger navigation system.

The ADBM-A350 is a low- power optical finger navigation sensor. It has a new, low-power architecture and automatic power management modes, making it ideal for battery-and power-sensitive applications such as mobile phones.

The ADBM-A350 is capable of high-speed motion detection – up to 20ips. In addition, it has an on-chip oscillator and integrated LED for optical navigation to minimize external components.

There are no moving parts, thus provide high reliability and less maintenance for the end user. In addition, precision optical alignment is not required, facilitating high volume assembly.

The sensor is programmed via registers through either a serial peripheral interface or a two wire interface port. It is packaged into a 17-pin FPC module for ease of assembly via ZIF connector.

Theory of Operation

The ADBM-A350 is based on Optical Finger Navigation (OFN) Technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement.

The ADBM-A350 contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a communication system.

The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the Δx and Δy relative displacement values.

The host reads the Δx and Δy information from the sensor serial port if a motion interrupt is published. The microcontroller then translates the data into cursor navigation, rocker switch, scrolling or other system dependent navigation data.

Features

- Low power architecture
- Self-adjusting power-saving modes for longer battery life
- High speed motion detection up to 20ips
- Self-adjusting frame rate for optimum performance
- Motion detect interrupt
- Finger detect interrupt
- Soft click and Tap detect interrupt
- Single Interrupt pin
- Optional PWM output to control LED driver to enable illumination feature when finger is on the sensor
- Optional switch input for center click function
- Internal oscillator – no clock input needed
- Selectable 125, 250, 500, 750, 1000 and 1250 cpi resolution
- Single 1.8V supply voltage for analog and digital
- Internal power up reset (POR)
- Selectable Input/Output voltage at 1.8V or 2.8V nominal
- 4-wire Serial peripheral interface (SPI) or Two wire interface (TWI)
- Integrated chip-on-board LED with wavelength of 870nm
- 17-pin FPC module

Applications

- Finger input devices
- Mobile devices
- Integrated input devices
- Battery-powered input device

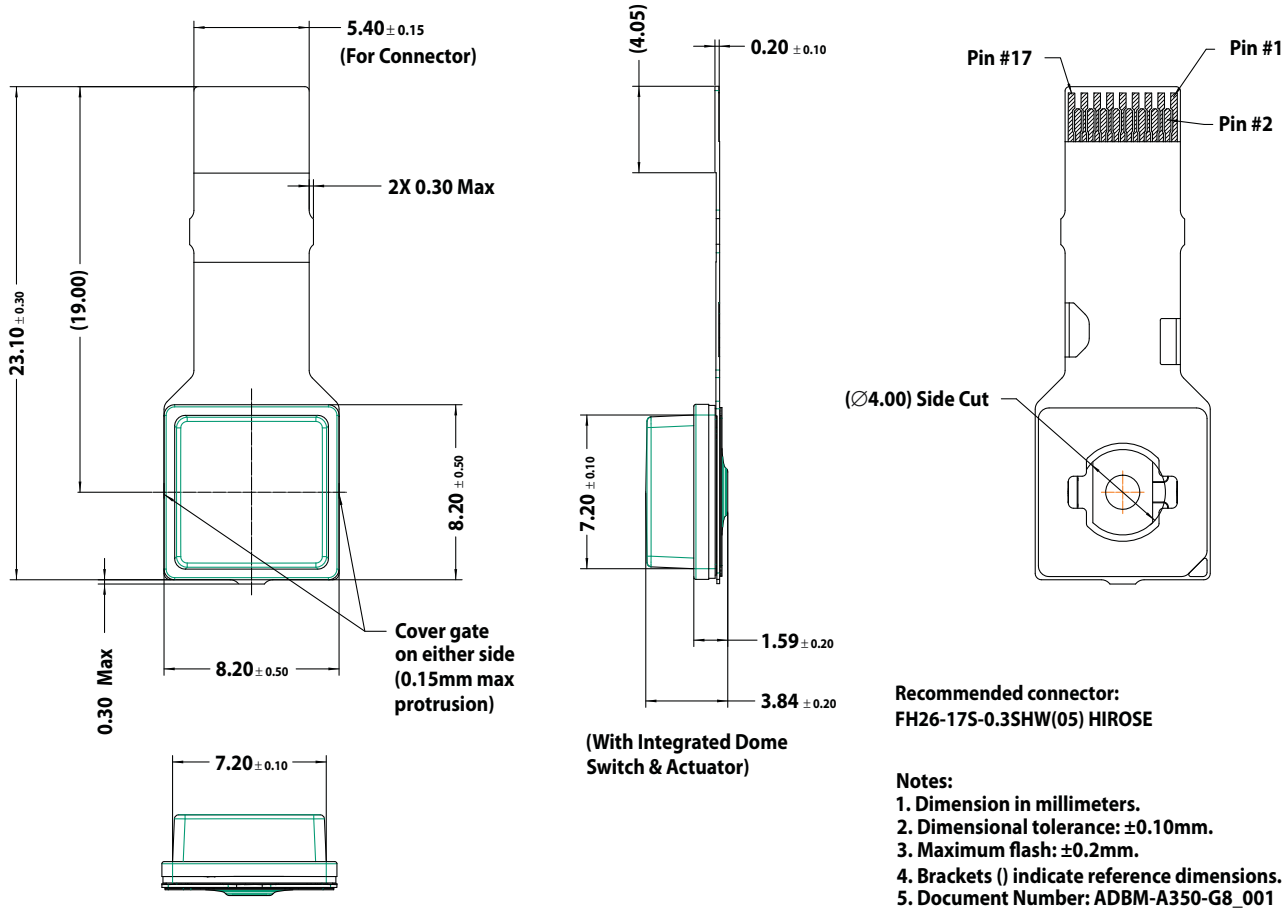
Avago customers purchasing the ADBM-350 OFN product are eligible to receive a royalty free license to our US patents 6977645, 6621483, 6950094, 6172354 and 7289649, for use in their end products.

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Pinout of ADBM-A350 Optical Sensor

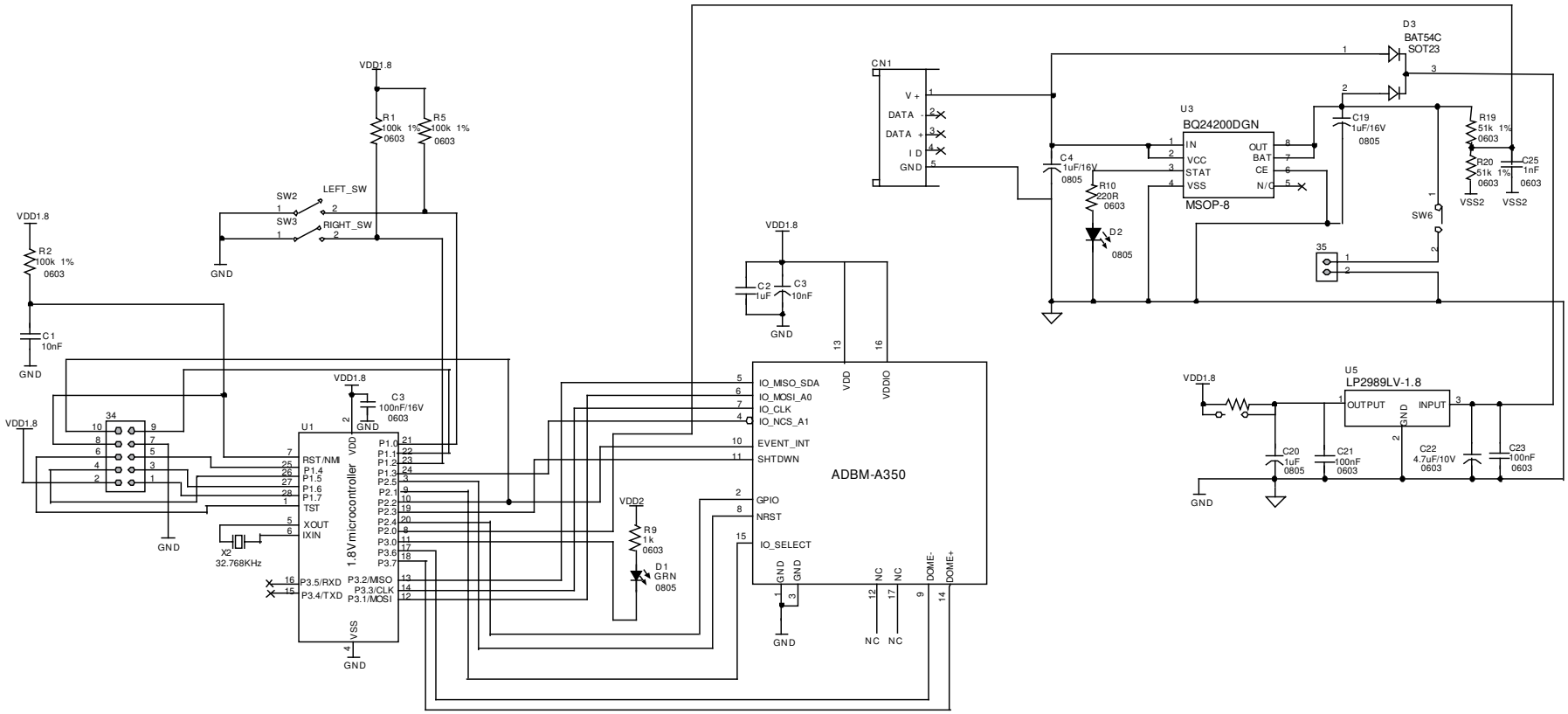
Pin	Name	Description	Input/Output pin	Function
1	GND_SHIELD	Ground shield		
2	GPIO	General Purpose Input/ Output pin	I (Schmitt trigger input)/ O (CMOS output)	Pin can be used for FPD output, PWM output or Dome/ Button click input. If configure as input do not leave pin unconnected
3	GND	Ground		
4	IO_NCS_A1	TWI address set or Chip Select	I (Schmitt trigger input)	SPI : NCS (chip select) active low signal TWI Address Select, A1 Do no leave pin unconnected
5	IO_MISO_SDA	TWI serial data or Master In Slave Out	In SPI – CMOS output. In TWI – open drain I/O	SPI : MISO (Master Input Slave Out) signal TWI : serial data signal
6	IO_MOSI_A0	TWI address set or Master Out Slave In	I (Schmitt trigger input)	SPI : MOSI (Master Out Slave In) signal TWI Address Select, A0 Do no leave pin unconnected
7	IO_CLK	Serial clock input	I (Schmitt trigger input)	Serial clock signal
8	NRST	Hardware Chip Reset	I (Schmitt trigger input)	Set to high when not used Active low signal
9	DOME-	Dome -		
10	EVENT_INT	Event Interrupt (active low output)	O (CMOS output)	Open when not used Default active low signal, can be changed in Event control register 0x1d
11	SHTDWN	Shutdown (active high input)	I (Schmitt trigger input)	Set to low when not used Active high signal
12	NC	No Connect		No connection
13	VDD	Voltage supply		Supply 1.8V
14	DOME+	Dome +		
15	IO_SELECT	SPI / TWI Select	I (Schmitt trigger input)	TWI : GND or SPI : High
16	VDDIO	Voltage supply for Input/ Output		Supply 1.8V or 2.8V
17	NC	No Connect		No connection

Note:
1. NC pins can be tied to VDD, GND or left open/ unconnected.



Notes:
1. Dimension in millimeters.
2. Dimensional tolerance: ±0.10mm.
3. Maximum flash: ±0.2mm.
4. Brackets () indicate reference dimensions.
5. Document Number: ADBM-A350-G8_001

Figure 1. Package outline drawing



Note :- Dome + must be connected to MCU to detect button change state and Dome – can be connected to GND.

Figure 2. Schematic diagram for interface between ADBM-A350 and 1.8V microcontroller via SPI

Regulatory Requirements

- Passes FCC or CISPR 22 Class B emission limits when assembled following Avago Technologies recommendations.
- Passes IEC 61000-4-3 and IEC61000-4-6 Class A Immunity limits when assembled following Avago Technologies recommendations.

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Analog and Digital Supply Voltage	VDD	-0.5	2.1	V	
I/O Supply Voltage	V_{DDIO}	-0.5	3.7	V	
ESD (sensor only)			2	kV	All pins, human body model JESD22-A114-E
Input Voltage	V_{IN}	-0.5	V_{DDIO}+0.5	V	
Latchup Current	Iout		20	mA	All Pins

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are the stress ratings only and functional operation of the device at these or any other condition beyond those indicated may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Operating Temperature	T_A	-20		70	°C	
Analog and Digital Supply Voltage [1]	V_{DD}	1.7	1.8	2.1	Volts	Including V_{NA} noise.
I/O Supply Voltage [2]	V_{DDIO}	1.65	1.8 or 2.8	3.6	Volts	Including V_{NA} noise. Sets I/O voltages. See fig 7.
Power Supply Rise Time	t_{VRT}	0.001		10	ms	0 to VDD. At minimum rise time, s/'
Power Supply Off Time for Valid POR (Power on Reset)	t_{OFF}	10			ms	Refer to section "POR During Power Cycling"
Power Off Voltage Level for Valid POR (Power on Reset)	V_{OFF}	0		300	mV	Refer to section "POR During Power Cycling"
Supply Noise (Sinusoidal)	V_{NA}			100	mV p-p	10 kHz - 50 MHz
Speed	S			20	in/sec	Using prosthetic finger as surface
Transient Supply Current	I_{DDT}			80	mA	Max supply current for 500 µsec for each supply voltages ramp from 0 to 1.8 V

Notes:
1. Operating temperature of less than -20°C down to -30°C, minimum VDD of 1.8V must be met.
2. To ensure minimum leakage current, VDDIO should be greater than or equal to VDD

Timing Specifications

Electrical Characteristics at 25° C, VDD=VDDIO=1.8V.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Motion Delay After Reset	$t_{MOT-RST}$	3.5		23	ms	From Hard reset or SOFT_RESET register write to valid register write/read and motion, assuming motion is present
Shutdown	t_{SHTDWN}			50	ms	From SHTDWN pin active to low current
Wake from Shutdown	t_{WAKEUP}	100			ms	From SHTDWN pin inactive to valid motion. Refer to section "Notes on Shutdown", also note $t_{MOT-RST}$
EVENT_INT Rise Time	$t_{r-EVENT\_INT}$		150	300	ns	C_L = 100 pF
EVENT_INT Fall Time	$t_{f-EVENT\_INT}$		150	300	ns	C_L = 100 pF
SHTDWN Pulse Width	$t_{P-SHTDWN}$	150			ms	
NRST Pulse Width	t_{NRST}	20			µs	From edge of valid NRST pulse
Reset Wait Time After Stable Supply Voltage	$t_{VRT-NRST}$	100			ms	

DC Electrical Specifications

Electrical Characteristics at 25° C, VDD=VDDIO=1.8V at default LED setting 13 mA.

Parameter		Typical	Max	Units	Notes
DC average supply current in Run mode	I_{VDD}	2.90	4.03	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=pull high.
DC average supply current in Rest1 mode	I_{VDD}	0.35	0.50	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=pull high.
DC average supply current in Rest2 mode	I_{VDD}	0.07	0.12	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=pull high.
DC average supply current in Rest3 mode	I_{VDD}	0.03	0.06	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=pull high.
Analog shutdown supply current	$I_{DDSHTDWN}$ VDD	1.54	26.7	µA	GPIO=pull low, SHTDWN=IO_MISO=NRST=pull high.

DC Electrical Specifications

Electrical Characteristics at 25° C, VDD=VDDIO=1.8V at default LED setting 13 mA.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
V_{DDIO} DC Supply Current	I V_{DDIO}			20	µA	
Digital peak supply current	I_{PEAK} VDD			10	mA	
LED+ peak supply current	I_{PEAK} LED+			35	mA	At LED register setting of 27 mA
Input Low Voltage	V_{IL}	-0.05	0	V_{DDIO}*0.35	V	IO_MOSI_A0, IO_CLK, IO_MISO_SDA, IO_NCS_A1, NRST, SHTDWN, IO_SELECT
Input High Voltage	V_{IH}	V_{DDIO} * 0.7	V_{DDIO}	V_{DDIO}+0.05	V	IO_MOSI_A0, IO_CLK, IO_MISO_SDA, IO_NCS_A1, NRST, SHTDWN, IO_SELECT
Input hysteresis	V_{HYS}	100			mV	
Input leakage current	I_{leak}		±1	±10	µA	IO_MOSI_A0, IO_CLK, IO_MISO_SDA, IO_NCS_A1, NRST, SHTDWN, IO_SELECT
Output Low Voltage	V_{OL}			0.2	V	I_{out} = 1.2 mA
Output High Voltage	V_{OH}	V_{DDIO}-0.2	V_{DDIO}-0.1		V	I_{out} = 600 µA
Input Capacitance	C_{in}			10	pF	MOSI, NCS, SCLK, SHTDWN

Notes on Power-up Sequence

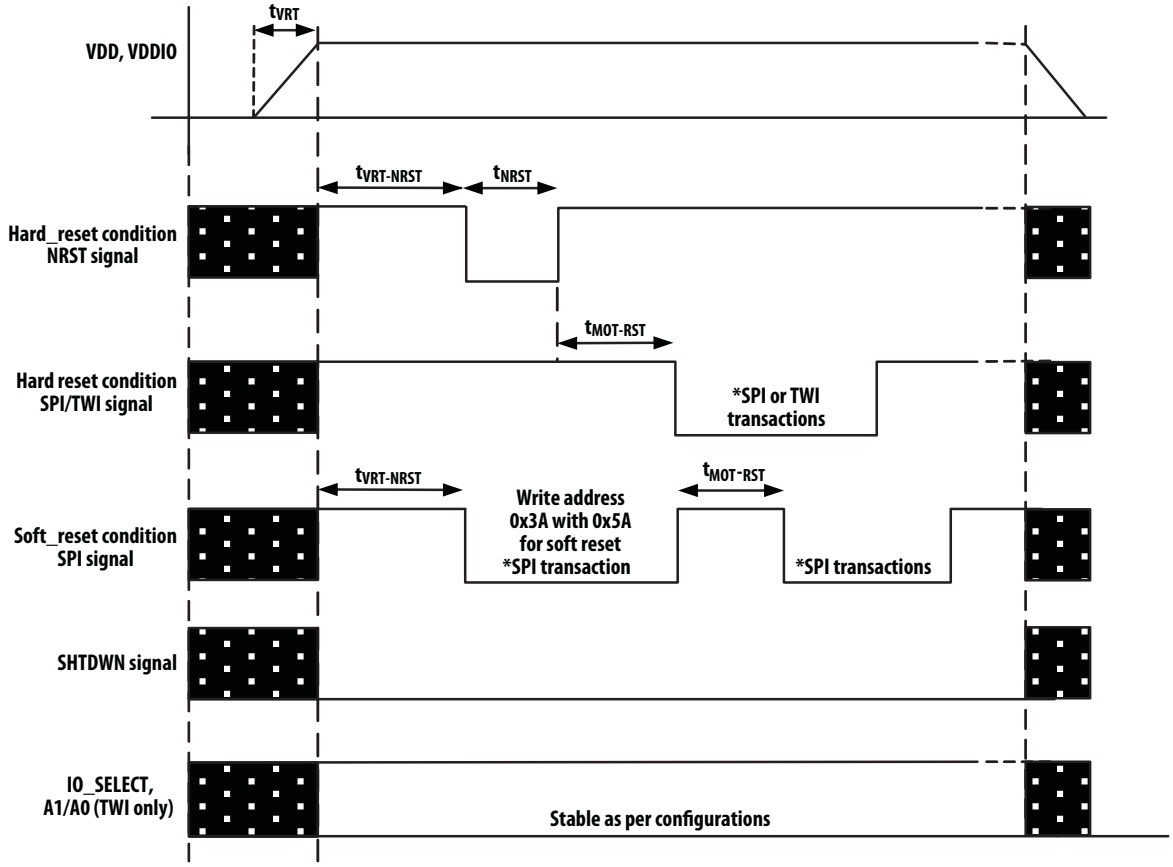
Below is the power up sequence for ADBS-A350:

For SPI:

1. Apply power. Refer timing diagram on power up sequence below.
2. Set IO_NCS_A1 pin high. Set SHTDWN pin low. Set IO_SELECT pin high.
3. Perform reset by driving NRST low then high OR by writing 0x5A to address 0x3A.
4. Read Product ID (PID) to ensure sensor is powered up and communicating properly with host.
5. Write 0xE4 to address 0x60
6. Write 0xC9 to address 0x61

For TWI:

1. Apply power. Refer timing diagram on power up sequence below.
2. Set SHTDWN and IO_SELECT pin low.
3. Set A0 and A1 according to the desired TWI slave address (from TWI slave address table in datasheet).
4. Drive NRST pin low then high. TWI slave address will only be valid and according to the address set in step 3 after a NRST toggle is applied.
5. Read Product ID (PID) to ensure sensor is powered up and communicating properly with host.
6. Write 0xE4 to address 0x60
7. Write 0xC9 to address 0x61



Note: Not to scale

Note on register settings

Please refer to the OFN A350 firmware design guide for tuning of Speed Switching, Assert/De-assert, Finger Presence Detect and XY Quantization register settings.

Notes on Shutdown and Reset

The ADBM-A350 can be set in Shutdown mode by asserting or setting SHTDWN pin high. During the shutdown state, supply voltages VDD must be maintained above the minimum level. If these conditions are not met, then the sensor must be restarted by powering down then powering up again for proper operation. Any register settings must then be reloaded.

During the shutdown state, supply voltage VDD must be maintained above the minimum level. For proper operation, SHTDWN pulse width must be at least $t_{P\text{-}SHTDWN}$. Shorter pulse widths may cause the chip to enter an undefined state. In addition, the SPI or TWI port of the sensor should not be accessed when SHTDWN is asserted. Other devices on the same SPI bus can be accessed, as long as the sensor's NCS pin is not asserted. The table below shows the state of various pins during shutdown. After deasserting SHTDWN, wait t_{WAKEUP} before accessing the SPI port. Reinitializing the sensor from shutdown state will retain all register data that were written to the sensor prior to shutdown.

The reset of the sensor via SOFT_RESET register or through the NRST pin would reset all registers to the default value. Any register settings must then be reloaded.

Pin	SHTDWN active
IO_NCS_A1	Functional
IO_MISO_SDA	Undefined
IO_CLK	Undefined
IO_MOSI_A0	Undefined
XY_LED	Low current
EVENT_INT	Undefined
NRST	High
IO_Select	SPI: High, TWI: Low
GPIO	Undefined

Note: There are long wakeup times from shutdown. These features should not be used for power management during normal sensor motion.

Power on Reset (POR) During Power Cycling

t_{VRT} is the power supply (VDD) rise time specification for a valid power on reset to happen when the sensor is powered up from 0V to VDD. At condition whereby the VDD of the sensor is cycled from VDD to 0 V and then to VDD again, the two parameters that govern a valid power on reset are v_{OFF} and t_{OFF}. Refer to timing diagram below.

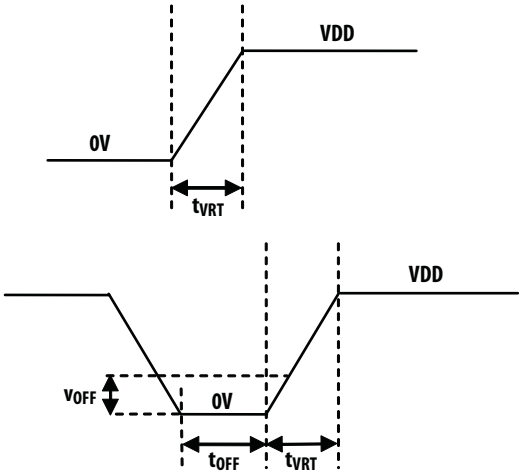


Figure 3. Power on Reset during power cycling

Power management modes

The ADBM-A350 has three power-saving modes. Each mode has a different motion detection period, affecting response time to sensor motion (Response Time). The sensor automatically changes to the appropriate mode, depending on the time since the last reported motion (Downshift Time). The parameters of each mode are shown in the following table.

Mode	Response Time (nominal)	Downshift Time (nominal)
Rest 1	19.5 ms	250 ms
Rest 2	96 ms	9.5 s
Rest 3	482 ms	582 s

EVENT_INT Pin

The Event_Int pin is a level-sensitive interrupt output that is used to trigger the host micro-controller when one of these events occurs:

- FPD – A change in finger state (finger on to finger off and vice versa) is detected
- Soft Click – Soft Click is detected
- Button – Mechanical button is asserted or de-asserted
- Motion – Motion delta is present.

A read to event register is required to determine the specific event that toggles the interrupt for user to act upon.

The EVENT_INT will be reset after the user responds to it by reading the respective event status register:

- FPD – reading FPD_STATUS register (0x7a)
- Soft Click – reading SC_STATUS register (0x7f)
- Button – reading BUTTON_STATUS register (0x12)
- Motion – reading DELTA_X and DELTA_Y registers until motion are cleared.

GPIO Pin

The GPIO pin is a level-sensitive input/ output that can be used as

- FPD output – to display FPD status
- Pulse Width Modulated (PWM) output – to control LED driver to enable illumination feature in a product eg mobile phone
- Dome/ Button click input – can be connected to a dome switch that provides an input to the sensor and when a click is detected, sensor can respond by triggering button interrupt and channel the interrupt status through EVENT pin.

Refer to A350 Firmware Design Guide for more details and settings of registers for these features.

LED Mode

For power savings, the LED will not be continuously on. ADBM-A350 will flash the LED only when needed.

I/O Pin Status Test

This feature allows the user to verify the connectivity and the state of the I/O pin.

To run the test for input pins such as GPIO, SHUTDOWN, NRST and IO_SELECT, first enable the PAD_Chk_On bit (or bit-1) of OFN_ENGINE2 (0x61) register. Then write any value to PAD_STATUS (0x31) register to start the test. Wait for approximately 12us before reading the actual pin status and PAD_STATUS register. The test will be considered a PASS to indicate the sensor is responding accordingly if the actual pin status matches PAD_STATUS register content. Refer to the table below for I/O pin status definition.

For output pins (EVENT_INT, GPIO, MOSI and MISO) testing, first enable bit-4 of PAD_FUNCTION (0x34) register. Then program or set the output state via PAD_TEST_OUT register (0x33) and do a READ on the actual pin status. Actual pin status results should match the output set in PAD_TEST_OUT. (Note: SPI/TWI communication will be disabled after this test is enabled. Once this test is completed, an external hardware reset on sensor is required)

Bit(s)	Name	Reset	Description	Remarks
7:6	NRST_STATE	0x0	0x0: unknown	
			0x1: Low	Invalid as the chip will be in reset state.
			0x2: High	
			0x3: Hi-Z	Indicate a floating high
5:4	SHUTDOWN_STATE	0x0	0x0: unknown	
			0x1: Low	
			0x2: High	Invalid as the chip will be in shutdown state.
			0x3: Hi-Z	Indicate a floating low
3:2	GPIO_STATE	0x0	0x0: unknown	
			0x1: Low	
			0x2: High	
			0x3: Hi-Z	
1:0	IO_SELECT_STATE	0x0	0x0: unknown	
			0x1: Low	
			0x2: High	
			0x3: Hi-Z	

Fast Video Dump

ADBS-A350 comes with a unique feature that enables user to capture the image the optical sensor is seeing on the tracking surface. This is achieved through storing the pixel data, transferring or dumping the pixels data out to the host for processing and rebuilding the video dump image. The rebuilding of video dump image is mainly converting each 8-bit pixel data to form a grayscale digital image.

Some useful applications for this feature are sensor contamination inspection at manufacturing lines, image recognition, motion sensing applications and etc.

Fast Video Dump Setups and Commands

Fast Video Dump (FVD) in the sensor requires three main signal lines for communications with host MCU as shown below.

Pin	Status	Description
GPIO	Input	24MHz clock signal
MISO_SDA	Output	Pixel data bits 7 to 4
EVENT_INT	Output	Pixel data bits 3 to 0

Connect an external clock signal of up to 24MHz to GPIO pin. Execute the FVD commands below and capture the 64burst cycles of data clocked out on the two output pins (MISO_SDA and EVENT_INT).

FVD Commands

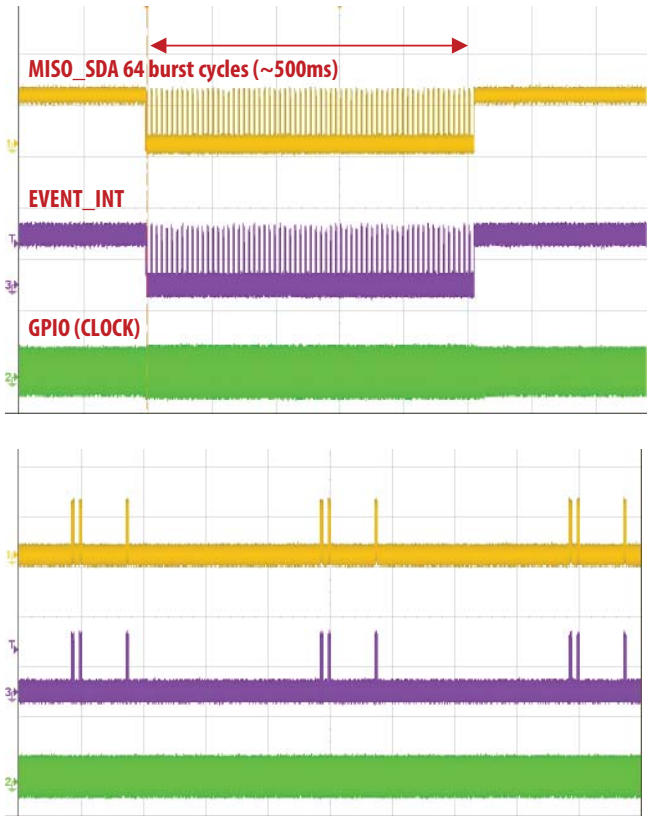
1. Power up sensor
2. Read register 0x00, to get returned value of 0x88 for correct product ID (ensure communication with sensor is established)
3. Write register 0x3a with 0x5a
4. Write register 0x11 with 0x53
5. Write register 0x30 with 0x13
6. Write register 0x2b with 0x30
7. Write register 0x2c with 0x13
8. Write register 0x28 with 0x01 to initiate video dump.
9. Sensor will start to video dump for about 500ms (see timing diagram on signals decoding versus actual signal captured).
10. Once video dump is completed, write register 0x3a with 0x5a to soft reset sensor back to normal operation.

    (Note: During FVD, the sensor is in 3-wire SPI communication with host MCU by design. Therefore a soft reset is necessary to reset back to 4-wire SPI communication for normal operation or to perform another FVD)
11. To capture another 64 burst cycles, repeat Step 2- Step10.

Video Dump Signals Capturing and Decoding

64 burst cycles of FVD will be present on the MISO_SDA and EVENT_INT pins after executing the fast video dump commands.

Zooming into each burst cycle, 3 frames in each burst cycle will be observed.



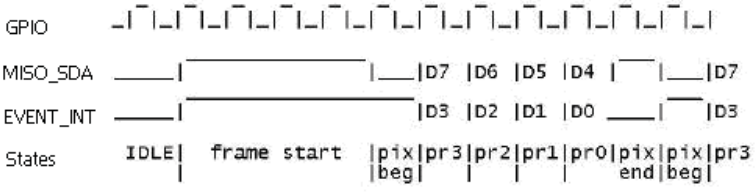


Figure 4. Signals for frame start

As shown in Figure 4 above, frame start of video dump is denoted by MISO_SDA pin and EVENT_INT pin clocking high for 4 clock cycles or 4 x b'11 (binary 11). Then after 4 clock cycles, MISO_SDA pin will go low and EVENT_INT pin remains high. This indicates pixel begin state.

The pixel read data will start to clock thereafter. Subsequent 4 bits are D7-D4 (on MISO_SDA) and D3-D0 (on EVENT_INT) followed by b'10 for pixel end (b'1 in MISO_SDA, b'0 in EVENT_INT). This completes the first pixel data (address 0). The next pixel data (address 1) will begin with pixel begin state (b'01- 0 in MISO_SDA, 1 in EVENT_INT) header followed by the 4 clock cycles of data followed by a pixel end state in the same manner. This will continue until all the 361 pixels (19x19 pixel array) data is read. Once done, the pixel end of the pixel data (address 360) will be followed by frame end state (b'00 – 0 in MISO_SDA, 0 in EVENT_INT). Refer to Figure 5.

Below is the pixel array address map. The figure shows the view of the chip from the top of the OFN aperture. Rows are read from top to bottom and columns from left to right.

Pin 1

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75
76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94
95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113
114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132
133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151
152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170
171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189
190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208
209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227
228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246
247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265
266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284
285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303
304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322
323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341
342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360

Pin 18

The signal to indicate the end of the video dump frame is shown in Figure 5 below where pix end state is followed by a low in both MISO_SDA and EVENT_INT. This will inform the Host of the pixel end and frame end state.

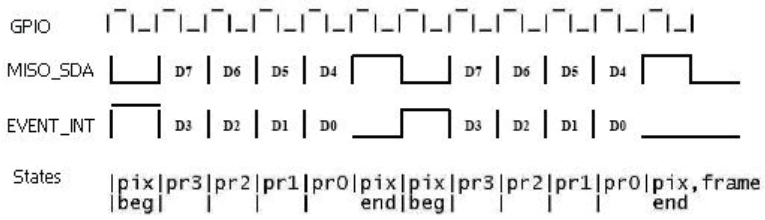
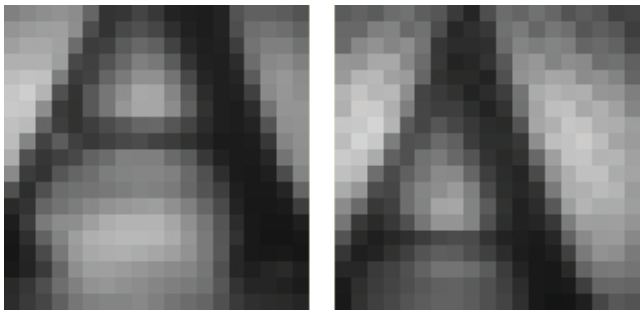


Figure 5. Frame End

Note: It is advisable to have a counter at the Host to keep count of the number of pixel addresses and data byte. If the number of pixel data byte does not correspond to the sensor number of pixel then this video dump data is invalid. In this case the sensor must be reset and a new video dump must be initiated.

Fast Video Dump Image

These are some examples of grayscale images captured using fast video dump on an object 'A' (size of 1mmx1mm) at the surface of the sensor that is converted from the fast video dump data.



4-wire Serial Peripheral Interface (SPI)

SPI Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25° C, VDD = 1.8 V.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Serial Port Clock Frequency	f_{sclk}			1	MHz	Active drive, 50% duty cycle
MISO rise time	$t_{r\text{-}MISO}$		150	300	ns	C_L = 100 pF
MISO fall time	$t_{f\text{-}MISO}$		150	300	ns	C_L = 100 pF
MISO delay after SCLK	t_{DLY_MISO}			120	ns	From SCLK falling edge to MISO data valid, no load conditions
MISO hold time	t_{hold_MISO}	0.5		$1/f_{SCLK}$	µs	Data held until next falling SCLK edge
MOSI hold time	t_{hold_MOSI}	200			ns	Amount of time data is valid after SCLK rising edge
MOSI setup time	t_{setup_MOSI}	120			ns	From data valid to SCLK rising edge
SPI time between write commands	t_{SWW}	30			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI time between write and read commands	t_{SWR}	20			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte.
SPI time between read and subsequent commands	t_{SRW} t_{SRR}	500			ns	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command.
SPI read address-data delay	t_{SRAD}	4			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read.
NCS inactive after motion burst	t_{BEXIT}	500			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS to SCLK active	$t_{NCS\text{-}SCLK}$	120			ns	From NCS falling edge to first SCLK falling edge
SCLK to NCS inactive (for read operation)	$t_{SCLK\text{-}NCS}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer
SCLK to NCS inactive (for write operation)	$t_{SCLK\text{-}NCS}$	20			us	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer
NCS to MISO high-Z	$t_{NCS\text{-}MISO}$			500	ns	From NCS rising edge to MISO high-Z state

Synchronous Serial Port

The synchronous serial port is used to set and read parameters in the ADBM-A350, and to read out the motion information.

The port is a four wire serial port. The host micro-controller always initiates communication; the ADBM-A350 never initiates data transfers. SCLK, MOSI, and NCS may be driven directly by a micro-controller. The port pins may be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored and the output is tri-stated.

The lines that comprise the 4-wire SPI port:

SCLK: Clock input. It is always generated by the master (the micro-controller).

MOSI: Input data. (Master Out/Slave In)

MISO: Output data. (Master In/Slave Out)

NCS: Chip select input (active low). NCS needs to be low to activate the serial port; otherwise, MISO will be high Z, and MOSI & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. This is true for all transactions. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction. To improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because ESD events could be interpreted as serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.

Write Operation

Write operation, defined as data going from the micro-controller to the ADBM-A350, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The ADBM-A350 reads MOSI on rising edges of SCLK.

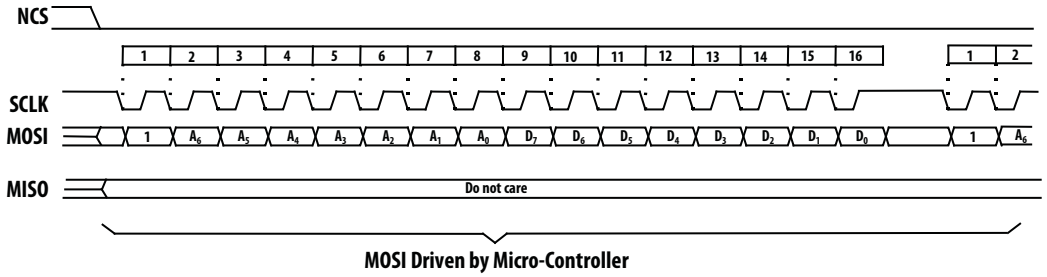


Figure 6. Write Operation

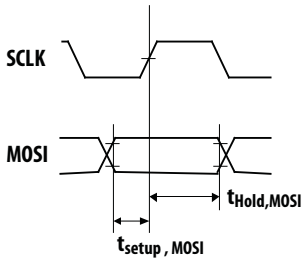


Figure 7. MOSI Setup and Hold Time

Read Operation

A read operation, defined as data going from the ADBM-A350 to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is sent by the micro-controller over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the ADBM-A350 over MISO. The sensor outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.

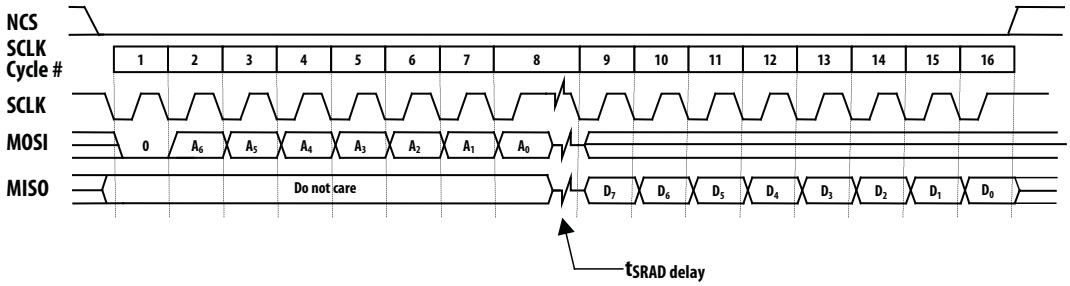
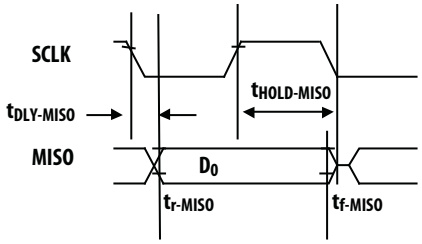


Figure 8. Read Operation



NOTE: The $0.5/f_{SCLK}$ minimum high state of SCLK is also the minimum MISO data hold time of the ADBM-A350. Since the falling edge of SCLK is actually the start of the next read or write command, the ADBM-A350 will hold the state of data on MISO until the falling edge of SCLK.

Figure 9. MISO Delay and Hold Time

Required timing between Read and Write Commands

There are minimum timing requirements between read and write commands on the serial port.

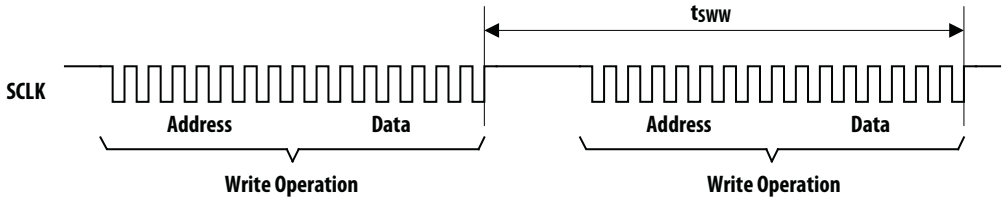


Figure 10. Timing between two write commands

If the rising edge of the SCLK for the last data bit of the second write command occurs before the required delay (t_{SWW}), then the first write command may not complete correctly.

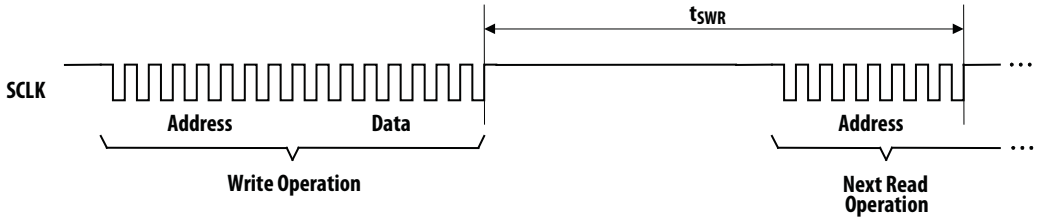


Figure 11. Timing between write and read commands

If the rising edge of SCLK for the last address bit of the read command occurs before the required delay (t_{SWR}), the write command may not complete correctly.

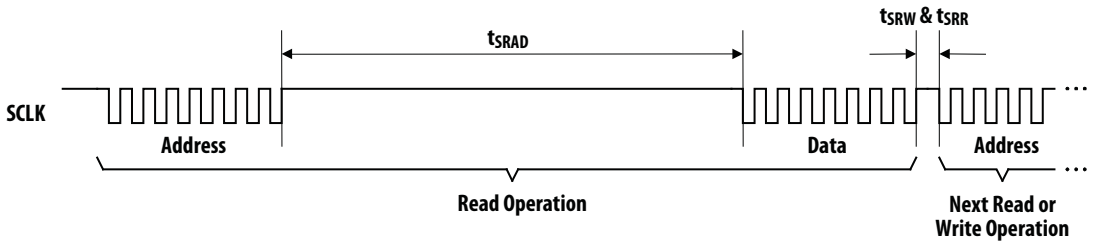


Figure 12. Timing between read and either write or subsequent read commands

During a read operation SCLK should be delayed at least t_{SRAD} after the last address data bit to ensure that the ADBM-A350 has time to prepare the requested data. The falling edge of SCLK for the first address bit of either the read or write command must be at least t_{SRR} or t_{SRW} after the last SCLK rising edge of the last data bit of the previous read operation.

Burst Mode Operation

Burst mode is a special serial port operation mode that may be used to reduce the serial transaction time for a motion read. The speed improvement is achieved by continuous data clocking from multiple registers without the need to specify the register address, and by not requiring the normal delay period between data bytes.

Burst mode is activated by writing 0x10 to register 0x1c IO_MODE. Then the burst mode data can be read by reading the Motion register 0x02. The ADBM-A350 will respond with the contents of the Motion, Delta_Y, Delta_X, SQUAL, Shutter_Upper, Shutter_Lower and Maximum_ Pixel registers in that order. The burst transaction can be terminated after the first 3 bytes of the sequence are read by bringing the NCS pin high. After sending the register address, the micro-controller must wait t_{SRAD} and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data is latched into the output buffer after the last address bit is received. After the burst transmission is complete, the micro-controller must raise the NCS line for at least t_{BEXIT} to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

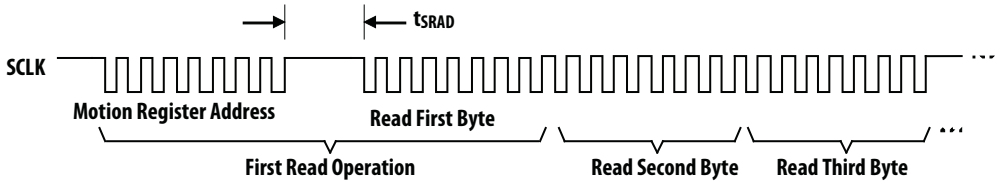


Figure 13. Motion Burst Timing

Two – Wire Interface (TWI)

ADBM-A350 uses a two-wire serial control interface compatible with I2C. The parameters are listed below.

TWI Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25° C, VDD = 1.8 V.

Parameter	Symbol	Minimum	Maximum	Units	Notes
SCL clock frequency	fscl		400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	t_{HD_STA}	0.6	–	µs	
LOW period of the SCL clock	t_{LOW}	1.0	–	µs	
HIGH period of the SCL clock	t_{HIGH}	0.6	–	µs	
Set up time for a repeated START condition	t_{SU_STA}	0.6	–	µs	
Data hold time	t_{HD_DAT}	0(2)	0.9(3)	µs	
Data set-up time	t_{SU_DAT}	100	–	ns	
Rise time of both SDA and SCL signals	t_r	$20+0.1C_b$(4)	300	ns	
Fall time of both SDA and SCL signals	t_f	$20+0.1C_b$(4)	300	ns	
Set up time for STOP condition	t_{SU_STO}	0.6	–	µs	
Bus free time between a STOP and START condition	t_{BUF}	1.3	–	µs	
Capacitive load for each bus line	C_b	–	400	pF	
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 VDD	–	V	
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 VDD		V	

Notes:
1. All values referred to V_{IHMIN} and V_{ILMAX} levels.
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum has t_{HD_DAT} only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. C_B = total capacitance of one bus line in pF.

The ADBM-A350 responds to one of the following selectable slave device addresses depending on the IO_MOSI_A0 and IO_NCS_A1 input pin state. These pins should be set to avoid conflict with any other devices that might be sharing the bus.

Table 1. TWI slave address

A0	A1	Slave Address (Hex)
0	0	33
0	1	3b
1	0	53
1	1	57

Serial Transfer Clock and Serial Data signals

The serial control interface uses two signals: a serial transfer clock (SCL) signal and a serial data (SDA) signal. Always driven by the master, SCL synchronizes the serial transmission of data bits on SDA. The frequency of SCL may vary throughout a transfer, as long as the timing is greater than the minimum timing.

SDA is bi-directional. The host (master) can read from or write to the ADBM-A350. The host (typically a microcontroller) drives SCL and SDA in a write operation or requesting information from the ADBM-A350. The ADBM-A350 drives the SDA only under two conditions. First, when responding with an acknowledge (ACK) bit after receiving data from the host, or second, when sending data to the host at the host's request. Data is sent in Eight-bit packets.

Start and Stop of Synchronous Operation

The host initiates and terminates all data transfers. Data transfers are initiated by driving SDA from high to low while holding SCL high. Data transfers are terminated by driving SDA from low to high while SCL is held high.

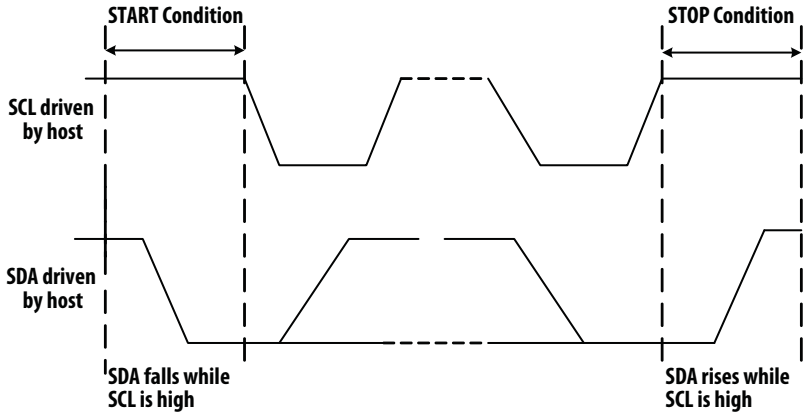


Figure 14. TWI Start and Stop operation

Acknowledge/Not Acknowledge Bit

After a start condition, a single acknowledge/not acknowledge bit follows each Eight-bit data packet. The device receiving the data drives the acknowledge/not acknowledge signal on SDA. Acknowledge (ACK) is defined as 0 and not acknowledge (NAK) is defined as 1.

Packet Formats

Read and write operations between the host and the ADBM-A350 use three types of host driven packets and one type of ADBM-A350 driven packet. All packets are eight bits long with the most significant bit first, followed by an acknowledge bit.

Slave Device Address (DA)

Command packets contain a 7-bit ADBM-A350 device address and an active low read/write bit (R/W).

First bit of packet							Last bit of packet
Device Address							R/$\overline{W}$
DA[6]	DA[5]	DA[4]	DA[3]	DA[2]	DA[1]	DA[0]	Write = 0 Read = 1

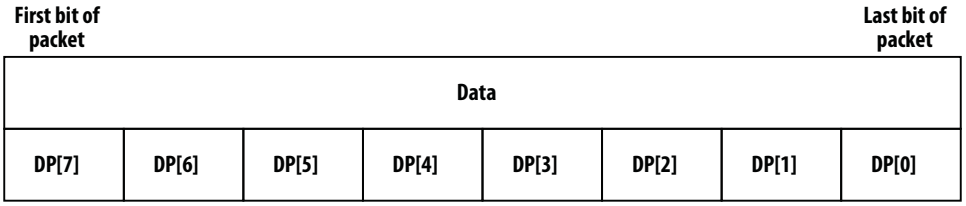
Register Address Packets (RA)

The address packets contain an auto-increment (ai) bit and a 7-bit address. If the 'ai' bit is set, the slave will process data from successive addresses in successive bytes. For example, registers 0x01, 0x02, and 0x03 can be written by setting the 'ai' bit to one with address 0x01. The host would send three bytes of data, and the host would terminate with a P condition.

First bit of packet							Last bit of packet
Auto increment	Register Address						
Auto increment=1, No increment=0	RA[6]	RA[5]	RA[4]	RA[3]	RA[2]	RA[1]	RA[0]

Data Packet (DP)

Contains 8 data bits and may be sent by the host or the ADBM-A350.



Host Driven Packets

The host initiates all data transmission with a START condition. Next, slave address and register address packets are sent. If there is a device address match, the ADBM-A350 then responds to each Eight-bit data transmission with an acknowledge signal (SDA = 0). Data is transmitted with the most significant bit first.

To terminate the transfer of host driven packets, the host follows the ADBM-A350's ACK with a STOP condition. The host can also issue a START condition after the ADBM-A350's ACK if it wants to start a new data transfer.

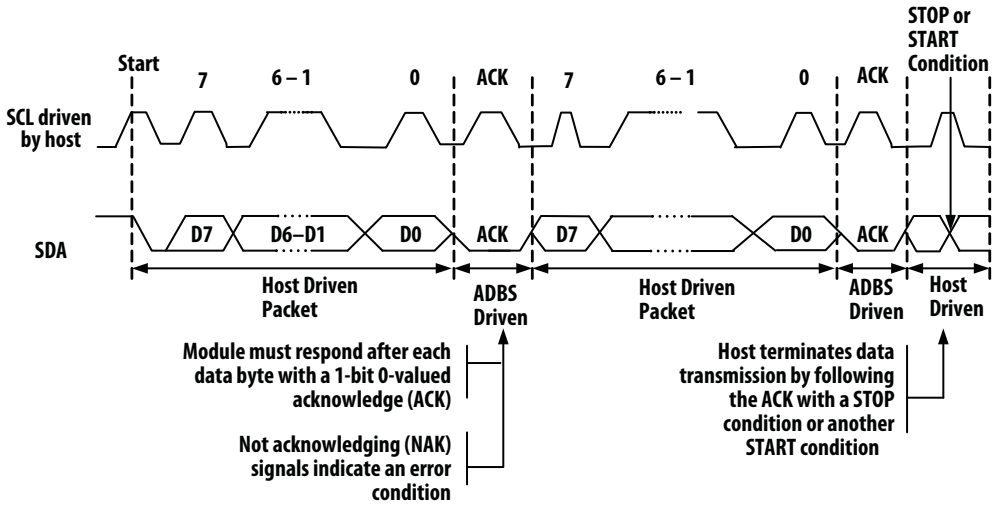


Figure 15. Host packets

ADBM-A350 Driven Packets

By request of the host, the ADBM-A350 acknowledges a read request and then outputs a data byte transmitting the most significant bit (7) first. If the host intends to continue the data transfer, the host acknowledges the ADBM-A350. If the host intends to terminate the transfer, it responds with not acknowledge (SDA = 1), and then drives SDA to generate a STOP condition. The host can also drive a START condition if it wants to begin a new data transfer with the same ADBM-A350.

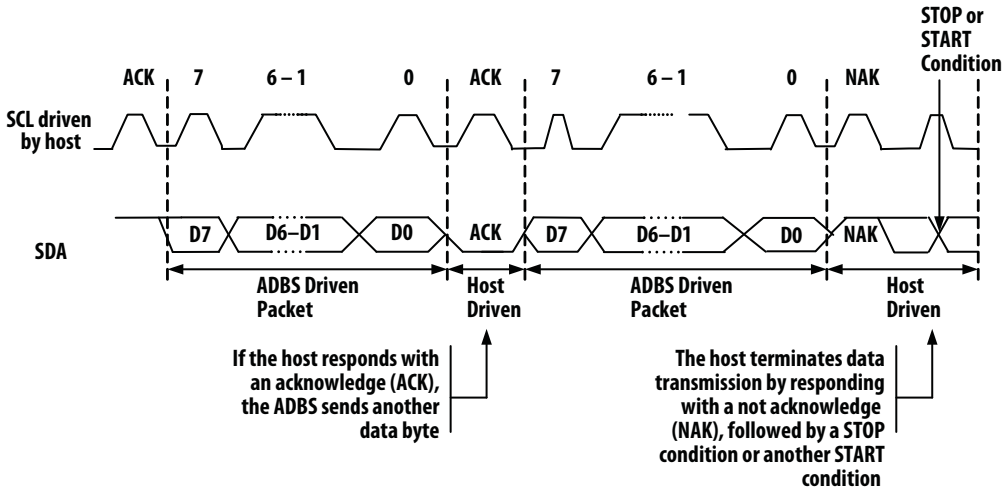


Figure 16. Sensor packets

Example: Writing Data to Sensor Registers

The host writes a value of 0x02 to address 0x07 in the following illustration.

The example ADBM-A350 address is 0x57.

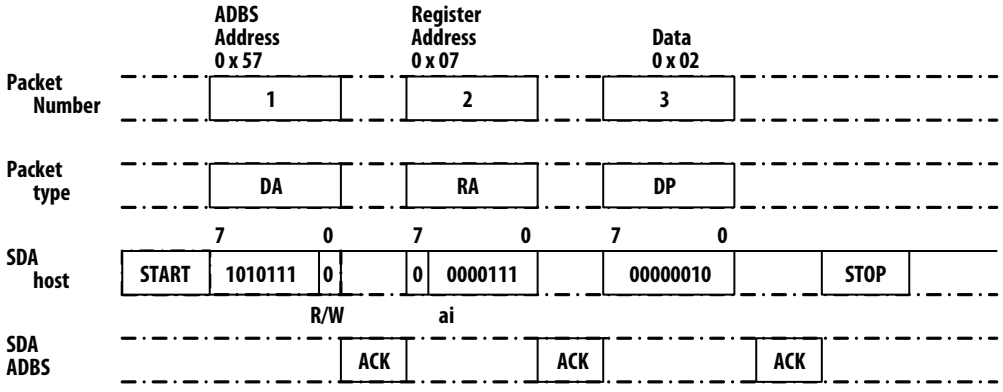


Figure 17. TWI write

Example: Single Byte Read from Sensor Register

The sensor reads a value 0x01from the register address 0x02 in the following illustration. Again, the example ADBM-A350 address is 0x57.

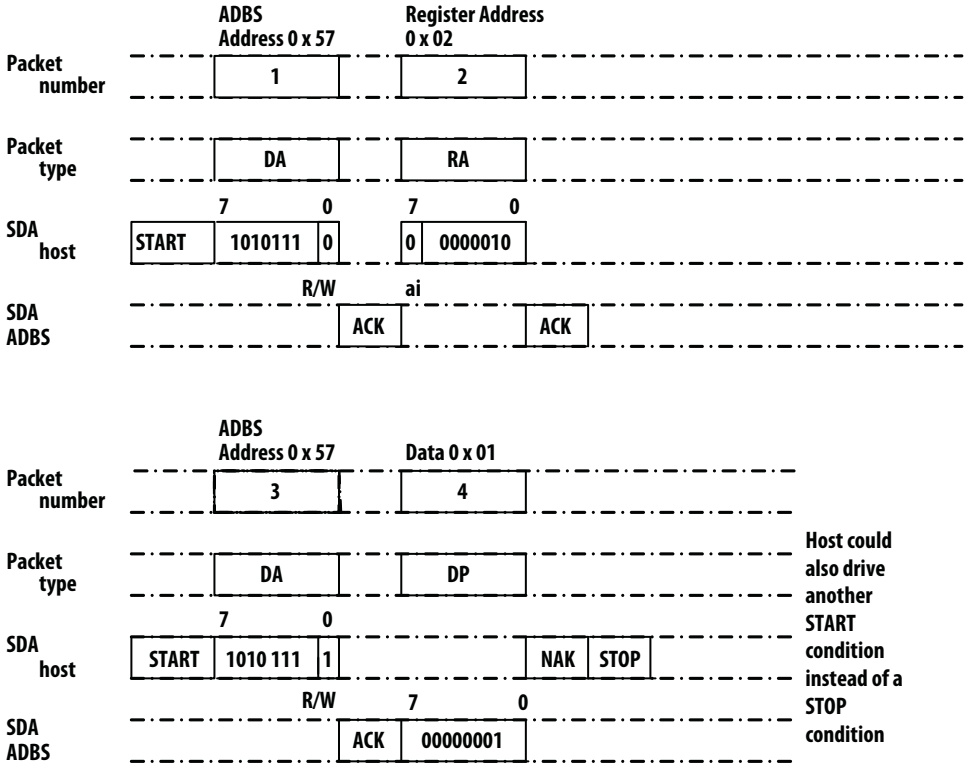


Figure 18. TWI single byte read

Example: Polling of Status register (X-Y Motion Bit and Button bits)

To poll the STATUS register, the following structure can be used:

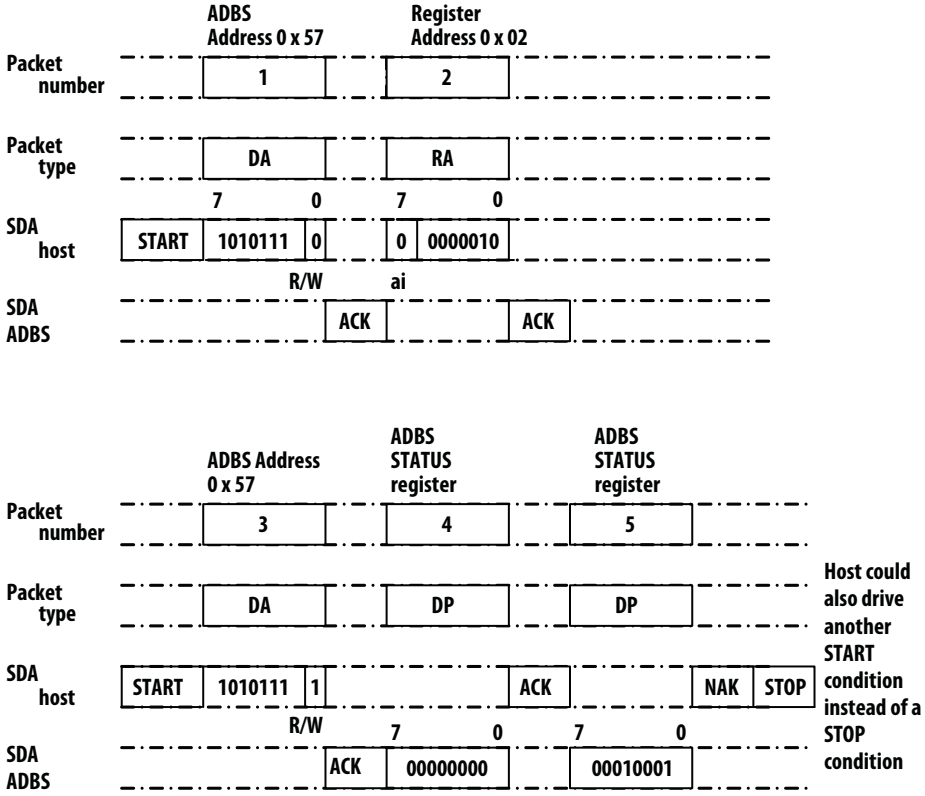


Figure 19. TWI polling

In this case, the host read ADBM-A350 data packets until the update bit (bit 4). Then the host could read successive registers using the ai bit example below.

Note: polling the Status register rather than using the DATA_RDY pin increases power consumption

Example: Multiple-Byte Read from Sensor Register using 'ai' bit

The ai is a useful feature, especially in the case of reading Delta_X, Delta_Y, and Delta_HI in succession once either the DATA_RDY interrupt pin and/or update bit in the STATUS register bit are set.

Once the ai bit is set, the slave will deliver data packets from successive addresses until the 'STOP' condition from the host.

In the example below, 3 bytes are read successively from registers 0x03, 0x04, and 0x05.

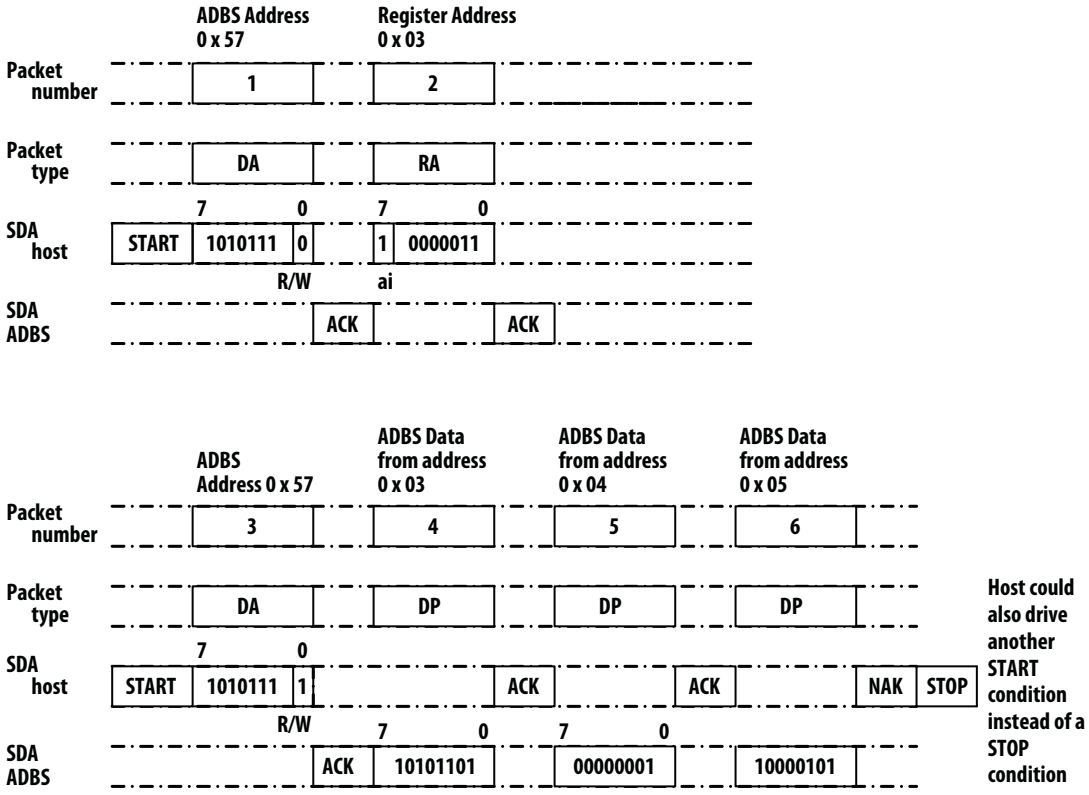


Figure 20. TWI ai bit

SCL and SDA Timing

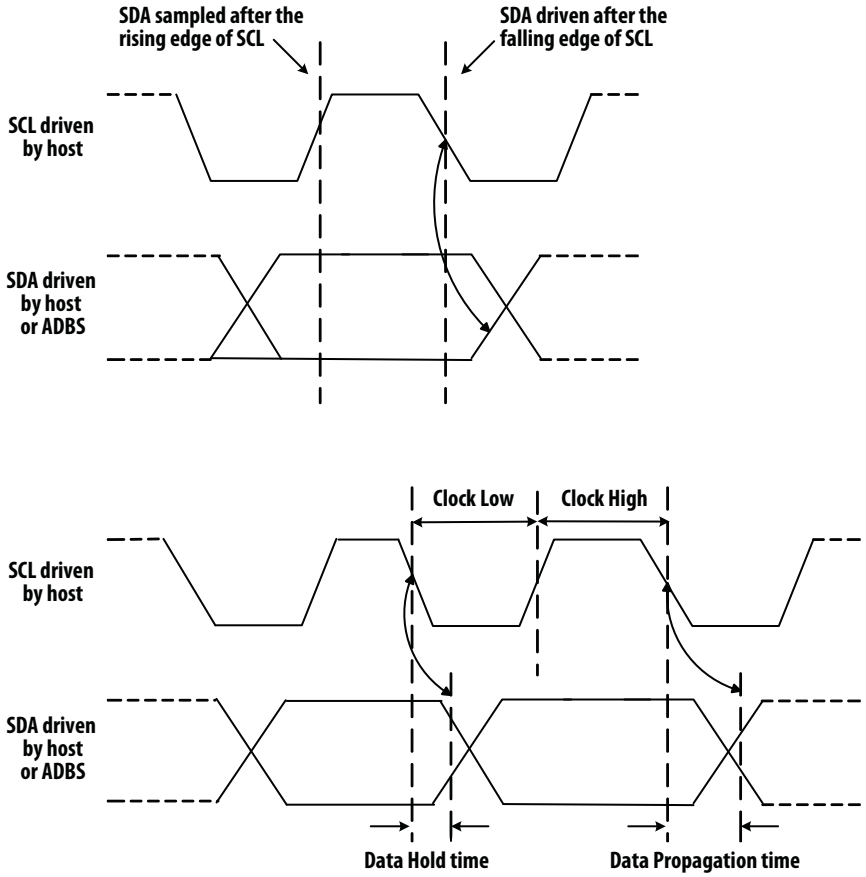


Figure 21. TWI SCL and SDA Timing

ADBM-A350 driven SDA

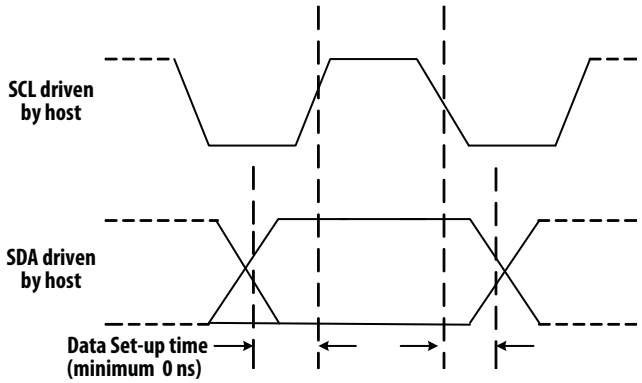


Figure 22. Sensor driven SDA

Registers

The ADBM-A350 registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Address	Register	Read/ Write	Default Value	Address	Register	Read/ Write	Default Value
0x00	Product_ID	R	0x88	0x40-0x5f	Reserved		
0x01	Revision_ID	R	0x00	0x60	OFN_Engine1	R/W	0x84
0x02	EVENT	R/W	Any	0x61	OFN_Engine2	R/W	0x89
0x03	Delta_X	R	Any	0x62	Resolution	R/W	0x22
0x04	Delta_Y	R	Any	0x63	Speed_Ctrl	R/W	0x0e
0x05	SQUAL	R	Any	0x64	Speed_ST12	R/W	0x08
0x06	Shutter_Upper	R	Any	0x65	Speed_ST21	R/W	0x06
0x07	Shutter_Lower	R	Any	0x66	Speed_ST23	R/W	0x40
0x08	Maximum_Pixel	R	Any	0x67	Speed_ST32	R/W	0x08
0x09	Pixel_Sum	R	Any	0x68	Speed_ST34	R/W	0x48
0x0a	Minimum_Pixel	R	Any	0x69	Speed_ST43	R/W	0x0a
0x0b	Pixel_Grab	R/W	Any	0x6a	Speed_ST45	R/W	0x50
0x0c	CRC0	R	0x00	0x6b	Speed_ST54	R/W	0x48
0x0d	CRC1	R	0x00	0x6c	GPIO_CTRL	R/W	0x80
0x0e	CRC2	R	0x00	0x6d	AD_CTRL	R/W	0xc4
0x0f	CRC3	R	0x00	0x6e	AD_ATH_HIGH	R/W	0x3a
0x10	Self_Test	W	0x00	0x6f	AD_DTH_HIGH	R/W	0x40
0x11	Reserved			0x70	AD_ATH_LOW	R/W	0x35
0x12	BUTTON_STATUS	R/W	0x00	0x71	AD_DTH_LOW	R/W	0x3b
0x13	Run_Downshift	R/W	0x04	0x72	QUANTIZE_CTRL	R/W	0x99
0x14	Rest1_Period	R/W	0x01	0x73	XYQ_THRESH	R/W	0x02
0x15	Rest1_Downshift	R/W	0x1f	0x74	MOTION_CTRL	R/W	0x00
0x16	Rest2_Period	R/W	0x09	0x75	FPD_CTRL	R/W	0xfa
0x17	Rest2_Downshift	R/W	0x2f	0x76	FPD_THRESH	R/W	0x2c
0x18	Rest3_Period	R/W	0x31	0x77	ORIENT_CTRL	R/W	0x00
0x19	Reserved			0x78	FPD_SQUAL_THRESH	R/W	0x40
0x1a	LED_CTRL	R/W	0x00	0x79	FPD_VALUE	R/W	0x00
0x1b	Reserved			0x7a	FPD_STATUS	R	0x20
0x1c	IO_Mode	R/W	0x00	0x7b	SC_CTRL	R/W	0x25
0x1d	EVENT_CTRL	R/W	0x04	0x7c	SC_T_TAPNHOLD	R/W	0x45
0x28	Fast_Video_Dump	R/W	0x00	0x7d	SC_T_DOUBLE	R/W	0x1e
0x2e	Observation	R/W	Any	0x7e	SC_DELTA_THRESH	R/W	0x19
0x31	Pad_Status	R	0x00	0x7f	SC_STATUS	R/W	0x00
0x32	Reserved						
0x33	Pad_Test_Out	RW	0x00				
0x34	Pad_Function	W	0x00				
0x3a	SOFT_RESET	W	0x00				
0x3b	Shutter_Max_Hi	R/W	0x0b				
0x3c	Shutter_Max_Lo	R/W	0x71				
0x3d	Reserved						
0x3e	Inverse_Revision_ID	R	0xFF				
0x3f	Inverse_Product_ID	R	0x77				